Simulation of a Regular Sampled Pulsewidth Modulation (PWM) Technique for a Multilevel Inverter

M. S. Bakar and N. A. Azli

Abstract--**Simulation of a multilevel inverter for high power applications employing a PWM unipolar symmetrical regular sampled technique based on a single carrier multilevel modulation strategy is presented in this paper. The equations related to this technique are used to design the gate signal generator blocks using Matlab's Simulink. These blocks generate the gate signals for each of the multilevel inverter power devices and can later be compiled and downloaded to a dSPACE DSP controller board for real time digital implementation. The gate signal generator blocks are tested for various values of modulation index. The results of the simulation study are shown in the form of the PWM waveforms of the multilevel inverter modules as well as the gate signals for its power devices for comparison purposes.**

***Keywords*--Inverter, multilevel, PWM, regular sampled, simulation**

I. Introduction

THE multilevel inverter topology has gained increasing attention in recent years particularly in applications involving high voltage and power. This is mostly due to the limitations of the conventional two-level output inverters in handling high power conversion. The main feature of a multilevel inverter is its ability to reduce the voltage stress on each power device due to the utilization of multiple levels on the DC bus. This is especially important when a high DC side voltage is imposed by an application. There are several types of multilevel inverters but the one considered in this work is the modular structured multilevel inverter (MSMI).

Works that are based on the extension of the carrier-based subharmonic natural PWM strategy in traditional two-level output inverters to the multilevel inverters have been reported in literatures. In this case, the idea is to use several triangular carrier signals with only one modulating signal. Thus, this strategy is commonly known as the multicarrier modulation strategy. A single carrier multilevel modulation strategy has also been proposed as a basis to a regular sampled PWM strategy for the MSMI, with digital techniques such as a microprocessor or a digital signal processor (DSP) as its practical implementation method [1]. Further work on the regular sampled PWM strategy has been reported with the development of equations that represent the leading edges of the PWM pulses for the multilevel inverter and its implementation using a microcontroller [2].

This paper presents the results of a simulation study on a MSMI that utilizes the developed equations [2] in generating the gating signals for its power devices. The gate signal generation model based on these equations is designed and developed using Matlab's Simulink so that it can later be compiled and downloaded to a dSPACE DSP controller board for real time digital implementation. The gate signal generator model is tested for various values of modulation index. The results of the simulation study are shown in the form of the PWM waveforms of the multilevel inverter modules as well as the gate signals for its power devices, for comparison purposes.

II. Modular Structured Multilevel Inverter (MSMI)

A. Circuit Topology

Fig. 1 shows a single-phase 5-level configuration of the MSMI. The MSMI is unique when compared to other types of multilevel inverters in sense that it consists of several modules that require separate DC sources. Compared to other types of multilevel inverters, the MSMI requires less number of components with no extra clamping diodes or voltage balancing capacitors that only further complicate the overall inverter operation.

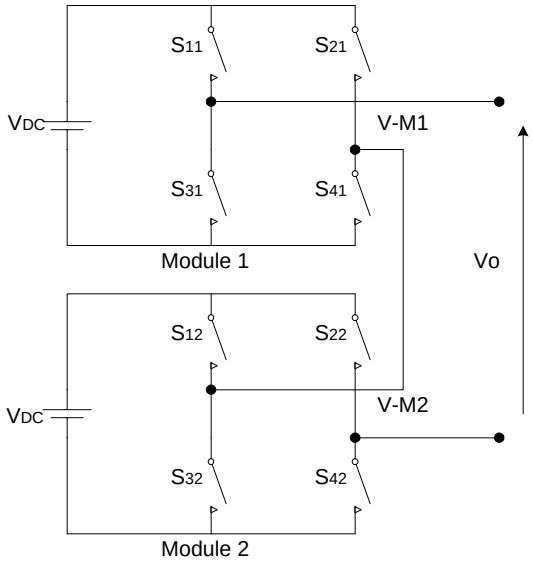

Fig. 1. Single-phase 5-level MSMI configuration

M. S. Bakar is with the Power System Department, Faculty of Electrical and Electronic Engineering Technology, University College of Engineering and Technology, 25000 Kuantan, Pahang, Malaysia (e-mail: shafie@kuktem.edu.my)

N. A. Azli is with the Energy Conversion Department, Faculty of Electrical Engineering, Universiti Teknologi Malaysia, 81310 UTM Skudai, Johor, Malaysia (e-mail: naziha@fke.utm.my).

As can be seen from Fig. 1, each module of the MSMI has the same structure where by it is represented by a single phase full-bridge inverter. This simple modular structure not only allows practically unlimited number of levels for the MSMI by stacking up the modules but also facilitates its packaging.

The operation of the MSMI can be easily understood where by the output phase voltage is equal to the summation of the output voltage of the respective modules that are connected in series. The number of modules (M) which is equal to the number of DC sources required depends on the number of levels (N) of the MSMI. It is usually assumed that N is odd as this would give an integer valued M which would simplify further analysis. As an example, for an output voltage consisting of five levels which include $+2V_{DC}$, $+V_{DC}$, 0 , $-V_{DC}$ and $-2V_{DC}$, the number of modules needed is 2. The following equation gives the relationship between N and M.

$$M = (N-1)/2 \quad (1)$$

B. PWM Unipolar Symmetrical Regular Sampled Technique

The PWM unipolar symmetrical regular sampled technique is developed [2] based on a single carrier multilevel modulation strategy. The main idea is to use one triangular carrier signal with two sampled sinusoidal modulation signals. The number of sampled sinusoidal modulation signals is equal to the number of modules in the MSMI. Both the sampled modulation signals and the single carrier signal are required to develop the switching angle equations. These switching angle equations are then used to obtain the rising edge time as presented by (2) and the falling edge time as given by (3), of the PWM pulses.

$$tneg(k) = \frac{Tc}{2Ac} + \left(\begin{array}{l} (2k-1)Ac + Bc - \\ Am\sin\left(\frac{2\Pi}{Tm}\left(k-\frac{1}{2}\right)Tc\right) - Bm \end{array} \right) \quad (2)$$

$$tpos(k) = (2k-1)Tc - tneg(k) \quad (3)$$

where;
tneg(k) is the rising edge time and represented as the timings of LOGIC 1.
tpos(k) is the falling edge time and represented as the timings of LOGIC 0.
k is the number of intersections of the carrier signal.
Tc is the period of the carrier signal.
Tm is the period of the sampled modulation signals.
Ac is the amplitude of the carrier signal.
Am is the amplitude of the sampled modulation signals.
Bm is the cross-point at Y-axis.
Bc is the cross-point at X-axis.

Based on (1) and (2) the design of the gate signal generator blocks using Matlab's Simulink is developed. In this case, the design is limited to a fixed frequency modulation ratio (mf) of 20, while the modulation index (mi) can be varied between 0 and 1.

III. DESIGN OF THE GATE SIGNAL GENERATOR

Basically, two main Simulink blocks are developed to represent the gate signal generator. The functions of these blocks are:

- To generate the timings of LOGIC 1 and the timings of LOGIC 0.
- To generate LOGIC 1 and LOGIC 0.

Fig. 2 shows the subsystem of the Simulink block developed to generate the timings of LOGIC 1 and the timings of LOGIC 0.

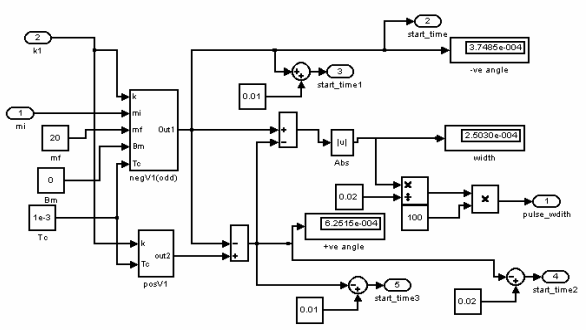

Fig. 2. Subsystem of the Simulink block to generate the timings of LOGIC 1 and LOGIC 0

Block *negV1(odd)* is used to generate the timings of LOGIC 1 while block *posV1* is used to generate the timings of LOGIC 0. Table 1 provides the related parameters that are utilized to obtain the timing values for mi = 0.4 and mi = 0.8.

TABLE 1
RELATED PARAMETERS TO GENERATE THE TIMINGS OF LOGIC 1 AND LOGIC 0.

mi	mf	Am	Bm	Modules
0.4	20	0.8	0	1
0.4	20	0.8	-1	2
0.8	20	1.6	0	1
0.8	20	1.6	-1	2

The time values obtained are for the first quarter cycle of the PWM waveforms. For the same value of k, the subsystem of the Simulink block as shown in Fig. 2, can be manipulated to generate the first half cycle of the PWM waveforms. Table 2 shows the relationships between the timings for ¼ cycle, ½ cycle, ¾ cycle and one complete cycle of the PWM waveforms.

TABLE 2
RELATIONSHIPS BETWEEN THE TIME VALUES OF THE PWM WAVEFORMS

tneg(k) [1/4 cycle]	tpos(k) [1/4 cycle]	tneg(k) [1/2 cycle]	tpos(k) [1/2 cycle]	tneg(k) [3/4 cycle]	tpos(k) [3/4 cycle]	tneg(k) [1 cycle]	tpos(k) [1 cycle]
A	B	0.01-A	0.01-B	0.01+A	0.01+B	0.02-A	0.02-B

where;
A = timings of LOGIC 1.
B = timings of LOGIC 0.

The pulsewidths obtained from the Simulink block of Fig. 2 become the input to the second Simulink block whose subsystem is shown in Fig. 3 developed to generate LOGIC 1 and LOGIC 0.

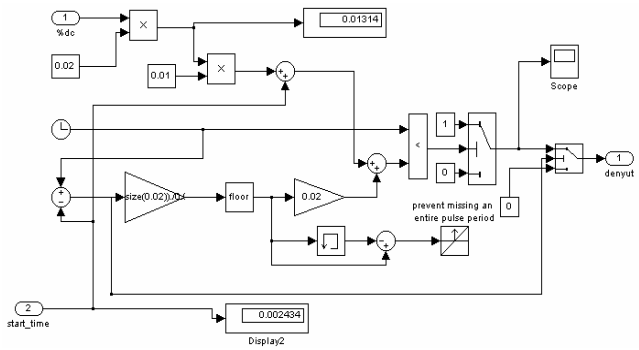

Fig. 3. Subsystem of the Simulink blocks to generate LOGIC 1 and LOGIC 0.

Using the *signal generator block* from Simulink's Library, suitable modifications are made to fulfill the simulation objective. The duty cycles of the pulsewidths obtained from the Simulink block of Fig. 2 are calculated. The value of the *start_time* in Fig. 2 is then compared with the value of *clock* in Fig. 3. The comparison will produce LOGIC 1 and LOGIC 0.

IV. SIMULATION RESULTS

Fig. 4 shows the overall simulation blocks used in the simulation study, in this case for mi=0.4 and mf=20, consisting of the gate signal generator and the MSMI.

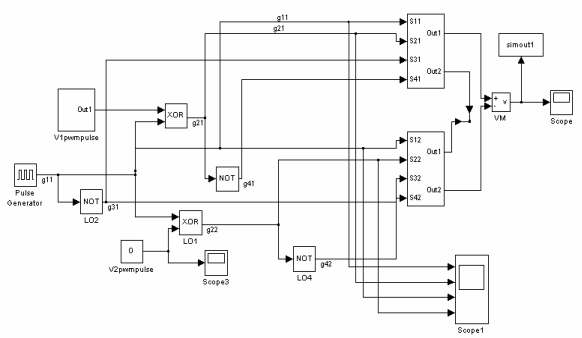

Fig. 4. Simulation blocks for mi=0.4 and mf=20

Fig. 5 shows the PWM waveforms obtained for the first and second MSMI module. Blocks *V1pwmpulse* and *V2pwmpulse* are the blocks that generate LOGIC 1 and LOGIC 0 respectively. For the second module, a constant zero value is used to represent the condition where by there are no intersections between the sampled modulation signals and the carrier signal.

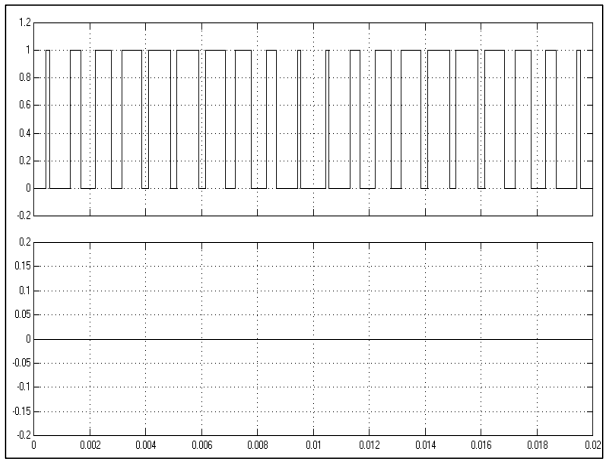

Fig. 5. PWM waveforms of the first (upper) and second (lower) modules of the MSMI for mi=0.4 and mf=20

Fig. 6 shows the gate signals generated when mi=0.4 and mf=20. The signals for the power devices S11, S12 and S22 are at the MSMI operating frequency of 50 Hz compared to the gate signal for S21 which is at a higher switching frequency.

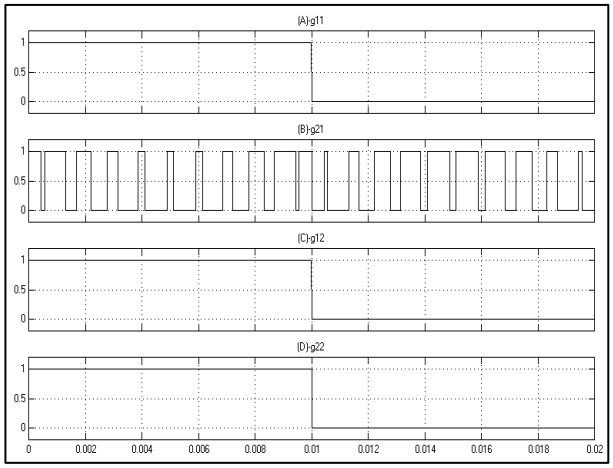

Fig. 6. Gate signals when mi=0.4 and mf=20.

Fig. 7 shows the overall simulation blocks for mi=0.8 and mf=20. In this case, blocks *1stmodule* and *2ndmodule* are the blocks that generate LOGIC 1 and LOGIC 0 respectively.

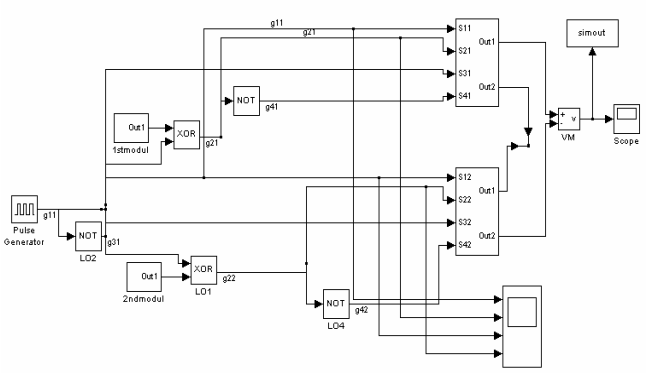

Fig. 7. Simulation blocks for mi=0.8 and mf=20.

Fig. 8 shows the PWM waveforms obtained for the first and second MSMI modules.

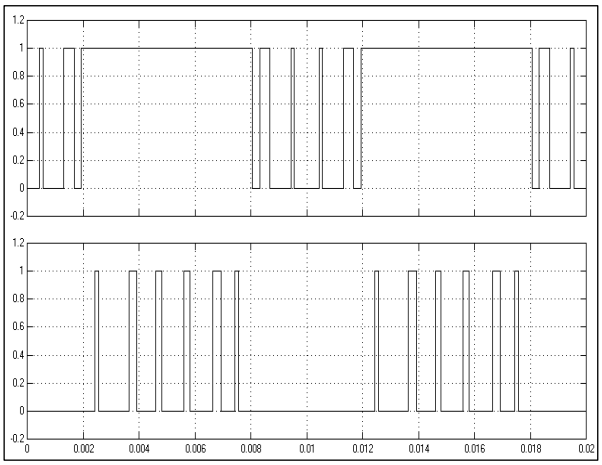

Fig. 8. PWM waveforms of the first (upper) and second (lower) modules of the MSMI for mi=0.8 and mf=20

Fig. 9 shows the gate signals generated when mi=0.8 and mf=20.

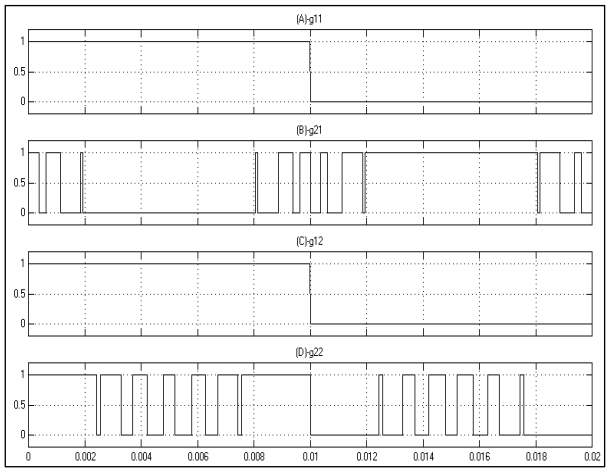

Fig. 9. Gate signals when mi=0.8 and mf=20.

The signals for the power devices S11 and S12 are at the MSMI operating frequency of 50 Hz while the gate signals for S21 and S22 are at a higher switching frequency. As almost half of the power devices are switching at low switching frequencies, the MSMI switching losses particularly in high power applications can further be reduced.

V. CONCLUSIONS

The unipolar symmetrical regular sampled technique [2] has been briefly described in terms of implementing the equations related to it using Matlab's Simulink, as the gate signal generator for the MSMI. Comparison has been made in terms of the PWM waveforms of each module and the gate signals for two different values of mi. The Simulink blocks designed to represent the gate signal generator based on the unipolar symmetrical regular sampled technique can be used as a basis to generate the gate signals for the MSMI in real time. This is possible through automatic code generation using a dSPACE controller board, which is based on a Texas Instruments TMS320C31 floating-point DSP.

VI. REFERENCES

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