DEVELOPMENT OF AUTO RE-CLOSER EARTH LEAKAGE CIRCUIT BREAKER (AR-ELCB)

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A thesis submitted in fulfillment of the requirements for the award of the degree of Bachelor of Electrical Engineering (Power Systems)

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Dedicated to
my beloved parents,
Jantan Anua Jah Bin Nawang and Huzaimah Binti Ismail,
sisters and brother,
Raihan, Nur Ain, and Mohamad Rosman
for giving a constant source of support and encouragement.

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Lastly, thanks to my father, mother and my siblings who were constant and active source of support throughout the endeavor.

ABSTRACT

An Earth Leakage Circuit Breaker (ELCB) is an electrical device that disconnects protected circuit whenever it detects unbalance current between the phase conductor and the neutral conductor. Such an unbalance is sometimes caused by current leakage through the body of a person who is grounded when accidentally touching the energized part of the circuit. A lethal shock can result from these conditions. ELCB are designed to disconnect this fault fast enough to mitigate the harm caused by such shocks. Currently, there is no Earth Leakage Circuit Breaker (ELCB) with auto re-closer features in the market. The current ELCB that available in the market is a manual type and cannot differentiate between temporary disturbances and permanent faults. It's means that, if a disturbance or fault occurs on the protected area (house or shop), the protection system will force ELCB to trip. One of the drawbacks of the common ELCB is that, it's can't turn on the power supply back to the normal operation condition although only a short disturbance occurs. Such disturbance is lightning strike on the transmission line in the distribution site near to the protected area. To turn the power back to normal operation, consumers need to do that manually. To overcome this problem, Auto Re-closer Earth Leakage Circuit Breaker (AR-ELCB) has been developed. This thesis presents the development of AR-ELCB. This device was designed to differentiate between permanent fault and short disturbances (lightning).

ABSTRAK

Alat pemutus litar bocor ke bumi (ELCB) ialah sejenis alat yang akan memutuskan litar yang dilindungi apabila ianya mengesan sebarang ketidakstabilan arus antara fasa konduktor dan neutral konduktor. Ketidakstabilan arus biasanya disebabkan oleh kebocoran arus menerusi badan manusia yang secara tidak sengaja tersentuh bahagian litar yang sedang aktif. Ianya boleh menghasilkan kejutan arus elektrik yang membawa kepada maut. ELCB dicipta untuk memutuskan kesilapan ini secepat yang mungkin untuk mengurangkan bahaya yang dihasilkan oleh kesilapan sedemikian. Pada masa sekarang, masih tiada lagi alat pemutus litar kebocoran bumi (ELCB) dengan fungsi penutup automatik di pasaran. ELCB yang terdapat di pasaran sekarang adalah dari jenis yang manual dan tidak dapat membezakan antara gangguan sementara ataupun kerosakan berkekalan. Ini bermakna, jika gangguan ataupun kesilapan berlaku di kawasan perlindungan (rumah ataupun kedai), sistem perlindungan akan menyebabkan ELCB memutuskan litar. Salah satu kekurangan pada ELCB yang biasa ialah, ia tidak boleh mengembalikan bekalan arus kepada keadaan operasi biasa walaupun gangguan yang berlaku hanyalah gangguan kecil sahaja. Contohnya gangguan oleh kilat yang menyambar pada saluran pangiriman di tapak pembahagian arus elektrik berhampiran dengan kawasan perlindungan. Untuk menghidupkan bekalan arus balik pelanggan mestilah melakukannya secara manual. Untuk mengatasi masalah ini alat penutup automatik pemutus litar bocor ke bumi (AR-ELCB) telah dibangunkan. Tesis ini membentangkan tentang pembangunan AR-ELCB. Alat ini dicipta untuk membezakan antara kerosakan berkekalan ataupun gangguan sebentar (kilat).

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LIST OF SYMBOLS

V	–	Voltage
ac	–	Alternating Current
dc	–	Direct Current
Ω	–	Ohm
I_i	–	Input Current
Io	–	Output Current
V_{in}	–	Input Voltage
V_o	–	Output Voltage
R_L	–	Load Resistor
Θ	–	Angle

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1 Project Background

The project is based on the problems of today ELCB that is controlled manually and cannot differentiate between permanent and temporary fault. This sometimes bring the problems to the consumer who were not at home and do not understand the danger of permanent fault that can cause fatal hazard.

This project is focused on the design and building a unit of auto re-closer earth leakage circuit breaker (ELCB) that can differentiate and act differently with different type of fault. The concept is if there are faulty occurred, the ELCB will trip, if the fault is from temporary fault type like lightning, ELCB will close back automatically after three seconds. But if the faulty is eternal/permanent fault like from electrical, electronic device or short circuit ELCB will eternally trip and the permanent faulty lamp/buzzer will on until the fault root cause is removed and the switch is “on” back by someone again. In this project the microcontroller processor has been chosen as a control element.

Firstly, the problem in this project is to understand and know what kind of differentiation between permanent fault and temporary fault. All aspect must be considered and there must be no neglecting even a little reason to gain the good result. And surely is to think how to trace the faulty with new device and combined it with other devices like control element and old ELCB to get the new Auto re-closer circuit

breaker. In this combination, all power and source value of voltage and currents of each device must be considered, and for that reason the designing of the additional circuit is important to match the voltage and currents value so that it is suitable with control element and the devices could work together.

1.2 Objectives:

The objectives of this project are:

i. To improve the ability of earth leakage circuit breaker (ELCB) unit
ii. To notify the type of fault whether temporary or eternal/permanent fault.
iii. To develop the Auto-Re closer ELCB

1.3 Scope of project

i. This project is focused to modify and improve the ELCB where the additional circuit with a system is added to the ELCB and automatically will make ELCB trigger/open when the permanent fault occurred and auto re-closed when temporary fault happened.
ii. To make the circuit more accurate and better, the microcontroller is used as a control element and the model is MC68HC11AI MOTOROLA Microprocessor.

1.4 Literature Review

ELCB is the **E**arth **L**eakage **C**ircuit **B**reaker. There are two types of ELCBs, the voltage operated device and the differential current operated device vELCB and iELCB. vELCBs were first introduced about sixty years ago and iELCB were first introduced about forty years ago.

The principle of operation of the vELCB is as follows. Under normal conditions the closed contacts of the vELCB feed the supply current to the load. The load is protected by a metal frame, such as in an electric cooker. The vELCB also has a relay coil, one end of which is connected to the metal frame and one end connected directly to ground. A shock risk will arise if a breakdown in the insulation occurs in the load which causes the metal frame to rise to a voltage above earth. A resultant current will flow from the metalwork through the relay coil to earth and when the frame voltage reaches a dangerous level, e.g. 50 volts, the current flowing through the relay coil will be sufficient to activate the relay thereby causing opening of the supply contacts and removal of the shock risk.

ELCB is essentially a voltage sensing device intended to detect dangerous voltage and current fault. The level of shock protection provided by the vELCB was somewhat limited as these devices would not provide shock protection in the event of direct contact with a live part. An additional problem with the vELCB was its tendency to be tripped by earth currents originating in other installations.

For many years, the voltage operated ELCB and the differential current operated ELCB were both referred to as ELCBs because it was a simpler name to remember. However, the use of a common name for two different devices gave rise to considerable confusion in the electrical industry. If the wrong type was used on an installation, the level of protection given could be substantially less than that intended. To remove this confusion, IEC decided to apply the term Residual Current Device (RCD) to differential

current operated ELCBs. Residual current refers to any current over and above the load current.

Through early research that have been done and the guidelines from articles, it states that the development of ELCB is focused to only development of better device and not to improve the system of ELCB cause there are no articles that give the idea how to add the function and system to this ELCB. Until today what the article said is the type, function and process of each component in ELCB. So it is important to struggle and combine all knowledge to design something new for this device.

1.5 Thesis Outline

This thesis contains 5 chapter which is every chapter have its own purpose. After viewing the entire chapter in this thesis hopefully viewer can understand the whole system design for this project.

Chapter 1 describe on the background of the project, objectives, scope of the project and the literature review that referred to in the development of Auto Re-Closer Earth Leakage Circuit Breaker (AR-ELCB).

Chapter 2 is focused to the theory of the Earth Leakage Circuit Breaker (ELCB), where it described about problems, ELCB design, the components inside ELCB and the operation of this device.

Chapter 3 elaborated more on the designing and operation of the new AR-ELCB systems. Besides it also describe the functions of each components used in the circuit especially on the second stage circuit.

Chapter 4 only focused to the control element circuit which is the most important part of the system. It described about the system of microcontroller detailed from the hardware until the software that has been used in this project.

Chapter 5 presents the data and result that have been got from the experiments while in development process. The result of this project also is accompanied by the discussions for each problem statements.

Lastly is chapter 6, in this chapter the conclusion have been made for the project from the whole aspect and there are also suggestions to improve the AR-ELCB on the future, it is for the commercialization. There is also the costing stated to produce the AR-ELCB.

CHAPTER 2

EARTH LEAKAGE CIRCUIT BREAKER

2.1 Introduction

An Earth Leakage Circuit Breaker (ELCB) is a device used to directly detect currents leaking to earth from an installation and cut the power. It was mainly used in TT earthing systems. The device could detect the leakage current and protect consumer from electrical shock if leakage current occurred to the consumer equipments. This device will cut off the electrical supply instantaneously when current leakage is detected. There are two types of ELCB:

i. Voltage Earth Leakage Circuit Breaker (vELCB)
ii. Current Earth Leakage Current Earth Leakage Circuit Breaker (iELCB)

This chapter describe about nowadays earth leakage circuit breaker that used in 240Vac for home and offices user. Before begin any project, whether to make any development or upgrading at least, it is important to understand the basic of the equipment and know how the device works. To achieve the objective for this chapter, the research of Earth Leakage Circuit Breaker is done by exploring the 240Vac ELCB that normally used for home or offices.

The objectives of this chapter are:

i. To know the system of basic Earth Leakage Circuit Breaker
ii. To know the components of Earth Leakage Circuit Breaker and know the function of each component.
iii. To understand how the device work

2.2 vELCB

vELCB is a voltage operated circuit breaker, the device will function when the Current passes through the ELCB. vELCB contains relay loop which it being connected to the metallic load body at one end and it is connected to ground wire at the other end. If the voltage of the load body is rise which could cause the difference between earth and load body voltage, the danger of electric shock will occur. This voltage difference will produce an electric current from the load metallic body passes the relay loop and to earth. When voltage on the load metallic body raised to the danger level which exceed to 50Volt, the flowing current through relay loop could move the relay contact by disconnecting the supply current to avoid from any danger electric shock.

2.3 iELCB

iELCB is current operated circuit breaker. The device will function with when the Current passes through ELCB. This current admitted to current transform device and on the load. Current from the load also admitted again to transform device. In normal state, total current applied to load is equal with total current out of the load. Because of the balance of in and out of current, it does not affect the current transform device. If there is any earth current leakage caused by earth damage, then the in and out current

will no longer in balance. These unbalance current phenomena will generate the current and if the current exceeded the prescribed rate, the ELCB will jerked and cut off the supply. The device also is called RCD, residual current device in IEC or RCCB residual current circuit breaker.

2.4 Problems of ELCB or RCCB

Earth Leakage Circuit Breaker is one type of electrical equipment that used as a protection device. The main purpose of this type of equipment is to cut off the power when the problem occurred. But the problem is will the device back to normally condition and function if the error occurred and there are no a human that can switch on back the device due to many reasons.

The device is using mechanical switch that must be switch on manually, after ELCB is being tripped it will stay off until there is someone push it back to the on condition although the problem that occurred is temporary fault and occurred in one millisecond.

The device also can not differentiate whether the fault is temporary or permanent fault where there are the differentiations between these two types. It also do not act differently for these two types of faulty.

2.5 Electrical faults

A fault is any abnormal situation in an electrical system in which the electrical current may or may not flow through the intended parts. Equipment failure also attributable to some defect in the circuit, example are loose connection, insulation failure or short circuit etc. Types of faults in a distribution network circuit are:

i) Over-load
ii) Faults on electrical equipments
iii) Transmission lines faults

Over-load faults are caused by the unexpected increasing of loads. Faults on electrical equipments are caused by lightning, insulator breakage, Product design which is out of specification and Improper installations of equipments.

Most faults on transmission lines of 100kV and higher are caused by lightning, which results in the flash over of insulators. Transmission lines faults are caused by, lightning, storm, fallen trees, Snow. One of the temporary faulty is cause by direst lightning phenomena. Where example of permanent fault is faults on electrical equipment.

2.6 ELCB Features

Figure 2.1 shows about Home ELCB with the housing, the function of this housing as the protection for the circuit. What who can be seen from this condition is only mechanical switch and the black box.

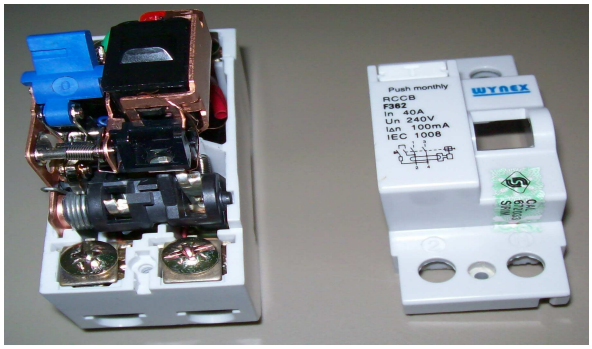

Figure 2.1: Home ELCB/RCCB with housing.

Figure 2.2 shows the whole ELCB component inside the housing, the most important thing in the system is the good insulator must be used for live and neutral cable, it is to avoid from ELCB self fault.

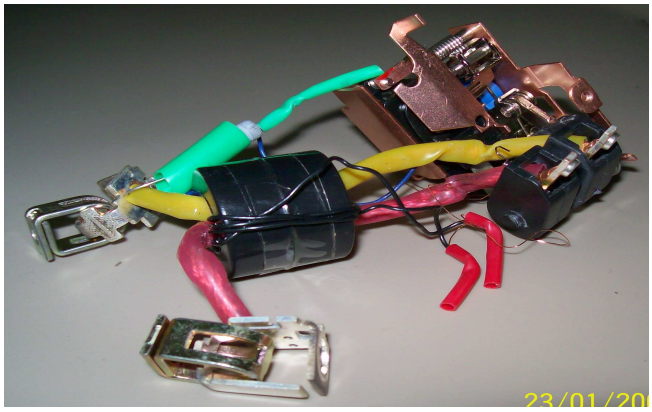

Figure 2.2: The system inside ELCB

2.7 ELCB Design

Figure 2.3 shows the design of ELCB, the design consists of mechanical switch, ZCT, Black Box, High level transistor and the reset button. Mechanical switch is a contact of black box, the function of this component is to trigger and cut off the power with cut off the life and neutral line altogether. The function of high level transistor is to limit the current flowing through its line when the reset button is pushed. Then the ZCT, the function of this component is to detect the unbalance current in the system and send the signal (induced current) to Black Box. In a black box there is a coil, the coil will activate the mechanical switch after received the minimum current level 100mA (theoretically) from the ZCT. Lastly, there is also reset button, the function of the reset button is to re-set back the device to the initial condition and also as a point to detect whether the device still in good condition or damage/expired.

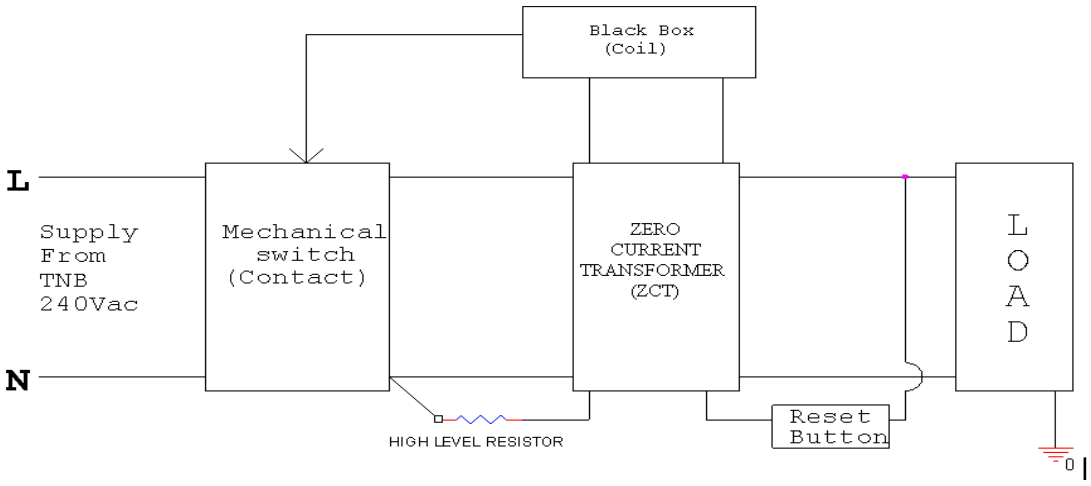

Figure 2.3: Earth Leakage Circuit Breaker design

2.8 Operation of ELCB

Based on the Figure 2.4 when the faulty occurred, ZCT will detect the imbalance current in the system, so the induced current will happened in ZCT, induced current that reached the min value to activate the coil will be send as a signal to the Black Box, when the coil is activated, it will sense the contact to trigger and automatically the mechanical switch is triggered and this will cut off the supply from main line.

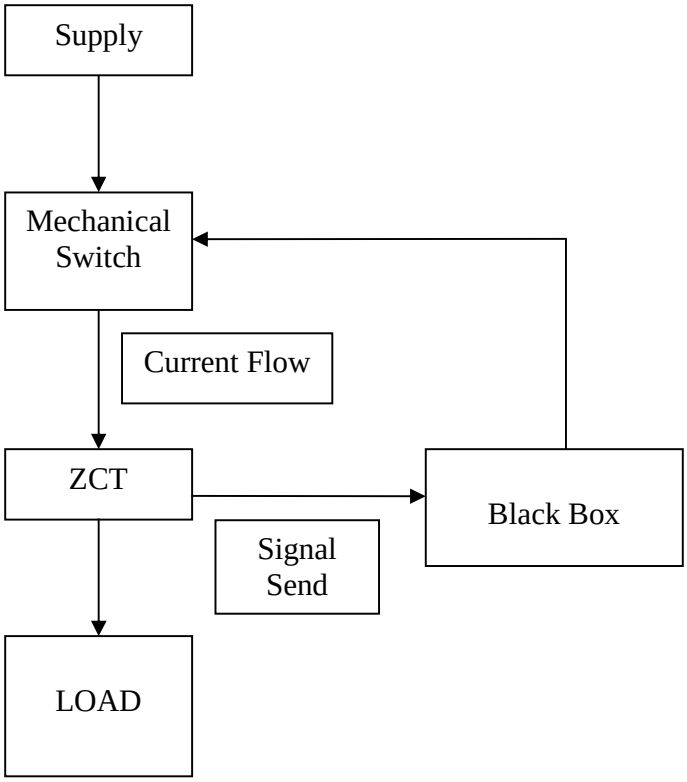

Figure 2.4: Earth Leakage Circuit Breaker Operation Flow

2.9 Summary

There are two types of ELCB, both device used for protection device for electrical equipment and for safety for human being from fatality hazard. Each device has a little differentiation in operation. If there are the faulty occurred the device will with cut off the supply in the main line. So the equipment will be safe. ELCB also must be able to act differently between permanent fault and temporary fault. It can improve ELCB ability and can its function. From this study, it helps to understand the principles, operation, and function of each device.

CHAPTER 3

DEVELOPMENT OF AUTO RE-CLOSER EARTH LEAKAGE CIRCUIT BREAKER

3.1 Introduction

This chapter explained about the methodology and technical aspect that used in the development of the AR-ELCB from the project flow, circuit design until the device chosen. Beside of it also describes about final hardware design of auto re-closer circuit breaker, the reason, advantages and the function of each circuit. The effectiveness of new idea have been considered, then several efforts and changed have been done to the new circuit design in order to decrease the cost and maintain the function of the product.

3.2 Project Flow

This project is began with study the problem of old device, this is done by took at look at the physical and consumer problem. The next stage is identified the element that can be improved due to the budget and knowledge for this type of device. After that, studied the operation of old device and knew all functions of each component inside ELCB and understand how the devices work. Next is proposed the idea to improve the device altogether with problem solving. The next stage is implement the knowledge and make development to the project, it includes designing process for the new device, install the control element circuit(Microcontroller), design the programming software of microcontroller and program it into Microcontroller IC. After finish in control element part, installation of the IC linear voltage regulator circuit, current transducer circuit has been done. Lastly is all circuit was combined with ELCB. Then the new Auto Re-closer ELCB was tested in laboratory, there were several problems occur, the hardware has been troubleshooting, and the retest process was done again until the hardware fully functions and the objectives of this project achieved.

3.3 AR-ELCB Design

From the Figure 3.1, the Heavy Duty Power Relay replaced the function of mechanical switch in old ELCB. Function of Zero Current Transformer (ZCT) is to detect the unbalanced current between life and neutral line. Function of 240/15 Vac Transformer is to reduced the voltage and supply to IC linear Voltage Regulator. As an early protection at control supply line, the zener diode was used to ground the over voltage instantly if over voltage occurred in this line.

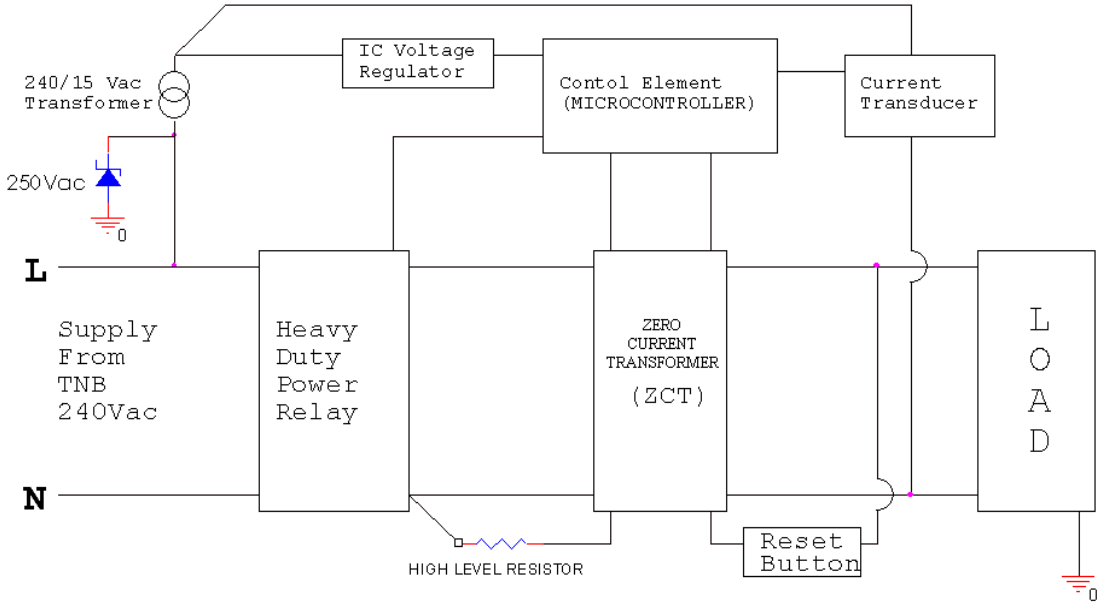

Figure 3.1: Proposed design of Auto Re-closer Circuit Breaker

For IC Voltage Regulator, the model of LM7805 was used to fix the voltage from 15V of Transformer to 5V for control element circuit. The function of current transducer is to detect the range of current in neutral line and send the signal to the microcontroller.

3.4 Improvement and Hardware Design

Refer to the Figure 3.2 it shows the block diagram for the whole system of AR-ELCB. Heavy Duty Power Relay replaced the function of mechanical switch in old ELCB. Function of Zero Current Transformer (ZCT) is to detect the unbalanced current between life and neutral line. Function of 240/15 Vac Transformer is to reduced the voltage and supply to power supply circuit. As an early protection at control supply line, the zener diode was used, the device is used to ground the over voltage to earth instantly if over voltage occurred in this line.

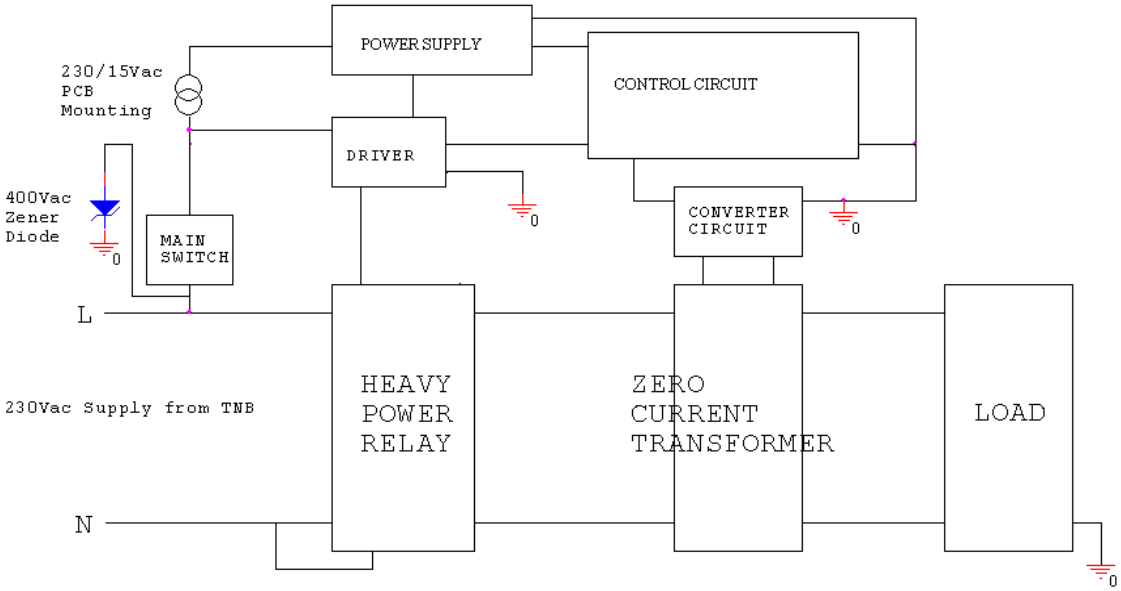

Figure 3.2: Final Design of Auto Re-Closer ELCB

The model of IC used is Motorola MC68HC11A1 it will function as a brain of the control element circuit. Then the IC Voltage Regulator circuit is used for power supply circuit. The Main switch is 250Vac switch. Driver also is used for intermediary between Heavy Power Relay with microcontroller and with main power supply, and then the TRD-5VDC-FB-CL has been chosen for the driver.

Lastly is the converter circuit, the converter circuit will convert the current from Zero Current Transformers (ZCT) to voltage and the voltage will be sent to switch circuit and the Op-Amp has been chosen as the main device.

3.5 Stage 1 Circuit

Refer to the Figure 3.3 it is control element circuit bootstrap mode, this circuit is the combination from one MC68HC11A1 MOTOROLA microprocessor that act as the brain of the system, there is also MAXIM 233, the function of MAXIM or MAX233 is to interface the computer with microprocessor. DPST switch, function as reset button in this circuit, there is also 8MHz crystal used to control the clock cycle of the system. The LM7805 was used for voltage regulator circuit, it is to produce $5V_{dc}$ output to supply the power to microcontroller circuit. There are also one 10MΩ, four 4.7kΩ resistors, two for each 4.7uF, 1uF, and 22pF capacitors. The detailed is described in Chapter 4.

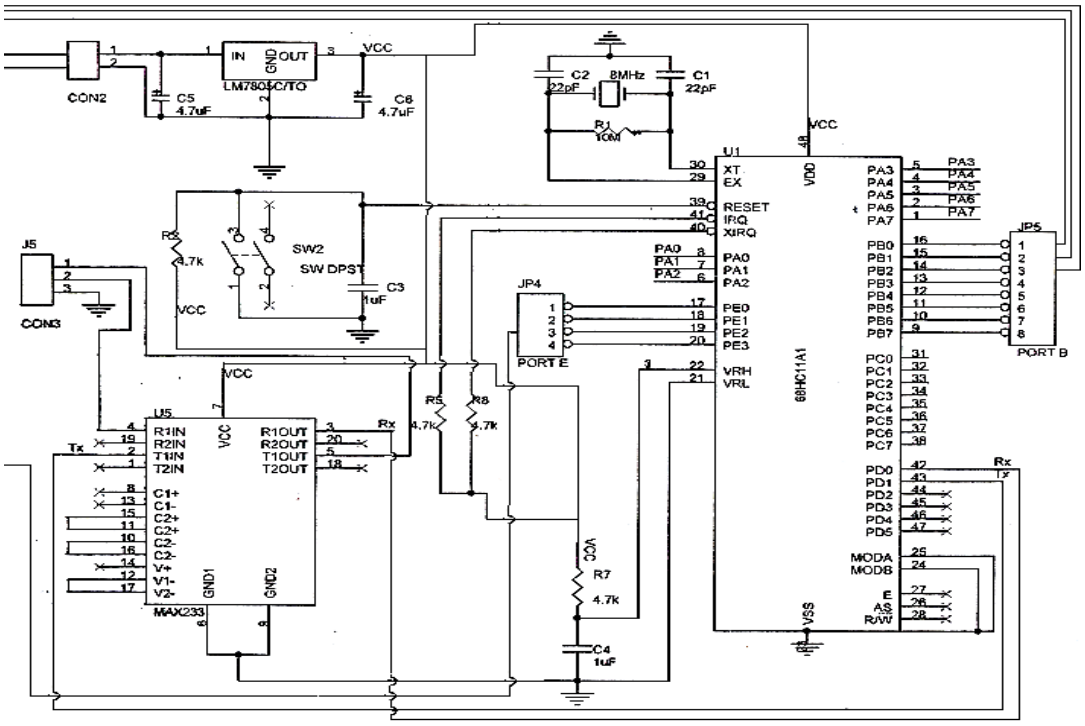

Figure 3.3: Bootstrap Mode Circuit

3.6 Stage 2 Circuit

Figure 3.4 shows the detailed of additional circuit except for control element circuit. This is the second stage circuit, the combination of both stage one and stage two circuits will complete the AR-ELCB. The detailed description of each components consist in this circuit will be describe on the next page.

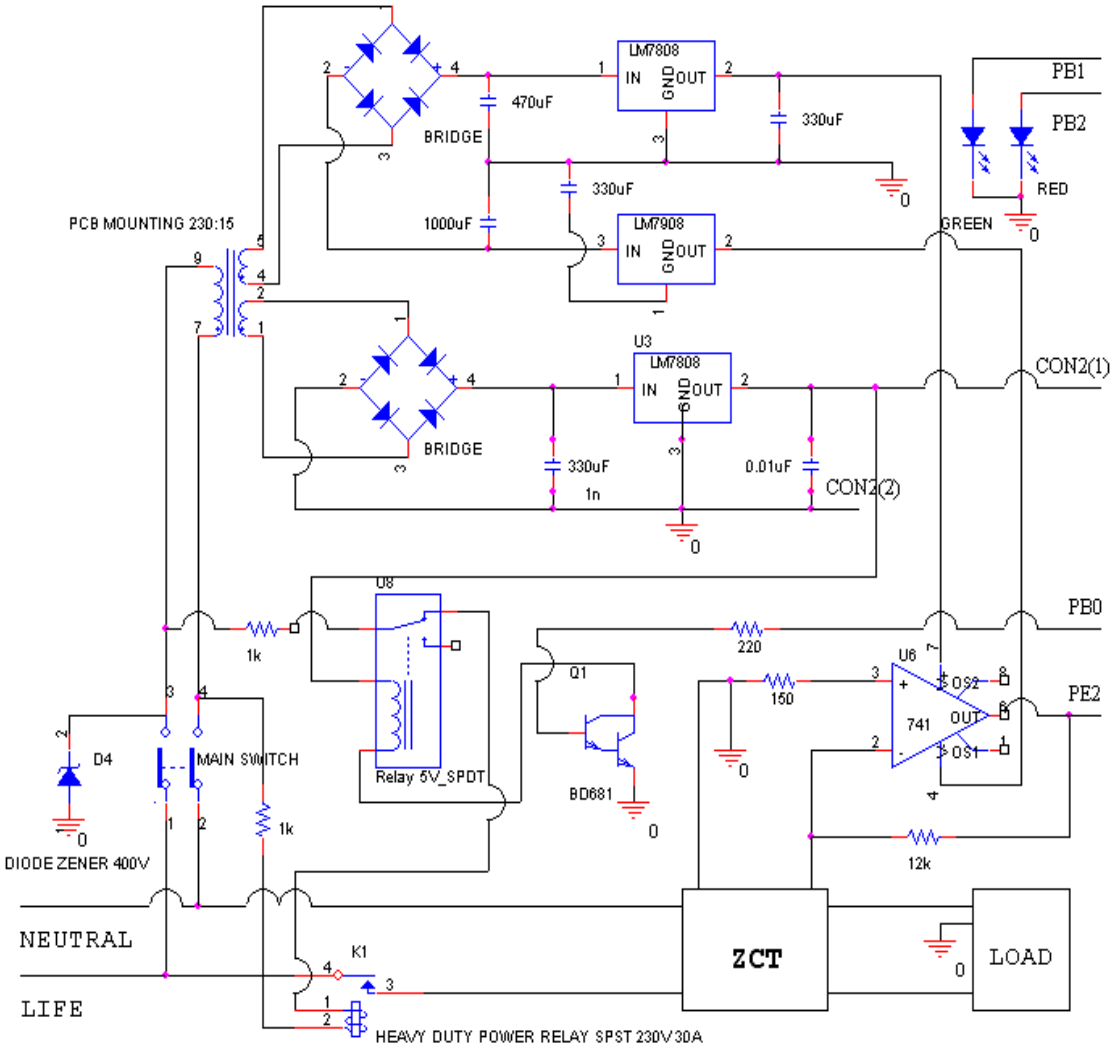

Figure 3.4: Additional circuit

3.6.1 Heavy Duty Power Relay

Refer to the Figure 3.5 the Heavy Duty Power Relay is a high-capacity, high-dielectric-strength relay and compatible with Momentary Voltage Drops.

Figure 3.5: Heavy Duty Power Relay

For this product there is no contact chattering for momentary voltage drops up to 50% of rated voltage. It also has a wide-range AC-activated coil that handles 100 to 120 or 200 to 240 Vac at either 50 or 60 Hz. The miniature is hinge for maximum switching power, Flame-resistance materials (UL94V-0-qualifying) and used for all insulation material.

It replaced the function of mechanical switch in old ELCB, it will cut-off the main incoming live supply power cable or retract back if the unbalanced current occur in the system.

3.6.2 Zero Current Transformers (ZCT)

Figure 3.6 shows the ZCT, the function of ZCT is to detect the unbalanced current between life and neutral line. Then the induced current will be sent to converter circuit, the polarity connection of this device must be invert so that the positive supply will be produce from converter circuit.

Figure 3.6: Zero Current Transformers

3.6.3 PCB MOUNTING 230/15 Vac Transformer

Figure 3.7 shows the PCB MOUNTING, it is one type of transformer that used to reduce the voltage from 230Vac to 15Vac and supply the voltage to the power supply circuit. It is the most comprehensive choice of secondary voltages. It also is flame retardant bobbins and shrouds. Besides, fully shrouded construction

Figure 3.7: PCB MOUNTING

3.6.4 400V Zener Diode

Refer to Figure 3.8 the component function as an early protection at the control supply line, it will ground the over voltage to the earth instantly if over voltage occurred in this line. So the whole system will be turn off means that there is no supply can be flow to the home because the AR-ELCB is deactivated.

Figure 3.8: 400V Zener Diode

3.6.5 TRD-5VDC-FB-CL

Figure 3.9 shows the TRD-5VDC-FB-CL relay, this device function as a driver in the second stage circuit, it is use to be the intermediary between Heavy Duty Power Relay with microcontroller and with main power supply.

Figure 3.9: 5Vdc Relay

For this AR-ELCB circuit, 5V relay must be installed in normally closed condition.

3.6.6 Power Supply Circuit

Figure 3.10 shows the model of UTC LM 78XX. The UTC LM78XX family is monolithic fixed voltage regulator integrated circuit. They are suitable for applications that required supply current up to 1 A.

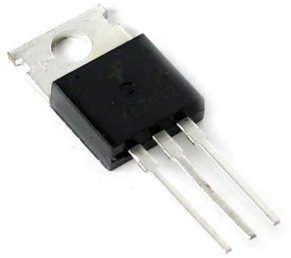

Figure 3.10: UTC LM78XX

The UTC LM79XX series of three-terminal negative regulators are available in TO-220 package and with several fixed output voltage, making them useful in a wide range of application. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible.

There are three IC Voltage Regulator circuits that have been used, two LM7808, and one LM7908 to fix the voltage from 15V of Transformer to 8V and -8V for control element and converter circuit.

3.6.7 Bridge

Refer to the Figure 3.11 it is the KBPC3510 Bridge model, it is used to rectify the voltage from AC supply to DC power supply for IC voltage regulator device. This AR-ELCB need two bridges because it was used both PCB MOUNTING output terminals.

Figure 3.11: Bridge

3.6.8 250Vac Switch

Figure 3.12 shows the 250Vac Switch, it is the main switch for the whole circuit. The function of this Main switch is to open and closed the whole system. This switch functions manually.

Figure 3.12: 250Vac Switch

3.6.9 BD681 Darlington Transistor

Figure 3.13 shows the BD681, it is a silicon epitaxial-base NPN power transistors in monolithic Darlington configuration mounted in Jade SOT-32 plastic package. They are intended for use in medium power liner and switching applications

BD681 was used as the intermediary between MC68HC11A1 with TRD-5VDC-FB-CL relays; it will drive the high current from power supply and function when 5V output voltage from microcontroller is supplied to it.

Figure 3.13: BD681 Darlington Transistor

3.6.10 Converter Circuit (UA741)

Figure 3.14 shows the UA741, the UA741 model is a high performance monolithic operational amplifier constructed on a single silicon chip. It is intended for a wide range of analog applications, example:

a) Summing amplifier
b) Voltage follower
c) Integrator
d) Active filter
e) Function generator

The UA741 is the high gain and wide ranges of operating voltages provide superior performances in integrator, summing amplifier and general feedback applications. The internal compensation network (6dB/ octave) insures stability in closed loop circuits.

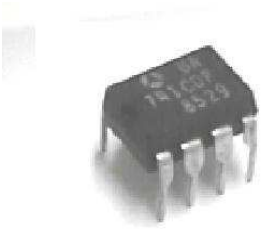

Figure 3.14: UA741

The UA741 is the model of Op-Amp that used in this AR-ELCB circuit, it is used for current controlled voltage source, the function of this circuit is to convert the current from zero current transformers (ZCT) to voltage and the voltage will be sent to MC68HC11A1 microprocessor and the voltage classified as input for microcontroller element.

3.6.11 Green and Red Light Emitting Diode (LED)

Figure 3.15 shows green and red light-emitting-diode (LED), LED is a semiconductor diode that emits light when an electric current is applied in the forward direction of the device, as in the simple LED circuit. The effect is a form of electroluminescence where incoherent and narrow-spectrum light is emitted from the p-n junction.

Figure 3.15: Light Emitting Diode (LED)

In this project, the green LED was used to show that there are lightning occur, and the circuit trigger will re-close back after 9.8 seconds. Besides the red LED is use to show that there are short circuit or permanent fault occur and the circuit will permanently cut-off the incoming supply until the fault root cause is remove and the reset button is pushed by someone.

3.7 Flow Chart

Refer to the Figure 3.16, when the fault occur, zero current transformers (ZCT) will send the unbalance current that means there are fault occurred in the system. ZCT then will send the current induced to the converter and converter will produce voltage from it, then the converter will send the signal to input pin in the microcontroller. In the microcontroller it will collect the data and transmit the output to the driver, where each data that collected were stored in memory so that it can be used to differentiate the type of fault and produce the output. If the fault occurred only once, that means the lightning disturbance occurred, besides if the fault occurred thrice in 20.61 seconds continuously, the short circuit occurred and the continuously output will be send to the driver to activate the relay, if lightning the output will be only for a few seconds so that the Heavy Duty Power Relay will retract and the circuit will normally operates.

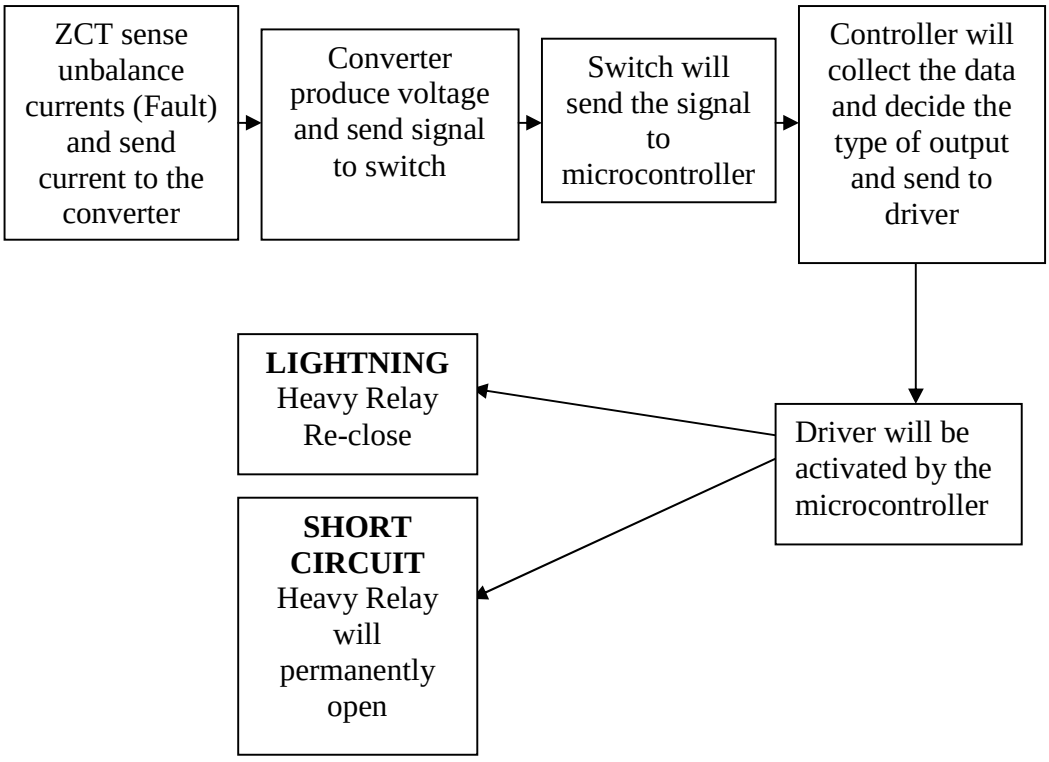

Figure 3.16: Flow chart of the system

3.8 Hardware Operation Process

From the flow on the Figure 3.17 started with the supply voltage from TNB, then the supply will flow to the system through Power Relay switch, the function of this relay is as Main switch for the whole Home supply system. If the unbalanced current between life and neutral line occurred and the value reached Δ100mA, the current will be induced automatically in the ZCT and transferred to the converter circuit. Then the output voltage will be send the signal of 5V to the port E of microcontroller. All command process will be done like programmed in the microcontroller, microcontroller will identify what type of output that will be sent to the driver due to programmed software. Then the output will be send to the port B that connect to the driver and lastly driver will active and send the signal to the Heavy Duty Power Relay.

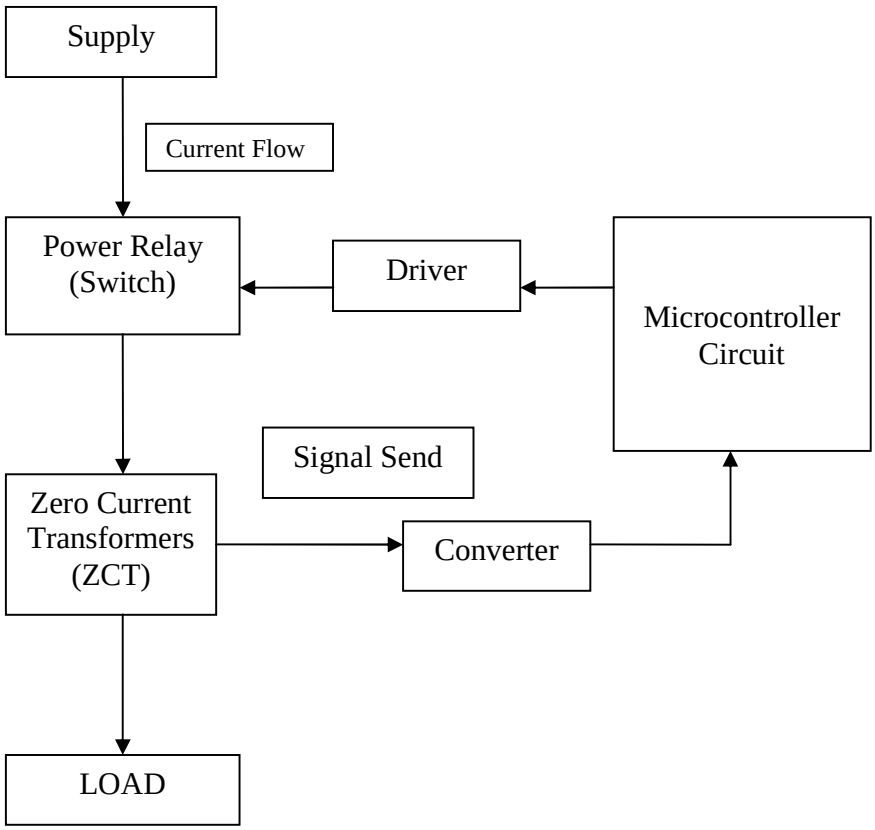

Figure 3.17: Hardware operation process of Auto Re-Closer ELCB

3.9 Summary

The concept and method of AR-ELCB development have been described. Understanding each components concepts and functions has made the development process easier than thought. The function of second stage circuit is very important because almost half of this circuit functions more to the electromechanical actions like the main components to cut-off the main supply is Heavy Duty Power Relay. Based on this new improvement circuit, the more efficient system has been developed.

CHAPTER 4

CONTROL ELEMENT CIRCUIT

4.1 Introduction

Control circuit act like the brain the system. In this system the Motorola MC68HC11A1P model has been used microcontroller. The HCMOS MC68HC11A8 is an advanced 8-bit microcontroller (MCU) with highly sophisticated on-chip peripheral capabilities. A fully static design and high-density complementary metal-oxide semiconductor (HCMOS) fabrication process allow E-series devices to operate at frequencies from 3 MHz to dc, with very low power consumption. For programming the MC68HC11A8, the use of the low level language have been decided due to it is only use one input pin and three output pin. To compile this type of programming language, the ASM.11 program is used. Besides, the WP11 software has been used to program the command into the EEPROM chip of the IC.

4.2 48 Pin Dip Microcontroller Picture

Figure 4.1 shows the 48 Pin Dip Microcontroller picture, except this type, the MC68HC11A8 also available in the 52-pin plastic leaded chip carrier (PLCC), or the 64-pin quad flat pack (QFP). But for AR-ELCB project the 48 pin DIP microcontroller has been used.

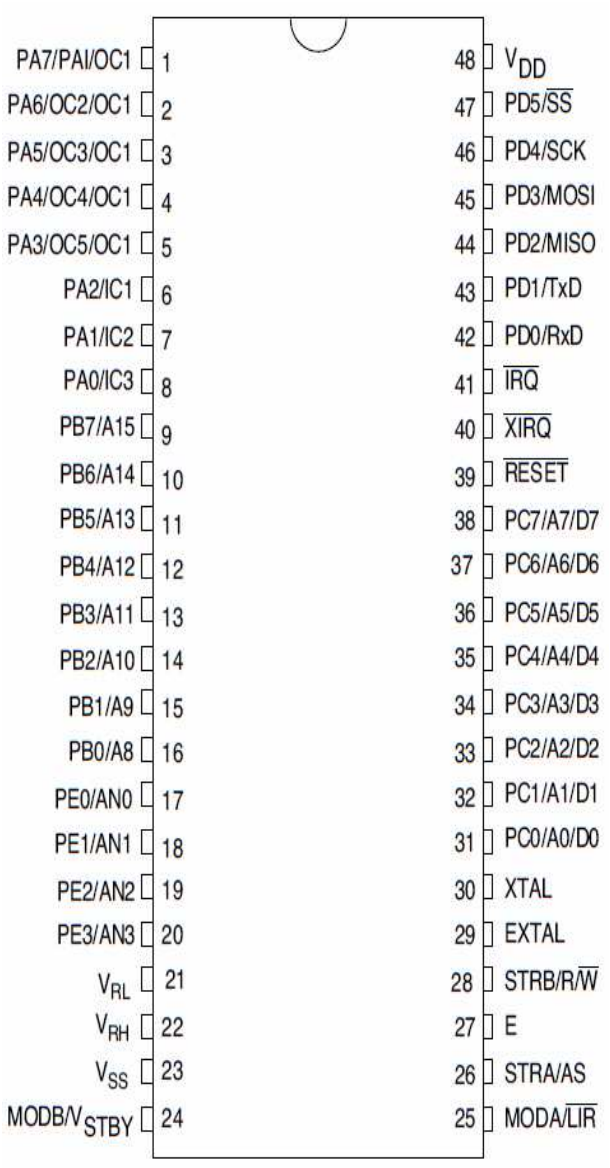

Figure 4.1: 48 Pin Dip Microcontroller

4.3 Hardware Features

The features of the microcontroller are as follows:

- 8 Kbytes of ROM
- 512 Bytes of EEPROM
- 256 Bytes of RAM (All Saved During Standby) Relocatable to Any 4K Boundary
- Enhanced 16-Bit Timer System:
  - Four Stage Programmable Prescaler
  - Three Input Capture Functions
  - Five Output Compare Functions
- 8-Bit Pulse Accumulator Circuit
- Enhanced NRZ Serial Communications Interface (SCI)
- Serial Peripheral Interface (SPI)
- Eight Channel, 8-Bit Analog-to-Digital Converter
- Real Time Interrupt Circuit
- Computer Operating Properly (COP) Watchdog System
- Available in Dual-In-Line or Leaded Chip Carrier Packages

4.4 Software Features

The software features for the microcontroller are as follows:

- Enhanced M6800/M6801 Instruction Set
- 16 x 16 Integer and Fractional Divide Features
- Bit Manipulation
- WAIT Mode
- STOP Mode

4.5 General Description

Figure 4.2 shows the MC68HC11A1P microprocessor model. The high-density CMOS technology (HCMOS) used on the MC68HC11A8 combines smaller size and higher speeds with the low power and high noise immunity of CMOS. On-chip memory systems include 8 Kbytes of ROM, 512 bytes of electrically erasable programmable ROM (EEPROM), and 256 bytes of static RAM.

Figure 4.2: MC68HC11A1P Microprocessor

Major peripheral functions are provided on-chip. An eight channel analog-to-digital (A/D) converter is included with eight bits of resolution. An asynchronous serial communications interface (SCI) and a separate synchronous serial peripheral interface (SPI) are included. The main 16-bit free-running timer system has three input capture lines, five outputs compare lines, and a real-time interrupt function. An 8-bit pulse accumulator subsystem can count external events or measure external periods. Self monitoring circuitry is included on-chip to protect against system errors. A computer operating properly (COP) watchdog system protects against software failures. A clock monitor system generates a system reset in case the clock is lost or runs too slow. An illegal opcode detection circuit provides a non-maskable interrupt if an illegal opcode is detected. Two software controlled operating modes, WAIT and STOP, are available to conserve additional power.

4.6 Input and Output Port Used

This subchapter is described about the input port and output port that has been used in the development of AR-ELCB project. Input port is connected to the output port of the current controlled voltage sources circuit, besides one output port is connected to the BD681 and two to the LEDs.

4.6.1 Port B

While in single-chip operating modes, all of the port B pins are general-purpose output pins. During MCU reads of this port, the level sensed at the input side of the port B output drivers is read. Port B may also be used in a simple strobe output mode where an output pulse appears at the STRB signal each time data is written to port B. When in expanded multiplexed operating modes, all of the port B pins acts as high order address output signals. During each MCU cycle, bits 8 through 15 of the address are output on the PB0-PB7 lines respectively.

4.6.2 Port E

Port E is used for general-purpose inputs and/or analog-to-digital (A/D) input channels. Reading port E during the sampling portion of an A/D conversion could cause very small disturbances and affect the accuracy of that result. If very high accuracy is required, avoid reading port E during conversions. But due to the input and output pin used is only four ports, it is recommended to use this port to avoid from disturbing the programmed set.

4.7 Operating Modes

There are four operating modes for the MC68HC11A8: single-chip operating mode expanded multiplexed operating mode, special bootstrap operating mode, and special test operating mode. But for this project the special bootstrap operating mode has been chosen due to the less of input and output pin use and simple programming.

4.7.1 Special Bootstrap Operating Mode

The bootstrap mode is considered a special operating mode as distinguished from the normal single-chip operating mode. This is a very versatile operating mode since there are essentially no limitations on the special purpose program that can be loaded into the internal RAM. The boot loader program is contained in the 192 byte bootstrap ROM. This ROM is enabled only if the MCU is reset in special bootstrap operating mode, and appears as internal memory space at locations $BF40-$BFFF. The boot loader program will use the SCI to read a 256 byte program into on-chip RAM at locations $0000-$00FF. After the character for address $00FF is received, control is automatically passed to that program at location $0000. The MC68HC11A8 communicates through the SCI port. After reset in special bootstrap operating mode, the SCI is running at E clock/16 (7812 baud for E clock equal 2 MHz). If the security feature was specified and the security bit is set, $FF is output by the SCI transmitter. The EEPROM is then erased. If erasure is unsuccessful, $FF is output again and erasure is attempted again. Upon successful erasure of the EEPROM, all internal RAM is written over with $FF. The CONFIG register is then erased. The boot loader program now proceeds as though the part had not been in security mode.

If the part is not in security mode (or has completed the above erase sequence), a break character is output by the SCI transmitter. For normal use of the boot loader program, the user sends $FF to the SCI receiver at either E clock/16 (7812 baud for E clock = 2 MHz) or E clock/104 (1200 baud for E clock = 2 MHz).

The user must download 256 bytes of program data to be put into RAM starting at location $0000. These characters are echoed through the transmitter. When loading is complete, the program jumps to location $0000 and begins executing that code.

If the SCI transmitter pin is to be used, an external pull-up resistor is required because port D pins are configured for wire-OR operation. In special bootstrap operating mode the interrupt vectors are directed to RAM as shown in Table 4.1. This allows the user to use interrupts by way of a jump table. For example: to use the SWI interrupt, a jump instruction would be placed in RAM at locations $00F4, $00F5, and $00F6. When an SWI is encountered, the vector (which is in the boot loader ROM program) will direct program control to location $00F4 in RAM which in turn contains a JUMP instruction to the interrupt service routine.

Table 4.1: Bootstrap mode interrupt vector

Address	Vector
00C4	SCI
00C7	SPI
00CA	Pulse Accumulator Input Edge
00CD	Pulse Accumulator Overflow
00D0	Timer Overflow
00D3	Timer Output Compare 5
00D6	Timer Output Compare 4
00D9	Timer Output Compare 3
00DC	Timer Output Compare 2
00DF	Timer Output Compare 1
00E2	Timer Input Capture 3
00E5	Timer Input Capture 2
00E8	Timer Input Capture 1
00EB	Real Time Interrupt
00EE	IRQ
00F1	XIRQ
00F4	SWI
00F7	Illegal Opcode
00FA	COP Fail
00FD	Clock Monitor
BF40 (Boot)	Reset

4.7.2 Hardware Picture

Figure 4.3 shows the real bootstrap mode hardware connection circuit has been installed for AR-ELCB control element circuit, in this circuit there are eight LEDs installed, the function of these components (LED) is as output sign to check the programming command whether the programming is right or wrong, it is to ensure that there were no any problems on the control element circuit before the whole circuit is compiled. By used this method, there will be easier to detect any problems by trouble shoot the right circuit.

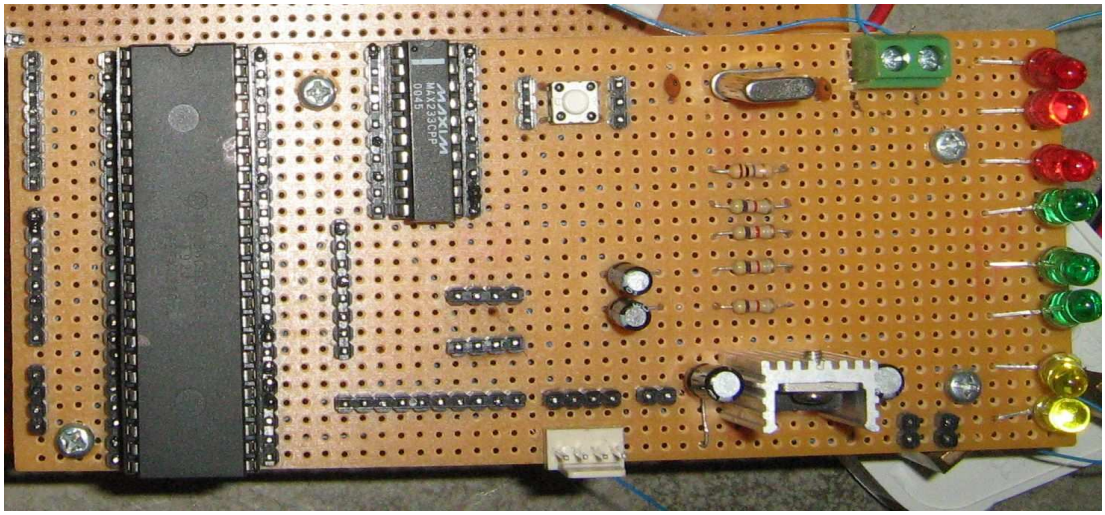

Figure 4.3: Control Element Circuit

4.8 Programming Flowchart

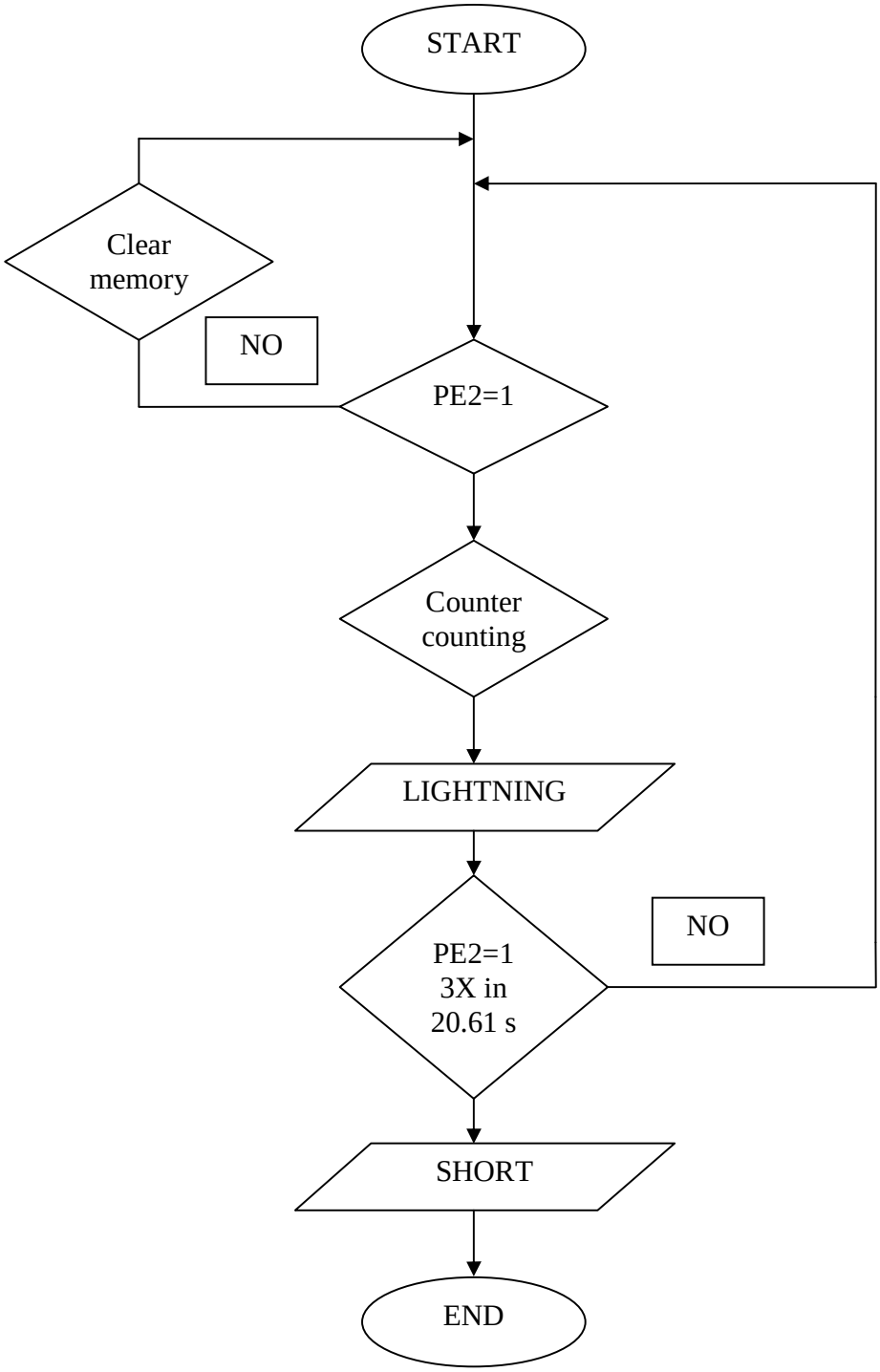

Figure 4.4: Flow of programming software

From Figure 4.4, Firstly the start sign show the beginning of the program so the program will always running in the microcontroller, If the input port of microcontroller PE2 detect the signal 1 the memory will identify the faulty is Lightning and the output port will active also produce output 5V for 9.8 seconds only. If not the system will clear the memory and rescan the input port again, if there is no signal at the input pin the system will ignore the action and keep rescanning continuously. But if the input signal is always 1 or positive for thrice scan continuously in 20.61 seconds, the system will identify as short circuit and the output port will be set to give the 5V output permanently until the reset button is pushed.

4.9 Programming Description

Firstly, the value and address for each port used must be defined. Then in this program, The LDX command is used because of the command used inclusive the index register command and add instruction for the address. For bootstrap mode the system operation range is started with $B600 address.

When the microcontroller circuit is activated, the first thing that microcontroller will do is clear accumulator A, B and index register Y. It is for make sure that there is no other data that is not erased after the reset button is pushed to avoid it from the system erroneous each time it begin to operate. The first command is scan, where the contents input port E,X is sent to the accumulator A, then the contents of accumulator A or ACCA is subtract with the value of #$04 from CMPA instruction, if the result is zero that means value in the ACCA from the input port E,X also #$04 the next instruction of BEQ must be followed, if the value is not same so the program will clear index register Y from command CLRY and rescanning again to the scan command again from BRA instruction. If the result is branch equal (BEQ) the program will followed the instruction in the LIGHT command.

In the LIGHT, first is command INY increment Y where each time the process of light occurred the value will be hold in the index register Y and the addition process will occurred. If the value of index register Y reach #$03 the instruction will jump to SHORT, if it is not the contents or value of #$03 will be load (read instruction) to the ACCA, then the contents of ACCA is transform to write operation (STAA) to port B,X and the BSR instruction will function and the output will appear due to the DELAY instruction. After that the system will clear A (CLRA) then the contents of ACCA is stored to the address $1004 and the process will occurred as long as like programmed in AKU instruction. After AKU instruction have done the system will rescanning to the SCAN again and the process will rotate continuously.

If the program go to the SHORT command the contents or value of #$05 will be load (read instruction) to the ACCA, then the contents of ACCA is transform to write operation (STAA) to port B,X and the BSR instruction will function and the output will appear due to the DELAY instruction. After that the command will rescan to the short command again and the process will continuously short until the reset button is pushed.

For AKU firstly ACCA is pushed into stack, then IX is pushed into stack, next the value of #02 is load to the ACCA, then the #$FFFE is load into IX register, next is the DEX decrement value of the IX register will running one by one till the end, if it is not it will repeat to DEX. After that the DECA decrement ACCA will operate followed to its value #02. If it is not equal the repeat instruction will be done to the same value. then the IX is pulled back from stack followed by ACCA also from stack. The process from AKU command occurred in 0.458 seconds.

For DELAY firstly ACCA is pushed into stack, then IX is pushed into stack, next the value of #43 is load to the ACCA, then the #$FFFE is load into IX register, next is the DEX decrement value of the IX register will running one by one till the end, if it is not it will repeat to DEX. After that the DECA decrement ACCA will operate followed to its value #43. If it is not equal the repeat instruction will be done to the same

value. Then the IX is pulled back from stack followed by ACCA also from stack. The process from AKU command occurred in 9.847 seconds. Then the programming END.

4.10 Summary

The use of microcontroller has made the system more reliable, acting faster and has wider chances to be upgraded soon especially if there are changes in programming system. Besides it has reduces the cost and space of control circuit, compared to the use of fully mechanical controller components like portable timer and portable counter. The programming for MC68HC11A1 also is easier with the existence of ASM.11 and WP11 software especially for the programming that involve only one input port and three output port.

CHAPTER 5

RESULTS & DISCUSSIONS

5.1 Introduction

This chapter describes about the results and discussions for the whole development of Auto Re-Closer Earth Leakage Circuit Breaker (AR-ELCB) project process. The result that will be discussed in this chapter is for the measurement of Zero Current Transformer (ZCT), the calculation to built converter circuit and the result for the whole AR-ELCB systems. The calculation involve in this chapter is depends on the result of measurement of ZCT. It is due to the ZCT function as the sensor in the system, only system with the great sensor can achieve the objectives. There is no meaning if the sensor of this system failed to operate. Every discussion stated in this chapter also is for the whole system problems, the priority must be to overcome the problems of this AR-ELCB system.

5.2 Measurement of ZCT

The objectives of measurement ZCT is to get the value of output current from the winding wire of the ZCT, the induced current will be absorbed by the core then is transferred to the winding and the currents will flow through the winding. The priority must be taken care for the current magnitude, which one is positive and negative. This is very important while in designing the current controlled voltage source.

The 240Vac single phase Motor has been used as the load, the significant of used the motor is it drew high current for starting, this situation theoretically produced the spark at the beginning but after that the condition will back to normal, this condition could be assume as lightning occurred, the concept is same. But the most important thing is from this experiment is to gain the lowest value of currents that could be detected by ZCT to produce the output current.

To measure the ZCT, only live line supply is passed through ZCT hole, where the neutral line will not passed though it, so the flux produce by both line will not overlapped to each other and the ZCT theoretically should sense the flux and produce output current at the starting motor.

Measurement result of Zero Current Transformer with AC Motor in free load in single phase motor = 1A, (I_{in} = I Starting Torque Motor).

Table 5.1: Measured Value of ZCT

No	Io (A)
1	0.125m
2	0.202m
3	0.146m
4	0.179m
5	0.437m
6	0.035m
7	0.134m
8	0.51
9	4.41
10	4.59
11	0.52
12	0.032m
13	0.27
14	1.37m
15	1.5m

Refer to the Table 5.1, it shows the result of output current from ZCT, the value of output current varied due to the instability of the load motor at the starting, the current drew by the motor at the beginning is not same, thus affect the value of output current. The higher current drew by the motor at starting, the higher value of the output current of ZCT.

This result will be used to design the Converter Circuit, see Figure 5.1. This Current Controlled Voltage Source Circuit used the model of UA741 Op-Amp. The output voltage is dependent on the input current of the ZCT.

It is easier to choose the value of ZCT output current if the data is reconstructed again and the middle or average value is taken for design process.

Table 5.2: Reconstructed Data of ZCT.

No	Io (A)(Reconstructed data)
1	4.59
2	4.41
3	0.52
4	0.52
5	0.27
6	1.5m
7	1.37m
8	0.437m
9	0.202m
10	0.179m
11	0.146m
12	0.134m
13	0.125m
14	0.035m
15	0.032m

Current Control Voltage Source Circuit

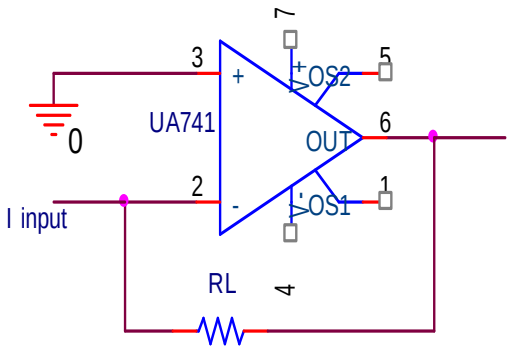

Figure 5.1: Converter Circuit.

Op-Amp Current controlled voltage source calculation

Theoritically

$V_o = -I_i R_L$

V_o is set to 5V

$R_L = - V_o/(-I_i)$

$R_L = 5/0.437$ m

$= 11441.64\ \Omega \approx 11k\ \Omega$

For above calculation, firstly the value of V_o has been set to 5V, but why 5V? It is due to the output voltage of this circuit is connected to the input port of microcontroller that need the 5V supply to be activated. From the reconstructed data on the Table 5.2, the value of o.437mA was taken. This value must be set and was assumed fix, it is due to find the value of R_L for permanent resistant. The current must be inverted to get the positive 5V output, this could be done by change the polarity for the real circuit of input and ground terminal for the converter circuit.

For RL 12kΩ

Vo = -(-Ii)RL

= 0.437 m (10k)

= 4.37 V

For RL 12kΩ

Vo = -(-Ii)RL

= 0.437 m (12k)

= 5.24 V

*The current must be inverted to produce positive output

To get the better resistant value and for safety, the calculation is repeated by used two different value of resistors.

From the result and the calculation above the average value was taken and the control circuit was built. The value of 12kΩ has been chosen for R_L due to the lack of resistance in stock. The problems stated in this section is the input current can not be measured scientifically due to the lack of apparatus and it was assumed to be 9A at the starting motor.

5.3 Project Results

The results of this project are presented as below:

i. MC68HC11A1 Controller can act like commanded in the programming.
ii. The AR-ELCB successfully built, operating like command and can differentiate between permanent and temporary fault
iii. AR-ELCB hold the circuit for 9.8 second if the lightning or spark occur, green LED light and retract to the normal condition after that besides the Green LED will off.
iv. AR-ELCB permanently closed the circuit if the circuit trigger thrice continuously in 20.61 second and the red LED light, the circuit will only back to normal condition and the red LED will off after the reset button is pushed by someone.

5.4 Discussions

From the whole project aspects, the discussions that have been stated are:

i. Datasheet about former ELCB do not complete. So the process of measuring the ZCT does not have the guideline. Besides, the knowledge about this component is very limited.
ii. Hard to analysis the ZCT due to lack of apparatus. The apparatus like power analyzer should be added in the laboratory and the student must be introducing to this type of device from year first in the University yet.
iii. Lack of references. This project is the development so everything that new must be creatively thinks how to solve although a little problem. The combination from own readings and the analog electronic knowledge help a lot.

iv. The MC68HC11A1 microcontroller can not do the multitasking process, thus make the programming hard to design. This problem occurred while in designing the timer programming, and because of that the programmer has manipulate and change the name sign for delay instruction to get the different timer in one way process.

v. The most annoying problem in this project is the microcontroller circuit does not stable while in building process. It takes more than one month to troubleshoot the whole circuit. The unstable problem comes from the wrapping method of the circuit, and the grounding of the microcontroller circuit.

vi. Lastly the low current draw from microcontroller has result the additional circuit designed to drive the alternative relay. Microcontroller can draw only limited current, the over current draw of microcontroller will result the overheat of microcontroller and will cause the dysfunction for the whole controller circuit.

5.5 Summary

From the results and discussions in this project, there are the things that could be consider to complete the whole AR-ELCB system, it is the sensitivity of this product, it comes from the experiment of the Zero Current Transformer (ZCT), the sensitivity of the product or device depends on this result, it is due to the only device that can control the sensitivity is the ZCT and converter circuit.

CHAPTER 6

CONCLUSIONS & SUGGESTIONS

6.1 Conclusions

The objective of the development of Auto Re-closer Earth Leakage Circuit Breaker was successfully fulfilled. In the designing the Auto Re-closer Earth Leakage Circuit Breaker it need the combination of analog electronics knowledge, autotronics knowledge, Microprocessor knowledge, power electronic knowledge and individual self skilled method to create the new circuit, it is due to there is no AR-ELCB circuit in the internet for comparison and as references, it is the new product. The use of LM7808 and LM7908 voltage regulators have increase the efficiency and reduce the cost of the system compared to by using the transformer less circuit. The use of Heavy power relay compared to solid state relay have reduce the cost and increase the reliability of the device where the device is not easy to burn out if wrong polarity installed to this device. So for the learning process it is better choice to use the heavy power relay because it is more to electromechanical system. The MC68HC11AC Motorola microprocessor as a brain has made the system more reliable for modern technology and the timer and delay for the system can be adjusted by changing the programming command. It also has improved the ability of Auto Re-closer Earth Leakage Circuit Breaker (AR-ELCB). Then the system also can act accurately besides can be updated by reprogram the IC. The successful of this AR-ELCB system has made the circuit can differentiate between permanent and temporary fault and acting differently between each type of fault.

6.2 Suggestions

There are several suggestions after the process for improvement AR-ELCB is successful:

i. For next improvement process the student must study the former ELCB detailed and make sure to understand for the system process before make the new design for the new device.

ii. In designing the circuit the choosing of correct device is important, the priority must be for the current rating and the device endurance.

iii. Make analysis for the Zero Current Transformer (ZCT) before buy the device for converter circuit. Make sure use power analyzer for analysis ZCT, the thing that must be measured is input and output of ZCT. Try to get the datasheet of ZCT from the device supplier.

iv. Replace mechanical switch of former ELCB with Heavy Duty Power Relay (DPST)-Double pole, not (SPST)-Single pole device. It is for totally hundred percent protection from incoming power supply cable where DPST will cut-off both neutral and life line if the unbalance current occurred.

v. Replace the bridge with 4 diode, array and connect it in the full wave rectifier connection, it will reduce the cost of bridge that is really expensive.

vi. For converter circuit replace the 741 Op-amp with 358 Op-amp, it is due to the 358 Op-amp just needs positive supply and ground to operate compared to 741 need positive, negative and grounding to operate, this will cause the designer must add the multiple power supply for the circuit, and surely the cost will increase.

vii. Replace the 40 pin MC68HC11A8 MOTOROLA microprocessor with 18 pin PIC16F83AT PIC. It is due to the programming of this type of PIC is easier compared to Motorola, besides it is compact. The PIC is built to overcome the weaknesses of microprocessor, so it has the better performance compared to MC68HC11A8, PIC programming also can do the multitasking process where it can do two job in a time or parallel process, compared to MC68HC11A8 that

only do single flow process or non multitasking process. Lastly the price of PIC16F83AT also is 100 percent cheaper than MC68HC11A8.

viii. It is recommended that the addition of Display screen (LCD), where this screen will tell the consumer what type of fault and what they should do. It is important to modernize the device.

ix. Replace the R_L for current controlled voltage source with the variable resistor where the variable resistor will make the rating for unbalance current can be variable. So the variable AR-ELCB can be produce. Variable AR-ELCB is more productive where the rating of unbalance current can be adjusted by consumer themselves or by industry to fulfill their demand.

6.3 Costing and Commercialization

The total cost of the development of Auto Re-closer Earth Leakage Circuit Breaker is RM 322.63. But the actual price of the whole AR-ELCB circuit is only RM 201.87. It is due to the changing of component in the development process, besides there were the components that do not function and need to be replaced while in circuit building process. The cost stated above is for the electronic and electric components that used and involve in this project. The cost for the AR-ELCB can be reduced by following the suggestion stated in the suggestion section and buy the components in bulk.

This project can be commercialize by built the new AR-ELCB that follow the feature that have been recommended in the suggestion section, it is due to the cost of the recommended new AR-ELCB is more cheaper than this new invention one. The estimated cost should be around RM 154.57 only without buy components in bulk way.

The new AR-ELCB has the higher commercialize value because it can resolve the existence ELCB problems.

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APPENDIX A

AR-ELCB Programming

AUTO RE-CLOSER EARTH LEAKAGE CIRCUIT BREAKER (AR-ELCB) PROGRAMMING USING MC68HC11A1 MOTOROLA MICROCONTROLLER

```
REGS    EQU   $1000
PORTB   EQU   4
PORTE   EQU   $A
        LDX   #REGS

        ORG   $B600          ; origin

MULA    CLRA                 ; clear accumulator A (ACCA)
        CLRB                 ; clear accumulator B (ACCB)
        CLRY                 ; clear index register Y

SCAN    LDAA  PORTE,X        ; load contents of address $100A into ACCA
        CMPA  #$04           ; compare the value of #$04 to the ACCA
        BEQ   LIGHT          ; if the result is equal, branch to LIGHT
instruction
        CLRY                 ; clear index register Y
        BRA   SCAN           ; toggle to the first instruction SCAN again

LIGHT   INY                  ; increment index register Y
        CPY   #$03           ; compare Y to the value of #$03
        BEQ   SHORT          ; if equal branch to SHORT
        LDAA  #$03           ; load value of #$03 to the ACCA
        STAA  PORTB,X        ; store the contents of ACCA to the $1004
        BSR   DELAY          ; branch to DELAY
        CLRA                 ; clear ACCA
        STAA  PORTB,X        ; store contents of ACCA to the $1004
        BSR   AKU            ; branch to AKU
        BRA   SCAN           ; branch to SCAN

SHORT   LDAA  #$05           ; load value #$05 into ACCA
        STAA  PORTB,X        ; store contents of ACCA to $1004
        BSR   DELAY          ; branch to DELAY
        BRA   SHORT          ; branch to SHORT

AKU     PSHA                 ; push ACCA onto stack
        PSHX                 ; push IX onto stack
        LDAA  #2             ; load the value of #02 into ACCA
RPT     LDX   #$FFFE         ; load IX register
RT      DEX                  ; decrement IX
        BNE   RT             ; not equal branch to RT
        DECA                 ; decrement A
        BNE   RPT            ; not equal branch to RPT
```

```
            PULX                ; pull IX from stack
            PULA                ; pull ACCA from stack
            RTS                 ; return to subroutine

DELAY       PSHA                ; push ACCA onto stack
            PSHX                ; push IX onto stack
            LDAA  #43           ; load the value of #43 into ACCA
REPEAT      LDX   #$FFFE        ; load IX register
REPT        DEX                 ; decrement IX
            BNE   REPT          ; not equal branch to REPT
            DECA                ; decrement A
            BNE   REPEAT        ; not equal branch to REPEAT
            PULX                ; pull IX from stack
            PULA                ; pull ACCA from stack
            RTS                 ; return to subroutine

            END                 ; end of programming
```

APPENDIX B

MC68HC11A8 CPU, Addressing Modes, and Instruction Set

CPU, ADDRESSING MODES, AND INSTRUCTION SET

This section provides a description of the CPU registers, addressing modes, and a Summary of the M68HC11 instruction set. Special operations such as subroutine calls and interrupts are described and cycle-by-cycle operations for all instructions are presented.

10.1 CPU Registers

In addition to being able to execute all M6800 and M6801 instructions, the MC68HC11A8 uses a 4-page opcode map to allow execution of 91 new opcodes Seven registers, discussed in the following paragraphs, are available to programmers as shown in **Figure 10-1**.

10.1.1 Accumulators A and B

Accumulator A and accumulator B are general-purpose 8-bit registers used to hold operands and results of arithmetic calculations or data manipulations. These two accumulators can be concatenated into a single 16-bit accumulator called the D accumulator.

10.1.2 Index Register X (IX)

The 16-bit IX register is used for indexed mode addressing. It provides a 16-bit indexing value which is added to an 8-bit offset provided in an instruction to create an effective address. The IX register can also be used as a counter or as a temporary storage register.

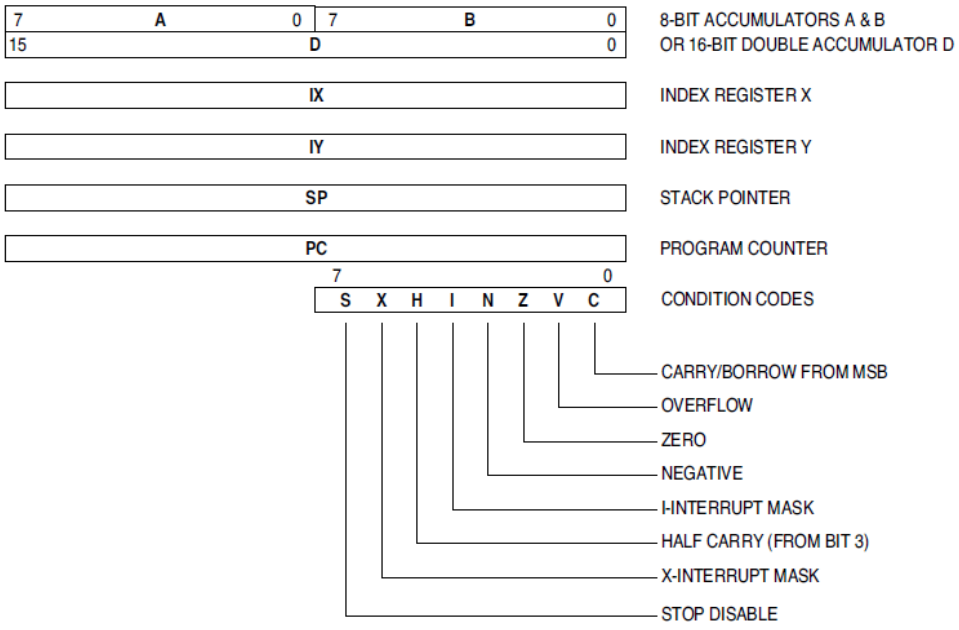


Figure 10-1 Programming Model

10.1.3 Index Register Y (IY)

The 16-bit IY register is also used for indexed mode addressing similar to the IX register; however, all instructions using the IY register require an extra byte of machine code and an extra cycle of execution time since they are two byte opcodes.

10.1.4 Stack Pointer (SP)

The stack pointer (SP) is a 16-bit register that contains the address of the next free location on the stack. The stack is configured as a sequence of last-in-first-out read/write registers which allow important data to be stored during interrupts and subroutine calls. Each time a new byte is added to the stack (a push instruction), the SP is decrement; whereas, each time a byte is removed from the stack (a pull instruction) the SP is incremented.

10.1.5 Program Counter (PC)

The program counter is a 16-bit register that contains the address of the next instruction to be executed.

10.1.6 Condition Code Register (CCR)

The condition code register is an 8-bit register in which each bit signifies the results of the instruction just executed. These bits can be individually tested by a program and a specific action can be taken as a result of the test. Each individual condition code register bit is explained below.

10.1.6.1 Carry/Borrow (C)

The C bit is set if there was a carry or borrow out of the arithmetic logic unit (ALU) during the last arithmetic operation. The C bit is also affected during shift and rotate instructions.

10.1.6.2 Overflow (V)

The overflow bit is set if there was an arithmetic overflow as a result of the operation; otherwise, the V bit is cleared.

10.1.6.3 Zero (Z)

The zero bit is set if the result of the last arithmetic, logic, or data manipulation operation was zero; otherwise, the Z bit is cleared.

10.1.6.4 Negative (N)

The negative bit is set if the result of the last arithmetic, logic, or data manipulation operation was negative; otherwise, the N bit is cleared. A result is said to be negative if its most significant bit is a one.

10.1.6.5 Interrupt Mask (I)

The interrupt mask bit is set either by hardware or program instruction to disable (mask) all maskable interrupt sources (both external and internal).

10.1.6.6 Half Carry (H)

The half carry bit is set to a logic one when a carry occurs between bits 3 and 4 of the arithmetic logic unit during an ADD, ABA, or ADC instruction; otherwise, the H bit is cleared.

10.1.6.7 X Interrupt Mask (X)

The X interrupt mask bit is set only by hardware (RESET or XIRQ acknowledge); and it is cleared only by program instruction (TAP or RTI).

10.1.6.8 Stop Disable (S)

The stop disable bit is set to disable the STOP instruction, and cleared to enable the STOP instruction. The S bit is program controlled. The STOP instruction is treated as no operation (NOP) if the S bit is set.

10.2 Addressing Modes

Six addressing modes can be used to reference memory; they include: immediate, direct, extended, indexed (with either of two 16-bit index registers and an 8-bit offset), inherent and relative. Some instructions require an additional byte before the opcode to accommodate a multi-page opcode map; this byte is called a prebyte. The following paragraphs provide a description of each addressing mode plus a discussion of the prebyte. In these descriptions the term effective address is used to indicate the address in memory from which the argument is fetched or stored, or from which execution is to proceed.

10.2.1 Immediate Addressing

In the immediate addressing mode, the actual argument is contained in the byte(s) immediately following the instruction, where the number of bytes matches the size of the register. These are two, three, or four (if prebyte is required) byte instructions.

10.2.2 Direct Addressing

In the direct addressing mode (sometimes called zero page addressing), the least significant byte of the operand address is contained in a single byte following the opcode and the most significant byte is assumed to be $00. Direct addressing allows the user to access $0000 through $00FF using two byte instructions and execution time is reduced by eliminating the additional memory access. In most applications, this 256-byte area is reserved for frequently referenced data. In the MC68HC11A8, software can configure the memory map so that internal RAM, and/or internal registers, or external memory space can occupy these addresses

10.2.3 Extended Addressing

In the extended addressing mode, the second and third bytes (following the opcode) contain the absolute address of the operand. These are three or four (if prebyte is required) byte instructions: one or two for the opcode, and two for the effective address.

10.2.4 Indexed Addressing

In the indexed addressing mode, one of the index registers (X or Y) is used in calculating the effective address. In this case, the effective address is variable and depends on two factors: 1) the current contents of the index register (X or Y) being used, and 2) the 8-bit unsigned offset contained in the instruction.This addressing mode allows referencing any memory location in the 64 Kbyte address space. These are usually two or three (if prebyte is required) byte instructions, the opcode plus the 8-bit offset.

10.2.5 Inherent Addressing

In the inherent addressing mode, all of the information is contained in the opcode. The operands (if any) are registers and no memory reference is required. These are usually one or two byte instructions.

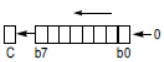
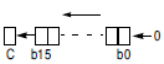
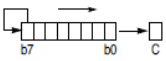
10.2.6 Relative Addressing

The relative addressing mode is used for branch instructions. If the branch condition is true, the contents of the 8-bit signed byte following the opcode (the offset) is added to the contents of the program counter to form the effective branch address; otherwise, control proceeds to the next instruction. These are usually two byte instructions.

10.3 Instruction Set

The central processing unit (CPU) in the MC68HC11A8 is basically a proper extension of the MC6801 CPU. In addition to its ability to execute all M6800 and M6801 instructions, the MC68HC11A8 CPU has a paged operation code (opcode) map with a total of 91 new opcodes. Major functional additions include a second 16-bit index register
(Y register), two types of 16-by-16 divide instructions, STOP and WAIT instructions, and bit manipulation instructions. **Table 10-1** shows all MC68HC11A8 instructions in all possible addressing modes. For each instruction, the operand construction is shown as well as the total number of machine code bytes and execution time in CPU E-clock cycles. Notes are provided at the end of **Table 10-1** which explain the letters in the Operand and Execution Time columns for some instructions.

Table 10-1 MC68HC11A8 Instructions, Addressing Modes, and Execution Times (Sheet 1 of 6)

Source Form(s)	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal)		Bytes	Cycle	Cycle by Cycle*	Condition Codes
				Opcode	Operand(s)				S X H I N Z V C
ABA	Add Accumulators	A + B → A	INH	1B		1	2	2-1	--↕-↕↕↕↕
ABX	Add B to X	IX + 00:B → IX	INH	3A		1	3	2-2	--------
ABY	Add B to Y	IY + 00:B → IY	INH	18 3A		2	4	2-4	--------
ADCA (opr)	Add with Carry to A	A + M + C → A	A IMM	89	ii	2	2	3-1	--↕-↕↕↕↕
			A DIR	99	dd	2	3	4-1	
			A EXT	B9	hh ll	3	4	5-2	
			A IND,X	A9	ff	2	4	6-2	
			A IND,Y	18 A9	ff	3	5	7-2	
ADCB (opr)	Add with Carry to B	B + M + C → B	B IMM	C9	ii	2	2	3-1	--↕-↕↕↕↕
			B DIR	D9	dd	2	3	4-1	
			B EXT	F9	hh ll	3	4	5-2	
			B IND,X	E9	ff	2	4	6-2	
			B IND,Y	18 E9	ff	3	5	7-2	
ADDA (opr)	Add Memory to A	A + M → A	A IMM	8B	ii	2	2	3-1	--↕-↕↕↕↕
			A DIR	9B	dd	2	3	4-1	
			A EXT	BB	hh ll	3	4	5-2	
			A IND,X	AB	ff	2	4	6-2	
			A IND,Y	18 AB	ff	3	5	7-2	
ADDB (opr)	Add Memory to B	B + M → B	B IMM	CB	ii	2	2	3-1	--↕-↕↕↕↕
			B DIR	DB	dd	2	3	4-1	
			B EXT	FB	hh ll	3	4	5-2	
			B IND,X	EB	ff	2	4	6-2	
			B IND,Y	18 EB	ff	3	5	7-2	
ADDD (opr)	Add 16-Bit to D	D + M:M + 1 → D	IMM	C3	jj kk	3	4	3-3	----↕↕↕↕
			DIR	D3	dd	2	5	4-7	
			EXT	F3	hh ll	3	6	5-10	
			IND,X	E3	ff	2	6	6-10	
			IND,Y	18 E3	ff	3	7	7-8	
ANDA (opr)	AND A with Memory	A•M → A	A IMM	84	ii	2	2	3-1	----↕↕0-
			A DIR	94	dd	2	3	4-1	
			A EXT	B4	hh ll	3	4	5-2	
			A IND,X	A4	ff	2	4	6-2	
			A IND,Y	18 A4	ff	3	5	7-2	
ANDB (opr)	AND B with Memory	B•M → B	B IMM	C4	ii	2	2	3-1	----↕↕0-
			B DIR	D4	dd	2	3	4-1	
			B EXT	F4	hh ll	3	4	5-2	
			B IND,X	E4	ff	2	4	6-2	
			B IND,Y	18 E4	ff	3	5	7-2	
ASL (opr)	Arithmetic Shift Left		EXT	78	hh ll	3	6	5-8	----↕↕↕↕
			IND,X	68	ff	2	6	6-3	
ASLA			IND,Y	18 68	ff	3	7	7-3	
			A INH	48		1	2	2-1	
ASLB			B INH	58		1	2	2-1	
ASLD	Arithmetic Shift Left Double		INH	05		1	3	2-2	----↕↕↕↕
ASR (opr)	Arithmetic Shift Right		EXT	77	hh ll	3	6	5-8	----↕↕↕↕
			IND,X	67	ff	2	6	6-3	
ASRA			IND,Y	18 67	ff	3	7	7-3	
			A INH	47		1	2	2-1	
ASRB			B INH	57		1	2	2-1	
BCC (rel)	Branch if Carry Clear	? C = 0	REL	24	rr	2	3	8-1	--------
BCLR (opr) (msk)	Clear Bit(s)	M•($\overline{mm}$) → M	DIR	15	dd mm	3	6	4-10	----↕↕0-
			IND,X	1D	ff mm	3	7	6-13	
			IND,Y	18 1D	ff mm	4	8	7-10	
BCS (rel)	Branch if Carry Set	? C = 1	REL	25	rr	2	3	8-1	--------
BEQ (rel)	Branch if = Zero	? Z = 1	REL	27	rr	2	3	8-1	--------
BGE (rel)	Branch if ≥ Zero	? N ⊕ V = 0	REL	2C	rr	2	3	8-1	--------
BGT (rel)	Branch if > Zero	? Z + (N ⊕ V) = 0	REL	2E	rr	2	3	8-1	--------
BHI (rel)	Branch if Higher	? C + Z = 0	REL	22	rr	2	3	8-1	--------
BHS (rel)	Branch if Higher or Same	? C = 0	REL	24	rr	2	3	8-1	--------

*Cycle-by-cycle number provides a reference to Tables 10-2 through 10-8 which detail cycle-by-cycle operation.
Example: Table 10-1 Cycle-by-Cycle column reference number 2-4 equals Table 10-2 line item 2-4.

Table 10-1 MC68HC11A8 Instructions, Addressing Modes, and Execution Times (Sheet 2 of 6)

Source Form(s)	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal)		Bytes	Cycle	Cycle by Cycle*	Condition Codes
				Opcode	Operand(s)				S X H I N Z V C
BITA (opr)	Bit(s) Test A with Memory	A•M	A IMM A DIR A EXT A IND,X A IND,Y	85 95 B5 A5 18 A5	ii dd hh ll ff ff	2 2 3 2 3	2 3 4 4 5	3-1 4-1 5-2 6-2 7-2	- - - - ↕ ↕ 0 -
BITB (opr)	Bit(s) Test B with Memory	B•M	B IMM B DIR B EXT B IND,X B IND,Y	C5 D5 F5 E5 18 E5	ii dd hh ll ff ff	2 2 3 2 3	2 3 4 4 5	3-1 4-1 5-2 6-2 7-2	- - - - ↕ ↕ 0 -
BLE (rel)	Branch if ≤ Zero	? Z + (N ⊕ V) = 1	REL	2F	rr	2	3	8-1	- - - - - - - -
BLO (rel)	Branch if Lower	? C = 1	REL	25	rr	2	3	8-1	- - - - - - - -
BLS (rel)	Branch if Lower or Same	? C + Z = 1	REL	23	rr	2	3	8-1	- - - - - - - -
BLT (rel)	Branch If < Zero	? N ⊕ V = 1	REL	2D	rr	2	3	8-1	- - - - - - - -
BMI (rel)	Branch if Minus	? N = 1	REL	2B	rr	2	3	8-1	- - - - - - - -
BNE (rel)	Branch if Not = Zero	? Z = 0	REL	26	rr	2	3	8-1	- - - - - - - -
BPL (rel)	Branch if Plus	? N = 0	REL	2A	rr	2	3	8-1	- - - - - - - -
BRA (rel)	Branch Always	? 1 = 1	REL	20	rr	2	3	8-1	- - - - - - - -
BRCLR(opr) (msk) (rel)	Branch if Bit(s) Clear	? M • mm = 0	DIR IND,X IND,Y	13 1F 18 1F	dd mm rr ff mm rr ff mm rr	4 4 5	6 7 8	4-11 6-14 7-11	- - - - - - - -
BRN (rel)	Branch Never	? 1 = 0	REL	21	rr	2	3	8-1	- - - - - - - -
BRSET(opr) (msk) (rel)	Branch if Bit(s) Set	? ($\overline{M}$) • mm = 0	DIR IND,X IND,Y	12 1E 18 1E	dd mm rr ff mm rr ff mm rr	4 4 5	6 7 8	4-11 6-14 7- 11	- - - - - - - -
BSET(opr) (msk)	Set Bit(s)	M + mm → M	DIR IND,X IND,Y	14 1C 18 1C	dd mm ff mm ff mm	3 3 4	6 7 8	4-10 6-13 7-10	- - - - ↕ ↕ 0 -
BSR (rel)	Branch to Subroutine	See Special Ops	REL	8D	rr	2	6	8-2	- - - - - - - -
BVC (rel)	Branch if Overflow Clear	? V = 0	REL	28	rr	2	3	8-1	- - - - - - - -
BVS (rel)	Branch if Overflow Set	? V = 1	REL	29	rr	2	3	8-1	- - - - - - - -
CBA	Compare A to B	A – B	INH	11		1	2	2-1	- - - - ↕ ↕ ↕ ↕
CLC	Clear Carry Bit	0 → C	INH	0C		1	2	2-1	- - - - - - - 0
CLI	Clear Interrupt Mask	0 → I	INH	0E		1	2	2-1	- - - 0 - - - -
CLR (opr)	Clear Memory Byte	0 → M	EXT IND,X IND,Y	7F 6F 18 6F	hh ll ff ff	3 2 3	6 6 7	5-8 6-3 7-3	- - - - 0 1 0 0
CLRA	Clear Accumulator A	0 → A	A INH	4F		1	2	2-1	- - - - 0 1 0 0
CLRB	Clear Accumulator B	0 → B	B INH	5F		1	2	2-1	- - - - 0 1 0 0
CLV	Clear Overflow Flag	0 → V	INH	0A		1	2	2-1	- - - - - - 0 -
CMPA (opr)	Compare A to Memory	A – M	A IMM A DIR A EXT A IND,X A IND,Y	81 91 B1 A1 18 A1	ii dd hh ll ff ff	2 2 3 2 3	2 3 4 4 5	3-1 4-1 5-2 6-2 7-2	- - - - ↕ ↕ ↕ ↕
CMPB (opr)	Compare B to Memory	B – M	B IMM B DIR B EXT B IND,X B IND,Y	C1 D1 F1 E1 18 E1	ii dd hh ll ff ff	2 2 3 2 3	2 3 4 4 5	3-1 4-1 5-2 6-2 7-2	- - - - ↕ ↕ ↕ ↕
COM (opr)	1's Complement Memory Byte	$FF – M → M	EXT IND,X IND,Y	73 63 18 63	hh ll ff ff	3 2 3	6 6 7	5-8 6-3 7-3	- - - - ↕ ↕ 0 1
COMA	1's Complement A	$FF – A → A	A INH	43		1	2	2-1	- - - - ↕ ↕ 0 1
COMB	1's Complement B	$FF – B → B	B INH	53		1	2	2-1	- - - - ↕ ↕ 0 1
CPD (opr)	Compare D to Memory 16-Bit	D – M:M + 1	IMM DIR EXT IND,X IND,Y	1A 83 1A 93 1A B3 1A A3 CD A3	jj kk dd hh ll ff ff	4 3 4 3 3	5 6 7 7 7	3-5 4-9 5-11 6-11 7-8	- - - - ↕ ↕ ↕ ↕

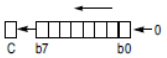
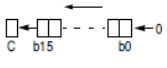
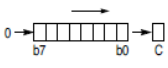
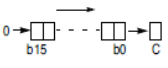
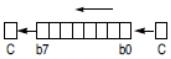
*Cycle-by-cycle number provides a reference to Tables 10-2 through 10-8 which detail cycle-by-cycle operation.
Example: Table 10-1 Cycle-by-Cycle column reference number 2-4 equals Table 10-2 line item 2-4.

Table 10-1 MC68HC11A8 Instructions, Addressing Modes, and Execution Times (Sheet 3 of 6)

Source Form(s)	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal)		Bytes	Cycle	Cycle by Cycle*	Condition Codes
				Opcode	Operand(s)				S X H I N Z V C
CPX (opr)	Compare X to Memory 16-Bit	IX – M:M + 1	IMM	8C	jj kk	3	4	3-3	- - - - ↕ ↕ ↕ ↕
			DIR	9C	dd	2	5	4-7	
			EXT	BC	hh ll	3	6	5-10	
			IND,X	AC	ff	2	6	6-10	
			IND,Y	CD AC	ff	3	7	7-8	
CPY (opr)	Compare Y to Memory 16-Bit	IY – M:M + 1	IMM	18 8C	jj kk	4	5	3-5	- - - - ↕ ↕ ↕ ↕
			DIR	18 9C	dd	3	6	4-9	
			EXT	18 BC	hh ll	4	7	5-11	
			IND,X	1A AC	ff	3	7	6-11	
			IND,Y	18 AC	ff	3	7	7-8	
DAA	Decimal Adjust A	Adjust Sum to BCD	INH	19		1	2	2-1	- - - - ↕ ↕ ↕ ↕
DEC (opr)	Decrement Memory Byte	M – 1 → M	EXT	7A	hh ll	3	6	5-8	- - - - ↕ ↕ ↕ -
			IND,X	6A	ff	2	6	6-3	
			IND,Y	18 6A	ff	3	7	7-3	
DECA	Decrement Accumulator A	A – 1 → A	A INH	4A		1	2	2-1	- - - - ↕ ↕ ↕ -
DECB	Decrement Accumulator B	B – 1 → B	B INH	5A		1	2	2-1	- - - - ↕ ↕ ↕ -
DES	Decrement Stack Pointer	SP – 1 → SP	INH	34		1	3	2-3	- - - - - - - -
DEX	Decrement Index Register X	IX – 1 → IX	INH	09		1	3	2-2	- - - - - ↕ - -
DEY	Decrement Index Register Y	IY – 1 → IY	INH	18 09		2	4	2-4	- - - - - ↕ - -
EORA (opr)	Exclusive OR A with Memory	A ⊕ M → A	A IMM	88	ii	2	2	3-1	- - - - ↕ ↕ 0 -
			A DIR	98	dd	2	3	4-1	
			A EXT	B8	hh ll	3	4	5-2	
			A IND,X	A8	ff	2	4	6-2	
			A IND,Y	18 A8	ff	3	5	7-2	
EORB (opr)	Exclusive OR B with Memory	B ⊕ M → B	B IMM	C8	ii	2	2	3-1	- - - - ↕ ↕ 0 -
			B DIR	D8	dd	2	3	4-1	
			B EXT	F8	hh ll	3	4	5-2	
			B IND,X	E8	ff	2	4	6-2	
			B IND,Y	18 E8	ff	3	5	7-2	
FDIV	Fractional Divide 16 by 16	D/IX → IX; r → D	INH	03		1	41	2-17	- - - - - ↕ ↕ ↕
IDIV	Integer Divide 16 by 16	D/IX → IX; r → D	INH	02		1	41	2-17	- - - - - ↕ 0 ↕
INC (opr)	Increment Memory Byte	M + 1 → M	EXT	7C	hh ll	3	6	5-8	- - - - ↕ ↕ ↕ -
			IND,X	6C	ff	2	6	6-3	
			IND,Y	18 6C	ff	3	7	7-3	
INCA	Increment Accumulator A	A + 1 → A	A INH	4C		1	2	2-1	- - - - ↕ ↕ ↕ -
INCB	Increment Accumulator B	B + 1 → B	B INH	5C		1	2	2-1	- - - - ↕ ↕ ↕ -
INS	Increment Stack Pointer	SP + 1 → SP	INH	31		1	3	2-3	- - - - - - - -
INX	Increment Index Register X	IX + 1 → IX	INH	08		1	3	2-2	- - - - - ↕ - -
INY	Increment Index Register Y	IY + 1 → IY	INH	18 08		2	4	2-4	- - - - - ↕ - -
JMP (opr)	Jump	See Special Ops	EXT	7E	hh ll	3	3	5-1	- - - - - - - -
			IND,X	6E	ff	2	3	6-1	
			IND,Y	18 6E	ff	3	4	7-1	
JSR (opr)	Jump to Subroutine	See Special Ops	DIR	9D	dd	2	5	4-8	- - - - - - - -
			EXT	BD	hh ll	3	6	5-12	
			IND,X	AD	ff	2	6	6-12	
			IND,Y	18 AD	ff	3	7	7-9	
LDAA (opr)	Load Accumulator A	M → A	A IMM	86	ii	2	2	3-1	- - - - ↕ ↕ 0 -
			A DIR	96	dd	2	3	4-1	
			A EXT	B6	hh ll	3	4	5-2	
			A IND,X	A6	ff	2	4	6-2	
			A IND,Y	18 A6	ff	3	5	7-2	
LDAB (opr)	Load Accumulator B	M → B	B IMM	C6	ii	2	2	3-1	- - - - ↕ ↕ 0 -
			B DIR	D6	dd	2	3	4-1	
			B EXT	F6	hh ll	3	4	5-2	
			B IND,X	E6	ff	2	4	6-2	
			B IND,Y	18 E6	ff	3	5	7-2	
LDD (opr)	Load Double Accumulator D	M → A,M + 1 → B	IMM	CC	jj kk	3	3	3-2	- - - - ↕ ↕ 0 -
			DIR	DC	dd	2	4	4-3	
			EXT	FC	hh ll	3	5	5-4	
			IND,X	EC	ff	2	5	6-6	
			IND,Y	18 EC	ff	3	6	7-6	

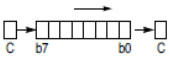
*Cycle-by-cycle number provides a reference to Tables 10-2 through 10-8 which detail cycle-by-cycle operation.
Example: Table 10-1 Cycle-by-Cycle column reference number 2-4 equals Table 10-2 line item 2-4.

Table 10-1 MC68HC11A8 Instructions, Addressing Modes, and Execution Times (Sheet 4 of 6)

Source Form(s)	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal)		Bytes	Cycle	Cycle by Cycle*	Condition Codes
				Opcode	Operand(s)				S X H I N Z V C
LDS (opr)	Load Stack Pointer	M:M + 1 → SP	IMM	8E	jj kk	3	3	3-2	- - - - ↕ ↕ 0 -
			DIR	9E	dd	2	4	4-3	
			EXT	BE	hh ll	3	5	5-4	
			IND,X	AE	ff	2	5	6-6	
			IND,Y	18 AE	ff	3	6	7-6	
LDX (opr)	Load Index Register X	M:M + 1 → IX	IMM	CE	jj kk	3	3	3-2	- - - - ↕ ↕ 0 -
			DIR	DE	dd	2	4	4-3	
			EXT	FE	hh ll	3	5	5-4	
			IND,X	EE	ff	2	5	6-6	
			IND,Y	CD EE	ff	3	6	7-6	
LDY (opr)	Load Index Register Y	M:M + 1 → IY	IMM	18 CE	jj kk	4	4	3-4	- - - - ↕ ↕ 0 -
			DIR	18 DE	dd	3	5	4-5	
			EXT	18 FE	hh ll	4	6	5-6	
			IND,X	1A EE	ff	3	6	6-7	
			IND,Y	18 EE	ff	3	6	7-6	
LSL (opr) LSLA LSLB	Logical Shift Left		EXT	78	hh ll	3	6	5-8	- - - - ↕ ↕ ↕ ↕
			IND,X	68	ff	2	6	6-3	
			IND,Y	18 68	ff	3	7	3-7	
			A INH	48		1	2	2-1	
			B INH	58		1	2	2-1	
LSLD	Logical Shift Left Double		INH	05		1	3	2-2	- - - - ↕ ↕ ↕ ↕
LSR (opr) LSRA LSRB	Logical Shift Right		EXT	74	hh ll	3	6	5-8	- - - - ↕ ↕ ↕ ↕
			IND,X	64	ff	2	6	6-3	
			IND,Y	18 64	ff	3	7	7-3	
			A INH	44		1	2	2-1	
			B INH	54		1	2	2-1	
LSRD	Logical Shift Right Double		INH	04		1	3	2-2	- - - - 0 ↕ ↕ ↕
MUL	Multiply 8 by 8	AxB → D	INH	3D		1	10	2-13	- - - - - - - ↕
NEG (opr)	2's Complement Memory Byte	0 – M → M	EXT	70	hh ll	3	6	5-8	- - - - ↕ ↕ ↕ ↕
			IND,X	60	ff	2	6	6-3	
			IND,Y	18 60	ff	3	7	7-3	
NEGA	2's Complement A	0 – A → A	A INH	40		1	2	2-1	- - - - ↕ ↕ ↕ ↕
NEGB	2's Complement B	0 – B → B	B INH	50		1	2	2-1	- - - - ↕ ↕ ↕ ↕
NOP	No Operation	No Operation	INH	01		1	2	2-1	- - - - - - - -
ORAA (opr)	OR Accumulator A (Inclusive)	A + M → A	A IMM	8A	ii	2	2	3-1	- - - - ↕ ↕ 0 -
			A DIR	9A	dd	2	3	4-1	
			A EXT	BA	hh ll	3	4	5-2	
			A IND,X	AA	ff	2	4	6-2	
			A IND,Y	18 AA	ff	3	5	7-2	
ORAB (opr)	OR Accumulator B (Inclusive)	B + M → B	B IMM	CA	ii	2	2	3-1	- - - - ↕ ↕ 0 -
			B DIR	DA	dd	2	3	4-1	
			B EXT	FA	hh ll	3	4	5-2	
			B IND,X	EA	ff	2	4	6-2	
			B IND,Y	18 EA	ff	3	5	7-2	
PSHA	Push A onto Stack	A → Stk, SP = SP–1	A INH	36		1	3	2-6	- - - - - - - -
PSHB	Push B onto Stack	B → Stk, SP = SP–1	B INH	37		1	3	2-6	- - - - - - - -
PSHX	Push X onto Stack (Lo First)	IX → Stk, SP = SP–2	INH	3C		1	4	2-7	- - - - - - - -
PSHY	Push Y onto Stack (Lo First)	IY → Stk, SP = SP–2	INH	18 3C		2	5	2-8	- - - - - - - -
PULA	Pull A from Stack	SP = SP + 1, A←Stk	A INH	32		1	4	2-9	- - - - - - - -
PULB	Pull B from Stack	SP = SP + 1, B←Stk	B INH	33		1	4	2-9	- - - - - - - -
PULX	Pull X from Stack (Hi First)	SP = SP + 2, IX←Stk	INH	38		1	5	2-10	- - - - - - - -
PULY	Pull Y from Stack (Hi First)	SP = SP + 2, IY←Stk	INH	18 38		2	6	2-11	- - - - - - - -
ROL (opr) ROLA ROLB	Rotate Left		EXT	79	hh ll	3	6	5-8	- - - - ↕ ↕ ↕ ↕
			IND,X	69	ff	2	6	6-3	
			IND,Y	18 69	ff	3	7	7-3	
			A INH	49		1	2	2-1	
			B INH	59		1	2	2-1	

*Cycle-by-cycle number provides a reference to Tables 10-2 through 10-8 which detail cycle-by-cycle operation.
Example: Table 10-1 Cycle-by-Cycle column reference number 2-4 equals Table 10-2 line item 2-4.

Table 10-1 MC68HC11A8 Instructions, Addressing Modes, and Execution Times (Sheet 5 of 6)

Source Form(s)	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal)		Bytes	Cycle	Cycle by Cycle*	Condition Codes
				Opcode	Operand(s)				S X H I N Z V C
ROR (opr) RORA RORB	Rotate Right		EXT IND,X IND,Y A INH B INH	76 66 18 66 46 56	hh ll ff ff	3 2 3 1 1	6 6 7 2 2	5-8 6-3 7-3 2-1 2-1	- - - - ↕ ↕ ↕ ↕
RTI	Return from Interrupt	See Special Ops	INH	3B		1	12	2-14	↕ ↕ ↕ ↕ ↕ ↕ ↕ ↕
RTS	Return from Subroutine	See Special Ops	INH	39		1	5	2-12	- - - - - - - -
SBA	Subtract B from A	A – B → A	INH	10		1	2	2-1	- - - - ↕ ↕ ↕ ↕
SBCA (opr)	Subtract with Carry from A	A – M – C → A	A IMM A DIR A EXT A IND,X A IND,Y	82 92 B2 A2 18 A2	ii dd hh ll ff ff	2 2 3 2 3	2 3 4 4 5	3-1 4-1 5-2 6-2 7-2	- - - - ↕ ↕ ↕ ↕
SBCB (opr)	Subtract with Carry from B	B – M – C → B	B IMM B DIR B EXT B IND,X B IND,Y	C2 D2 F2 E2 18 E2	ii dd hh ll ff ff	2 2 3 2 3	2 3 4 4 5	3-1 4-1 5-2 6-2 7-2	- - - - ↕ ↕ ↕ ↕
SEC	Set Carry	1 → C	INH	0D		1	2	2-1	- - - - - - - 1
SEI	Set Interrupt Mask	1 → I	INH	0F		1	2	2-1	- - - 1 - - - -
SEV	Set Overflow Flag	1 → V	INH	0B		1	2	2-1	- - - - - - 1 -
STAA (opr)	Store Accumulator A	A → M	A DIR A EXT A IND,X A IND,Y	97 B7 A7 18 A7	dd hh ll ff ff	2 3 2 3	3 4 4 5	4-2 5-3 6-5 7-5	- - - - ↕ ↕ 0 -
STAB (opr)	Store Accumulator B	B → M	B DIR B EXT B IND,X B IND,Y	D7 F7 E7 18 E7	dd hh ll ff ff	2 3 2 3	3 4 4 5	4-2 5-3 6-5 7-5	- - - - ↕ ↕ 0 -
STD (opr)	Store Accumulator D	A → M, B → M + 1	DIR EXT IND,X IND,Y	DD FD ED 18 ED	dd hh ll ff ff	2 3 2 3	4 5 5 6	4-4 5-5 6-8 7-7	- - - - ↕ ↕ 0 -
STOP	Stop Internal Clocks		INH	CF		1	2	2-1	- - - - - - - -
STS (opr)	Store Stack Pointer	SP → M:M + 1	DIR EXT IND,X IND,Y	9F BF AF 18 AF	dd hh ll ff ff	2 3 2 3	4 5 5 6	4-4 5-5 6-8 7-7	- - - - ↕ ↕ 0 -
STX (opr)	Store Index Register X	IX → M:M + 1	DIR EXT IND,X IND,Y	DF FF EF CD EF	dd hh ll ff ff	2 3 2 3	4 5 5 6	4-4 5-5 6-8 7-7	- - - - ↕ ↕ 0 -
STY (opr)	Store Index Register Y	IY → M:M + 1	DIR EXT IND,X IND,Y	18 DF 18 FF 1A EF 18 EF	dd hh ll ff ff	3 4 3 3	5 6 6 6	4-6 5-7 6-9 7-7	- - - - ↕ ↕ 0 -
SUBA (opr)	Subtract Memory from A	A – M → A	A IMM A DIR A EXT A IND,X A IND,Y	80 90 B0 A0 18 A0	ii dd hh ll ff ff	2 2 3 2 3	2 3 4 4 5	3-1 4-1 5-2 6-2 7-2	- - - - ↕ ↕ ↕ ↕
SUBB (opr)	Subtract Memory from B	B – M → B	B IMM B DIR B EXT B IND,X B IND,Y	C0 D0 F0 E0 18 E0	ii dd hh ll ff ff	2 2 3 2 3	2 3 4 4 5	3-1 4-1 5-2 6-2 7-2	- - - - ↕ ↕ ↕ ↕
SUBD (opr)	Subtract Memory from D	D – M:M + 1→ D	IMM DIR EXT IND,X IND,Y	83 93 B3 A3 18 A3	jj kk dd hh ll ff ff	3 2 3 2 3	4 5 6 6 7	3-3 4-7 5-10 6-10 7-8	- - - - ↕ ↕ ↕ ↕
SWI	Software Interrupt	See Special Ops	INH	3F		1	14	2-15	- - - 1 - - - -
TAB	Transfer A to B	A → B	INH	16		1	2	2-1	- - - - ↕ ↕ 0 -
TAP	Transfer A to CC Register	A → CCR	INH	06		1	2	2-1	↕ ↕ ↕ ↕ ↕ ↕ ↕ ↕
TBA	Transfer B to A	B → A	INH	17		1	2	2-1	- - - - ↕ ↕ 0 -

*Cycle-by-cycle number provides a reference to Tables 10-2 through 10-8 which detail cycle-by-cycle operation.
Example: Table 10-1 Cycle-by-Cycle column reference number 2-4 equals Table 10-2 line item 2-4.

Table 10-1 MC68HC11A8 Instructions, Addressing Modes, and Execution Times (Sheet 6 of 6)

Source Form(s)	Operation	Boolean Expression	Addressing Mode for Operand	Machine Coding (Hexadecimal)		Bytes	Cycle	Cycle by Cycle*	Condition Codes
				Opcode	Operand(s)				S X H I N Z V C
TEST	TEST (Only in Test Modes)	Address Bus Counts	INH	00		1	**	2-20	- - - - - - - -
TPA	Transfer CC Register to A	CCR → A	INH	07		1	2	2-1	- - - - - - - -
TST (opr)	Test for Zero or Minus	M – 0	EXT IND,X IND,Y	7D 6D 18 6D	hh ll ff ff	3 2 3	6 6 7	5-9 6-4 7-4	- - - - ↕ ↕ 0 0
TSTA		A – 0	A INH	4D		1	2	2-1	- - - - ↕ ↕ 0 0
TSTB		B – 0	B INH	5D		1	2	2-1	- - - - ↕ ↕ 0 0
TSX	Transfer Stack Pointer to X	SP + 1 → IX	INH	30		1	3	2-3	- - - - - - - -
TSY	Transfer Stack Pointer to Y	SP + 1 → IY	INH	18 30		2	4	2-5	- - - - - - - -
TXS	Transfer X to Stack Pointer	IX – 1 → SP	INH	35		1	3	2-2	- - - - - - - -
TYS	Transfer Y to Stack Pointer	IY – 1 → SP	INH	18 35		2	4	2-4	- - - - - - - -
WAI	Wait for Interrupt	Stack Regs & WAIT	INH	3E		1	***	2-16	- - - - - - - -
XGDX	Exchange D with X	IX → D, D → IX	INH	8F		1	3	2-2	- - - - - - - -
XGDY	Exchange D with Y	IY → D, D → IY	INH	18 8F		2	4	2-4	- - - - - - - -

*Cycle-by-cycle number provides a reference to Tables 10-2 through 10-8 which detail cycle-by-cycle operation.
Example: Table 10-1 Cycle-by-Cycle column reference number 2-4 equals Table 10-2 line item 2-4.

**Infinity or Until Reset Occurs

***12 Cycles are used beginning with the opcode fetch. A wait state is entered which remains in effect for an integer number of MPU E-clock cycles (n) until an interrupt is recognized. Finally, two additional cycles are used to fetch the appropriate interrupt vector (14 + n total).

dd = 8-Bit Direct Address ($0000 –$00FF) (High Byte Assumed to be $00)
ff = 8-Bit Positive Offset $00 (0) to $FF (255) (Is Added to Index)
hh = High Order Byte of 16-Bit Extended Address
ii = One Byte of Immediate Data
jj = High Order Byte of 16-Bit Immediate Data
kk = Low Order Byte of 16-Bit Immediate Data
ll = Low Order Byte of 16-Bit Extended Address
mm = 8-Bit Bit Mask (Set Bits to be Affected)
rr = Signed Relative Offset $80 (– 128) to $7F (+ 127)
(Offset Relative to the Address Following the Machine Code Offset Byte)

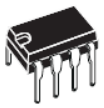
APPENDIX C

UA741 Op-Amp Datasheet

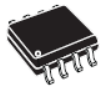
UA741

GENERAL PURPOSE SINGLE OPERATIONAL AMPLIFIER

- LARGE INPUT VOLTAGE RANGE
- NO LATCH-UP
- HIGH GAIN
- SHORT-CIRCUIT PROTECTION
- NO FREQUENCY COMPENSATION
- REQUIRED
- SAME PIN CONFIGURATION AS THE UA709



N
DIP8
(Plastic Package)



D
SO8
(Plastic Micropackage)

DESCRIPTION

The UA741 is a high performance monolithic operational amplifier constructed on a single silicon chip. It is intented for a wide range of analog applications.

- Summing amplifier
- Voltage follower
- Integrator
- Active filter
- Function generator

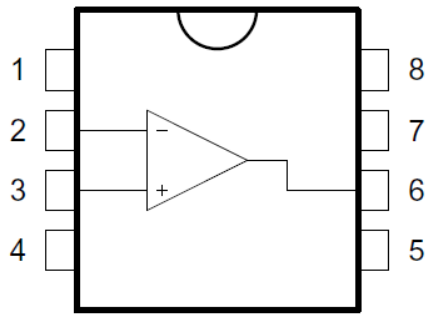
The high gain and wide range of operating voltages provide superior performances in integrator, summing amplifier and general feedback applications. The internal compensation network (6dB/ octave) insures stability in closed loop circuits.

ORDER CODE

Part Number	Temperature Range	Package	
		N	D
UA741C	0°C, +70°C	•	•
UA741I	-40°C, +105°C	•	•
UA741M	-55°C, +125°C	•	•
Example : UA741CN			

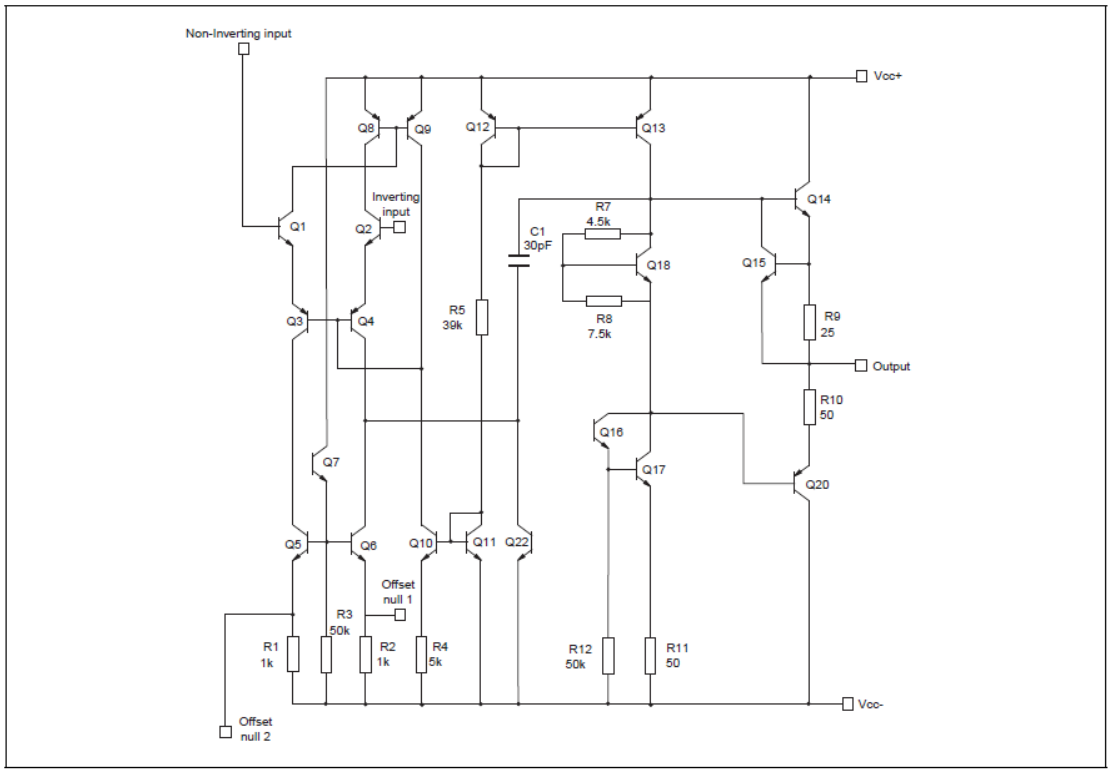
N = Dual in Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)

PIN CONNECTIONS (top view)



1 - Offset null 1
2 - Inverting input
3 - Non-inverting input
4 - V_{CC}^-
5 - Offset null 2
6 - Output
7 - V_{CC}^+
8 - N.C.

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	UA741M	UA741I	UA741C	Unit
V_{CC}	Supply voltage	±22			V
V_{id}	Differential Input Voltage	±30			V
V_i	Input Voltage	±15			V
P_{tot}	Power Dissipation [1)]	500			mW
	Output Short-circuit Duration	Infinite			
T_{oper}	Operating Free-air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to +150			°C

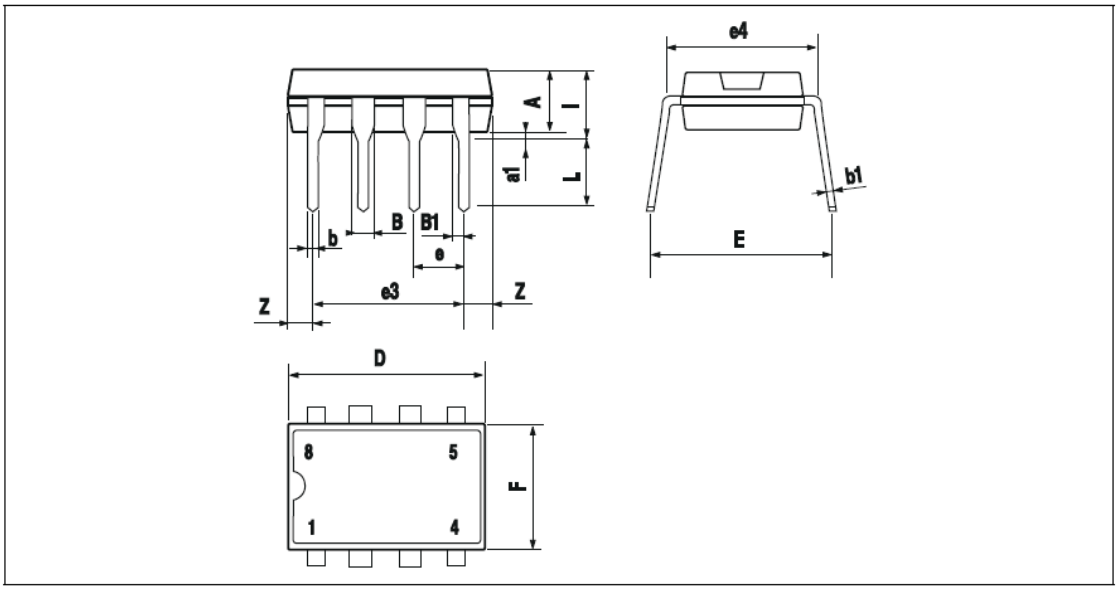
1. Power dissipation must be considered to ensure maximum junction temperature (Tj) is not exceeded.

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage ($R_s \leq 10k\Omega$) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$		1	5 6	mV
I_{io}	Input Offset Current T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$		2	30 70	nA
I_{ib}	Input Bias Current T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$		10	100 200	nA
A_{vd}	Large Signal Voltage Gain (V_o = ±10V, R_L = 2kΩ) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	 50 25	200		V/mV
SVR	Supply Voltage Rejection Ratio ($R_s \leq 10k\Omega$) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	 77 77	90		dB
I_{CC}	Supply Current, no load T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$		1.7	2.8 3.3	mA
V_{icm}	Input Common Mode Voltage Range T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	 ±12 ±12			V
CMR	Common Mode Rejection Ratio ($R_S \leq 10k\Omega$) T_{amb} = +25°C $T_{min} \leq T_{amb} \leq T_{max}$	 70 70	90		dB
I_{OS}	Output short Circuit Current	10	25	40	mA
$\pm V_{opp}$	Output Voltage Swing T_{amb} = +25°C R_L = 10kΩ R_L = 2kΩ $T_{min} \leq T_{amb} \leq T_{max}$ R_L = 10kΩ R_L = 2kΩ	 12 10 12 10	 14 13		V
SR	Slew Rate V_i = ±10V, R_L = 2kΩ, C_L = 100pF, unity Gain	0.25	0.5		V/µs
t_r	Rise Time V_i = ±20mV, R_L = 2kΩ, C_L = 100pF, unity Gain		0.3		µs
K_{ov}	Overshoot V_i = 20mV, R_L = 2kΩ, C_L = 100pF, unity Gain		5		%
R_i	Input Resistance	0.3	2		MΩ
GBP	Gain Bandwith Product V_i = 10mV, R_L = 2kΩ, C_L = 100pF, f =100kHz	0.7	1		MHz
THD	Total Harmonic Distortion f = 1kHz, A_v = 20dB, R_L = 2kΩ, V_o = $2V_{pp}$, C_L = 100pF, T_{amb} = +25°C		0.06		%
e_n	Equivalent Input Noise Voltage f = 1kHz, R_s = 100Ω		23		$\frac{nV}{\sqrt{Hz}}$
Øm	Phase Margin		50		Degrees

PACKAGE MECHANICAL DATA
8 PINS - PLASTIC DIP



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
i			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

APPENDIX D

BD681 Datasheet

SGS-THOMSON MICROELECTRONICS

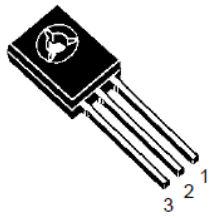
BD677/A/679/A/681
BD678/A/680/A/682

COMPLEMENTARY SILICON POWER DARLINGTON TRANSISTORS

- SGS-THOMSON PREFERRED SALESTYPES
- COMPLEMENTARY PNP - NPN DEVICES
- MONOLITHIC DARLINGTON CONFIGURATION
- INTEGRATED ANTIPARALLEL COLLECTOR-EMITTER DIODE

APPLICATION

- LINEAR AND SWITCHING INDUSTRIAL EQUIPMENT



SOT-32

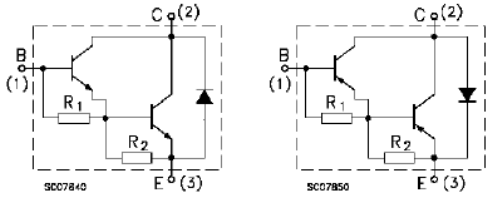
DESCRIPTION

The BD677, BD677A, BD679, BD679A and BD681 are silicon epitaxial-base NPN power transistors in monolithic Darlington configuration mounted in Jedec SOT-32 plastic package.

They are intended for use in medium power linar and switching applications

The complementary PNP types are BD678, BD678A, BD680, BD680A and BD682 respectively.

INTERNAL SCHEMATIC DIAGRAM



R_1 Typ.= 7K Ω R_2 Typ.= 230 Ω

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value			Unit
		NPN	BD677/A	BD679/A	BD681	
		PNP	BD678/A	BD680/A	BD682	
V_{CBO}	Collector-Base Voltage (I_E = 0)		60	80	100	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)		60	80	100	V
V_{EBO}	Emitter-Base Voltage (I_C = 0)		5			V
I_C	Collector Current		4			A
I_{CM}	Collector Peak Current		6			A
I_B	Base Current		0.1			A
P_{tot}	Total Dissipation at $T_c \leq 25$ °C		40			W
T_{stg}	Storage Temperature		-65 to 150			°C
T_j	Max. Operating Junction Temperature		150			°C

For PNP types voltage and current values are negative.

THERMAL DATA

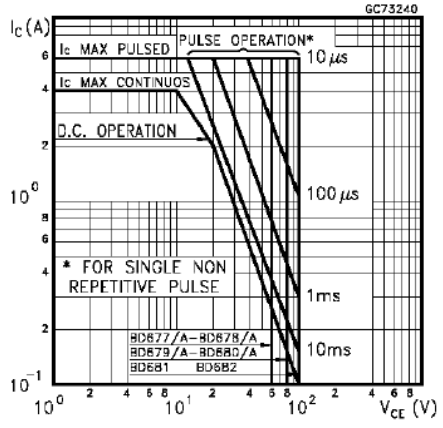
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	3.12	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

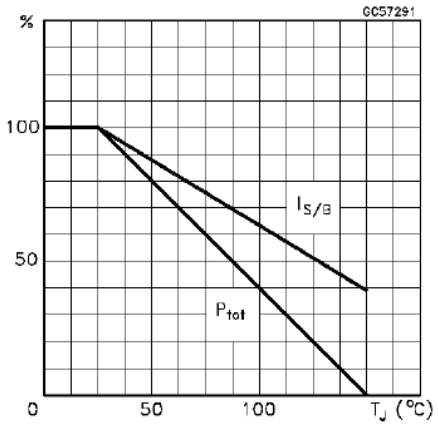
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector Cut-off Current (I_E = 0)	V_{CE} = rated V_{CBO} V_{CE} = rated V_{CBO} T_C = 100 °C			0.2 2	mA mA
I_{CEO}	Collector Cut-off Current (I_B = 0)	V_{CE} = half rated V_{CEO}			0.5	mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5 V			2	mA
$V_{CEO(sus)}$*	Collector-Emitter Sustaining Voltage	I_C = 50 mA for **BD677/677A/678/678A** for **BD679/679A/680/680A** for **BD681/682**	 60 80 100			 V V V
$V_{CE(sat)}$*	Collector-Emitter Saturation Voltage	for **BD677/678/679/680/681/682** I_C = 1.5 A I_B = 30 mA for **BD677A/678A/679A/680A** I_C = 2 A I_B = 40 mA			 2.5 2.8	 V V
V_{BE}*	Base-Emitter Voltage	for **BD677/678/679/680/681/682** I_C = 1.5 A V_{CE} = 3 V for **BD677A/678A/679A/680A** I_C = 2 A V_{CE} = 3 V			 2.5 2.5	 V V
h_{FE}*	DC Current Gain	for **BD677/678/679/680/681/682** I_C = 1.5 A V_{CE} = 3 V for **BD677A/678A/679A/680A** I_C = 2 A V_{CE} = 3 V	 750 750			
h_{fe}	Small Signal Current Gain	I_C = 1.5 A V_{CE} = 3 V f = 1MHz	1			

* Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

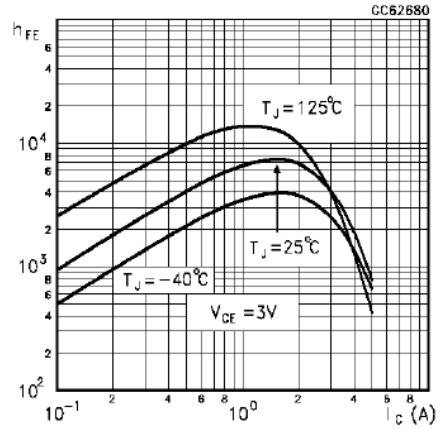
Safe Operating Areas



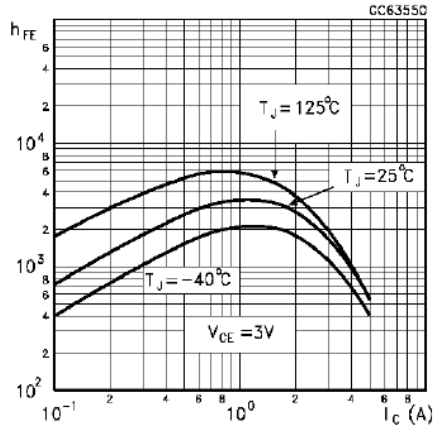
Derating Curve



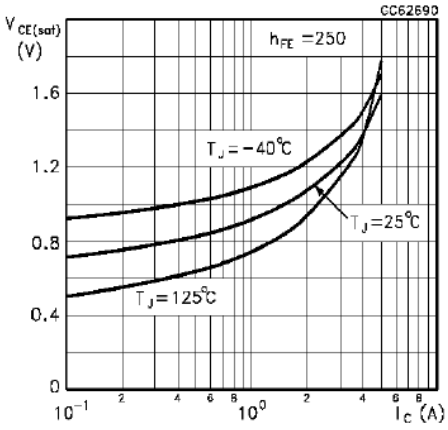
DC Current Gain (NPN type)



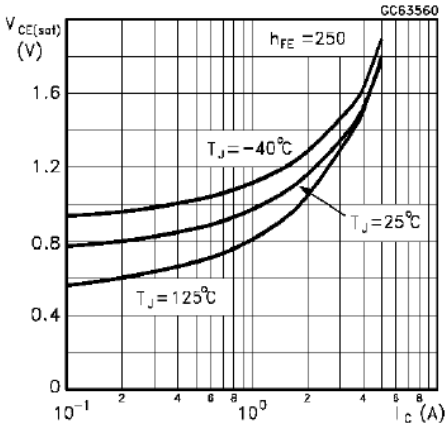
DC Current Gain (PNP type)



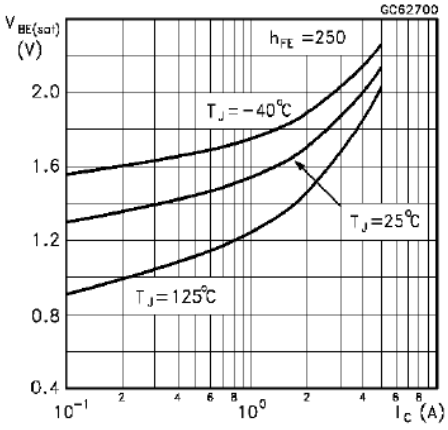
Collector-Emitter Saturation Voltage (NPN type)



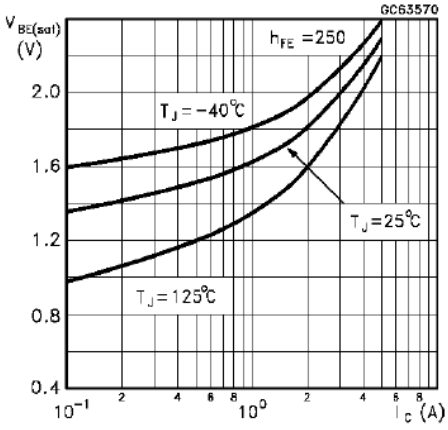
Collector-Emitter Saturation Voltage (PNP type)



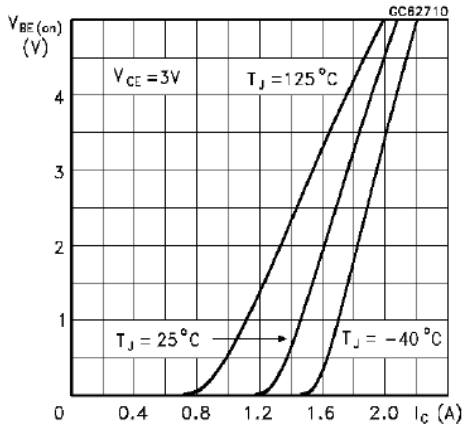
Base-Emitter Saturation Voltage (NPN type)



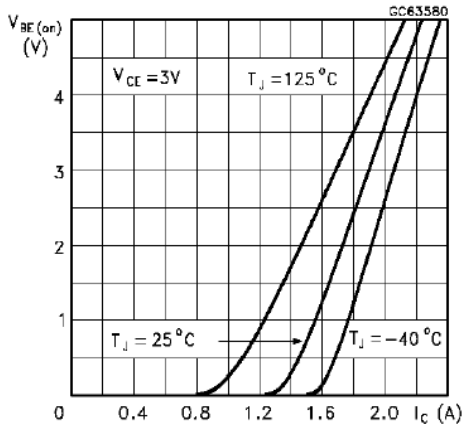
Base-Emitter Saturation Voltage (PNP type)



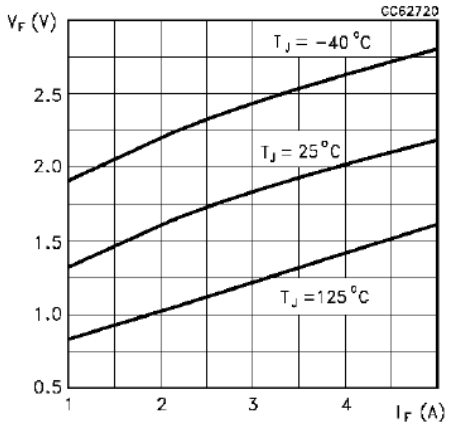
Base-Emitter On Voltage (NPN type)



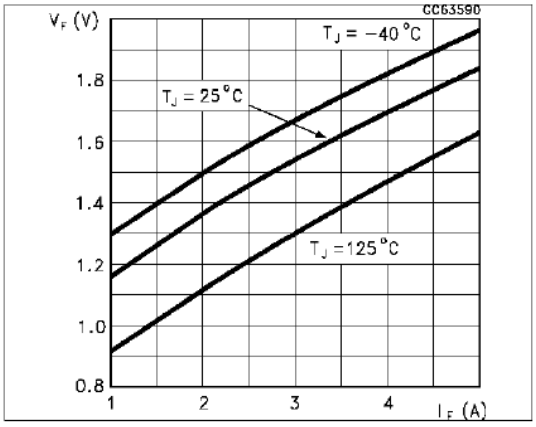
Base-Emitter On Voltage (PNP type)



Freewheel Diode Forward Voltage (NPN types)

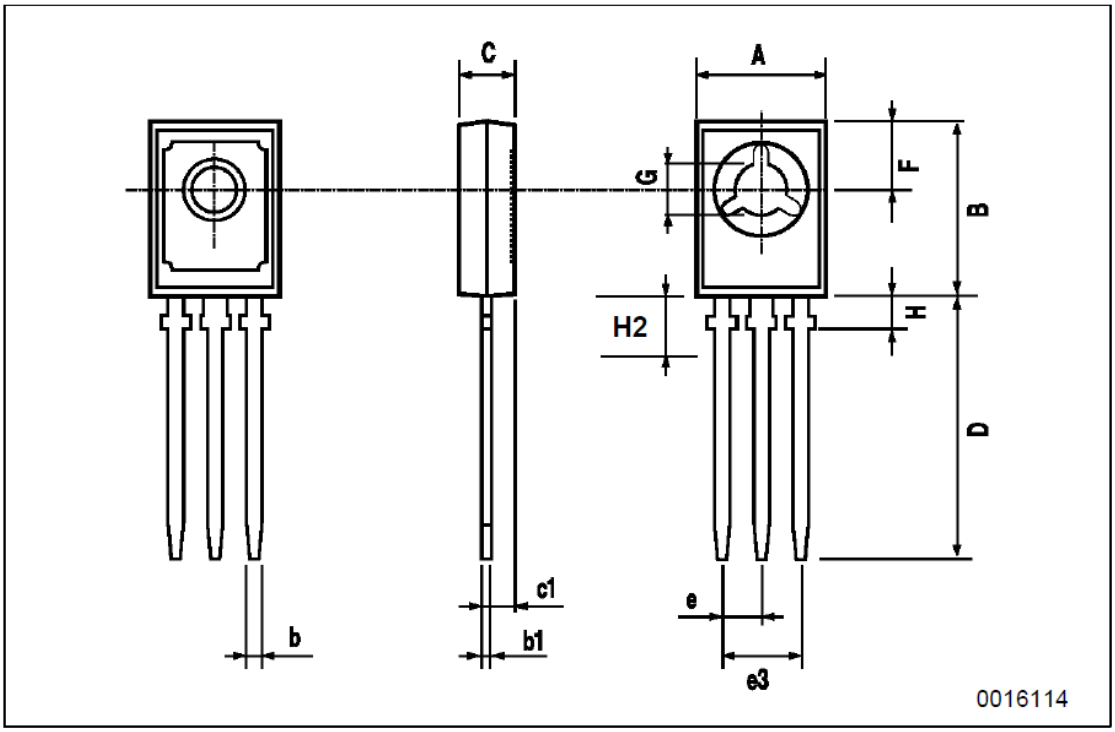


Freewheel Diode Forward Voltage (PNP types)



SOT-32 (TO-126) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	7.4		7.8	0.291		0.307
B	10.5		10.8	0.413		0.445
b	0.7		0.9	0.028		0.035
b1	0.49		0.75	0.019		0.030
C	2.4		2.7	0.040		0.106
c1	1.0		1.3	0.039		0.050
D	15.4		16.0	0.606		0.629
e		2.2			0.087	
e3	4.15		4.65	0.163		0.183
F		3.8			0.150	
G	3		3.2	0.118		0.126
H			2.54			0.100
H2		2.15			0.084	



APPENDIX E

Heavy Duty Power Relay G7L-1A-T Datasheet

■ Coil Ratings

Rated voltage		Rated current	Coil resistance	Must operate voltage	Must release voltage	Max. voltage	Power consumption (approx.)
AC (~)	12 V	142 mA	---	75% max. of rated voltage	15% min. of rated voltage	110% of rated voltage	1.7 to 2.5 VA (60 Hz)
	24 V	71 mA	---				
	50 V	34 mA	---				
	100 to 120 V	17.0 to 20.4 mA	---	75 V	18 V	132 V	
	200 to 240 V	8.5 to 10.2 mA	---	150 V	36 V	264 v	
DC (=)	6 V	317 mA	18.9 Ω	75% max. of rated voltage	15% min. of rated voltage	110% of rated voltage	1.9 W
	12 V	158 mA	75 Ω				
	24 V	79 mA	303 Ω				
	48 V	40 mA	1220 Ω				
	100 V	19 mA	5260 Ω				

Note: 1. The rated current and coil resistance are measured at a coil temperature of 23°C with tolerances of +15%/–20% for AC rated current and ±15% for DC coil resistance.

2. Performance characteristic data are measured at a coil temperature of 23°C.

3. ~ indicates AC and = indicates DC (IEC417 publications).

■ Contact Ratings

Model	G7L-1A-T j /G7L-1A-B j		G7L-2A-T j /G7L-2A-B j		G7L-1A-P/G7L-2A-P	
	Resistive load (cosϕ = 1)	Inductive load (cosϕ = 0.4)	Resistive load (cosϕ = 1)	Inductive load (cosϕ = 0.4)	Resistive load (cosϕ = 1)	Inductive load (cosϕ = 0.4)
Rated load	30 A, 220 VAC (~)	25 A, 220 VAC (~)	25 A, 220 VAC (~)		20 A, 220 VAC (~)	
Rated carry current	30 A		25 A		20 A	
Max. switching voltage	250 VAC (~)					
Max. switching current	30 A		25 A		20 A	
Max. switching power	6,600 VAC (~)	5,500 VAC (~)	5,500 VAC (~)		4,400 VAC (~)	
Min. permissible load*	100 mA, 5 VDC (=)					

***Note:** P level: $\lambda_{60} = 0.1 \times 10^{-6}$/operation

■ Characteristics

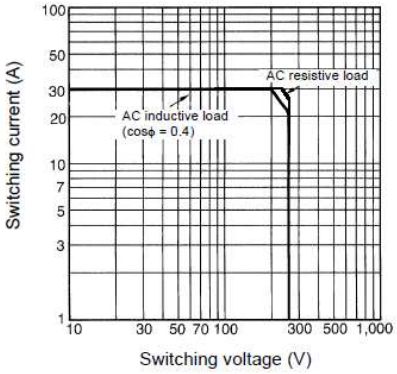
Contact resistance	50 mΩ max.
Operate time	30 ms max.
Release time	30 ms max.
Max. operating frequency	Mechanical: 1,800 operations/hr Electrical: 1,800 operations/hr (under rated load)
Insulation resistance	1,000 MΩ min. (at 500 VDC)
Dielectric strength	4,000 VAC min., 50/60 Hz for 1 min between coil and contacts 2,000 VAC, 50/60 Hz for 1 min between contacts of same polarity 2,000 VAC, 50/60 Hz for 1 min between contacts of different polarity (DPST-NO model)
Impulse withstand voltage	10,000 V between coil and contact (with 1.2 x 50 μs impulse wave)
Vibration resistance	Destruction: 10 to 55 Hz, 1.5-mm double amplitude Malfunction: 10 to 55 Hz, 1.5-mm double amplitude
Shock resistance	Destruction: 1,000 m/s^2 Malfunction: 100 m/s^2
Life expectancy	Mechanical: 1,000,000 operations min. (at 1,800 operations/hr) Electrical: 100,000 operations min. (at 1,800 operations/hr under rated load)
Ambient temperature	Operating: –25°C to 60°C (with no icing)
Ambient humidity	Operating: 35% to 85%
Weight	Quick-connect terminal models: approx. 90 g PCB terminal models: approx. 100 g Screw terminal models: approx. 120 g

Note: The values given above are initial values.

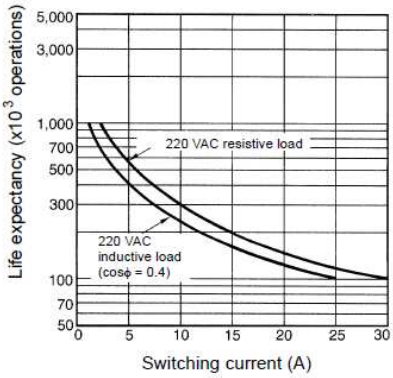
Engineering Data

G7L-1A-T/G7L-1A-B

Maximum Switching Power

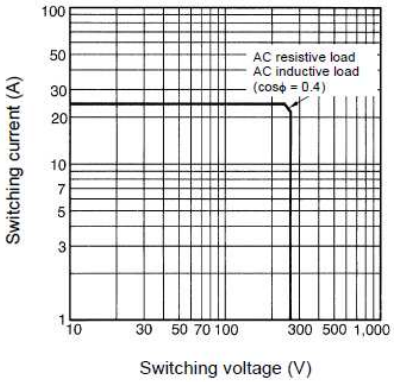


Life Expectancy

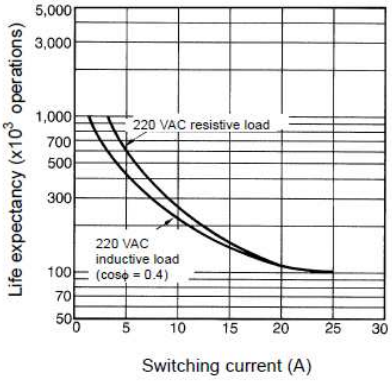


G7L-2A-T/G7L-2A-B

Maximum Switching Power

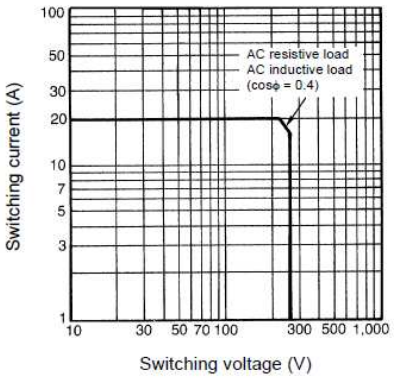


Life Expectancy

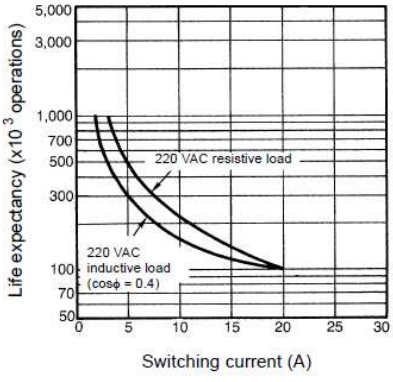


G7L-1A-P/G7L-2A-P

Maximum Switching Power



Life Expectancy



■ Approved by Standards

UL 508, 1950 Recognitions (File No. E41643)
CSA 22.2 No.14 Listings (File No.LR35535)

Model	Contact Form	Coil ratings	Contact ratings	Operations
G7L-1A-T j G7L-1A-B j	SPST-NO	12 to 240 VAC 5 to 220 VDC	30 A, 277 VAC (RES) 25 A, 277 VAC (GEN) 30 A, 120 VAC (GEN)	100 x 10^3
			1.5 kW, 120 VAC (T) 1.5 HP, 120 VAC	6 x 10^3
			3 HP, 277 VAC	100 x 10^3 (CSA; 6 x 10^3)
			20 FLA/120 LRA, 120 VAC 17 FLA/102 LRA, 265 VAC	30 x 10^3
			TV-10, 120 VAC	25 x 10^3
G7L-2A-T j G7L-2A-B j	DPST-NO		25 A, 277 VAC (RES) 25 A, 277 VAC (GEN) 25 A, 120 VAC (GEN)	100 x 10^3
			1.3 kW, 120 VAC (T) 1 HP, 120 VAC	6 x 10^3
			2 HP, 277 VAC	100 x 10^3 (CSA; 6 x 10^3)
			20 FLA/120 LRA, 120 VAC 17 FLA/102 LRA, 265 VAC	30 x 10^3
			TV-8, 120 VAC	25 x 10^3
G7L-1A-P	SPST-NO		20 A, 277 VAC (RES) 20 A, 277 VAC (GEN) 20 A, 120 VAC (GEN)	100 x 10^3
			1.5 kW, 120 VAC (T) 1.5 HP, 120 VAC	6 x 10^3
			3 HP, 277 VAC	100 x 10^3 (CSA; 6 x 10^3)
			20 FLA/120 LRA, 120 VAC 17 FLA/102 LRA, 265 VAC	30 x 10^3
			TV-10, 120 VAC	25 x 10^3
G7L-2A-P	DPST-NO		20 A, 277 VAC (RES) 20 A, 277 VAC (GEN) 20 A, 120 VAC (GEN)	100 x 10^3
			1.3 kW, 120 VAC (T) 1 HP, 120 VAC	6 x 10^3
			2 HP, 277 VAC	100 x 10^3
			20 FLA/120 LRA, 120 VAC 17 FLA/102 LRA, 265 VAC	30 x 10^3
			TV-8, 120 VAC	25 x 10^3

TÜV: File No. R9051158 (VDE 0435, IEC 255, IEC 950, EN60950)

Model	Contact Form	Coil ratings	Contact ratings	Operations
G7L-1A-B j	SPST-NO	6, 12, 24, 48, 100, 110, 200, 220 VDC 12, 24, 50, 100 to 120, 200 to 240 VAC	30 A, 240 VAC ($\cos\phi$=1.0) 25 A, 240 VAC ($\cos\phi$=0.4) 30 A, 120 VAC ($\cos\phi$=0.4)	100 x 10^3
G7L-2A-B j	DPST-NO		25 A, 240 VAC ($\cos\phi$=1.0) 25 A, 240 VAC ($\cos\phi$=0.4)	
G7L-1A-T j	SPST-NO		25 A, 240 VAC ($\cos\phi$=1.0) 25 A, 240 VAC ($\cos\phi$=0.4)	
G7L-2A-T j	DPST-NO		25 A, 240 VAC ($\cos\phi$=1.0) 25 A, 240 VAC ($\cos\phi$=0.4)	
G7L-1A-P	SPST-NO		20 A, 240 VAC ($\cos\phi$=1.0) 20 A, 240 VAC ($\cos\phi$=0.4)	
G7L-2A-P	DPST-NO		20 A, 240 VAC ($\cos\phi$=1.0) 20 A, 240 VAC ($\cos\phi$=0.4)	

APPENDIX F

AR-ELCB Hardware Picture

Figure A1: Auto Re-closer Earth Leakage Circuit Breaker (AR-ELCB).

Figure A2: Output port for AR-ELCB.

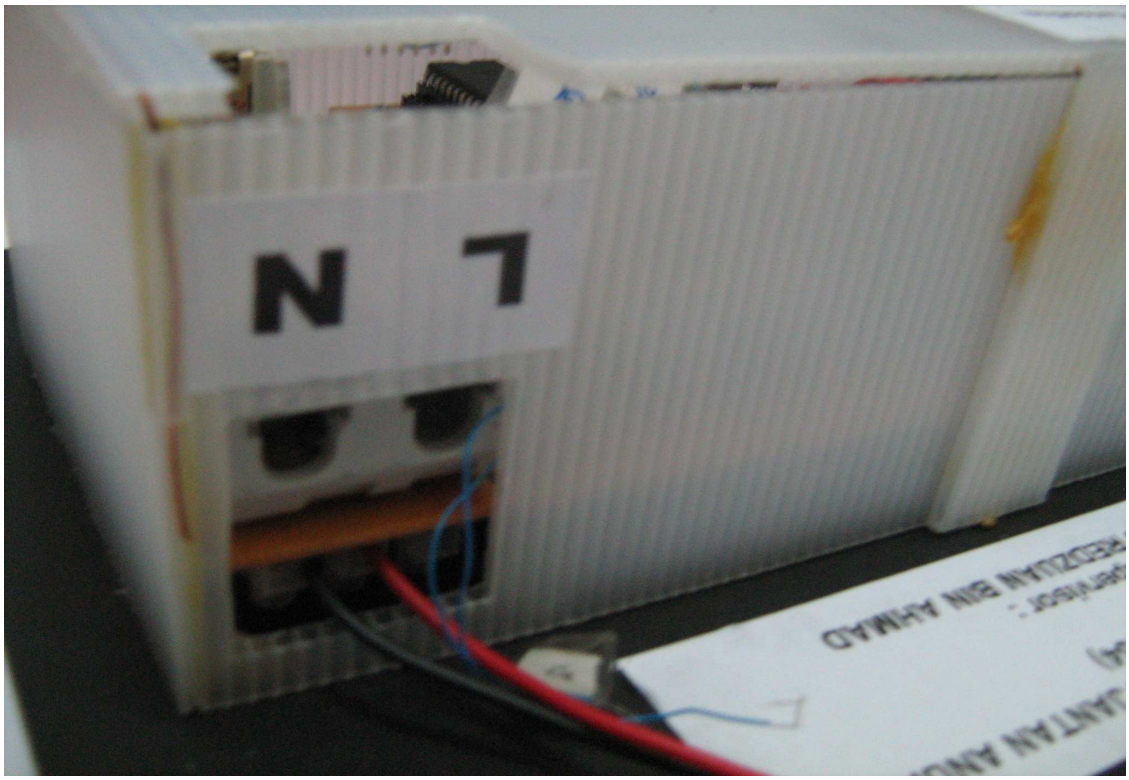


Figure A3: Incoming supply for AR-ELCB.

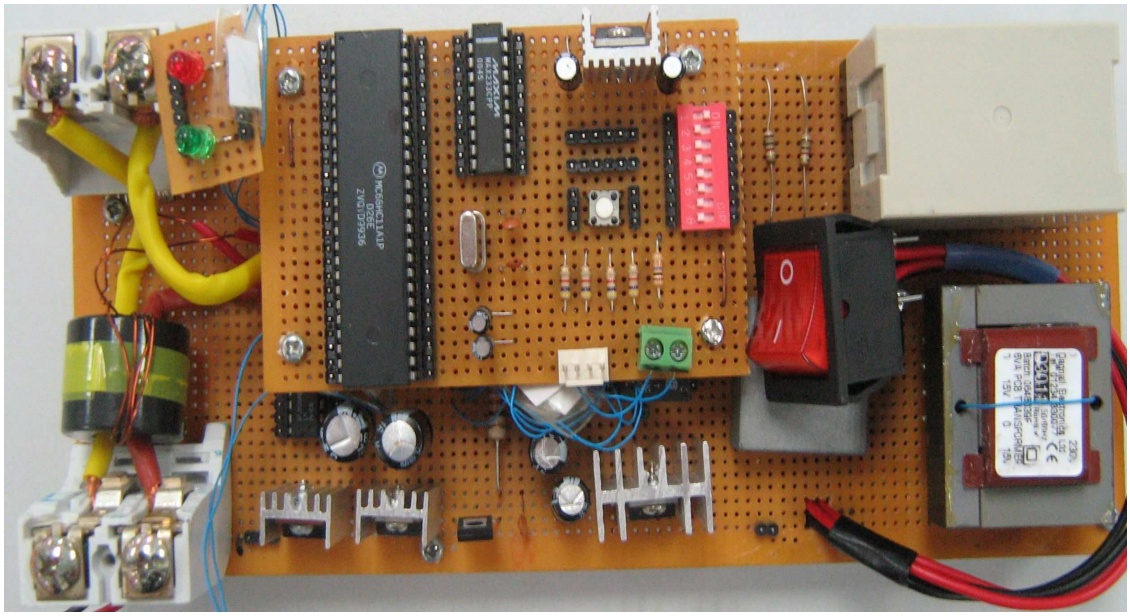


Figure A4: First layer circuit inside the housing.

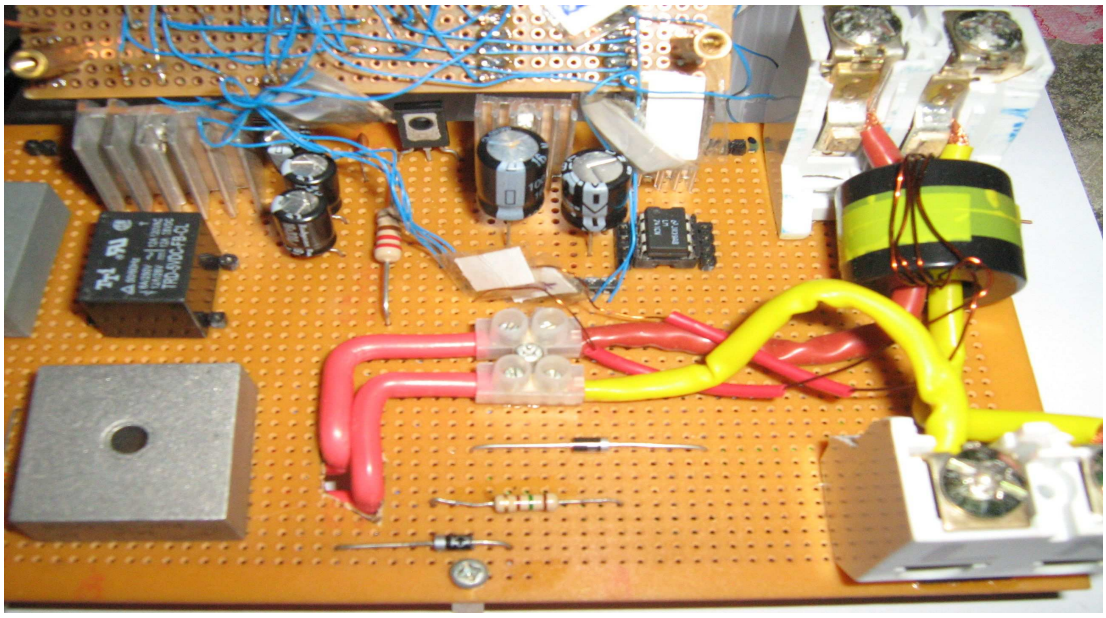


Figure A5: Second layer circuit inside the housing.

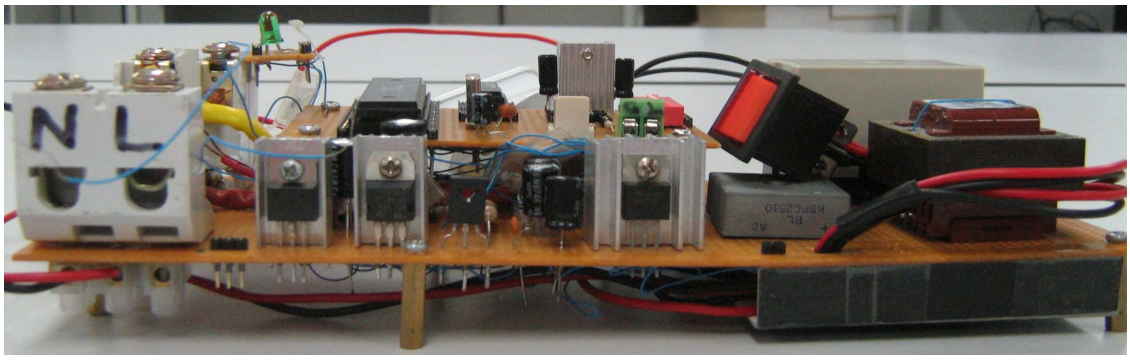


Figure A6: Upward view of circuit inside the housing.

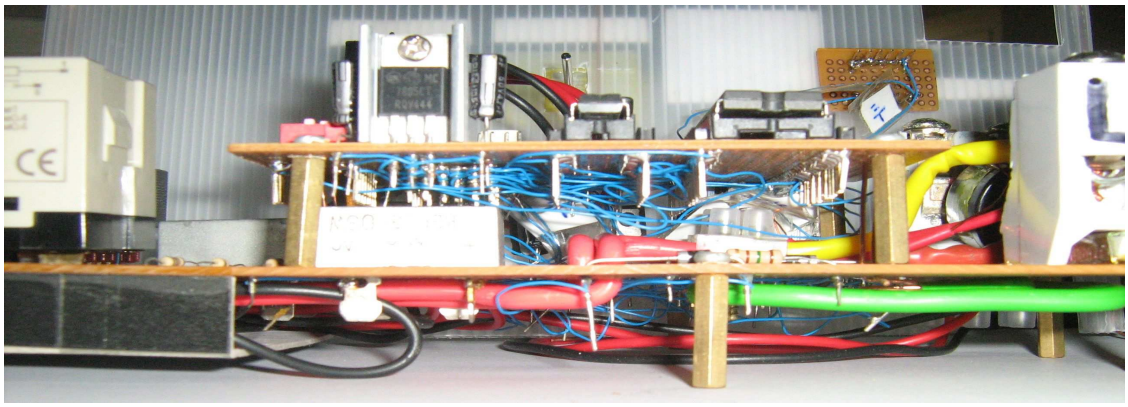


Figure A6: Downward view of circuit inside the housing.

APPENDIX G

Biodata of the Author

AUTHOR'S BIODATA

Ahmad Khairul Azwan Bin Jantan Anua Jah was born on 30th November 1985 in kg. Bendang Pak Yong Tumpat Kelantan, his permanent address is at Quarters LPP Kuala Balah, 17610 Jeli, Kelantan. he is an eldest brother from five siblings, he was completed his secondary studies in Civil Engineering course at Sekolah Menengah Teknik Pasir Mas, Kelantan at 2003. Then he was further study in Science physics course at Kedah Matriculation College from 9 May 2004 until 14 April 2005. He is currently (2008) a Bachelor's student in the Electrical Engineering (Power System), faculty of Electrical and Electronics Engineering, University Malaysia Pahang. His research fields are power electronics and power system. He is a student member of the IEM of Malaysia.