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A Review on Transistors in Nano Dimensions

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***Abstract*—In this paper, a review on characterization of transistors in nano dimension for improving ICs integration was presented. Various novel device structures are being extensively explored because the conventional silicon MOSFET has scaling limits. This work was focused on fabrication technology and characterization of nanowire transistor, FinFET transistor, and carbon nanotube transistor and its applications.**

***Index Terms*—Transistor, Nanowire, Nanotube, FinFET, MOSFET, Inverter.**

I. INTRODUCTION

Nowadays electronics components are subjected to Nano dimensions to maximize integration in integrated circuits (ICs) as possible to increase its efficiency. The most important device in minimization is transistor were the integration of ICs measures by transistors per chip. Complementary metal–oxide–semiconductor (CMOS) technology has led to the steady minimization of transistors with each new generation, thereby yielding continuous improvements in transistor performance. However, the International Technology Roadmap for Semiconductors (ITRS) had indicated that the scaling of gate transistor lengths to sub-22 nm levels could yield several serious problems, such as high sub-threshold leakages, short-channel effects, device-to device variations, and so on [1]. Several studies have attempted to overcome these problems by designing new transistor structures, such as the double-gate field-effect transistor (DG-FET), Fin-shaped Field Effect Transistor (FinFET), Carbon Nanotube Transistor (CNT), and Silicon Nanowire Field Effect Transistor (SiNWT).

II. NANO-TRANSISTORS

Planar DG-FETs are shown in Figure 1. This structure contains two gates, top and bottom, that control the channel. The DG-FET provides better control of the short-channel effects, lowers leakage, and provides better yield in aggressively scaled traditional CMOS technology [2].

To overcome the difficulty of aligning the two gates, a special type of DG-FET, known as the FinFET, is used. FinFETs are relatively easy to manufacture and feature no alignment problems that plague many other DG-FET structures. Furthermore, the use of a lightly doped channel in FinFETs allows them to become resistant to random dopant variations [1].