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Optimization of Nanowires Ratio in Nano-scale SiNWT Based SRAM Cell

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Abstract. This paper represents the impact of nanowires ratio of silicon nanowire transistors on the characteristics of 6-transistors SRAM cell. This study is the first to demonstrate nanowires ratio optimization of Nano-scale SiNWT Based SRAM Cell. Noise margins and inflection voltage of transfer characteristics are used as limiting factors in this optimization. Results indicate that optimization depends on both nanowires ratio and digital voltage level (V_{dd}). And increasing of logic voltage level from 1V to 3V tends to decreasing in optimization ratio but with increasing in current and power. SRAM using nanowires transistors must use logic level (2V or 2.5V) to produce SRAM with lower dimensions and lower inflection currents and then with lower power consumption.

1 Introduction

Static random access memory (SRAM) cell with six transistors (6T) is the primary memory used in many applications in digital circuits. As is well known, designing an integrated circuit chips that having the greatest possible number of individual 6T SRAM cells with two inverters circuits was considered a main goal of semiconductor technologies in our days, with a view to provide the integrated circuit chip with a largest memory as possible within the available area thereon. To achieve this objective, layouts for the transistors making up the cells integrated circuit have been developed by designers to reduce the area required for each. As the conventional silicon metal-oxide-semiconductor field-effect transistor (MOSFET) approaches its down scaling limits, many novel transistors' structures are being extensively explored. Among them, the silicon nanowire transistor (SiNWT) has attracted broad attention from both the semiconductor industry and academic fields [1-4].

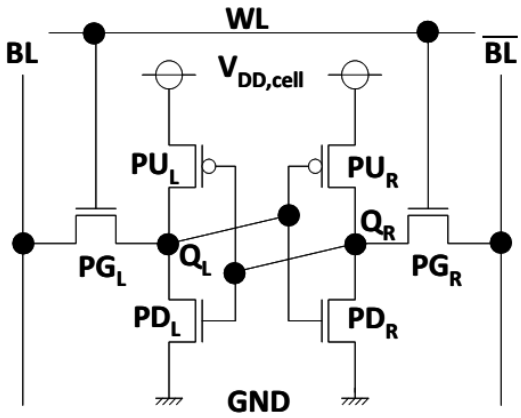

Figure 1. circuit diagram of a Static Random Access Memory (SRAM).

Fig. 1 shows the most commonly used SRAM bit-cell architecture that is the six MOSFET transistors (6-T) SRAM cell. It consists of two cross-coupled inverters (PMOS pull-up transistors PUL and PUR and NMOS pull-down transistors PDL and PDR) and two access transistors (NMOS pass-gate transistors PGL and PGR). When the horizontally-running word-line (WL) is enabled, the access transistors are turned on, and connect the storage nodes to the vertically-running bit-lines (BL and BL). In other words, they allow access to the cell for read and write operations, acting as bidirectional transmission gates.

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2 Results and discussions

Construction of SRAM cells and its inverters using nanowires, include a number of PMOS and NMOS devices disposed on nanowires that are arranged on a wafer. Since the properties of the nanowires (e.g., nanowire diameters) affect the operation of the devices, it is desirable to arrange the devices such that the effects of the differences in the nanowire properties are reduced.

In the present paper, a computer-based model that discussed in [5] used to produce static characteristics of SRAM cells. The MATLAB software is designed to calculate the working points of the matched curves of the output characteristic of the two transistors connected as a CMOS inverter circuit. The MATLAB software is designed to calculate output (V_{out}-V_{in}) and current (I_{out}-V_{in}) characteristics of the NW-CMOS inverter depending on the I_d-V_d characteristics of SiNWTs [5]. This model used MuGFET tool [6, 7] to produce NW N- and P-channel transistor output characteristics to fully simulate the NW-CMOS. These characteristics are then implemented in the MATLAB model to find the final static characteristics of the two transistors connected as a CMOS inverter circuit the main part of SRAM. [5]

The nanowires ratio of two SiNWTs was selected to make the SRAM work in the best possible conditions. The dimension ratio (Kp/Kn) of the two transistors (where K=Diameter (D)/Length (L)) in a normal CMOS inverter is (≈3/1) when the width of the PMOS is increased or the length of the NMOS is decreased. The parameters in Table 1 are used to study the effect of dimensions on the characteristics of the SRAM.

Table 1. Nanowire transistors parameters

Parameter Name	N-nanowire	P-nanowire
Channel length L	30 nm	30 nm
Source length	10 nm	10 nm
Drain length	10 nm	10 nm
Channel diameter D	20 nm	20 nm
Oxide thickness SiO_2	2 nm	2 nm
Channel concentration	$1*10^{10}/cm^3$	$1*10^{10}/cm^3$
Source and drain concentration	$1*10^{20}/cm^3$ (n-type)	$1*10^{20}/cm^3$ (p-type)

Fig 2 illustrates the shift of inflection point to the right with increasing nanowires ratio (Np/Nn) by increasing numbers of nanowire in PMOS transistor, where ((Np/Nn) =1, 3, and 7) at logic level voltage V_{dd}=1. The increase in I_{ds} by increasing numbers of nanowire in the P-channel transistor tends to compensate for the lower mobility of carriers (holes) in P-channel NWs. This process tends to improve noise margins of the inverter circuit. The dimensional optimization principle depends on noise margins and the inflection voltage (V_{inf}). These parameters are used as limitation factors. The best inverter has equal noise margin low (NM_L) and noise margin high (NM_H) values. Both NM_L and NM_H must have high values, and the V_{inf} must be close to (V_{dd}/2) value, according to Fig 2, increasing of Np/Nn tends to increase in NM_L and decrease in NM_H without reaching optimized value (0.5V). NM_H and NM_L are the high- and low-state noise margins, respectively. In current characteristics it is clear that the current was increased at inflection point with increasing nanowires ratio. According to Fig 3, and at V_{dd}=1V there is no optimization point where NM_H and NM_L curves cross in it and be nearer to V_{dd}/2 line with inflection voltage curve, and this figure illustrates that NM_L and NM_H are impossible to be equal.

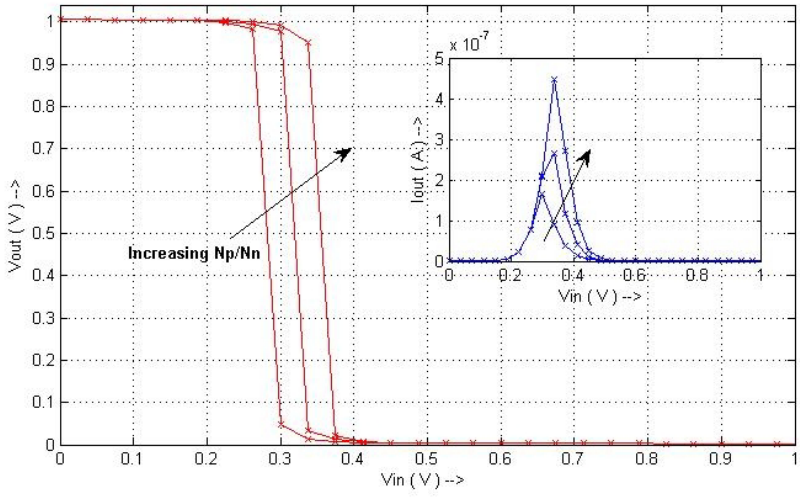

Figure 2. Transfer and current characteristics with different (Np/Nn) and V_{dd}=1V.

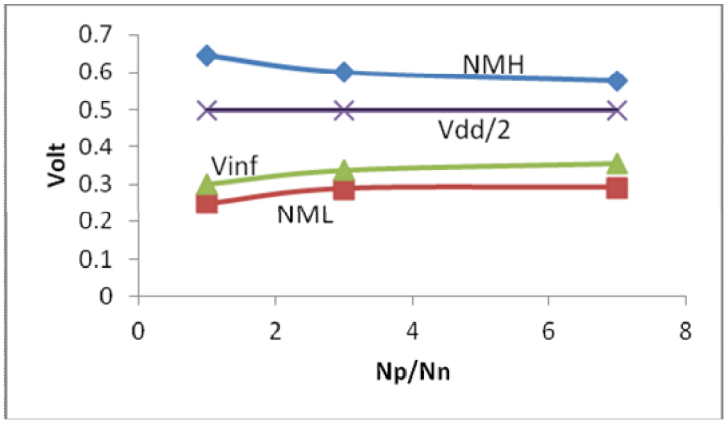

Figure 3. NM_H, NM_L and V_{inf} curves with (Np/Nn) at V_{dd} = 1 V.

In Fig 4 the transfer characteristics of same inverters in SRAM with same dimensions in Table1 and also with same nanowires ratios ((Np/Nn) =1, 3, and 7) but with logic level voltage V_{dd}=2, this figure illustrates the shift of inflection point to the right with increasing nanowires ratio (Np/Nn) at this logic level (2V), according to Fig 4, increasing of (Np/Nn) tends to increase in NM_L and decrease in NM_H and reaching optimized value (1V). In current characteristics it is clear that the current was increased at inflection point with increasing nanowires ratio. Fig 5 shows that the crossing between NM_H and NM_L curves happen at Np/Nn=4.8 (around 5) which represent the optimized value for nanowires ratio. At this optimization point NM_H=NM_L=0.74V, V_{inf}=0.95V at this optimization point, which is close to V_{dd}/2 (1 V).

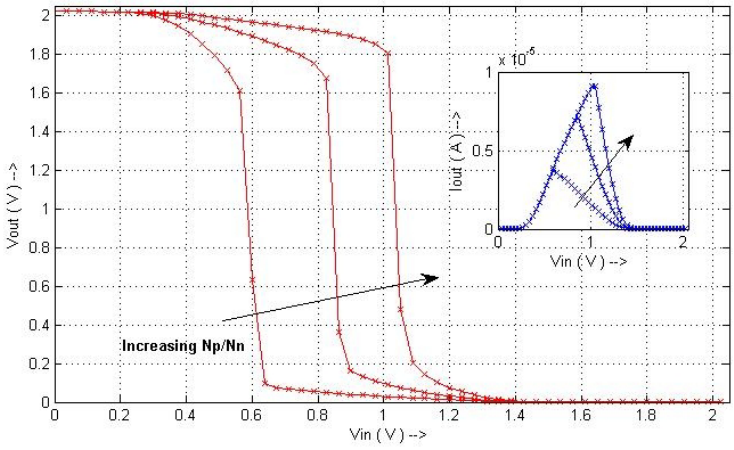

Figure 4. Transfer and current characteristics with different (Np/Nn) and V_{dd}=2V.

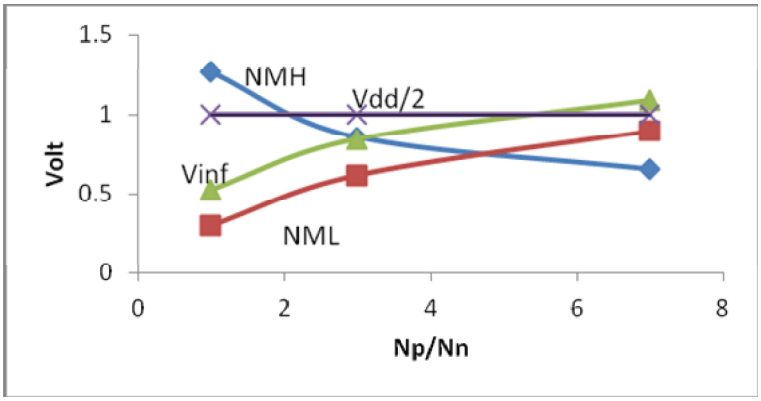

Figure 5. NM_H, NM_L and V_{inf} curves with (Np/Nn) at Vdd = 2 V.

The transfer and current characteristics of the inverters in SRAM with same dimensions in Table1 and also with same nanowires ratios ((Np/Nn) =1, 3, and 7) but with logic level voltage V_{dd}=3 was shown in Fig 6, this figure

illustrates the shift of inflection point to the right with increasing nanowires ratio (Np/Nn) at logic level 3V. According to Fig 6, increasing of (Np/Nn) tends to increase in NM_L and decrease in NM_H with reaching (and crossing over) optimized value (1.5V). In current characteristics it is clear that the current was increased at inflection point with increasing nanowires ratio. Fig 7 shows that the crossing between NM_H and NM_L curves happen at Np/Nn=2.6 which represent the optimized value for nanowires ratio. At this optimization point NM_H=NM_L=0.9V, V_{inf}=1.4V at this optimization point, which is close to V_{dd}/2 (1.5 V).

According to figures (3, 5 and 7), optimization point will happen at lower value of nanowires ratio (lower dimensions) by increasing digital level voltage from 1V to 3V, but this also will tends to increase inflection current and power consumption in SRAM. under this fact, the fabrication of SRAM using nanowires transistors must use logic level (2V or 2.5V) to produce SRAM with lower dimensions and lower inflection currents and then with lower power consumption.

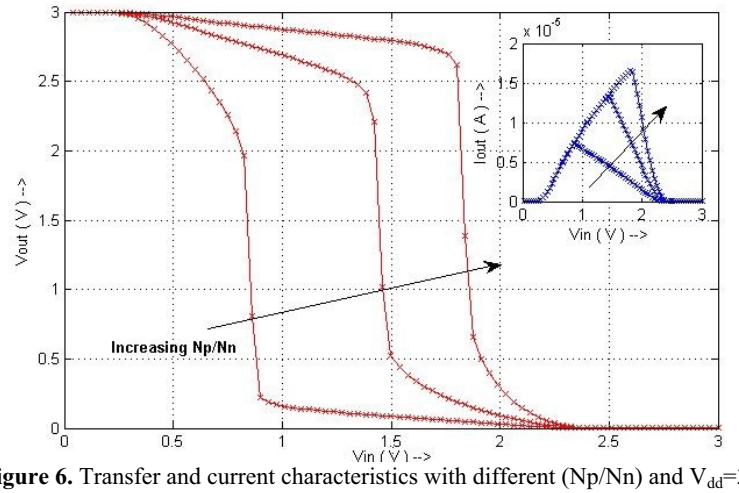

Figure 6. Transfer and current characteristics with different (Np/Nn) and V_{dd}=3V.

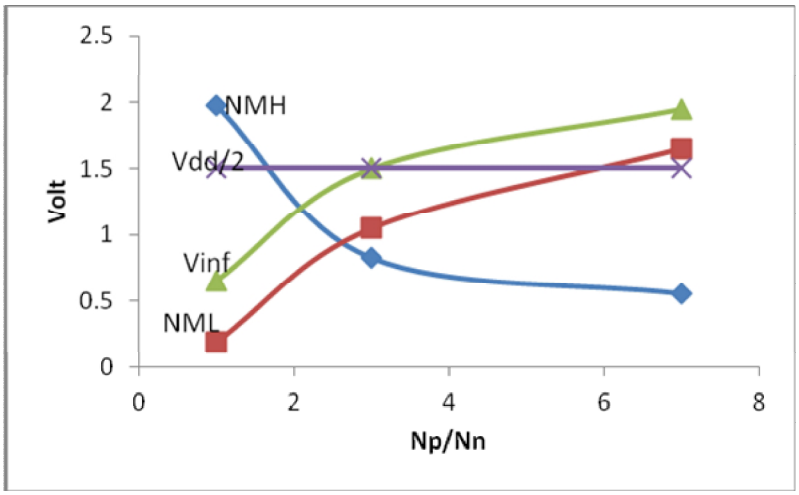

Figure 7. NM_H, NM_L and V_{inf} curves with (Np/Nn) at Vdd = 3 V.

3 Summary

Effect of nanowires ratio of silicon nanowire transistors in SRAM with different logic levels was studded in this paper. The limiting factors of this optimization were noise margins and inflection voltage of transfer characteristics. Results indicate that optimization depends on both nanowires ratio and digital voltage level (V_{dd}). And increasing of logic voltage level from 1V to 3V tends to decreasing in optimization ratio from very high nanowire ratio to 2.5, but with increasing in current. the fabrication of SRAM using nanowires transistors must use logic level (2V or 2.5V) to produce SRAM with lower dimensions and lower inflection currents and then with lower power consumption.

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