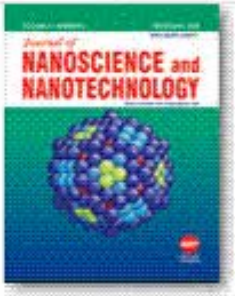

A New Approach for Dimensional Optimization of Inverters in 6T-Static Random-Access Memory Cell Based on Silicon Nanowire Transistor

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Abstract | References | Citations | Supplementary Data | Data/Media | Metrics

This study explores dimensional optimization at different high logic-level voltages for six silicon nanowire transistor (SiNWT)-based static random-access memory (SRAM) cell. This study is the first to demonstrate diameter and length of nanowires with different logic voltage level (V_{dd} optimizations of nanoscale SiNWT-based SRAM cell. Noise margins and inflection voltage of butterfly characteristics are used as limiting factors in this optimization. Results indicate that optimization depends on nanowire dimensions and V_{dd}. The increase in V_{dd} from 1 V to 3 V tends to decrease the dimensions of the optimized nanowires but increases the current and power. SRAM using nanowire transistors must use V_{dd} of 2 or 2.5 V to produce SRAM with lower dimensions, inflection currents, and power consumption.

Keywords: CMOS; Digital Inverter; Nanowire; SRAM; SiNWT

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