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Optimization of Channel Length Nano-Scale SiNWT Based SRAM Cell

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Abstract. This paper represents a channel length ratio optimization at a different high logic level voltage for 6-Silicon Nanowire Transistors (SiNWT) SRAM cell. This study is the first to demonstrate an optimized length ratio of nanowires with different V_{dd} of nano-scale SiNWT based SRAM cell. Noise margins (NM) and inflection voltage (V_{inf}) of transfer characteristics are used as limiting factors in this optimization. Results indicate that optimization depends on both length ratios of nanowires and logic voltage level (V_{dd}), and increasing of high logic voltage level of the SiNWT based SRAM cell tends to decrease in the optimized nanowires length ratio with decreasing in current and power.

Nomenclatures

D	Diameter of nanowire, m
L	Length of nanowire, m
NM_H	Noise margin high, V
NM_L	Noise margin low, V
V_{dd}	High level logic voltage, V
V_{inf}	Inflection voltage,

Abbreviations

BL	Bit line
CMOS	Complementary Metal Oxide Semiconductor
MuGFET	Multi Gate Field Effect
NMOS	N type Metal Oxide Semiconductor
NW	Nano Wire
PU_L	Pull-up left transistors
PU_R	Pull-up right transistors
PD_L	Pull-down left transistors
PD_R	Pull-down right transistors
PG_L	Pass-gate left transistors
PG_R	Pass-gate right transistors
PMOS	P type Metal Oxide Semiconductor
SiNWT	Silicon Nano Wire Transistor
WL	Word-line

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INTRODUCTION

Static random access memory (SRAM) cell with six transistors (6T) is the primary memory used in many applications in digital circuits. As is well known, designing an integrated circuit chip that having the greatest possible number of individual 6T SRAM cells with two inverter circuits was considered a main goal of semiconductor technologies in our days, with a view to provide the integrated circuit chip with the largest memory as possible within the available area thereon. To achieve this objective, layouts for the transistors making up the cells integrated circuit have been developed by designers to reduce the area required for each. As the conventional silicon metal-oxide-semiconductor-field-effect transistor (MOSFET) approaches it down scaling limits, many novel transistor structures are being extensively explored. Among them, the silicon nanowire transistor (SiNWT) has attracted broad attention from both the semiconductor industry and academic fields [1-6].

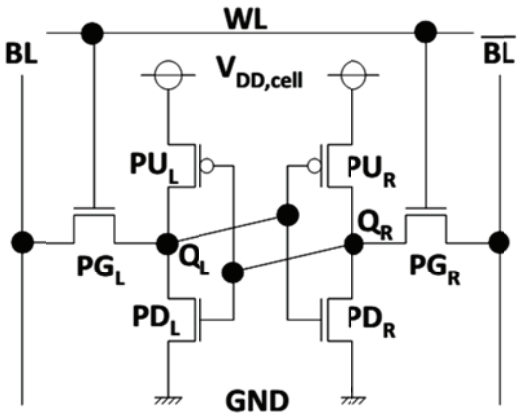

FIGURE 1. Circuit diagram of a Static Random Access Memory (SRAM).

Fig. 1 shows the most commonly used SRAM bit-cell architecture that is the six MOSFET transistors (6-T) SRAM cell. It consists of two cross-coupled inverters (PMOS pull-up transistors PU_L and PU_R and NMOS pull-down transistors PD_L and PD_R) and two access transistors (NMOS pass-gate transistors PG_L and PG_R).
When the horizontal-running word-line (WL) is enabled, the access transistors are turned on, and connect the storage nodes to the vertically-running bit lines (BL and BL). In other words, they allow access to the cell for read and write operations, acting as bidirectional transmission gates.

RELATED WORK

Construction of SRAM cells and its inverters using nanowires, include a number of PMOS and NMOS devices disposed on nanowires that are arranged on a wafer. Since the dimensions of nanowires effect on the operation of SRAM, it is desirable to arrange the devices such that these effects of the dimensions of nanowire are optimized.

In the present paper, a computer-based model that discussed in [7] used to produce static characteristics of SRAM cells. The MATLAB software is designed to calculate the working points of the matched curves of the output characteristic of the two nanowire transistors connected as a CMOS inverter circuit in SRAM. The MATLAB software is designed to calculate output (V_{out}-V_{in}) and current (I_{out}-V_{in}) characteristics of the NW-CMOS inverter depending on the I_d-V_d characteristics of SiNWTs [7]. This model used MuGFET tool [8] to produce NW N- and P-channel transistor output characteristics to fully simulate the NW-CMOS. These characteristics are then implemented in the MATLAB model to find the final static characteristics of the two transistors connected as a CMOS inverter circuit the main part of SRAM. [7]

METHODOLOGY

The nanowires ratio of two SiNWTs was selected to make the SRAM work in the best possible conditions. The dimension ratio (Kp/Kn) of the two transistors (where K=Diameter (D)/Length (L)) in a normal CMOS inverter is (≈3/1) when the width of the PMOS is increased or the length of the NMOS is decreased. The parameters in Table 1 are used to study the effect of dimensions on the characteristics of the SRAM.

Table 1 Nanowire transistors initial dimensions' parameters and concentrations

Parameter Name	N-nanowire	P-nanowire
Channel length L	30 nm	30 nm
Source length	10 nm	10 nm
Drain length	10 nm	10 nm
Channel diameter D	20 nm	20 nm
Oxide thickness SiO_2	2 nm	2 nm
Channel concentration	$1*10^{10}/cm^3$	$1*10^{10}/cm^3$
Source and drain concentration	$1*10^{20}/cm^3$ (n-type)	$1*10^{20}/cm^3$ (p-type)

The optimization will depend strongly on increasing current (I_{ds}) of PMOS transistor. Increasing in I_{ds} of a nanowire in the P-channel transistor tends to compensate for the lower mobility of carriers (holes) in P-channel NWs [9]. This process tends to improve noise margins of the inverter circuit. The dimensional optimization principle depends on noise margins and the inflection voltage (V_{inf}). These parameters are used as limitation factors. The best inverter has an equal noise margin low (NM_L) and noise margin high (NM_H) values. Both NM_L and NM_H must have high values, and the V_{inf} must be close to ($V_{dd}/2$) value.

RESULTS AND DISCUSSIONS

Fig. 2 illustrates the shift of inflection point to the right with increasing nanowires length ratio (Ln/Lp) by increasing the length of the nanowire in NMOS transistor, where ((Ln/Lp) =1, 5, and 9) at logic level voltage V_{dd}=1. According to Fig 2, increasing of Ln/Lp tends to increase in NM_L and decrease in NM_H without reaching optimized value (0.5V). In current characteristics, it is clear that the current was decreased at the inflection point with increasing nanowires length ratio. According to Fig 3, and at V_{dd}=1V there is no optimization point where NM_H and NM_L curves cross in it and be nearer to $V_{dd}/2$ line with an inflection voltage curve, and this figure illustrates that NM_L and NM_H can't be equal with any Ln/Lp ratio.

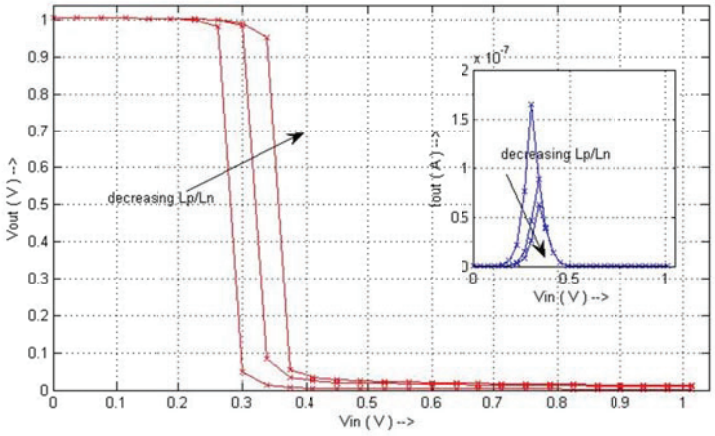

FIGURE 2. Transfer and current characteristics with different (Ln/Lp) and Vdd=1V.

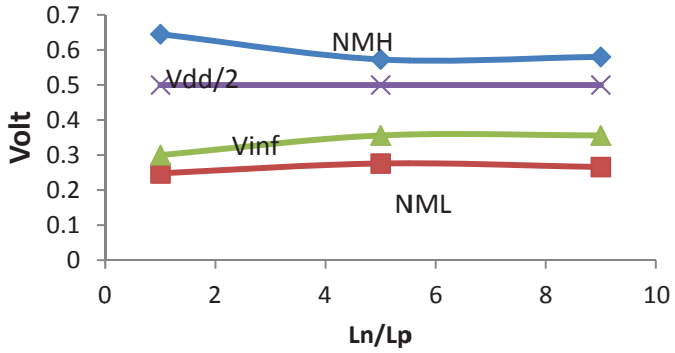

FIGURE 3. NMH, NML and Vinf curves with (Ln/Lp) at V_{dd} = 1 V.

In Fig 4 the transfer characteristics of same inverters in SRAM with same dimensions in Table1 and also with same nanowires length ratios ((Ln/Lp) =1, 5, and 9) but with logic level voltage V_{dd}=2, Fig 4 illustrates the shift of inflection point to the right with increasing nanowires length ratio (Ln/Lp) at this logic level (2V), according to Fig 4, increasing of (Ln/Lp) tends to increase in NM_L and decrease in NM_H and near to the optimized value (1V). In current characteristics, it is clear that the current was decreased at the inflection point with increasing nanowires length ratio. Fig 5 shows that the crossing between NM_H and NM_L curves may happen at Ln/LP =11.4 which represent the optimized value of the nanowires length ratio. At this optimal point NM_H=NM_L=0.6V, V_{inf}=0.9V at this optimal point, which is near to V_{dd}/2 (1 V).

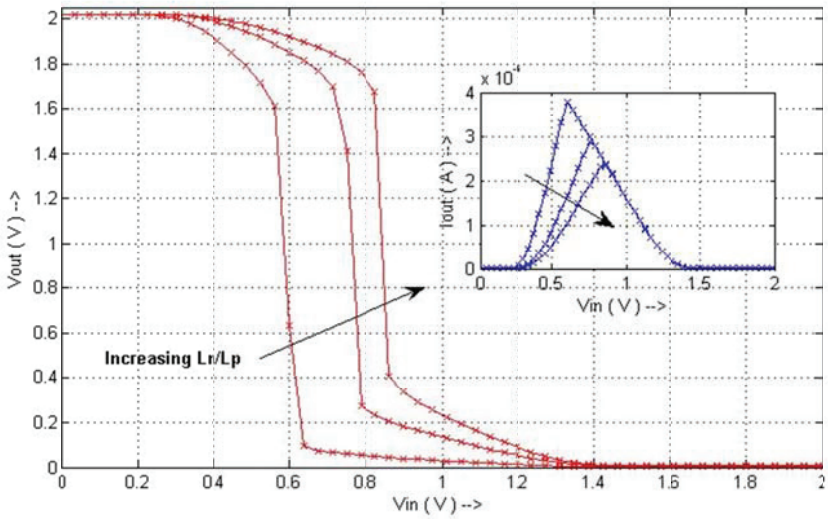

FIGURE 4. Transfer and current characteristics with different (Ln/Lp) and V_{dd}=2V.

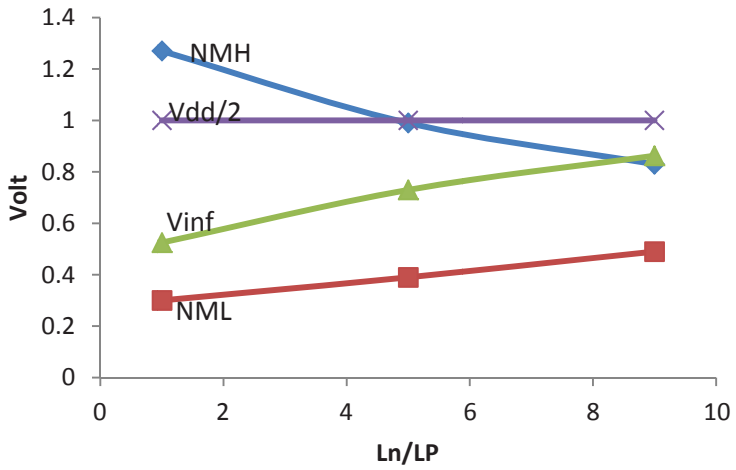

FIGURE 5. NM_H, NM_L and V_{inf} curves with (Ln/Lp) at V_{dd} = 2 V.

The transfer and current characteristics of the inverters in SRAM with same dimensions in Table1 and also with same nanowires length ratios ((Ln/Lp) =1, 5, and 9) but with logic level voltage V_{dd}=3 was shown in Fig 6, this figure illustrates the shift of inflection point to the right with increasing nanowires length ratio (Ln/Lp) at logic level 3V. According to Fig 6, increasing of (Ln/Lp) tends to increase in NM_L and decrease in NM_H with nearing to optimized value (1.5V). In current characteristics, it is clear that the current was decreased at the inflection point with increasing nanowires length ratio. Fig 7 shows that the crossing between NM_H and NM_L curves may happen at Ln/Lp =10 which represent the optimized value of nanowires ratio. At this optimal point NM_H=NM_L=0.65V, V_{inf}=1.45V at this optimal point, which is very close to V_{dd}/2 (1.5 V).

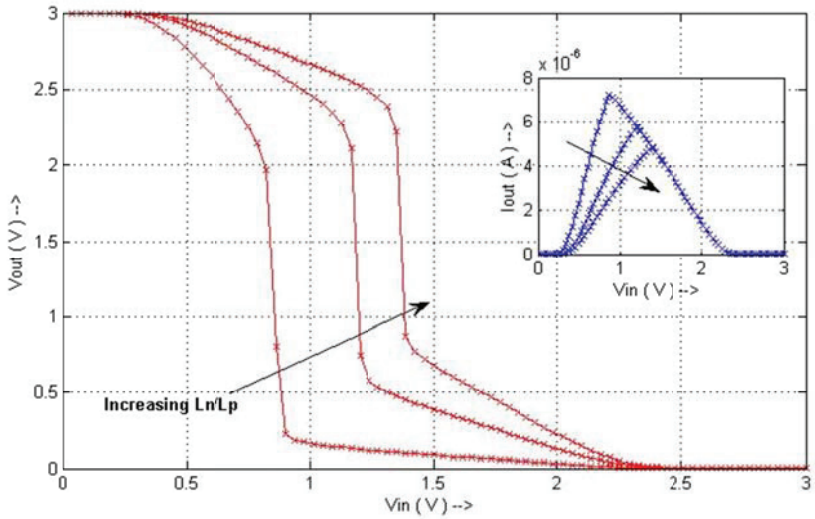

FIGURE 6. Transfer and current characteristics with different (Ln/Lp) and Vdd=3V.

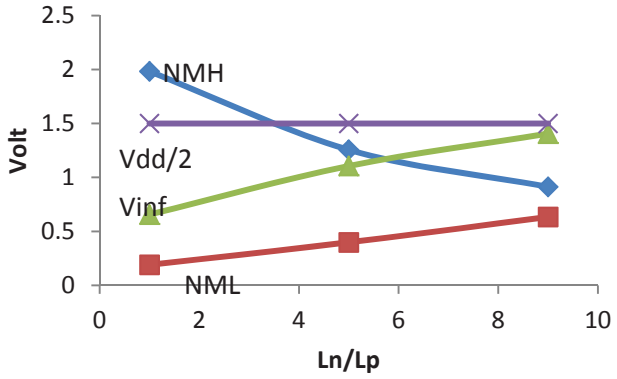

FIGURE 7. NM_H, NM_L and V_{inf} curves with (Ln/Lp) at V_{dd} = 3 V.

Depending on results for length ratio optimization in figures (2) to (7), and according to Fig 8, optimization point will happen at the lower value of length ratio Ln/Lp by increasing V_{dd} from 1V to 3V, and this also will tend to decrease the inflection current and power consumption in SRAM. But increasing of length ratio will increase Ln and this will increase the size of the device, Under this optimization in length, the fabrication of SRAM using nanowires transistors must use V_{dd} (2V to 3V) to produce SRAM lower inflection currents and then with lower power consumption, but with higher dimensions.

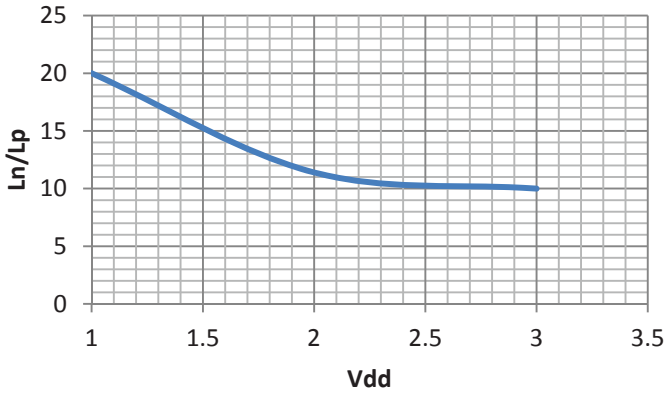

FIGURE 8. Optimized Ln/Lp by increasing V_{dd} from 1V to 3V.

CONCLUSION

The effect of the nanowires length ratio of silicon nanowire transistors in SRAM with different logic levels was studied in this paper. The limiting factors of this optimization were noise margins and inflection voltage of transfer characteristics. Results indicate that optimization depends on both nanowires ratio length and high-level digital voltage (V_{dd}). And increasing of logic voltage level from 1V to 3V tends to decrease in the optimization length ratio of nanowires for transistors from very high nanowire length ratio to 10, with decreasing the current. The fabrication of SRAM using nanowires transistors must use V_{dd} (2.5V or 3V) to produce SRAM with lower dimensions and lower inflection currents and then with lower power consumption.

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