A SIMULATION STUDY OF THE EFFECT OF EQUIVALENT SERIES RESISTANCE (ESR) IN DC-DC CONVERTER

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Thesis submitted in fulfillment of the requirements
for the award of the Bachelor of Electrical Engineering (Hons.) (Power System)

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ABSTRAK

Penukar arus terus ialah litar elektronik yang menukarkan sumber arus terus dari satu tahap voltan yang lain. Permodelan penukar arus terus dengan kapasitor Setaraf Siri Rintangan (ESR) dipertimbangkan dalam projek ini. ESR atau parasit adalah bukan parameter ideal digunakan dalam litar reka bentuk. idealities bukan atau parasitics peranti praktikal dan komponen yang memberi kesan kepada beberapa parameter prestasi dalam penukar arus terus. Terdapat tiga penukar dikaji dalam projek ini yang 'buck converter., rangsangan penukar dan flyback penukar. Operasi penukar berada dalam mod berterusan pengaliran (SSM) yang diambil kira. Simulasi penukar dijalankan menggunakan Matlab Simulink. Analisis penukar telah dilakukan di bawah suis idea, diod dan andaian komponen pasif. Dalam projek ini, nilai ESR yang (rC) adalah 1.2Ω, 0.14 Ω dan 0,014 Ω digunakan. Kesan ESR pada riak voltan keluaran dan kecekapan penukar

ABSTRACT

DC-DC Converters is an electronic circuit which converts a source of direct current from one voltage level to another. Modelling of DC-DC converter with capacitor Equivalent Series Resistance (ESR) are considered in this project. ESR or parasitic is non-ideal parameter used in the design circuit. Non idealities or parasitics of practical devices and components affect some performance parameter in dc-dc converters. There are three converters studied in this project which are buck converter, boost converter and flyback converter. The operation of the converter is in the continuous conduction mode (CCM) is assumed. The simulation of the converter is carried out using the Matlab Simulink. The analysis of converters has been performed under idea switch, diode and passive component assumptions. In this project, the ESR value (rC) are 1.2Ω, 0.14 Ω and 0.014 Ω used. The effects of ESR on output voltage ripple and efficiency of converters

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LIST OF SYMBOLS

rC	Equivalent Series Resistor
ΔVo	Output Voltage Ripple
Ŋ	Efficiency
D	Duty Cycle
Vs	Voltage Source
C	Capacitor

LIST OF ABBREVIATION

ESR	Equivalent Series Resistor
CCM	Continuous Conduction Mode
DC	Direct Current

CHAPTER 1

INTRODUCTION

1.1 Overview

This chapter consists of four elements which are background of study, problem statement, objectives, and scope of project. For background of study, it is about the general introduction of this project. Problem statement of this project was included in this chapter. It stated about how this project will be doing. Besides that, this chapter is also as the main support for the objectives in order to ensure the relevancy of the project. There are two objectives that must be achieved at the end of this project. Lastly, for the scope of project, this sub topic is explaining on what this project is focused on.

1.2 Background of Study

Converter is a device for altering the nature of an electric current or signal. It consists of AC-AC converter and DC-DC converter. DC-DC converter is an electronic circuit which converts a source of direct current from one voltage level to another [1]. DC-DC converter can be divided into two main types which are hard-switching pulse width modulated (PWM) converters and resonant and soft-switching converters [2]. The PWM converters have been very popular for the last three decades [3]. They are widely used at all power levels. Advantages of PWM converters include low component count, high efficiency, constant frequency operation, relatively simple control and commercial availability of integrated circuit controller and ability to achieve high conversion ratios for both step down and step up application [3]. The disadvantage of PWM DC-DC converter is that PWM rectangular voltage and current waveform cause turn-on and turn-off losses in semi-conductor devices which limit practical operating frequencies to a megahertz range. Parasitic is non-ideal parameter used such as resistance, capacitance and inductance [2]. Non-idealities or parasitic of

practical devices and component may, however greatly affect some performance parameters of DC-DC converter [2].

1.3 Problem Statement

No study ranges for ESR in order to determine the output voltage ripple and efficiency in particular converters.

1.4 Objectives

The aim of this project is to study the effect of the ESR (Equivalent Series Resistor) on the performance parameter of DC-DC converter.

The main objectives of this project are:

1. To analyse the effect of parasitic on output voltage ripple.
2. To analyse the effect of parasitic on efficiency.

1.5 Scope of Study

The works undertaken in this project are limited to the DC-DC buck converter, DC-DC boost converter and DC-DC flyback converter. All of these three converters must run in CCM. The value of the voltage used for buck is 11 V, for boost is 12 V and for flyback is 36 V.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

DC-DC converters are important in subsystems and in portable electronic devices, which are supplied with power from batteries. Such electronic devices often contain several sub-circuits, each with its own voltage level requirement often different from that supplied by the battery. Additionally, the battery voltage declines as its stored power drained[4].

2.2 Equivalent Series Resistance (ESR)

Capacitors are needed for storage and smoothing of DC output voltage of power supplies and converters. ESR of a capacitor is particularly important in power supply designs. When analysing a circuit, a capacitor should be depicted as its equivalent circuit including the ideal capacitor, but also with its series ESR value [4]. ESR also is non-idealities or parasitic of practical devices and components may, however, greatly effect some performance parameters of DC-DC converters. The simulation study of the effects of parasitic on output voltage ripple and efficiency have been run using Matlab Simulink.

2.3 Buck Converter

Buck converter is a step down converter. It consists of dc input voltage source Vs, controlled switch S, diode D, filter inductor L, filter capacitor C and load resistance, R. the state of the converter in which the inductor current is never zero for any period of time is called continuous conduction mode (CCM) [5]. It can be seen from the circuit that when the switch S is commanded to the on state the diode D is reverse biased. When the switch S is off, the diode conducts to support an uninterrupted current in the inductor.

In the preceding analysis, the capacitor was assumed to be very large to keep the output voltage constant. In practice, the output voltage cannot be kept perfectly constant with finite capacitance. The variation in output voltage, or ripple, is compute from the voltage-current relationship of the capacitor[1]. The current in the capacitor is

$$i_C = i_L - i_R \qquad 2\text{-}1$$

While the capacitor current is positive, the capacitor is charging. From the definition of capacitance,

$$Q = CV_o \qquad 2\text{-}2$$

$$\Delta Q = C\Delta V_o \qquad 2\text{-}3$$

$$\Delta V_o = \frac{\Delta Q}{C} \qquad 2\text{-}4$$

The change in charge ΔQ is the area of triangle above the time axis

$$\Delta Q = \frac{1}{2}\left(\frac{T}{2}\right)\left(\frac{\Delta i_L}{2}\right) = \frac{T\Delta i_L}{8} \qquad 2\text{-}5$$

Resulting in

$$\Delta V_o = \frac{T\Delta i_L}{8C} \qquad 2\text{-}6$$

For the preceding analysis to be valid, continuous current in the inductor must be verified. An easy check for continuous current is to calculate the minimum inductor current. Since the minimum value of inductor current must be positive for continuous current, a negative minimum calculated is not allowed due to the diode and indicates discontinuous current. The circuit will operate for discontinuous inductor current, but the preceding analysis is not valid. Discontinuous-current operation is discussed later in this chapter.

Equation below can be used to determine the combination of L and f that will result in continuous current. Since $I_{min} = 0$ is the boundary between continuous and discontinuous current,

$$I_{min} = 0 = V_o\left(\frac{1}{R} - \frac{1-D}{2Lf}\right) \qquad 2\text{-}7$$

$$(Lf)_{min} = \frac{(1-D)R}{2} \qquad 2\text{-}8$$

If the desired switching frequency is established,

$$L_{min} = \frac{(1-D)R}{2f} \qquad 2\text{-}9 \text{ for continuous current}$$

Where L_{min} is the minimum inductance required for continuous current. In practice, a value of inductance greater than L_{min} is desirable to ensure continuous current.

2.4 Boost Converter

The boost converter is another well-known switched-mode converter that is capable of producing a dc output voltage greater in magnitude than the dc input voltage. A practical realization of the switch, using MOSFET and diode.

The preceding equation were developed on the assumption that the output voltage was a constant, implying an infinite capacitance. In practice, a finite capacitance will result in some fluctuation in output voltage or ripple. The peak-to-peak output voltage ripple can be calculated from the capacitor current waveform. The change in the capacitor charge can be calculated from,

$$|\Delta Q| = \left(\frac{V_o}{R}\right) DT = C\Delta V_o \qquad 2\text{-}10$$

An expression for ripple voltage is then

$$\Delta V_o = \frac{V_o DT}{RC} = \frac{V_o D}{RCf} \qquad 2\text{-}11$$

$$\text{Or } \frac{\Delta V_o}{V_o} = \frac{D}{RCf} \qquad 2\text{-}12$$

Where f is the switching frequency. Alternatively, expressing capacitance in terms of output voltage ripple yields

$$C = \frac{D}{R\left(\frac{\Delta V_o}{V_o}\right) f} \qquad 2\text{-}13$$

As with the buck converter, equivalent series resistance of the capacitor can contribute significantly to the output voltage ripple. The peak to peak variation in capacitor current

is the same as the maximum current in the inductor. The voltage ripple due to the ESR is

$$\Delta V_{o,ESR} = \Delta i_C r_C = I_{L,max} r_C \qquad 2\text{-}14$$

Thus, all the experiment values were recorded in a table according the value of rC used. Then, the result was finalized into a table of output voltage ripple and a table of efficiency.

2.5 Flyback Converter

Flyback converter is a DC-DC converter that provides isolation between input and output. The effects of losses and leakage inductances are important when considering switch performance and protection, but the overall operation of the circuit is best understood with this simplified transformer model. CCM operation required that $I_{Lm,min} > 0$ in equation

$$I_{Lm,min} = I_{Lm} - \frac{\Delta i_{Lm}}{2} \qquad 2\text{-}15$$

$$= \frac{V_s D}{(1-D)^2 R}\left(\frac{N_2}{N_1}\right)^2 - \frac{V_S DT}{2L_m} \qquad 2\text{-}16$$

In flyback converter design, L_m is selected to be larger than $L_{m,min}$ to ensure continuous current operations

$$L_m = \frac{V_S DT}{\Delta i_{Lm}} = \frac{V_s D}{\Delta i_L f} \qquad 2\text{-}17$$

The output configuration for the flyback converter is the same as for buck-boost converter, so the output ripple voltage for the two converters are also the same.

$$\frac{\Delta V_O}{V_O} = \frac{D}{RCf} \qquad 2\text{-}18$$

The equivalent series resistance of the capacitor can contribute significantly to the output voltage ripple. The peak-to-peak variation in capacitor current is the same as the maximum current in the diode and the transformer secondary. The voltage ripple due to the ESR is

$$\Delta V_{o,ESR} = \Delta i_C r_C = I_{Lm,max}(\frac{N_1}{N_2})r_C \qquad 2\text{-}19$$

CHAPTER 3

METHODOLOGY

3.1 Flow Chart

Using Matlab Simlink, the circuit of buck converter, boost converter and flyback converter were designed based on the ideal circuit. From the ideal circuit, the value of ESR was added to check the effect on the performance parameter. There are three ESR value used while running the experiment. The data were collected based on the scope obtained for voltage and current on the input and output. Figure 3-1 shows the flow chart of this project. From the flow chart, the process to run the experiment are same for all the converters. Firstly, all the three converters were designed in Matlab Simulink. Then, the parameter were set according the standard value of converter used. The ESR was added into the design and the value of $rC = 1.2\ \Omega$ was set. Next, set 0.05 of the duty cycle. After that, the simulink was rn for 0.3S and the data were collected from the scope designed in the circuit. All the data were recorded in the excel. The process keep repeating with the changing of the value of duty cycle. The value of duty cycle increased by 0.05 until the duty cycle reached 0.95. After all the collected data saved in excel, the value of rC change to 0.14 Ω and 0.014 Ω. Then, the process keep repeating unti finish. From the data collected, a graph of output voltage ripple against duty cycle and a graph of efficiency against duty cycle were constructed.

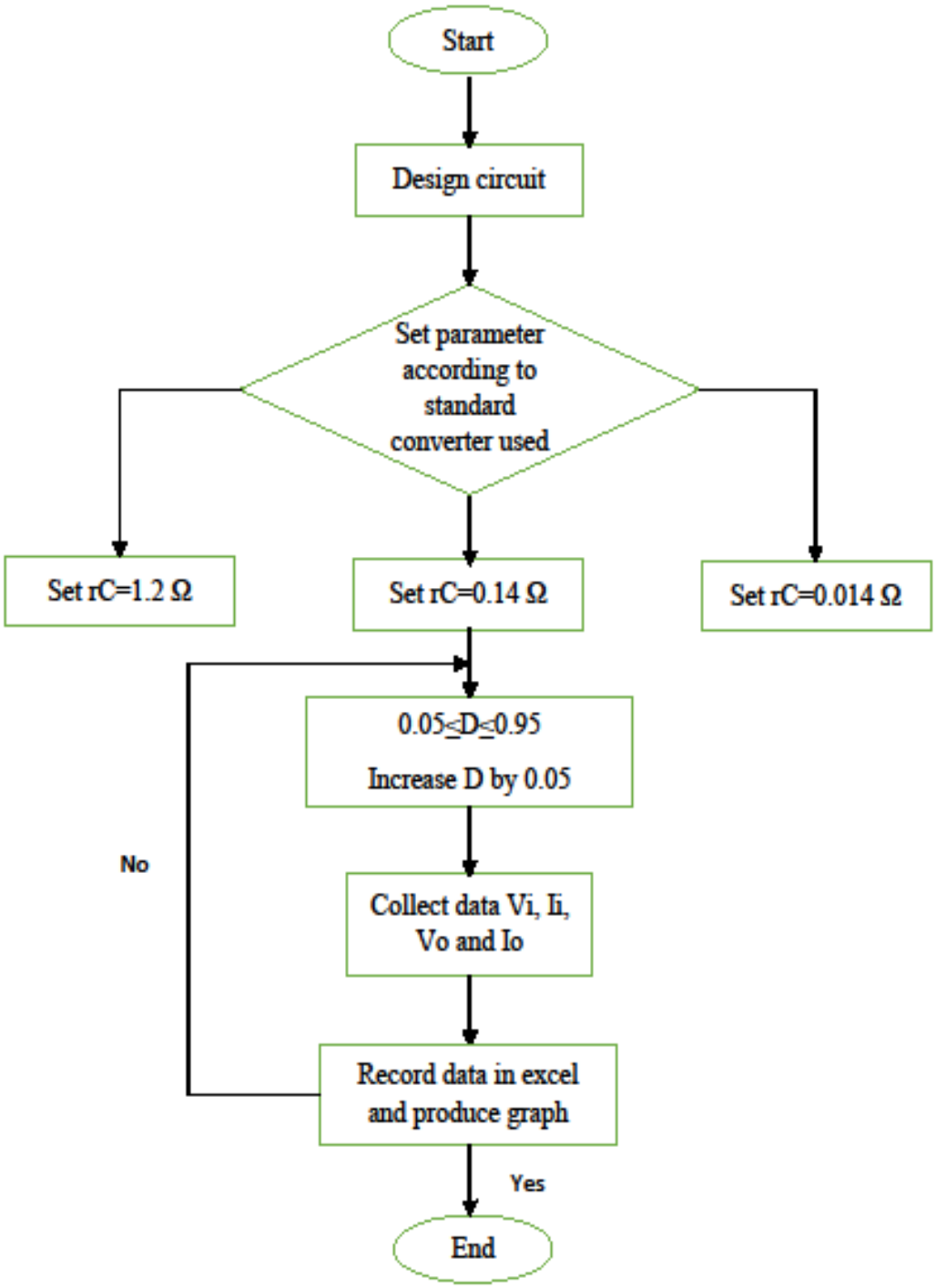

Figure 3-1 Flow Chart

3.2 Design

Figure 3-2 shows the circuit of buck converter with the present of ESR were designed using Matlab Simulink based on standard buck converter circuit. The experiment run using different value of duty cycle (D) between 0.5 to 0.95. The data were collected for every change of 0.5 of duty cycle without changing other parameter. For the first data collected, the value of ESR was 1.2Ω then after collected all the data for all duty cycle, the value of ESR was change to 0.14Ω and 0.014Ω

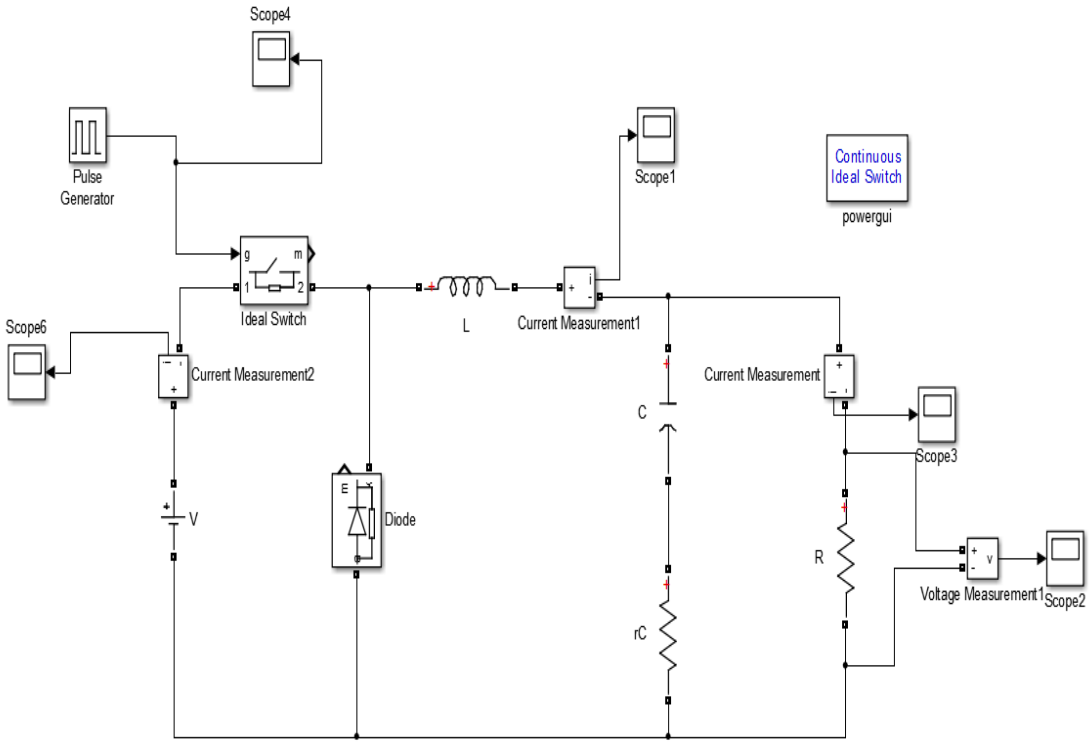

Figure 3-2 Design of buck converter in Matlab Simulink

Figure 3-3 shows the circuit of boost converter with the present of ESR were designed using Matlab Simulink based on standard boost converter circuit. The experiment run using different value of duty cycle (D) between 0.5 to 0.95. The data were collected for every change of 0.5 of duty cycle without changing other parameter. For the first data

collected, the value of ESR was 1.2Ω then after collected all the data for all duty cycle, the value of ESR was change to 0.14Ω and 0.014Ω

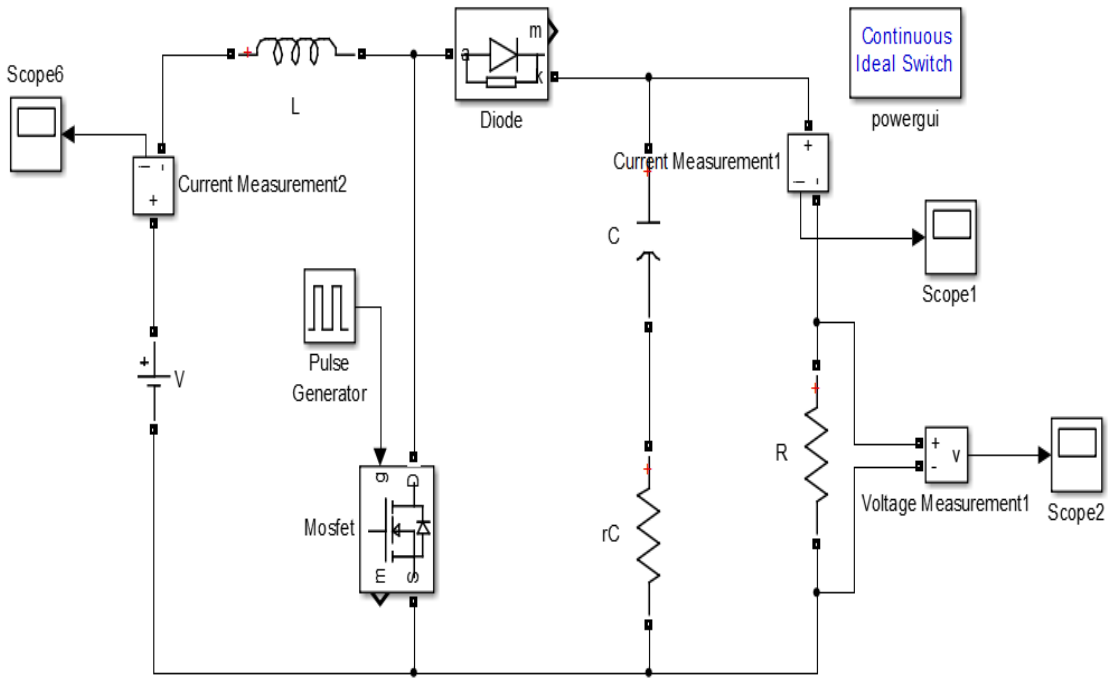

Figure 3-3 Design of boost converter in Matlab Simulink

Figure 3-4 shows the circuit of flyback converter with the present of ESR were designed using Matlab Simulink based on standard flyback converter circuit. The experiment run using different value of duty cycle (D) between 0.5 to 0.95. The data were collected for every change of 0.5 of duty cycle without changing other parameter. For the first data collected, the value of ESR was 1.2Ω then after collected all the data for all duty cycle, the value of ESR was change to 0.14Ω and 0.014Ω

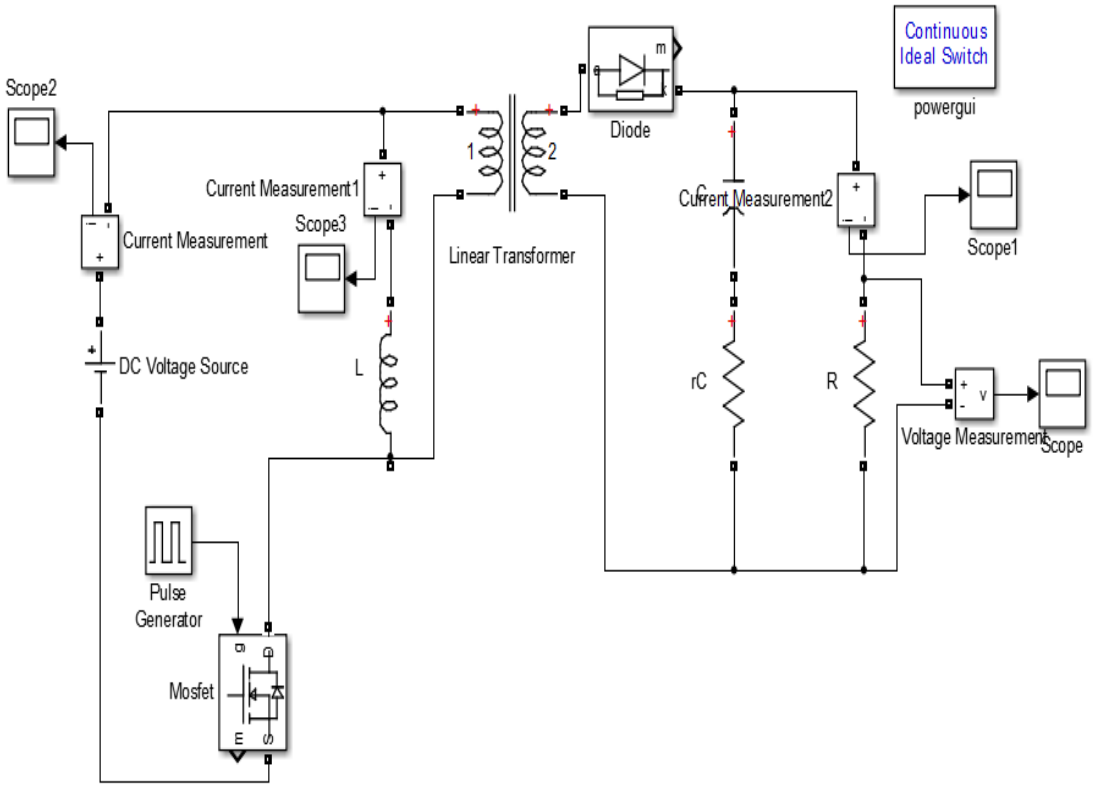

Figure 3-4 Design of flyback converter in Matlab Simulink

3.3 Design parameter

There are standard parameter used for all the converters. The simulation parameters used for buck DC-DC converter are shown in Table 3-1. There are three different value used for ESR which are 1.2 Ω, 0.14 Ω and 0.014 Ω. The value of duty cycle change every 0.05 from 0.05 to 0.95.

Table 3-1 Parameter of buck converter

Parameter	**Value**
L	37.5μH
C	400μF
rC	14mΩ/0.14Ω/1.2Ω
R	1Ω
V_g	11V
T_S	20μS

Source: [6]

There are standard parameter used for all the converters. The simulation parameters used for boost DC-DC converter are shown in Table 3-2. There are three different value used for ESR which are 1.2 Ω, 0.14 Ω and 0.014 Ω. The value of duty cycle change every 0.05 from 0.05 to 0.95.

Table 3-2 Parameter of boost converter

Parameter	**Value**
L	48μH
C	100μF
rC	14mΩ/0.14Ω/1.4Ω
R	50Ω
V_g	11V
T_S	40μS

Source: [1]

There are standard parameter used for all the converters. The simulation parameters used for flyback DC-DC converter are shown in Table 3-1. There are three different value used for ESR which are 1.2 Ω, 0.14 Ω and 0.014 Ω. The value of duty cycle change every 0.05 from 0.05 to 0.95.

Table 3-3 Parameter of flyback converter

Parameter	**Value**
L	500µH
C	200µF
rC	14mΩ/0.14Ω/1.4Ω
R	5Ω
V_g	24V
T_S	25µS

Source: [1]

3.3.1 Buck converter

The minimum value of inductor used in designed circuit must 10 times greater than above equation. So, the value of L used in this circuit can be choose which is equal or greater than 50µH. Figure 3-2 shows that the scope of inductor current while running the project in Matlab Simulink. This scope was checked before running the experiment to makesure that all the collected data are in CCM.

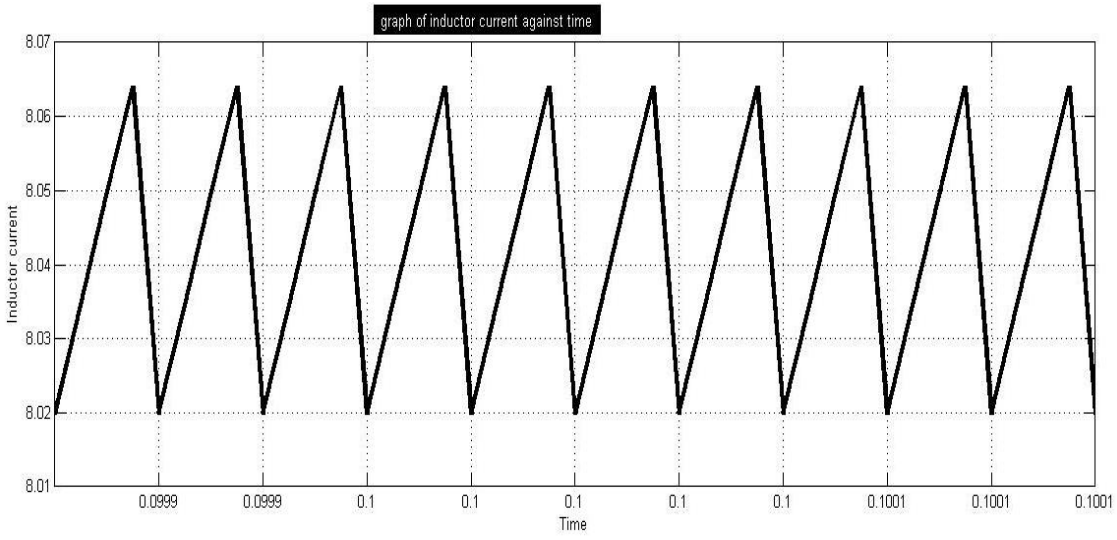

Figure 3-5 Scope of inductor current of buck converter in Matlab

3.3.2 Boost Converter

The minimum value of inductor used in designed circuit must 10 times greater than above equation. So, the value of L used in this circuit can be choose which is equal or greater than 1.25mH. Figure 3-6 shows that the scope of inductor current while running the project in Matlab Simulink. This scope was checked before running the experiment to makesure that all the collected data are in CCM.

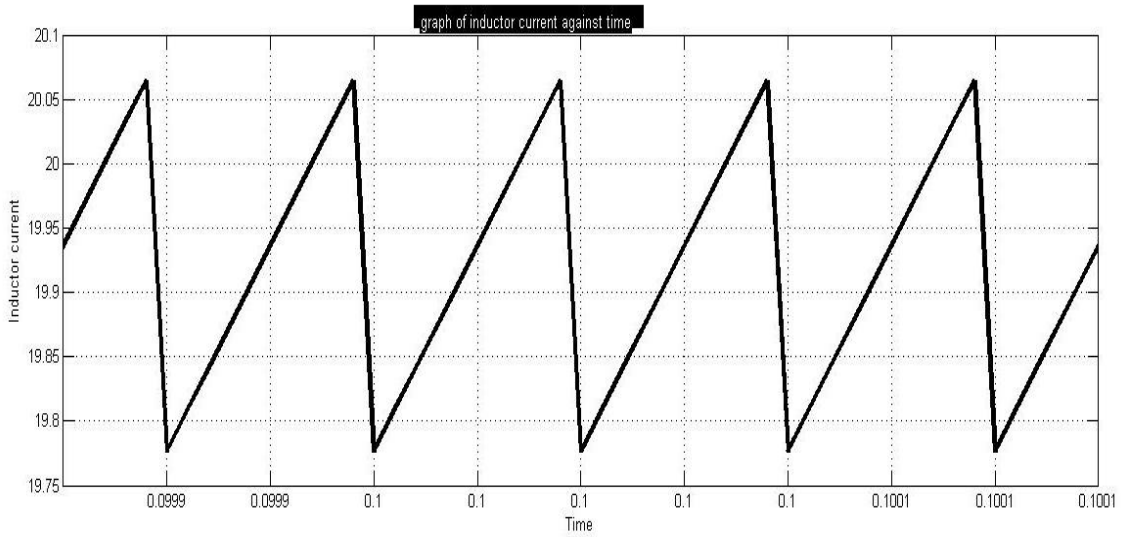

Figure 3-6 Scope of inductor current of boost converter in Matlab

3.3.3 Flyback Converter

Figure 3-7 shows that the scope of inductor current while running the project in Matlab Simulink. This scope was checked before running the experiment to makesure that all the collected data are in CCM.

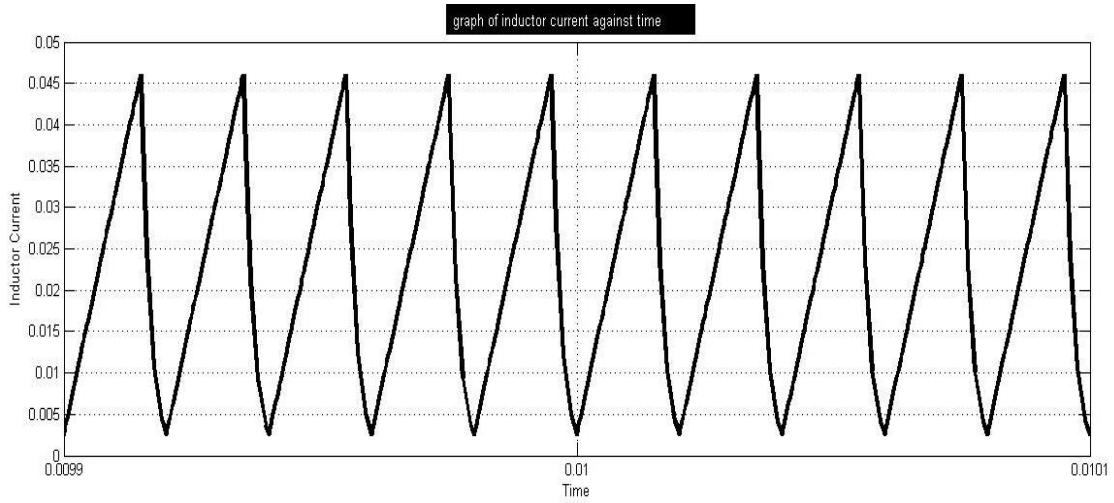

Figure 3-7 Scope of inductor current of flyback converter in Matlab

CHAPTER 4

RESULT & DISCUSSION

4.1 Buck converter

Buck converter is a step down converter which is the input value must higher than the output value. From the table showed that the output voltage value must not exceed the value of voltage input. From the value obtained from the experiment, it proved that this experiment is valid for standard buck converter. The value of ESR used was 1.2Ω. The manipulated variable of the buck converter is duty cycle. The output voltage and current were measured from the changing of 0.05 of duty cycle value. The experiment run from 0.05 until 0.95 of duty cycle. the result obtained from the scope of output voltage and current were recorded. The value of ESR changed to 0.14Ω and 0.014Ω. The results of output voltage ripple produced obtained with the present of three different ESR. The graph of output voltage ripple against duty cycle resulting the quadratic graph. Duty cycle does give effect to the performance parameter. From Figure 4-2, the efficiency increase as the duty cycle increase. The linear graph of efficiency against duty cycle produced. From Figure 4-1 it can be seen that the value of output voltage ripple increase as the value of duty cycle increase from 0.05 to 0.5. When duty cycle at 0.55, the value of output voltage ripple keep decrease until the duty cycle at 0.95. As the value of rC used larger, the value of output voltage ripple also large.

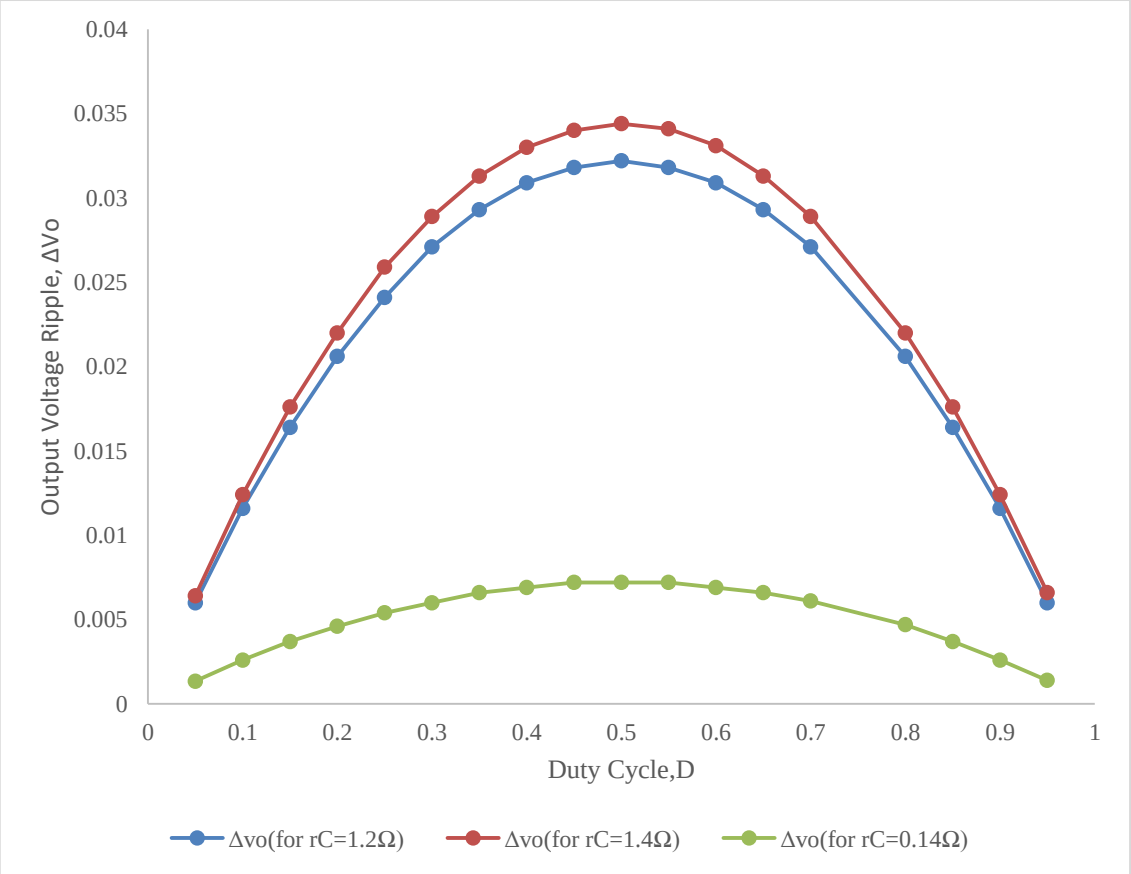

Figure 4-1 Graph of output voltage ripple against duty cycle of buck converter

From Figure 4-2 shows that the efficiency of the all the rC value used almost the same. The value of efficiency increase linearly as the value of duty cycle also increase. Besides that, efficiency increase as the value of duty cycle increase.

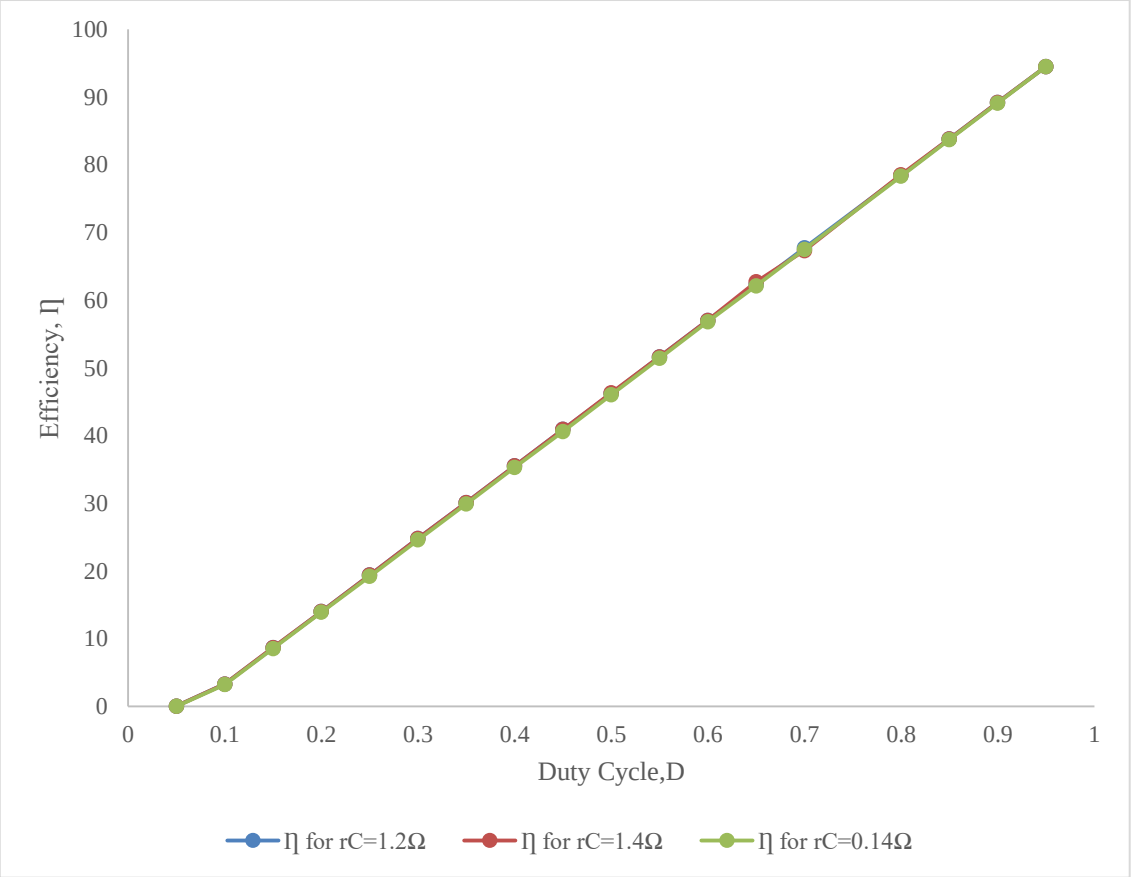

Figure 4-2 Graph of efficiency against duty cycle of buck converter

4.2 Boost

Since the boost converter is step up, resulting the output voltage value is higher than the input voltage. From the tables showed that the output voltage values must exceed the input voltage.

The value of ESR used was 1.2Ω. The manipulated variable of the boost converter is duty cycle. The output voltage and current were measured from the changing of 0.05 of duty cycle value. The experiment run from 0.05 until 0.95 of duty cycle the result obtained from the scope of output voltage and current were recorded. The value of ESR changed to 0.14Ω and 0.014Ω. The results were recorded. The finalized result of output voltage ripple produced obtained with the present of three different ESR. The graph of output voltage ripple against duty cycle produced. Duty cycle does give effect to the

performance parameter. The efficiency obtained in boost converter different from the buck converter. The graph of efficiency against duty cycle produced. From Figure 4- 3 it can be seen that the value of output voltage ripple in steady state from 0.05 to 0.45 of duty cycle. It increased as the value of duty cycle increase from 0.50 to 0.95.

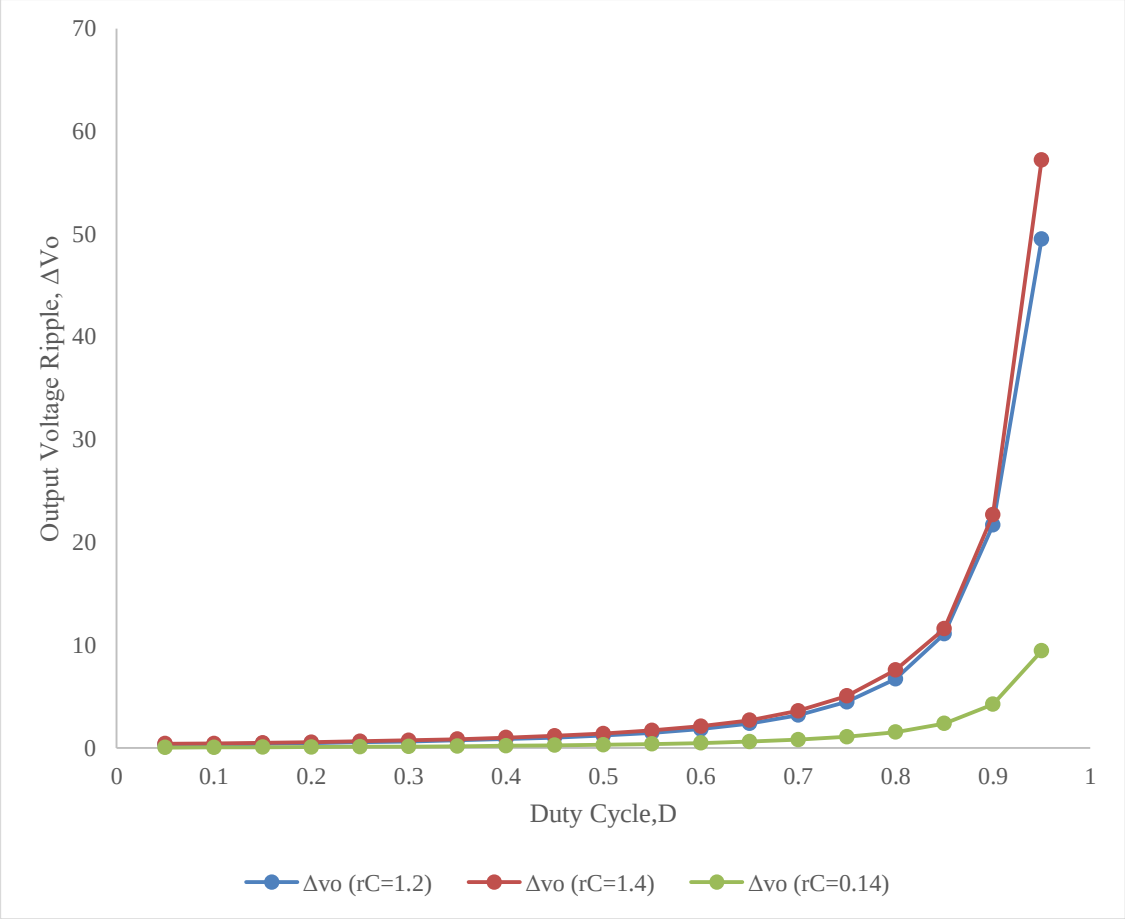

Figure 4-3 Graph of output voltage ripple against duty cycle of boost converter

From Figure 4-4 shows that the efficiency of the all three rC decrease from 0.05 to 0.25 of duty cycle. Then, it increased from 0.3 to 0.9 of duty cycle for rC=1.2Ω but for rC=0.14 and rC=0.014, it increased from duty cycle of 0.3 to 0.85. After that, it decreased sharply.

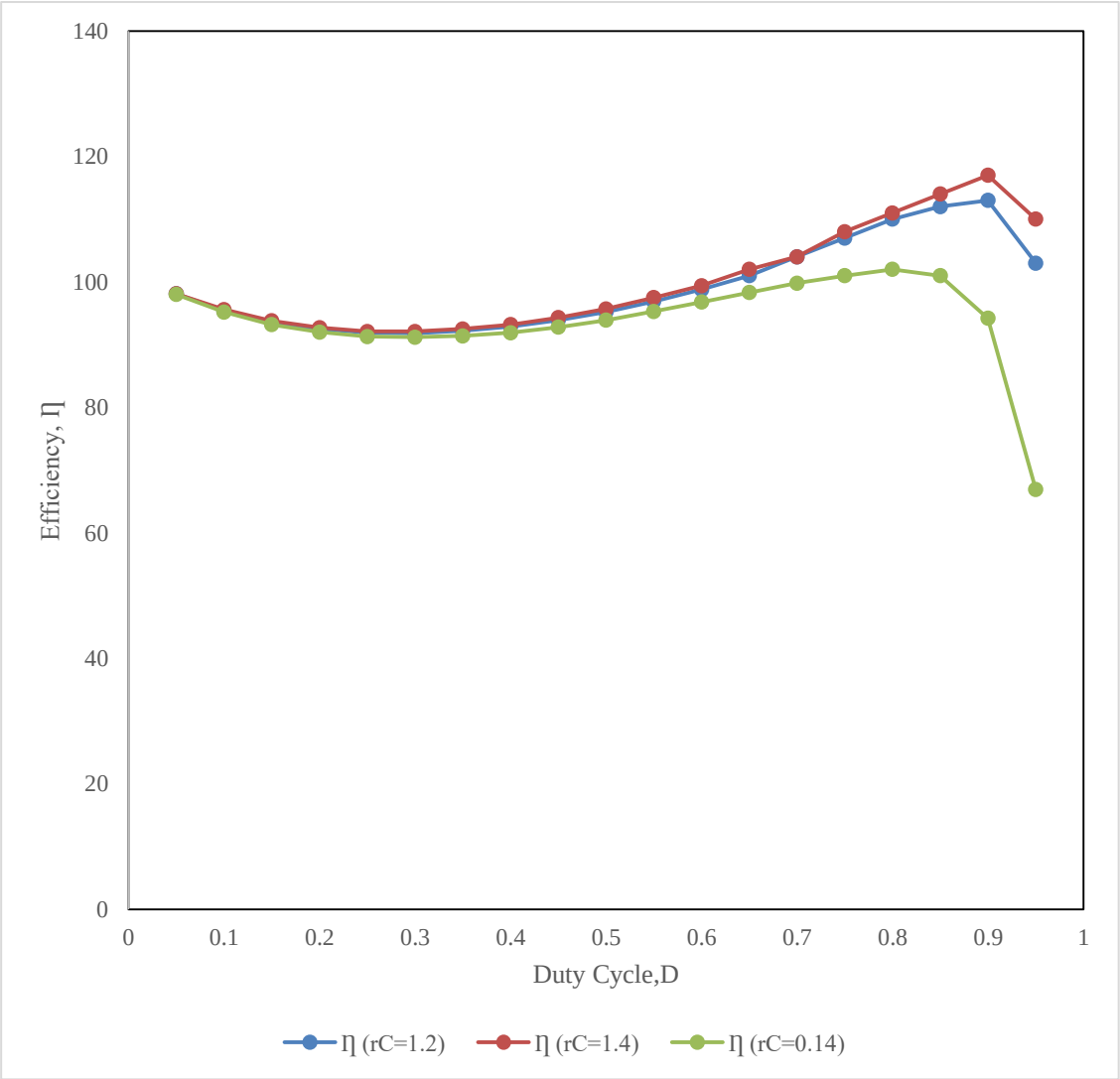

Figure 4-4 Graph of efficiency against duty cycle of boost converter

4.3 Flyback

Flyback converter provides isolation between input and output. From the tables showed that the output voltage value is lower that the input value. The manipulated variable of the buck converter is duty cycle. The output voltage and current were measured from the changing of 0.05 of duty cycle value. The experiment run from 0.05 until 0.95 of duty cycle. The result obtained from the scope of output voltage and current were recorded. The value of ESR changed to 0.14Ω and 0.014Ω. The finalized result of output voltage ripple produced obtained with the present of three different ESR. The

graph of output voltage ripple against duty cycle produced. Duty cycle does give effect to the performance parameter.

From Figure 4-5 it can be seen that the value of output voltage ripple decreased from 0.05 to 0.60. Next, it increased from 0.65 to 0.95 of duty cycle.

From Figure 4-6 the efficiency obtained in flyback converter different from the buck and boost converter.

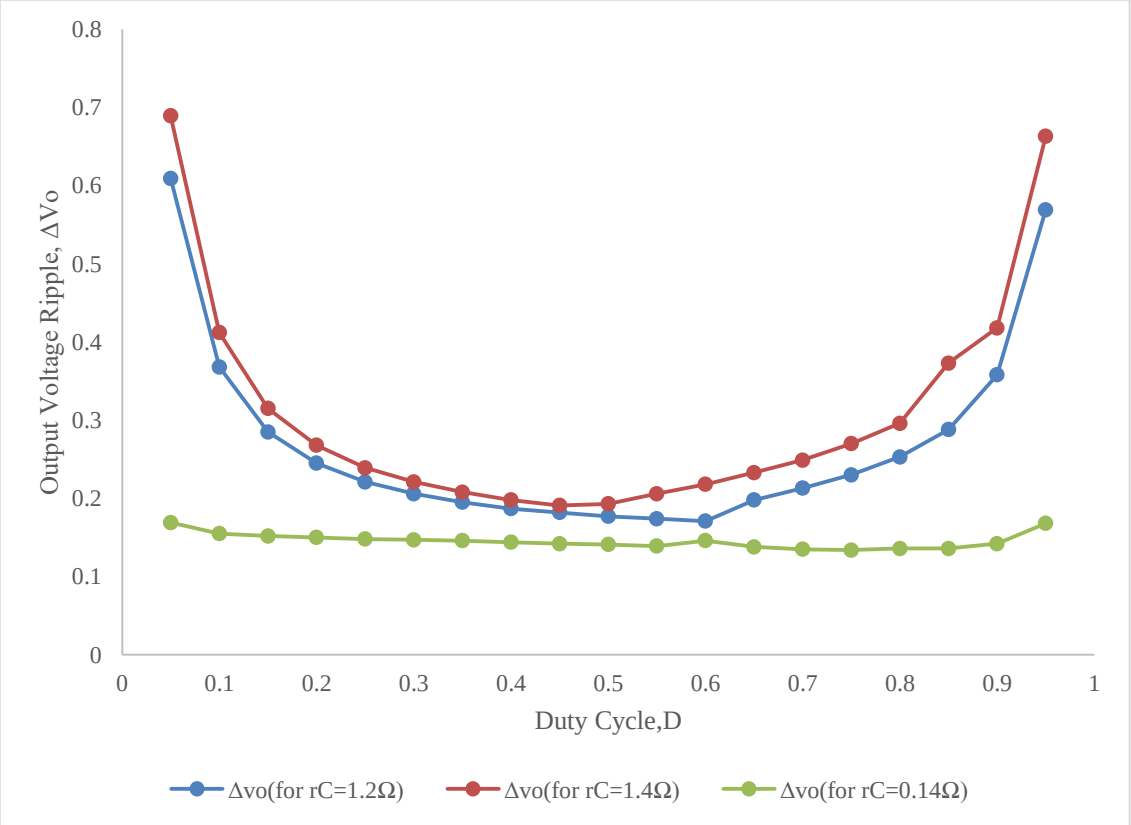

Figure 4-5 Graph of output voltage ripple against duty cycle of flyback converter

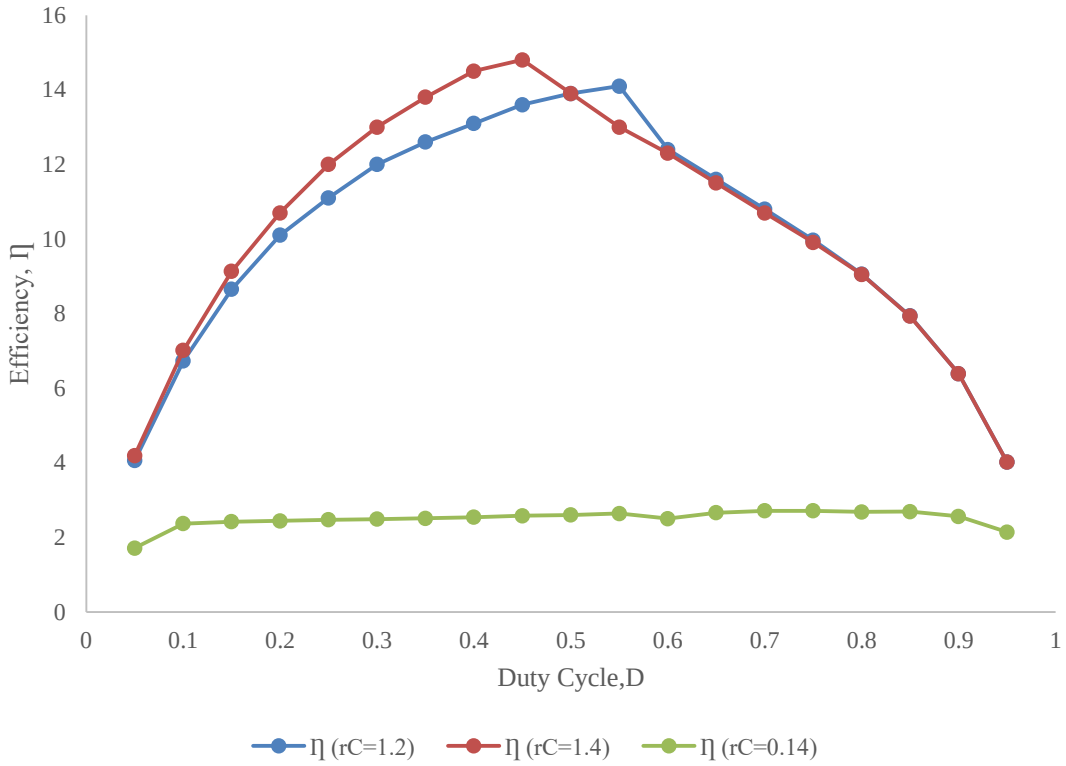

Figure 4-6 Graph of efficiency against duty cycle of flyback converter

From Figure 4-6 showed that the efficiency of the flyback converter increased from 0.05 to 0.55 of duty cycle. Then, it decreased from 0.60 to 0.95 of duty cycle.

CHAPTER 5

CONCLUSION

5.1 Conclusion

In conclusion, the aim of this project are to analyse the effect of parasitic on output voltage ripple and analyse the effect of parasitic on efficiency. The value of 1.2Ω ESR gives higher output voltage ripple for all converter while the value of 0.014Ω gives the lowest output voltage. Efficiency higher when the value of 1.2Ω of ESR used in design circuit for all converter while the value of 0.014Ω gives the lowest efficiency.

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