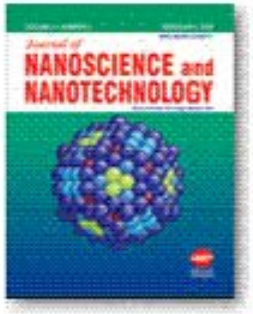

Optimization of Resistance Load in 4T-Static Random-Access Memory Cell Based on Silicon Nanowire Transistor

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This study explores optimization of resistance load (*R*-Load) of four silicon nanowire transistor (SiNWT)-based static random-access memory (SRAM) cell. Noise margins and inflection voltage of butterfly characteristics with static power consumption of SRAM cell are used as limiting factors in this optimization. Range of *R*-Load used in this study was 20–1000 KΩ with V_{dd} = 1 V. Results indicate that optimization depends critically on resistance load value. The optimized range of *R*-Load is 100–200 KΩ.

Keywords: 4T-SRAM; CMOS; Digital Inverter; Nanowire; R-Load; SiNWT

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