DEVELOPMENT OF AUTOMATIC POWER FACTOR CORRECTION DEVICE

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This thesis is submitted as partial fulfillment of the requirements for the award of the
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Specially dedicated to my beloved family and those people who
have guided and inspired me throughout my journey of education

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ABSTRACT

Nowadays the life cost more getting higher and higher. People more consider every dollar that they spend in their daily life. The price of gasoline more getting higher every year, this also make the life cost for each family increase. The price of electricity also increases because of the increase gasoline price. The people should spend their money with efficiently to make sure that the money that they spend is totally useful. There have two methods to save the electricity usage; the first one is using the electricity energy with smart, for example when the air-conditioner is not used it should turn off. The second is using the power factor correction technique, but this method just for inductive load such as air-conditioner, washing machine and refrigerator. The inductive load running causes the leading power factor, means the current that used is more and not totally used. To overcome this problem the reactive component is added, the capacitor is added to improve the power factor and also reduce the current that transfer to the inductive load. The microcontroller (PIC) is use as a control element that switching the capacitor to the power line. The sensor is place at the power line to giving the signal to the microcontroller, microcontroller analyze the signal that feed from the sensor. Microcontroller execute the instruction depend to the signal that giving.

ABSTRAK

Pada setiap tahun taraf hidup semakin meningkat dan setiap orang mengira setiap ringgit yang mereka belanjakan. Pada setiap tahun juga harga bahan api terutamanya petrol meningkat berikutan perminataan yang tinggi oleh setiap Negara. Ini menyebabkan tarif elektrik meningkat berikutan meningkatnya harga bahan api di pasaran. Setiap orang perlu menggunakan duit mereka dengan bijaknya bagi menanpung perbelanjaan sara hidup yang makin meningkat. Bagi mengurangkan beban yg ade mereka seharusnya menggunakan elektrik dengan sebaiknya. Ada dua kaedah untuk menjumatkan penggunaan elektrik, salas satunya ialah menggunakan elektrik dengan jimat cermat sebagai contoh apabila tmeninggalkan bilik penyaman udara dan perkakas elektrik yang lain seharusnya dimatikan. Keadah ini berkesan bagi menjimatkan elektrik tetapi penggunaan elektrik masih tidak efisyen. Kaedah kedua adalah menggunakan teknik pembetulan faktor kuasa, tetapi kaedah ini hanya berkesan bagi alat yang mengunakkan applikasi moto. Apabila alat berplikasi moto bekerja faktor kuasa dalam talian kuasa menjadi rendah iaitu mengekori. Bagi membetulkan balik komponent reaktif diperlukan, kapasitor adalah komponent reaktif digunakan bagi membetulkan balik faktor kuasa. Pemprosesan Kawalan Mikro (PIC) digunakan bagi mengawal kemasukan kapasitor dalam talian. Kemasukan kapasitor bergantung kepada masukan data daripada peranti pengesan. Ini mengelakan daripada faktor kuasa mendahui daripada terjadi.

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LIST OF ABBREVIATIONS

AC   –   Alternate Current

ADC   –   Analog to Digital Converter

DC   –   Direct Current

APFC   –   Automatic Power Factor Correction

Vac   –   Voltage alternate Current

LED   –   Light Emitting Diode

LCD   –   Liquid Crystal Display

PIC   –   Programmable Intelligent Computer

Vdc   –   Voltage Direct Current

TNB   –   Tenaga Nasional Berhad

VAR   –   Unit of Appearent Power

V_o –   Output Voltage

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CHAPTER 1

INTRODUCTION

1.1.   Project Background

In the recent year the life cost is getting more expensive and the people need to consider all the money that they spend. The electric tariff from TNB getting higher in every year because the electric tariff, depend to the price of gasoline. The electricity bills is the one of the life cost that need to support because without electric people can't do their daily life. To minimize the electric bill in the manual method is try to use the electric with the smart. The other method to minimize the electric bill is used the automatic power factor correction (power saver).

This project is focus on the design and building a unit of automatic power factor correction, this device more suitable and effective in the house that used a lot of inductive component such as air-conditioner, washing machine and etc. This device is function as the power factor corrector to improve the power factor to unity. The value of capacitor that insert in the system is depend to the value of power factor that control by microcontroller.

The problems of this we have to determine the value of the power factor and the value of the capacitor that we need to insert in the system. The value of the

capacitor is the most important because it will change the power factor to unity and significantly the current to the load is reduce. This is the main problem we have to focus because it will determine the percentage of the save the electricity.

1.2. Objectives:

The objectives of this project are:

I. Develop automatic power factor correction (power saver)
II. This device able to reduce the power consumption in the house and minimize the electricity cost.
III. To help the people reduce the life cost by reduce the electricity cost.

1.3. Scope of Project

The scope of this project can be summarizing as follows:

I. This projects focus on the single-phase system 240Vac, for house application.
II. The maximum current rating is 40A, suitable for house that usually current rating is same.
III. Device use 4 parallel capacitors to improve power factor.
IV.

1.4. Literature Review

The power factor of an AC electric power system is defined as the ratio of the real power to the apparent power, and is a number between 0 and 1. Real power is the capacity of the circuit for performing work in a particular time. Apparent power is the product of the current and voltage of the circuit. Due to energy stored in the load and returned to the source, or due to a non-linear load that distorts the wave shape of the current drawn from the source, the apparent power can be greater than the real power. Low-power-factor loads increase losses in a power distribution system and result in increased energy costs [1].

The significance of power factor lies in the fact that utility companies supply customers with volt-amperes, but bill them for watts. Power factors below 1.0 require a utility to generate more than the minimum volt-amperes necessary to supply the real power (watts). This increases generation and transmission costs. For example, if the load power factor were as low as 0.7, the apparent power would be 1.4 times the real power used by the load. Line current in the circuit would also be 1.4 times the current required at 1.0 power factor, so the losses in the circuit would be doubled (since they are proportional to the square of the current). Alternatively all components of the system such as generators, conductors, transformers, and switchgear would be increased in size (and cost) to carry the extra current [2].

Interfacing the microprocessor with the AC power lines need to consider the voltage, current and also power dissipated by the microcontroller (PIC). The PIC chip only support 1W power dissipation [1]. The phase voltage and current is detected using the current and voltage transducer. Using the external existing unique function (zero crossing detector) in PIC16F77 the phase shift between voltage and current is determine [1]. High external resistor must be connect place before connect to input circuit, to ensure that PIC not damage. PIC 16C5X series is design to short the input when the large voltage is applied to protect the chip from static electric short [3].

The Hall Effect sensor is the one device that used to interface between the power line and the microcontroller (PIC) [4]. This sensor is connecting series with the inductive load. It has an internal current transducer that senses the electromagnetic field. It also produce the output voltage that suitable for the PIC (0V-5V), this output voltage is in AC because use in the AC application, it also suitable use in DC application. This device precise is depending to the temperature, it sense the fully scale current at the 25^oC [4].

1.5.   Report Outline

This report is divided into six chapters. Chapter 1 is explaining about the background of the project, objectives, scope of project and literature review. Chapter 2 explaining about the power factor, phase and phasor diagram, automatic power factor correction, current sense conventional APFC and summary for this chapter. The new automatic power factor correction device (power saver) should have ability to reduce the power factor to unity when the inductive component exists in the system. This device should have a correct trigger the step of the capacitor to accomplish the value VAR in the system and the current transfer to load is less. Chapter 3 explain about the control element circuit, the PIC 18F4550 is used as a brain of the system, this microcontroller PIC is used to monitor all the changing current in the system that feed by the current sensor. The porta is used to feed the input because only porta have the special features that can receive analog input. The oscillator is the important thing that generates the frequency when the voltage is given. The frequency generate is feed to the microcontroller and as a clock for microcontroller to function. Microcode studio is used to write and compile. It convert pbp file to the hex file. The PICkit is used to burn the program to the microcontroller, the hex file is transfer to the PICkit program and it transfer into microcontroller. Chapter 4 explains about methodology of the project. The power factors is study fist and also find the technique to improve the power factor. The purpose design for this project is using the current sensor as the input and the driver

relay circuit as an output. The current sensor is feed the signal to the microcontroller, the microcontroller analyze and give the output to the driver relay circuit according the condition that stated in the programming. Chapter five explain about the result and discussion, the result of the power factor is determined using the motor load. There have two type of motor used, first is 600W motor, the current 0.3A are reduce after the APFC operate. The initial power factor is 0.83pf and after insert the capacitor insert the power factor become 0.92pf. Second is 1.32KW motor, current 0.5A are reduce after APFC operate. The initial power factor is 0.77pf and after insert capacitor the current is 0.83pf. Chapter 6 explains about the conclusion and suggestion. This device is able to reduce the current usage by the inductive load.

CHAPTER 2

AUTOMATC POWER FACTOR CORRECTION (APFC)

2.1.   Introduction

Power factor is the ratio of true power or watts to apparent power or volt amps. They are identical only when current and voltage are in phase then the power factor is 1.0. The power in an ac circuit is very seldom equal to the direct product of the volts and amperes. In order to find the power of a single phase ac circuit the product of volts and amperes must be multiplied by the power factor. Ammeters and voltmeters indicate the effective value of amps and volts. True power or watts can be measured with a wattmeter. If the true power is 1870 watts and the volt amp reading is 2200. Than the power factor is 0.85 or 85 percent. Real power divided by apparent power. The power factor is expressed in decimal or percentage. Thus power factors of 0.8 are the same as 80 percent. Low power factor is usually associated with motors and transformers. An incandescent bulb would have a power factor of close to 1.0. A one hp motor has power factor about 0.80. With low power factor loads, the current flowing through electrical system components is higher than necessary to do the required work. These results in excess heating, which can damage or shorten the life of equipment, a low power factor can also cause low-voltage conditions, resulting in dimming of lights and sluggish motor operation.

Low power factor is usually not that much of a problem in residential

homes. It does however become a problem in industry where multiple large motors are used. So there is a requirement to correct the power factor in industries. Generally the power factor correction capacitors are used to try to correct this problem.

For a DC circuit the power is P=VI and this relationship also holds for the instantaneous power in an AC circuit. However, the average power in an AC circuit expressed in terms of the rms voltage and current is

$$P_{avg} = VI \cos\varphi$$

Where, φ is the phase angle between the voltage and current. The additional term is called the power factor. Power factor triangle is shown in Figure 2.1.
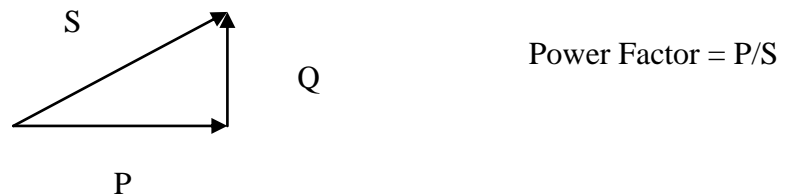
Power Factor = P/S

Figure 2.1: Power Factor triangle

From the phasor diagram for AC impedance, it can be seen that the power factor is P/S. For a purely resistive AC circuit, P=S and the power factor = 1.

2.2.   Phase and Phasor Diagram

When capacitors or inductors are involved in an AC circuit, the current and voltage do not peak at the same time. The fraction of a period difference between the peaks expressed in degrees is said to be the phase difference. The phase difference is <= 90 degrees. It is customary to use the angle by which the voltage leads the current. This leads to a positive phase for inductive circuits since current

lags the voltage in an inductive circuit. The phase is negative for a capacitive circuit since the current leads the voltage. Figure 2.2 shows the waveform for voltage and current when the power factor is leading. The current lead the voltage because the inductive component running.
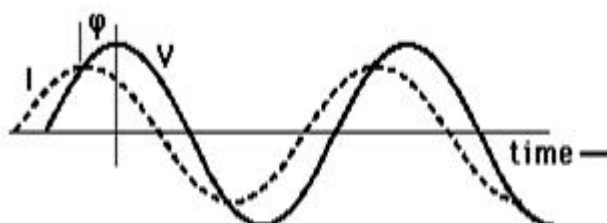
Figure 2.2: Phase Diagram for leading PF

2.3   Automatic Power Factor Correction

An automatic power factor correction (APFC) is a device that used to improve the power factor to unity using the microcontroller. Usually the automatic power factor correction is used in the industry such as the factory that used the biggest horse power (hp) motor. Such as the chiller system, chiller system is the one of the type air-conditioner. This chiller used the motor to operate; motor is used as pump to pump the water for each floor in the building. The motors that used have 200hp each to pump the water in each floor. This motor is operate when the temperature high inside the building and off when the temperature reach at the desire level. The automatic power factor correction is needed here because to maintain the value of the power factor unity. The value of power factor unity is important because it will affect the current and voltage drop in the system. Second is TNB will give the penalty if the power factor below that 0.8, power factor below that 0.8 need to supply more energy to this system and make them loss out. This device is function to monitor the system that makes sure that the value of the power factor approach to unity.

2.4   Operation of APFC

The automatic power factor correction is the device the used the microcontroller to analyze the power factor in the system. The microcontroller is the brain of the system because where the power factor is analyze and determine the value. Microprocessor receives the signal from the voltage and current transducer. Microprocessor is build in the analog digital converter,   This ADC is used to convert analog signal to the digital signal, the digital signal from the current and voltage transducer is analyze. To determine the power factor zero-crossing detector is used. The programming of microprocessor is the most important because, if the inductive components running the voltage are lagging current. The signal from the current transducer will on the timer and the signal from voltage off the timer, from the delay between the current and voltage the power factor is determine. Figure 2.3 show the time delay between current and voltage.
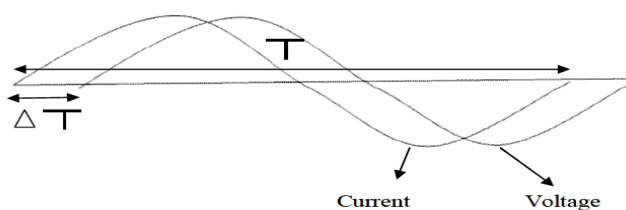
Figure 2.3: Waveform voltage and current

The value of capacitor is depends to the value of the VAR that used in the system (motors). The microprocessor will give the signal the contactor to turn on capacitor to the system depend to the value of VAR that used. The steps of the capacitor usually for the system is depend to the how many the inductive component (VAR) in the system. That means before the automatic power factor is design the value of the VAR in system need to know first and the how many steps of the capacitor will determine. The figure 3.2 shows the block diagram for the system.
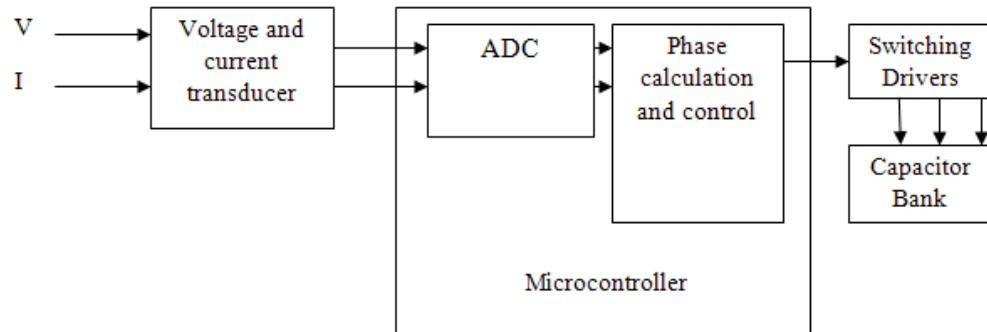
Figure 2.4: Block diagram Power factor Controller

2.5   APFC Design

There are two circuits for design automatic power factor correction. First is control circuit that consists of microcontroller, two transducers and driver relays. Second is power circuit that consists of capacitor bank and relay.

2.5.1   Relay

A relay is an electrical switch that opens and closes under the control of another electrical circuit. In the original form, the switch is operated by an electromagnet to open or close one or many sets of contacts. Because a relay is able to control an output circuit of higher power than the input circuit, it can be considered, in a broad sense, to be a form of an electrical amplifier. Current flowing

through the coil of the relay creates a magnetic field which attracts a lever and changes the switch contacts. The coil current can be on or off so relays have two switch positions and they are double throw (changeover) switches. Usually this is a spring, but gravity is also used commonly in industrial motor starters. Most relays are manufactured to operate quickly. In a low voltage application, it is used to reduce noise. In a high voltage or high current application, it is used to reduce arcing. The symbol circuit of relay and the relay are shown in Figure
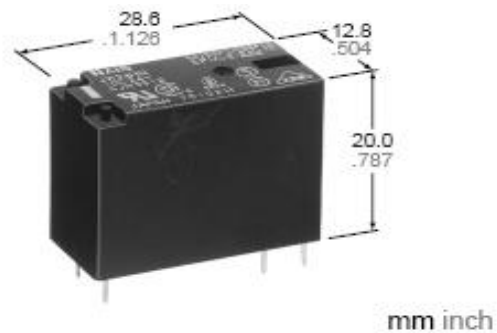
Figure 2.5: Relay

2.5.2   Current Transducer

There are several types of current detector such as current transducer, transtronics current detector and current transformer which are use for detected current by sensing the AC current. This device is function when the wire carrying the current through the coil. The magnetic field form from the wire will detect, the coil consist in the current transducer will induce the current, acting like transformer. Figure 3.4 below the current transducer. The application of current transducer normally use in sensing overload current, ground fault detection, metering and analog to digital circuit.
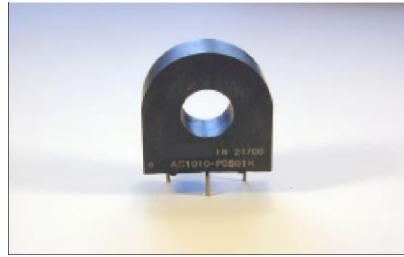
Figure 2.6: Current Transduccer

2.5.3 Voltage Transducer

Voltage transducer is function like a transformer. The voltage in the system will step down; the voltage step down is depending to the coil. For this project the voltage is step down from 240Vac to 5Vac, before the signal sense to the microcontroller the current is limited using the large value of the resistor. The high current produce when the transformer is step down, current is limited because the microcontroller can accept only 1W power consumption. The higher current will damage the microcontroller. Figure 3.5 show the LV 25-P voltage transducer.
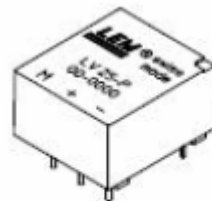
Voltage Transducer
LV 25-P

Figure 2.7: Voltage Transducer

2.5.4   Capacitor

Capacitor is the main important because it will improve the power factor and reduce the current that transfer to the load. The capacitor that used is has the voltage rating 400V. This value of the voltage rating is suitable for single phase. Figure 3.6 show the ELCO capacitor.
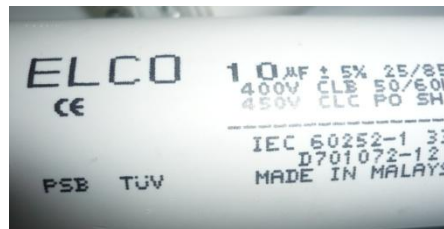
Figure 2.8: Capacitor

2.6   Summary

The power factor is exists when the capacitor and inductor component operate in the ac circuit. Usually the load is inductive load such as motor application, when the motor running the power factor in the system is low; to improve the power factor the capacitor component which called capacitor bank is inserting in the system. The value of the capacitor is depending to the value of the VAR that used. The current sense for APFC is not suitable because not efficiency to improve the power factor and also reduce the current used by inductive components. The automatic power factor correction device consist two circuits, control and power circuit. The control circuit consist of transducers, microcontroller and drivers relay. The signal is feed to the microcontroller using the transducers. Microcontroller analyzes the power factor in the system and sends the signal to the drivers relay. The

driver relay will on the steps of capacitor depend to the power factor. This process continuous until the power reaches to power factor unity.

CHAPTER 3

CONTROL ELEMENT CIRCUIT

3.1   Introduction

PIC is widely used to as a control element circuit for the device or electrical equipment. PIC is a family of Harvard architecture microcontrollers made by Microchip Technology, derived from the PIC164originally developed by General Instrument's Microelectronics Division. The name PIC initially referred to "**Peripheral Interface Controller**". PICs are popular with developers and hobbyists alike due to their low cost, wide availability, large user base, extensive collection of application notes, availability of low cost or free development tools, and serial programming (and re-programming with flash memory) capability. The Harvard architecture is different with the von Neumann architecture because it can read an instruction and perform the data memory access at the same time. This is because this Harvard architecture can read and writing in the same time and this significantly to the times taken to execute the instruction. This Harvard architecture also take less time and more efficiency to execute the instruction and it user friendly because the programmer easy to write the program.

3.2   Microcontroller (PIC) Features

The feature of microcontroller (PIC) is can only operate when two Vcc (5Vdc), two Gnd (0Vdc) and one oscillator. The PIC will blow if the voltage exceed 5Vdc is given and the polarity is reverse are connected. The microcontroller (PIC) is easy to use because is no additional memory and no need to connect the buffer or latch circuit to interface with the input or output device.

3.2.1   PIC 18F4550

The type of the microcontroller (PIC) that chooses for this project is PIC 18F4550, this PIC has 40 pins and has four ports. The PIC function when the 5Vdc is apply and the oscillator is connect, the diode is add at the Vcc pin to avoid the damage when the user incorrect connect between Vcc and Gnd. The port for this PIC is porta, portb, portc and portd, porta is the special port because it has the analog digital converter. The function analog digital converter is to convert the analog signal form to the digital signal form because build in microprocessor only understand the digital signal to function. Another port is use as the digital port, it only understand the logic 1 (5Vdc) or logic 0(0Vdc). This port can be set whether input the output using the program declaration. The oscillator is used to generate the frequency (pulse form) to the microcontroller, the more high value of oscillator more fast the program or instruction execute by the PIC. The pins 11 and 32 are connecting with the Vcc (5Vdc0), pins 12 and 31 are connecting with the Gnd (0Vdc) and the pins 13 and 14 are connecting to the oscillator. The figures 3.1 below show the PIC 18F4550 pins.
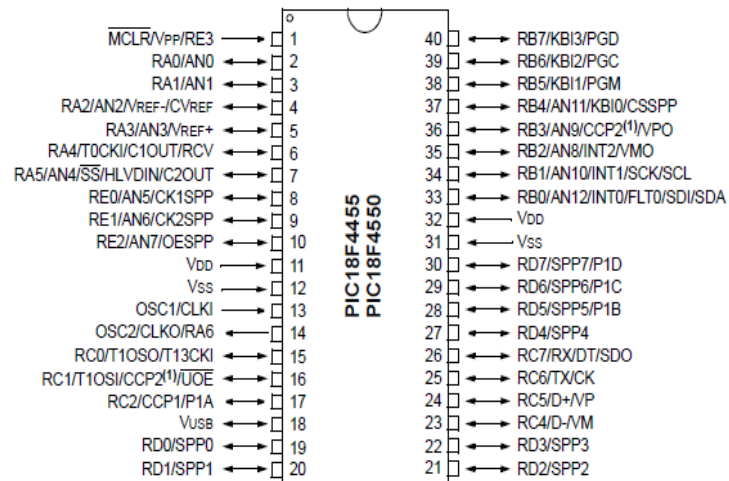
Figure 3.1: PIC 18F4550 Pins Diagram

3.2.2 Input and Output Port Used

The input and output use for this project are porta, portb and portd. The porta is set as a input port, this port receive the signal from the sensor circuit. Porta ia a special port for the all type of PIC because it use for the analog input, this port is use for this project to given signal to the build in microprocessor, it convert the voltage level that receive from the sensor circuit to the digital form and send to the microprocessor. The maximum bit for ADC this PIC is 10 bits, this will define when the program is write. The pin no 2 is use as a analog signal output. The portb is use as an output to give the signal to the driver relay circuit to operate, it give the logic 1 (5Vdc) to the transistor to operate the relay. The portc is also use as an output for the LCD display. The interface with the LCD, PIC need use the special instruction in the program to operate the LCD. The figure 3.2 below show the connection input and output device with the PIC.
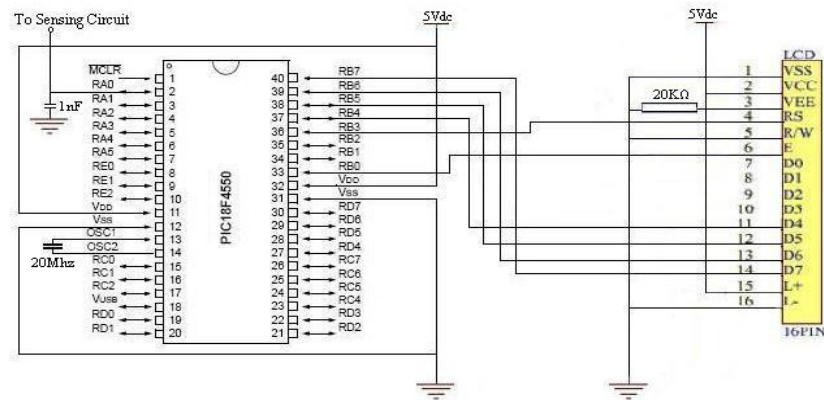
Figure 3.2: Connection Input and Output

3.2.3   Crystal Oscillator

Crystal Oscillator is electronic circuits that use the mechanical resonant of a vibrating crystal of piezoelectric material to create an electrical signal with a very precise frequency. This frequency is commonly used to keep track of time (as in quartz wristwatches), to provide a stable clock signal for digital integrated circuits, and to stabilize frequencies for radio transmitters and receivers. The quartz need to cut properly to make sure that the amount of the frequency is reaches. When the voltage is applying to the quartz it will beat and generate the frequency, the quartz crystal is behaved like a circuit composes of an inductor, capacitor and resistor with precise of the frequency. The quartz crystal is equivalent with the RLC circuit. The value of the crystal come to many size (Mhz), it depend to the cutting of the quartz stone. The figures 3.3 show the symbol and equivalent circuit for the crystal oscillator.
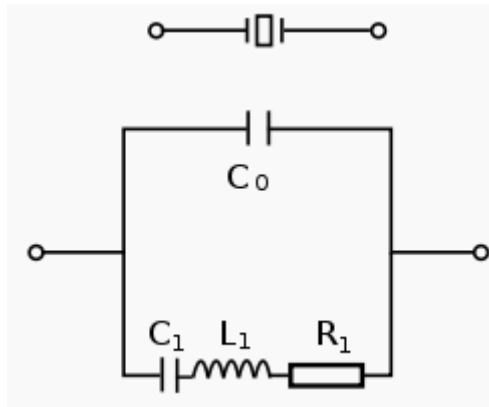
Figure 3.3: Symbol Crystal and Equivalent Circuit

3.3   Software and Hardware Implementation

Software that use for this project function to make the programmer easier to write the program, the language used is C language. The C language is easy because the programmer easy t understand the function of the instruction. The instruction is the word that has the sir turn task for the microcontroller (PIC) to execute the task that has been burn into microcontroller.

3.3.1   Microcode Studio

MicroCode Studio is a powerful, visual Integrated Development Environment (IDE) with In Circuit Debugging (ICD) capability designed specifically for microEngineering Labs PICBasic PRO compiler. The code explorer allows you to automatically jump to include files, defines, constants, variables, aliases and modifiers,

symbols and labels that are contained within your source code. It's easy to set up your compiler, assembler and programmer options or you can let MicroCode Studio do it for you with its built in autosearch feature. Compilation and assembler errors can easily be identified and corrected using the error results window. MicroCode Studio even comes with a serial communications window

The In Circuit Debugger (ICD) enables you to execute a PICBasic Program on a host PIC microcontroller and view variable values, Special Function Registers (SFR), memory and EEPROM as the program is executing. You can toggle multiple breakpoints and step through your PICBasic code line by line. The graphical interface is built on microEngineering Labs debug architecture, which is both efficient and robust. In this project, there are several steps that have to setup first before write the program and compile it.

Step 1, below, is step to configure programming. In this project, we use PIC18F4550. So, we must select configuration of PIC18F4550 in figure 3.4 below.
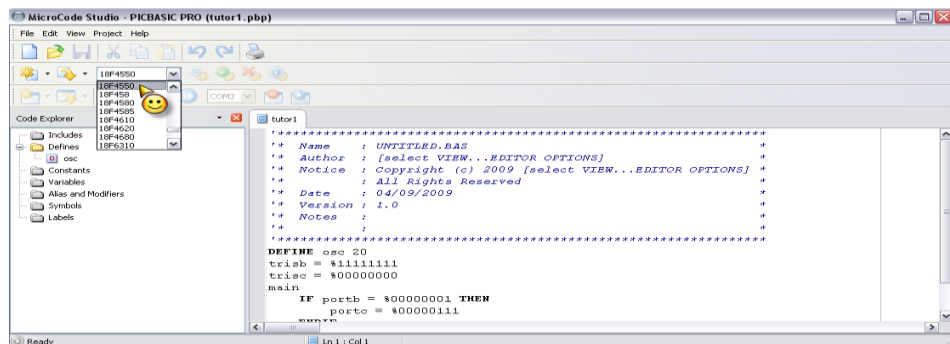
Figure 3.4: Configuration PIC18F4550

Step 2, we must define oscillator 20MHz. It is because, in the project we use oscillator 20MHz. Define ADC (analog to digital) 8 bits. ADC clock sample = 3 and ADC sampleus = 50. Figure 3.5 below show how to setting.
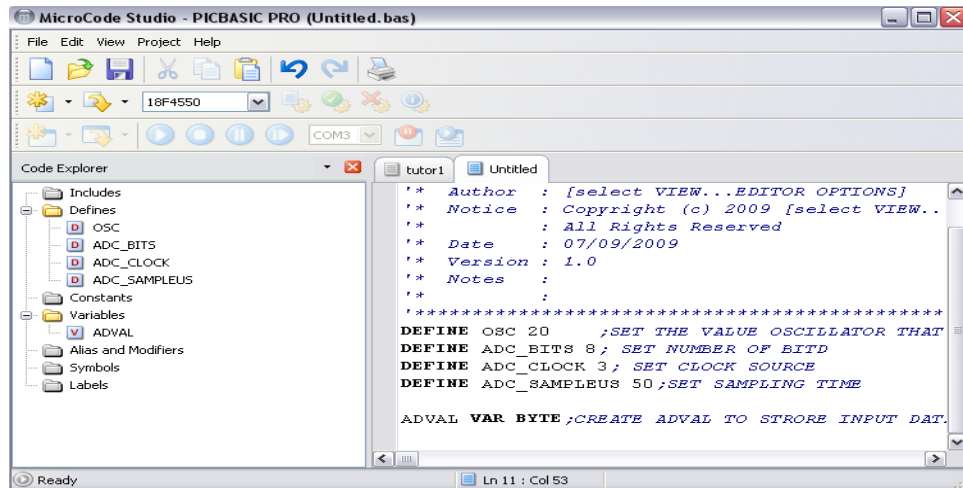
Figure 3.5: Setting the Analog Digital Converter

Step 3, after all of setting has been configured, it may be able to be written according to the flowchart of microcontroller based power factor correction Cart program. Then after finishing write the program, it has to be compiling using the compiler button or press F9. This action has to be perform because it can check whether there is error or misuse command while write the program. The Figure 3.6 shown how to compile and checking error.
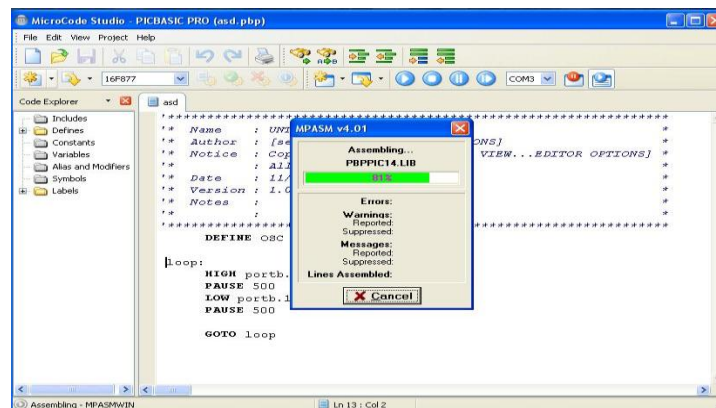
Figure 3.6: Compile and Checking Error

3.3.2   PICkit USB Programmer

PICkit USB programmer is used to write (burn) PIC. The device is design to interface between the computer and the microcontroller (PIC). The USB port is used to transfer the data from the computer to the PIC. This device has the PIC holder that used to make sure the PIC's pins connect with the holder. Figure 3.7 show the picture of the PICkit programmer. There have five component to operate this device, first UIC00A is used as a driver to interface between PIC and computer, second mini USB cable, third rainbow cable to connect between UIC00A with the no five, fourth software installation and user's manual CD and fifth UIC-S socket board use to hold the PIC.

Figure 3.7: PICkit USB Programming

3.3.2.1 Plugging the Microcontroller (PIC)

The microcontroller must be plugging in the UIC-S socket with proper because cause the damage to the microcontroller (PIC) if the wrong instruction use. There have two types to program the PIC, first if the pins of the PIC if less than 18 pins the switch

of the bottom must be select 18 pins and the microcontroller (PIC) must be put at the UIC-S socket as show in the figure 3.8. The first step, place the PIC at the UIC-S socket, second make sure that the dot mark at PIC is the right as show in the figure (2) above and the last is make sure that the switch is select at the 18 pins direction like show in figure.
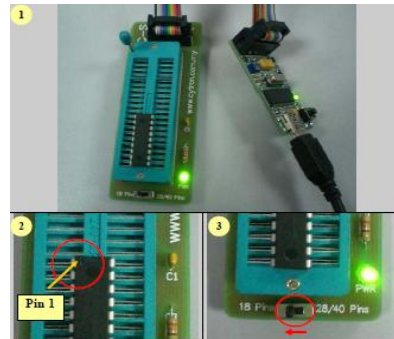
Figure 3.8: Plugging 18 pins PIC

The second type is the PIC pin is 28 to 40 pins, the switch must be select at the 28/40 pins. The figure 3.9 below show the PIC has the 40 pins put at the UIC-S socket. The first step, place the PIC at the UIC-S socket, second make sure the dot mark at OIC is the right side as show in figure and third is make sure the switch is select at the 28/40 pins direction.
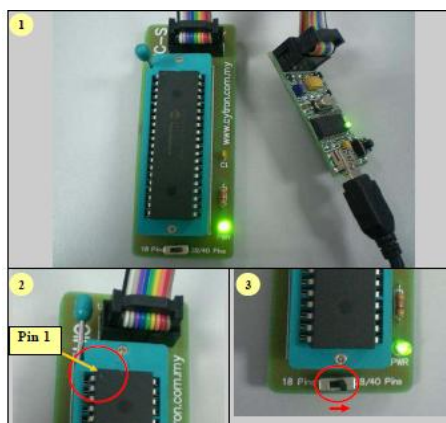
Figure 3.9: Plugging 40 pins PIC

3.3.2.2 Program the PIC Microcontroller

To program the PIC using the PICkit USB programmer, the Hex file must be produce first. The Hex file is getting from the microcode, where the C language is write and the language is compile using the compiler that has in the microcode. After C language is compile and the error has been check the Hex file will exist, this Hex file is at the where the Sps file is save. The software PICkit is install in the computer using the instruction that stated in the CD. Finish the installation the icon PICkit appear in the desktop, double click the icon and the software is running, it automatically detect the PIC that place at the UIC-S socket as show in figure 3.10 below.
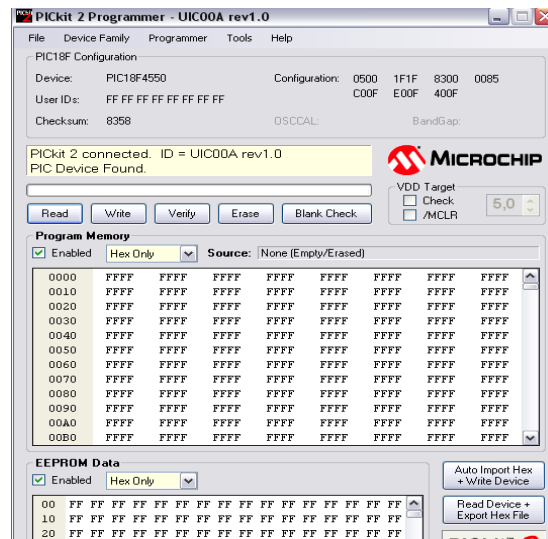
Figure 3.10: PIckit Programmer

Before the Hex file imported, the PIC nee to blank check first to make sure that there no program that exist in PIC. If have the program in the PIC the program need to erase first, to erase the program the erase button is press. The erase is complete when the no blinking red LED in the UIC00A. Then the verify button is press to verify the PIC is located at the right pins. Lastly click file at the top of the PICkit program and choose import Hex. After Hex file is import the button write is press to write the program to the PIC. The red LED is blink at the UIC00A and when red led stop blink the green LED id

turn on, it show that the program is completely transfer to the PIC. This called burn process. The figures 3.11 above show the import Hex file to PICkit programmer.
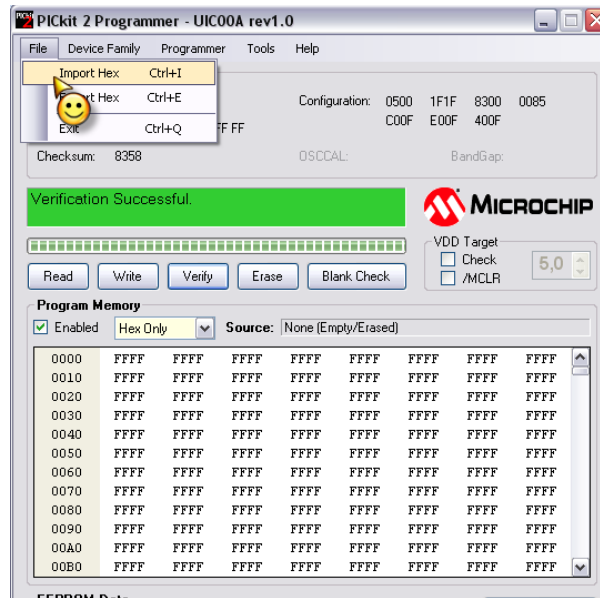
Figure 3.11: Import Hex File

3.4   Summary

This chapter explains about the function of the PIC as the control element, there have four port at the PIC which is porta, portb, portc and last portd. Porta is the special port because it analog input, this port function to interface with the analog signal that produce from the input circuit. Microcode studio is the software that used to write the C language, the user is easier to write using this language compare to the assembly language. This software also converts the Sps file to the Hex file. The programmer PICkit is used to program the PIC, it functions to interface between the PIC and the user computer. The Hex file that produce from the microcode studio is imports to this programmer and transfer to the PIC with press the write button.

CHAPTER 4

DEVELOPMENT OF AUTOMATIC POWER FACTOR CORRECTION DEVICE

4.1   Introduction

This chapter explains about the hardware design include the power supply circuit, PIC controller circuit, current sensor circuit and driver relays circuit. This chapter also explains about the software design that used to program the microcontroller (PIC) that using the C language, PIC18F4550 and the complete operation of the project system.

4.2   Project Flow

The project begins with study the equipment in the house that uses the inductive component to operate. The inductive component in the house such as washing machine, air-conditioner and refrigerator, all this component make the power circuit in the system has a power factor. The lagging power factor is happened when this equipment running and also draw more current. To prevent this happen the power factor correction technique is studies, according to the power factor correction the lagging power factor can be improve to unity by adding the capacitor series with equipment. The value of the

capacitor is determined depending to the load that running in one time. This can be avoiding from the power factor become leading. The leading power factor is also become a problem, the capacitor become a load and also draw a current. The sensor is used to sense the current in the system, the type of the sensor is Hall-effect current sensor. The rating of this current sensor is up to 50A, which is suitable for house application. This current sensor converts the current signal into voltage form that suitable for PIC. The analog input PIC is used to monitor the current in the system. The microcode studio is the program that used to write the program to the PIC. It converts the pbp file to hex file. This hex file used to program PIC using PICkit programmer. Before program is writing we need to study the features of the PIC that used. After programming is finish the hardware is test using the single phase motor that located in the library.

4.3   Proposed Design
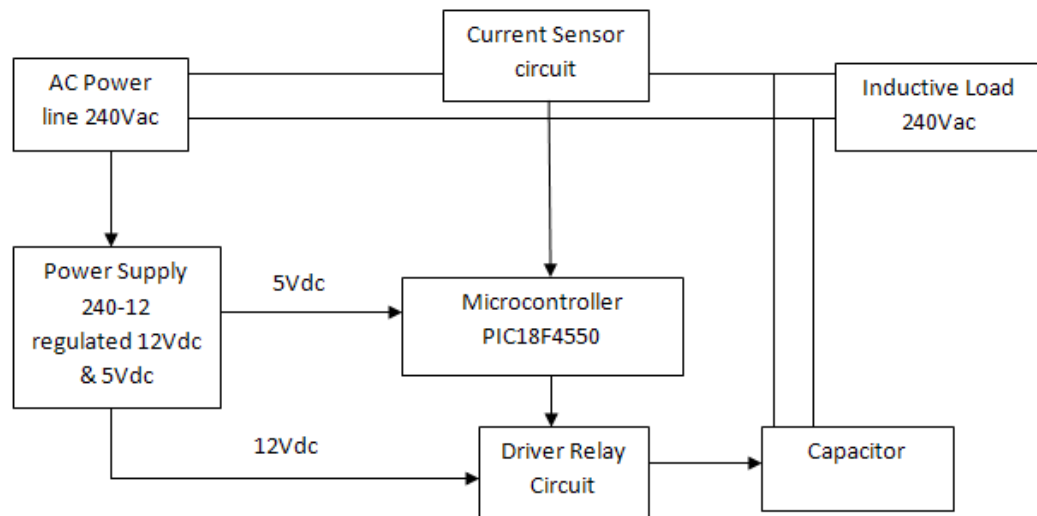
Figure 4.1: Propose Design of APFC

Figure 3.1 above show the proposed design for single phase automatic power factor correction device. It divide into four parts, the first part is power supply. The

power supply design to supply the voltage to the microcontroller and the driver relay circuit. The transformer is used to step down the voltage 240Vac to 12Vac and the bridge rectifier to rectify the AC to DC. There have two voltage regulator, first is regulate 5Vdc to supply to the microcontroller and regulate 12Vdc to supply to the driver relay circuit. The second part is current sensor circuit; the current sensor is specially design to the microcontroller to interface with the ac lines power because it produce maximum voltage 5V, for example rating current sensor 50A maximum the output voltage is 5V. This part is monitoring the current in the system and gives the signal to the microcontroller in the voltage form. In the part also has a bridge rectifier to rectify the signal that produce by the current sensor (AC voltage) into DC voltage. This process to make sure that the program is not complicated and more accurate to compare with the interface with the AC voltage. The third part is microcontroller part (PIC), the PIC function as a brain of the system it analyze the signal input that given by the current sensor circuit and given the output signal to the driver relay to insert the capacitor in the system. The fourth part is driven relay circuit. This circuit is use to interface between the relay and the output of the microcontroller using the transistor, the relay is used the 12Vdc to operate. The signal from microcontroller is used to turn on the transistor and when transistor on automatically relay function.

4.4   Hardware Design

Hardware designs are dividing in four parts. The first part is design the power supply part by using the Orcad for simulation. The second part is current sensor circuit by using the same method of simulation. The third part is constructing the PIC circuit and finally the fourth part is driver relay circuit also simulates using Orcad.

4.4.1 Power Supply

In this part, a power supply is developing to give supply to microcontroller (PIC) and the driver relay circuit. The transformer is use to step down the 240Vav to 12Vac, the 12Vac voltage is rectifier using the bridge rectifier. The full wave rectified flow to the capacitor to make the signal become DC wave, the function of capacitor is to eliminate the ripple that exist acting like the low pass filter. The more large size of capacitor more ripple is eliminated and smoother DC is getting. After the ripple is eliminate the voltage regulator is use LM7805, this regulator is function to maintain the output voltage to 5Vac. This is important because PIC only function well in this voltage level, if the voltage for PIC exceeds the 5Vdc the PIC will blow and damage. The voltage regulator can support up to 24Vdc, if more the voltage regulator will blow. The relay that use is need the 12Vdc to function, the supply for this circuit is taken before the voltage regulator. Figure 3.2 below show the simulation of the schematic power supply.
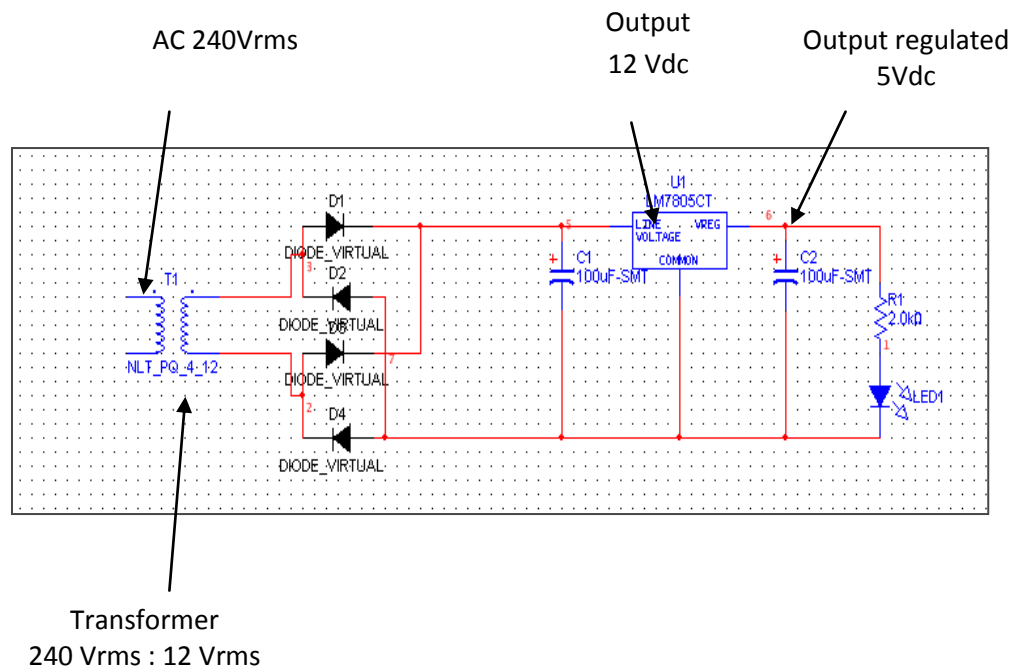
Figure 4.2: Schematic Power Supply

4.4.2   Current Sensor

Current sensor is use to interface the AC line with the microcontroller (PIC), the type of current sensor is use a ACS 754Xcb-050, this type of current sensor support up to 50A current rating which is suitable for this project. This sensor is connect series with the ac, inside this sensor it has the build in current transducer that function to detect the strength of the magnetic field produce by the wire when the load running. The AC lines are connecting with the terminal no 4 and no 5. This current sensor use 5Vdc supply to operate (pin no 1). The amplifier is amplifying the signal from current transducer and send to the low pass filter. This filter use to reduce the harmonic and send to the pin no 3 to the output signal. If no current is detecting the output voltage is 2.5V. This output pin produce the Vac but in small voltage. Figure 3.3 below show the block diagram of the current sensor.
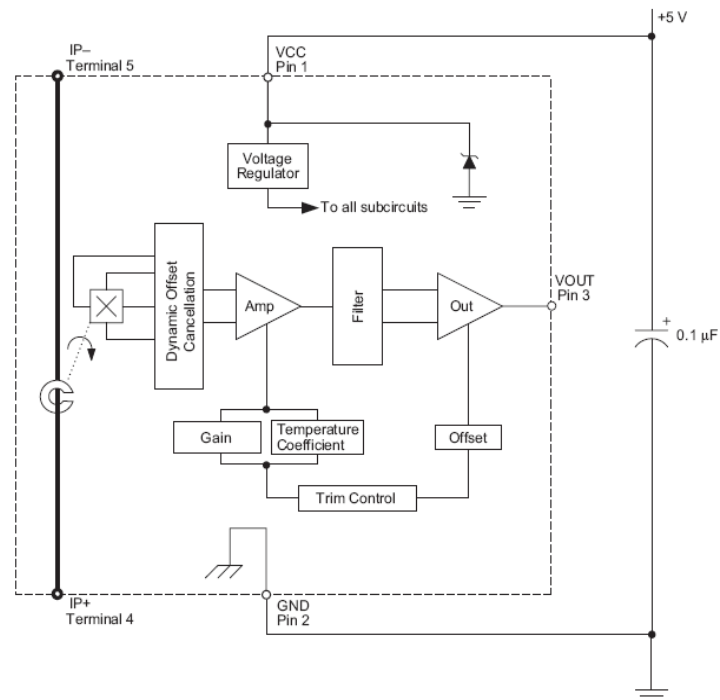
Figure 4.3: Block Diagram Current Sensor

To make this current sensor easier to use the output pin is connect with the bridge rectifier , the output of rectifier is connect with the capacitor to eliminate the ripple and the smooth DC voltage is getting. This make current sensor more easy to interface with

the PIC, the porta at the PIC is use to connect with the DC voltage that getting from rectifier. Porta is an analog input for PIC that use in this project. Programming is also easier if compare with the DC input voltage with the AC input voltage.

4.4.3   Driver Relay Circuit

Driver relay circuit is use to interface between the microcontroller (PIC) with the relay, because the relay that used in this project is 12Vdc to operate. The outputs signal that microcontroller produce (PIC) from the output pins is only 5Vdc. The control element that use is transistor, transistor is acting like a switch when the signal is given at the base pin. There have to type of transistors, first PNP type. It turns on (fire) when the logic zero or 0Vdc is given at base pin and allow the current through from the collector pin to emitter pin. The second type is PNP type, it operate when the logic one or 5Vdc is feed at pin base, transistor turn on and allow the current through from emitter pin to collector pin. The type of transistor is use in this project is NPN, because is easy to program and more simple circuit. The diode is connecting between two coil pins because to make sure that the relay is totally energize or deenergize. The Figure 3.4 below show the circuit diagram of the driver relay circuit.

12Vdc

Output from
PIC 5Vdc

Relay

NPN Transistor
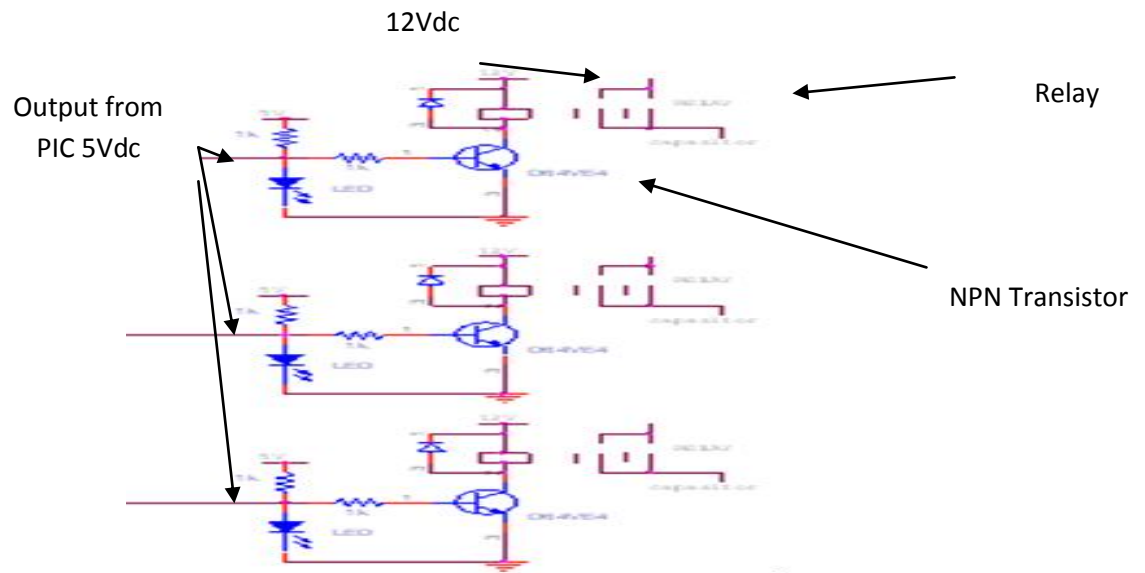
Figure 4.4: Schematic Driver Relay Circuit

4.4.4   Control Circuit

This is the most important part because these part functions as a brain of the system. The microcontroller (PIC) fully functions when the two Vcc, two Gnd and one oscillator is connecting. The 5Vdc Vcc is connecting to the pins 11 and 32, 0Vdc or ground is connecting at pins 12 and 31. The oscillator is use to generate the frequency for microcontroller to function, the bigger value of oscillator faster the microcontroller execute the operation. The value for oscillator is use in this project is 20MHz that connect at pins 14 and 15. The microcontroller monitors all the changing of the input voltage that produces by the current sensor circuit, the changing current in the power circuit effect to the output voltage that produce by current sensor. This signal is send to the analog input PIC. The 8 bit ADC use for this project, it means 0V represent 0bit and 5V represent 255 bits. The microcontroller analyze the voltage from the input that feed through the porta input pin, it working to send the signal (5Vdc) to the input pin and the

driver relay circuit to operate. Figure 4.5 below show the connection between PIC with input and output.
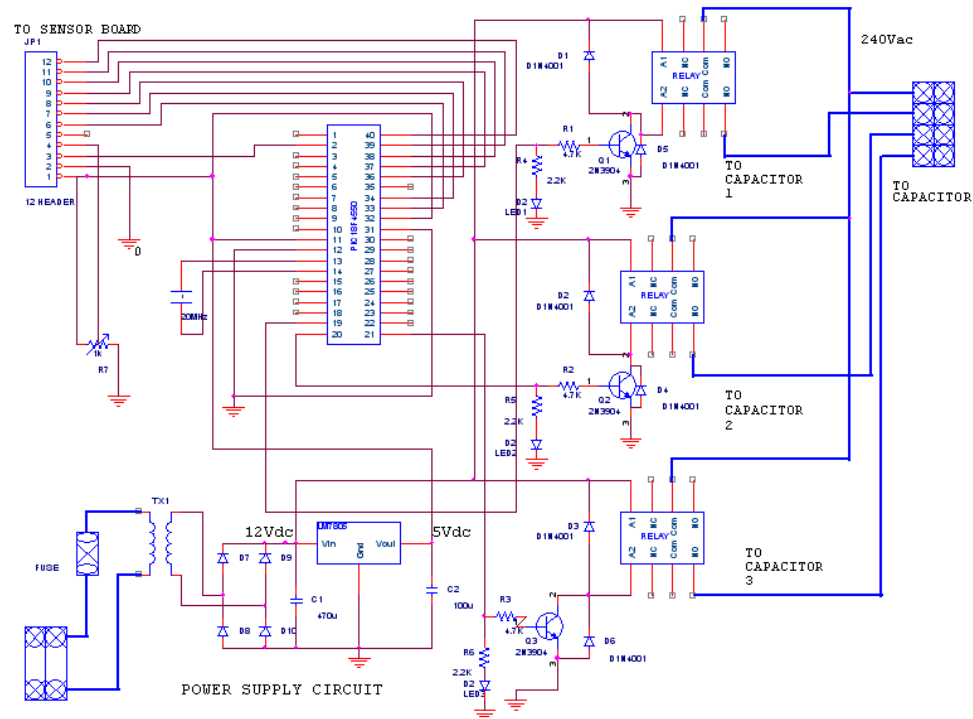
Figure 4.5: PIC with Input and Output Connection

4.5   Flow Chart

This project being with the current sensor read the value of the current in the power circuit and determine the value of the current and convert into voltage form. This value of the voltage is feed to the microcontroller (PIC). The PIC analyzes the signal and given the output to the driver relay circuit. If the current in range 4A < I < 6A the microcontroller PIC send the signal to insert one capacitor in the system, and if the current below that 4A return to the analyze signal again. Second is if the current in range 8 < I < 10A the microcontroller (PIC) switch on two relay which insert two capacitor in the system, and if this condition not meet rules the PIC test input again. Third is if the

current in range 12A < I < 14A the microcontroller (PIC) switch on three relay which insert three capacitor in the system. This flow always feedback to maintain the inductive load running with the inserted capacitor in the power line. Figure 4.6 below show the flow chart of the system.

```
                          ┌─────────┐
                          │  START  │
                          └─────────┘
                               │
        ┌──────────────────────┤
        │                      │
        │              ◇ If current ◇
   No   │              ◇  4A<I <6A  ◇
   ←────┤              ◇            ◇
        │                      │ Yes
        │              ┌───────────────┐
        │              │ One capacitor on │
        │              └───────────────┘
        │                      │
   No   │              ◇ If current ◇
   ←────┤              ◇ 8A<I <10A  ◇
        │                      │ Yes
        │              ┌───────────────┐
        │              │ Two capacitors on │
        │              └───────────────┘
        │                      │
   No   │              ◇ If current ◇
   ←────┤              ◇ 12A<I <14A ◇
        │                      │ Yes
        │              ┌───────────────┐
        │              │ Three capacitors on │
        │              └───────────────┘
        │                      │
                          ┌─────────┐
                          │   END   │
                          └─────────┘
```
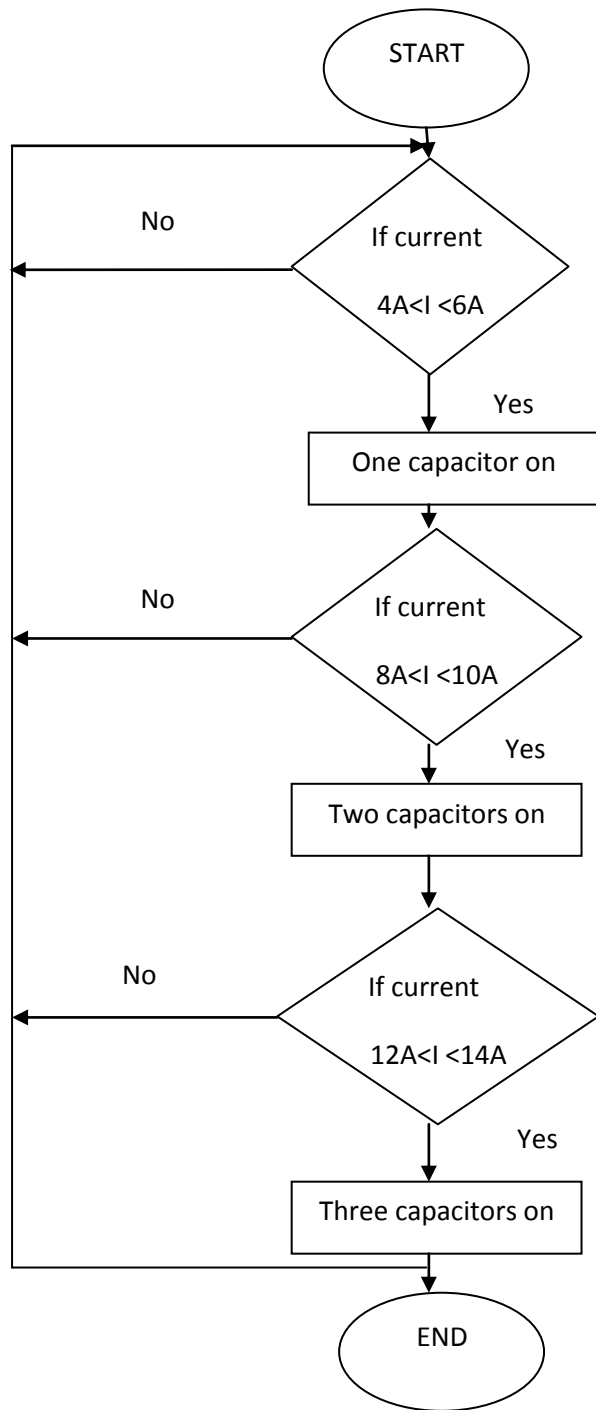
Figure 4.6**:** Flow Chart of the system

4.6   Hardware Operation Process

The operation process begin with the power supply, the power supply is used to given the supply voltage for PIC to working. The step-down transformer is used to step-down the voltage from 240Vac to 12Vac, the bridge rectifier is used to rectifier the ac voltage into full wave rectifier. The voltage regulator is used to regulate the voltage for supply to the PIC to make sure that the voltage supply to PIC is maintaining 5Vdc. The supply 12Vdc is used to supply to the relay. The current sensor is supply 5Vdc, if no current through the output voltage is 2.5V, every 1A current increase the output voltage increase 0.05V. The microcontroller monitors the output voltage increase and it executes the instruction when the condition in the figure 4.6 is satisfied. If the condition $4A < I < 6A$ satisfy the microcontroller (PIC) send the signal to the driver relay circuit. The drivers relay turn on one relay and insert on capacitor in the system. It the same if condition $8A < I < 10A$ and condition $12A < I < 14A$, but the value of the insert capacitor is different 2 capacitors for $8A < I < 10A$ condition and 3 capacitors for $12A < I < 14A$ condition. This process always feed back to make sure the value of the capacitor insert in the system is correct with the running motor and to avoid from the leading power factor.

4.7   Summary

The development of power factor correction is begin with identify the inductive component in the house. Then the power factor correction technique is study to overcame the lagging power factor thus to reduce the using current when the motor running. The current sensor is a suitable input device that used to interface with the PIC because the max output produce by current sensor is 5V. The software microcode studio is used to write the program and convert into hex file. The analog digital converter

(ADC) is used to write the program and to interface between the input signals with the PIC. The flow chat is build and the value of the capacitor is determined and the value of the current running is known. The program is write in the microcode studio is referred to the flow chart in figure 4.6 below.

CHAPTER 5

RESULT AND DISCUSSIONS

After completing the project, the result is so impressive where all expected results are achieved. The system can detect and improve power factor. Also that, the program is successfully developed.

5.1 Result of Power Supply

In this part, a power supply is developing to give supply to the microcontroller and relay. This to make sure the potential decrease the sensitivity will change if the supply is not enough. The LM7805 is a voltage regulator which is for regulate and stabilize the voltage to the circuit.

The power supply get a source from ac supply (240V/50 Hz).then go through transformer to step down the voltage to 12Vrms. switch is to control an AC voltage before is rectifying by bridge rectifier. After that a steady DC voltage is obtained by bridge rectifier the AC voltage.

The voltage regulator LM78L05 is to reduce a DC voltage from filtering sections. The regulation is usually obtained from an IC voltage regulators unit, which takes a DC voltage and provides a somewhat lower DC voltage, which remains the same even if the input DC voltage varies or the output Load connected to the DC voltages changes.

The 15V we connect to relay because we use 12VDC to energize the relay. 5V use as supply to microcontroller PIC 18F4550. The result we can show below.
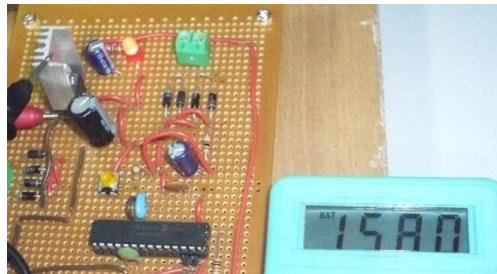
Figure 5.1: Result Input LM7805
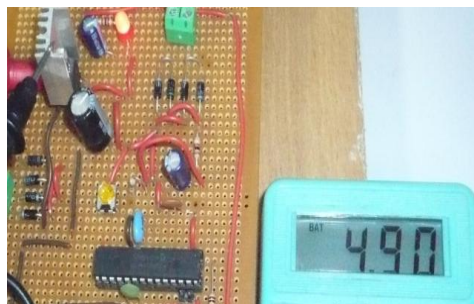
Figure 5.2: Result Output LM7805

5.2   Result Current Sensor

Result from the current sensor circuit we can obtain using multimeter. When the current flow into current sensor and produce the magnetic field. The magnetic fields are analyzed and convert into voltage form. The rating current sensor that used for this project is 50A, which means for every 1A current increase the output voltage increase 0.05V. The current sensor is tested using DC motor, because the current from this motor can varied by using the pressure as a load connected to the shaft. The result of the current sensor is show table below.

Load (psi)	Current (A)	Output Voltage (Vout)
0	1.55	2.50
20	2.05	2.52
40	2.72	2.55
60	3.42	2.59
80	4.30	2.63

Table 5.1: Output Current Sensor

5.3   Result for Power Factor Correction

There have two inductive load is used to test this project. The first one is inductive load (motor) that has a 600W real power. The running current is measure using the clamp mete before the power factor correction circuit is on. The current draw is 3A, blow show the figure for current draw.
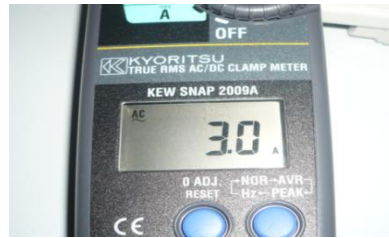
Figure 5.3**:** Current Draw before APFC function (600W)

After the automatic power factor correction function the current form 600W motor is reduce to the 2.7A. That means the power factor for this load is improved, below show the current draw after APFC function.
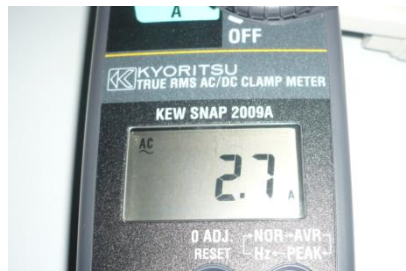
Figure 5.4**:** Current Draw after APFC operated (600W).

The second is inductive load (motor) has a 13200W real power. The running current is measure before the APFC operate using clamp meter. The value of running current measure is 7.1A, below show the current draw before APFC function.
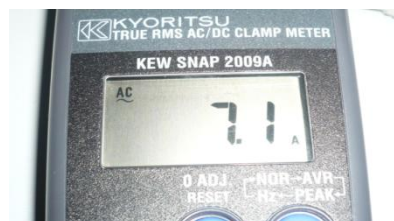
Figure 5.5**:** Current Draw before APFC operate (1.32KW)

After the automatic power factor correction function the current draw from this 1.32KW) load is 6.6A. That means the power factor is improved, below show the current is measure after the APFC operate.

Figure 5.6**:** Current Draw after APFC operated (1.32KW).

5.4 Analysis of the Load Tested

The analysis for this project is to determine the power factor after the capacitor is inserted in the system. The first is the analysis for the 600W motor; the apparent power is calculate by multiplying the load voltage with the load current. Determine the power factor with real power is dividing with the apparent power. The value of the apparent power before the APFC device function is calculate first, below show the calculation before using APFC device.

S=IV

S= (3 × 240)

 = 720 VA

Power factor = Real power

            Apparent power

            = 600
               720

            = 0.833 pf

After the automatic power factor correction operates the apparent power is also calculate to find the new value of the power factor. Below show the new power factor after the APFC device operate.

S=IV

S= (2.7 × 240)

 = 648 VA

Power factor = Real power
　　　　　　　　Apparent power

　　　　　= $\frac{600}{648}$

　　　　　= 0.92 pf

From the calculation we can see that the automatic power factor correction device is operating well and improving the power factor. The second analysis is 1.32KW motor. The same procedure with the 600W motor is made; first determine the apparent power by multiplying the load voltage with the load current. Determine the power factor with dividing the real power with the apparent power. Below show the calculations before APFC device operate.

S=IV

S= (7.1 × 240)

 = 1.704kVA

Power factor = Real power
　　　　　　　　Apparent power

　　　　　= $\frac{1.32kW}{1.704kVA}$

= 0.77 pf

The same procedure is also taken to calculate the power factors after the APFC device operate. The new value of power factor is determining using calculation below.

S=IV

S= (6.6 × 240)

 = 1.584kVA

Power factor = $\frac{\text{Real power}}{\text{Apparent power}}$

$= \frac{1.32\text{kW}}{1.584\text{kVA}}$
= 0.833 pf

From this calculation we can see that the value of the power factor is improved, by the power factor is still low because the value of the capacitor that used is not enough to improve the power factor. Below show the result for tested load.

Table 5.2: Result for Tested Load

Power (W)	Current Before APFC operate	Current After APFC operate	Pf before Correction	Pf after Correction
600	3A	2.7A	0.833pf	0.92pf
13200	7.1A	6.6A	0.77pf	0.83pf

5.5   Discussions

After all the analyses have done, some of the required thing must be discussed. The power factor exists when the inductive load running. The lower power factor causes the more current draw by load. Before the APFC device operates the current is draw more and after the APFC device operates the current became lower. Those show the power factor is improved. For the 1.32KW motor the pf before improve is 0.77 and after improve with insert the capacitor the pf become 0.83. The power factor for this motor is still low because the value of the apparent power that used is not suitable with the value of the capacitor that used. To overcome this problem the bigger value of capacitor is needed, but to determine the value of capacitor some calculation is needed.

5.6   Summary

The power supply is developing to give the power for microcontroller (PIC) to operate, which means the constant 5Vdc is needed to make PIC operate well. The 12Vdc is used to operate the relay. The current sensor is the most important thing because giving the input for the PIC. The current senor automatically converts the signal into voltage form, this important to interface with the microcontroller. There have two types of motor that used to test APFC device, first is 600W motor. The 600W motor draw 3A running current before APFC device operate, after operate the current is reduce to 2.7A. The power factor from 0.83pf is improved to the 0.92pf. The 1.32KW motor draw 7.1A running current before APFC device operate, after operate the current is reduce to 6.6A. The power factor is improve from 0.77pf to the 0.83pf.

CHAPTER 6

CONCLUSION AND SUGGESTIONS

6.1   Conclusion

The objectives of the development of automatic power factor correction device were successfully fulfilled. The operation of automatic power factor correction device is make the current that draw by inductive load (motor) is reduce and effect to the electricity bill and also reduce the life cost. This project utilized the use of microcontroller PIC, current sensor and driver relay circuit has successfully integrated between each other. In other word the synchronization between each circuit which is power supply circuit, sensing circuit, driver relay circuit and LCD make it can operate with each other without any problems. The combination knowledge of analog electronics knowledge, autotoronic knowledge, microcontroller knowledge and individual self skilled method to create the new circuit is important in order to make this project success.

PIC 18F4550 is the brain of the system make the system more reliable for modern technology and the input, output, timer and delay for the system can be adjusted by changing the programming command. This means this PIC can be used almost for all application such as control security system or to develop power electronic device. This also can reduce the power consumption in the house with precise without disturb the stability of the system controlled by microcontroller PIC.

6.2   Suggestion

There are several suggestions to improve the automatic power factor correction device in the future.

I.   For the improvement process the student must study the new automatic power factor correction device in detailed and make sure every flaw of the of this APFC can be fix and thus a new upgrade can be done to make APFC more effectiveness.

II.   To get the more prices value of the power factor, the integrate circuit that can be able to determine the power factor must be used.

III.   The used of Hall Effect current sensor is already proven successfully, so in the future it is recommended using current sensor but different rating. The currently current rating for current sensor is 50A with input 5Vdc. In the future it is better used 30A because every change in current is more precise to detect and giving the output voltage for microcontroller.

IV.   Replace the PIC 18F4550 with the PIC18F2550. It due to the PIC 18F2550 less port compare to PIC 18F4550 which are 40-pins over 28-pins. The PIC 18F2550 is enough to interface between driver relay and current sensor circuit.

V.   The current reduce after the insert capacitor in the system can be display to show that the project is successful.

6.3   Costing and Commercialization

This will describe the overall cost for this project. This part also will explain the commercialization of project.

6.3.1   Costing

Table 6.1 below show the cost of the component and the total cost for build this project.

Table 6.1: The cost of components

Device	Qty	Model	Unit	Manufacture	Unit cost(RM)	Extended cost (RM)
Transformer	1	T1201	-230V,50Hz - Vo : 12 - 0 - 12. Output -Power : 6 VA	TELETRON	10.00	10.00
Bridge Rectifier	1	KBPC6005PBF	-Vrrm:50V -Current Rating: 6A	INTERNATIONAL RECTIFIER	6.60	6.60
Capacitor	1		-470uF		0.15	0.15
Capacitor	2		-10uF		0.15	0.70
Capacitor	1		-1nF		0.15	0.15
Voltage Regulator	1	LM7805	-+5V dc		1.00	1.00
LED	3				0.10	0.30
Resistor	4		$2k\Omega$		0.10	0.40
Resistor	3		470Ω		0.10	0.30
Variable Resistor	1		$20k\Omega$		1.00	1.00
Zener Diode	1		5.1V		0.50	0.50
PCB Header	4				1.00	4.00
LCD	1	2X16 JHD16A			15.00	15.00
PIC	1	18F4550		Microchip	30.00	30.00
Connector	2				1.00	2.00

Zif socket	1				15.00	15.00
Fuse	1		0.3A		0.20	0.20
Wrapping wire	1				15.00	15.00
Capacitor motor	3		10uF		8.00	24.00
					Total	126.30

6.3.2   Commercialization

This project can be commercialize by built the APFC that follow the features that have been recommended in the suggestion section, it is due to the target cost of the recommended the APFC is more efficient. The APFC has the high commercialize because it can reduce the electricity usage and also reduce the electric bills.

REFERENCES

1. Microprocessor based automatic power factor controller, IEE by ***Mr. Y. V. Joshi***
2. Programming of PIC Micro-Controller Power factor Correction, IEEE by *Nader Barsoum.*
3. Electric circuit Book, second edition author *Charles K. Alexander and Mattew N.O Sadiku*
4. Elecreical Devices and Circuit Theoary Book, ninth edition, author *Robert L.Boylested*

APPENDIX A

Transistor 2N3904 Data Sheet

DATA SHEET
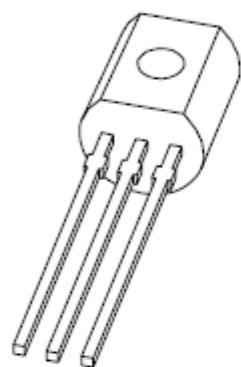
2N3904
NPN switching transistor

NPN switching transistor   2N3904

FEATURES

- Low current (max. 200 mA)
- Low voltage (max. 40 V).

APPLICATIONS

- High-speed switching.

DESCRIPTION

NPN switching transistor in a TO-92; SOT54 plastic package. PNP complement: 2N3906.

PINNING

PIN	DESCRIPTION
1	collector
2	base
3	emitter

Fig.1   Simplified outline (TO-92; SOT54) and symbol.
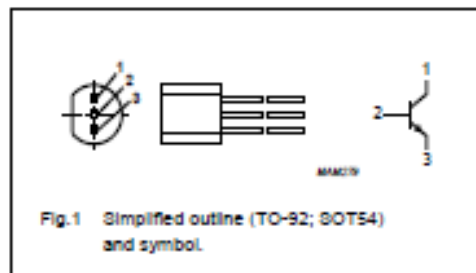
ORDERING INFORMATION

TYPE NUMBER	PACKAGE		VERSION
	NAME	DESCRIPTION	
2N3904	SC-43A	plastic single-ended leaded (through hole) package; 3 leads	SOT54

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	−	60	V
V_{CEO}	collector-emitter voltage	open base	−	40	V
V_{EBO}	emitter-base voltage	open collector	−	6	V
I_C	collector current (DC)		−	200	mA
I_{CM}	peak collector current		−	300	mA
I_{BM}	peak base current		−	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\ °C$; note 1	−	500	mW
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		−	150	°C
T_{amb}	ambient temperature		−65	+150	°C

Note

1.   Transistor mounted on an FR4 printed-circuit board.

NPN switching transistor
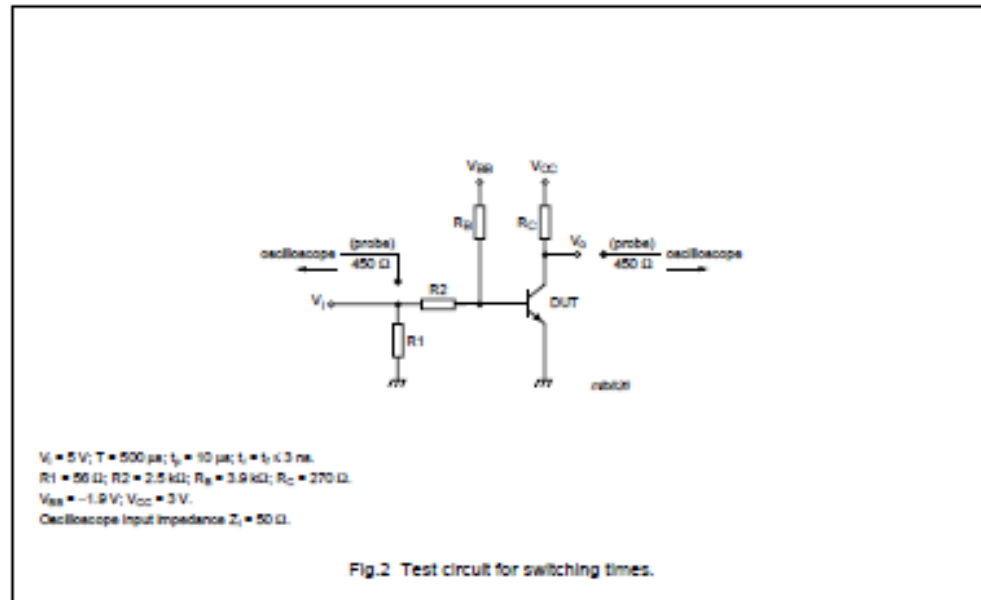
2N3904

V_i = 5 V; T = 500 μs; t_p = 10 μs; t_r = t_f < 3 ns.
R1 = 50 Ω; R2 = 2.5 kΩ; R_B = 3.9 kΩ; R_C = 270 Ω.
V_{BB} = −1.9 V; V_{CC} = 3 V.
Oscilloscope input impedance Z_i = 50 Ω.

Fig.2 Test circuit for switching times.

NPN switching transistor

2N3904

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b₁	c	D	d	E	e	e₁	L	Lₚ (1) max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.30	4.8 4.4	1.7 1.4	4.2 3.8	2.54	1.27	14.5 12.7	3.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			~~97-03-28~~ 04-06-20

NPN switching transistor

2N3904

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	note 1	250	K/W

Note

1. Transistor mounted on an FR4 printed-circuit board.

CHARACTERISTICS

T_{amb} = 25 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	V_{CB} = 30 V; I_E = 0 A	–	50	nA
I_{EBO}	emitter-base cut-off current	V_{EB} = 6 V; I_C = 0 A	–	50	nA
h_{FE}	DC current gain	V_{CE} = 1 V; note 1			
		I_C = 0.1 mA	60	–	
		I_C = 1 mA	80	–	
		I_C = 10 mA	100	300	
		I_C = 50 mA	60	–	
		I_C = 100 mA	30	–	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 1 mA; note 1	–	200	mV
		I_C = 50 mA; I_B = 5 mA; note 1	–	200	mV
V_{BEsat}	base-emitter saturation voltage	I_C = 10 mA; I_B = 1 mA; note 1	–	850	mV
		I_C = 50 mA; I_B = 5 mA; note 1	–	950	mV
C_c	collector capacitance	V_{CB} = 5 V; I_E = I_e = 0 A; f = 1 MHz	–	4	pF
C_e	emitter capacitance	V_{EB} = 500 mV; I_C = I_c = 0 A; f = 1 MHz	–	8	pF
f_T	transition frequency	V_{CE} = 20 V; I_C = 10 mA; f = 100 MHz	300	–	MHz
F	noise figure	V_{CE} = 5 V; I_C = 100 µA; R_s = 1 kΩ; f = 10 Hz to 15.7 kHz	–	5	dB
Switching times (between 10 % and 90 % levels); see Fig.2					
t_{on}	turn-on time	I_{Con} = 10 mA; I_{Bon} = 1 mA; I_{Boff} = –1 mA	–	65	ns
t_d	delay time		–	35	ns
t_r	rise time		–	35	ns
t_{off}	turn-off time		–	240	ns
t_s	storage time		–	200	ns
t_f	fall time		–	50	ns

Note

1. Pulse test: t_p ≤ 300 µs; δ ≤ 0.02.

NPN switching transistor
2N3904

PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads
SOT54

DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b₁	c	D	d	E	e	e₁	L	L₃[1]
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.30	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note
1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			~~97-03-28~~ 04-08-20
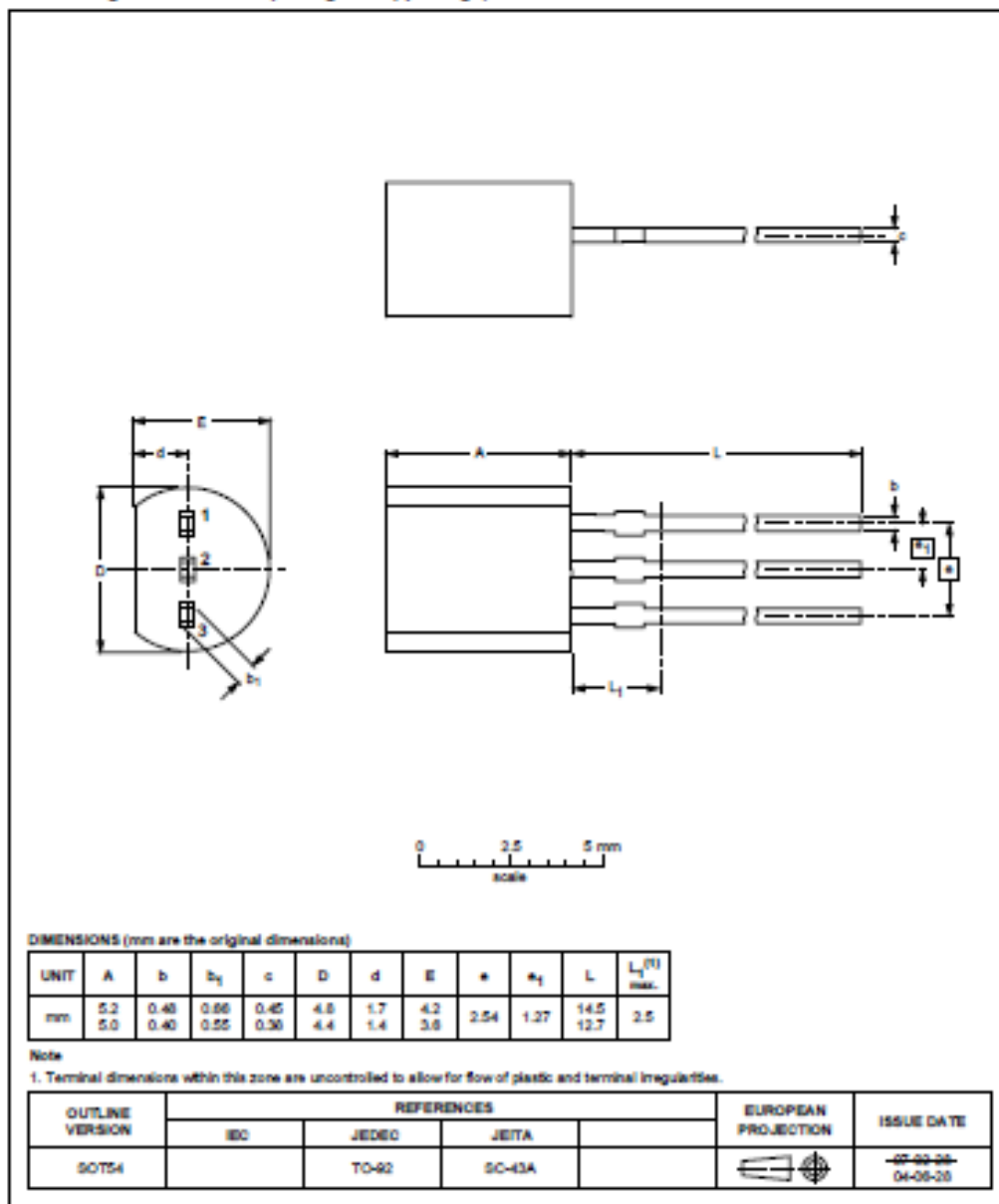
APPENDIX B

PIC18F4550 Microcontroller, Addressing Modes, and Instruction Set

PIC18F4550 MICROCONTROLLER, ADDRESSING MODES AND INSTRUCTION SET

MICROCHIP   PIC18F2455/2550/4455/4550

28/40/44-Pin, High-Performance, Enhanced Flash, USB Microcontrollers with nanoWatt Technology

Universal Serial Bus Features:

- USB V2.0 Compliant
- Low Speed (1.5 Mb/s) and Full Speed (12 Mb/s)
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- Supports up to 32 Endpoints (16 bidirectional)
- 1-Kbyte Dual Access RAM for USB
- On-Chip USB Transceiver with On-Chip Voltage Regulator
- Interface for Off-Chip USB Transceiver
- Streaming Parallel Port (SPP) for USB streaming transfers (40/44-pin devices only)

Power-Managed Modes:

- Run: CPU on, peripherals on
- Idle: CPU off, peripherals on
- Sleep: CPU off, peripherals off
- Idle mode currents down to 5.8 µA typical
- Sleep mode currents down to 0.1 µA typical
- Timer1 Oscillator: 1.1 µA typical, 32 kHz, 2V
- Watchdog Timer: 2.1 µA typical
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Four Crystal modes, including High Precision PLL for USB
- Two External Clock modes, up to 48 MHz
- Internal Oscillator Block:
  - 8 user-selectable frequencies, from 31 kHz to 8 MHz
  - User-tunable to compensate for frequency drift
- Secondary Oscillator using Timer1 @ 32 kHz
- Dual Oscillator options allow microcontroller and USB module to run at different clock speeds
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if any clock stops

Peripheral Highlights:

- High-Current Sink/Source: 25 mA/25 mA
- Three External Interrupts
- Four Timer modules (Timer0 to Timer3)
- Up to 2 Capture/Compare/PWM (CCP) modules:
  - Capture is 16-bit, max. resolution 5.2 ns (TCY/16)
  - Compare is 16-bit, max. resolution 83.3 ns (TCY)
  - PWM output: PWM resolution is 1 to 10-bit
- Enhanced Capture/Compare/PWM (ECCP) module:
  - Multiple output modes
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
- Enhanced USART module:
  - LIN bus support
- Master Synchronous Serial Port (MSSP) module supporting 3-wire SPI (all 4 modes) and I2C™ Master and Slave modes
- 10-bit, up to 13-channel Analog-to-Digital Converter module (A/D) with Programmable Acquisition Time
- Dual Analog Comparators with Input Multiplexing

Special Microcontroller Features:

- C Compiler Optimized Architecture with optional Extended Instruction Set
- 100,000 Erase/Write Cycle Enhanced Flash Program Memory typical
- 1,000,000 Erase/Write Cycle Data EEPROM Memory typical
- Flash/Data EEPROM Retention: > 40 years
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 41 ms to 131s
- Programmable Code Protection
- Single-Supply 5V In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via two pins
- Optional dedicated ICD/ICSP port (44-pin devices only)
- Wide Operating Voltage Range (2.0V to 5.5V)

Device	Program Memory		Data Memory		I/O	10-Bit A/D (ch)	CCP/ECCP (PWM)	SPP	MSSP		EAUSART	Comparators	Timers 8/16-Bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)					SPI	Master I2C™			
PIC18F2455	24K	12288	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F2550	32K	16384	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F4455	24K	12288	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3
PIC18F4550	32K	16384	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3

PIC18F2455/2550/4455/4550

Pin Diagrams

28-Pin PDIP, SOIC
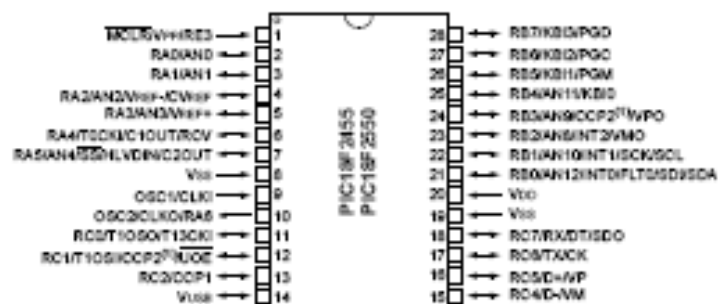
40-Pin PDIP
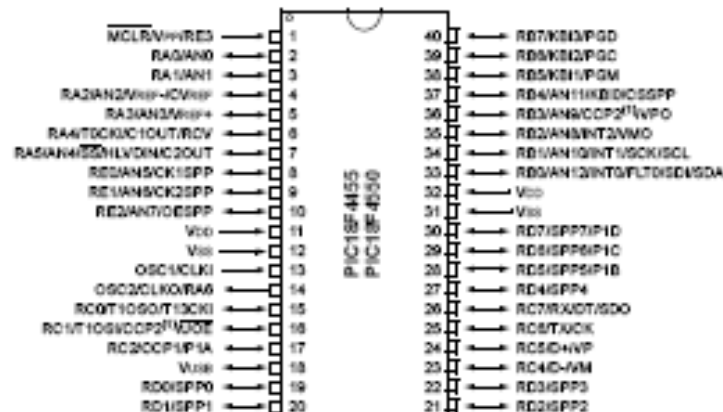
Note 1: RB3 is the alternate pin for CCP2 multiplexing.

PIC18F2455/2550/4455/4550

TABLE 1-1: DEVICE FEATURES

Features	PIC18F2455	PIC18F2550	PIC18F4455	PIC18F4550
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	24576	32768	24576	32768
Program Memory (Instructions)	12288	16384	12288	16384
Data Memory (Bytes)	2048	2048	2048	2048
Data EEPROM Memory (Bytes)	256	256	256	256
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/ Compare/PWM Modules	0	0	1	1
Serial Communications	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART
Universal Serial Bus (USB) Module	1	1	1	1
Streaming Parallel Port (SPP)	No	No	Yes	Yes
10-Bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Comparators	2	2	2	2
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT
Programmable Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled
Packages	28-pin PDIP 28-pin SOIC	28-pin PDIP 28-pin SOIC	40-pin PDIP 44-pin QFN 44-pin TQFP	40-pin PDIP 44-pin QFN 44-pin TQFP

FIGURE 1-2: PIC18F4455/4550 (40/44-PIN) BLOCK DIAGRAM

Note 1: RE3 is multiplexed with MCLR and is only available when the MCLR Resets are disabled.
2: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. Refer to Section 2.0 "Oscillator Configurations" for additional information.
3: These pins are only available on 44-pin TQFP packages under certain conditions. Refer to Section 25.9 "Special ICPORT Features (Designated Packages Only)" for additional information.
4: RB3 is the alternate pin for CCP2 multiplexing.

PIC18F2455/2550/4455/4550

TABLE 1-2: PIC18F2455/2550 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number PDIP, SOIC	Pin Type	Buffer Type	Description
MCLR/Vpp/RE3	1			Master Clear (input) or programming voltage (input).
MCLR		I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
Vpp		P		Programming voltage input.
RE3		I	ST	Digital input.
OSC1/CLKI	9			Oscillator crystal or external clock input.
OSC1		I	Analog	Oscillator crystal input or external clock source input.
CLKI		I	Analog	External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)
OSC2/CLKO/RA6	10			Oscillator crystal or clock output.
OSC2		O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO		O	—	In select modes, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6		I/O	TTL	General purpose I/O pin.

Legend:
TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels I = Input
O = Output P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.
2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

PIC18F2455/2550/4455/4550

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
MCLR/Vpp/RE3	1	18	18			Master Clear (input) or programming voltage (input).
MCLR				I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
Vpp				P		Programming voltage input.
RE3				I	ST	Digital input.
OSC1/CLKI	13	32	30			Oscillator crystal or external clock input.
OSC1				I	Analog	Oscillator crystal input or external clock source input.
CLKI				I	Analog	External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)
OSC2/CLKO/RA6	14	33	31			Oscillator crystal or clock output.
OSC2				O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO				O	—	In RC mode, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6				I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels   I = Input
O = Output   P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.
2: Default assignment for CCP2 when CCP2MX Configuration bit is set.
3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

    Preliminary

PIC18F2455/2550/4455/4550

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTA is a bidirectional I/O port.
RA0/AN0	2	19	19			
RA0				I/O	TTL	Digital I/O.
AN0				I	Analog	Analog Input 0.
RA1/AN1	3	20	20			
RA1				I/O	TTL	Digital I/O.
AN1				I	Analog	Analog Input 1.
RA2/AN2/VREF-/ CVREF	4	21	21			
RA2				I/O	TTL	Digital I/O.
AN2				I	Analog	Analog Input 2.
VREF-				I	Analog	A/D reference voltage (low) input.
CVREF				O	Analog	Analog comparator reference output.
RA3/AN3/VREF+	5	22	22			
RA3				I/O	TTL	Digital I/O.
AN3				I	Analog	Analog Input 3.
VREF+				I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/C1OUT/ RCV	6	23	23			
RA4				I/O	ST	Digital I/O.
T0CKI				I	ST	Timer0 external clock input.
C1OUT				O	—	Comparator 1 output.
RCV				I	TTL	External USB transceiver RCV input.
RA5/AN4/SS/ HLVDIN/C2OUT	7	24	24			
RA5				I/O	TTL	Digital I/O.
AN4				I	Analog	Analog Input 4.
SS				I	TTL	SPI slave select input.
HLVDIN				I	Analog	High/Low-Voltage Detect input.
C2OUT				O	—	Comparator 2 output.
RA6	—	—	—	—	—	See the OSC2/CLKO/RA6 pin.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
         ST = Schmitt Trigger input with CMOS levels   I = Input
         O   = Output   P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.
     2: Default assignment for CCP2 when CCP2MX Configuration bit is set.
     3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

PIC18F2455/2550/4455/4550

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/AN12/INT0/ FLT0/SDI/SDA	33	9	8			
RB0				I/O	TTL	Digital I/O.
AN12				I	Analog	Analog Input 12.
INT0				I	ST	External Interrupt 0.
FLT0				I	ST	Enhanced PWM Fault input (ECCP1 module).
SDI				I	ST	SPI data in.
SDA				I/O	ST	I²C™ data I/O.
RB1/AN10/INT1/SCK/ SCL	34	10	9			
RB1				I/O	TTL	Digital I/O.
AN10				I	Analog	Analog Input 10.
INT1				I	ST	External Interrupt 1.
SCK				I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL				I/O	ST	Synchronous serial clock input/output for I²C mode.
RB2/AN8/INT2/VMO	35	11	10			
RB2				I/O	TTL	Digital I/O.
AN8				I	Analog	Analog Input 8.
INT2				I	ST	External Interrupt 2.
VMO				O	—	External USB transceiver VMO output.
RB3/AN9/CCP2/VPO	36	12	11			
RB3				I/O	TTL	Digital I/O.
AN9				I	Analog	Analog Input 9.
CCP2[1]				I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
VPO				O	—	External USB transceiver VPO output.
RB4/AN11/KBI0/CSSPP	37	14	14			
RB4				I/O	TTL	Digital I/O.
AN11				I	Analog	Analog Input 11.
KBI0				I	TTL	Interrupt-on-change pin.
CSSPP				O	—	SPP chip select control output.
RB5/KBI1/PGM	38	15	15			
RB5				I/O	TTL	Digital I/O.
KBI1				I	TTL	Interrupt-on-change pin.
PGM				I/O	ST	Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC	39	16	16			
RB6				I/O	TTL	Digital I/O.
KBI2				I	TTL	Interrupt-on-change pin.
PGC				I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	40	17	17			
RB7				I/O	TTL	Digital I/O.
KBI3				I	TTL	Interrupt-on-change pin.
PGD				I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
         ST   = Schmitt Trigger input with CMOS levels   I   = Input
         O   = Output   P   = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.
     2: Default assignment for CCP2 when CCP2MX Configuration bit is set.
     3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

PIC18F2455/2550/4455/4550

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
RC0/T1OSO/T13CKI	15	34	32			PORTC is a bidirectional I/O port.
RC0				I/O	ST	Digital I/O.
T1OSO				O	—	Timer1 oscillator output.
T13CKI				I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2/ UOE	16	35	35			
RC1				I/O	ST	Digital I/O.
T1OSI				I	CMOS	Timer1 oscillator input.
CCP2[2]				I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
UOE				O	—	External USB transceiver OE output.
RC2/CCP1/P1A	17	36	36			
RC2				I/O	ST	Digital I/O.
CCP1				I/O	ST	Capture 1 input/Compare 1 output/PWM 1 output.
P1A				O	TTL	Enhanced CCP1 PWM output, channel A.
RC4/D-/VM	23	42	42			
RC4				I	TTL	Digital input.
D-				I/O	—	USB differential minus line (input/output).
VM				I	TTL	External USB transceiver VM input.
RC5/D+/VP	24	43	43			
RC5				I	TTL	Digital input.
D+				I/O	—	USB differential plus line (input/output).
VP				I	TTL	External USB transceiver VP input.
RC6/TX/CK	25	44	44			
RC6				I/O	ST	Digital I/O.
TX				O	—	EUSART asynchronous transmit.
CK				I/O	ST	EUSART synchronous clock (see RX/DT).
RC7/RX/DT/SDO	26	1	1			
RC7				I/O	ST	Digital I/O.
RX				I	ST	EUSART asynchronous receive.
DT				I/O	ST	EUSART synchronous data (see TX/CK).
SDO				O	—	SPI data out.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels   I   = Input
O   = Output   P   = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.
2: Default assignment for CCP2 when CCP2MX Configuration bit is set.
3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

PIC18F2455/2550/4455/4550

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTD is a bidirectional I/O port or a Streaming Parallel Port (SPP). These pins have TTL input buffers when the SPP module is enabled.
RD0/SPP0	19	38	38			
RD0				I/O	ST	Digital I/O.
SPP0				I/O	TTL	Streaming Parallel Port data.
RD1/SPP1	20	39	39			
RD1				I/O	ST	Digital I/O.
SPP1				I/O	TTL	Streaming Parallel Port data.
RD2/SPP2	21	40	40			
RD2				I/O	ST	Digital I/O.
SPP2				I/O	TTL	Streaming Parallel Port data.
RD3/SPP3	22	41	41			
RD3				I/O	ST	Digital I/O.
SPP3				I/O	TTL	Streaming Parallel Port data.
RD4/SPP4	27	2	2			
RD4				I/O	ST	Digital I/O.
SPP4				I/O	TTL	Streaming Parallel Port data.
RD5/SPP5/P1B	28	3	3			
RD5				I/O	ST	Digital I/O.
SPP5				I/O	TTL	Streaming Parallel Port data.
P1B				O	—	Enhanced CCP1 PWM output, channel B.
RD6/SPP6/P1C	29	4	4			
RD6				I/O	ST	Digital I/O.
SPP6				I/O	TTL	Streaming Parallel Port data.
P1C				O	—	Enhanced CCP1 PWM output, channel C.
RD7/SPP7/P1D	30	5	5			
RD7				I/O	ST	Digital I/O.
SPP7				I/O	TTL	Streaming Parallel Port data.
P1D				O	—	Enhanced CCP1 PWM output, channel D.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
         ST = Schmitt Trigger input with CMOS levels   I = Input
         O = Output   P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.
    2: Default assignment for CCP2 when CCP2MX Configuration bit is set.
    3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

TABLE 1-3: **PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)**

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
RE0/AN5/CK1SPP RE0 AN5 CK1SPP	8	25	25	 I/O I O	 ST Analog —	PORTE is a bidirectional I/O port. Digital I/O. Analog input 5. SPP clock 1 output.
RE1/AN6/CK2SPP RE1 AN6 CK2SPP	9	26	26	 I/O I O	 ST Analog —	 Digital I/O. Analog input 6. SPP clock 2 output.
RE2/AN7/OESPP RE2 AN7 OESPP	10	27	27	 I/O I O	 ST Analog —	 Digital I/O. Analog input 7. SPP output enable output.
RE3	—	—	—	—	—	See MCLR/VPP/RE3 pin.
Vss	12, 31	6, 30, 31	6, 29	P	—	Ground reference for logic and I/O pins.
VDD	11, 32	7, 8, 28, 29	7, 28	P	—	Positive supply for logic and I/O pins.
VUSB	18	37	37	O	—	Internal USB 3.3V voltage regulator output.
NC/ICCK/ICPGC[3] ICCK ICPGC	—	—	12	 I/O I/O	 ST ST	No Connect or dedicated ICD/ICSP™ port clock. In-Circuit Debugger clock. ICSP programming clock.
NC/ICDT/ICPGD[3] ICDT ICPGD	—	—	13	 I/O I/O	 ST ST	No Connect or dedicated ICD/ICSP port clock. In-Circuit Debugger data. ICSP programming data.
NC/ICRST/ICVPP[3] ICRST ICVPP	—	—	33	 I P	 — —	No Connect or dedicated ICD/ICSP port Reset. Master Clear (Reset) input. Programming voltage input.
NC/ICPORTS[3] ICPORTS	—	—	34	P	—	No Connect or 28-pin device emulation. Enable 28-pin device emulation when connected to Vss.
NC	—	13	—	—	—	No Connect.

Legend: TTL = TTL compatible input   CMOS = CMOS compatible input or output
        ST = Schmitt Trigger input with CMOS levels   I = Input
        O = Output   P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.
     2: Default assignment for CCP2 when CCP2MX Configuration bit is set.
     3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

PIC18F2455/2550/4455/4550

2.0 OSCILLATOR CONFIGURATIONS

2.1 Overview

Devices in the PIC18F2455/2550/4455/4550 family incorporate a different oscillator and microcontroller clock system than previous PIC18F devices. The addition of the USB module, with its unique requirements for a stable clock source, make it necessary to provide a separate clock source that is compliant with both USB low-speed and full-speed specifications.

To accommodate these requirements, PIC18F2455/2550/4455/4550 devices include a new clock branch to provide a 48 MHz clock for full-speed USB operation. Since it is driven from the primary clock source, an additional system of prescalers and postscalers has been added to accommodate a wide range of oscillator frequencies. An overview of the oscillator structure is shown in Figure 2-1.

Other oscillator features used in PIC18 enhanced microcontrollers, such as the internal oscillator block and clock switching, remain the same. They are discussed later in this chapter.

2.1.1 OSCILLATOR CONTROL

The operation of the oscillator in PIC18F2455/2550/4455/4550 devices is controlled through two Configuration registers and two control registers. Configuration registers, CONFIG1L and CONFIG1H, select the oscillator mode and USB prescaler/postscaler options. As Configuration bits, these are set when the device is programmed and left in that configuration until the device is reprogrammed.

The OSCCON register (Register 2-2) selects the Active Clock mode; it is primarily used in controlling clock switching in power-managed modes. Its use is discussed in Section 2.4.1 "Oscillator Control Register".

The OSCTUNE register (Register 2-1) is used to trim the INTRC frequency source, as well as select the low-frequency clock source that drives several special features. Its use is described in Section 2.2.6.2 "OSCTUNE Register".

2.2 Oscillator Types

PIC18F2455/2550/4455/4550 devices can be operated in twelve distinct oscillator modes. In contrast with previous PIC18 enhanced microcontrollers, four of these modes involve the use of two oscillator types at once. Users can program the FOSC3:FOSC0 Configuration bits to select one of these modes:

1. XT   Crystal/Resonator
2. XTPLL   Crystal/Resonator with PLL enabled
3. HS   High-Speed Crystal/Resonator
4. HSPLL   High-Speed Crystal/Resonator with PLL enabled
5. EC   External Clock with Fosc/4 output
6. ECIO   External Clock with I/O on RA6
7. ECPLL   External Clock with PLL enabled and Fosc/4 output on RA6
8. ECPIO   External Clock with PLL enabled, I/O on RA6
9. INTHS   Internal Oscillator used as microcontroller clock source, HS Oscillator used as USB clock source
10. INTXT   Internal Oscillator used as microcontroller clock source, XT Oscillator used as USB clock source
11. INTIO   Internal Oscillator used as microcontroller clock source, EC Oscillator used as USB clock source, digital I/O on RA6
12. INTCKO Internal Oscillator used as microcontroller clock source, EC Oscillator used as USB clock source, Fosc/4 output on RA6

2.2.1 OSCILLATOR MODES AND USB OPERATION

Because of the unique requirements of the USB module, a different approach to clock operation is necessary. In previous PIC® devices, all core and peripheral clocks were driven by a single oscillator source; the usual sources were primary, secondary or the internal oscillator. With PIC18F2455/2550/4455/4550 devices, the primary oscillator becomes part of the USB module and cannot be associated to any other clock source. Thus, the USB module must be clocked from the primary clock source; however, the microcontroller core and other peripherals can be separately clocked from the secondary or internal oscillators as before.

Because of the timing requirements imposed by USB, an internal clock of either 6 MHz or 48 MHz is required while the USB module is enabled. Fortunately, the microcontroller and other peripherals are not required to run at this clock speed when using the primary oscillator. There are numerous options to achieve the USB module clock requirement and still provide flexibility for clocking the rest of the device from the primary oscillator source. These are detailed in Section 2.3 "Oscillator Settings for USB".

PIC18F2455/2550/4455/4550

FIGURE 2-1: PIC18F2455/2550/4455/4550 CLOCK DIAGRAM

Preliminary © 2007 Microchip Technology Inc.
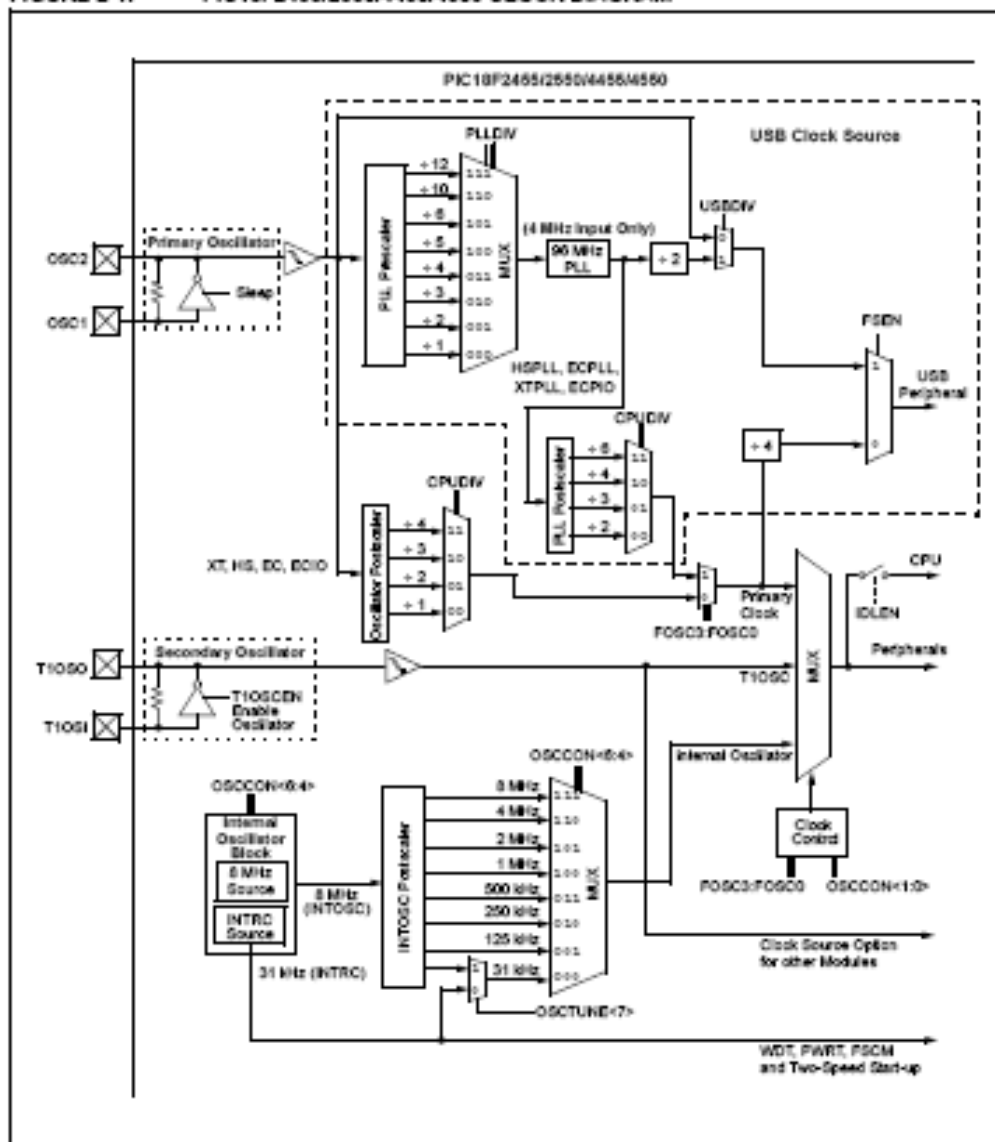
PIC18F2455/2550/4455/4550

2.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In HS, HSPLL, XT and XTPLL Oscillator modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation. Figure 2-2 shows the pin connections.

The oscillator design requires the use of a parallel cut crystal.

Note:	Use of a series cut crystal may give a frequency out of the crystal manufacturer's specifications.

FIGURE 2-2: CRYSTAL/CERAMIC RESONATOR OPERATION (XT, HS OR HSPLL CONFIGURATION)

Note 1: See Table 2-1 and Table 2-2 for initial values of C1 and C2.
2: A series resistor (Rs) may be required for AT strip cut crystals.
3: RF varies with the oscillator mode chosen.
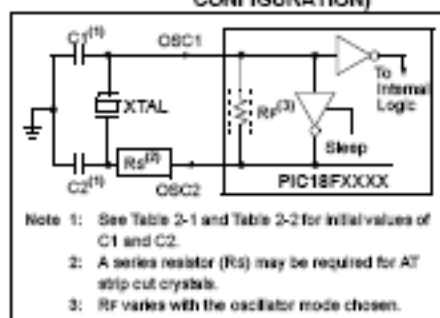
TABLE 2-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

	Typical Capacitor Values Used:		
Mode	Freq	OSC1	OSC2
XT	4.0 MHz	33 pF	33 pF
HS	8.0 MHz	27 pF	27 pF
	16.0 MHz	22 pF	22 pF

Capacitor values are for design guidance only.

These capacitors were tested with the resonators listed below for basic start-up and operation. These values are not optimized.

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.

See the notes following Table 2-2 for additional information.

Resonators Used:
4.0 MHz
8.0 MHz
16.0 MHz

TABLE 2-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Crystal Freq	Typical Capacitor Values Tested:	
		C1	C2
XT	4 MHz	27 pF	27 pF
HS	4 MHz	27 pF	27 pF
	8 MHz	22 pF	22 pF
	20 MHz	15 pF	15 pF

Capacitor values are for design guidance only.

These capacitors were tested with the crystals listed below for basic start-up and operation. These values are not optimized.

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.

See the notes following this table for additional information.

Crystals Used:
4 MHz
8 MHz
20 MHz

Note 1: Higher capacitance increases the stability of oscillator but also increases the start-up time.

2: When operating below 3V VDD, or when using certain ceramic resonators at any voltage, it may be necessary to use the HS mode or switch to a crystal oscillator.

3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.

4: Rs may be required to avoid overdriving crystals with low drive level specification.

5: Always verify oscillator performance over the VDD and temperature range that is expected for the application.

An internal postscaler allows users to select a clock frequency other than that of the crystal or resonator. Frequency division is determined by the CPUDIV Configuration bits. Users may select a clock frequency of the oscillator frequency, or 1/2, 1/3 or 1/4 of the frequency.

An external clock may also be used when the microcontroller is in HS Oscillator mode. In this case, the OSC2/CLKO pin is left open (Figure 2-3).

PIC18F2455/2550/4455/4550

FIGURE 2-3: EXTERNAL CLOCK INPUT OPERATION (HS OSC CONFIGURATION)

2.2.3 EXTERNAL CLOCK INPUT

The EC, ECIO, ECPLL and ECPIO Oscillator modes require an external clock source to be connected to the OSC1 pin. There is no oscillator start-up time required after a Power-on Reset or after an exit from Sleep mode.

In the EC and ECPLL Oscillator modes, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic. Figure 2-4 shows the pin connections for the EC Oscillator mode.

FIGURE 2-4: EXTERNAL CLOCK INPUT OPERATION (EC AND ECPLL CONFIGURATION)

The ECIO and ECPIO Oscillator modes function like the EC and ECPLL modes, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6). Figure 2-5 shows the pin connections for the ECIO Oscillator mode.

FIGURE 2-5: EXTERNAL CLOCK INPUT OPERATION (ECIO AND ECPIO CONFIGURATION)

The internal postscaler for reducing clock frequency in XT and HS modes is also available in EC and ECIO modes.

2.2.4 PLL FREQUENCY MULTIPLIER

PIC18F2455/2550/4255/4550 devices include a Phase Locked Loop (PLL) circuit. This is provided specifically for USB applications with lower speed oscillators and can also be used as a microcontroller clock source.

The PLL is enabled in HSPLL, XTPLL, ECPLL and ECPIO Oscillator modes. It is designed to produce a fixed 96 MHz reference clock from a fixed 4 MHz input. The output can then be divided and used for both the USB and the microcontroller core clock. Because the PLL has a fixed frequency input and output, there are eight prescaling options to match the oscillator input frequency to the PLL.

There is also a separate postscaler option for deriving the microcontroller clock from the PLL. This allows the USB peripheral and microcontroller to use the same oscillator input and still operate at different clock speeds. In contrast to the postscaler for XT, HS and EC modes, the available options are 1/2, 1/3, 1/4 and 1/6 of the PLL output.

The HSPLL, ECPLL and ECPIO modes make use of the HS mode oscillator for frequencies up to 48 MHz. The prescaler divides the oscillator input by up to 12 to produce the 4 MHz drive for the PLL. The XTPLL mode can only use an input frequency of 4 MHz which drives the PLL directly.

FIGURE 2-6: PLL BLOCK DIAGRAM (HS MODE)
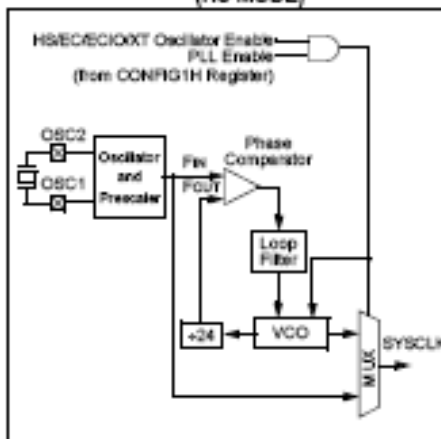
PIC18F2455/2550/4455/4550

4.0 RESET

The PIC18F2455/2550/4455/4550 devices differentiate between various kinds of Reset:

a) Power-on Reset (POR)
b) MCLR Reset during normal operation
c) MCLR Reset during power-managed modes
d) Watchdog Timer (WDT) Reset (during execution)
e) Programmable Brown-out Reset (BOR)
f) RESET Instruction
g) Stack Full Reset
h) Stack Underflow Reset

This section discusses Resets generated by MCLR, POR and BOR and covers the operation of the various start-up timers. Stack Reset events are covered in Section 6.1.2.4 "Stack Full and Underflow Resets". WDT Resets are covered in Section 25.2 "Watchdog Timer (WDT)".

A simplified block diagram of the on-chip Reset circuit is shown in Figure 4-1.

4.1 RCON Register

Device Reset events are tracked through the RCON register (Register 4-1). The lower five bits of the register indicate that a specific Reset event has occurred. In most cases, these bits can only be cleared by the event and must be set by the application after the event. The state of these flag bits, taken together, can be read to indicate the type of Reset that just occurred. This is described in more detail in Section 4.6 "Reset State of Registers".

The RCON register also has control bits for setting interrupt priority (IPEN) and software control of the BOR (SBOREN). Interrupt priority is discussed in Section 9.0 "Interrupts". BOR is covered in Section 4.4 "Brown-out Reset (BOR)".

FIGURE 4-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

Note 1: This is the INTRC source from the internal oscillator block and is separate from the RC oscillator of the CLKI pin.
2: See Table 4-2 for time-out situations.
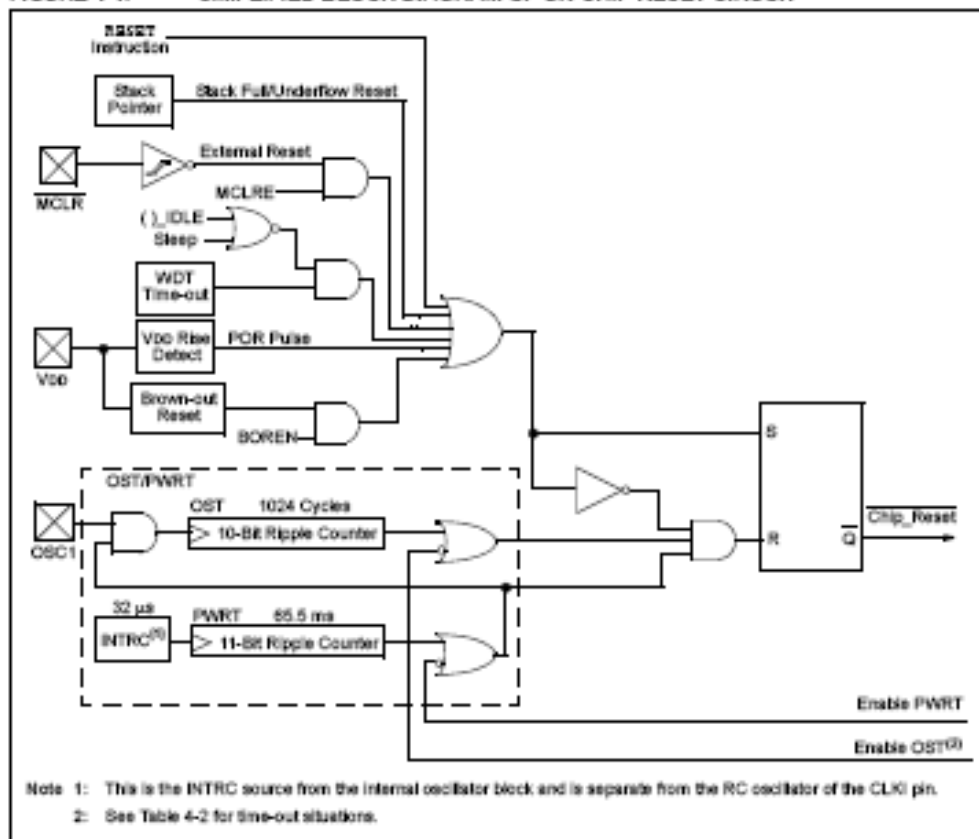
4.2 Master Clear Reset ($\overline{\text{MCLR}}$)

The $\overline{\text{MCLR}}$ pin provides a method for triggering an external Reset of the device. A Reset is generated by holding the pin low. These devices have a noise filter in the $\overline{\text{MCLR}}$ Reset path which detects and ignores small pulses.

The $\overline{\text{MCLR}}$ pin is not driven low by any internal Resets, including the WDT.

In PIC18F2455/2550/4455/4550 devices, the $\overline{\text{MCLR}}$ input can be disabled with the MCLRE Configuration bit. When $\overline{\text{MCLR}}$ is disabled, the pin becomes a digital input. See **Section 10.5 "PORTE, TRISE and LATE Registers"** for more information.

4.3 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip whenever VDD rises above a certain threshold. This allows the device to start in the initialized state when VDD is adequate for operation.

To take advantage of the POR circuitry, tie the $\overline{\text{MCLR}}$ pin through a resistor (1 kΩ to 10 kΩ) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset delay. A minimum rise rate for VDD is specified (parameter D004, **Section 28.1 "DC Characteristics"**). For a slow rise time, see Figure 4-2.

When the device starts normal operation (i.e., exits the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

POR events are captured by the $\overline{\text{POR}}$ bit (RCON<1>). The state of the bit is set to '0' whenever a POR occurs; it does not change for any other Reset event. $\overline{\text{POR}}$ is not reset to '1' by any hardware event. To capture multiple events, the user manually resets the bit to '1' in software following any POR.

FIGURE 4-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)

Note 1: External Power-on Reset circuit is required only if the VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

2: R < 40 kΩ is recommended to make sure that the voltage drop across R does not violate the device's electrical specification.

3: R1 ≥ 1 kΩ will limit any current flowing into $\overline{\text{MCLR}}$ from external capacitor C, in the event of MCLR/VPP pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

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5.0   MEMORY ORGANIZATION

There are three types of memory in PIC18 enhanced microcontroller devices:

* Program Memory
* Data RAM
* Data EEPROM

As Harvard architecture devices, the data and program memories use separate busses; this allows for concurrent access of the two memory spaces. The data EEPROM, for practical purposes, can be regarded as a peripheral device, since it is addressed and accessed through a set of control registers.

Additional detailed information on the operation of the Flash program memory is provided in **Section 6.0 "Flash Program Memory"**. Data EEPROM is discussed separately in **Section 7.0 "Data EEPROM Memory"**.

5.1   Program Memory Organization

PIC18 microcontrollers implement a 21-bit program counter which is capable of addressing a 2-Mbyte program memory space. Accessing a location between the upper boundary of the physically implemented memory and the 2-Mbyte address will return all '0's (a NOP instruction).

The PIC18F2455 and PIC18F4455 each have 24 Kbytes of Flash memory and can store up to 12,288 single-word instructions. The PIC18F2550 and PIC18F4550 each have 32 Kbytes of Flash memory and can store up to 16,384 single-word instructions.

PIC18 devices have two interrupt vectors. The Reset vector address is at 0000h and the interrupt vector addresses are at 0008h and 0018h.

The program memory maps for PIC18FX455 and PIC18FX550 devices are shown in Figure 5-1.

FIGURE 5-1:   PROGRAM MEMORY MAP AND STACK FOR PIC18F2455/2550/4455/4550 DEVICES
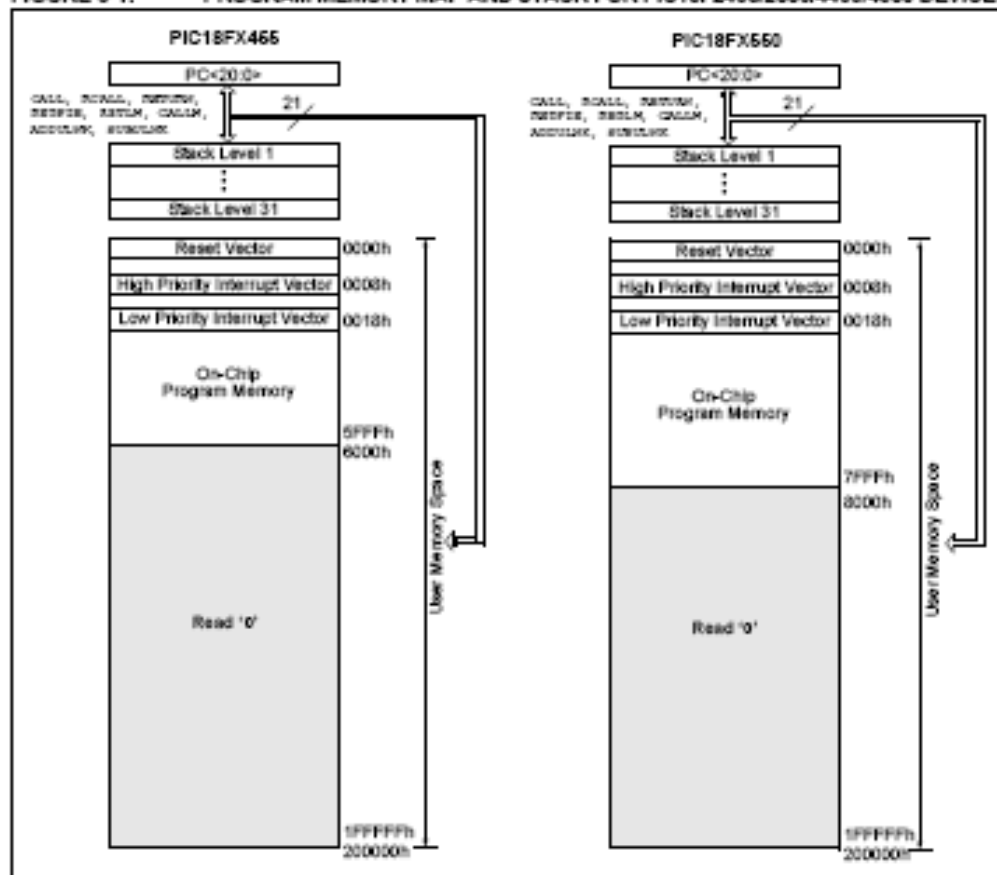
PIC18F2455/2550/4455/4550

5.1.1 PROGRAM COUNTER

The Program Counter (PC) specifies the address of the instruction to fetch for execution. The PC is 21 bits wide and is contained in three separate 8-bit registers. The low byte, known as the PCL register, is both readable and writable. The high byte, or PCH register, contains the PC<15:8> bits; it is not directly readable or writable. Updates to the PCH register are performed through the PCLATH register. The upper byte is called PCU. This register contains the PC<20:16> bits; it is also not directly readable or writable. Updates to the PCU register are performed through the PCLATU register.

The contents of PCLATH and PCLATU are transferred to the program counter by any operation that writes PCL. Similarly, the upper two bytes of the program counter are transferred to PCLATH and PCLATU by an operation that reads PCL. This is useful for computed offsets to the PC (see Section 5.1.4.1 "Computed GOTO").

The PC addresses bytes in the program memory. To prevent the PC from becoming misaligned with word instructions, the Least Significant bit of PCL is fixed to a value of '0'. The PC increments by 2 to address sequential instructions in the program memory.

The CALL, RCALL and GOTO program branch instructions write to the program counter directly. For these instructions, the contents of PCLATH and PCLATU are not transferred to the program counter.

5.1.2 RETURN ADDRESS STACK

The return address stack allows any combination of up to 31 program calls and interrupts to occur. The PC is pushed onto the stack when a CALL or RCALL instruction is executed or an interrupt is Acknowledged. The PC value is pulled off the stack on a RETURN, RETLW or a RETFIE instruction. PCLATU and PCLATH are not affected by any of the RETURN or CALL instructions.

The stack operates as a 31-word by 21-bit RAM and a 5-bit Stack Pointer, STKPTR. The stack space is not part of either program or data space. The Stack Pointer is readable and writable and the address on the top of the stack is readable and writable through the Top-of-Stack Special Function Registers. Data can also be pushed to, or popped from the stack, using these registers.

A CALL type instruction causes a push onto the stack. The Stack Pointer is first incremented and the location pointed to by the Stack Pointer is written with the contents of the PC (already pointing to the instruction following the CALL). A RETURN type instruction causes a pop from the stack. The contents of the location pointed to by the STKPTR are transferred to the PC and then the Stack Pointer is decremented.

The Stack Pointer is initialized to '00000' after all Resets. There is no RAM associated with the location corresponding to a Stack Pointer value of '00000'; this is only a Reset value. Status bits indicate if the stack is full, has overflowed or has underflowed.

5.1.2.1 Top-of-Stack Access

Only the top of the return address stack (TOS) is readable and writable. A set of three registers, TOSU:TOSH:TOSL, hold the contents of the stack location pointed to by the STKPTR register (Figure 5-2). This allows users to implement a software stack if necessary. After a CALL, RCALL or interrupt, the software can read the pushed value by reading the TOSU:TOSH:TOSL registers. These values can be placed on a user-defined software stack. At return time, the software can return these values to TOSU:TOSH:TOSL and do a return.

The user must disable the global interrupt enable bits while accessing the stack to prevent inadvertent stack corruption.

FIGURE 5-2:   RETURN ADDRESS STACK AND ASSOCIATED REGISTERS
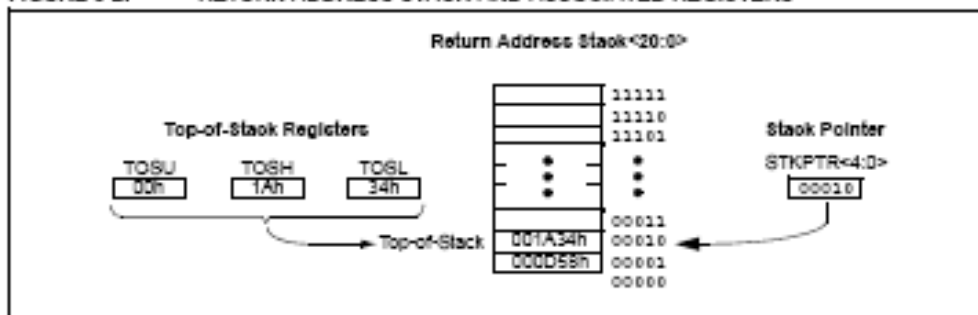
5.2 PIC18 Instruction Cycle

5.2.1 CLOCKING SCHEME

The microcontroller clock input, whether from an internal or external source, is internally divided by four to generate four non-overlapping quadrature clocks (Q1, Q2, Q3 and Q4). Internally, the program counter is incremented on every Q1; the instruction is fetched from the program memory and latched into the Instruction Register (IR) during Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 5-3.

5.2.2 INSTRUCTION FLOW/PIPELINING

An "Instruction Cycle" consists of four Q cycles: Q1 through Q4. The instruction fetch and execute are pipelined in such a manner that a fetch takes one instruction cycle, while the decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 5-3).
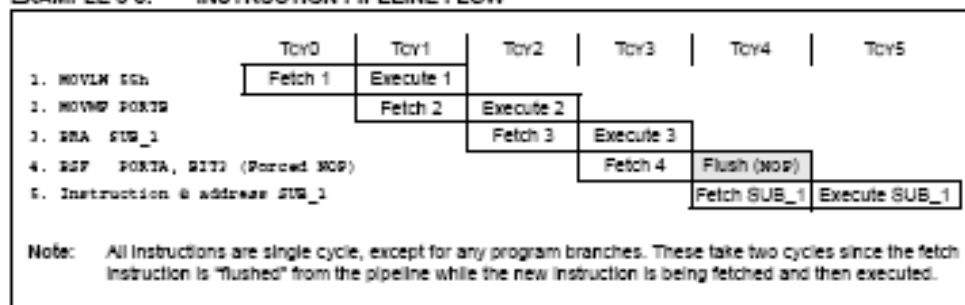
A fetch cycle begins with the Program Counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 5-3:   CLOCK/INSTRUCTION CYCLE
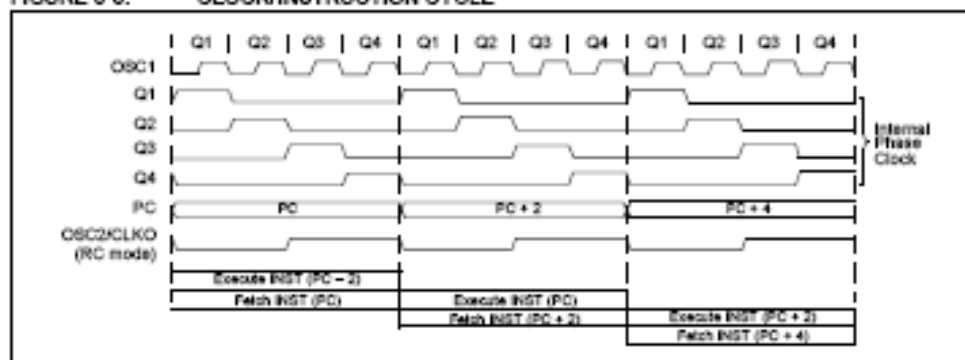
EXAMPLE 5-3:   INSTRUCTION PIPELINE FLOW

Note: All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.
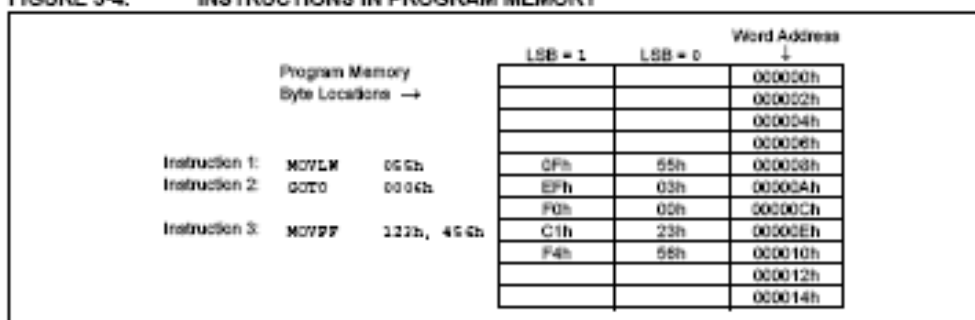
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5.2.3 INSTRUCTIONS IN PROGRAM MEMORY

The program memory is addressed in bytes. Instructions are stored as two bytes or four bytes in program memory. The Least Significant Byte of an instruction word is always stored in a program memory location with an even address (LSb = 0). To maintain alignment with instruction boundaries, the PC increments in steps of 2 and the LSb will always read '0' (see Section 6.1.1 "Program Counter").

Figure 5-4 shows an example of how instruction words are stored in the program memory.

The CALL and GOTO instructions have the absolute program memory address embedded into the instruction. Since instructions are always stored on word boundaries, the data contained in the instruction is a word address. The word address is written to PC<20:1>, which accesses the desired byte address in program memory. Instruction #2 in Figure 5-4 shows how the instruction, GOTO 0006h, is encoded in the program memory. Program branch instructions, which encode a relative address offset, operate in the same manner. The offset value stored in a branch instruction represents the number of single-word instructions that the PC will be offset by. Section 26.0 "Instruction Set Summary" provides further details of the instruction set.

FIGURE 5-4: INSTRUCTIONS IN PROGRAM MEMORY

			LSB = 1	LSB = 0	Word Address ↓
	Program Memory Byte Locations →				000000h
					000002h
					000004h
					000006h
Instruction 1:	MOVLW	055h	0Fh	55h	000008h
Instruction 2:	GOTO	0006h	EFh	03h	00000Ah
			F0h	00h	00000Ch
Instruction 3:	MOVFF	123h, 456h	C1h	23h	00000Eh
			F4h	56h	000010h
					000012h
					000014h

5.2.4 TWO-WORD INSTRUCTIONS

The standard PIC18 instruction set has four two-word instructions: CALL, MOVFF, GOTO and LFSR. In all cases, the second word of the instructions always has '1111' as its four Most Significant bits; the other 12 bits are literal data, usually a data memory address.

The use of '1111' in the 4 MSbs of an instruction specifies a special form of NOP. If the instruction is executed in proper sequence, immediately after the first word, the data in the second word is accessed and used by the instruction sequence. If the first word is skipped for some reason and the second word is executed by itself, a NOP is executed instead. This is necessary for cases when the two-word instruction is preceded by a conditional instruction that changes the PC. Example 5-4 shows how this works.
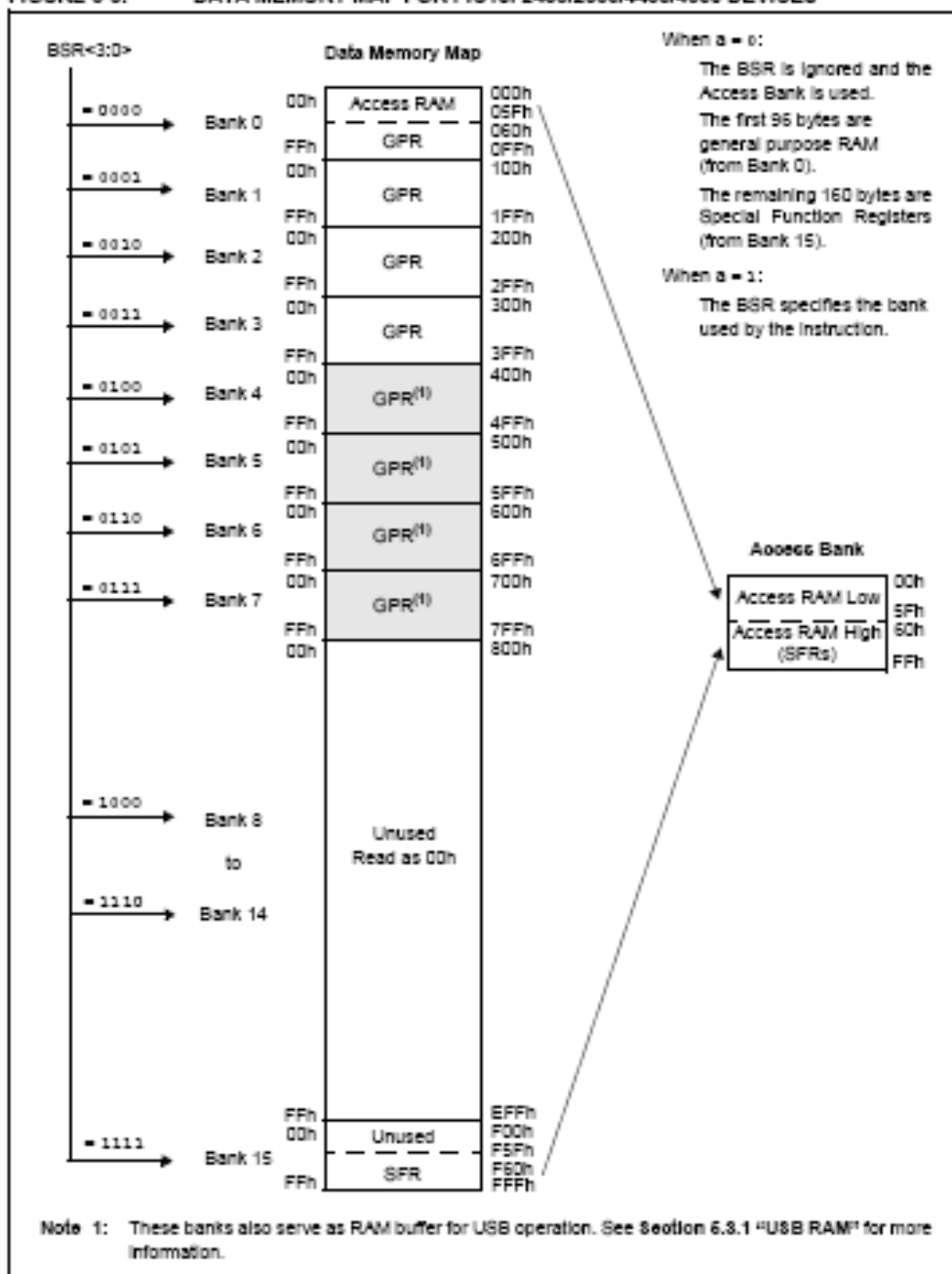
> Note: See Section 6.5 "Program Memory and the Extended Instruction Set" for information on two-word instruction in the extended instruction set.

EXAMPLE 5-4: TWO-WORD INSTRUCTIONS

CASE 1:			
Object Code	**Source Code**		
0110 0110 0000 0000	TSTFSZ	REG1	; is RAM location 0?
1100 0001 0010 0011	MOVFF	REG1, REG2	; No, skip this word
1111 0100 0101 0110			; Execute this word as a NOP
0010 0100 0000 0000	ADDWF	REG1	; continue code
CASE 2:			
Object Code	**Source Code**		
0110 0110 0000 0000	TSTFSZ	REG1	; is RAM location 0?
1100 0001 0010 0011	MOVFF	REG1, REG2	; Yes, execute this word
1111 0100 0101 0110			; 2nd word of instruction
0010 0100 0000 0000	ADDWF	REG1	; continue code

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FIGURE 5-5:   DATA MEMORY MAP FOR PIC18F2455/2550/4455/4550 DEVICES

When a = 0:

The BSR is ignored and the Access Bank is used.

The first 96 bytes are general purpose RAM (from Bank 0).

The remaining 160 bytes are Special Function Registers (from Bank 15).

When a = 1:

The BSR specifies the bank used by the instruction.

Note 1:   These banks also serve as RAM buffer for USB operation. See Section 6.3.1 "USB RAM" for more information.

FIGURE 5-6:   USE OF THE BANK SELECT REGISTER (DIRECT ADDRESSING)

Note   1:   The Access RAM bit of the instruction can be used to force an override of the selected bank (BSR<3:0>) to
              the registers of the Access Bank.

        2:   The MOVFF instruction embeds the entire 12-bit address in the instruction.
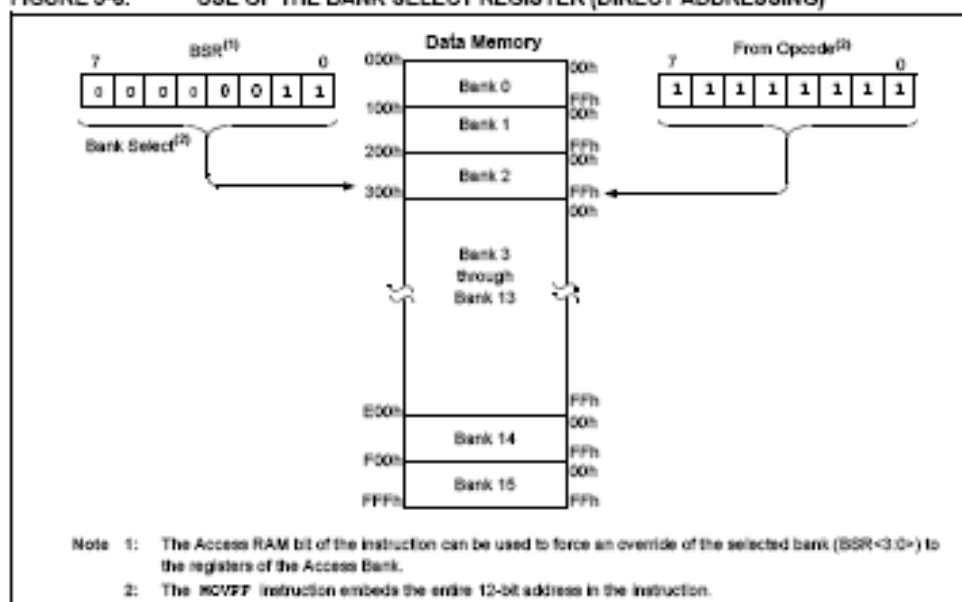
5.3.3   ACCESS BANK

While the use of the BSR, with an embedded 8-bit address, allows users to address the entire range of data memory, it also means that the user must always ensure that the correct bank is selected. Otherwise, data may be read from or written to the wrong location. This can be disastrous if a GPR is the intended target of an operation but an SFR is written to instead. Verifying and/or changing the BSR for each read or write to data memory can become very inefficient.

To streamline access for the most commonly used data memory locations, the data memory is configured with an Access Bank, which allows users to access a mapped block of memory without specifying a BSR. The Access Bank consists of the first 96 bytes of memory (00h-5Fh) in Bank 0 and the last 160 bytes of memory (60h-FFh) in Block 15. The lower half is known as the "Access RAM" and is composed of GPRs. The upper half is where the device's SFRs are mapped. These two areas are mapped contiguously in the Access Bank and can be addressed in a linear fashion by an 8-bit address (Figure 5-5).

The Access Bank is used by core PIC18 instructions that include the Access RAM bit (the 'a' parameter in the instruction). When 'a' is equal to '1', the instruction uses the BSR and the 8-bit address included in the opcode for the data memory address. When 'a' is '0',

however, the instruction is forced to use the Access Bank address map; the current value of the BSR is ignored entirely.

Using this "forced" addressing allows the instruction to operate on a data address in a single cycle without updating the BSR first. For 8-bit addresses of 60h and above, this means that users can evaluate and operate on SFRs more efficiently. The Access RAM below 60h is a good place for data values that the user might need to access rapidly, such as immediate computational results or common program variables. Access RAM also allows for faster and more code efficient context saving and switching of variables.

The mapping of the Access Bank is slightly different when the extended instruction set is enabled (XINST Configuration bit = 1). This is discussed in more detail in Section 5.6.3 "Mapping the Access Bank in Indexed Literal Offset Mode".

5.3.4   GENERAL PURPOSE REGISTER FILE

PIC18 devices may have banked memory in the GPR area. This is data RAM which is available for use by all instructions. GPRs start at the bottom of Bank 0 (address 000h) and grow upwards towards the bottom of the SFR area. GPRs are not initialized by a Power-on Reset and are unchanged on all other Resets.

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10.0   I/O PORTS

Depending on the device selected and features enabled, there are up to five ports available. Some pins of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Each port has three registers for its operation. These registers are:

* TRIS register (data direction register)
* PORT register (reads the levels on the pins of the device)
* LAT register (output latch)

The Data Latch register (LATA) is useful for read-modify-write operations on the value driven by the I/O pins.

A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 10-1.

FIGURE 10-1:   GENERIC I/O PORT OPERATION

Note 1:   I/O pins have diode protection to Vdd and Vss.
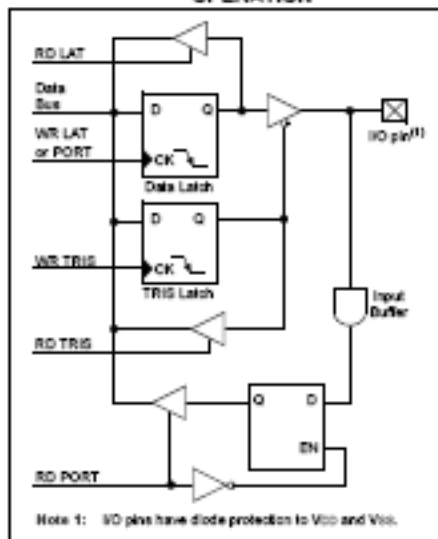
10.1   PORTA, TRISA and LATA Registers

PORTA is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins; writing to it will write to the port latch.

The Data Latch register (LATA) is also memory mapped. Read-modify-write operations on the LATA register read and write the latched output value for PORTA.

The RA4 pin is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA6 pin is multiplexed with the main oscillator pin; it is enabled as an oscillator or I/O pin by the selection of the main oscillator in Configuration Register 1H (see Section 25.1 "Configuration Bits" for details). When not used as a port pin, RA6 and its associated TRIS and LAT bits are read as '0'.

RA4 is also multiplexed with the USB module; it serves as a receiver input from an external USB transceiver. For details on configuration of the USB module, see Section 17.2 "USB Status and Control".

Several PORTA pins are multiplexed with analog inputs, the analog Vref+ and Vref- inputs and the comparator voltage reference output. The operation of pins RA5 and RA3:RA0 as A/D converter inputs is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register 1).

> Note: On a Power-on Reset, RA5 and RA3:RA0 are configured as analog inputs and read as '0'. RA4 is configured as a digital input.

All other PORTA pins have TTL input levels and full CMOS output drivers.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE 10-1:   INITIALIZING PORTA

```
CLRF    PORTA    ; Initialize PORTA by
                 ; clearing output
                 ; data latches
CLRF    LATA     ; Alternate method
                 ; to clear output
                 ; data latches
MOVLW   0Fh      ; Configure A/D
MOVWF   ADCON1   ; for digital inputs
MOVLW   07h      ; Configure comparators
MOVWF   CMCON    ; for digital input
MOVLW   0CFh     ; Value used to
                 ; initialize data
                 ; direction
MOVWF   TRISA    ; Set RA<3:0> as inputs
                 ; RA<5:4> as outputs
```

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TABLE 10-1: PORTA I/O SUMMARY

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RA0/AN0	RA0	0	OUT	DIG	LATA<0> data output; not affected by analog input.
		1	IN	TTL	PORTA<0> data input; disabled when analog input enabled.
	AN0	1	IN	ANA	A/D input channel 0 and Comparator C1- input. Default configuration on POR; does not affect digital output.
RA1/AN1	RA1	0	OUT	DIG	LATA<1> data output; not affected by analog input.
		1	IN	TTL	PORTA<1> data input; reads '0' on POR.
	AN1	1	IN	ANA	A/D input channel 1 and Comparator C2- input. Default configuration on POR; does not affect digital output.
RA2/AN2/ VREF-/CVREF	RA2	0	OUT	DIG	LATA<2> data output; not affected by analog input. Disabled when CVREF output enabled.
		1	IN	TTL	PORTA<2> data input. Disabled when analog functions enabled; disabled when CVREF output enabled.
	AN2	1	IN	ANA	A/D input channel 2 and Comparator C2+ input. Default configuration on POR; not affected by analog output.
	VREF-	1	IN	ANA	A/D and comparator voltage reference low input.
	CVREF	x	OUT	ANA	Comparator voltage reference output. Enabling this feature disables digital I/O.
RA3/AN3/ VREF+	RA3	0	OUT	DIG	LATA<3> data output; not affected by analog input.
		1	IN	TTL	PORTA<3> data input; disabled when analog input enabled.
	AN3	1	IN	ANA	A/D input channel 3 and Comparator C1+ input. Default configuration on POR.
	VREF+	1	IN	ANA	A/D and comparator voltage reference high input.
RA4/T0CKI/ C1OUT/RCV	RA4	0	OUT	DIG	LATA<4> data output; not affected by analog input.
		1	IN	ST	PORTA<4> data input; disabled when analog input enabled.
	T0CKI	1	IN	ST	Timer0 clock input.
	C1OUT	0	OUT	DIG	Comparator 1 output; takes priority over port data.
	RCV	x	IN	TTL	External USB transceiver RCV input.
RA5/AN4/SS/ HLVDIN/C2OUT	RA5	0	OUT	DIG	LATA<5> data output; not affected by analog input.
		1	IN	TTL	PORTA<5> data input; disabled when analog input enabled.
	AN4	1	IN	ANA	A/D input channel 4. Default configuration on POR.
	SS	1	IN	TTL	Slave select input for SSP (MSSP module).
	HLVDIN	1	IN	ANA	High/Low-Voltage Detect external trip point input.
	C2OUT	0	OUT	DIG	Comparator 2 output; takes priority over port data.
OSC2/CLKO/ RA6	OSC2	x	OUT	ANA	Main oscillator feedback output connection (all XT and HS modes).
	CLKO	x	OUT	DIG	System cycle clock output (Fosc/4); available in EC, ECPLL and INTCKO modes.
	RA6	0	OUT	DIG	LATA<6> data output. Available only in ECIO, ECPIO and INTIO modes; otherwise, reads as '0'.
		1	IN	TTL	PORTA<6> data input. Available only in ECIO, ECPIO and INTIO modes; otherwise, reads as '0'.

Legend: OUT = Output, IN = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option)

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10.2 PORTB, TRISB and LATB Registers

PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

The Data Latch register (LATB) is also memory mapped. Read-modify-write operations on the LATB register read and write the latched output value for PORTB.

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit, RBPU (INTCON2<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

> **Note:** On a Power-on Reset, RB4:RB0 are configured as analog inputs by default and read as '0'; RB7:RB5 are configured as digital inputs.
>
> By programming the Configuration bit, PBADEN (CONFIG3H<1>), RB4:RB0 will alternatively be configured as digital inputs on POR.

Four of the PORTB pins (RB7:RB4) have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur. Any RB7:RB4 pin configured as an output is excluded from the interrupt-on-change comparison. The pins are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are ORed together to generate the RB Port Change Interrupt with Flag bit, RBIF (INTCON<0>).

The interrupt-on-change can be used to wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB (except with the MOVFF (ANY), PORTB instruction). This will end the mismatch condition.

b) Clear flag bit, RBIF.

A mismatch condition will continue to set flag bit, RBIF. Reading PORTB will end the mismatch condition and allow flag bit, RBIF, to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

Pins, RB2 and RB3, are multiplexed with the USB peripheral and serve as the differential signal outputs for an external USB transceiver (TRIS configuration). Refer to Section 17.2.2.2 "External Transceiver" for additional information on configuring the USB module for operation with an external transceiver.

RB4 is multiplexed with CSSPP, the chip select function for the Streaming Parallel Port (SPP) – TRIS setting. Details of its operation are discussed in Section 18.0 "Streaming Parallel Port".

EXAMPLE 10-2: INITIALIZING PORTB

```
CLRF    PORTB   ; Initialize PORTB by
                ; clearing output
                ; data latches
CLRF    LATB    ; Alternate method
                ; to clear output
                ; data latches
MOVLW   0Eh     ; Set RB<4:0> as
MOVWF   ADCON1  ; digital I/O pins
                ; (required if config bit
                ; PBADEN is set)
MOVLW   0CFh    ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISB   ; Set RB<3:0> as inputs
                ; RB<5:4> as outputs
                ; RB<7:6> as inputs
```

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TABLE 10-3:   PORTB I/O SUMMARY (CONTINUED)

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RB6/KBI2/ PGC	RB6	0	OUT	DIG	LATB<6> data output.
		1	IN	TTL	PORTB<6> data input; weak pull-up when RBPU bit is cleared.
	KBI2	1	IN	TTL	Interrupt-on-pin change.
	PGC	x	IN	ST	Serial execution (ICSP™) clock input for ICSP and ICD operation.[3]
RB7/KBI3/ PGD	RB7	0	OUT	DIG	LATB<7> data output.
		1	IN	TTL	PORTB<7> data input; weak pull-up when RBPU bit is cleared.
	KBI3	1	IN	TTL	Interrupt-on-pin change.
	PGD	x	OUT	DIG	Serial execution data output for ICSP and ICD operation.[3]
		x	IN	ST	Serial execution data input for ICSP and ICD operation.[3]

Legend: OUT = Output, IN = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input,
I²C/SMB = I²C/SMBus input buffer, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option)

Note   1:   Configuration on POR is determined by PBADEN Configuration bit. Pins are configured as analog inputs when PBADEN is set and digital inputs when PBADEN is cleared.
        2:    Alternate pin assignment for CCP2 when CCP2MX = 0. Default assignment is RC1.
        3:    All other pin functions are disabled when ICSP™ or ICD operation is enabled.
        4:    40/44-pin devices only.

TABLE 10-4:   SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	54
LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	54
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	54
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RBIP	51
INTCON3	INT2P	INT1P	—	INT2IE	INT1IE	—	INT2IF	INT1IF	51
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	52
SPPCON[1]	—	—	—	—	—	—	SPPOWN	SPPEN	55
SPPCFG[1]	CLKCFG1	CLKCFG0	CSEN	CLK1EN	WS3	WS2	WS1	WS0	55
UCON	—	PPBRST	SE0	PKTDIS	USBEN	RESUME	SUSPND	—	55

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTB.
Note   1:   These registers are unimplemented on 28-pin devices.

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TABLE 10-3: PORTB I/O SUMMARY (CONTINUED)

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RB6/KBI2/ PGC	RB6	0	OUT	DIG	LATB<6> data output.
		1	IN	TTL	PORTB<6> data input; weak pull-up when $\overline{RBPU}$ bit is cleared.
	KBI2	1	IN	TTL	Interrupt-on-pin change.
	PGC	x	IN	ST	Serial execution (ICSP™) clock input for ICSP and ICD operation.[3]
RB7/KBI3/ PGD	RB7	0	OUT	DIG	LATB<7> data output.
		1	IN	TTL	PORTB<7> data input; weak pull-up when $\overline{RBPU}$ bit is cleared.
	KBI3	1	IN	TTL	Interrupt-on-pin change.
	PGD	x	OUT	DIG	Serial execution data output for ICSP and ICD operation.[3]
		x	IN	ST	Serial execution data input for ICSP and ICD operation.[2]

Legend: OUT = Output, IN = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, I²C/SMB = I²C/SMBus input buffer, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option)

Note 1: Configuration on POR is determined by PBADEN Configuration bit. Pins are configured as analog inputs when PBADEN is set and digital inputs when PBADEN is cleared.

2: Alternate pin assignment for CCP2 when CCP2MX = 0. Default assignment is RC1.

3: All other pin functions are disabled when ICSP™ or ICD operation is enabled.

4: 40/44-pin devices only.

TABLE 10-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	54
LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	54
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	54
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
INTCON2	$\overline{RBPU}$	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RBIP	51
INTCON3	INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF	51
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	52
SPPCON[1]	—	—	—	—	—	—	SPPOWN	SPPEN	55
SPPCFG[1]	CLKCFG1	CLKCFG0	CSEN	CLK1EN	WS3	WS2	WS1	WS0	55
UCON	—	PPBRST	SE0	PKTDIS	USBEN	RESUME	SUSPND	—	55

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTB.

Note 1: These registers are unimplemented on 28-pin devices.

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21.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) converter module has 10 inputs for the 28-pin devices and 13 for the 40/44-pin devices. This module allows conversion of an analog input signal to a corresponding 10-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 21-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 21-2, configures the functions of the port pins. The ADCON2 register, shown in Register 21-3, configures the A/D clock source, programmed acquisition time and justification.

REGISTER 21-1: ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS3:CHS0:** Analog Channel Select bits

    0000 = Channel 0 (AN0)
    0001 = Channel 1 (AN1)
    0010 = Channel 2 (AN2)
    0011 = Channel 3 (AN3)
    0100 = Channel 4 (AN4)
    0101 = Channel 5 (AN5)[1,2]
    0110 = Channel 6 (AN6)[1,2]
    0111 = Channel 7 (AN7)[1,2]
    1000 = Channel 8 (AN8)
    1001 = Channel 9 (AN9)
    1010 = Channel 10 (AN10)
    1011 = Channel 11 (AN11)
    1100 = Channel 12 (AN12)
    1101 = Unimplemented[2]
    1110 = Unimplemented[2]
    1111 = Unimplemented[2]

bit 1 **GO/DONE:** A/D Conversion Status bit

    When ADON = 1:
    1 = A/D conversion in progress
    0 = A/D Idle

bit 0 **ADON:** A/D On bit

    1 = A/D converter module is enabled
    0 = A/D converter module is disabled

Note 1: These channels are not implemented on 28-pin devices.
    2: Performing a conversion on unimplemented channels will return a floating input measurement.

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REGISTER 21-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0[1]	R/W[1]	R/W[1]	R/W[1]
—	—	VCFG0	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **VCFG0:** Voltage Reference Configuration bit (V$_{REF}$- source)

1 = V$_{REF}$- (AN2)
0 = V$_{SS}$

bit 4 **VCFG0:** Voltage Reference Configuration bit (V$_{REF}$+ source)

1 = V$_{REF}$+ (AN3)
0 = V$_{DD}$

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits:

PCFG3: PCFG0	AN12	AN11	AN10	AN9	AN8	AN7[2]	AN6[2]	AN5[2]	AN4	AN3	AN2	AN1	AN0
0000[1]	A	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A	A
0011	D	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	D	A	A	A	A	A	A	A	A	A
0111[1]	D	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input   D = Digital I/O

Note 1: The POR value of the PCFG bits depends on the value of the PBADEN Configuration bit. When PBADEN = 1, PCFG<3:0> = 0000; when PBADEN = 0, PCFG<3:0> = 0111.

2: AN5 through AN7 are available only on 40/44-pin devices.

PIC18F2455/2550/4455/4550

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (VDD and VSS) or the voltage level on the RA3/AN3/VREF+ and RA2/AN2/VREF-/CVREF pins.

The A/D converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0 register) is cleared and A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 21-1.

FIGURE 21-1: A/D BLOCK DIAGRAM

Note 1: Channels AN5 through AN7 are not available on 28-pin devices.

2: I/O pins have diode protection to VDD and VSS.

Preliminary
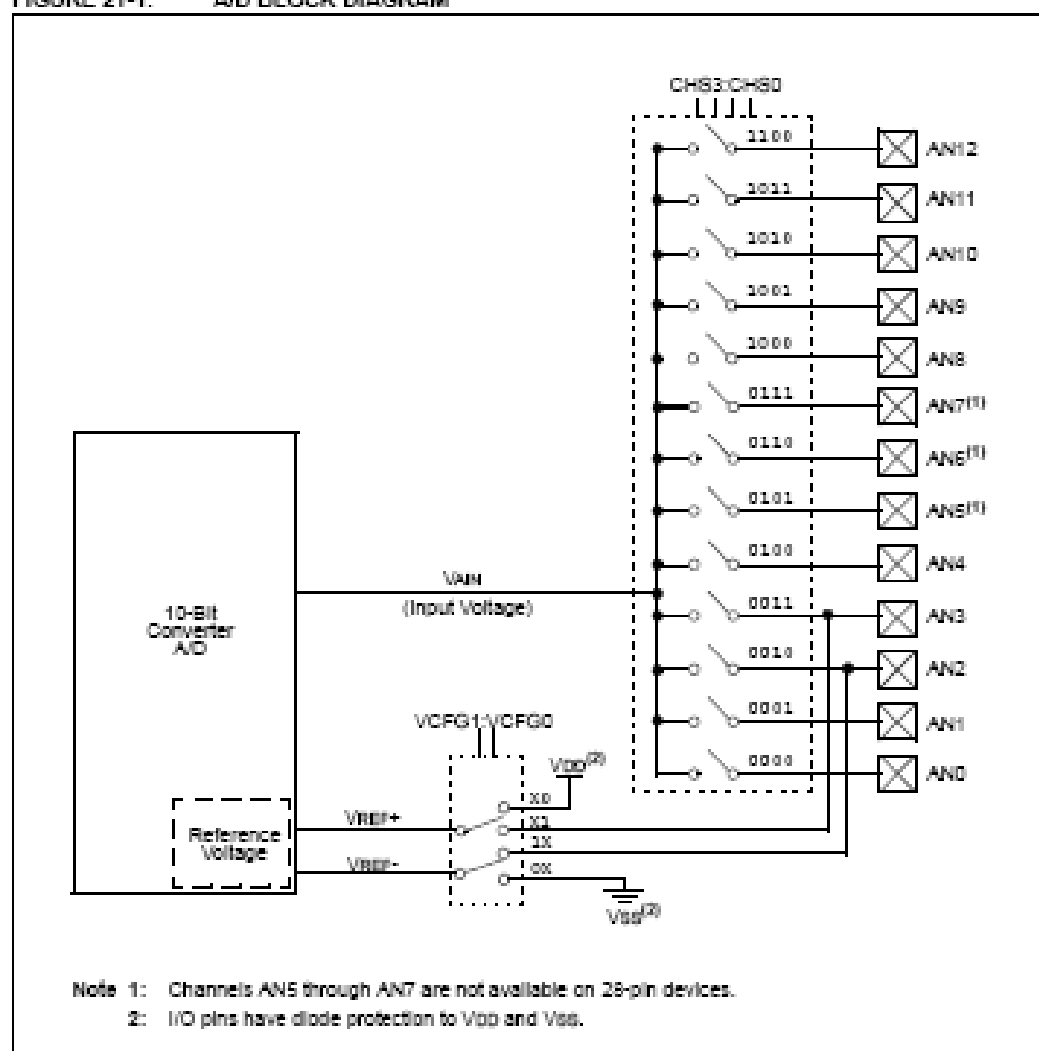
APPENDIX C

LM7805 Voltage Regulator Datasheet

FAIRCHILD
SEMICONDUCTOR®

March 2008

LM78XX/LM78XXA
3-Terminal 1A Positive Voltage Regulator

Features

- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

General Description

The LM78XX series of three terminal positive regulators are available in the TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

Ordering Information

Product Number	Output Voltage Tolerance	Package	Operating Temperature
LM7805CT	±4%	TO-220	-40°C to +125°C
LM7806CT			
LM7808CT			
LM7809CT			
LM7810CT			
LM7812CT			
LM7815CT			
LM7818CT			
LM7824CT			
LM7805ACT	±2%		0°C to +125°C
LM7806ACT			
LM7808ACT			
LM7809ACT			
LM7810ACT			
LM7812ACT			
LM7815ACT			
LM7818ACT			
LM7824ACT			

LM78XX/LM78XXA 3-Terminal 1A Positive Voltage Regulator

Block Diagram

Figure 1.

Pin Assignment

TO-220
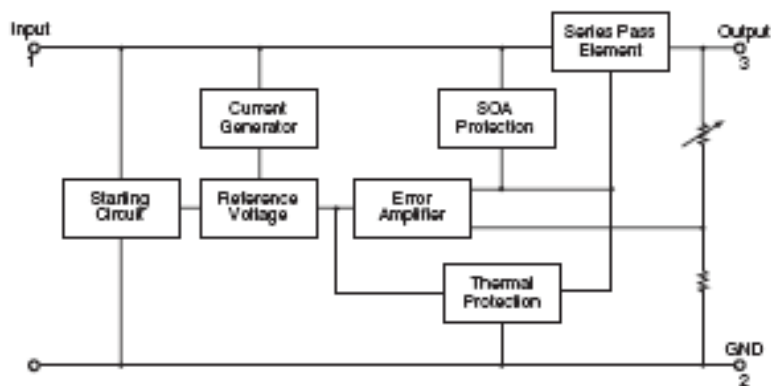
1. Input
2. GND
3. Output
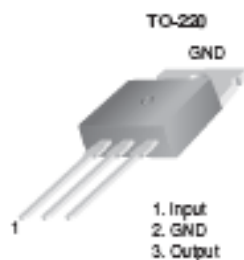
Figure 2.

Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Symbol	Parameter		Value	Unit
V_I	Input Voltage	V_O = 5V to 18V	35	V
		V_O = 24V	40	V
$R_{\theta JC}$	Thermal Resistance Junction-Cases (TO-220)		5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction-Air (TO-220)		65	°C/W
T_{OPR}	Operating Temperature Range	LM78xx	-40 to +125	°C
		LM78xxA	0 to +125	
T_{STG}	Storage Temperature Range		-65 to +150	°C

<div style="text-align: right">LM78XX/LM78XXA 3-Terminal 1A Positive Voltage Regulator</div>

Electrical Characteristics (LM7805)

Refer to the test circuits. -40°C < T_J < 125°C, I_O = 500mA, V_I = 10V, C_I = 0.1μF, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_J = +25°C		4.8	5.0	5.2	V
		5mA ≤ I_O ≤ 1A, P_O ≤ 15W, V_I = 7V to 20V		4.75	5.0	5.25	
Regline	Line Regulation[1]	T_J = +25°C	V_O = 7V to 25V	–	4.0	100	mV
			V_I = 8V to 12V	–	1.6	50.0	
Regload	Load Regulation[1]	T_J = +25°C	I_O = 5mA to 1.5A	–	9.0	100	mV
			I_O = 250mA to 750mA	–	4.0	50.0	
I_Q	Quiescent Current	T_J = +25°C		–	5.0	8.0	mA
ΔI_Q	Quiescent Current Change	I_O = 5mA to 1A		–	0.03	0.5	mA
		V_I = 7V to 25V		–	0.3	1.3	
$\Delta V_O/\Delta T$	Output Voltage Drift[2]	I_O = 5mA		–	-0.8	–	mV/°C
V_N	Output Noise Voltage	f = 10Hz to 100kHz, T_A = +25°C		–	42.0	–	μV/V_O
RR	Ripple Rejection[2]	f = 120Hz, V_O = 8V to 18V		62.0	73.0	–	dB
V_{DROP}	Dropout Voltage	I_O = 1A, T_J = +25°C		–	2.0	–	V
r_O	Output Resistance[2]	f = 1kHz		–	15.0	–	mΩ
I_{SC}	Short Circuit Current	V_I = 35V, T_A = +25°C		–	230	–	mA
I_{PK}	Peak Current[2]	T_J = +25°C		–	2.2	–	A

Notes:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

2. These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7805A) (Continued)

Refer to the test circuits. $0°C < T_J < 125°C$, $I_O = 1A$, $V_I = 10V$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_O	Output Voltage	$T_J = +25°C$		4.9	5.0	5.1	V
		$I_O = 5mA$ to $1A$, $P_O \leq 15W$, $V_I = 7.5V$ to $20V$		4.8	5.0	5.2	
Regline	Line Regulation[19]	$V_I = 7.5V$ to $25V$, $I_O = 500mA$		–	5.0	50.0	mV
		$V_I = 8V$ to $12V$		–	3.0	50.0	
		$T_J = +25°C$	$V_I = 7.3V$ to $20V$	–	5.0	50.0	
			$V_I = 8V$ to $12V$	–	1.5	25.0	
Regload	Load Regulation[19]	$T_J = +25°C$, $I_O = 5mA$ to $1.5A$		–	9.0	100	mV
		$I_O = 5mA$ to $1A$		–	9.0	100	
		$I_O = 250mA$ to $750mA$		–	4.0	50.0	
I_Q	Quiescent Current	$T_J = +25°C$		–	5.0	6.0	mA
ΔI_Q	Quiescent Current Change	$I_O = 5mA$ to $1A$		–	–	0.5	mA
		$V_I = 8V$ to $25V$, $I_O = 500mA$		–	–	0.8	
		$V_I = 7.5V$ to $20V$, $T_J = +25°C$		–	–	0.8	
$\Delta V_O/\Delta T$	Output Voltage Drift[20]	$I_O = 5mA$		–	-0.8	–	mV/°C
V_N	Output Noise Voltage	$f = 10Hz$ to $100kHz$, $T_A = +25°C$		–	10.0	–	$\mu V/V_O$
RR	Ripple Rejection[20]	$f = 120Hz$, $I_O = 500mA$, $V_I = 8V$ to $18V$		–	68.0	–	dB
V_{DROP}	Dropout Voltage	$I_O = 1A$, $T_J = +25°C$		–	2.0	–	V
r_O	Output Resistance[20]	$f = 1kHz$		–	17.0	–	mΩ
I_{SC}	Short Circuit Current	$V_I = 35V$, $T_A = +25°C$		–	250	–	mA
I_{PK}	Peak Current[20]	$T_J = +25°C$		–	2.2	–	A

Notes:

19. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

20. These parameters, although guaranteed, are not 100% tested in production.

Typical Performance Characteristics
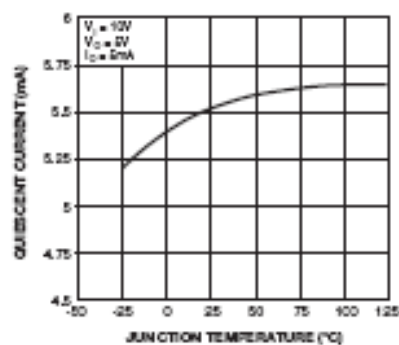
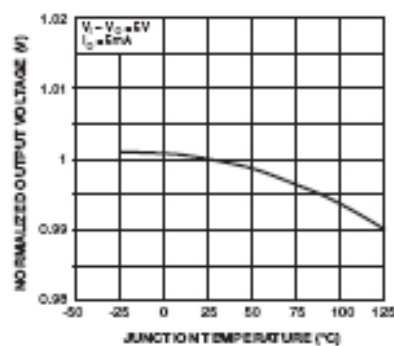Figure 3. Quiescent Current
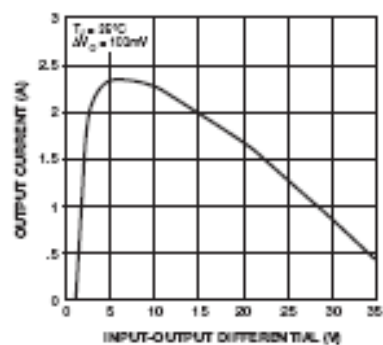
Figure 4. Peak Output Current
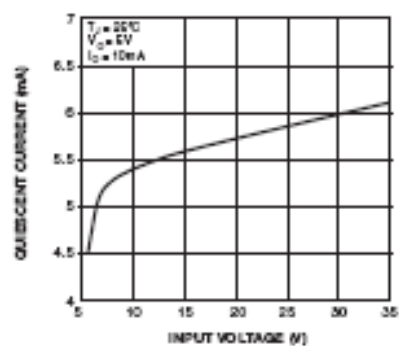

Figure 5. Output Voltage

Figure 6. Quiescent Current
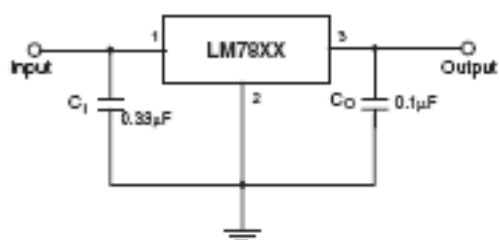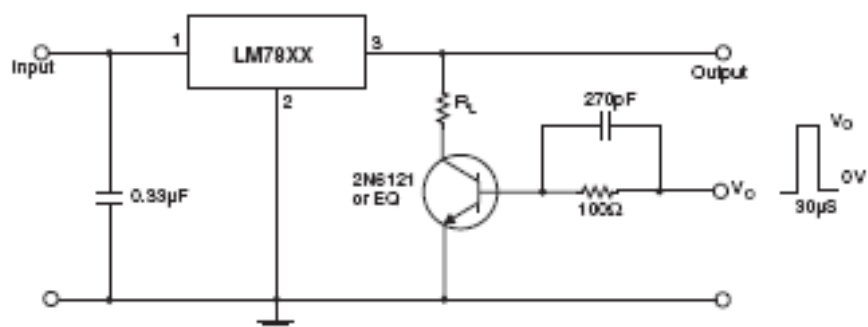
Typical Applications

Figure 7. DC Parameters

Figure 8. Load Regulation
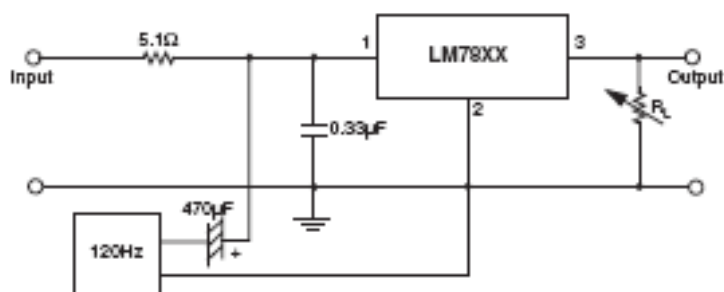
Figure 9. Ripple Rejection

LM78XX/LM78XXA 3-Terminal 1A Positive Voltage Regulator
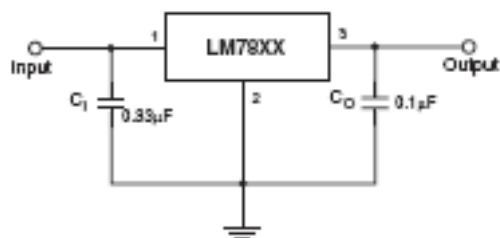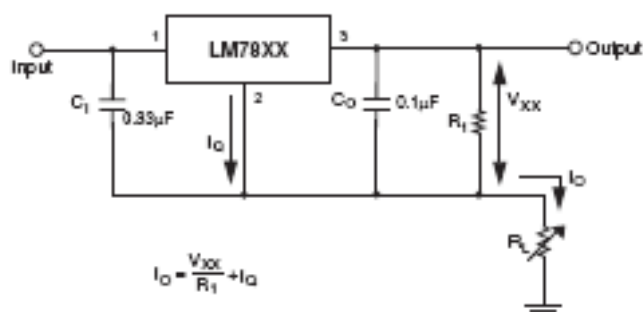
Figure 10. Fixed Output Regulator

$$I_O = \frac{V_{XX}}{R_1} + I_Q$$

Notes:
1. To specify an output voltage, substitute voltage value for "XX." A common ground is required between the input and the output voltage. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.
2. C_I is required if regulator is located an appreciable distance from power supply filter.
3. C_O improves stability and transient response.

Figure 11.

$$I_R \geq 5\ I_Q$$
$$V_O = V_{XX}(1 + R_2/R_1) + I_Q R_2$$
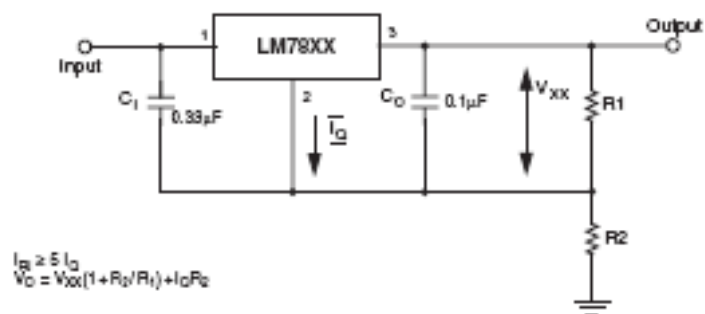
Figure 12. Circuit for Increasing Output Voltage

Mechanical Dimensions
Dimensions in millimeters

TO-220

Dimensions are in mm

NOTES: UNLESS OTHERWISE SPECIFIED
A) REFERENCE JEDEC, TO-220, ISSUE K, VARIATION AB, DATED APRIL, 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1973
D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E) DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS REPRESENT LIKE BELOW: SINGLE GAUGE = 0.51 - 0.61

G) DRAWING FILE NAME: TO220B03REV6
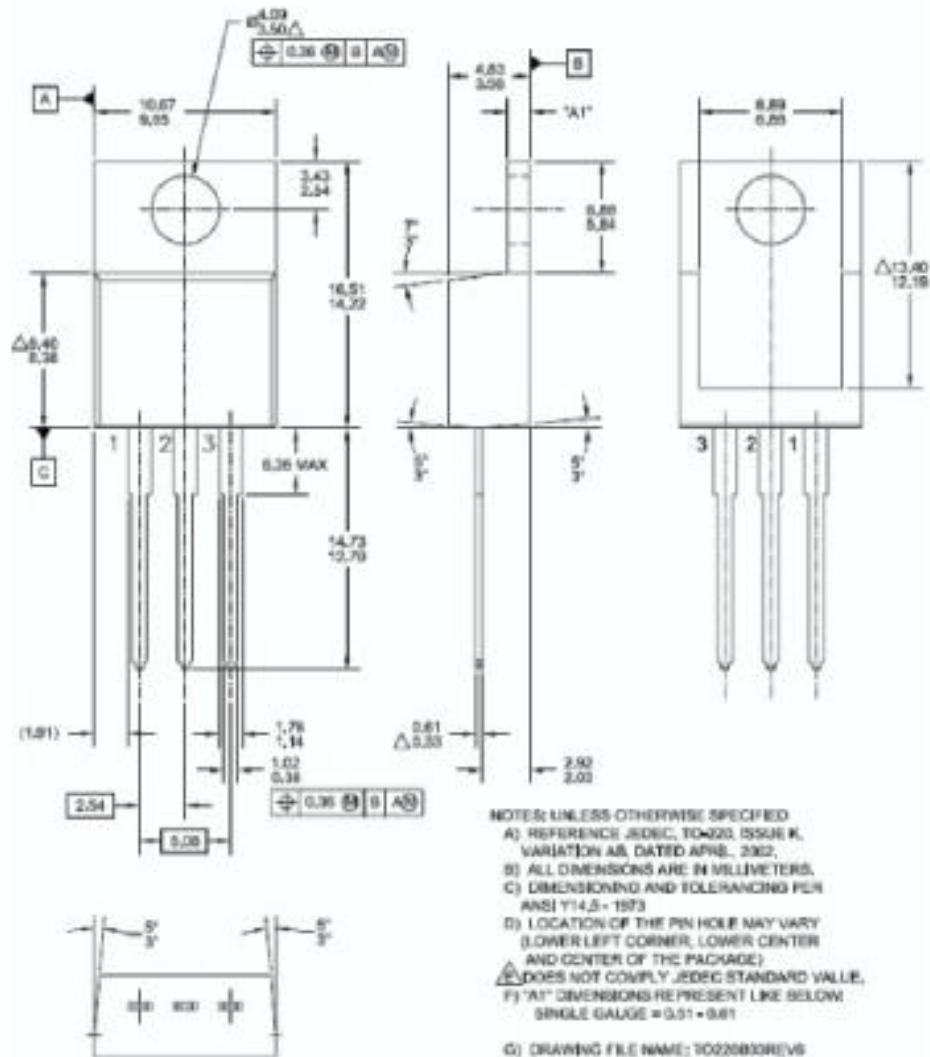
APPENDIX D

JHD162A Series Datasheet

JHD162A SERIES

DISPLAY CONTENT = 16 CHAR x 2ROW

CHAR. DOTS: 5 x 8

DRIVING MODE: 1/16D

AVAILABLE TYPES:

TN: STN(YELLOW GREEN: GREY: B/W)
REFLECTIVE: WITH EL OR LED BACKLIGHT
EL/100VAC: 400HZ
LED/4.2VDC

Parameter	Symbol	Testing Criteria	Standard Values				
			Min.	Typ.	Max.	Unit
Supply voltage	$V_{DD}-V_{SS}$	-	4.5	5.0	5.5	V
Input high voltage	V_{IH}	-	2.2	-	V_{DD}	V
Input low voltage	V_{IL}	-	-0.3	-	0.6	V
Output high voltage	V_{OH}	-Ioh=0.2mA	2.4	-	-	V
Output low voltage	V_{OL}	Iol=1.2mA	-	-	0.4	V
Operating voltage	I_{DD}	$V_{DD}=5.0V$	-	1.5	3.0	mA
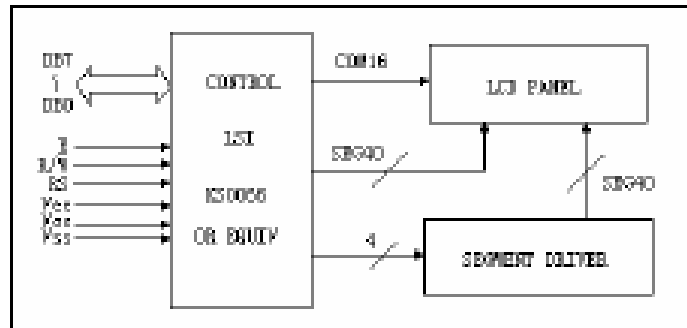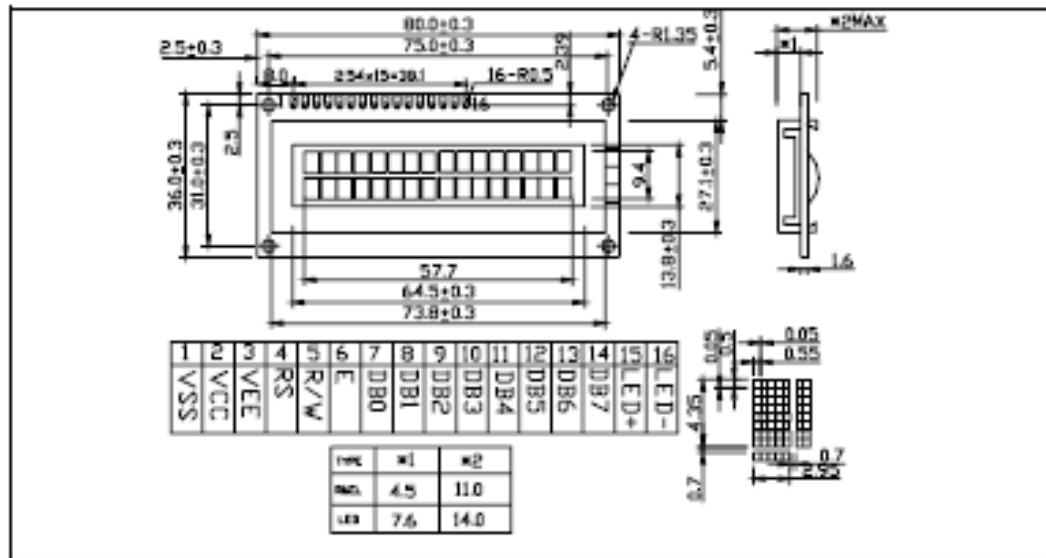
| 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
VSS	VCC	VEE	RS	R/W	E	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	LED+	LED-

■ AC Characteristics Read Mode Timing Diagram

Table 12. AC Characteristics (V_{DD} = 4.5V ~ 5.5V, Ta = -30 ~ +85°C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode (Refer to Fig-6)	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	t_R, t_F	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu1	40	-	-	
	R/W and RS Hold Time	t_{H1}	10	-	-	
	Data Setup Time	tsu2	80	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode (Refer to Fig-7)	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	t_R, t_F	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu	40	-	-	
	R/W and RS Hold Time	t_H	10	-	-	
	Data Output Delay Time	t_D	-	-	120	
	Data Hold Time	t_{DH}	5	-	-	

Table 13. AC Characteristics (V_{DD} =2.7V ~ 4.5V, Ta = -30 ~ +85°C)

| Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode (Refer to Fig-6)	E Cycle Time	tc	1000	-	-	ns
	E Rise / Fall Time	t_R, t_F	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu1	60	-	-	
	R/W and RS Hold Time	t_{H1}	20	-	-	
	Data Setup Time	tsu2	195	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode (Refer to Fig-7)	E Cycle Time	tc	1000	-	-	ns
	E Rise / Fall Time	t_R, t_F	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu	60	-	-	
	R/W and RS Hold Time	t_H	20	-	-	
	Data Output Delay Time	t_D	-	-	360	
	Data Hold Time	t_{DH}	5	-	-	
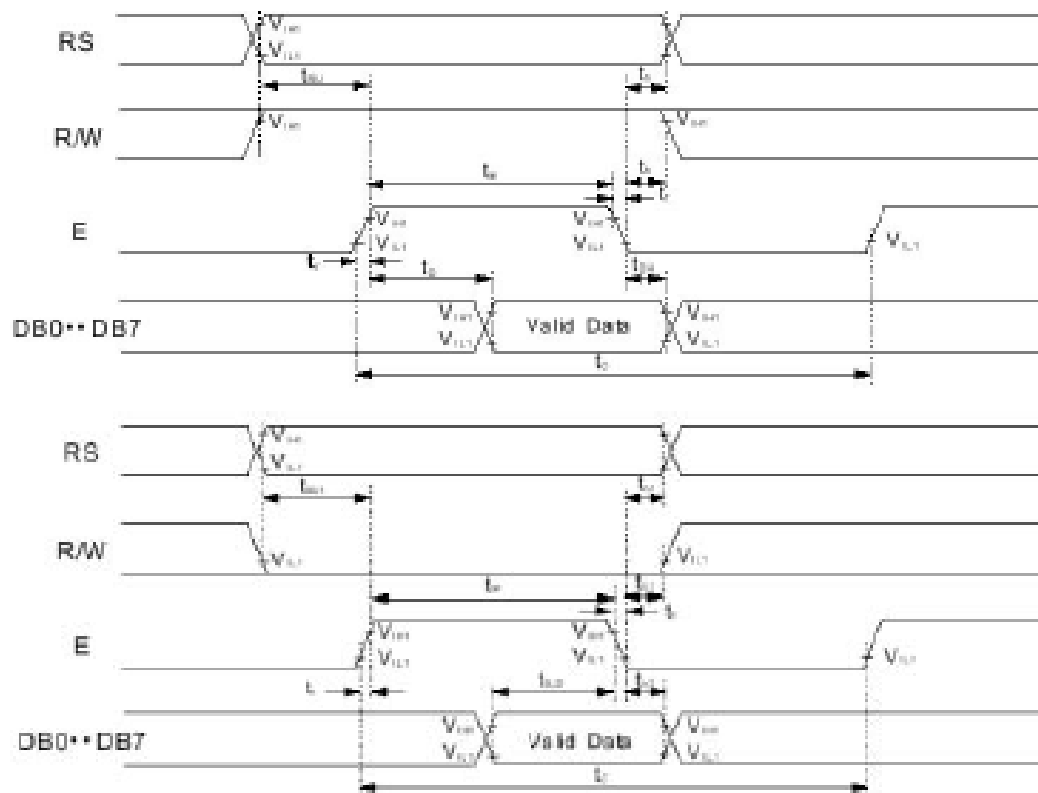
Write Mode Timing Diagram

Timing

1) Interface with 8-bit MPU
   When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7.
   Example of timing sequence is shown below.
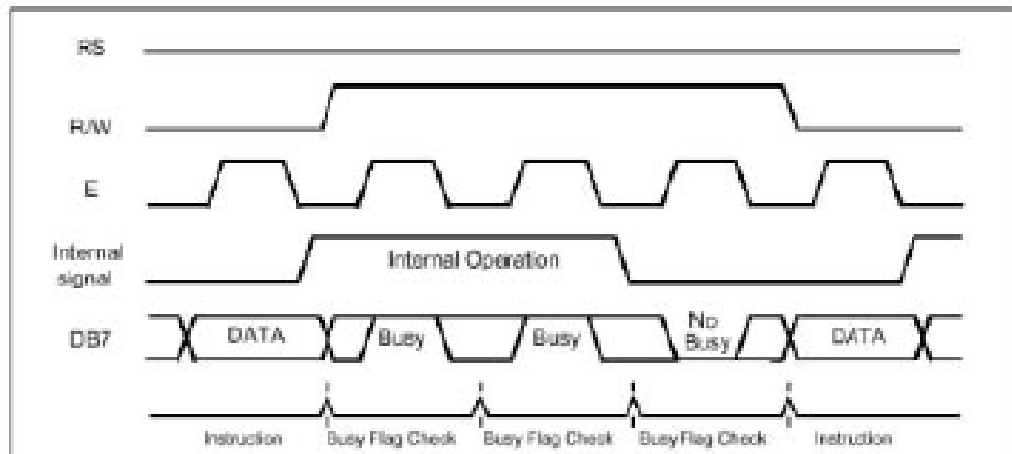
APPENDIX E

Current Sensor Data Sheet

Current Sensor: ACS754xCB-050

Package CB-PFF

Package CB-PSF

Package CB-PSS

Pin 1: VCC   Terminal 4: IP+
Pin 2: GND   Terminal 5: IP–
Pin 3: VOUT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	16 V
Reverse Supply Voltage, V_{RCC}	–16 V
Output Voltage, V_{OUT}	16 V
Reverse Output Voltage, V_{ROUT}	–0.1 V
Output Current Source, $I_{OUT(Source)}$	3 mA
Output Current Sink, $I_{OUT(Sink)}$	10 mA
Operating Temperature,	
Ambient, T_A, L range	–40 to 150°C
Ambient, T_A, S range	–20 to 85°C
Maximum Junction, $T_{J(max)}$	165°C
Maximum Storage Temperature, T_S	–65 to 170°C

TÜV America
Certificate Number:
U8V 04 11 54214 001

The Allegro ACS75x family of current sensors provides economical and precise solutions for current sensing in industrial, automotive, commercial, and communications systems. The device package allows for easy implementation by the customer. Typical applications include motor control, load detection and management, power supplies, and overcurrent fault protection.

The device consists of a precision, low-offset linear Hall sensor circuit with a copper conduction path located near the die. Applied current flowing through this copper conduction path generates a magnetic field which is sensed by the integrated Hall IC and converted into a proportional voltage. Device accuracy is optimized through the close proximity of the magnetic signal to the Hall transducer. A precise, proportional voltage is provided by the low-offset, chopper-stabilized BiCMOS Hall IC, which is programmed for accuracy at the factory.

The output of the device has a positive slope ($>V_{CC}/2$) when an increasing current flows through the primary copper conduction path (from terminal 4 to terminal 5), which is the path used for current sensing. The internal resistance of this conductive path is typically 100 μΩ, providing low power loss. The thickness of the copper conductor allows survival of the device at up to 5× overcurrent conditions. The terminals of the conductive path are electrically isolated from the sensor leads (pins 1 through 3). This allows the ACS75x family of sensors to be used in applications requiring electrical isolation without the use of opto-isolators or other costly isolation techniques.

The device is fully calibrated prior to shipment from the factory. The ACS75x family is lead-free. All leads are coated with 100% matte tin, and there is no lead inside the package. The heavy gauge leadframe is made of oxygen-free copper.

Features and Benefits
- Monolithic Hall IC for high reliability
- Single +5 V supply
- 3 kV$_{RMS}$ isolation voltage between terminals 4/5 and pins 1/2/3
- 35 kHz bandwidth
- Automotive temperature range
- End-of-line factory-trimmed for gain and offset
- Ultra-low power loss: 100 μΩ internal conductor resistance
- Ratiometric output from supply voltage
- Extremely stable output offset voltage
- Small package size, with easy mounting capability
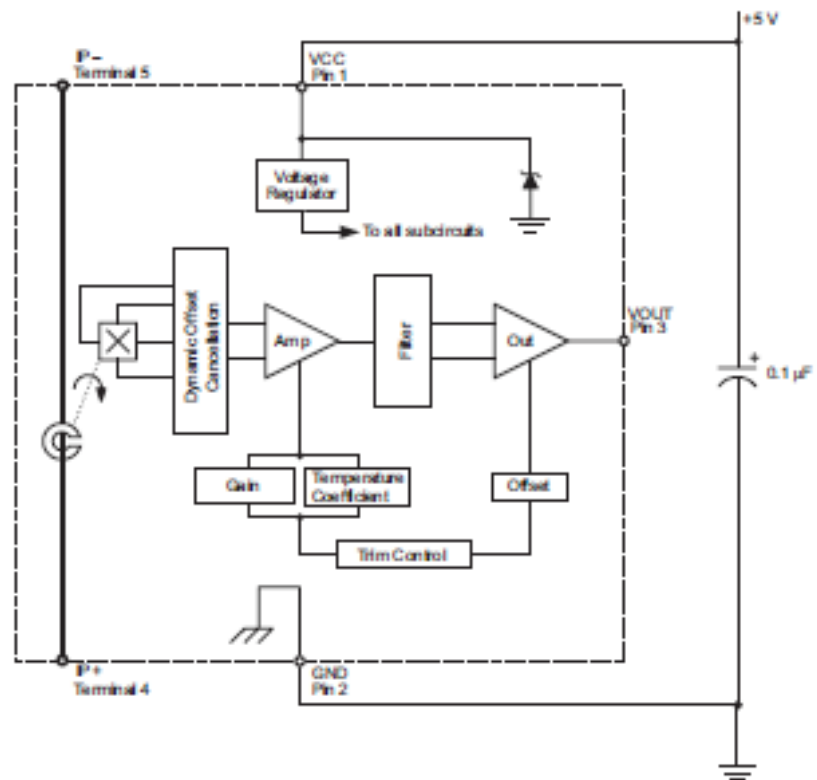- Output proportional to ac and dc currents

Applications
- Automotive systems
- Industrial systems
- Motor control
- Servo systems
- Power conversion
- Battery monitors

Use the following complete part numbers when ordering:

Part Number	Signal Pins	Terminals	Ambient
ACS754LCB-050-PFF	Formed	Formed	
ACS754LCB-050-PSF	Formed	Straight	–40 to 150°C
ACS754LCB-050-PSS	Straight	Straight	
ACS754SCB-050-PFF	Formed	Formed	
ACS754SCB-050-PSF	Formed	Straight	–20 to 85°C
ACS754SCB-050-PSS	Straight	Straight	

ACS754050-DS, Rev. 3

Allegro
MicroSystems, Inc.

115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

Current Sensor: ACS754xCB-050

Functional Block Diagram

Current Sensor: ACS754xCB-050

ELECTRICAL CHARACTERISTICS, over operating ambient temperature range unless otherwise stated

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Primary Sensed Current	I_P		−50	−	50	A
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Supply Current	I_{CC}	V_{CC} = 5.0 V, output open	6.5	8	10	mA
Output Resistance	R_{OUT}	I_{OUT} = 1.2 mA	−	1	2	Ω
Output Capacitance Load	C_{LOAD}	VOUT to GND	−	−	10	nF
Output Resistive Load	R_{LOAD}	VOUT to GND	4.7	−	−	kΩ
Primary Conductor Resistance	$R_{PRIMARY}$	I_P = ±100A; T_A = 25°C	−	100	−	µΩ
		Pins 1-3 and 4-5; 60 Hz, 1 minute	3.0	−	−	kV
PERFORMANCE CHARACTERISTICS, -20°C to +85°C, V_{CC} = 5 V unless otherwise specified						
Propagation time	t_{PROP}	I_P = ±50 A, T_A = 25°C	−	4	−	µs
Response time	$t_{RESPONSE}$	I_P = ±50 A, T_A = 25°C	−	12	−	µs
Rise time	t_r	I_P = ±50 A, T_A = 25°C	−	11	−	µs
Frequency Bandwidth	f	−3 dB , T_A = 25°C	−	35	−	kHz
Sensitivity	Sens	Over full range of I_P, T_A = 25°C	−	40	−	mV/A
		Over full range of I_P	37.8	−	42.0	mV/A
Noise	V_{NOISE}	Peak-to-peak, T_A = 25°C, no external filter	−	65	−	mV
Nonlinearity	E_{LIN}	Over full range of I_P	−	−	±1.5	%
Symmetry	E_{SYM}	Over full range of I_P	98	100	102	%
Zero Current Output Voltage	$V_{OUT(Q)}$	I = 0 A, T_A = 25°C	−	V_{CC}/2	−	V
Electrical Offset Voltage (Magnetic error not included)	V_{OE}	I = 0 A, T_A = 25°C	−10	−	10	mV
		I = 0 A	−20	−	20	mV
Magnetic Offset Error	I_{ERROM}	I = 0 A, after excursion of 100 A	−	±0.1	±0.30	A
Total Output Error (Including all offsets)	E_{TOT}	Over full range of I_P, T_A = 25°C	−	±1.0	−	%
		Over full range of I_P	−	−	±5.0	%
PERFORMANCE CHARACTERISTICS, -40°C to +160°C, V_{CC} = 5 V unless otherwise specified						
Propagation time	t_{PROP}	I_P = ±50 A, T_A = 25°C	−	4	−	µs
Response time	$t_{RESPONSE}$	I_P = ±50 A, T_A = 25°C	−	12	−	µs
Rise time	t_r	I_P = ±50 A, T_A = 25°C	−	11	−	µs
Frequency Bandwidth	f	−3 dB , T_A = 25°C	−	35	−	kHz
Sensitivity	Sens	Over full range of I_P, T_A = 25°C	−	40	−	mV/A
		Over full range of I_P	36.0	−	42.8	mV/A
Noise	V_{NOISE}	Peak-to-peak, T_A = 25°C, no external filter	−	65	−	mV
Nonlinearity	E_{LIN}	Over full range of I_P	−	−	±1.8	%
Symmetry	E_{SYM}	Over full range of I_P	98	100	102	%
Zero Current Output Voltage	$V_{OUT(Q)}$	I = 0 A, T_A = 25°C	−	V_{CC}/2	−	V
Electrical Offset Voltage (Magnetic error not included)	V_{OE}	I = 0 A, T_A = 25°C	−10	−	10	mV
		I = 0 A	−35	−	35	mV
Magnetic Offset Error	I_{ERROM}	I = 0 A, after excursion of 100 A	−	±0.1	±0.40	A
Total Output Error (Including all offsets)	E_{TOT}	Over full range of I_P, T_A = 25°C	−	±1.0	−	%
		Over full range of I_P	−	−	±9.9	%

Current Sensor: ACS754xCB-050

Definitions of Accuracy Characteristics

Sensitivity (Sens): The change in sensor output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is trimmed at the factory to optimize the sensitivity (mV/A) for the full-scale current of the device.

Noise (V_{NOISE}): The product of the linear IC amplifier gain (mV/G) and the noise floor for the Allegro Hall effect linear IC ($\approx$1 G). The noise floor is derived from the thermal and shot noise observed in Hall elements. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

Linearity (E_{LIN}): The degree to which the voltage output from the sensor varies in direct proportion to the primary current through its full-scale amplitude. Linearity reveals the maximum deviation from the ideal transfer curve for this transducer. Nonlinearity in the output can be attributed to the gain variation across temperature and saturation of the flux concentrator approaching the full-scale current. The following equation is used to derive the linearity:

$$100 \left\{ 1 - \left[\frac{\Delta \text{ gain } \times \% \text{ sat } (V_{out\_full\text{-}scale\ amperes} - V_{OUT(Q)})}{2 (V_{out\_half\text{-}scale\ amperes} - V_{OUT(Q)})} \right] \right\}$$

where

Δ gain = the gain variation as a function of temperature changes from 25°C,

% sat = the percentage of saturation of the flux concentrator, which becomes significant as the current being sensed approaches full-scale $\pm I_P$, and

$V_{out\_full\text{-}scale\ amperes}$ = the output voltage (V) when the sensed current approximates full-scale $\pm I_P$.

Symmetry (E_{SYM}): The degree to which the absolute voltage output from the sensor varies in proportion to either a positive or negative full-scale primary current. The following equation is used to derive symmetry:

$$100 \left[\frac{V_{out\ +full\text{-}scale\ amperes} - V_{OUT(Q)}}{V_{OUT(Q)} - V_{out\ -full\text{-}scale\ amperes}} \right]$$

Quiescent output voltage ($V_{OUT(Q)}$): The output of the sensor when the primary current is zero. For a unipolar supply voltage, it nominally remains at $V_{CC}/2$. Thus, $V_{CC} = 5$ V translates into $V_{OUT(Q)} = 2.5$ V. Variation in $V_{OUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim, magnetic hysteresis, and thermal drift.

Electrical offset voltage (V_{OE}): The deviation of the device output from its ideal quiescent value of $V_{CC}/2$ due to nonmagnetic causes.

Magnetic offset error (I_{ERROM}): The magnetic offset is due to the residual magnetism (remnant field) of the core material. The magnetic offset error is highest when the magnetic circuit has been saturated, usually when the device has been subjected to a full-scale or high-current overload condition. The magnetic offset is largely dependent on the material used as a flux concentrator. The larger magnetic offsets are observed at the lower operating temperatures.

Accuracy (E_{TOT}): The accuracy represents the maximum deviation of the actual output from its ideal value. This is also known as the total ouput error. The accuracy is illustrated graphically in the Output Voltage versus Current chart on the following page.

Accuracy is divided into four areas:

- **0 A at 25°C:** Accuracy of sensing zero current flow at 25°C, without the effects of temperature,

- **0 A over temperature:** Accuracy of sensing zero current flow including temperature effects,

- **Full-scale current at 25°C:** Accuracy of sensing the full-scale current at 25°C, without the effects of temperature.

- **Full-scale current over Δ temperature:** Accuracy of sensing full-scale current flow including temperature effects.

Current Sensor: ACS754xCB-050

Typical Percentage Error versus Ambient Temperature
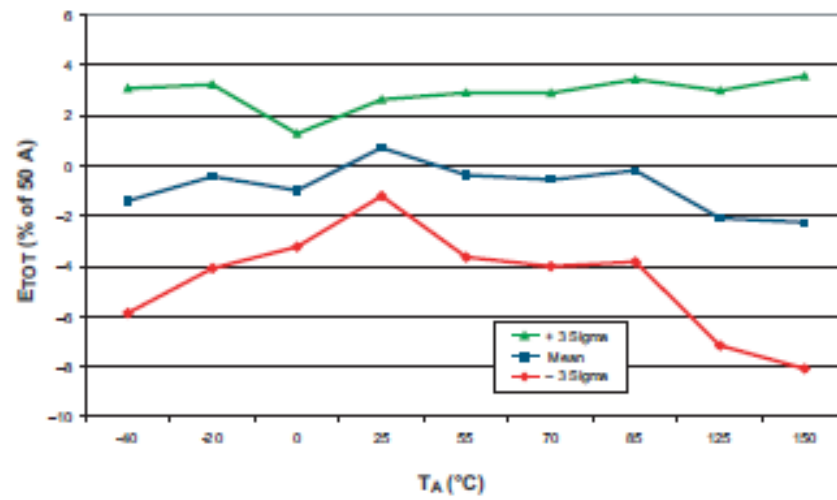
Current Sensor: ACS754xCB-050

Definitions of Dynamic Response Characteristics

Propagation delay (t_{PROP}): The time required for the sensor output to reflect a change in the primary current signal. Propagation delay is attributed to inductive loading within the linear IC package, as well as in the inductive loop formed by the primary conductor geometry. Propagation delay can be considered as a fixed time offset and may be compensated.
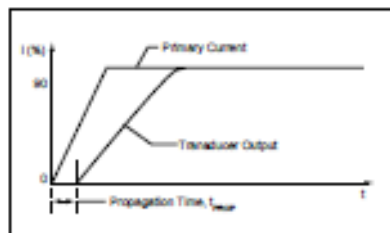
Response time ($t_{RESPONSE}$): The time interval between a) when the primary current signal reaches 90% of its final value, and b) when the sensor reaches 90% of its output corresponding to the applied current.
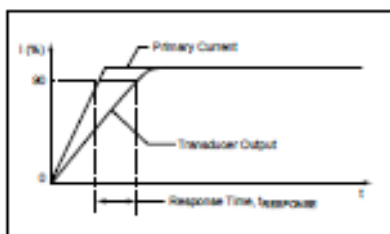
Rise time (t_r): The time interval between a) when the sensor reaches 10% of its full scale value, and b) when it reaches 90% of its full scale value. The rise time to a step response is used to derive the bandwidth of the current sensor, in which $f(-3\ dB) = 0.35/t_r$. Both t_r and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane and, to varying degrees, in the ferrous flux concentrator within the current sensor package.
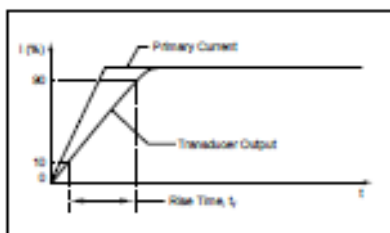
APPENDIX F

APFC Program

AUTOMATIC POWER FACTOR CORRECTION DEVICE PROGRAMMING USING PIC-C (COMPILER)

```c
#include <18F4550.h>
#device adc=8
#use delay(clock=20000000)
#use standard_io ( A )
#use standard_io ( B )
#use standard_io ( C )
#FUSES NOWDT,HS,NOPROTECT,NOBROWNOUT,NOLVP

// LCD STUFF
#define LCD_D0     PIN_B4
#define LCD_D1     PIN_B5
#define LCD_D2     PIN_B6
#define LCD_D3     PIN_B7
#define LCD_RW     PIN_B1
#define LCD_EN     PIN_B3
#define LCD_RS     PIN_B0
#define LINE_1     0x00
#define LINE_2     0x40
#define CLEAR_DISP  0x01
#define DEGREE_SYM  0xdf

void LCD_Init ( void );
void LCD_SetPosition ( unsigned int cX );
void LCD_PutChar ( unsigned int cX );
void LCD_PutCmd ( unsigned int cX );
void LCD_PulseEnable ( void );
void LCD_SetData ( unsigned int cX );

void main()
{byte k;
 delay_ms ( 200 );
 output_low(PIN_B1);



 // set adc port
 setup_adc_ports(AN0|VSS_VDD);
 setup_adc( ADC_CLOCK_DIV_16);

 LCD_Init();
 LCD_SetPosition ( LINE_1 + 2 );
 printf ( LCD_PutChar, "MOHD AZUARI " );
 delay_us (3000);
 LCD_SetPosition ( LINE_2 + 4 );
```

```
printf ( LCD_PutChar, "EC 07070 ");


while ( TRUE )
{
set_adc_channel(0);
delay_us(80);
k=read_adc();
output_d(0b0000000);


if(k>12){output_d(0b00000001);
LCD_SetPosition ( LINE_2 + 0 );
printf ( LCD_PutChar, "CAPACITOR STEP 1");
LCD_SetPosition ( LINE_1 + 1 );
printf ( LCD_PutChar, "P.F CORRECTION" );}
else if(60>k>70){output_d(0b00000011);
printf ( LCD_PutChar, "CAPACITOR STEP 2");
LCD_SetPosition ( LINE_1 + 1 );
printf ( LCD_PutChar, "P.F CORRECTION" ); }
else if(150>k>200){output_d(0b00000111);
LCD_SetPosition ( LINE_2 + 0 );
printf ( LCD_PutChar, "CAPACITOR STEP 3");
LCD_SetPosition ( LINE_1 + 1 );
printf ( LCD_PutChar, "P.F CORRECTION" );}


}
}

void LCD_Init ( void )
  {
  LCD_SetData ( 0x00 );
  delay_ms ( 200 );      // wait enough time after Vdd rise
  output_low ( LCD_RS );
  LCD_SetData ( 0x03 );   // init with specific nibbles to start 4-bit mode
  LCD_PulseEnable();
  LCD_PulseEnable();
  LCD_PulseEnable();
  LCD_SetData ( 0x02 );   // set 4-bit interface
  LCD_PulseEnable();      // send dual nibbles hereafter, MSN first
  LCD_PutCmd ( 0x2C );    // function set (all lines, 5x7 characters)
  LCD_PutCmd ( 0x0C );    // display ON, cursor off, no blink
  LCD_PutCmd ( 0x01 );    // clear display
  LCD_PutCmd ( 0x06 );    // entry mode set, increment
  }
```

```
void LCD_SetPosition ( unsigned int cX )
  {
  // this subroutine works specifically for 4-bit Port A
  LCD_SetData ( swap ( cX ) | 0x08 );
  LCD_PulseEnable();
  LCD_SetData ( swap ( cX ) );
  LCD_PulseEnable();
  }

void LCD_PutChar ( unsigned int cX )
  {
  // this subroutine works specifically for 4-bit Port A
  output_high ( LCD_RS );
  LCD_SetData ( swap ( cX ) );    // send high nibble
  LCD_PulseEnable();
  LCD_SetData ( swap ( cX ) );    // send low nibble
  LCD_PulseEnable();
  output_low ( LCD_RS );
  }

void LCD_PutCmd ( unsigned int cX )
  {
  // this subroutine works specifically for 4-bit Port A
  LCD_SetData ( swap ( cX ) );    // send high nibble
  LCD_PulseEnable();
  LCD_SetData ( swap ( cX ) );    // send low nibble
  LCD_PulseEnable();
  }

void LCD_PulseEnable ( void )
  {
  output_high ( LCD_EN );
  delay_us ( 10 );
  output_low ( LCD_EN );
  delay_ms ( 5 );
  }

void LCD_SetData ( unsigned int cX )
  {
  output_bit ( LCD_D0, cX & 0x01 );
  output_bit ( LCD_D1, cX & 0x02 );
  output_bit ( LCD_D2, cX & 0x04 );
  output_bit ( LCD_D3, cX & 0x08 );
  }
```

APPENDIX G

Biodata of the Author

AUTHOR'S BIODATA

Mohd Azuari bin Mustapha was born on 27th September 1986 in Kota Bharu, Kelantan. His permanent address is at 263, Kg Serian Beta, 15100 Kota Bharu, Kelantan. He is eight from nine siblings, he has four brother and four sister. His first education is Sekolah Rendah Kebangsaan Dewan Beta. After 5 year searching for knowledge there, he enter his secondary education at Sekolah Mengah Kebangsann Dewan Beta. Soon after five year there, he got an opportunity to advance his study Diploma Level at University Malaysia Pahang. He completed his studies there in Electrical Engineering course at 2007. Then he has been accepted to continue study also in University Malaysia Pahang and currently (2009) a Bachelor's student in Electrical Engineering (Power System), faculty of Electrical and Electronics Engineering, University Malaysia Pahang. His research fields are power electronics and power system. He is a student member of the IEM of Malaysia.