DEVELOPMENT OF AUTO RE-CLOSER EARTH LEAKAGE CIRCUIT BREAKER FOR DOMESTIC APPLIANCES

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JUDUL: **DEVELOPMENT OF AUTO RE-CLOSER EARTH LEAKAGE CIRCUIT BREAKER FOR DOMESTIC APPLIANCES**

SESI PENGAJIAN: **2007/2008**

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This thesis is submitted as partial fulfillment of the requirements for the award of the Bachelor of Electrical Engineering (Power System)

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NOVEMBER, 2009

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Date : 6 NOVEMBER 2009

Specially dedicated to my beloved family, sibling, supervisor and those people who giving me constant source of support and encouragement

ACKNOWLEDGEMENT

First and foremost, I am very grateful to the almighty ALLAH S.W.T for letting me to finish my Final Year Project.

Here, I wish to express my sincere appreciation to my supervisor, En. Mohd Redzuan bin Ahmad for encouragement, guidance, suggestions, critics and friendship throughout finishing this project.

I also thanked to En.Fadhil bin Abbas, En.Rosmadi bin Abdullah and all of the lecturer in FKEE for their accommodation, suggestion and opinion during the project progress in university. In particular, I would like to thank also to thank, staff and technicians, for their cooperation, indirect or directly contribution in finishing my project.

Most importantly, special thank also to my family for their external support when I told them I wanted to continue my education and especially friends for encouraging me done by research. Without their support the ideas could not have been realized.

ABSTRACT

System protection is the important requirement in electrical power system. The using of protection system can avoid and prevent system from damaged. Electrical energy has caused dangers to human life and machine. Earth leakage circuit breaker (ELCB) is one from protection device that introduced to protect the system. This device is the brain of protection system that monitors input current from power line by it sensor Zero Current Transformer (ZCT), then sending the tripping signal to mechanical switch to disconnected system. ELCB is widely applied by consumer weather is for resident, factory, laboratory and also in power distribution. Because industrial operation requires protection of their Equipment from the lightning, short-circuit and also over-current, so the ELCB will serve the purpose as the protection of their system. This project will focused to improve the ability of current ELCB so that it have ability in identify fault, act accordingly, display the fault(permanent fault and temporary fault) and also re-close it back to normal condition.PIC will execute their instruction when different current from both of current transducer is exceed pre-determine value of sensitivity,100mA. In this project PIC microcontroller will control and operate solid state relay which replacing the application of current mechanical switch.

ABSTRAK

Sistem perlindungan adalah keperluan penting di dalam sistem kuasa elektrik.Penggunaan sistem perlindungan boleh mencegah dan melindungi sistem dari kerosakan.Tenaga elektrik telah menyebabkan bahaya kepada kehidupan manusia dan mesin.Pemutus litar bocor ke bumi(ELCB) adalah salah satu sistem perlindungan yang diperkenalkan untuk melindungi sistem. Peralatan ini adalah otak bagi sistem perlindungan dimana ia bertindak sebagai pemerhati arus masukan daripada talian kuasa oleh pengesan Zero Pengubah Tanpa Arus (ZCT),seterusnya menghantar isyarat pemutus kepada mekanikal suis untuk memutuskan litar. ELCB digunakan secara menyeluruh oleh pengguna sama ada untuk kediaman, kilang, makmal dan juga pembahagian kuasa. Oleh kerana operasi industri memerlukan perlindungan mesin mereka daripada kilat, litar pintas dan juga lebihan arus, maka ELCB ini akan digunakan bagi tujuan perlindungan kepada sistem mereka.Projek ini menumpukan kepada penambah baikan keupayaan ELCB sedia ada yang mana ELCB berupaya dalam mengenalpasti kesilapan,bertindak sepatutnya, menunjukkan kesilapan dan juga menyambung kembali litar ELCB kepada keadaan asal.PIC akan melaksanakan arahan apabila perbezaan arus antara dua alat pengesan arus melebihi nilai sensitiviti ELCB,100mA. Dalam projek ini,pengawal PIC akan mengawal dan menghidupkan relay keadaan tetap(SSR) yang mana menggantikan penggunaan suis mekanikal yang sedia ada.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

AC	–	Alternate Current
ADC	–	Analog to Digital Converter
DC	–	Direct Current
I_i	–	Input Current
Io	–	Output Current
LED	–	Light Emitting Diode
LCD	–	Liquid Crystal Display
PIC	–	Programmable Intelligent Computer
SSR	–	Solid State Relay
V	–	Voltage
V_{in}	–	Input Voltage
V_o	–	Output Voltage
ZCT	–	Zero phase Current Transformer
Ω	–	Ohm

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1 Project Background

The idea of the project is refer on the problems and weakness of ELCB. Nowadays, ELCB that available in market is controlled manually and cannot turn ON automatically. Beside that, ELCB today cannot differentiate between permanent fault and temporary fault. According from that problem, it bring the problem to consumer who were not at home and do not understand the danger of permanent fault if the kind of fault happen.

This project s focused in the development and new design a unit of auto re-closer earth leakage circuit breaker (AR-ELCB).The main purpose of this project is more to upgrade the ability of ELCB. Auto re-closer ELCB can differentiate and act differently with different type of fault. The concept is easy to understand which if fault happen, ELCB will trip automatically and disconnect the circuit. If temporary fault lie lighting happen, ELCB will close back automatically and circuit is connected back in interval time that has been set. If permanent fault like electrical, electronic device or short circuit is detected, ELCB will eternally trip and permanent faulty lamp/buzzer will function as alert to consumer. When fault root cause is removed, the consumer need to manually switch ON the ELCB and that case is just especially for permanent fault.

In this project, I have planned to use the programmable interfacing controller (PIC) as control element and can make system more efficient and accurate. To get new auto re-closer ELCB, we must combined control element and old ELCB. In this combination, we must consider all power and source value for voltage and currents of each device and for it, we must know to design the new additional circuit to fix the voltage and currents which the value is suitable to interface with control element and could work together.

1.2 Objective

The objectives of this project are:

i. To develop the auto re-closer earth leakage circuit breaker(AR-ELCB)
ii. To improve the ability of earth leakage circuit breaker(ELCB) unit
iii. To notify the type of fault whether temporary or permanent fault

1.3 Scope of Project

The scopes of this project are:

i. Studied and explored about all the function of ELCB
ii. This project focused to modify and improve the ability of ELCB to assign whether permanent or temporary fault.
iii. Different output on the AR-ELCB device depend on the fault detected
iv. Development programmable interfacing controller (PIC) application as control element of circuit

1.4. Literature Review

There are two types of ELCB, the voltage operated device and the differential current operated device. For the convenience of this article only (and at the risk of causing even more confusion) I will refer to these as vELCB and iELCB. vELCBs were first introduced about sixty years ago and iELCBs were first introduced about forty years ago.

vELCB is a voltage operated circuit breaker, the device will function when the Current passes through the ELCB. vELCB contains relay loop which it being connected to the metallic load body at one end and it is connected to ground wire at the other end.If the voltage of the load body is rise which could cause the difference between earth and load body voltage, the danger of electric shock will occur. This voltage difference will produce an electric current from the load metallic body passes the relay loop and to earth. When voltage on the load metallic body raised to the danger level which exceed to 50Volt, the flowing current through relay loop could move the relay contact by disconnecting the supply current to avoid from any danger electric shock.

iELCB is current operated circuit breaker. The device will function with when the Current passes through ELCB. This current admitted to current transform device and on the load. Current from the load also admitted again to transform device. In normal state, total current applied to load is equal with total current out of the load. Because of the balance of in and out of current, it does not affect the current transform device. If there is any earth current leakage caused by earth damage, then the in and out current.[1]

In Europe, where electromechanical ELCB’s are used almost exclusively, the question of reliability of installed ELCB’s has become a subject of major concern and attention. The popular hype regarding perceived reliability of electronic components was not sufficient to prevent the major South African manufacturer, some five years ago

from changing their entire ELCB range from electromechanical to electronic technology ELCB's. The improvements in reliability that resulted from this decision are complemented by their freedom from safety performance limitations often found in lower specification electromechanical earth leakage circuit breakers. The pioneering South African developments in sensitive earth leakage protection originally used magnetic amplifier technologies to reach the required sensitive residual current tripping levels necessary for shock hazard protection in human beings. Respite the lack of maturity in electronic components during those early days, a move was made away from magnetic amplifiers to solid state electronic technology in order to overcome the identified problems of noise, size and cost. [2]

This paper traced the development of earth leakage circuit breaker and indicated the very real need for such protection against both shock hazard and fire risk. Largely influenced by the highly sensational issues of the effects of electricity on the human body. Most publicity and media coverage relating to earth circuit breaker has, quite naturally concentrated on shock hazard protection and the related life saving capabilities of the device. it is only, that understanding prevails in regard to the dramatic reduction of potential fire hazard in premises that have been fitted with sensitive earth leakage protection.[3]

Most problems in discrete relay schemes is that of contact racing and timing tolerance on pick-up and drop-off of the various relay elements within the schemes. To overcome this problem, it often necessary to add additional element, or very selective in the type relay used. Beside that, lightning never strike the same place twice. This means that in any one auto-reclose sequence several different types of fault could be present [4]

1.5. Report outline

Chapter 1 will explain about the early process before begin that project. It include the project background, objectives, scope of project and literature review. Project background is about ELCB today altogether with their problem. Objectives and scope of project is target to resolve that problem. Then, before we start that project, literature review about that device is most important to get more data and information about that device.

Chapter 2 will explain detail definition of ELCB. From that, we can find all information about that device. Beside that, we can see two type of ELCB available in market which has different characteristic and method operation. According from analytical about that device, this chapter is include the problem of ELCB with more detail.

From chapter 3,we will see the construction inside the ELCB device. It include component of Zero current transducer, black box, mechanical switch, reset button and high level resistor. From combination of that component, it will integrated together to perform ELCB operation.

Chapter 4 will explain about the development auto re-closer ELCB. It include project flow how to start that project. Other planning is proposed design circuit to replaced old circuit of ELCB. After that, we can see the flow chart how that new device is operate and how PIC application of PIC make the system more reliable and effective.

At chapter 5, it will explain about expected result and conclusion about early planning along produce the new device ELCB. From expected result, we can conclude whether the project will be successful or not.

Finally at end of chapter 6, this chapter will explain about costing and commercialization. We can estimate the cost for design one unit of auto re-closer earth leakage circuit breaker

CHAPTER 2

EARTH LEAKAGE CIRCUIT BREAKER

2.1 Introduction

This chapter describe about nowadays earth leakage circuit breaker that used in 240Vac for domestic appliances. Before start any project about that device, it is important to analyze and understand the basic of the ELCB device and know how the device work actually. To achieve the objective for this chapter, the research of earth leakage circuit breaker is done by exploring the 240Vac ELCB that normally used for domestic appliances.

The objectives of this chapter are:

i. To know the system of basic Earth Leakage Circuit Breaker
ii. To understand how the device work
iii. To analyze the problem of ELCB

2.2. Earth Leakage Circuit Breaker (ELCB) Device

An Earth Leakage Breaker (ELCB) is devices that detect leakage current and protect consumer from electric shock if leakage current occurred. the device is used to

directly detect current leaking to earth from and installation and cut the power. For example, if any fault happens, ELCB will detect and trip, so the electrical supply is disconnected.

ELCB must fitted in main switchboard in every home to prevent electric accident and this is very effective way. If we using electric water heater equipment, additional ELCB need to be specially fixed in order to monitor the heater water. This precaution is god in ensuring your house safety.

There are two type of ELCB mostly used and available in market. That type is voltage earth leakage circuit breaker (vELCB) and current earth leakage circuit breaker. Few years ago, the was vELCB is mostly used, but its utilization was currently had been abolished because it was less effective. Then, iELCB is introduced to replaced vELCB immediately. The iELCB is more sensitive to any damaged in assembly and electrical appliances at domestic

2.2.1 Voltage Earth Leakage Circuit Breaker (vELCB)

vELCB is a voltage operated circuit breaker, the device will function when the current passes through the ELCB. The principle of operation of the vELCB is as follows. Under normal conditions the closed contacts of the vELCB feed the supply current to the load. The load is protected by a metal frame, such as in an electric cooker. The vELCB also has a relay coil, one end of which is connected to the metal frame and one end connected directly to ground. A shock risk will arise if a breakdown in the insulation occurs in the load which causes the metal frame to rise to a voltage above earth. A resultant current will flow from the metalwork through the relay coil to earth and when the frame voltage reaches a dangerous level, e.g. 50 volts, the current flowing through

the relay coil will be sufficient to activate the relay thereby causing opening of the supply contacts and removal of the shock risk.

As can be seen from the above description, this type of ELCB is essentially a voltage sensing device intended to detect dangerous touch voltages. The level of shock protection provided by the vELCB was somewhat limited as these devices would not provide shock protection in the event of direct contact with a live part. An additional problem with the vELCB was its tendency to be tripped by earth currents originating in other installation

2.2.2 Current Earth Leakage Circuit Breaker (iELCB)

The iELCB was introduced in the late 1950's. It operates on the following principle. Under normal conditions the closed contacts of the iELCB feed the supply current to the load. The load conductors are passed through a current transformer (CT), a doughnut shaped device. The load conductors act as primary windings of the transformer. The CT is fitted with a secondary winding. Under normal conditions, the total current flowing from the supply to the load will be the same as the total current flowing back to the supply from the load. As the current in both directions is equal but opposite, it has no effect on the CT. However, if some current flows to earth after the iELCB, possibly due to an earth fault, the current flowing to the load and from the load will be different. This differential current will cause a resultant output from the CT. This output is detected and if above a predetermined safe level, it will cause the iELCB to trip and disconnect the supply from the load.

2.3 Problem of ELCB

Earth leakage circuit breaker is one type of device used especially as a protection device. The main function of ELCB is to cut off the electrical supply when the fault is detected. But, the disadvantage for ELCB device nowadays, it cannot turn on itself and back to normally condition if fault occurred. To connect the electrical supply back, the consumer must turn on manually. But, if any person not in home, the electrical supply is remain in turn off condition.

Beside that, ELCB cannot recognize fault whether temporary fault or permanent fault. The principles of operation just to trip and disconnect circuit, but it actually not recognize the type of fault. The ELCB will trip depend on temporary fault only and for permanent fault problem, there is no output is created to ensuring the consumer safety.

The device is also cannot act differentially for these two types of fault. ELCB device just detect and trip depend on temporary fault only. If permanent fault happen, the consumer know the root of that problem and can see the reaction from ELCB. But in permanent fault case, there is no output showed at ELCB, so it can create the danger like electrical shock and other problem to consumer.

2.4 Electrical Fault

A fault is any abnormal situation in an electrical system in which the electrical current may or may not flow through the intended parts. Also equipment failure attributable to some defect in a circuit (loose connection or insulation failure or short circuit etc.). Types of faults in a distribution network circuit are:

i) Over-load

ii) Faults on electrical equipments

iii) Transmission lines faults

Over-load faults are caused by the unexpected increasing of loads. Faults on electrical equipments are caused by lightning, insulator breakage, Product design which is out of specification and Improper installations of equipments.

Most faults on transmission lines of 100kV and higher are caused by lightning, which results in the flash over of insulators. Transmission lines faults are caused by, lightning, storm, fallen trees, Snow. One of the temporary fault, is a fault lightning . Where example of permanent fault is faults on electrical equipment.

2.5 ELCB Features

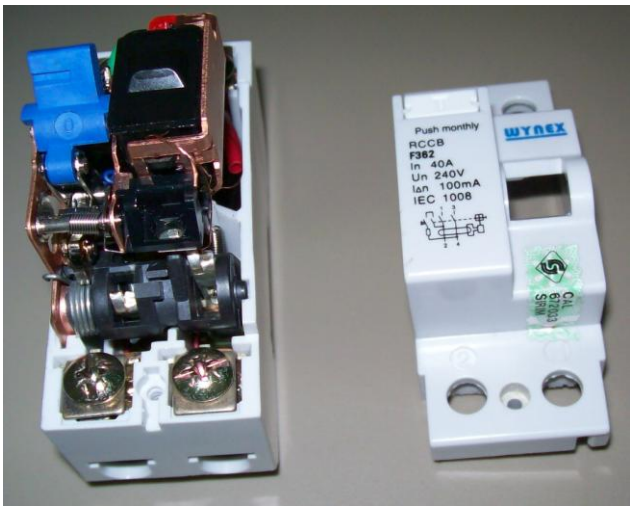


Figure 2.1: Home ELCB/RCCB with housing

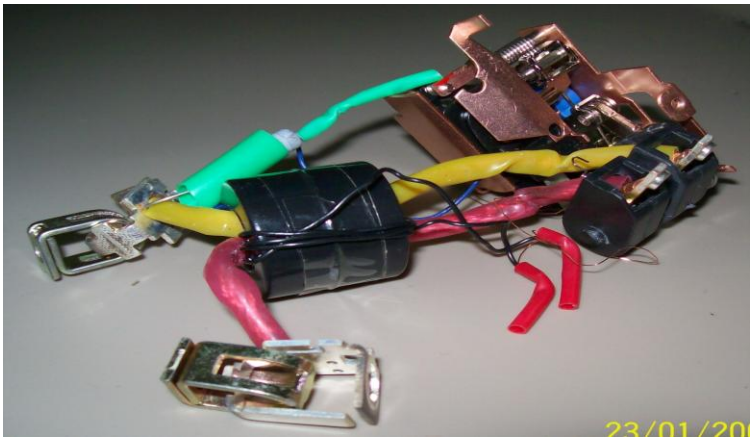


Figure 2.2: ELCB Structure

The figure 3.1 shows the ELCB home with the housing. figure 3.2 show the basic construction inside ELCB.After separate that device,we can see all component inside ELCB include ZCT,blackbox,result button.Three cable connection cable are labeled with red,yellow and green to show the connection life,neutral and earth inside ELCB.

2.6 ELCB Design

The earth leakage circuit breaker consist the black box (coil),mechanical switch, zero current transducer, high level resistor and reset button. Every component has different operation and it combined in one circuit to create ELCB device. With supply from TNB 240Vac, those devices flow through every component and lastly go to load.

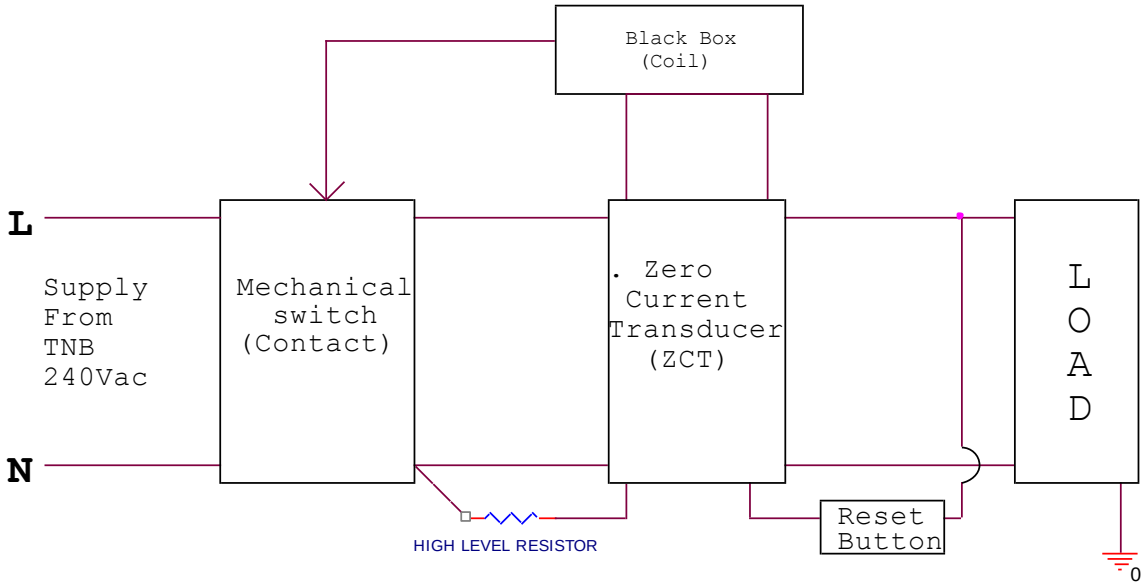


Figure 2.3: Earth Leakage Circuit Breaker design

2.6.1. Zero Transducer Current (ZCT)

Zero current transformers are used to detect unbalance current and send signal to black box. In unbalance current condition, induced current is produced and it flow from ZCT to other device in system.

2.6.2. Black Box

Black box in ELCB consist a coil. The function of black box is received the signal (induced current) from zero current transducer. The coil in black box will activate the mechanical switch after received the minimum current level 100mA from ZCT.

2.6.3. Mechanical switch

Mechanical switch act as contact of black box and it used especially to cut off the power and disconnect circuit immediately. Mechanical switch is directly connect with coil which if coil is activated, it will removed the mechanical switch.

2.6.4. Reset Button

The main function of the reset button is to reset back the device to initial condition. It is also used as a point to detect whether the device in good condition or damage.

2.6.5. High Level Resistor

The high level resistor is used to limit the current flowing through its line when reset button is pushed. When unbalance current happen, that device will fully function to control the flow of current.

2.7 Operation of ELCB

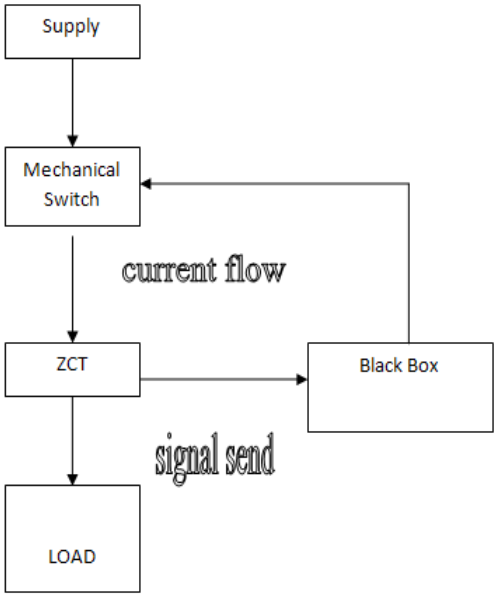


Figure 2.4: Earth Leakage Circuit Breaker Operation Flow

This flow showed the operation of ELCB during fault happen. In normal condition, mechanical switch is already closed and give permission to supply through ELCB and directly go to load. When the fault occurred, the unbalance phenomena are detected by ZCT in ELCB. So the induced current will happened at ZCT. Induced current that reached the min value level will send to black box and automatically will activate the coil in black box. Then, when the coil is activated, it will remove the contact of mechanical switch to trigger and cut off the supply instantaneously. If the condition back to normal and has no fault detected, reset button is pushed to connect the electrical flow.

2.8 Summary

ELCB is an important device in electrical system and it available with two type. iELCB and vELCB is the kind of type but both device is used for protection device for electrical equipment and protect consumer from danger and hazard. Both device has different operation to detect the current leakage and different characteristic. The main purpose of ELCB is to cut-off the power when fault occurred. To make that ELCB device more effective, ELCB must be able to act differentially following the kind of faulty, so it can improve ELCB ability.

CHAPTER 3

CONTROL ELEMENT CIRCUIT

3.1 Introduction

Control element circuit is the main controller for overall of the system. In this project, it focused on using PIC18F4550 microcontroller as brain element for our system. Earlier project, there is 3 type of PIC is considered to used in our project as PIC18F2255,PIC18F4455 and PIC 18F4550.But in final decision,PIC18F4550 is choosed based on their feature and it mostly used in many project before. PIC18F4550 microcontrollers use flash technology to allow rapid erasing and reprogramming to speed program debugging. PIC18F4550 offer twelve different oscillator options, allowing users a wide range of choices in developing application hardware. With the click of the mouse in the programming software, the flash PIC micro MCU can be instantly erased and then reprogrammed again and again. PIC18F4550 have large amounts of RAM memory for buffering and Enhanced Flash program memory thus make it ideal for embedded control and monitoring applications that require periodic connection with a (legacy free) personal computer via USB for data upload or download and firmware updates. Programming the PIC18F4550 is done by using C-language. Besides, Microcode Studio software has been used to write the programming coding of the PIC. Finally compile this type of programming language, the use of PIC Basic Compiler have been used.

3.2 PIC Microcontroller Feature

PIC is a family of Harvard architecture microcontrollers made by Microchip Technology, derived from the PIC1640 originally developed by General Instrument's Microelectronics Division. The name PIC initially referred to "Programmable Interface Controller", but shortly thereafter was renamed "Programmable Intelligent Computer".

PICs are popular with developers and hobbyists alike due to their low cost, wide availability, large user base, extensive collection of application notes, availability of low cost or free development tools, and serial programming (and reprogramming with flash memory) capability.

PIC microcontrollers are frequently used in automatically controlled products and devices, such as automobile engine control systems, remote controls, office machines, appliances, power tools, and toys. By reducing the size, cost, and power consumption compared to a design using a separate microprocessor, memory, and input/output devices, microcontrollers make it economical to electronically control many more electrical and mechanical devices.

3.2.1 PIC 18F4550

In this project, the PIC18F4550 is choose to used as brain for our system, thus it can make system more reliable and beside high computational performance. This PIC is attached with 40 pin and every pin has different function. In this PIC, there are 4 type port available like port A, port B, port C and port D. Port A is design especially with ADC (analog digital converter). The function of ADC is to convert analog form to digital form. It actually used to interface with PIC which PIC can operate if they understand the information given in digital signal form. In PIC reader, PIC just can

assign the logic signal whether logic 0 (0Vdc) logic 1 (5Vdc). From the PIC port configuration, this port can be set whether be output or input depend on the user programming. To set the port, user must be decide early and make programming to choose whether used port as input or output, thus PIC can understand and can perform their instruction. Beside that, the crystal oscillator is used to generate the frequency (pulse form) to the PIC. the relationship oscillator and PIC showed if high value oscillator generate, PIC will execute the instruction more faster and in this project, oscillator 20MHz is used to generate the pulse form. The figure 3.1 and 3.2 show the two type of PIC18F4550 that usually used in other project. The number of pin is different and method installation for pin TQFP microcontroller are more difficult to compare with PDIP microcontroller.

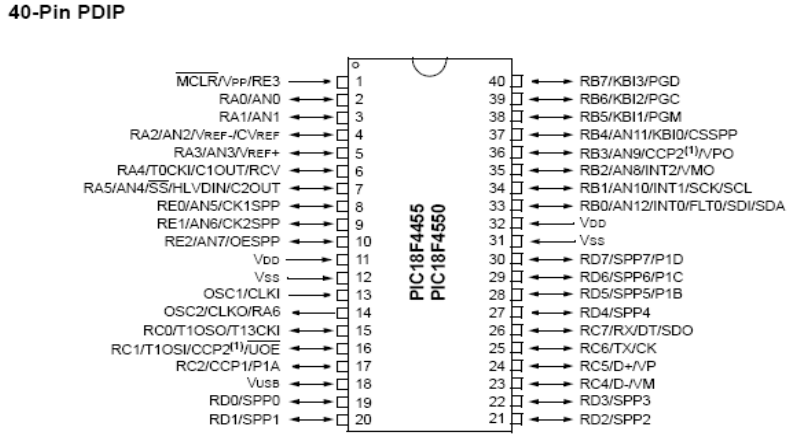


Figure 3.1: 40-Pin PDip Microcontroller

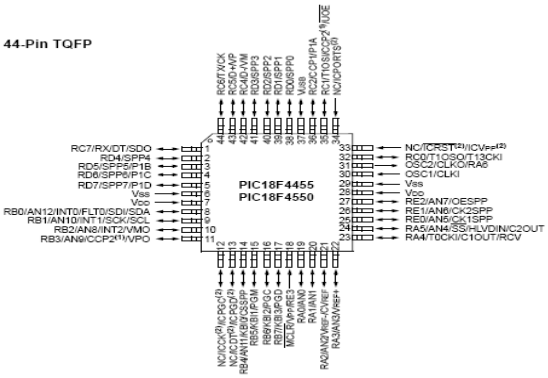


Figure 3.2: 44-Pin TQFP Microcontrollers

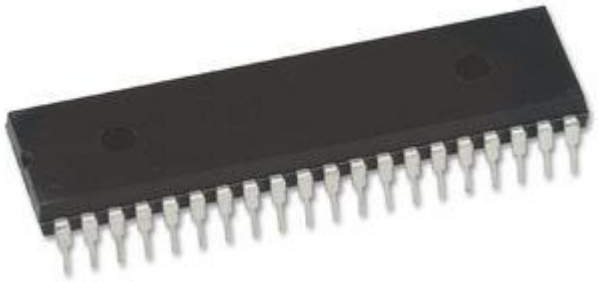


Figure 3.3: PIC18F4550

Below is the detail information about PIC 18F4550 features

- 8BIT FLASH MCU, 18F4550, DIP40
- Series:PIC18F
- Memory Size, Flash:32KB
- EEPROM Memory Size:256Byte
- RAM Memory Size:2048Byte
- No of I/O Lines:35
- No. of ADC Inputs:13
- No. of Timers:4
- No. of PWM Channels:5
- Clock Frequency:48MHz
- Interface Type: EUSART, I2C, SPI, SPP, USB
- Voltage, Supply Min:4.2V
- Voltage, Supply Max:5.5V
- Termination Type: Through Hole
- Case Style: DIP
- No. of Pins:40
- Operating Temperature Range:-40°C to +85°C
- Max Operating Temperature:85°C
- Min Temperature Operating:-40°C

- Base Number:18
- Bits, Number In Timer:16
- Bits, Number in ADC:10

Table 3.4: PIC18F4550 Features

Pin Name	Pin Number PDIP, SOIC	Pin Type	Buffer Type	Description
MCLR/VPP/RE3	1			Master Clear (input) or programming voltage (input).
MCLR		I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP		P		Programming voltage input.
RE3		I	ST	Digital input.
OSC1/CLKI	9			Oscillator crystal or external clock input.
OSC1		I	Analog	Oscillator crystal input or external clock source input.
CLKI		I	Analog	External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)
OSC2/CLKO/RA6	10			Oscillator crystal or clock output.
OSC2		O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO		O	—	In select modes, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6		I/O	TTL	General purpose I/O pin.
				PORTA is a bidirectional I/O port.
RA0/AN0	2			
RA0		I/O	TTL	Digital I/O.
AN0		I	Analog	Analog input 0.
RA1/AN1	3			
RA1		I/O	TTL	Digital I/O.
AN1		I	Analog	Analog input 1.
RA2/AN2/VREF-/CVREF	4			
RA2		I/O	TTL	Digital I/O.
AN2		I	Analog	Analog input 2.
VREF-		I	Analog	A/D reference voltage (low) input.
CVREF		O	Analog	Analog comparator reference output.
RA3/AN3/VREF+	5			
RA3		I/O	TTL	Digital I/O.
AN3		I	Analog	Analog input 3.
VREF+		I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/C1OUT/RCV	6			
RA4		I/O	ST	Digital I/O.
T0CKI		I	ST	Timer0 external clock input.
C1OUT		O	—	Comparator 1 output.
RCV		I	TTL	External USB transceiver RCV input.
RA5/AN4/SS/ HLVDIN/C2OUT	7			
RA5		I/O	TTL	Digital I/O.
AN4		I	Analog	Analog input 4.
SS		I	TTL	SPI slave select input.
HLVDIN		I	Analog	High/Low-Voltage Detect input.
C2OUT		O	—	Comparator 2 output.
RA6	—	—	—	See the OSC2/CLKO/RA6 pin.

3.2.2 Input and Output Port Used

According from circuit project, the output PIC is LCD and solid state relay and the PIC input is signal/data from op-amp LM358.Port A is set with input which port A is special pin with ADC attachment and it desired to send logic signal digital to PIC. The source of port A is come from op-amp which that device convert current to voltage and from there, it directly give signal to PIC whether logic low(0) or logic high(1).Meanwhile for port C, it set with output connected to LCD and solid state relay. If fault occurred, PIC will send signal to operate the solid state relay which it will trigger switch off and automatically disconnected the circuit. Then, at the same time PIC will send output signal to LCD to display what happen to user. Pin 13 and pin 14 is built in to directly connect with crystal oscillator 20 MHz. Beside that, pin 11 and 32 will connected together as Vcc that act as supply to on the PIC. Lastly, pin 12 and 31 is connected together to flow go directly to ground.

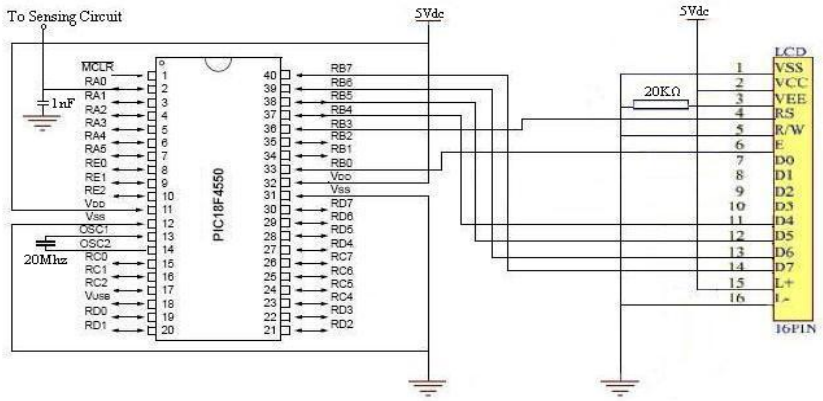


Figure 3.5: Interfacing LCD and PIC18F4550

3.2.3 Crystal Oscillator

A crystal oscillator is electronic circuit device that designed to generate electrical signal with accurate frequency. It work using mechanical resonance of a vibrating crystal of piezoelectric material to create an electrical signal. The using of precise frequency is to keep track of time, to provide a stable clock signal for digital integrated circuit, and to stabilize frequencies for radio transmitter and receivers. The most common type of piezoelectric resonator used is the quartz crystal, so oscillator circuits designed around them were called "crystal oscillators". A crystal has a natural frequency of resonance. Build in with quartz material, it can be shaped or cut to have a certain frequency. When a crystal of quartz is properly cut and mounted, it can be made to distort in an electric field by applying a voltage to an electrode near or on the crystal. This property is known as piezoelectricity. When the field is removed, the quartz will generate an electric field as it returns to its previous shape, and this can generate a voltage. The result is that a quartz crystal behaves like a circuit composed of an inductor, capacitor and resistor, with a precise resonant frequency. In this project, crystal oscillator 20 MHz is choosed to interface with PIC. The 20MHZ or more below than that is suitable to generate the precise frequency, so the PIC can operate better.

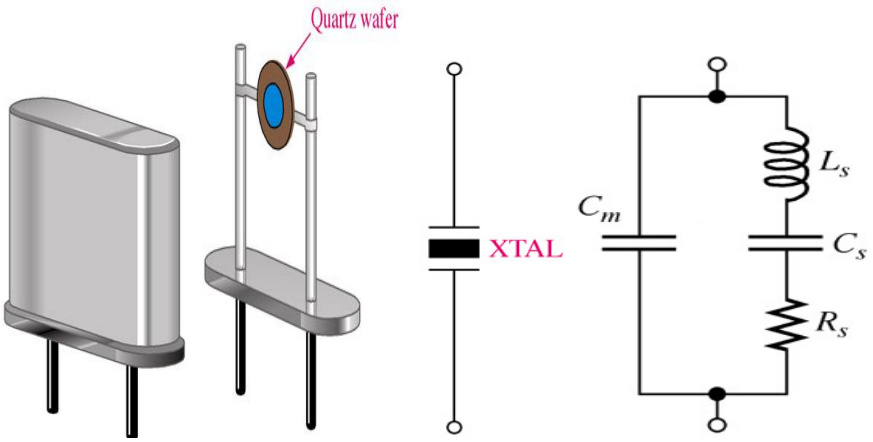


Figure 3.6: Crystal Oscillator Basic Instruction

3.3 Software and Hardware Implementation

This section will discuss about software which has been implemented in this project which are PicBasic Pro Compilers (MicroCode Studio) for programming PIC18F4550, OrCAD Capture CIS for designing the circuit and PicBasic Pro Compilers (Micro Code Studio) for the programming and also Cytron Programmer for writing the programming language into the PICF4550.

3.3.1 Microcode Studio

Microsoft studio is software that has been used to convert source file to HEX file code and act as assembler. To interface with PIC, all the source file must be converted to HEX file because PIC just can read and understand the hex file only.

MicroCode Studio is a powerful, visual Integrated Development Environment (IDE) with In Circuit Debugging (ICD) capability designed specifically for microEngineering Labs PICBasic PRO compiler. The code explorer allows you to automatically jump to include files, defines, constants, variables, aliases and modifiers, symbols and labels that are contained within your source code. It's easy to set up your compiler, assembler and programmer options or you can let MicroCode Studio do it for you with its built in autosearch feature. Compilation and assembler errors can easily be identified and corrected using the error results window. MicroCode Studio even comes with a serial communications window.

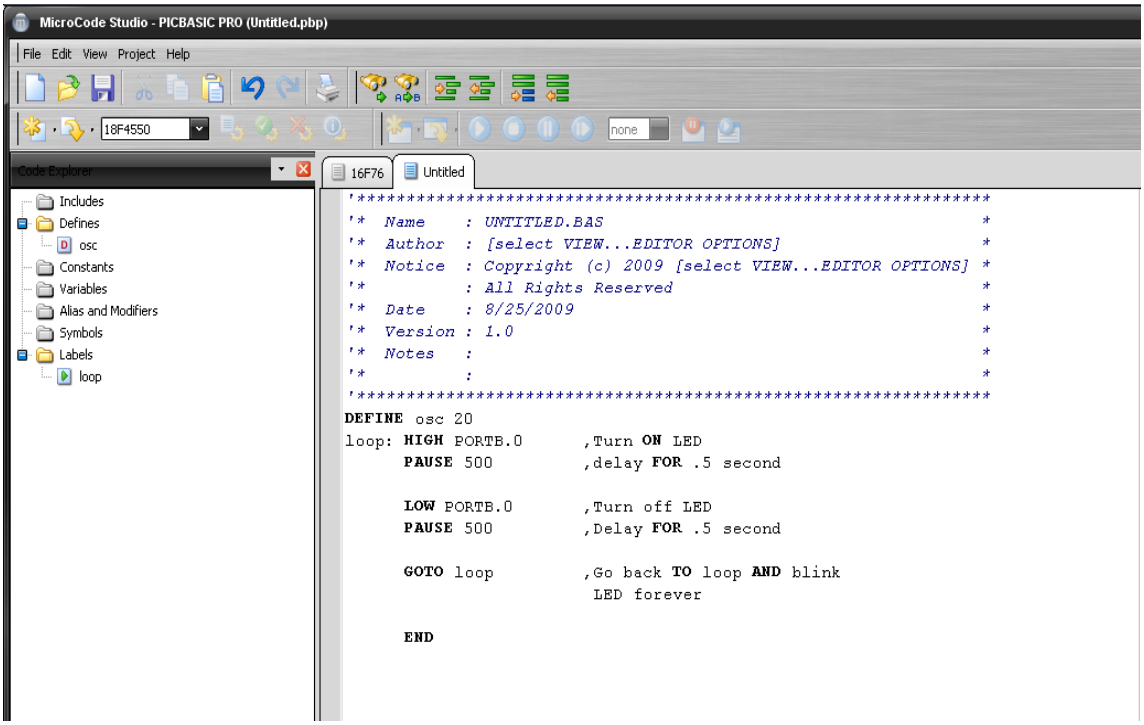


Figure 3.7: Basic program Written in Microcode Studio

3.3.2 CYTRON USB Programmer

In this project, UP00A CYTRON USB programmer is used and it attached with PIC programmer and winpic800.It fully functions as burner device and both of software and hardware act as medium to write the c- language in the PIC18F4550. CYTRON USB programmer UP00A provides an effective and low-cost solution in developing wide range of Microchip PIC microcontroller. That device has not using external supply, just directly connect to USB desktop PC or laptop and we can start write the program.

UP00A CYTRON USB programmer is equipped with 40 pin universal ZIF socket that provide a comfort and easy operation during plug in and plug out the chip. Besides ZIF socket, header pin for ICSP (In-Circuit Serial Programming) also provided.

This header pin can be used for in-circuit programming and to program the PIC with different socket which is not supported by the ZIF-socket. That device is comes with 28/40 pin and 8/18 pin and it used depend on the number of IC pins. Other than that, that device complete with LED that will showed the loading and ready signal. The ready signal will ON when the USB programmer is plugged in onto the USB computer. Then, during that data is burner to PIC, the loading lamp will ON and it will show how the device work completely.

Features:

- Designed for Intel based PC, DO NOT support AMD based system.
- Fast, reliable and low-cost.
- Do not support Window Vista
- Require USB port only.
- Can be used in desktop PC and laptop.
- ZIF socket and ICSP header pin are prepared.
- The programmer can be used for Windows Me/NT/2000/XP.
- 12F, 16F and 18F PIC MCU are supported.
- USB cable, user manual and programming software are provided.

Package Including:

- UP00A Programmer Unit
- USB Cable
- User Manual and Programming software in CD Rom
- 6 months warranty against factory defect only

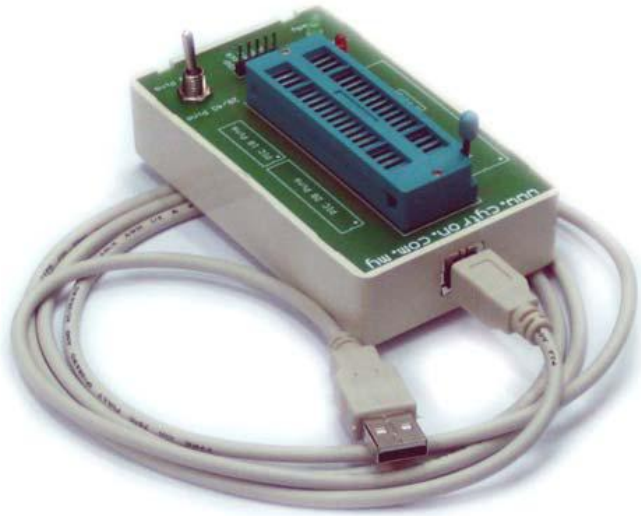
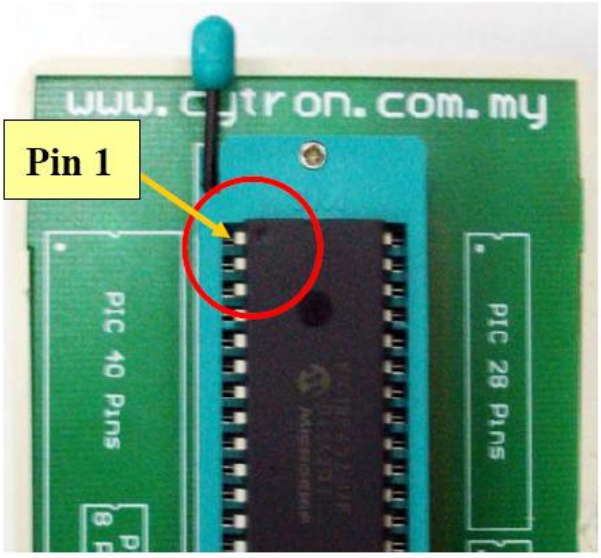


Figure 3.8: UP00A CYTRON USB programmer

3.3.2.1 Plugging The Microcontroller

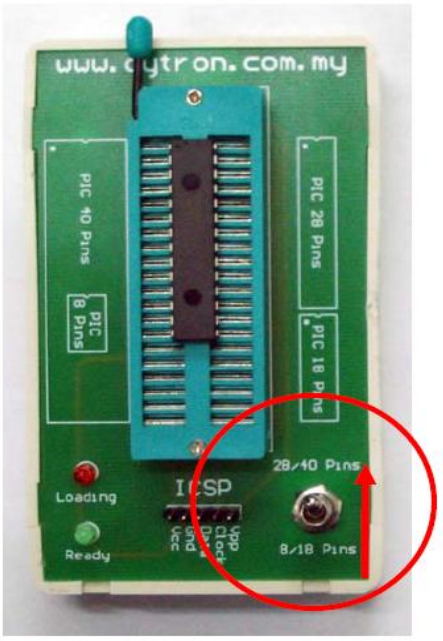
40-pin Microcontroller

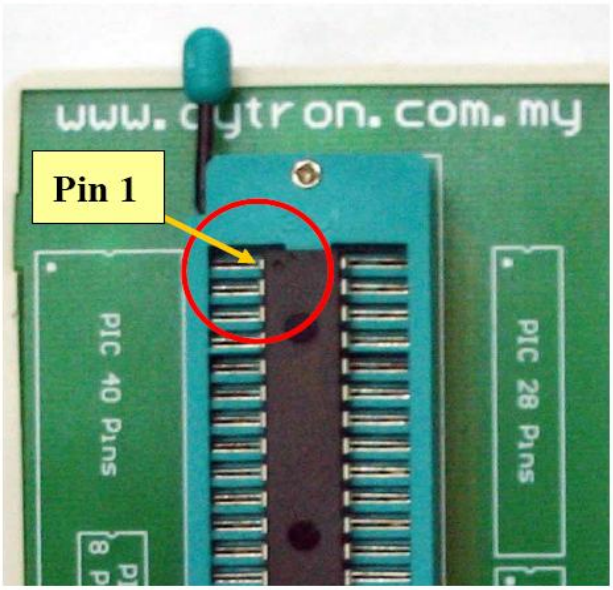
- Plug in the microcontroller at the socket (indicated on the board) and **push forward the toggle switch** as shown.



28-pin Microcontroller

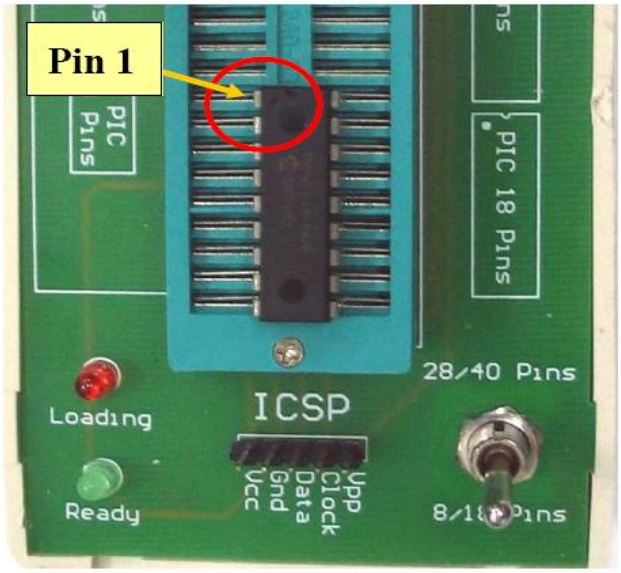
- Plug in the microcontroller at the upper portion of the socket (indicated on the board) and **push forward the toggle switch** as shown.





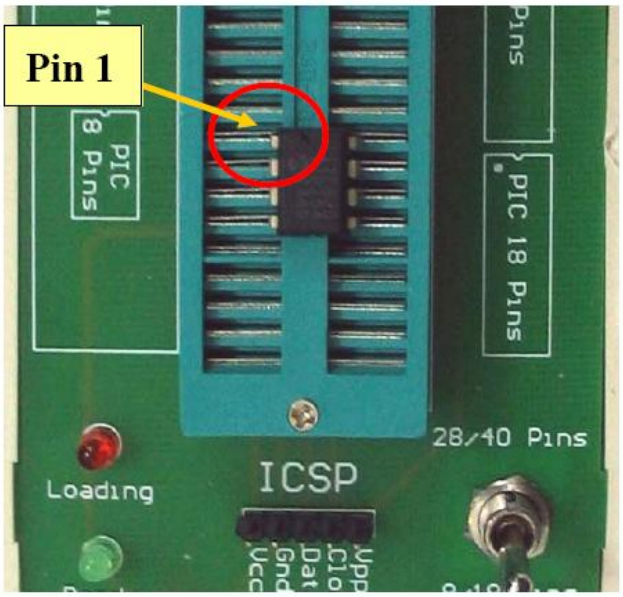
18-pin Microcontroller

- Plug in the microcontroller at the lower portion of the socket (indicated on the board) and **push backwards the toggle switch** as shown.



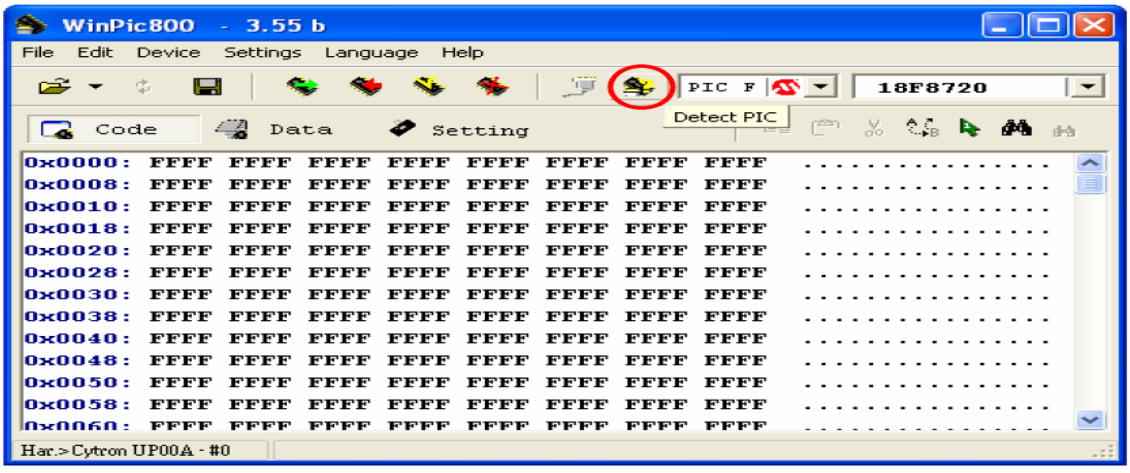
8-pin Microcontroller

- Plug in the microcontroller at the center portion of the socket (indicated on the board) and **push backwards the toggle switch** as shown.

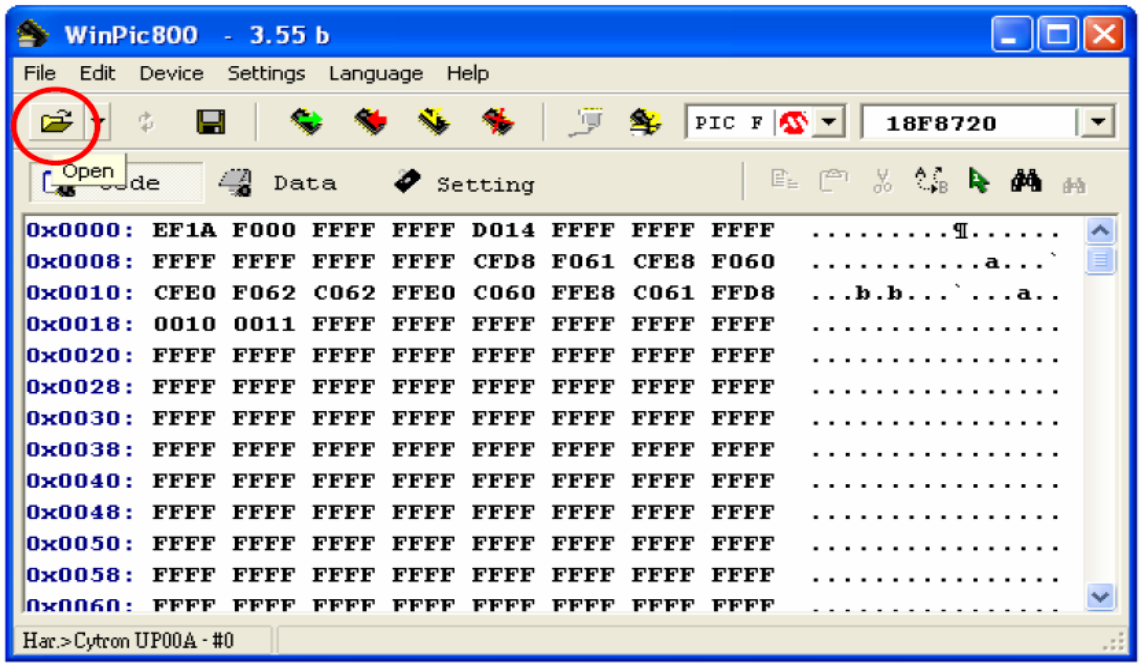


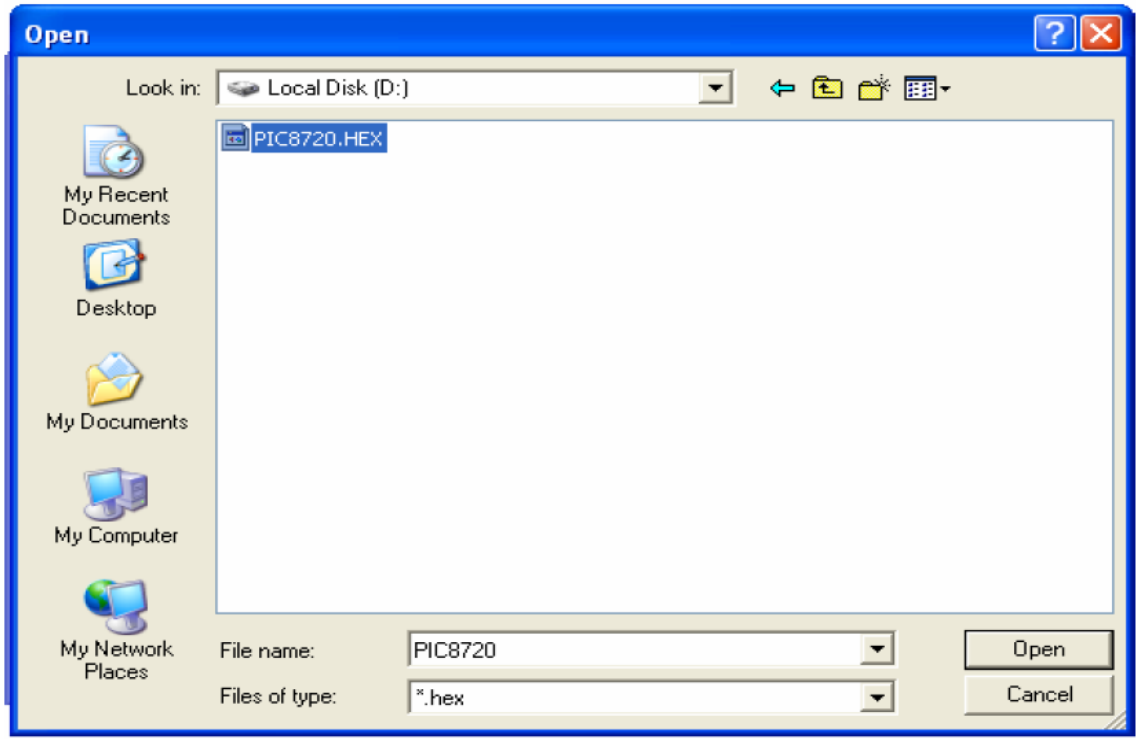
3.3.2.2 How to Program The PIC Microcontroller

1. Now WinPic800 is ready to program the PIC. This programmer is able to detect the PIC. By clicking the icon shown, the programmer will detect the type of PIC on the programmer.

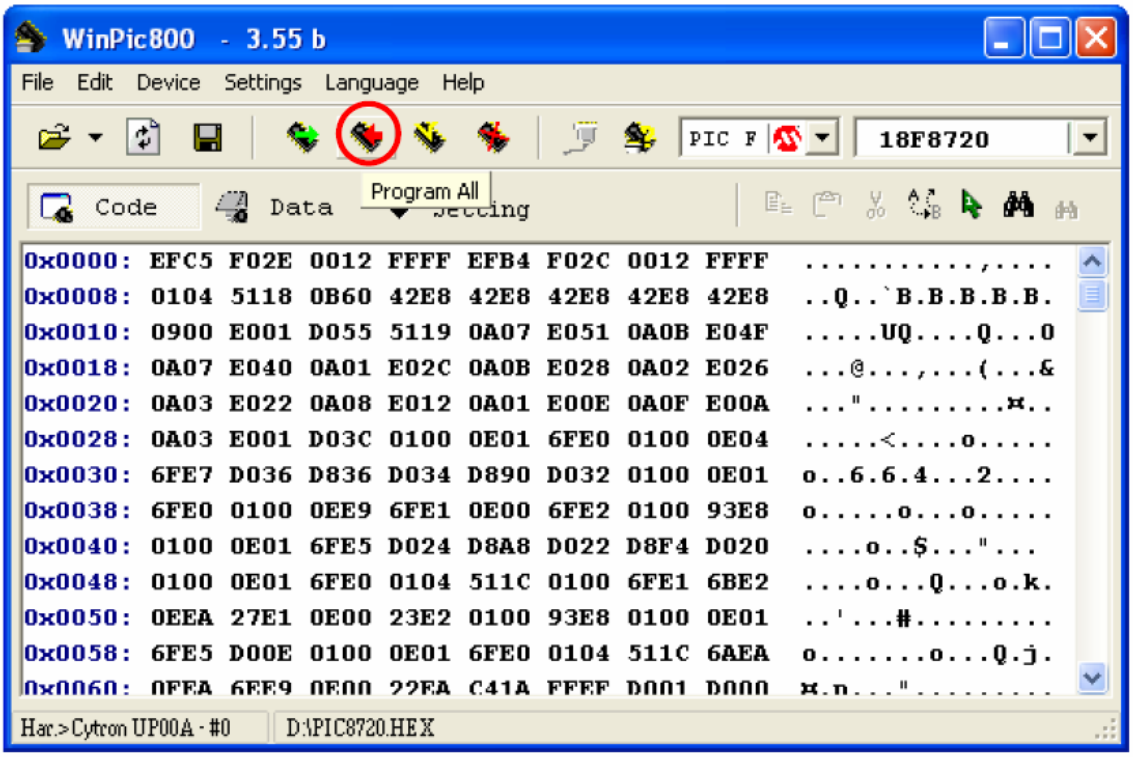


2. To write Hex code to PIC we must first open the hex file. By clicking the icon shown, a browse window will appear, open the hex file by clicking the file.

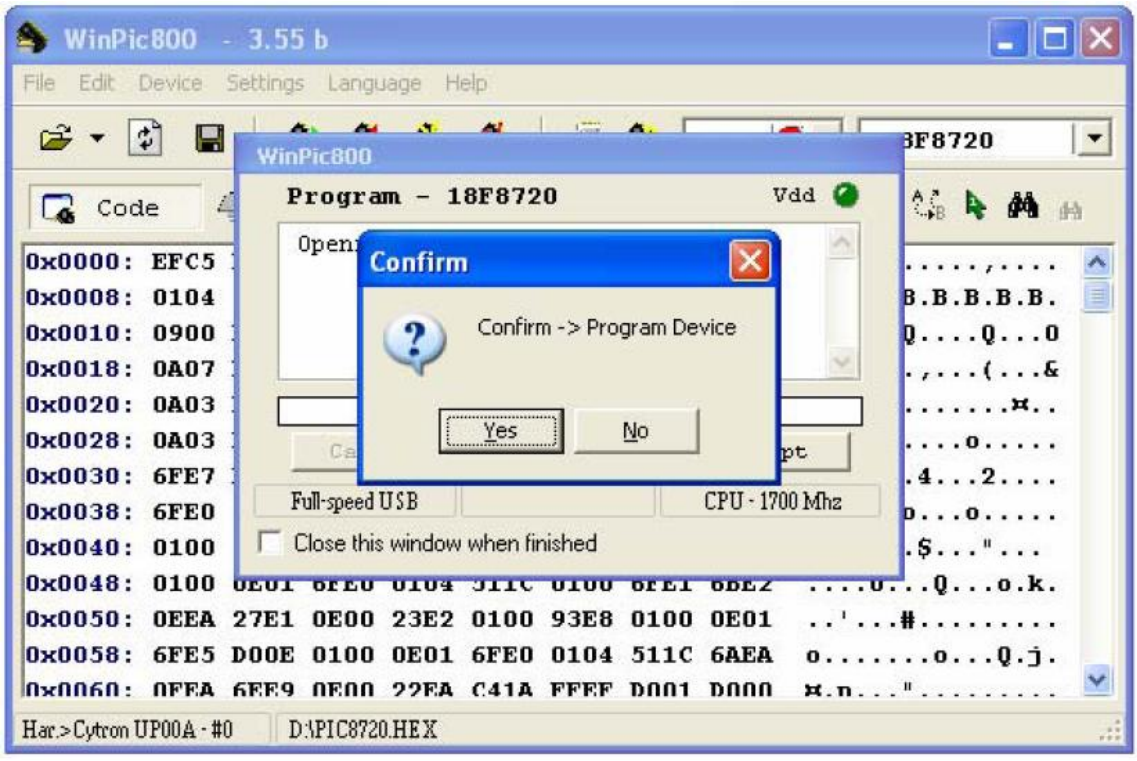


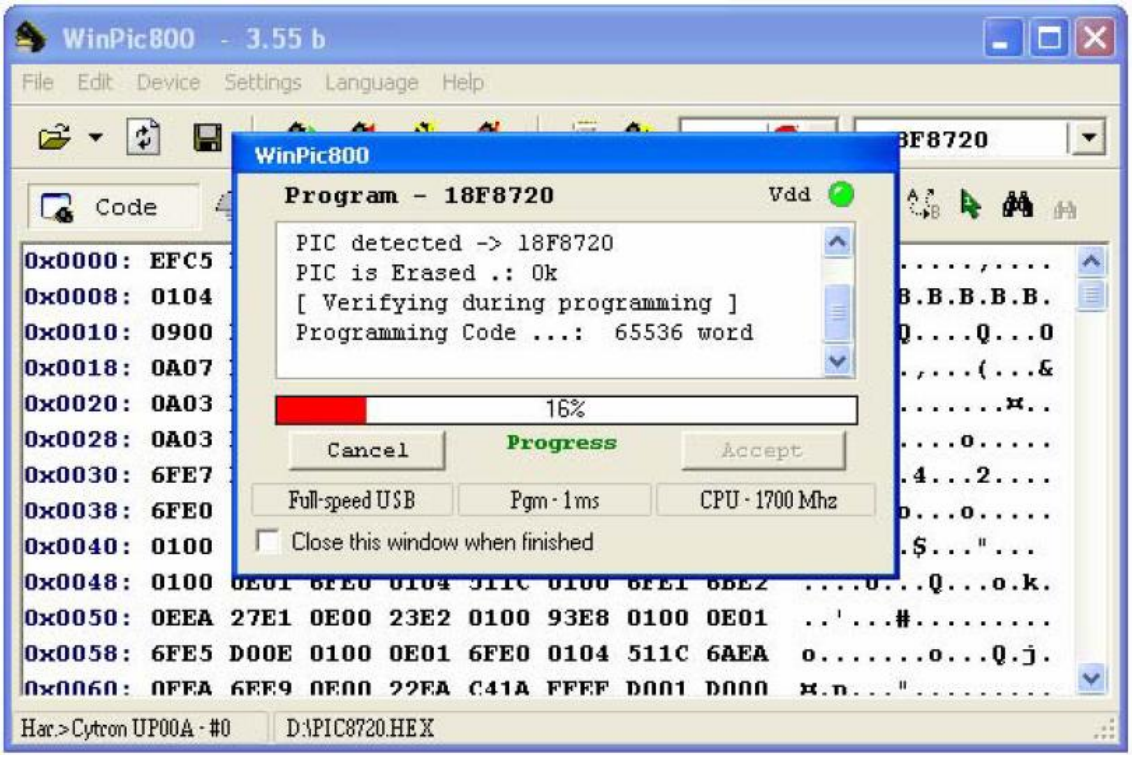


2. Program the file to PIC by clicking the icon shown.

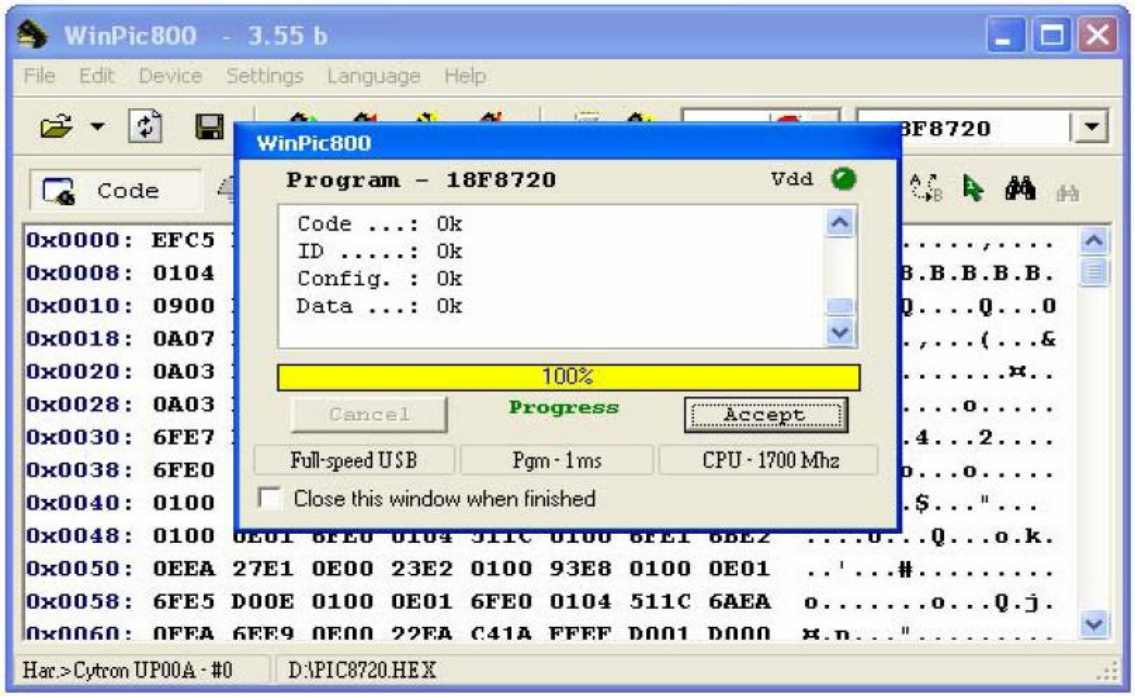


4. A confirmation window will appear, click *Yes* to proceed programming PIC.


WinPic800 - 3.55 b
File Edit Device Settings Language Help
Code
WinPic800
Program - 18F8720
Vdd
Confirm
Confirm -> Program Device
Yes
No
Full-speed USB
CPU - 1700 Mhz
Close this window when finished
0x0000: EFC5
0x0008: 0104
0x0010: 0900
0x0018: 0A07
0x0020: 0A03
0x0028: 0A03
0x0030: 6FE7
0x0038: 6FE0
0x0040: 0100
0x0048: 0100
0x0050: 0EEA 27E1 0E00 23E2 0100 93E8 0100 0E01
0x0058: 6FE5 D00E 0100 0E01 6FE0 0104 511C 6AEA
Har.>Cytron UP00A - #0
D:\PIC8720.HEX


WinPic800 - 3.55 b
File Edit Device Settings Language Help
Code
WinPic800
Program - 18F8720
Vdd
PIC detected -> 18F8720
PIC is Erased .: Ok
[Verifying during programming]
Programming Code ...: 65536 word
16%
Cancel
Progress
Accept
Full-speed USB
Pgm - 1ms
CPU - 1700 Mhz
Close this window when finished
0x0000: EFC5
0x0008: 0104
0x0010: 0900
0x0018: 0A07
0x0020: 0A03
0x0028: 0A03
0x0030: 6FE7
0x0038: 6FE0
0x0040: 0100
0x0048: 0100
0x0050: 0EEA 27E1 0E00 23E2 0100 93E8 0100 0E01
0x0058: 6FE5 D00E 0100 0E01 6FE0 0104 511C 6AEA
Har.>Cytron UP00A - #0
D:\PIC8720.HEX

5. When it is completed, the window will show the status. Click *Accept* and the PIC is ready to be plug out.



6. To disconnect UP00A, simply plug the USB out. No extra configuration or setting needed. Same applied when plug-in for the 2nd time, installation of driver is not required.

3.33 PIC Driver Circuit Hardware

At this part, it more focused on control element. The main component that control our system is PIC microcontroller. In this circuit there are consisted of oscillator 20MHz, Capacitor to reduced ripple for ADC, Connector to LCD and also output relay and also input ADC. This driver circuit has fewer components than the actual PIC driver circuit. It has been test that by reducing the capacitor in the circuit, there is not much changing in the operation of the circuit. Because the 5Volt input voltage that have been

supply to the driver circuit is already stable, and there is no reverse current from the Solid State Relay. So by using this driver circuit, the space and troubleshooting is easier to be done.

3.4 Programming Flowchart

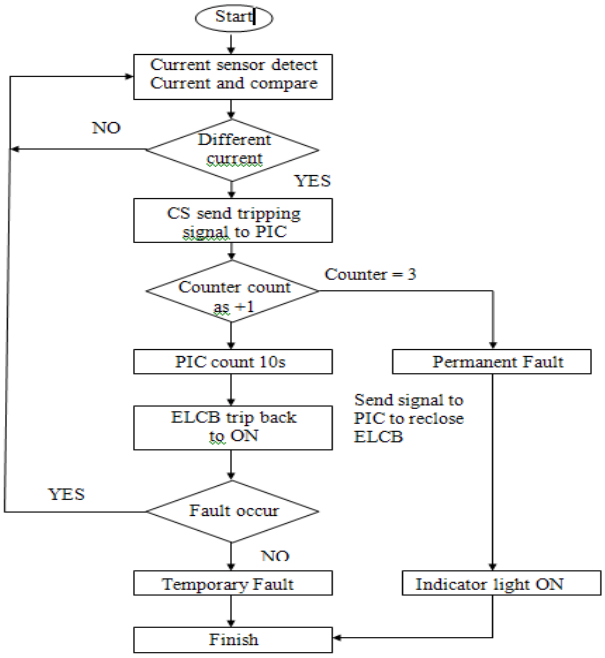


Figure 3.9: Flow of Programming Software

From the figure, when a fault occur current sensor will sense the imbalance current and then it will induced a signal current. This signal then is send to PIC microcontroller via sensing circuit.PIC controller will calculate the differential value of current between two of current sensor and if differential exist, it show fault exist and assigned.PIC will send signal to trip ELCB. At this moment the counter in the PIC will start count as 1. After 10 second, the ELCB will automatically switch back to normal condition. If there is no fault detect after the ELCB is turn on the LCD will display temporary fault and the ELCB will stay connected until next fault occurred and the

counter will be reset. Meanwhile if there is fault occurred instantly after the ELCB is turning back to on, the current sensor will detect the imbalance current and then will send back the signal to PIC. The ELCB then will turn on back after being trip. At this time PIC counter will count as 2, this process will be cycle until the counter reach 3. After PIC counter reach 3, PIC microcontroller will identify the fault as permanent fault such like short circuit and over-current. At the end, ELCB is permanently tripped and to turn on back the circuit, someone should manually turn on itself.

3.5 Summary

From this chapter, we are able to understand more about PIC basic configuration and their development. The advantage using PIC are the capability to interface directly with other device such as LCD, solid state relay are more reliable. Beside of that, PIC programming is much more simpler compared to other microcontroller. Based on pin configuration, there are four port in PIC that freely to used either input or output. Then from this chapter, we can learn much more about microcode studio that has been used to write programming in HEX file. Then for the next step, we can learn the using of CYTRON USB programmer as a device to transfer HEX file programming to PIC18F4550.From our observation, PIC can make system more reliable, faster and easier to handle.

CHAPTER 4

DEVELOPMENT OF AUTO-RECLOSER EARTH LEAKAGE CIRCUIT BREAKER

4.1 Introduction

This chapter explains our process to develop auto re-closer earth leakage circuit breaker include project flow, circuit design, hardware operation process and software implementation. This chapter also explains about designing the basic PIC circuit, LCD, current sensor circuit, interfacing PIC to circuit breaker, PIC programming.

This chapter will explain detail early process to design new auto re-closer earth leakage circuit breaker until last stage that connected our device and PIC. Beside that, this chapter also explains our component that has been used in this project and their advantage. Thus, to design effective ELCB, several changed has been made so that the size and the cost are acceptable for commercial purpose.

4.2 Project Flow

This project starts with study the basic design of an ELCB. This is done by explore and open a unit of ELCB rating 40A with sensitivity 100mA.From there, it showed our component that involve to build ELCB and how their function. The next stage is to think how to renovate in order to change from mechanical switching to

electrical switching. Next is to identify where the suitable component to connect with PIC microcontroller. After that process, new circuit of new auto re-close ELCB are designed. For early stage, the first thing to do are designing the basic of power circuit that include voltage regulator, bridge rectifier, transformer to produce 5Vdc that will be used to supply PIC, current sensor and LCD. Then follow by designing the controller circuit involve the application of PIC microcontroller. The next stage is designing the electronic switching circuit which needs to be used instead of original mechanical switch. The last stage of circuit is to design sensing circuit using current sensor that will sense to any fault occurred. Then finally stage, all the circuit is combined together and then trouble shooting is done to check our circuit connection. After hardware is finished, programming can be made to make the flow of process following the in flow chart. By using different method to different any fault, new auto re-closer is tested according each fault and when there were problem occur, the hardware is troubleshoot and the problem is correct. The process was done when the new auto re-closer ELCB running following the objective requirement.

4.3 proposed design

Based from proposed design in figure 3.1 below, transformer 240/15Vac step down is used to converting 240Vac from power line to 5Vdc by using full wave rectifier circuit. The 5Vdc will used to energize the LCD, PIC and current sensor. An protection at power line, metal oxide varistor 275V (MOV) is used to protect component in power circuit if fault like over current happen.

From that figure, the application of solid state relay is used as switch to replaced mechanical switch in old ELCB. SSR is selected as switching is because the reliability of the SSR itself as Electronic switch that can be operated at high voltage and current. LM 7805 voltage regulator will be used to step down the voltage from 15Vdc to 5Vdc to ensure it suitable to supply to PIC, LCD and current sensor.

For sensing circuit, half effect current sensor with rating 5A is used to detect the any leakage current between neutral and phase then send tripping signal to PIC which assigned the fault are occurred. The output of current sensor is fixed 5V and it will easier PIC to understand the information received.

For the control element, PIC 18F4550 is choosed to control our system. That PIC will receive the data information from current sensor and decide to connect or disconnected circuit. It can be done by connect PIC with solid state relay which PIC will control switching of SSR.

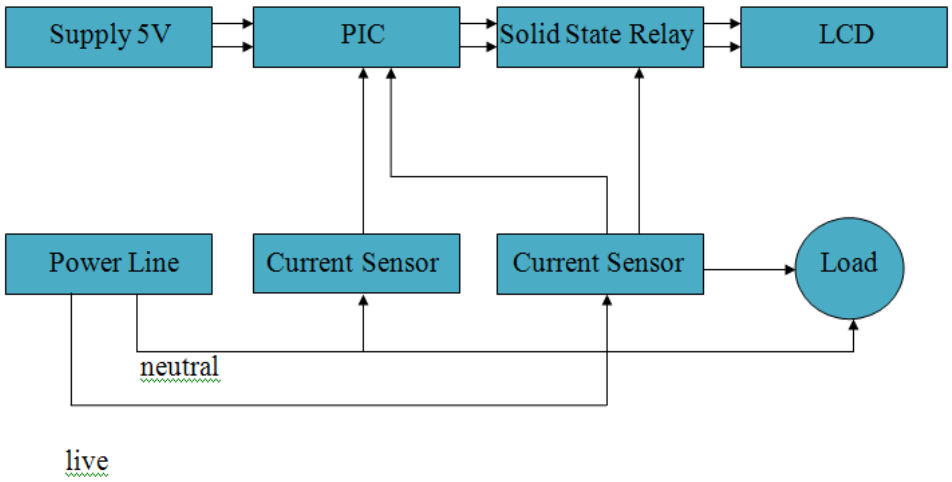


Figure 4.1: Basic Operation of Auto Re-closer ELCB

4.4 Stage 1 circuit

Refer from figure 4.2, this power circuit is the combination between transformer 240Vac/12Vac, bridge rectifier, LM7805, capacitor 470uF and capacitor 10uF.Transformer will step down the 240Vac to 15Vac then bridge will change from ac source current to dc source. After that, LM7805 will used to regulate voltage from

15Vdc to 5Vdc supply. Lastly, LED will connected at the end of 5V terminal to show that 5V is already give supply to LCD, PIC, and current sensor.

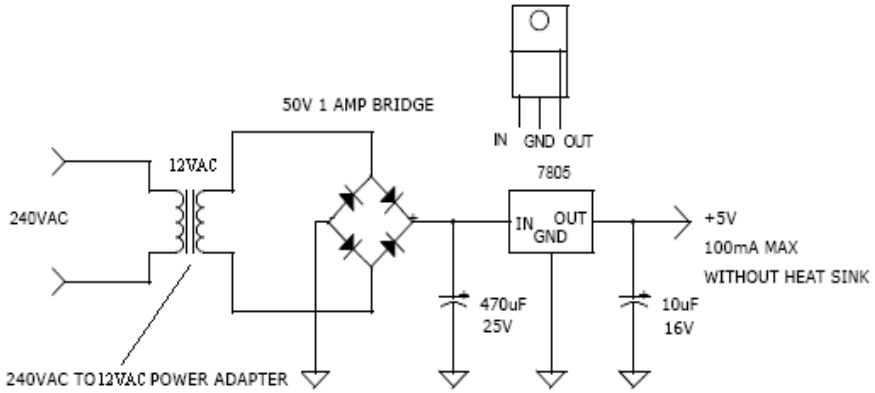


Figure 4.2: 5Vdc Power Supply Circuit

4.5 Stage 2 circuit

Based from that figure, it showed the interfacing between PIC and JHD162A LCD display. The LCD is used as output and PIC will assign connection of LCD pin with 0.If PIC receive tripping signal following fault occurred, PIC will send data to LCD to display either temporary fault or permanent fault was detected. To make system more simple and tidy, ribbon cable is used as connector between LCD and PIC. Both of PIC and LCD need 5V that come from power circuit to execute their operation. For PIC driver, 20Mhz crystal oscillator is used to control the clock cycle of the system. variable resistor 20K is used to control the LCD screen .

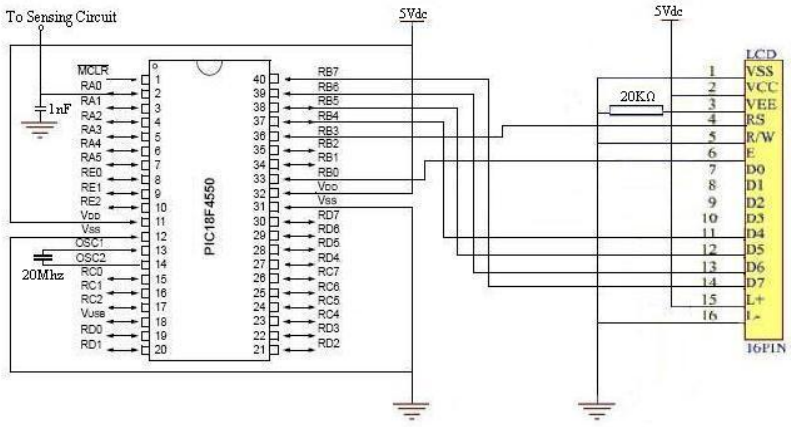


Figure 4.3: PIC Microcontroller and LCD circuit

According from the table 4.4, it show the total connection pin used for PIC18F4550.PIC18F4550 is connected with LCD, solid state relay and current sensor and total pin used is 16 pin. Pin 11 and 13 assigned as VDD pin, it connected together to receiving 5V supply. Beside that, pin 12 and 31 is assigned as Vss pin which it connected together directly go to ground.Meabwhile,OSC1 and OSC2 is connected to 20Mhz oscillator which act as clock for PIC 18F4550.Next,RA1 and RA2 is the pin from port A which it especially for analog input, which that port will understand any information in analog signal form from sensing circuit. Then, port B is placed by LCD and solid state relay and both of them is used as output.

Table 4.4: PIC18F4550 pin used detail

Pin Name	Pin No.	Description	Application
VDD	11, 32	Positive supply (+5V)	Power supply to PIC
VSS	12, 31	Ground references	Ground references
MCLR	1	Input	For reset button
OSC1,OSC2	13, 14	For oscillator	Connected to 20MHz

			crystal
RA1 and RA2	3,4	Analog input	Analog input from Sensing Circuit LM358
RB0, RB3-RB7	33, 36, 37, 38, 39, 40	Output	Connected to LCD data (DB0-DB7)
RB2	35	Output to 5V relay	To trip circuit breaker

4.6 Stage 3 Circuit

Figure is showed the sensing circuit that has been used in that project. The pair of half effect current sensor 5A is connected through life and neutral supply. The both of them will determine the current flow and send the value of current detected onto PIC. If PIC can differentiate value of current from both of current sensor, PIC will automatically understand and directly open the contact of switch from SSR. Thus, circuit will disconnected supply and break the power line.

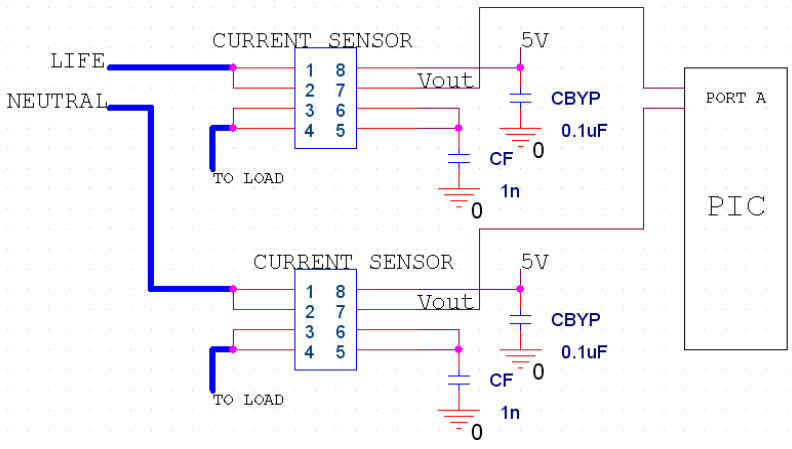


Figure 4.5: Sensing Circuit

4.6.1 Voltage Regulator

Figure 3.10 shows the model of UTC LM 7805. The UTC LM78XX family is monolithic fixed voltage regulator integrated circuit. They are suitable for applications that required supply current up to 1 A.

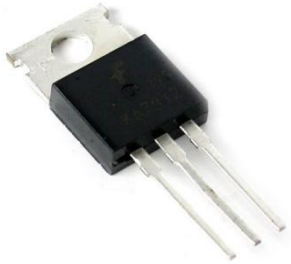


Figure 4.6: LM7805 Voltage Regulator

The UTC LM79XX series of three-terminal negative regulators are available in TO-220 package and with several fixed output voltage, making them useful in a wide range of application. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible.

4.6.2 Centre Tap Transformer 240/12Vac

Figure 3.9 shows the centre tap Transformer, it is one type of transformer that used to reduce the voltage from 230Vac to 12Vac and supply the voltage to the power supply circuit. It is the most comprehensive choice of secondary voltages. It also is flame retardant bobbins and shrouds. Besides, fully shrouded construction

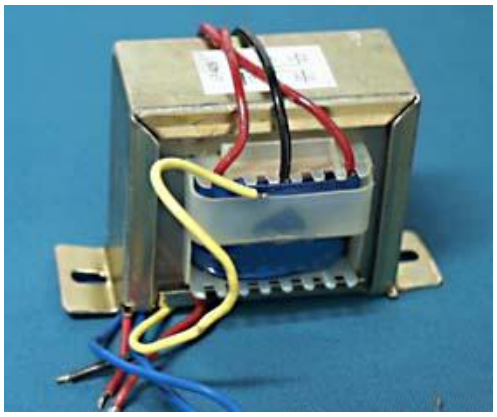


Figure 4.7: Centre Tap Transformer

4.6.3 Solid state relay

Refer to the Figure 3.7 the Solid State Relays (SSR) which is an electronic switch, which, unlike an electromechanical relay, contains no moving parts. A SSR is a semiconductor device that can be used in place of a mechanical relay to switch electricity to a load in many applications. SSRR are purely electronic, normally composed of a low current “control” side (equivalent to the coil on an electromechanical relay) and a high-current load side (equivalent to the contact on a conventional relay). SSR typically also feature electrical isolation to several thousand volts between the control and load sides. Because of this isolation, the load side of the relay is actually powered by the switched line, both line voltage and a load must be present for the relay to operate.

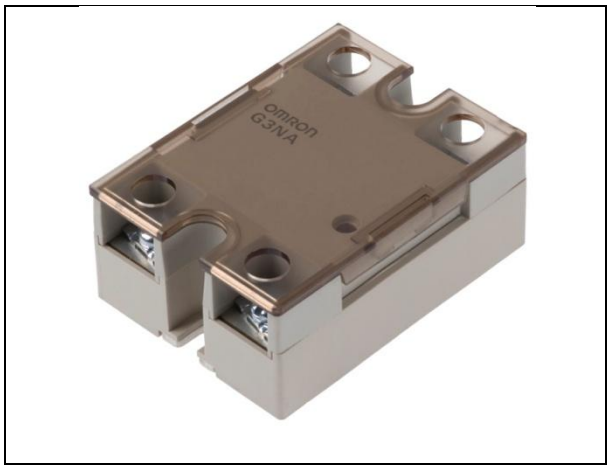


Figure 4.8: Solid State Relay (SSR)

SSR are faster than electromechanical relays; their switching time is dependent on the time needed to power the LED on and off, on the order of microseconds to milliseconds. SSR increased lifetime due to the fact that there are no moving parts, and thus no wear. SSR also decreased electrical noise when switching with totally silent operation.

There are many applications that require a moderate amount of power (W to kW) to be switched on and off fairly rapidly. A good example would be the operation of a heater element in a controlled-temperature system. Typically, the amount of heat put into the system is regulated using pulse-width modulation turning a fixed-power heating element on and off for time periods ranging from seconds to minutes. Mechanical relays have a finite cycle life, as their components tend to wear out over thousands to millions of cycles. SSR do not have this problem; in the proper application, they could be operated almost infinitely.

This project the use the SSR with specification:

Description

- Solid-State Panel Mount Relay
- Series:G3NA
- Control Voltage Type: DC
- Load Current RMS Max:40A
- Load Voltage RMS Max:240VAC
- Load Voltage RMS Min:24VAC
- Contacts: SPST-NO
- Control Voltage Max:24V
- Control Voltage Min:5V

4.6.4 Bridge Rectifier

Refer to the Figure 3.11 it is the BR1036432 Bridge model, it is used to rectify the voltage from AC supply to DC power supply for IC voltage regulator device.

Figure 4.9: Bridge Rectifier

4.6.5 One way Switch

Figure 3.12 shows the one way Switch, it is the main switch for the whole circuit. The function of this Main switch is to open and closed the whole system. This switch functions manually. In this project, switch is used to open and close 5V supply to LCD,PIC an current sensor.

Figure 4.10: One Way Switch

4.6.6 Light Emitting Diode

Figure 3.14 shows green and red light-emitting-diode (LED), LED is based on the semiconductor diode. When the diode is forward biased (switched on), electrons are able to recombine with holes and energy is released in the form of light. This effect is called electroluminescence and the color of the light is determined by the energy gap of the semiconductor.

Figure 4.11: Light Emitting Diode (LED)

In this project, the red LED was used to show that there are supply voltage entering the whole circuit. Meanwhile yellow LED used to indicate when the solid state relay is operated.

4.6.7 Liquid Crystal Display

A liquid crystal display (LCD) is an electronically-modulated optical device shaped into a thin, flat panel made up of any number of color or monochrome pixels filled with liquid crystals and arrayed in front of a light source (backlight) or reflector. It is often utilized in battery-powered electronic devices because it uses very small amounts of electric power. Figure 3.15 show the LCD model JHD162A SERIES that is used for this project.

Figure 4.12: Liquid Crystal Display

Each pixel of an LCD typically consists of a layer of molecules aligned between two transparent electrodes, and two polarizing filters, the axes of transmission of which are (in most of the cases) perpendicular to each other. With no actual liquid crystal between the polarizing filters, light passing through the first filter would be blocked by the second (crossed) polarizer.

LCD with a small number of segments, such as those used in digital watches and pocket calculators, has individual electrical contacts for each segment. An external dedicated circuit supplies an electric charge to control each segment. This display structure is unwieldy for more than a few display elements.

4.6.8 Half effect current sensor

A current sensor is a device that detects electrical current (AC or DC) in a wire, and generates a signal proportional to it.

The sensed current and the output signal can be:

- AC current input,
  - analog output, which duplicates the wave shape of the sensed current
  - unipolar output, which is proportional to the average or RMS value of the sensed current
- DC current input,
  - unipolar, with a unipolar output, which duplicates the wave shape of the sensed current
  - bipolar output, which duplicates the wave shape of the sensed current
  - digital output, which switches when the sensed current exceeds a certain threshold

Typical applications include motor control, load detection and management, switch mode power supplies, and over current fault protection. The device is not intended for automotive applications. The device consists of a precise, low-offset, linear Hall circuit with a copper conduction path located near the surface of the die. Applied

current flowing through this copper conduction path generates a magnetic field which the Hall IC converts into a proportional voltage. Device accuracy is optimized through the close proximity of the magnetic signal to the Hall transducer.

Figure 4.13: Half effect Current Sensor

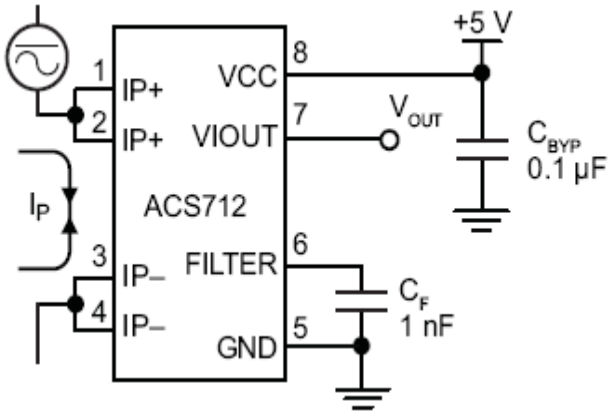


Figure 4.14: Current Sensor Pin Configuration

Table 4.15: Current Sensor Pin Description

Number	Name	Description
1 and 2	IP+	Terminals for current being sampled; fused internally
3 and 4	IP–	Terminals for current being sampled; fused internally
5	GND	Signal ground terminal
6	FILTER	Terminal for external capacitor that sets bandwidth
7	VIOUT	Analog output signal
8	VCC	Device power supply terminal

4.6.9 Adaptor SMD Current sensor

This adaptor is design especially as based to half effect current sensor. Type of pin half effect current sensor is SMD pin, so that base device will connected the small pin configuration of current sensor.

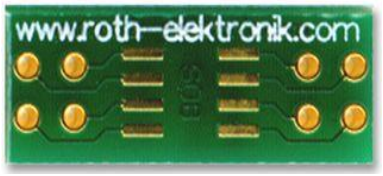


Figure 4.16: Adaptor SMD

4.6.10 Metal Oxide Varistor (MOV)

The most common type of varistor is the Metal Oxide Varistor (MOV). The boundary between each grain and its neighbour forms a diode junction, which allows current to flow in only one direction. When a small or moderate voltage is applied across the electrodes, only a tiny current flows, caused by reverse leakage through the diode junctions. When a large voltage is applied, the diode junction breaks down due to a combination of thermionic emission and electron tunneling, and a large current flows. The result of this behavior is a highly nonlinear current-voltage characteristic, in which the MOV has a high resistance at low voltages and a low resistance at high voltages. In this project, MOV is used to prevent line in power circuit from damage if fault like over current is detected.

Figure 4.17: Metal Oxide Varistor

4.6.11 Fuse 0.1A

Fuse used in electrical systems to protect against excessive current. In this project, fuse is used for protection purpose same like MOV function.

Figure 4.18: Fuse

4.7 Final Stage Circuit

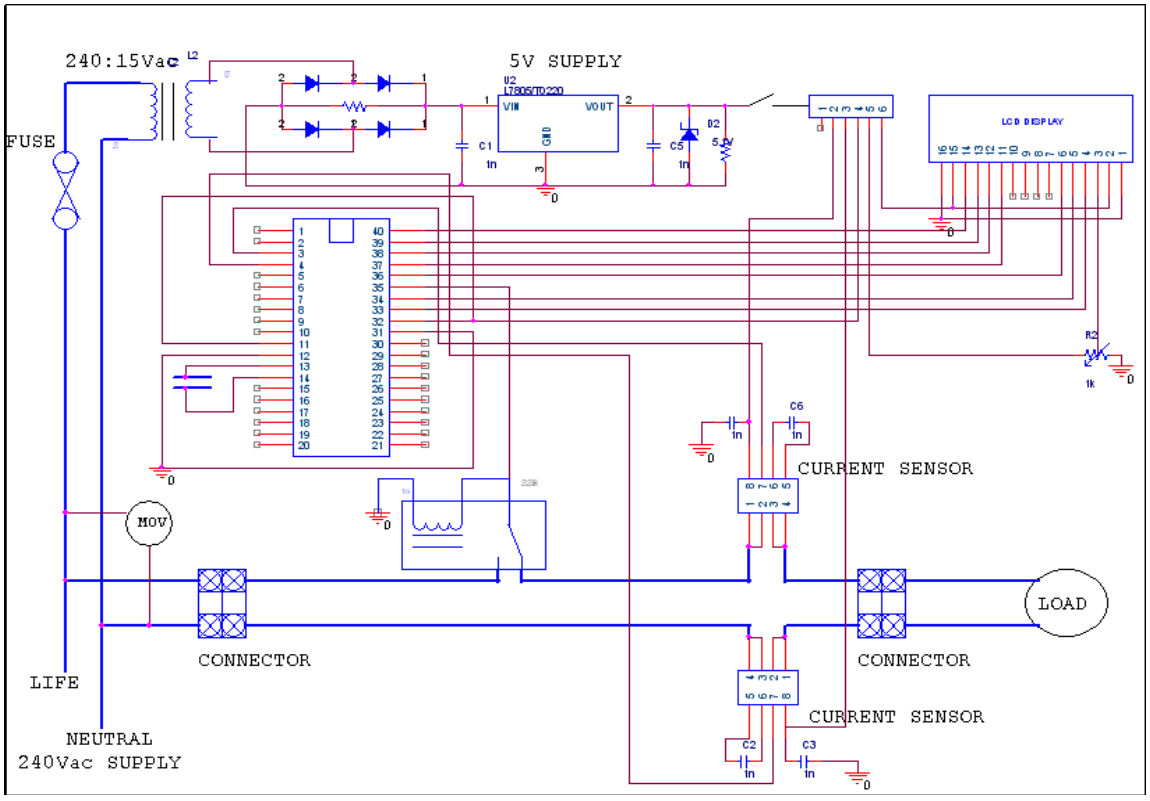


Figure 4.19: Final Stage Circuit

Figure show the final circuit for that project. By combining three stages of circuit, we can get the final hardware design for new auto re-closer ELCB. With arrangement for every stage, hardware is test and being troubleshoot. The main purpose make step by step stage is to avoid error in connection occurred and that device can integrated together. After design that hardware, it goes to next phase to designed software implementation.

4.8 Flow Chart

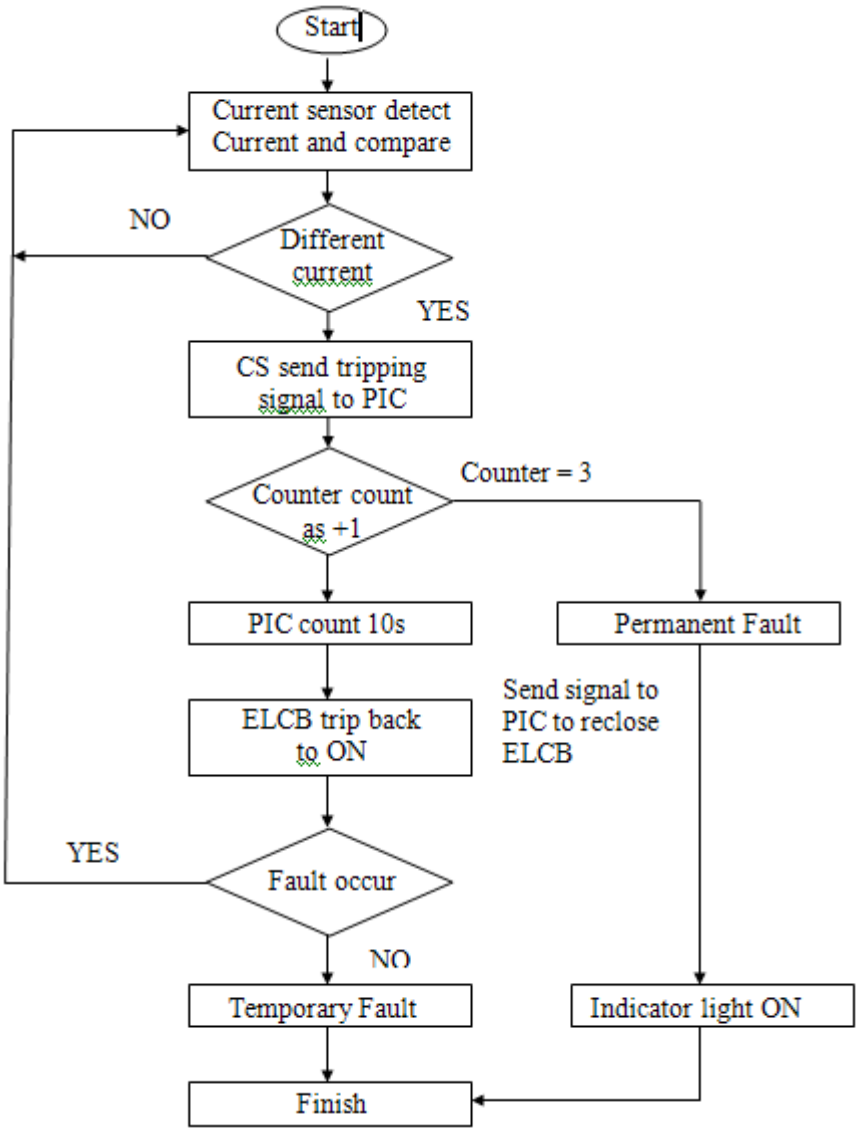


Figure 4.20: Flow chart of the system

Refer from figure when a fault occurred between line neutral and life, both of current sensor will sense the imbalance current and send the induced current at PIC.PIC will compaired the value of current between both of current sensor then if any differential current exist, PIC will send signal to trip ELCB. At this moment PIC will start to count as 1.After 10 second PIC will send signal to switch contact automatically to switch back to normal condition. If there is no fault detect after the ELCB is turn on the LCD will display temporary fault and the ELCB will stay connected until next fault occurred and the counter will be reset. Meanwhile if there any fault continuously occurred after the ELCB turning back ON, the current sensor will detect the imbalance current and then will send the signal to PIC and PIC will disconnected circuit and in 10 second, ELCB is turn back ON. At this time PIC counter will count as 2 and if fault continuosly detected, the process will be cycle until counter reach 3 count .After PIC counter reach 3 count, PIC will identify the fault as permanent fault such like short circuit or over current and LCD will display that type of fault. At the time, circuit is disconnected and tripped permanently. If any fault is cleared, user should turn ON manually the ELCB

4.9 Hardware Operation Process

From the flow on the figure, it early start with supply voltage 240Vac single phase from TNB and it directly connected to current sensor device and power circuit. At power circuit, transformer 240/15Vac will step down the supply from TNB and it rectified to DC source using bridge rectifier. Then regulator LM7805 will regulate that voltage to 5Vdc to energize PIC, current sensor and LCD. At the line of current sensor, if unbalanced current between life and neutral is detected, current sensor will send the signal to PIC.PIC will compare the differential value of current between both of them and if differential value current is exist, it show the value of current exceed 10mA.The output voltage from current sensor is fixed with 5V, thus it will easier PIC to receive the

information. The output voltage from current sensor is send to PIC through ADC (analog digital port).As the ELCB main switching, solid state relay is connected through port B. When fault occurred, PIC will detect the range of resolution that suitable for the condition of ELCB to trip when the imbalance current exceed Δ100mA, which is the minimum current value for the ELCB to trip. SSR then will be de-energized by the PIC and thus the ELCB is disconnected from the power line.

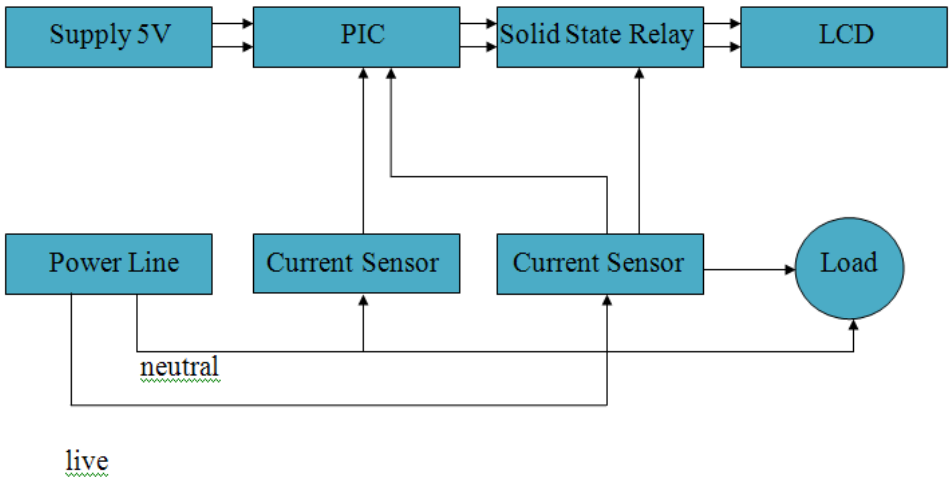


Figure 4.21 : Hardware operation process of Auto Re-Closer ELCB

4.10 Summary

This chapter explain detail about the concept and development new auto re-closer ELCB. Based from flow chart and final hardware design, it show how the device operate and execute their function. with combination hardware and software design, that device will be able to detect the type of fault. At this project, PIC microcontroller is the main brain to control the task and operate depend on the current that being sensed. Meanwhile, solid state relay will be the main output to connected or disconnected circuit

and LCD will monitor the display the fault condition. Beside that, installation stage by stage hardware is important to ensure all device operate their function. It will easier to trouble shoot if there problem exist.

CHAPTER 5

RESULT AND DISCUSSION

5.1 Introduction

This chapter shows the detail about the result and discussion for whole development of auto re-closer earth leakage circuit breaker. The result that will be discussed in this chapter is for data measurement of current sensor I in and I out. The induced of current depend on the load connected. From the data measurement, induced current that exceed 100mA sensitivity will cause tripping to ELCB. The sensing element is very important to ensure that device accurate in determine 100mA sensitivity. Because this project is based on protection system it is important to count every aspect of measurement in order to not mess with the original ELCB. Every discussion stated in this chapter also for the whole system problems, the better solution need to come-up in order to overcome every flaw and problems of this ELCB system.

5.2 Measurement of ZCT

In early planning, the application of ZCT and op-amp amplifier is used as sensing circuit. The objectives of measurement ZCT is to get the output value of induced current from the coil of the ZCT. Because there is magnetic material build in ZCT whenever there is unbalance current flow through the ZCT, the coil that winding around

the ZCT will induced current that is depend on the strength of the imbalance current. The induced current then will flow through the coil then it will flow to the sensing circuit. Because the induced current is Ac (Alternative current), the polarity of the current must be consider in order to avoid the effect of reverse current. This is very important in order to get a take measurement value while designing the current to voltage converter. Figure 5.1 show the operation of ZCT. But from the experiment before, it difficult to determine 100mA sensitivity and the current induced has not accurate to reach 100mA sensitivity. Thus, current sensor is replaced to improve the weakness of device before.

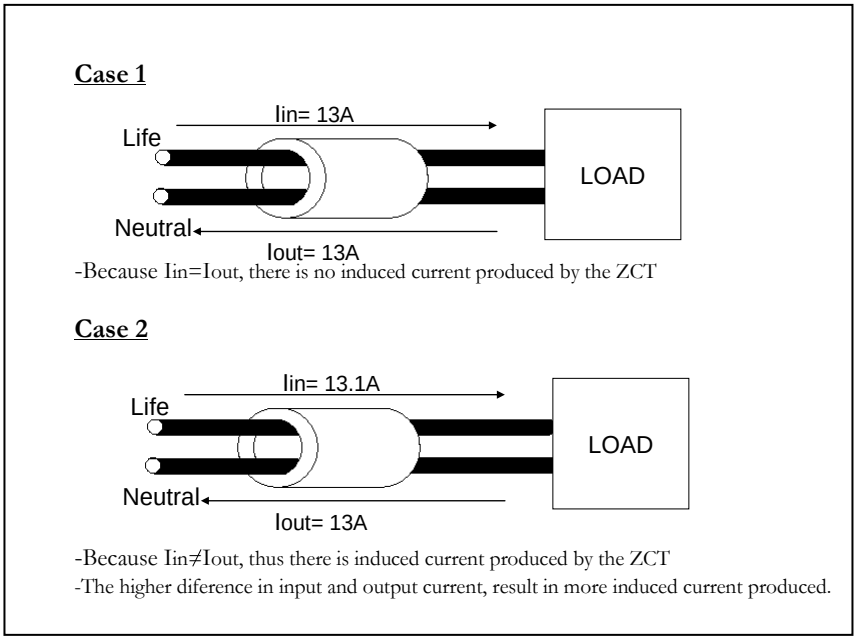


Figure 5.1: Operation of ZCT

5.3 Measurement of Current Sensor

The main objective of measurement current sensor is to get the output value induced current from the comparison between two of current sensor. If some load like motor and bulb lamp is connected to current sensor, it will produced induced current.

Actually for the current sensor, it already give output in voltage form, so it will easier to PIC for receive the signal information. The current sensor will fixed output voltage 5V and has rating current about 5A, but it can covered the load rating exceed 5A.in this experiment, two of current sensor is connected series. Current sensors need the 5V supply to operate and it directly connected to the motor. The figures 5.2 show the circuit connection to get the data measurement from current sensor.

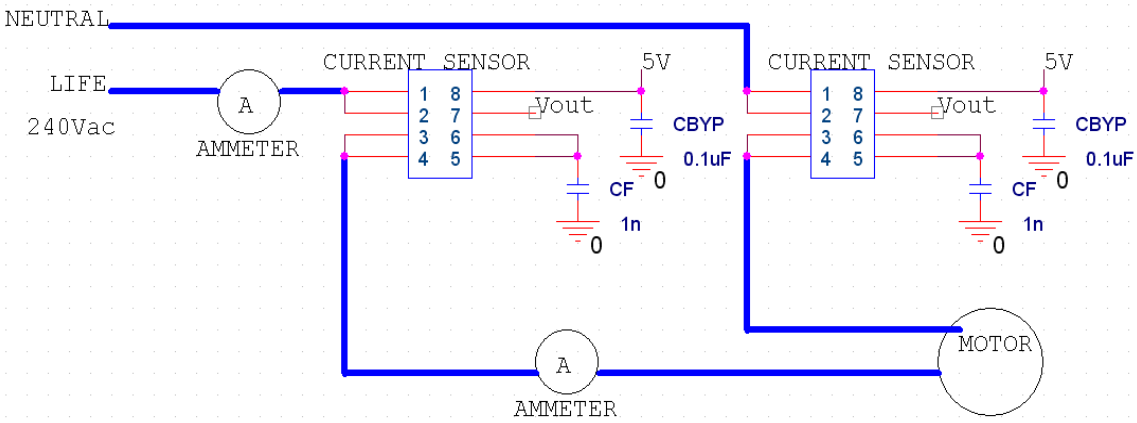


Figure 5.2: Connection for Current Sensor Measurement

That experiment is done by using pressure motor with rating 6A.The current sensor is directly connected to the load motor. The motor can control current to load by varied the pressure step by step. The advantage of using the motor is because motor drew high current during startup. This situation theoretically produced the surge current at the initially but soon after the current will be balance for the load. We can assume this condition of surge current from startup motor is approaching the condition of lightning. Even though the value of surge current of the lightning is too large and is over 100A, but the similarity can be consider since the sensitivity of the ZCT is 100mA. It has been proved that the induced current from current sensor by using this method is over 100mA which are the same of lightning that >100mA. The objective of this experiment is to find

the average value of induced current that is produced by ZCT in 10 measurements so that it can be taken as reference value for the input signal PIC. Figure 5.3 show the motor that is used for the experiment.

Figure 5.3: Pressure DC Motor 6A

To measure induced current from current sensor, life and current cable is directly connected to current sensor then it throw out connected to load motor. The motor is available with varied output which it can controlled by adjust the pressure of motor. If pressure is increase, induced current is more and otherwise. The experiment is done to show the relationship between supplies current and induce current and voltage produced from current sensor. Table below is show the data measurement from that experiment.

Table 5.4: Current Sensor Induced Current

Pressure	I in	I out	Vout1	Vout2
0	1.62	1.50	0.19	0.20
10	1.98	1.84	0.22	0.24
20	2.30	2.16	0.24	0.26
30	2.62	2.48	0.26	0.28
40	2.96	2.83	0.26	0.29
50	3.30	3.16	0.29	0.31
60	3.65	3.51	0.30	0.33
70	4.01	3.86	0.31	0.34
80	4.31	4.17	0.31	0.34

5.4 Arrangement of Fault Model

The main objective of arrangement fault model is to demonstrate how that device operation in assigned that kind of fault. It important to ensure circuit is functioning following the flow instruction. For this experiment, the model is design by using a 6A motor and 1A bulb. Both is used but with different function. Bulb is used as an indicator to see whether the ELCB is tripped or not. Meanwhile the motor used to produce the induced current sufficient to trip the ELCB.

For the simulation of temporary fault, the load line will on all the time to on the circuit system while the motor power supply will be turned on and turned off in that instant. It acts like the lightning which comes in only a few second or less than one second. So, the lamp will off when the motor on and then will be on back after the motor stop.

For the permanent fault model, the arrangement stills same but has a little different at time period of motor turned on. Motor will always switch on then the lamp will turn off along with the motor switch on. The PIC receives the voltage signal from sensing circuit and then it will on back the load (Bulb). Then the bulb will on back for a moment before it will turn of back because there is still signal voltage came from sensing circuit. This cycle will be continue for three cycle before PIC send signal to permanently switch off the bulb and the PIC will identify the fault is permanents fault. This is because permanent fault occur continuously unlike the temporary fault which is in only a moment. Figure 5.6 show the fault model arrangement circuit.

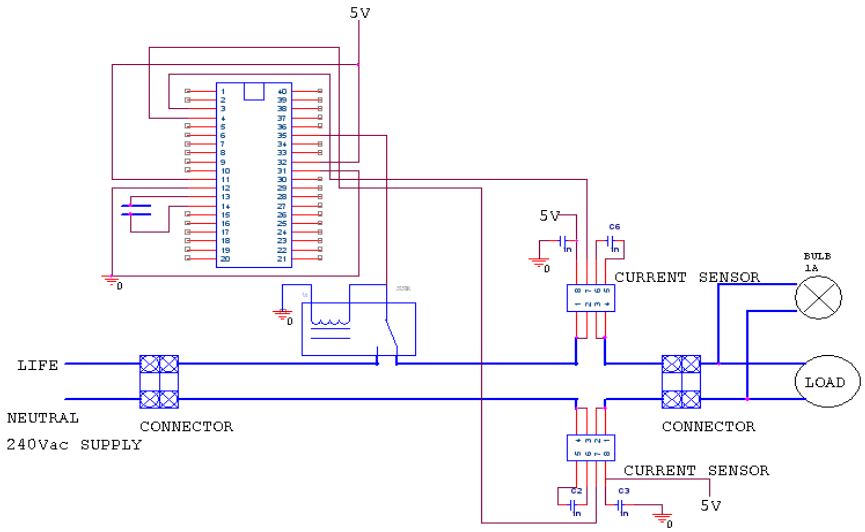


Figure 5.4: Fault Model Arrangement Circuit

5.5 Project Results

i. Based from testing and measurement, the result of this project are show as below:

ii. PIC microcontroller technology able to replace human to switch on or off the ELCB. From this project, PIC fully used to control the switch contact to cut-off the power line.

iii. The new auto re-closer ELCB are available to differentiate between permanent and temporary fault

iv. PIC application can be used for multi-purpose task depend on the programming

v. ELCB tripped the circuit for 5 second and count 1 to assigned temporary fault

vi. The ELCB permanently disconnected the circuit if the circuit detects the leakage continuously. The ELCB will re-close for the cycle of 3 times before it will notify that the fault is permanent fault via the display of LCD.

5.6 Discussions

From this project, what we can discuss is:

i. The development of auto re-closer is still new and there is no ELCB with auto re-closer available in the market. The process to make efficient ELCB should have the guideline from other resource as manufacturer itself.
ii. Beside the sensitivity of 100mAsensitivity for domestic and 300mA sensitivity for factory following standard IEEE thus we need to use the current setting so that there is no fatal error or hazard occurs.
iii. The lack of knowledge and references during make this project should be considered. It fully depend on creativity and experience from engineering lab subject before. Beside that, to measure the ability and connection of device, it fully depend on data sheet.

5.7 Summary

Based from the result and discussion, there are some important think to make our project be successful. The most important think is in order to get sensitivity 100mA which the application of current sensor is fully need to give data information to PIC. the function of current sensor is the main key to make PIC execute their instruction following the programming chart. There are currently 0.1A, 0.3A, 0.6A and also 1A sensitivity for nowadays ELCB but since most the resident application standard is 0.1A so the range sensitivity of 0.1A is picking so that any small change in unbalance current will result in tripping of the ELCB.

CHAPTER 6

CONCLUSIONS & SUGGESTIONS

6.1 Conclusions

Finally, the main to design and produced new ELCB with auto re-closer is fulfilled. ELCB is used in domestic as protection device. From new auto re-closer ELCB, it still has function same with old ELCB but our system is more intelligent. Aspect protection new auto re-closer ELCB more efficient if compared to old ELCB. Consumer will be alert if any fault occur and can avoid any bad situation, thus it makes human life easier that way.LCD will display that kind of fault and it will alert the consumer and avoid them from electric shock. This project are combined with PIC microcontroller, electronic switch, driver circuit and sensing circuit and all of them is integrated together to build the new auto re-closer ELCB.

The use of solid state relay compared heavy power relay have increase the reliability and effectiveness, even though the cost of solid state relay is higher than the cost of heavy power relay. Other reason, solid state has faster switching operation and it suitable to react immediately to avoid the equipment in circuit damage. The using of PIC18F4550 as control element made the system more reliable for modern technology. Every port in PIC microcontroller can be varied to be output or input and it fully depend on the programmer to set it. At the same time, it will improve the weak of old ELCB beside to replaced human action in order to control the ELCB.

The successful of this auto re-closer ELCB system has made the circuit can differentiate between permanent and temporary fault and acting differently between each type of fault. To make this project, knowledge from engineering lab, microprocessor, autotronic, power electronic and other skill is most important in order to make this project success

6.2 Suggestions

There are several suggestions after the process for improvement AR-ELCB in the future:

i. Before start designing the hardware, choosing the component with suitable rating, device specification, device endurance. Refer and study all the formation source from the data sheet and internet before choosing that kind of component.

ii. Replaced the application of bridge rectifier with diode. Use 4 pieces of diode and arrange it in full wave rectifier connection. Thus it can reduce the cost and make circuit design more economic

iii. In this project current sensor is used as sensing circuit. So for the next improvement , replaced it with the current transducer or current transformer. Compare which device has better sensitivity at the last. With the use of current transducer or current transformer, user might be able to improve the reliability of the ELCB.

iv. Replace the 40 PIC18F4550 microcontrollers with 28 pin PIC18F2550 microcontroller. It is due to the PIC18F2550 have less port compare to PIC18F4550 which are 40-pin over 28-pin. Other than that the function of PIC 18F2550 is similar to PIC18F4550. Even though PIC 18F2550 have less port

compare to PIC18F4550, but the port is sufficient to use in this project because for this project by using PIC18F4550 only 10 port for input and output signal. It is important to consider PIC18F4550 because we can save the cost along with the size.

v. The using of solid state relay in this project is to replaced the function of mechanical switch from old ELCB. Currently for this project, SSR rating 20A with 5~24Vdc has been used. So in the future recommended using SSR with differential rating. Try to choose low rating current such as 10A and 5 A with 5~24Vdc rating because the current used actually does not consumed higher than 10A.Beside that, it might be reduced the cost because the price of SSR is depend on the current rating

vi. In future improvement, I would suggest to used charger to replaced the using of transformer and voltage regulator. Output voltage for charger is fixed with 5V and it sufficient to supply to LCD,SSR and PIC microcontroller. Beside that, circuit seen more simpler and reduce the using spacing.

vii. Lastly for future recommendation, design that circuit in printed circuit board. By using software orcad or DXP protell, The actual size of Vera board can be reduced to 1:10 from the original size of the PCB prototype.

6.3 Costing And Commercialization

This part will describe overall cost to design one unit of auto re-closer ELCB. This part also will explain the commercialization of project.

6.3.1 Costing

Tables 6.1 show the cost of the component and the total cost. The total cost of the development of Earth Leakage Circuit Breaker with an auto re-closer unit is RM 358.67.It just involve the hardware implementation include electrical and electronic component. Due to changing of component in the development process, some component not fully function and need to be replaced during the hardware circuit designing. The total price in the table is just estimate cost which not involve to any problem component. The cost actually can be reduced, it can be done by using component with suitable rating and also by buying the component in mass quantity.

Table 6.1: The cost of components

Device	**Qty**	**Model**	**Unit**	**Manufacture**	**Unit cost(RM)**	**Extended cost (RM)**
Transformer	1	T1201	-230V,50Hz -Vo : 12 - 0 - 12. Output -Power : 6 VA	TELETRON	13.00	13.00
Bridge Rectifier	1	KBPC6005PBF	-Vrrm:50V -Current Rating: 6A	INTERNATIONAL RECTIFIER	3.00	3.00
Capacitor	1		-470uF		0.15	0.15
Capacitor	1		-10uF		0.15	0.15
Capacitor	1		-1nF		0.15	0.15
Voltage Regulator	1	LM7805	-+5V dc		1.00	1.00
LED	2				0.10	0.20
Resistor	1		1kΩ		0.10	0.10

Resistor	1		150Ω		0.10	0.10
Variable Resistor	1		20kΩ		2.50	2.50
Zener Diode	1		5.1V		0.50	0.50
PCB Header	6				1.00	6.00
LCD	1	2X16 JHD16A			15.00	15.00
PIC	1	18F4550		Microchip	30.00	30.00
Connector	2				2.20	4.40
Solid State Relay	1	G3NA-220B	-Vo: 240Vac -Vin: 5-24Vdc	Omron	153.92	153.92
MOV	1	BJ2205 S271K101	275Vac		3.28	3.28
Fuse	1		-0.3A		0.20	0.20
Switch	1				1.00	1.00
ZIF Socket	1				15.00	15.00
Current Sensor	2				20.36	40.72
Wrapping Wire	1				15.00	15.00
Adaptor SMD	2		260.15		**26.65**	53.30
					TOTAL	358.67

6.3.2 Commercialization

For commercialization purpose, next auto re-closer is more cheaper due to cost. If new auto re closer is built in following recommend suggestion, estimated cost should be around RM200.00 only. So that device can be more economic and not encumber the customer. There is no auto re-closer ELCB available in the market, so it has higher commercialize value due to resolve the problem existence in ELCB

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APPENDIX A

PIC18F4550 Microcontroller, Addressing Modes, and Instruction Set

PIC18F4550 MICROCONTROLLER, ADDRESSING MODES AND INSTRUCTION SET

MICROCHIP **PIC18F2455/2550/4455/4550**

28/40/44-Pin, High-Performance, Enhanced Flash, USB Microcontrollers with nanoWatt Technology

Universal Serial Bus Features:

- USB V2.0 Compliant
- Low Speed (1.5 Mb/s) and Full Speed (12 Mb/s)
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- Supports up to 32 Endpoints (16 bidirectional)
- 1-Kbyte Dual Access RAM for USB
- On-Chip USB Transceiver with On-Chip Voltage Regulator
- Interface for Off-Chip USB Transceiver
- Streaming Parallel Port (SPP) for USB streaming transfers (40/44-pin devices only)

Power-Managed Modes:

- Run: CPU on, peripherals on
- Idle: CPU off, peripherals on
- Sleep: CPU off, peripherals off
- Idle mode currents down to 5.8 µA typical
- Sleep mode currents down to 0.1 µA typical
- Timer1 Oscillator: 1.1 µA typical, 32 kHz, 2V
- Watchdog Timer: 2.1 µA typical
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Four Crystal modes, including High Precision PLL for USB
- Two External Clock modes, up to 48 MHz
- Internal Oscillator Block:
  - 8 user-selectable frequencies, from 31 kHz to 8 MHz
  - User-tunable to compensate for frequency drift
- Secondary Oscillator using Timer1 @ 32 kHz
- Dual Oscillator options allow microcontroller and USB module to run at different clock speeds
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if any clock stops

Peripheral Highlights:

- High-Current Sink/Source: 25 mA/25 mA
- Three External Interrupts
- Four Timer modules (Timer0 to Timer3)
- Up to 2 Capture/Compare/PWM (CCP) modules:
  - Capture is 16-bit, max. resolution 5.2 ns (TCY/16)
  - Compare is 16-bit, max. resolution 83.3 ns (TCY)
  - PWM output: PWM resolution is 1 to 10-bit
- Enhanced Capture/Compare/PWM (ECCP) module:
  - Multiple output modes
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
- Enhanced USART module:
  - LIN bus support
- Master Synchronous Serial Port (MSSP) module supporting 3-wire SPI (all 4 modes) and I^2C™ Master and Slave modes
- 10-bit, up to 13-channel Analog-to-Digital Converter module (A/D) with Programmable Acquisition Time
- Dual Analog Comparators with Input Multiplexing

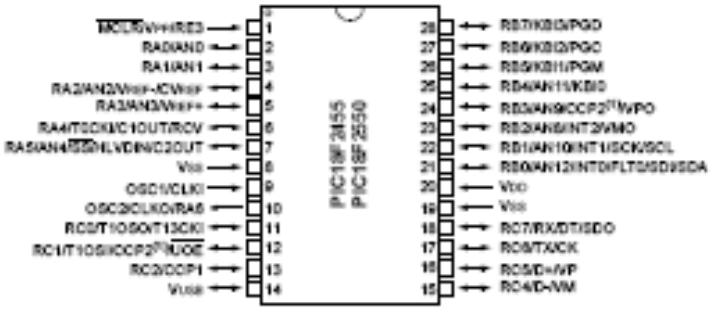
Special Microcontroller Features:

- C Compiler Optimized Architecture with optional Extended Instruction Set
- 100,000 Erase/Write Cycle Enhanced Flash Program Memory typical
- 1,000,000 Erase/Write Cycle Data EEPROM Memory typical
- Flash/Data EEPROM Retention: > 40 years
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 41 ms to 131s
- Programmable Code Protection
- Single-Supply 5V In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via two pins
- Optional dedicated ICD/ICSP port (44-pin devices only)
- Wide Operating Voltage Range (2.0V to 5.5V)

Device	Program Memory		Data Memory		I/O	10-Bit A/D (ch)	CCP/ECCP (PWM)	SPP	MSSP		EAUSART	Comparators	Timers 8/16-Bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)					SPI	Master I^2C™			
PIC18F2455	24K	12288	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F2550	32K	16384	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F4455	24K	12288	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3
PIC18F4550	32K	16384	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3

Pin Diagrams

28-Pin PDIP, SOIC



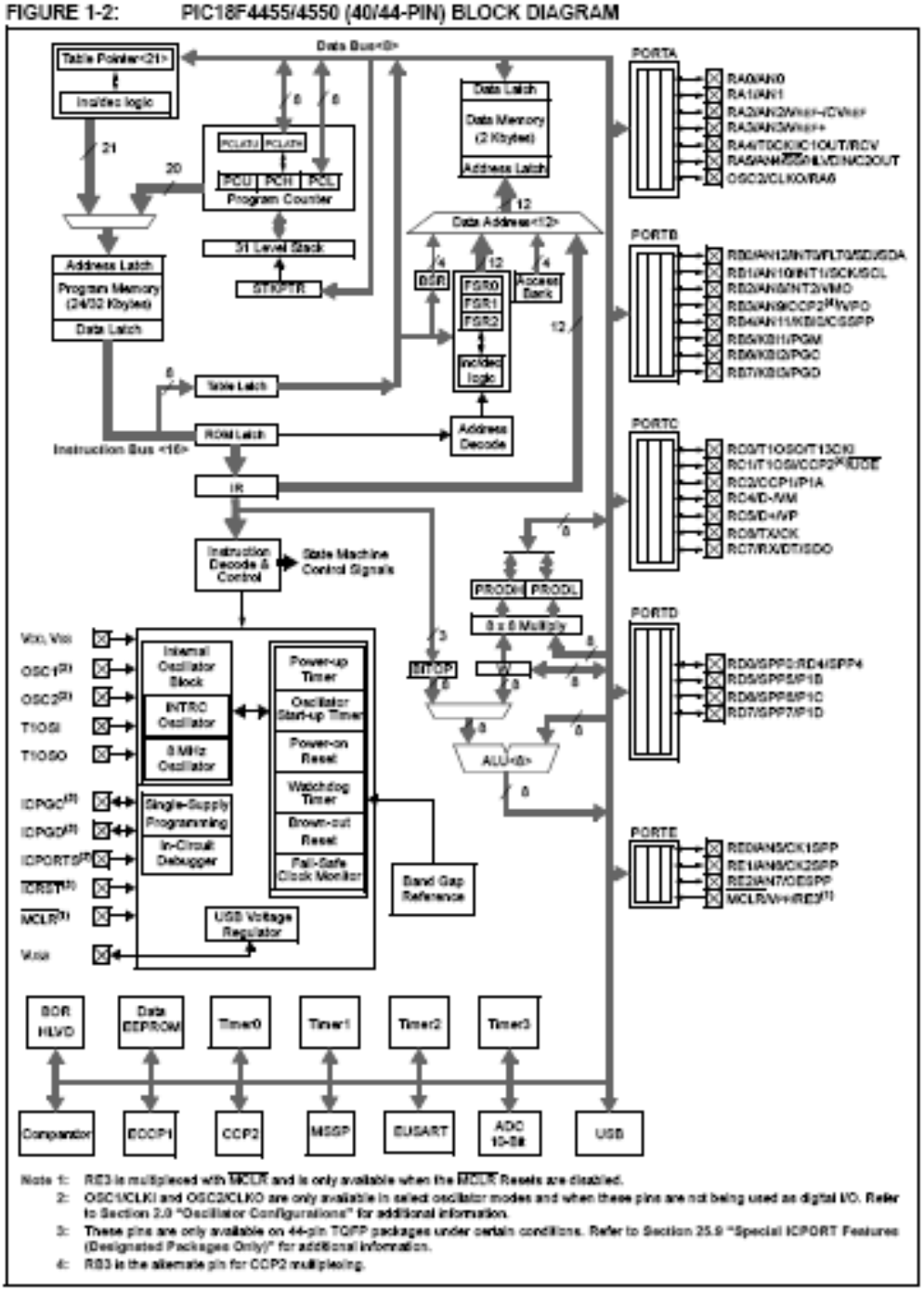
40-Pin PDIP

Note 1: RB3 is the alternate pin for CCP2 multiplexing.

TABLE 1-1: DEVICE FEATURES

Features	PIC18F2455	PIC18F2550	PIC18F4455	PIC18F4550
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	24576	32768	24576	32768
Program Memory (Instructions)	12288	16384	12288	16384
Data Memory (Bytes)	2048	2048	2048	2048
Data EEPROM Memory (Bytes)	256	256	256	256
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/ Compare/PWM Modules	0	0	1	1
Serial Communications	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART
Universal Serial Bus (USB) Module	1	1	1	1
Streaming Parallel Port (SPP)	No	No	Yes	Yes
10-Bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Comparators	2	2	2	2
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT
Programmable Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled
Packages	28-pin PDIP 28-pin SOIC	28-pin PDIP 28-pin SOIC	40-pin PDIP 44-pin QFN 44-pin TQFP	40-pin PDIP 44-pin QFN 44-pin TQFP

FIGURE 1-2: PIC18F4455/4550 (40/44-PIN) BLOCK DIAGRAM



Note 1: RE3 is multiplexed with MCLR and is only available when the MCLR Resets are disabled.
2: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. Refer to Section 2.0 "Oscillator Configurations" for additional information.
3: These pins are only available on 44-pin TQFP packages under certain conditions. Refer to Section 25.0 "Special ICPORT Features (Designated Packages Only)" for additional information.
4: RB3 is the alternate pin for CCP2 multiplexing.

TABLE 1-2: PIC18F2455/2550 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	PDIP, SOIC			
MCLR/VPP/RE3	1			Master Clear (input) or programming voltage (input).
MCLR		I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP		P		Programming voltage input.
RE3		I	ST	Digital input.
OSC1/CLKI	9			Oscillator crystal or external clock input.
OSC1		I	Analog	Oscillator crystal input or external clock source input.
CLKI		I	Analog	External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)
OSC2/CLKO/RA6	10			Oscillator crystal or clock output.
OSC2		O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO		O	—	In select modes, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6		I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
MCLR/VPP/RE3	1	18	18			Master Clear (input) or programming voltage (input).
MCLR				I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP				P		Programming voltage input.
RE3				I	ST	Digital input.
OSC1/CLKI	13	32	30			Oscillator crystal or external clock input.
OSC1				I	Analog	Oscillator crystal input or external clock source input.
CLKI				I	Analog	External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)
OSC2/CLKO/RA6	14	33	31			Oscillator crystal or clock output.
OSC2				O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO				O	—	In RC mode, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6				I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTA is a bidirectional I/O port.
RA0/AN0	2	19	19			
RA0				I/O	TTL	Digital I/O.
AN0				I	Analog	Analog input 0.
RA1/AN1	3	20	20			
RA1				I/O	TTL	Digital I/O.
AN1				I	Analog	Analog input 1.
RA2/AN2/VREF-/ CVREF	4	21	21			
RA2				I/O	TTL	Digital I/O.
AN2				I	Analog	Analog input 2.
VREF-				I	Analog	A/D reference voltage (low) input.
CVREF				O	Analog	Analog comparator reference output.
RA3/AN3/VREF+	5	22	22			
RA3				I/O	TTL	Digital I/O.
AN3				I	Analog	Analog input 3.
VREF+				I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/C1OUT/ RCV	6	23	23			
RA4				I/O	ST	Digital I/O.
T0CKI				I	ST	Timer0 external clock input.
C1OUT				O	—	Comparator 1 output.
RCV				I	TTL	External USB transceiver RCV input.
RA5/AN4/$\overline{SS}$/ HLVDIN/C2OUT	7	24	24			
RA5				I/O	TTL	Digital I/O.
AN4				I	Analog	Analog input 4.
$\overline{SS}$				I	TTL	SPI slave select input.
HLVDIN				I	Analog	High/Low-Voltage Detect input.
C2OUT				O	—	Comparator 2 output.
RA6	—	—	—	—	—	See the OSC2/CLKO/RA6 pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the $\overline{ICPRT}$ Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/AN12/INT0/FLT0/SDI/SDA	33	9	8			
RB0				I/O	TTL	Digital I/O.
AN12				I	Analog	Analog input 12.
INT0				I	ST	External interrupt 0.
FLT0				I	ST	Enhanced PWM Fault input (ECCP1 module).
SDI				I	ST	SPI data in.
SDA				I/O	ST	I^2C™ data I/O.
RB1/AN10/INT1/SCK/SCL	34	10	9			
RB1				I/O	TTL	Digital I/O.
AN10				I	Analog	Analog input 10.
INT1				I	ST	External interrupt 1.
SCK				I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL				I/O	ST	Synchronous serial clock input/output for I^2C mode.
RB2/AN8/INT2/VMO	35	11	10			
RB2				I/O	TTL	Digital I/O.
AN8				I	Analog	Analog input 8.
INT2				I	ST	External interrupt 2.
VMO				O	—	External USB transceiver VMO output.
RB3/AN9/CCP2/VPO	36	12	11			
RB3				I/O	TTL	Digital I/O.
AN9				I	Analog	Analog input 9.
CCP2(1)				I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
VPO				O	—	External USB transceiver VPO output.
RB4/AN11/KBI0/CSSPP	37	14	14			
RB4				I/O	TTL	Digital I/O.
AN11				I	Analog	Analog input 11.
KBI0				I	TTL	Interrupt-on-change pin.
CSSPP				O	—	SPP chip select control output.
RB5/KBI1/PGM	38	15	15			
RB5				I/O	TTL	Digital I/O.
KBI1				I	TTL	Interrupt-on-change pin.
PGM				I/O	ST	Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC	39	16	16			
RB6				I/O	TTL	Digital I/O.
KBI2				I	TTL	Interrupt-on-change pin.
PGC				I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	40	17	17			
RB7				I/O	TTL	Digital I/O.
KBI3				I	TTL	Interrupt-on-change pin.
PGD				I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTC is a bidirectional I/O port.
RC0/T1OSO/T13CKI	15	34	32			
RC0				I/O	ST	Digital I/O.
T1OSO				O	—	Timer1 oscillator output.
T13CKI				I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2/ $\overline{UOE}$	16	35	35			
RC1				I/O	ST	Digital I/O.
T1OSI				I	CMOS	Timer1 oscillator input.
CCP2(2)				I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
$\overline{UOE}$				O	—	External USB transceiver $\overline{OE}$ output.
RC2/CCP1/P1A	17	36	36			
RC2				I/O	ST	Digital I/O.
CCP1				I/O	ST	Capture 1 input/Compare 1 output/PWM 1 output.
P1A				O	TTL	Enhanced CCP1 PWM output, channel A.
RC4/D-/VM	23	42	42			
RC4				I	TTL	Digital input.
D-				I/O	—	USB differential minus line (input/output).
VM				I	TTL	External USB transceiver VM input.
RC5/D+/VP	24	43	43			
RC5				I	TTL	Digital input.
D+				I/O	—	USB differential plus line (input/output).
VP				I	TTL	External USB transceiver VP input.
RC6/TX/CK	25	44	44			
RC6				I/O	ST	Digital I/O.
TX				O	—	EUSART asynchronous transmit.
CK				I/O	ST	EUSART synchronous clock (see RX/DT).
RC7/RX/DT/SDO	26	1	1			
RC7				I/O	ST	Digital I/O.
RX				I	ST	EUSART asynchronous receive.
DT				I/O	ST	EUSART synchronous data (see TX/CK).
SDO				O	—	SPI data out.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the $\overline{DEBUG}$ Configuration bit is cleared.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTD is a bidirectional I/O port or a Streaming Parallel Port (SPP). These pins have TTL input buffers when the SPP module is enabled.
RD0/SPP0	19	38	38			
RD0				I/O	ST	Digital I/O.
SPP0				I/O	TTL	Streaming Parallel Port data.
RD1/SPP1	20	39	39			
RD1				I/O	ST	Digital I/O.
SPP1				I/O	TTL	Streaming Parallel Port data.
RD2/SPP2	21	40	40			
RD2				I/O	ST	Digital I/O.
SPP2				I/O	TTL	Streaming Parallel Port data.
RD3/SPP3	22	41	41			
RD3				I/O	ST	Digital I/O.
SPP3				I/O	TTL	Streaming Parallel Port data.
RD4/SPP4	27	2	2			
RD4				I/O	ST	Digital I/O.
SPP4				I/O	TTL	Streaming Parallel Port data.
RD5/SPP5/P1B	28	3	3			
RD5				I/O	ST	Digital I/O.
SPP5				I/O	TTL	Streaming Parallel Port data.
P1B				O	—	Enhanced CCP1 PWM output, channel B.
RD6/SPP6/P1C	29	4	4			
RD6				I/O	ST	Digital I/O.
SPP6				I/O	TTL	Streaming Parallel Port data.
P1C				O	—	Enhanced CCP1 PWM output, channel C.
RD7/SPP7/P1D	30	5	5			
RD7				I/O	ST	Digital I/O.
SPP7				I/O	TTL	Streaming Parallel Port data.
P1D				O	—	Enhanced CCP1 PWM output, channel D.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the $\overline{\text{DEBUG}}$ Configuration bit is cleared.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTE is a bidirectional I/O port.
RE0/AN5/CK1SPP	8	25	25			
RE0				I/O	ST	Digital I/O.
AN5				I	Analog	Analog input 5.
CK1SPP				O	—	SPP clock 1 output.
RE1/AN6/CK2SPP	9	26	26			
RE1				I/O	ST	Digital I/O.
AN6				I	Analog	Analog input 6.
CK2SPP				O	—	SPP clock 2 output.
RE2/AN7/OESPP	10	27	27			
RE2				I/O	ST	Digital I/O.
AN7				I	Analog	Analog input 7.
OESPP				O	—	SPP output enable output.
RE3	—	—	—	—	—	See $\overline{MCLR}$/VPP/RE3 pin.
VSS	12, 31	6, 30, 31	6, 29	P	—	Ground reference for logic and I/O pins.
VDD	11, 32	7, 8, 28, 29	7, 28	P	—	Positive supply for logic and I/O pins.
VUSB	18	37	37	O	—	Internal USB 3.3V voltage regulator output.
NC/ICCK/ICPGC[3]	—	—	12			No Connect or dedicated ICD/ICSP™ port clock.
ICCK				I/O	ST	In-Circuit Debugger clock.
ICPGC				I/O	ST	ICSP programming clock.
NC/ICDT/ICPGD[3]	—	—	13			No Connect or dedicated ICD/ICSP port clock.
ICDT				I/O	ST	In-Circuit Debugger data.
ICPGD				I/O	ST	ICSP programming data.
NC/$\overline{ICRST}$/ICVPP[3]	—	—	33			No Connect or dedicated ICD/ICSP port Reset.
$\overline{ICRST}$				I	—	Master Clear (Reset) input.
ICVPP				P	—	Programming voltage input.
NC/ICPORTS[3]	—	—	34	P	—	No Connect or 28-pin device emulation.
ICPORTS						Enable 28-pin device emulation when connected to VSS.
NC	—	13	—	—	—	No Connect.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

2.0 OSCILLATOR CONFIGURATIONS

2.1 Overview

Devices in the PIC18F2455/2550/4455/4550 family incorporate a different oscillator and microcontroller clock system than previous PIC18F devices. The addition of the USB module, with its unique requirements for a stable clock source, make it necessary to provide a separate clock source that is compliant with both USB low-speed and full-speed specifications.

To accommodate these requirements, PIC18F2455/2550/4455/4550 devices include a new clock branch to provide a 48 MHz clock for full-speed USB operation. Since it is driven from the primary clock source, an additional system of prescalers and postscalers has been added to accommodate a wide range of oscillator frequencies. An overview of the oscillator structure is shown in Figure 2-1.

Other oscillator features used in PIC18 enhanced microcontrollers, such as the internal oscillator block and clock switching, remain the same. They are discussed later in this chapter.

2.1.1 OSCILLATOR CONTROL

The operation of the oscillator in PIC18F2455/2550/4455/4550 devices is controlled through two Configuration registers and two control registers. Configuration registers, CONFIG1L and CONFIG1H, select the oscillator mode and USB prescaler/postscaler options. As Configuration bits, these are set when the device is programmed and left in that configuration until the device is reprogrammed.

The OSCCON register (Register 2-2) selects the Active Clock mode; it is primarily used in controlling clock switching in power-managed modes. Its use is discussed in **Section 2.4.1 "Oscillator Control Register"**.

The OSCTUNE register (Register 2-1) is used to trim the INTRC frequency source, as well as select the low-frequency clock source that drives several special features. Its use is described in **Section 2.2.6.2 "OSCTUNE Register"**.

2.2 Oscillator Types

PIC18F2455/2550/4455/4550 devices can be operated in twelve distinct oscillator modes. In contrast with previous PIC18 enhanced microcontrollers, four of these modes involve the use of two oscillator types at once. Users can program the FOSC3:FOSC0 Configuration bits to select one of these modes:

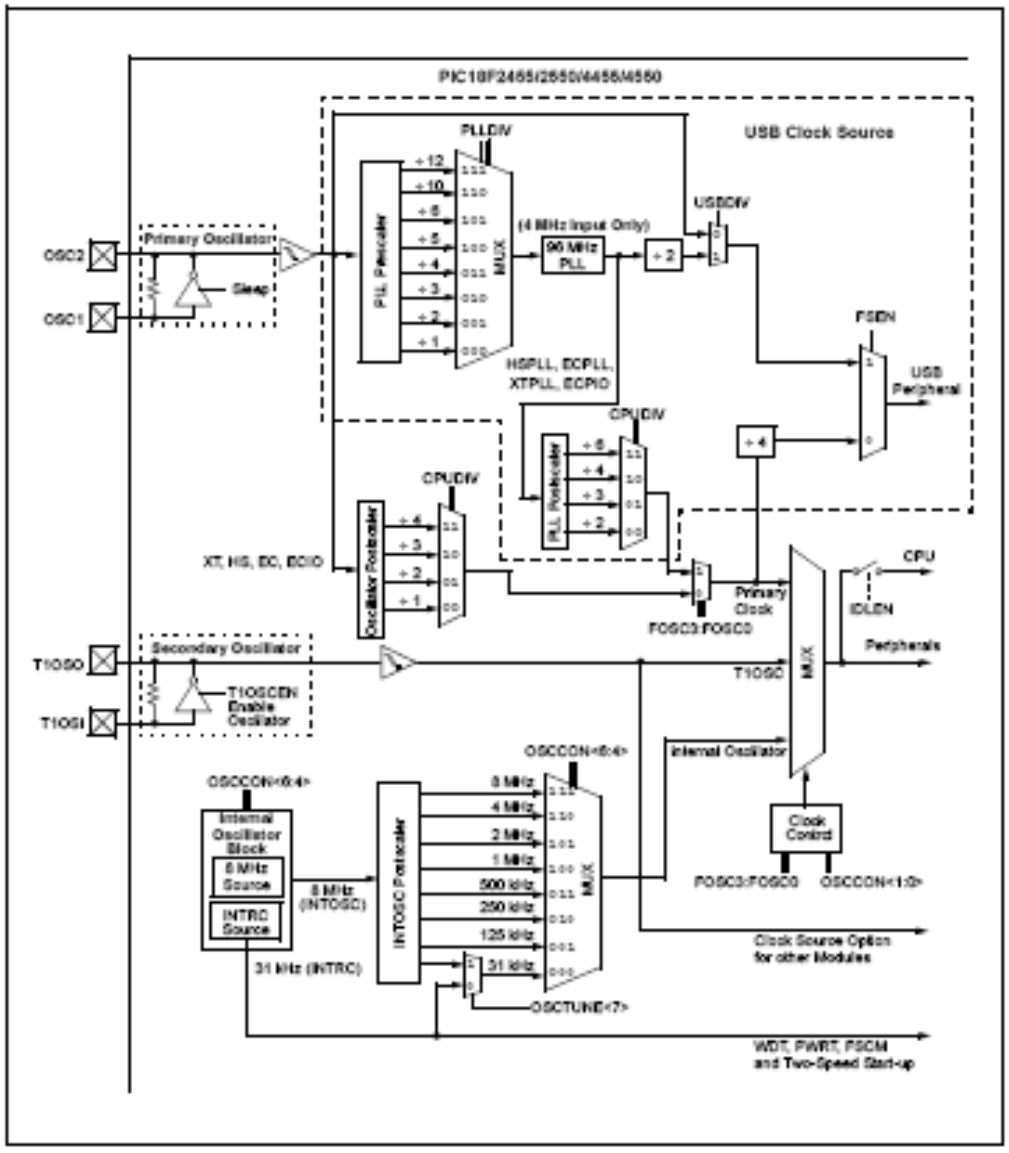
1. XT Crystal/Resonator
2. XTPLL Crystal/Resonator with PLL enabled
3. HS High-Speed Crystal/Resonator
4. HSPLL High-Speed Crystal/Resonator with PLL enabled
5. EC External Clock with Fosc/4 output
6. ECIO External Clock with I/O on RA6
7. ECPLL External Clock with PLL enabled and Fosc/4 output on RA6
8. ECPIO External Clock with PLL enabled, I/O on RA6
9. INTHS Internal Oscillator used as microcontroller clock source, HS Oscillator used as USB clock source
10. INTXT Internal Oscillator used as microcontroller clock source, XT Oscillator used as USB clock source
11. INTIO Internal Oscillator used as microcontroller clock source, EC Oscillator used as USB clock source, digital I/O on RA6
12. INTCKO Internal Oscillator used as microcontroller clock source, EC Oscillator used as USB clock source, Fosc/4 output on RA6

2.2.1 OSCILLATOR MODES AND USB OPERATION

Because of the unique requirements of the USB module, a different approach to clock operation is necessary. In previous PIC® devices, all core and peripheral clocks were driven by a single oscillator source; the usual sources were primary, secondary or the internal oscillator. With PIC18F2455/2550/4455/4550 devices, the primary oscillator becomes part of the USB module and cannot be associated to any other clock source. Thus, the USB module must be clocked from the primary clock source; however, the microcontroller core and other peripherals can be separately clocked from the secondary or internal oscillators as before.

Because of the timing requirements imposed by USB, an internal clock of either 6 MHz or 48 MHz is required while the USB module is enabled. Fortunately, the microcontroller and other peripherals are not required to run at this clock speed when using the primary oscillator. There are numerous options to achieve the USB module clock requirement and still provide flexibility for clocking the rest of the device from the primary oscillator source. These are detailed in **Section 2.3 "Oscillator Settings for USB"**.

FIGURE 2-1: PIC18F2455/2550/4455/4550 CLOCK DIAGRAM



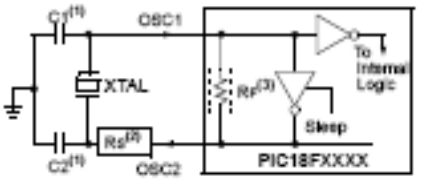
2.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In HS, HSPLL, XT and XTPLL Oscillator modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation. Figure 2-2 shows the pin connections.

The oscillator design requires the use of a parallel cut crystal.

Note:	Use of a series cut crystal may give a frequency out of the crystal manufacturer's specifications.

FIGURE 2-2: CRYSTAL/CERAMIC RESONATOR OPERATION (XT, HS OR HSPLL CONFIGURATION)



Note 1: See Table 2-1 and Table 2-2 for initial values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.
3: RF varies with the oscillator mode chosen.

TABLE 2-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Typical Capacitor Values Used:			
Mode	Freq	OSC1	OSC2
XT	4.0 MHz	33 pF	33 pF
HS	8.0 MHz	27 pF	27 pF
	16.0 MHz	22 pF	22 pF
Capacitor values are for design guidance only.			
These capacitors were tested with the resonators listed below for basic start-up and operation. **These values are not optimized.**			
Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.			
See the notes following Table 2-2 for additional information.			
Resonators Used:			
4.0 MHz			
8.0 MHz			
16.0 MHz			

TABLE 2-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

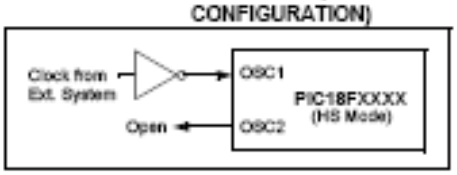
Osc Type	Crystal Freq	Typical Capacitor Values Tested:	
		C1	C2
XT	4 MHz	27 pF	27 pF
HS	4 MHz	27 pF	27 pF
	8 MHz	22 pF	22 pF
	20 MHz	15 pF	15 pF
Capacitor values are for design guidance only.			
These capacitors were tested with the crystals listed below for basic start-up and operation. **These values are not optimized.**			
Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.			
See the notes following this table for additional information.			
Crystals Used:			
4 MHz			
8 MHz			
20 MHz			

Note 1:	Higher capacitance increases the stability of oscillator but also increases the start-up time.
2:	When operating below 3V VDD, or when using certain ceramic resonators at any voltage, it may be necessary to use the HS mode or switch to a crystal oscillator.
3:	Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
4:	RS may be required to avoid overdriving crystals with low drive level specification.
5:	Always verify oscillator performance over the VDD and temperature range that is expected for the application.

An internal postscaler allows users to select a clock frequency other than that of the crystal or resonator. Frequency division is determined by the CPUDIV Configuration bits. Users may select a clock frequency of the oscillator frequency, or 1/2, 1/3 or 1/4 of the frequency.

An external clock may also be used when the microcontroller is in HS Oscillator mode. In this case, the OSC2/CLKO pin is left open (Figure 2-3).

FIGURE 2-3: EXTERNAL CLOCK INPUT OPERATION (HS OSC CONFIGURATION)

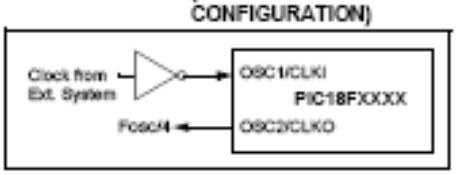


2.2.3 EXTERNAL CLOCK INPUT

The EC, ECIO, ECPLL and ECPIO Oscillator modes require an external clock source to be connected to the OSC1 pin. There is no oscillator start-up time required after a Power-on Reset or after an exit from Sleep mode.

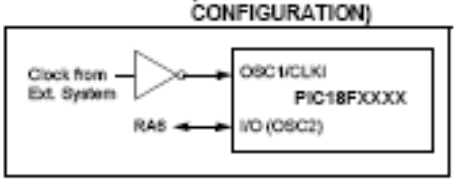
In the EC and ECPLL Oscillator modes, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic. Figure 2-4 shows the pin connections for the EC Oscillator mode.

FIGURE 2-4: EXTERNAL CLOCK INPUT OPERATION (EC AND ECPLL CONFIGURATION)



The ECIO and ECPIO Oscillator modes function like the EC and ECPLL modes, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6). Figure 2-5 shows the pin connections for the ECIO Oscillator mode.

FIGURE 2-5: EXTERNAL CLOCK INPUT OPERATION (ECIO AND ECPIO CONFIGURATION)



The internal postscaler for reducing clock frequency in XT and HS modes is also available in EC and ECIO modes.

2.2.4 PLL FREQUENCY MULTIPLIER

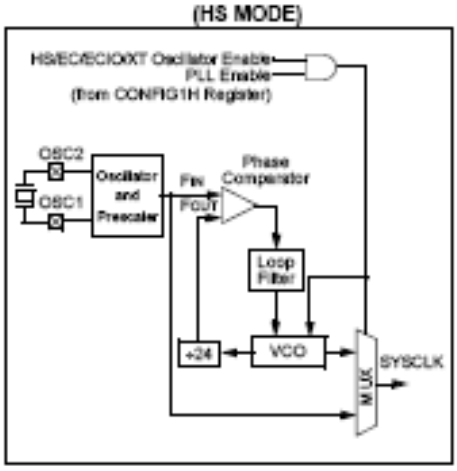
PIC18F2455/2550/4455/4550 devices include a Phase Locked Loop (PLL) circuit. This is provided specifically for USB applications with lower speed oscillators and can also be used as a microcontroller clock source.

The PLL is enabled in HSPLL, XTPLL, ECPLL and ECPIO Oscillator modes. It is designed to produce a fixed 96 MHz reference clock from a fixed 4 MHz input. The output can then be divided and used for both the USB and the microcontroller core clock. Because the PLL has a fixed frequency input and output, there are eight prescaling options to match the oscillator input frequency to the PLL.

There is also a separate postscaler option for deriving the microcontroller clock from the PLL. This allows the USB peripheral and microcontroller to use the same oscillator input and still operate at different clock speeds. In contrast to the postscaler for XT, HS and EC modes, the available options are 1/2, 1/3, 1/4 and 1/6 of the PLL output.

The HSPLL, ECPLL and ECPIO modes make use of the HS mode oscillator for frequencies up to 48 MHz. The prescaler divides the oscillator input by up to 12 to produce the 4 MHz drive for the PLL. The XTPLL mode can only use an input frequency of 4 MHz which drives the PLL directly.

FIGURE 2-6: PLL BLOCK DIAGRAM (HS MODE)



4.0 RESET

The PIC18F2455/2550/4455/4550 devices differentiate between various kinds of Reset:

a) Power-on Reset (POR)
b) MCLR Reset during normal operation
c) MCLR Reset during power-managed modes
d) Watchdog Timer (WDT) Reset (during execution)
e) Programmable Brown-out Reset (BOR)
f) RESET Instruction
g) Stack Full Reset
h) Stack Underflow Reset

This section discusses Resets generated by MCLR, POR and BOR and covers the operation of the various start-up timers. Stack Reset events are covered in **Section 6.1.2.4 "Stack Full and Underflow Resets"**. WDT Resets are covered in **Section 25.2 "Watchdog Timer (WDT)"**.

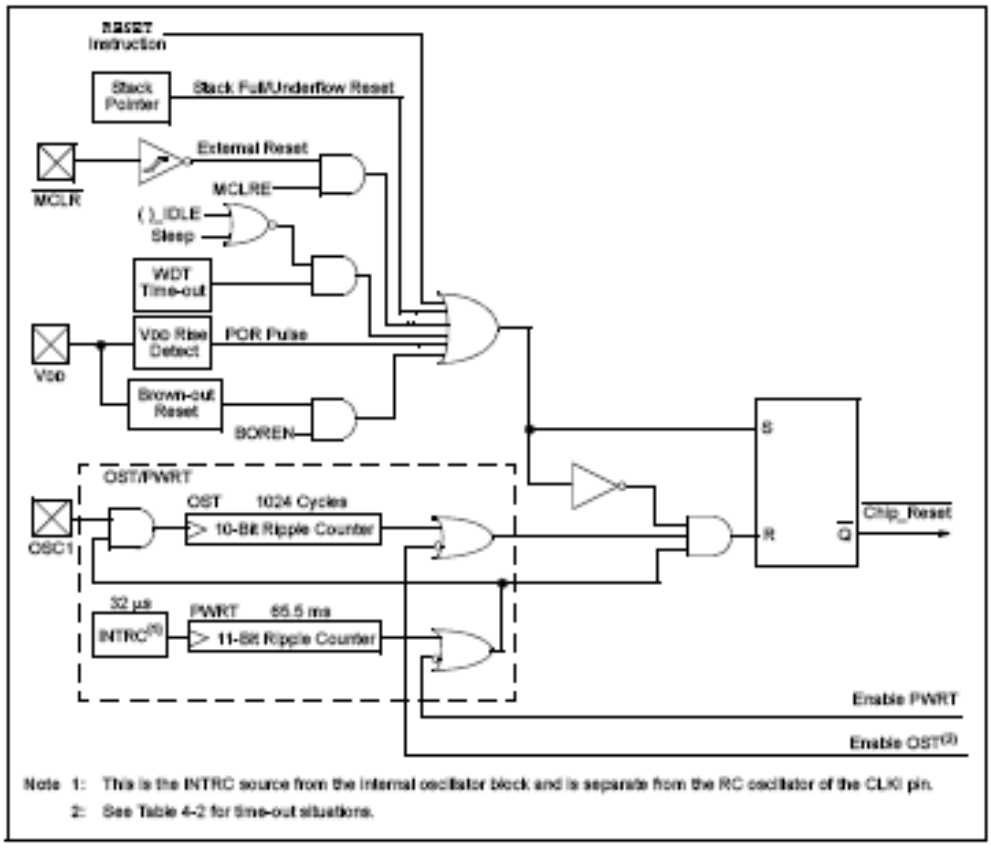
A simplified block diagram of the on-chip Reset circuit is shown in Figure 4-1.

4.1 RCON Register

Device Reset events are tracked through the RCON register (Register 4-1). The lower five bits of the register indicate that a specific Reset event has occurred. In most cases, these bits can only be cleared by the event and must be set by the application after the event. The state of these flag bits, taken together, can be read to indicate the type of Reset that just occurred. This is described in more detail in **Section 4.6 "Reset State of Registers"**.

The RCON register also has control bits for setting interrupt priority (IPEN) and software control of the BOR (SBOREN). Interrupt priority is discussed in **Section 9.0 "Interrupts"**. BOR is covered in **Section 4.4 "Brown-out Reset (BOR)"**.

FIGURE 4-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: This is the INTRC source from the internal oscillator block and is separate from the RC oscillator of the CLKI pin.
2: See Table 4-2 for time-out situations.

4.2 Master Clear Reset (MCLR)

The MCLR pin provides a method for triggering an external Reset of the device. A Reset is generated by holding the pin low. These devices have a noise filter in the MCLR Reset path which detects and ignores small pulses.

The MCLR pin is not driven low by any internal Resets, including the WDT.

In PIC18F2455/2550/4455/4550 devices, the MCLR input can be disabled with the MCLRE Configuration bit. When MCLR is disabled, the pin becomes a digital input. See **Section 10.5 "PORTE, TRISE and LATE Registers"** for more information.

4.3 Power-on Reset (POR)

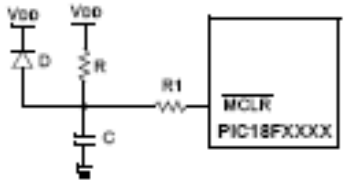
A Power-on Reset pulse is generated on-chip whenever VDD rises above a certain threshold. This allows the device to start in the initialized state when VDD is adequate for operation.

To take advantage of the POR circuitry, tie the MCLR pin through a resistor (1 kΩ to 10 kΩ) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset delay. A minimum rise rate for VDD is specified (parameter D004, **Section 28.1 "DC Characteristics"**). For a slow rise time, see Figure 4-2.

When the device starts normal operation (i.e., exits the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

POR events are captured by the POR bit (RCON<1>). The state of the bit is set to '0' whenever a POR occurs; it does not change for any other Reset event. POR is not reset to '1' by any hardware event. To capture multiple events, the user manually resets the bit to '1' in software following any POR.

FIGURE 4-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



Note 1: External Power-on Reset circuit is required only if the VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

2: R < 40 kΩ is recommended to make sure that the voltage drop across R does not violate the device's electrical specification.

3: R1 ≥ 1 kΩ will limit any current flowing into MCLR from external capacitor C, in the event of MCLR/VPP pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

5.0 MEMORY ORGANIZATION

There are three types of memory in PIC18 enhanced microcontroller devices:

- Program Memory
- Data RAM
- Data EEPROM

As Harvard architecture devices, the data and program memories use separate busses; this allows for concurrent access of the two memory spaces. The data EEPROM, for practical purposes, can be regarded as a peripheral device, since it is addressed and accessed through a set of control registers.

Additional detailed information on the operation of the Flash program memory is provided in **Section 6.0 "Flash Program Memory"**. Data EEPROM is discussed separately in **Section 7.0 "Data EEPROM Memory"**.

5.1 Program Memory Organization

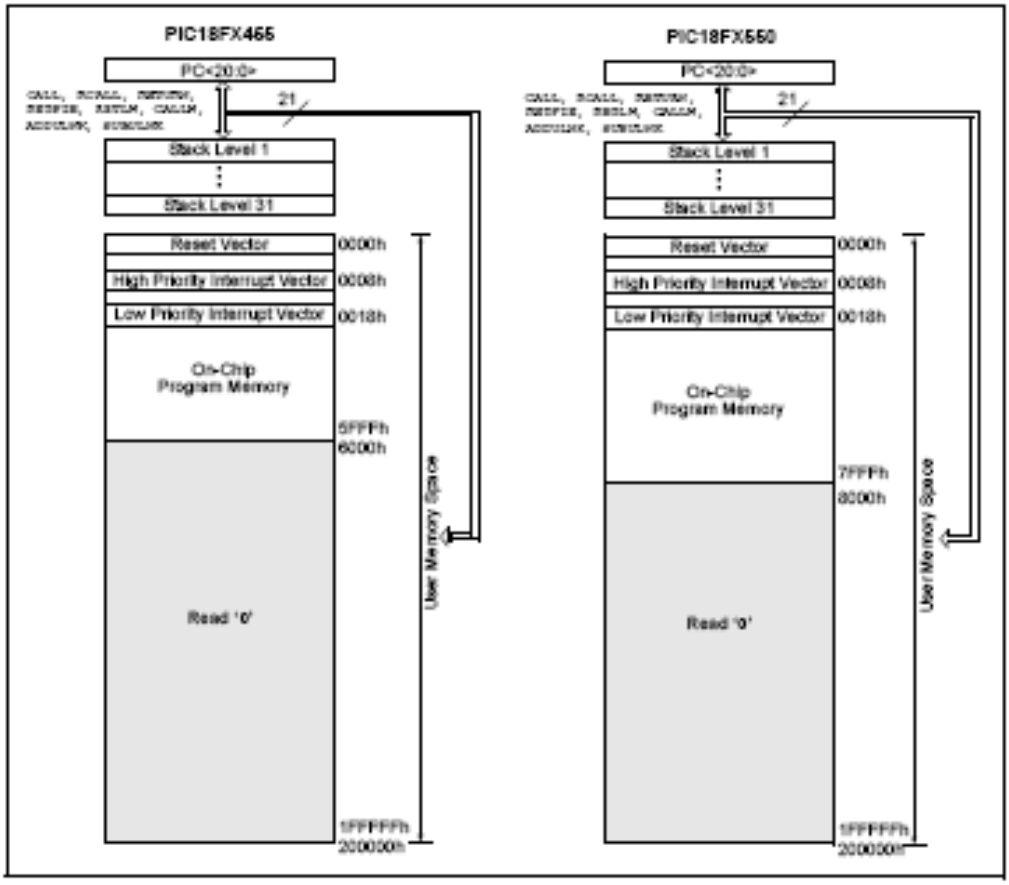
PIC18 microcontrollers implement a 21-bit program counter which is capable of addressing a 2-Mbyte program memory space. Accessing a location between the upper boundary of the physically implemented memory and the 2-Mbyte address will return all '0's (a NOP instruction).

The PIC18F2455 and PIC18F4455 each have 24 Kbytes of Flash memory and can store up to 12,288 single-word instructions. The PIC18F2550 and PIC18F4550 each have 32 Kbytes of Flash memory and can store up to 16,384 single-word instructions.

PIC18 devices have two interrupt vectors. The Reset vector address is at 0000h and the interrupt vector addresses are at 0008h and 0018h.

The program memory maps for PIC18FX455 and PIC18FX550 devices are shown in Figure 5-1.

FIGURE 5-1: PROGRAM MEMORY MAP AND STACK FOR PIC18F2455/2550/4455/4550 DEVICES



5.1.1 PROGRAM COUNTER

The Program Counter (PC) specifies the address of the instruction to fetch for execution. The PC is 21 bits wide and is contained in three separate 8-bit registers. The low byte, known as the PCL register, is both readable and writable. The high byte, or PCH register, contains the PC<15:8> bits; it is not directly readable or writable. Updates to the PCH register are performed through the PCLATH register. The upper byte is called PCU. This register contains the PC<20:16> bits; it is also not directly readable or writable. Updates to the PCU register are performed through the PCLATU register.

The contents of PCLATH and PCLATU are transferred to the program counter by any operation that writes PCL. Similarly, the upper two bytes of the program counter are transferred to PCLATH and PCLATU by an operation that reads PCL. This is useful for computed offsets to the PC (see **Section 5.1.4.1 "Computed GOTO"**).

The PC addresses bytes in the program memory. To prevent the PC from becoming misaligned with word instructions, the Least Significant bit of PCL is fixed to a value of '0'. The PC increments by 2 to address sequential instructions in the program memory.

The CALL, RCALL and GOTO program branch instructions write to the program counter directly. For these instructions, the contents of PCLATH and PCLATU are not transferred to the program counter.

5.1.2 RETURN ADDRESS STACK

The return address stack allows any combination of up to 31 program calls and interrupts to occur. The PC is pushed onto the stack when a CALL or RCALL instruction is executed or an interrupt is Acknowledged. The PC value is pulled off the stack on a RETURN, RETLW or a RETFIE instruction. PCLATU and PCLATH are not affected by any of the RETURN or CALL instructions.

The stack operates as a 31-word by 21-bit RAM and a 5-bit Stack Pointer, STKPTR. The stack space is not part of either program or data space. The Stack Pointer is readable and writable and the address on the top of the stack is readable and writable through the Top-of-Stack Special Function Registers. Data can also be pushed to, or popped from the stack, using these registers.

A CALL type instruction causes a push onto the stack. The Stack Pointer is first incremented and the location pointed to by the Stack Pointer is written with the contents of the PC (already pointing to the instruction following the CALL). A RETURN type instruction causes a pop from the stack. The contents of the location pointed to by the STKPTR are transferred to the PC and then the Stack Pointer is decremented.

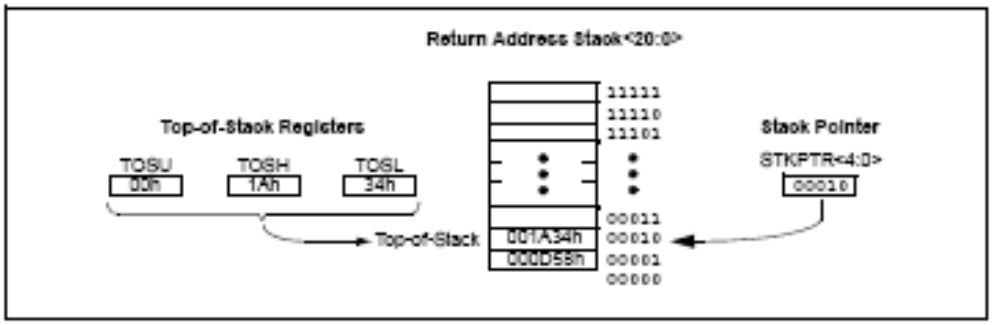
The Stack Pointer is initialized to '00000' after all Resets. There is no RAM associated with the location corresponding to a Stack Pointer value of '00000'; this is only a Reset value. Status bits indicate if the stack is full, has overflowed or has underflowed.

5.1.2.1 Top-of-Stack Access

Only the top of the return address stack (TOS) is readable and writable. A set of three registers, TOSU:TOSH:TOSL, hold the contents of the stack location pointed to by the STKPTR register (Figure 5-2). This allows users to implement a software stack if necessary. After a CALL, RCALL or interrupt, the software can read the pushed value by reading the TOSU:TOSH:TOSL registers. These values can be placed on a user-defined software stack. At return time, the software can return these values to TOSU:TOSH:TOSL and do a return.

The user must disable the global interrupt enable bits while accessing the stack to prevent inadvertent stack corruption.

FIGURE 5-2: RETURN ADDRESS STACK AND ASSOCIATED REGISTERS



5.2 PIC18 Instruction Cycle

5.2.1 CLOCKING SCHEME

The microcontroller clock input, whether from an internal or external source, is internally divided by four to generate four non-overlapping quadrature clocks (Q1, Q2, Q3 and Q4). Internally, the program counter is incremented on every Q1; the instruction is fetched from the program memory and latched into the Instruction Register (IR) during Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 5-3.

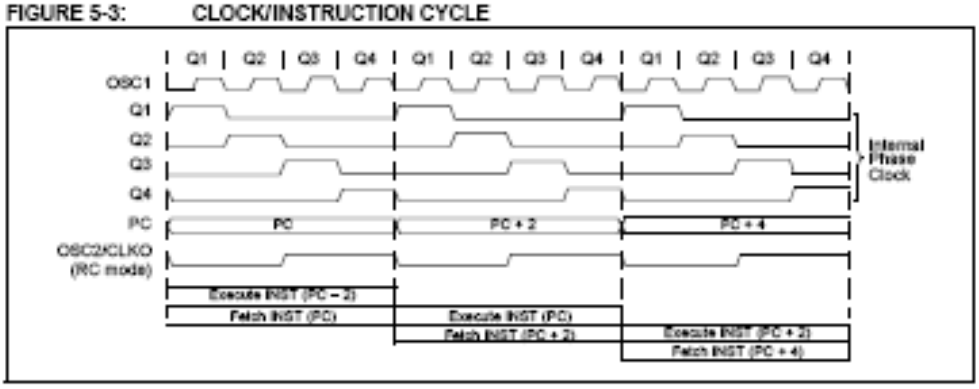
5.2.2 INSTRUCTION FLOW/PIPELINING

An "Instruction Cycle" consists of four Q cycles: Q1 through Q4. The instruction fetch and execute are pipelined in such a manner that a fetch takes one instruction cycle, while the decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 5-3).

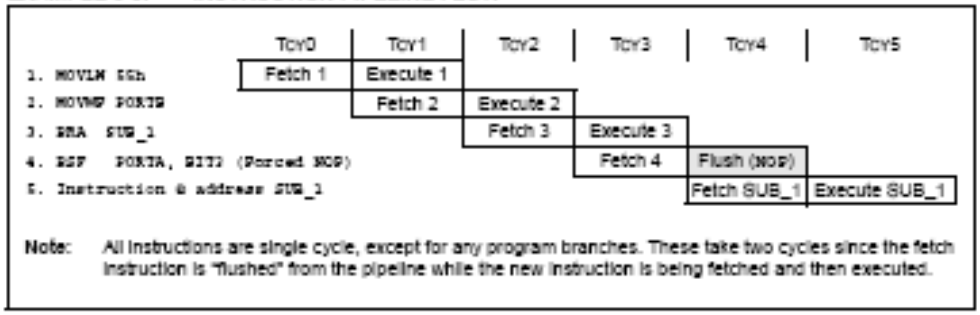
A fetch cycle begins with the Program Counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 5-3: CLOCK/INSTRUCTION CYCLE



EXAMPLE 5-3: INSTRUCTION PIPELINE FLOW



Note: All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

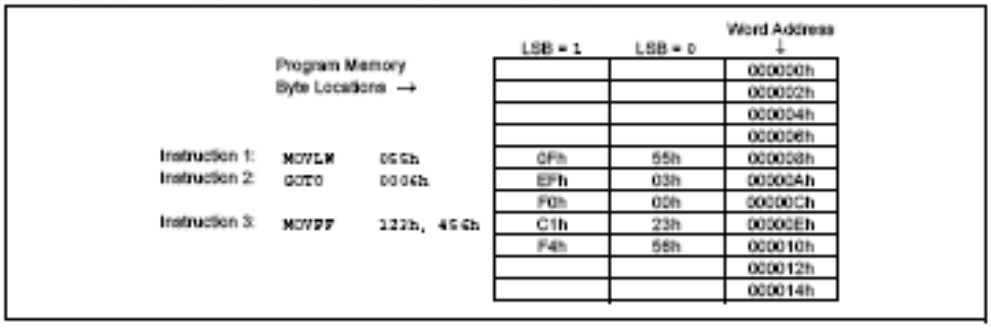
5.2.3 INSTRUCTIONS IN PROGRAM MEMORY

The program memory is addressed in bytes. Instructions are stored as two bytes or four bytes in program memory. The Least Significant Byte of an instruction word is always stored in a program memory location with an even address (LSb = 0). To maintain alignment with instruction boundaries, the PC increments in steps of 2 and the LSb will always read '0' (see **Section 6.1.1 "Program Counter"**).

Figure 5-4 shows an example of how instruction words are stored in the program memory.

The CALL and GOTO instructions have the absolute program memory address embedded into the instruction. Since instructions are always stored on word boundaries, the data contained in the instruction is a word address. The word address is written to PC<20:1>, which accesses the desired byte address in program memory. Instruction #2 in Figure 5-4 shows how the instruction, GOTO 0006h, is encoded in the program memory. Program branch instructions, which encode a relative address offset, operate in the same manner. The offset value stored in a branch instruction represents the number of single-word instructions that the PC will be offset by. **Section 28.0 "Instruction Set Summary"** provides further details of the instruction set.

FIGURE 5-4: INSTRUCTIONS IN PROGRAM MEMORY



5.2.4 TWO-WORD INSTRUCTIONS

The standard PIC18 instruction set has four two-word instructions: CALL, MOVFF, GOTO and LSFR. In all cases, the second word of the instructions always has '1111' as its four Most Significant bits; the other 12 bits are literal data, usually a data memory address.

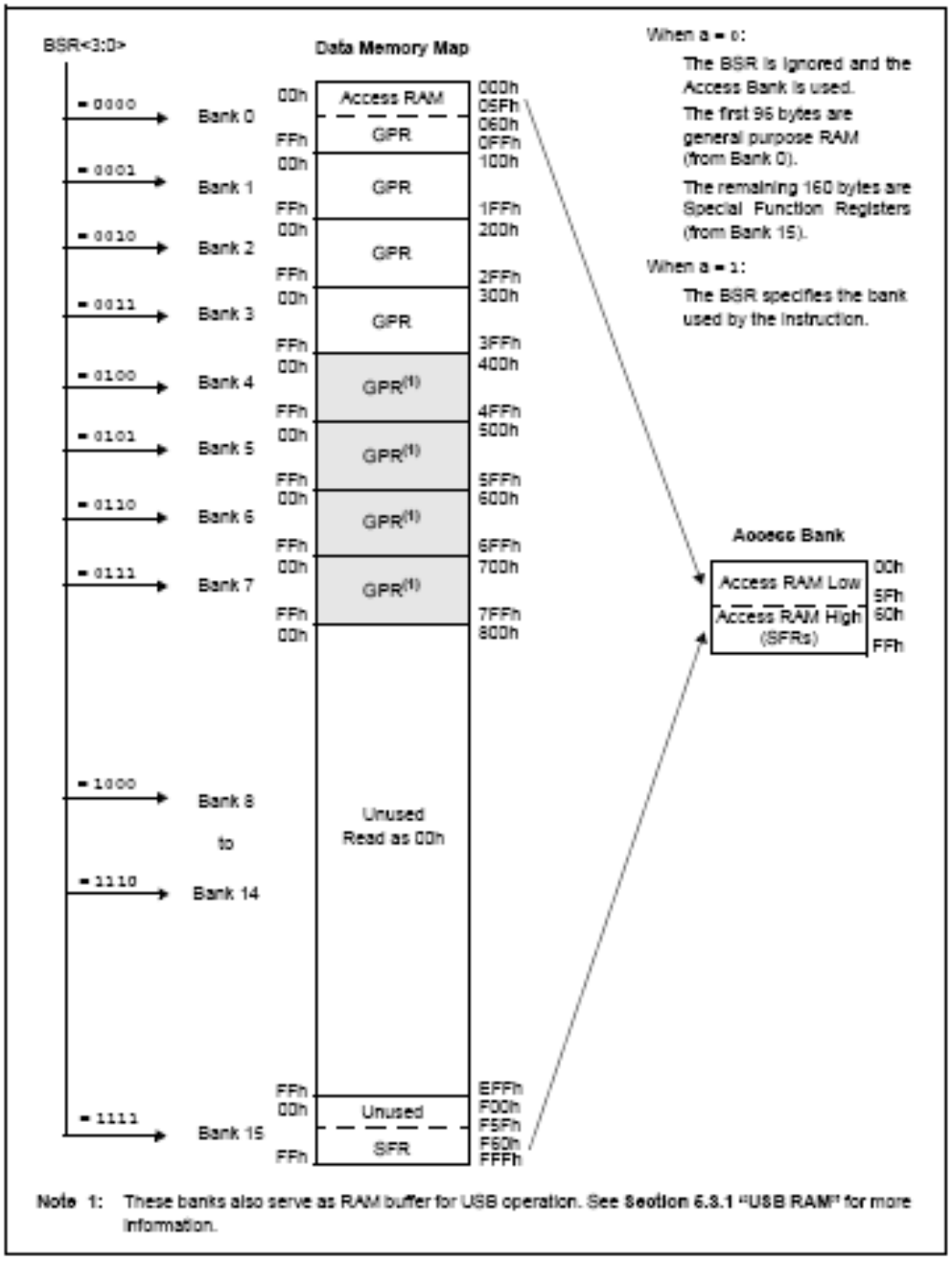
The use of '1111' in the 4 MSbs of an instruction specifies a special form of NOP. If the instruction is executed in proper sequence, immediately after the first word, the data in the second word is accessed and used by the instruction sequence. If the first word is skipped for some reason and the second word is executed by itself, a NOP is executed instead. This is necessary for cases when the two-word instruction is preceded by a conditional instruction that changes the PC. Example 5-4 shows how this works.

Note:	See **Section 6.5 "Program Memory and the Extended Instruction Set"** for information on two-word instruction in the extended instruction set.

EXAMPLE 5-4: TWO-WORD INSTRUCTIONS

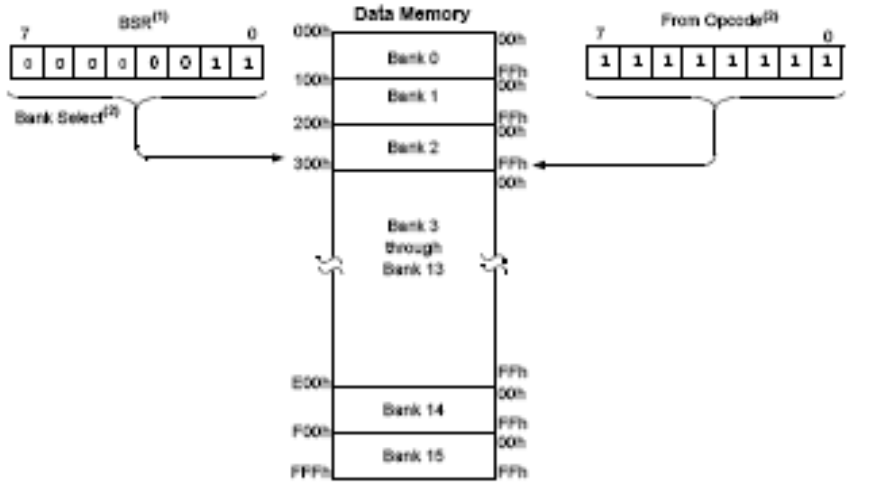
CASE 1:			
Object Code	**Source Code**		
0110 0110 0000 0000	TSTFSZ	REG1	; is RAM location 0?
1100 0001 0010 0011	MOVFF	REG1, REG2	; No, skip this word
1111 0100 0101 0110			; Execute this word as a NOP
0010 0100 0000 0000	ADDWF	REG1	; continue code
CASE 2:			
Object Code	**Source Code**		
0110 0110 0000 0000	TSTFSZ	REG1	; is RAM location 0?
1100 0001 0010 0011	MOVFF	REG1, REG2	; Yes, execute this word
1111 0100 0101 0110			; 2nd word of instruction
0010 0100 0000 0000	ADDWF	REG1	; continue code

FIGURE 5-5: DATA MEMORY MAP FOR PIC18F2455/2550/4455/4550 DEVICES



Note 1: These banks also serve as RAM buffer for USB operation. See Section 6.8.1 "USB RAM" for more information.

FIGURE 5-6: USE OF THE BANK SELECT REGISTER (DIRECT ADDRESSING)



Note 1: The Access RAM bit of the instruction can be used to force an override of the selected bank (BSR<3:0>) to the registers of the Access Bank.

2: The MOVFF instruction embeds the entire 12-bit address in the instruction.

5.3.3 ACCESS BANK

While the use of the BSR, with an embedded 8-bit address, allows users to address the entire range of data memory, it also means that the user must always ensure that the correct bank is selected. Otherwise, data may be read from or written to the wrong location. This can be disastrous if a GPR is the intended target of an operation but an SFR is written to instead. Verifying and/or changing the BSR for each read or write to data memory can become very inefficient.

To streamline access for the most commonly used data memory locations, the data memory is configured with an Access Bank, which allows users to access a mapped block of memory without specifying a BSR. The Access Bank consists of the first 96 bytes of memory (000h-5Fh) in Bank 0 and the last 160 bytes of memory (60h-FFh) in Block 15. The lower half is known as the "Access RAM" and is composed of GPRs. The upper half is where the device's SFRs are mapped. These two areas are mapped contiguously in the Access Bank and can be addressed in a linear fashion by an 8-bit address (Figure 5-5).

The Access Bank is used by core PIC18 instructions that include the Access RAM bit (the 'a' parameter in the instruction). When 'a' is equal to '1', the instruction uses the BSR and the 8-bit address included in the opcode for the data memory address. When 'a' is '0', however, the instruction is forced to use the Access Bank address map; the current value of the BSR is ignored entirely.

Using this "forced" addressing allows the instruction to operate on a data address in a single cycle without updating the BSR first. For 8-bit addresses of 60h and above, this means that users can evaluate and operate on SFRs more efficiently. The Access RAM below 60h is a good place for data values that the user might need to access rapidly, such as immediate computational results or common program variables. Access RAM also allows for faster and more code efficient context saving and switching of variables.

The mapping of the Access Bank is slightly different when the extended instruction set is enabled (XINST Configuration bit = 1). This is discussed in more detail in **Section 5.6.3 "Mapping the Access Bank in Indexed Literal Offset Mode"**.

5.3.4 GENERAL PURPOSE REGISTER FILE

PIC18 devices may have banked memory in the GPR area. This is data RAM which is available for use by all instructions. GPRs start at the bottom of Bank 0 (address 000h) and grow upwards towards the bottom of the SFR area. GPRs are not initialized by a Power-on Reset and are unchanged on all other Resets.

10.0 I/O PORTS

Depending on the device selected and features enabled, there are up to five ports available. Some pins of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

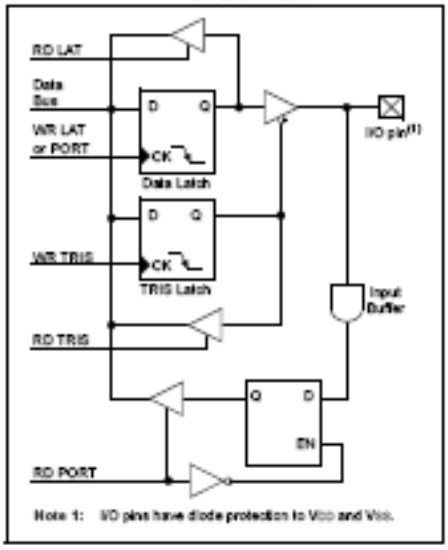
Each port has three registers for its operation. These registers are:

- TRIS register (data direction register)
- PORT register (reads the levels on the pins of the device)
- LAT register (output latch)

The Data Latch register (LATA) is useful for read-modify-write operations on the value driven by the I/O pins.

A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 10-1.

FIGURE 10-1: GENERIC I/O PORT OPERATION



Note 1: I/O pins have diode protection to VDD and VSS.

10.1 PORTA, TRISA and LATA Registers

PORTA is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins; writing to it will write to the port latch.

The Data Latch register (LATA) is also memory mapped. Read-modify-write operations on the LATA register read and write the latched output value for PORTA.

The RA4 pin is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA6 pin is multiplexed with the main oscillator pin; it is enabled as an oscillator or I/O pin by the selection of the main oscillator in Configuration Register 1H (see **Section 25.1 "Configuration Bits"** for details). When not used as a port pin, RA6 and its associated TRIS and LAT bits are read as '0'.

RA4 is also multiplexed with the USB module; it serves as a receiver input from an external USB transceiver. For details on configuration of the USB module, see **Section 17.2 "USB Status and Control"**.

Several PORTA pins are multiplexed with analog inputs, the analog VREF+ and VREF- inputs and the comparator voltage reference output. The operation of pins RA5 and RA3:RA0 as A/D converter inputs is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register 1).

Note:	On a Power-on Reset, RA5 and RA3:RA0 are configured as analog inputs and read as '0'. RA4 is configured as a digital input.

All other PORTA pins have TTL input levels and full CMOS output drivers.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE 10-1: INITIALIZING PORTA

```
CLRF    PORTA   ; Initialize PORTA by
                ; clearing output
                ; data latches
CLRF    LATA    ; Alternate method
                ; to clear output
                ; data latches
MOVLW   0Fh     ; Configure A/D
MOVWF   ADCON1  ; for digital inputs
MOVLW   07h     ; Configure comparators
MOVWF   CMCON   ; for digital input
MOVLW   0CFh    ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISA   ; Set RA<3:0> as inputs
                ; RA<5:4> as outputs
```

TABLE 10-1: PORTA I/O SUMMARY

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RA0/AN0	RA0	0	OUT	DIG	LATA<0> data output; not affected by analog input.
		1	IN	TTL	PORTA<0> data input; disabled when analog input enabled.
	AN0	1	IN	ANA	A/D input channel 0 and Comparator C1- input. Default configuration on POR; does not affect digital output.
RA1/AN1	RA1	0	OUT	DIG	LATA<1> data output; not affected by analog input.
		1	IN	TTL	PORTA<1> data input; reads '0' on POR.
	AN1	1	IN	ANA	A/D input channel 1 and Comparator C2- input. Default configuration on POR; does not affect digital output.
RA2/AN2/ VREF-/CVREF	RA2	0	OUT	DIG	LATA<2> data output; not affected by analog input. Disabled when CVREF output enabled.
		1	IN	TTL	PORTA<2> data input. Disabled when analog functions enabled; disabled when CVREF output enabled.
	AN2	1	IN	ANA	A/D input channel 2 and Comparator C2+ input. Default configuration on POR; not affected by analog output.
	VREF-	1	IN	ANA	A/D and comparator voltage reference low input.
	CVREF	x	OUT	ANA	Comparator voltage reference output. Enabling this feature disables digital I/O.
RA3/AN3/ VREF+	RA3	0	OUT	DIG	LATA<3> data output; not affected by analog input.
		1	IN	TTL	PORTA<3> data input; disabled when analog input enabled.
	AN3	1	IN	ANA	A/D input channel 3 and Comparator C1+ input. Default configuration on POR.
	VREF+	1	IN	ANA	A/D and comparator voltage reference high input.
RA4/T0CKI/ C1OUT/RCV	RA4	0	OUT	DIG	LATA<4> data output; not affected by analog input.
		1	IN	ST	PORTA<4> data input; disabled when analog input enabled.
	T0CKI	1	IN	ST	Timer0 clock input.
	C1OUT	0	OUT	DIG	Comparator 1 output; takes priority over port data.
	RCV	x	IN	TTL	External USB transceiver RCV input.
RA5/AN4/$\overline{SS}$/ HLVDIN/C2OUT	RA5	0	OUT	DIG	LATA<5> data output; not affected by analog input.
		1	IN	TTL	PORTA<5> data input; disabled when analog input enabled.
	AN4	1	IN	ANA	A/D input channel 4. Default configuration on POR.
	$\overline{SS}$	1	IN	TTL	Slave select input for SSP (MSSP module).
	HLVDIN	1	IN	ANA	High/Low-Voltage Detect external trip point input.
	C2OUT	0	OUT	DIG	Comparator 2 output; takes priority over port data.
OSC2/CLKO/ RA6	OSC2	x	OUT	ANA	Main oscillator feedback output connection (all XT and HS modes).
	CLKO	x	OUT	DIG	System cycle clock output (FOSC/4); available in EC, ECPLL and INTCKO modes.
	RA6	0	OUT	DIG	LATA<6> data output. Available only in ECIO, ECPIO and INTIO modes; otherwise, reads as '0'.
		1	IN	TTL	PORTA<6> data input. Available only in ECIO, ECPIO and INTIO modes; otherwise, reads as '0'.

Legend: OUT = Output, IN = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option)

10.2 PORTB, TRISB and LATB Registers

PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

The Data Latch register (LATB) is also memory mapped. Read-modify-write operations on the LATB register read and write the latched output value for PORTB.

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit, RBPU (INTCON2<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Note:	On a Power-on Reset, RB4:RB0 are configured as analog inputs by default and read as '0'; RB7:RB5 are configured as digital inputs. By programming the Configuration bit, PBADEN (CONFIG3H<1>), RB4:RB0 will alternatively be configured as digital inputs on POR.

Four of the PORTB pins (RB7:RB4) have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur. Any RB7:RB4 pin configured as an output is excluded from the interrupt-on-change comparison. The pins are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are ORed together to generate the RB Port Change Interrupt with Flag bit, RBIF (INTCON<0>).

The interrupt-on-change can be used to wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB (except with the `MOVFF (ANY), PORTB` instruction). This will end the mismatch condition.

b) Clear flag bit, RBIF.

A mismatch condition will continue to set flag bit, RBIF. Reading PORTB will end the mismatch condition and allow flag bit, RBIF, to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

Pins, RB2 and RB3, are multiplexed with the USB peripheral and serve as the differential signal outputs for an external USB transceiver (TRIS configuration). Refer to **Section 17.2.2.2 "External Transceiver"** for additional information on configuring the USB module for operation with an external transceiver.

RB4 is multiplexed with CSSPP, the chip select function for the Streaming Parallel Port (SPP) – TRIS setting. Details of its operation are discussed in **Section 18.0 "Streaming Parallel Port"**.

EXAMPLE 10-2: INITIALIZING PORTB

```
CLRF    PORTB   ; Initialize PORTB by
                ; clearing output
                ; data latches
CLRF    LATB    ; Alternate method
                ; to clear output
                ; data latches
MOVLW   0Eh     ; Set RB<4:0> as
MOVWF   ADCON1  ; digital I/O pins
                ; (required if config bit
                ; PBADEN is set)
MOVLW   0CFh    ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISB   ; Set RB<3:0> as inputs
                ; RB<5:4> as outputs
                ; RB<7:6> as inputs
```


TABLE 10-3: PORTB I/O SUMMARY (CONTINUED)

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RB6/KBI2/ PGC	RB6	0	OUT	DIG	LATB<6> data output.
		1	IN	TTL	PORTB<6> data input; weak pull-up when RBPU bit is cleared.
	KBI2	1	IN	TTL	Interrupt-on-pin change.
	PGC	x	IN	ST	Serial execution (ICSP™) clock input for ICSP and ICD operation.(3)
RB7/KBI3/ PGD	RB7	0	OUT	DIG	LATB<7> data output.
		1	IN	TTL	PORTB<7> data input; weak pull-up when RBPU bit is cleared.
	KBI3	1	IN	TTL	Interrupt-on-pin change.
	PGD	x	OUT	DIG	Serial execution data output for ICSP and ICD operation.(3)
		x	IN	ST	Serial execution data input for ICSP and ICD operation.(3)

Legend: OUT = Output, IN = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, I²C/SMB = I²C/SMBus input buffer, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option)

Note 1: Configuration on POR is determined by PBADEN Configuration bit. Pins are configured as analog inputs when PBADEN is set and digital inputs when PBADEN is cleared.

2: Alternate pin assignment for CCP2 when CCP2MX = 0. Default assignment is RC1.

3: All other pin functions are disabled when ICSP™ or ICD operation is enabled.

4: 40/44-pin devices only.

TABLE 10-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	54
LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	54
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	54
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RBIP	51
INTCON3	INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF	51
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	52
SPPCON(1)	—	—	—	—	—	—	SPPOWN	SPPEN	55
SPPCFG(1)	CLKCFG1	CLKCFG0	CSEN	CLK1EN	WS3	WS2	WS1	WS0	55
UCON	—	PPBRST	SE0	PKTDIS	USBEN	RESUME	SUSPND	—	55

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTB.

Note 1: These registers are unimplemented on 28-pin devices.

TABLE 10-3: PORTB I/O SUMMARY (CONTINUED)

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RB6/KBI2/ PGC	RB6	0	OUT	DIG	LATB<6> data output.
		1	IN	TTL	PORTB<6> data input; weak pull-up when RBPU bit is cleared.
	KBI2	1	IN	TTL	Interrupt-on-pin change.
	PGC	x	IN	ST	Serial execution (ICSP™) clock input for ICSP and ICD operation.(3)
RB7/KBI3/ PGD	RB7	0	OUT	DIG	LATB<7> data output.
		1	IN	TTL	PORTB<7> data input; weak pull-up when RBPU bit is cleared.
	KBI3	1	IN	TTL	Interrupt-on-pin change.
	PGD	x	OUT	DIG	Serial execution data output for ICSP and ICD operation.(3)
		x	IN	ST	Serial execution data input for ICSP and ICD operation.(3)

Legend: OUT = Output, IN = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, I^2C/SMB = I^2C/SMBus input buffer, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option)

Note 1: Configuration on POR is determined by PBADEN Configuration bit. Pins are configured as analog inputs when PBADEN is set and digital inputs when PBADEN is cleared.

2: Alternate pin assignment for CCP2 when CCP2MX = 0. Default assignment is RC1.

3: All other pin functions are disabled when ICSP™ or ICD operation is enabled.

4: 40/44-pin devices only.

TABLE 10-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	54
LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	54
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	54
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RBIP	51
INTCON3	INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF	51
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	52
SPPCON(1)	—	—	—	—	—	—	SPPOWN	SPPEN	55
SPPCFG(1)	CLKCFG1	CLKCFG0	CSEN	CLK1EN	WS3	WS2	WS1	WS0	55
UCON	—	PPBRST	SE0	PKTDIS	USBEN	RESUME	SUSPND	—	55

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTB.

Note 1: These registers are unimplemented on 28-pin devices.

21.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) converter module has 10 inputs for the 28-pin devices and 13 for the 40/44-pin devices. This module allows conversion of an analog input signal to a corresponding 10-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 21-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 21-2, configures the functions of the port pins. The ADCON2 register, shown in Register 21-3, configures the A/D clock source, programmed acquisition time and justification.

REGISTER 21-1: ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS3:CHS0:** Analog Channel Select bits

0000 = Channel 0 (AN0)
0001 = Channel 1 (AN1)
0010 = Channel 2 (AN2)
0011 = Channel 3 (AN3)
0100 = Channel 4 (AN4)
0101 = Channel 5 (AN5)(1,2)
0110 = Channel 6 (AN6)(1,2)
0111 = Channel 7 (AN7)(1,2)
1000 = Channel 8 (AN8)
1001 = Channel 9 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
1100 = Channel 12 (AN12)
1101 = Unimplemented(2)
1110 = Unimplemented(2)
1111 = Unimplemented(2)

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

When ADON = 1:
1 = A/D conversion in progress
0 = A/D Idle

bit 0 **ADON:** A/D On bit

1 = A/D converter module is enabled
0 = A/D converter module is disabled

Note 1: These channels are not implemented on 28-pin devices.
2: Performing a conversion on unimplemented channels will return a floating input measurement.

REGISTER 21-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0(1)	R/W(1)	R/W(1)	R/W(1)
—	—	VCFG0	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **VCFG0:** Voltage Reference Configuration bit (V_{REF-} source)
1 = V_{REF-} (AN2)
0 = V_{SS}

bit 4 **VCFG0:** Voltage Reference Configuration bit (V_{REF+} source)
1 = V_{REF+} (AN3)
0 = V_{DD}

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits:

PCFG3: PCFG0	AN12	AN11	AN10	AN9	AN8	AN7(2)	AN6(2)	AN5(2)	AN4	AN3	AN2	AN1	AN0
0000(1)	A	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A	A
0011	D	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	D	A	A	A	A	A	A	A	A	A
0111(1)	D	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input D = Digital I/O

Note 1: The POR value of the PCFG bits depends on the value of the PBADEN Configuration bit. When PBADEN = 1, PCFG<3:0> = 0000; when PBADEN = 0, PCFG<3:0> = 0111.
2: AN5 through AN7 are available only on 40/44-pin devices.

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (V_{DD} and V_{SS}) or the voltage level on the RA3/AN3/V_{REF+} and RA2/AN2/V_{REF-}/CVREF pins.

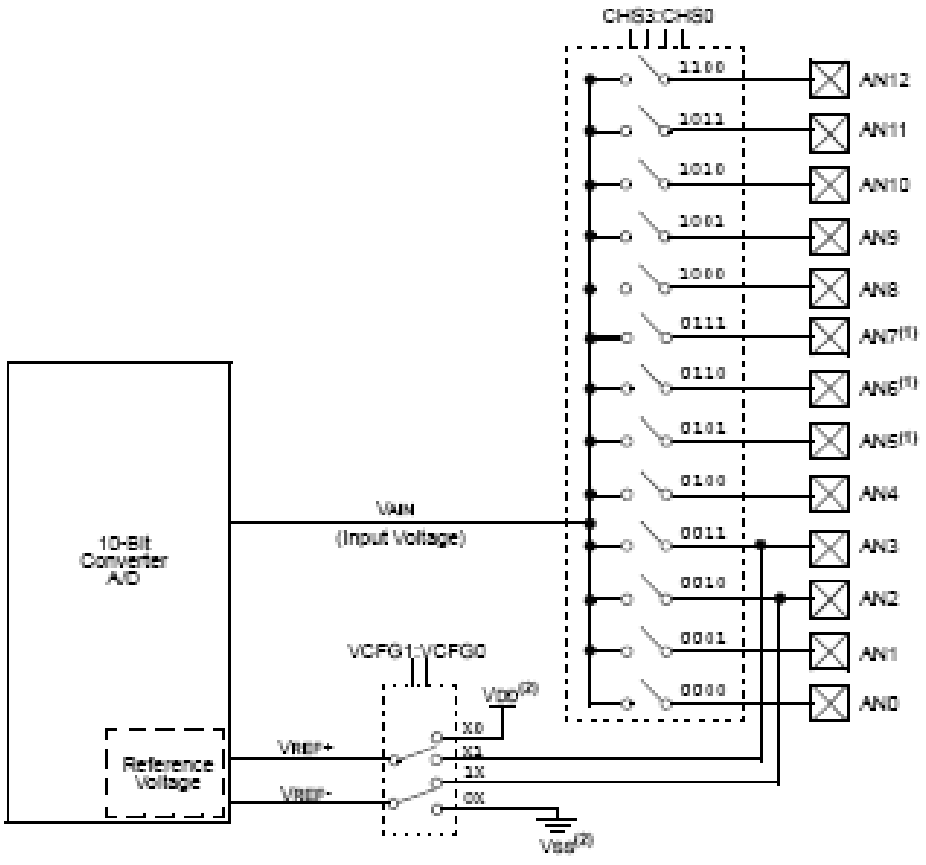
The A/D converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0 register) is cleared and A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 21-1.

FIGURE 21-1: A/D BLOCK DIAGRAM



Note 1: Channels AN5 through AN7 are not available on 28-pin devices.
2: I/O pins have diode protection to V_{DD} and V_{SS}.

APPENDIX B

LM7805 Voltage Regulator Datasheet

FAIRCHILD SEMICONDUCTOR®

March 2008

LM78XX/LM78XXA
3-Terminal 1A Positive Voltage Regulator

Features

- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

General Description

The LM78XX series of three terminal positive regulators are available in the TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

Ordering Information

Product Number	Output Voltage Tolerance	Package	Operating Temperature
LM7805CT	±4%	TO-220	-40°C to +125°C
LM7806CT			
LM7808CT			
LM7809CT			
LM7810CT			
LM7812CT			
LM7815CT			
LM7818CT			
LM7824CT			
LM7805ACT	±2%		0°C to +125°C
LM7806ACT			
LM7808ACT			
LM7809ACT			
LM7810ACT			
LM7812ACT			
LM7815ACT			
LM7818ACT			
LM7824ACT			

Block Diagram

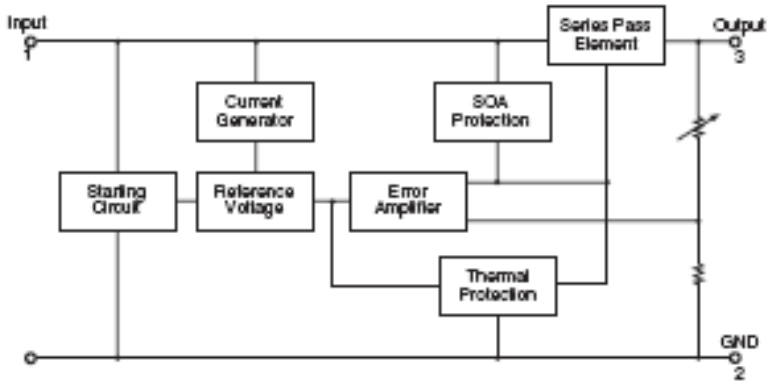


Figure 1.

Pin Assignment

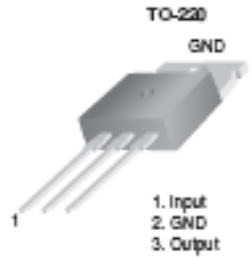


Figure 2.

Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Symbol	Parameter		Value	Unit
V_I	Input Voltage	V_O = 5V to 18V	35	V
		V_O = 24V	40	V
$R_{\theta JC}$	Thermal Resistance Junction-Cases (TO-220)		5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction-Air (TO-220)		65	°C/W
T_{OPR}	Operating Temperature Range	LM78xx	-40 to +125	°C
		LM78xxA	0 to +125	
T_{STG}	Storage Temperature Range		-65 to +150	°C

Electrical Characteristics (LM7805)

Refer to the test circuits. -40°C < T_J < 125°C, I_O = 500mA, V_I = 10V, C_I = 0.1µF, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_J = +25°C		4.8	5.0	5.2	V
		5mA ≤ I_O ≤ 1A, P_O ≤ 15W, V_I = 7V to 20V		4.75	5.0	5.25	
Regline	Line Regulation[1]	T_J = +25°C	V_O = 7V to 25V	–	4.0	100	mV
			V_I = 8V to 12V	–	1.6	50.0	
Regload	Load Regulation[1]	T_J = +25°C	I_O = 5mA to 1.5A	–	9.0	100	mV
			I_O = 250mA to 750mA	–	4.0	50.0	
I_Q	Quiescent Current	T_J = +25°C		–	5.0	8.0	mA
ΔI_Q	Quiescent Current Change	I_O = 5mA to 1A		–	0.03	0.5	mA
		V_I = 7V to 25V		–	0.3	1.3	
$\Delta V_O/\Delta T$	Output Voltage Drift[2]	I_O = 5mA		–	-0.8	–	mV/°C
V_N	Output Noise Voltage	f = 10Hz to 100kHz, T_A = +25°C		–	42.0	–	µV/V_O
RR	Ripple Rejection[2]	f = 120Hz, V_O = 8V to 18V		62.0	73.0	–	dB
V_{DROP}	Dropout Voltage	I_O = 1A, T_J = +25°C		–	2.0	–	V
r_O	Output Resistance[2]	f = 1kHz		–	15.0	–	mΩ
I_{SC}	Short Circuit Current	V_I = 35V, T_A = +25°C		–	230	–	mA
I_{PK}	Peak Current[2]	T_J = +25°C		–	2.2	–	A

Notes:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.
2. These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7805A) (Continued)

Refer to the test circuits. $0°C < T_J < 125°C$, I_O = 1A, V_I = 10V, C_I = 0.33µF, C_O = 0.1µF, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_J = +25°C		4.9	5.0	5.1	V
		I_O = 5mA to 1A, $P_O \leq$ 15W, V_I = 7.5V to 20V		4.8	5.0	5.2	
Regline	Line Regulation[19]	V_I = 7.5V to 25V, I_O = 500mA		–	5.0	50.0	mV
		V_I = 8V to 12V		–	3.0	50.0	
		T_J = +25°C	V_I = 7.3V to 20V	–	5.0	50.0	
			V_I = 8V to 12V	–	1.5	25.0	
Regload	Load Regulation[19]	T_J = +25°C, I_O = 5mA to 1.5A		–	9.0	100	mV
		I_O = 5mA to 1A		–	9.0	100	
		I_O = 250mA to 750mA		–	4.0	50.0	
I_Q	Quiescent Current	T_J = +25°C		–	5.0	6.0	mA
ΔI_Q	Quiescent Current Change	I_O = 5mA to 1A		–	–	0.5	mA
		V_I = 8V to 25V, I_O = 500mA		–	–	0.8	
		V_I = 7.5V to 20V, T_J = +25°C		–	–	0.8	
$\Delta V_O/\Delta T$	Output Voltage Drift[20]	I_O = 5mA		–	-0.8	–	mV/°C
V_N	Output Noise Voltage	f = 10Hz to 100kHz, T_A = +25°C		–	10.0	–	$\mu V/V_O$
RR	Ripple Rejection[20]	f = 120Hz, I_O = 500mA, V_I = 8V to 18V		–	68.0	–	dB
V_{DROP}	Dropout Voltage	I_O = 1A, T_J = +25°C		–	2.0	–	V
r_O	Output Resistance[20]	f = 1kHz		–	17.0	–	mΩ
I_{SC}	Short Circuit Current	V_I = 35V, T_A = +25°C		–	250	–	mA
I_{PK}	Peak Current[20]	T_J = +25°C		–	2.2	–	A

Notes:

19. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

20. These parameters, although guaranteed, are not 100% tested in production.

Typical Performance Characteristics

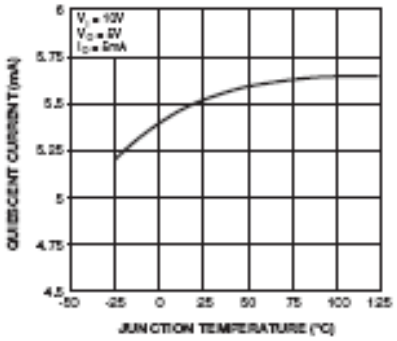


Figure 3. Quiescent Current

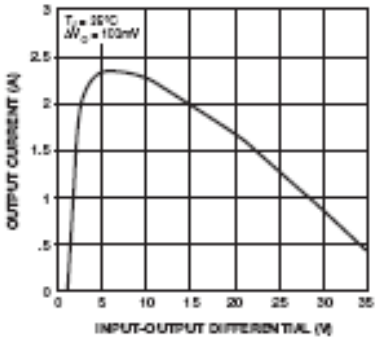


Figure 4. Peak Output Current

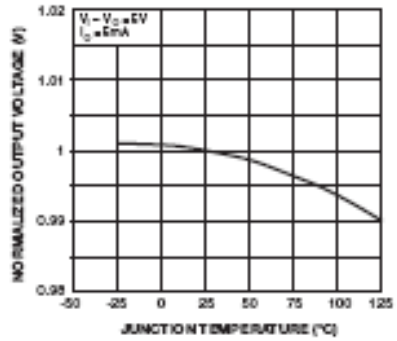


Figure 5. Output Voltage

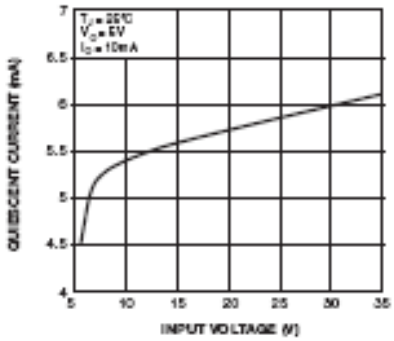


Figure 6. Quiescent Current

Typical Applications

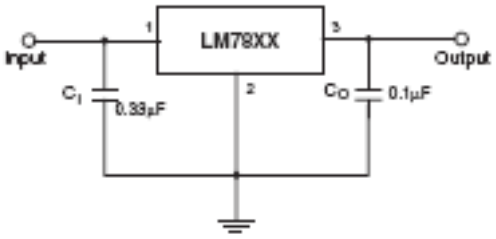


Figure 7. DC Parameters

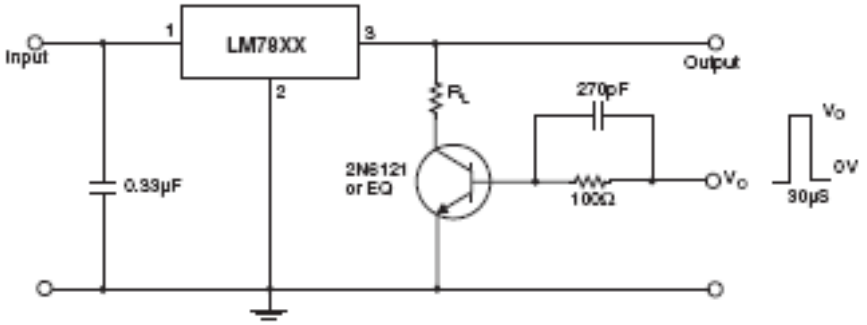


Figure 8. Load Regulation

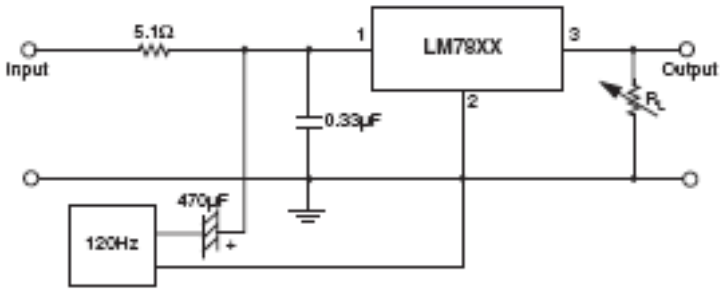


Figure 9. Ripple Rejection

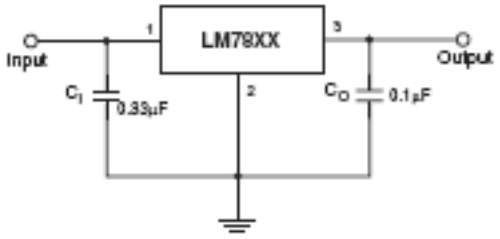
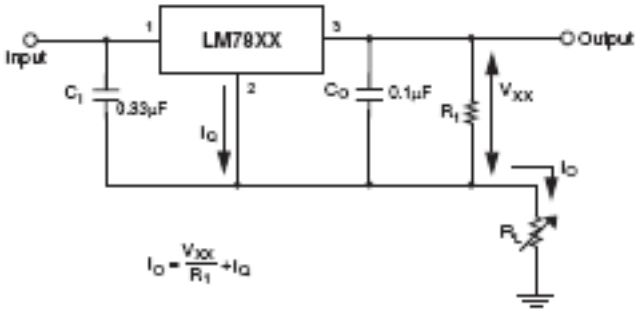


Figure 10. Fixed Output Regulator



Notes:
1. To specify an output voltage, substitute voltage value for "XX." A common ground is required between the input and the output voltage. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.
2. C_I is required if regulator is located an appreciable distance from power supply filter.
3. C_O improves stability and transient response.

Figure 11.

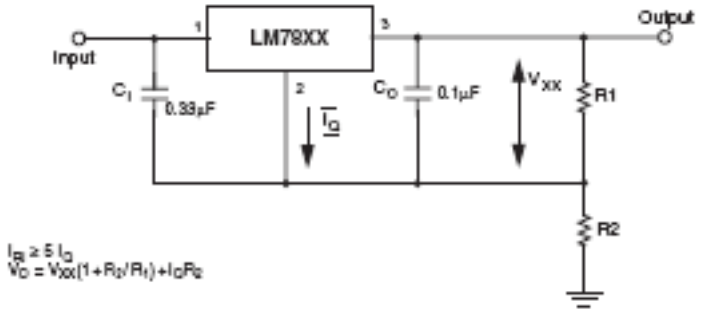
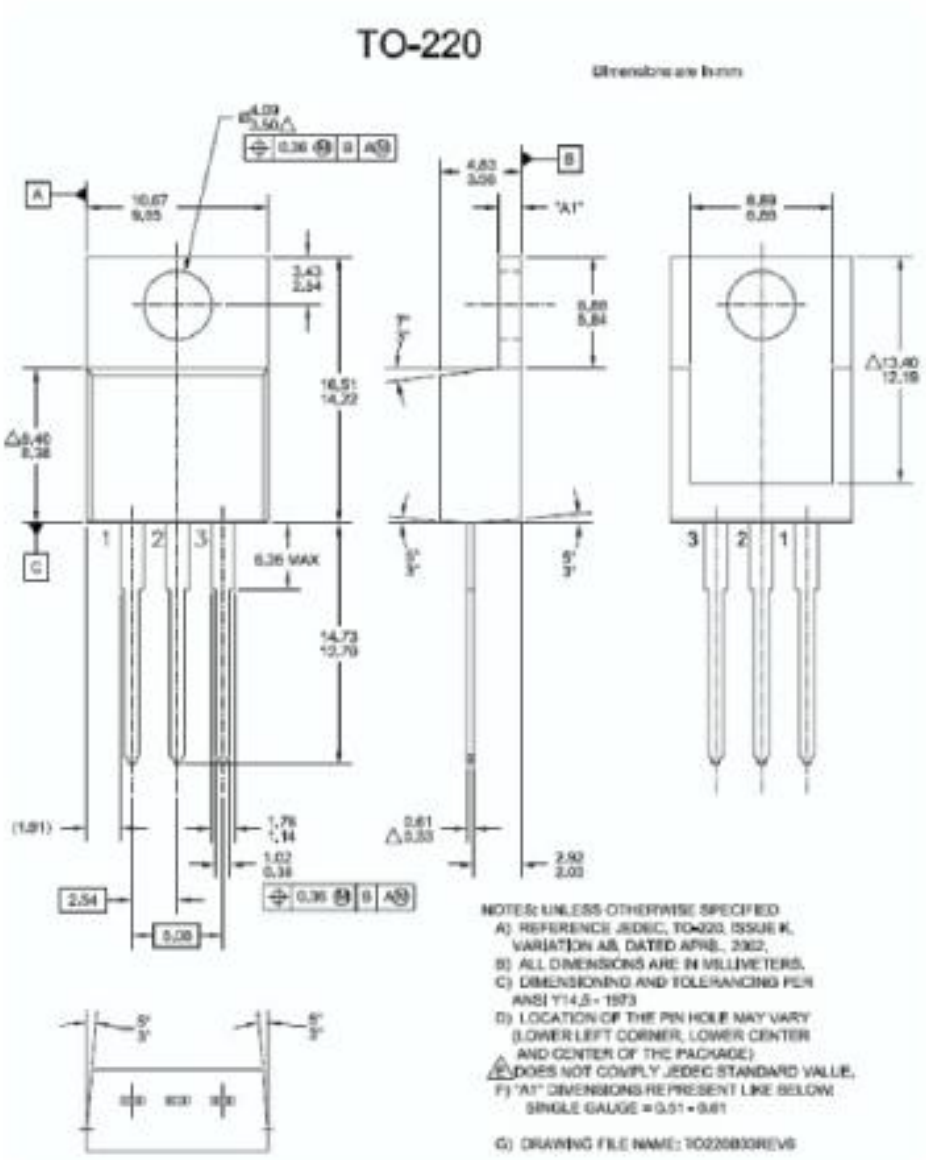


Figure 12. Circuit for Increasing Output Voltage

Mechanical Dimensions

Dimensions in millimeters



APPENDIX C

JHD162A Series Datasheet

JHD162A SERIES

• ..... DISPRAY CONTENT= 16 CHAR x 2ROW

CHAR. DOTS• 5 x 8

DRIVING MODE• 1/16D

AVAILABLE TYPES• •

TN• STN(YELLOW GREEN• GREY• B/W)

REFLECTIVE• WITH EL OR LED BACKLIGHT

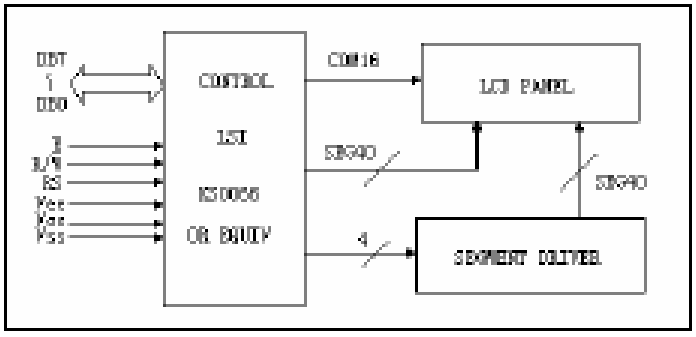
EL/100VAC• 400HZ

LED/4.2VDC

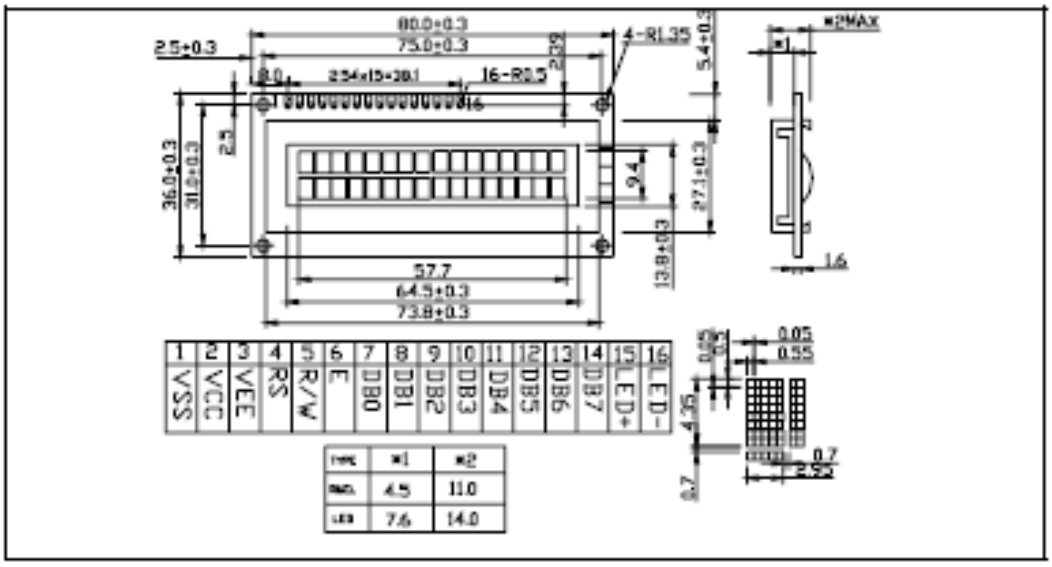
• .....

Parameter	Symbol	Testing Criteria	Standard Values			Unit
			Min.	Typ.	Max	
Supply voltage	V_{DD}-V_{SS}	-	4.5	5.0	5.5	V
Input high voltage	V_{IH}	-	2.2	-	V_{DD}	V
Input low voltage	V_{IL}	-	-0.3	-	0.6	V
Output high voltage	V_{OH}	-I$_{OH}$=0.2mA	2.4	-	-	V
Output low voltage	V_{OL}	I$_{OL}$=1.2mA	-	-	0.4	V
Operating voltage	I_{DD}	V_{DD}=5.0V	-	1.5	3.0	mA

• .....



• .....



	4.5	11.0
	7.6	14.0

. .....

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
VSS	VCC	VEE	RS	R/W	E	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	LED+	LED-

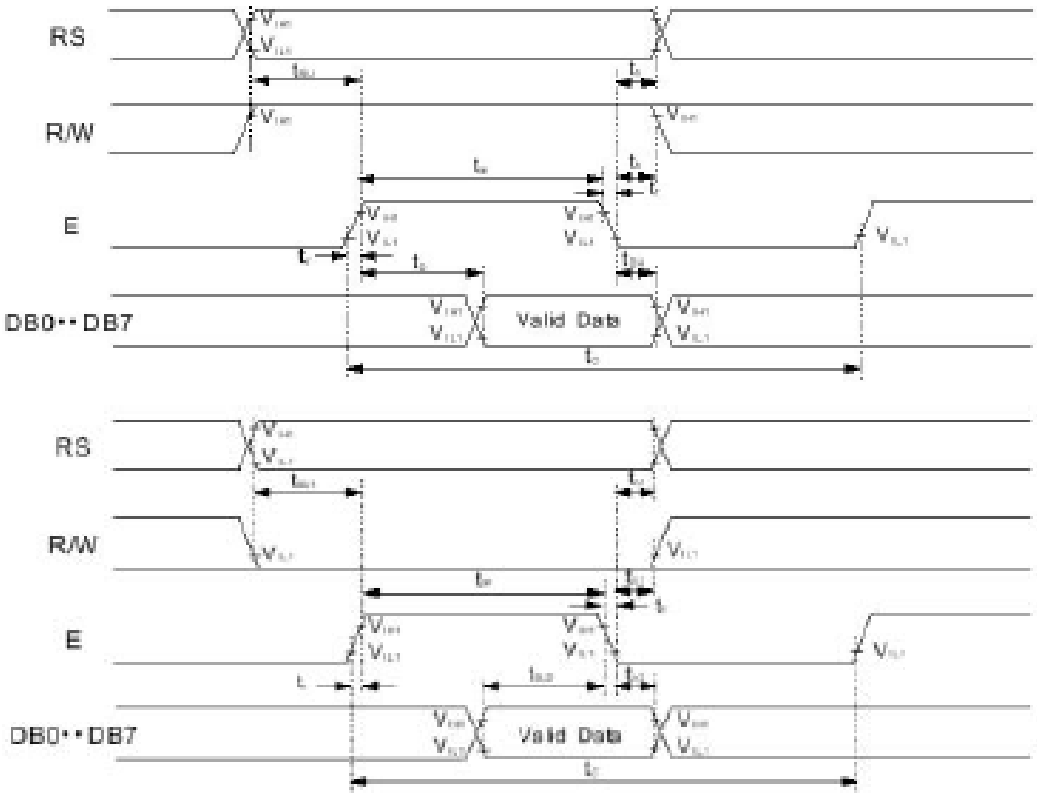
AC Characteristics Read Mode Timing Diagram

Table 12. AC Characteristics (V_{DD} = 4.5V ~ 5.5V, Ta = -30 ~ +85°C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode (Refer to Fig-6)	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu1	40	-	-	
	R/W and RS Hold Time	t_{H1}	10	-	-	
	Data Setup Time	tsu2	80	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode (Refer to Fig-7)	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu	40	-	-	
	R/W and RS Hold Time	t_H	10	-	-	
	Data Output Delay Time	t_D	-	-	120	
	Data Hold Time	t_{DH}	5	-	-	

Table 13. AC Characteristics (V_{DD} =2.7V ~ 4.5V, Ta = -30 ~ +85°C)

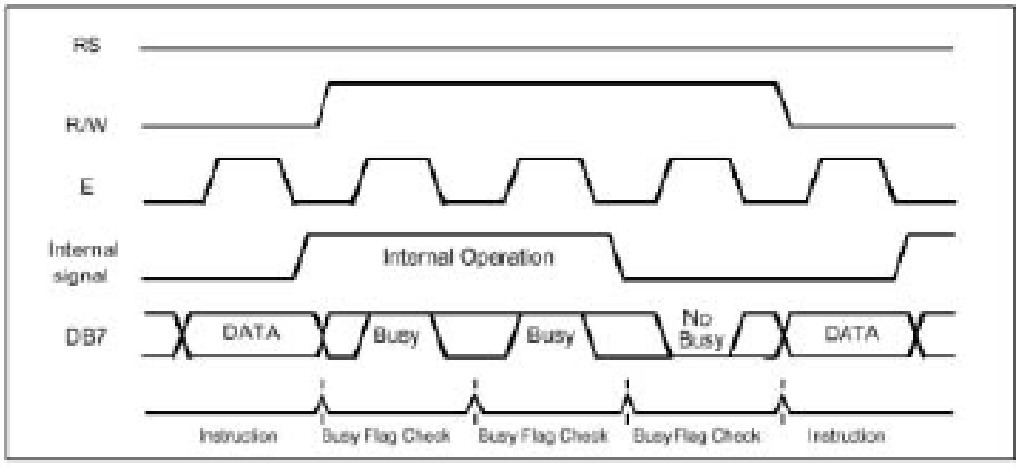
Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode (Refer to Fig-6)	E Cycle Time	tc	1000	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu1	60	-	-	
	R/W and RS Hold Time	t_{H1}	20	-	-	
	Data Setup Time	tsu2	195	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode (Refer to Fig-7)	E Cycle Time	tc	1000	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu	60	-	-	
	R/W and RS Hold Time	t_H	20	-	-	
	Data Output Delay Time	t_D	-	-	360	
	Data Hold Time	t_{DH}	5	-	-	

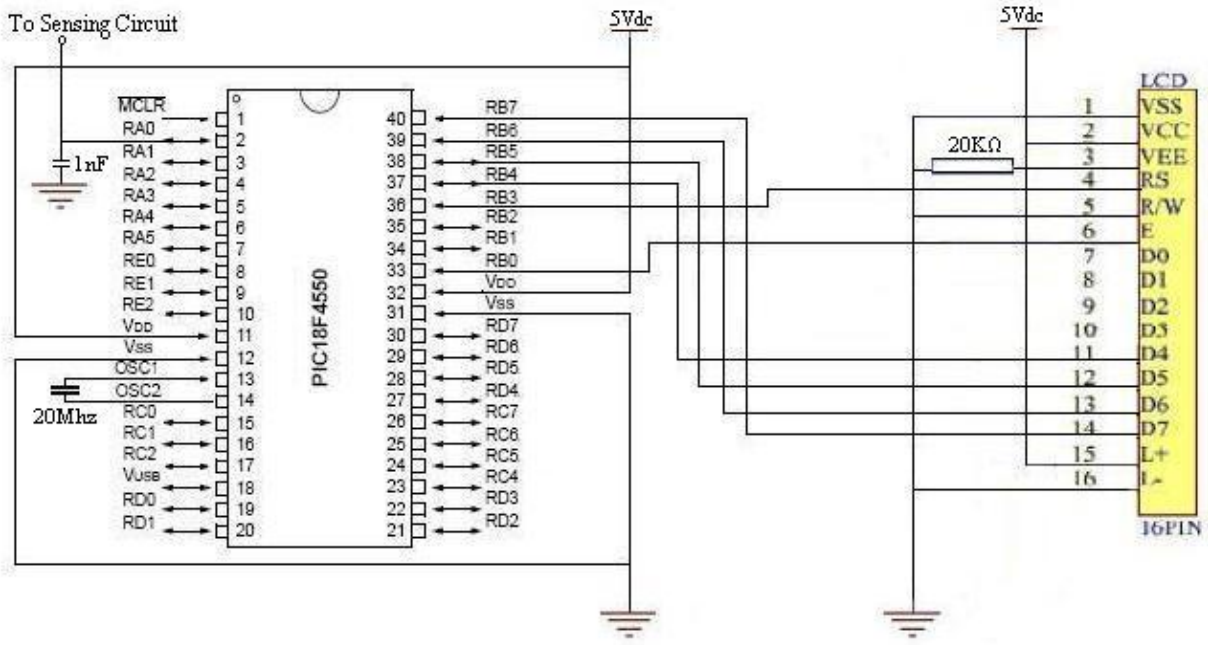


Write Mode Timing Diagram

Timing

1) Interface with 8-bit MPU
When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7.
Example of timing sequence is shown below.




To Sensing Circuit
5Vdc
5Vdc
1nF
20Mhz
20KΩ
PIC18F4550
MCLR
RA0
RA1
RA2
RA3
RA4
RA5
RE0
RE1
RE2
Vdd
Vss
OSC1
OSC2
RC0
RC1
RC2
Vuss
RD0
RD1
RB7
RB6
RB5
RB4
RB3
RB2
RB1
RB0
Vdd
Vss
RD7
RD6
RD5
RD4
RC7
RC6
RC5
RC4
RD3
RD2
LCD
VSS
VCC
VEE
RS
R/W
E
D0
D1
D2
D3
D4
D5
D6
D7
L+
L-
16PIN

APPENDIX F

Omron G3NA-220B Solid State Relay

OMRON

Solid-state Relay

G3NA

A Wide Range of Models with 5- to 40-A Output Currents and Up to 480-VAC/200-VDC Output Voltages

- All models feature the same compact dimensions to provide a uniform mounting pitch.
- Built-in varistor effectively absorb external surges.
- Operation indicator (red LED) enables monitoring operation.
- Protective cover for greater safety.
- Standard models approved by UL/CSA and -UTU models by VDE (TÜV).

Ordering Information

Isolation	Zero cross function	Indicator	Rated output load (Applicable output load)	Rated input voltage	Model
Phototriac	Yes	Yes	5 A at 24 to 240 VAC* (19 to 264 VAC)	5 to 24 VDC	G3NA-205B
Photocoupler				100 to 120 VAC	
				200 to 240 VAC	
Phototriac			10 A at 24 to 240 VAC* (19 to 264 VAC)	5 to 24 VDC	G3NA-210B
Photocoupler				100 to 120 VAC	
				200 to 240 VAC	
			10 A at 200 to 480 VAC* (180 to 528 VAC)	5 to 24 VDC	G3NA-410B
				100 to 240 VAC	
	—		10 A at 5 to 200 VDC* (4 to 220 VDC)	5 to 24 VDC	G3NA-D210B
				100 to 240 VAC	
Phototriac	Yes		20 A at 24 to 240 VAC* (19 to 264 VAC)	5 to 24 VDC	G3NA-220B
Photocoupler				100 to 120 VAC	
				200 to 240 VAC	
			20 A at 200 to 480 VAC* (180 to 528 VAC)	5 to 24 VDC	G3NA-420B
				100 to 240 VAC	
Phototriac			40 A at 24 to 240 VAC* (19 to 264 VAC)	5 to 24 VDC	G3NA-240B
Photocoupler				100 to 120 VAC	
				200 to 240 VAC	
			40 A at 200 to 480 VAC* (180 to 528 VAC)	5 to 24 VDC	G3NA-440B
				100 to 240 VAC	
			50 A at 200 to 480 VAC* (180 to 528 VAC)	5 to 24 VDC	G3NA-450B

*Loss time increases under 75 VAC. (Refer to page 148.)

Note: When ordering a TÜV-approved model, add "-UTU" to the model number as shown below.
Example: G3NA-210B-UTU

■ Accessories (Order Separately)

Heat Sink

The following heat sinks are thin and can be DIN-track mounted (except Y92B-P250).
See *Dimensions* for details.

Model	Applicable SSR
Y92B-N50	G3NA-205B, G3NA-210B, G3NA-D210B, G3NA-410B, G3NE-205T(L), G3NE-210T(L)
Y92B-N100	G3NA-220B, G3NA-420B, G3NE-220T(L)
Y92B-N150	G3NA-240B, G3NA-440B
Y92B-P250	G3NA-450B

Low-cost Models

Model	Applicable SSR
Y92B-A100	G3NA-205B, G3NA-210B, G3NA-D210B, G3NA-220B, G3NA-410B, G3NA-420B
Y92B-A150N	G3NA-240B, G3NA-440B
Y92B-A250	G3NA-440B

Mounting Bracket

Used to mount the G3NA with a mounting dimension of 56 mm.

Model	Applicable SSR
R88-11	G3NA-240B, G3NA-440B

See *Dimensions* for details. (Refer to page 148.)

Specifications

■ Ratings

Input (Ambient Temperature: 25°C)

Model	Rated voltage	Operating voltage	Impedance	Voltage level	
				Must operate voltage	Must release voltage
G3NA-2□□B	5 to 24 VDC	4 to 32 VDC	7 mA max.*	4 VDC max.	1 VDC min.
	100 to 120 VAC	75 to 132 VAC	36 kΩ±20%	75 VAC max.**	20 VAC min.**
	200 to 240 VAC	150 to 264 VAC	72 kΩ±20%	150 VAC max.**	40 VAC min.**
G3NA-4□□B	5 to 24 VDC	4 to 32 VDC	5 mA max.*	4 VDC max.	1 VDC min.
G3NA-D210B	100 to 240 VAC	75 to 264 VAC	72 kΩ±20%	75 VAC max.	20 VAC min.

Note: The input impedance is measured at the maximum value of the rated supply voltage (for example, with the model rated at 100 to 120 VAC, the input impedance is measured at 120 VAC).
*With constant current input circuit system. The impedance for the G3NA-□□□B-UTU is 15 mA max.
**Refer to the *Engineering Data* for further details.

Output

Model	Applicable load				
	Rated load voltage	Load voltage range	Load current		Inrush current
			With heat sink*	Without heat sink	
G3NA-205B	24 to 240 VAC	19 to 264 VAC	0.1 to 5 A	0.1 to 3 A	60 A (60 Hz, 1 cycle)
G3NA-210B			0.1 to 10 A	0.1 to 4 A	150 A (60 Hz, 1 cycle)
G3NA-410B	200 to 480 VAC	180 to 528 VAC	0.2 to 10 A	0.2 to 4 A	
G3NA-220B	24 to 240 VAC	19 to 264 VAC	0.1 to 20 A	0.1 to 4 A	220 A (60 Hz, 1 cycle)
G3NA-420B	200 to 480 VAC	180 to 528 VAC	0.2 to 20 A	0.2 to 4 A	
G3NA-240B	24 to 240 VAC	19 to 264 VAC	0.1 to 40 A	0.1 to 6 A	440 A (60 Hz, 1 cycle)
G3NA-440B	200 to 480 VAC	180 to 528 VAC	0.2 to 40 A	0.2 to 6 A	
G3NA-450B	200 to 480 VAC	180 to 528 VAC	0.2 to 50 A	0.2 to 6 A	
G3NA-D210B	5 to 200 VDC	4 to 220 VDC	0.1 to 10 A	0.1 to 4 A	20 A (10 ms)

*When OMRON's heat sink (refer to the accessories) or a heat sink of specified size is used.

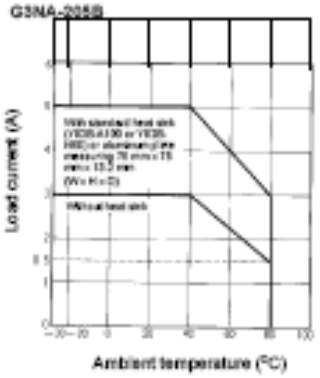
■ Characteristics

Item	G3NA-205B, -210B, -220B	G3NA-240B	G3NA-410B, -420B, -440B, -450B	G3NA-D210B
Operate time	1/2 of load power source cycle + 1 ms max. (DC input) 3/2 of load power source cycle + 1 ms max. (AC input)			1 ms max. (DC input) 30 ms max. (AC input)
Release time	1/2 of load power source cycle + 1 ms max. (DC input) 3/2 of load power source cycle + 1 ms max. (AC input)			5 ms max. (DC input) 30 ms max. (AC input)
Output ON voltage drop	1.6 V (RMS) max.		1.8 V (RMS) max.	1.5 V max.
Leakage current	5 mA max. (at 100 VAC) 10 mA max. (at 200 VAC)		10 mA max. (at 200 VAC) 20 mA max. (at 400 VAC)	5 mA max. (at 200 VDC)
Insulation resistance	100 MΩ min. (at 500 VDC)			
Dielectric strength	2,500 VAC, 50/60 Hz for 1 min			
Vibration resistance	Malfunction: 10 to 55 Hz, 1.5-mm double amplitude			
Shock resistance	Malfunction: 1,000 m/s^2			
Ambient temperature	Operating: −30°C to 80°C (with no icing or condensation) Storage: −30°C to 100°C (with no icing or condensation)			
Approved standards	UL508 File No.E84562/CSA C22.2 (No.0, No.14) File No.LR35535 TÜV R9151660 (EN60950)			
Ambient humidity	Operating: 45% to 85%			
Weight	Approx. 80 g	Approx. 70 g	Approx. 80 g	Approx. 70 g

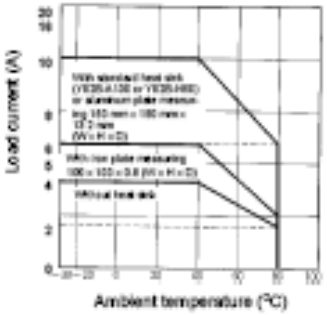
Engineering Data

Load Current vs. Ambient Temperature Characteristics

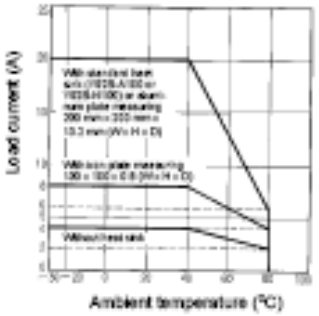
G3NA-205B



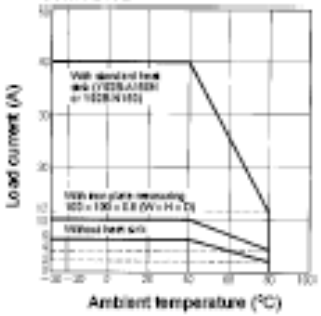
G3NA-210B/H10B



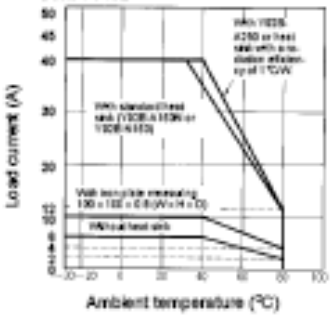
G3NA-220B/H20B



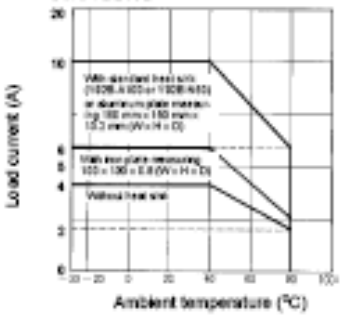
G3NA-240B



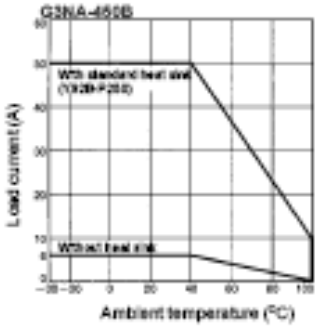
G3NA-440B



G3NA-D210B



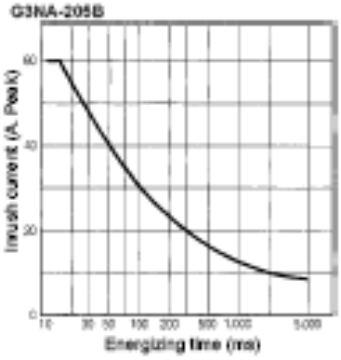
G3NA-450B



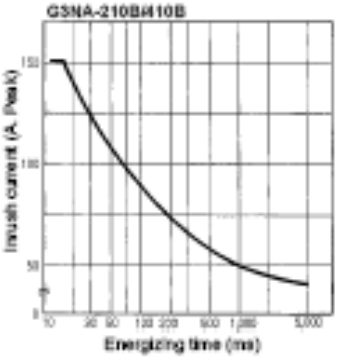
Inrush Current Reelstivity

Non-repetitive (Keep the inrush current to half the rated value if it occurs repetitively.)

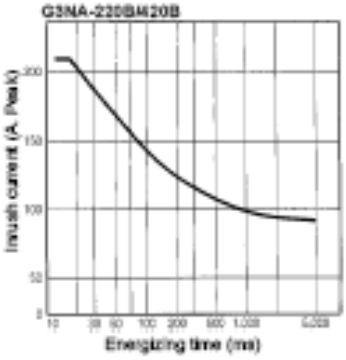
G3NA-205B



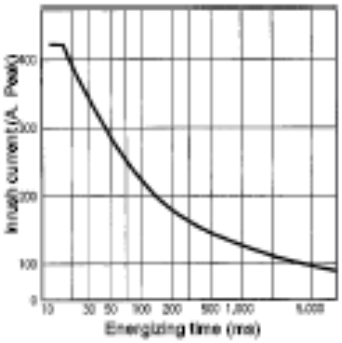
G3NA-210B/410B



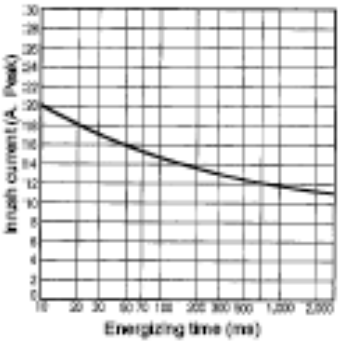
G3NA-220B/420B



G3NA-240B/440B/450B

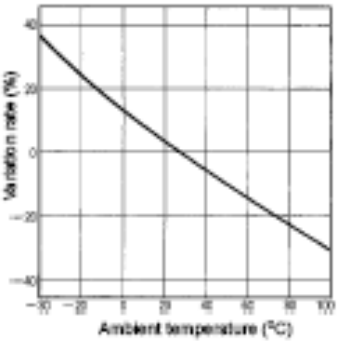


G3NA-D210B



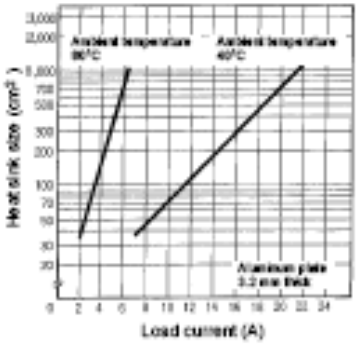
Temperature Characteristics (with Must Operate Voltage and Must Release Voltage)

G3NA-2□□B AC Input



Heat Sink Size vs. Load Current

G3NA-220B



Note: The heat sink size refers to the combined area of the sides of the heat sink that radiate heat. For example, when a current of 15 A is allowed to flow through the SSR at 40°C, the graph shows that the heat sink size is about 450 cm². Therefore, if the heat sink is square, one side of the heat sink must be 15 cm ($15^2 \times 2 = 450$) or longer.

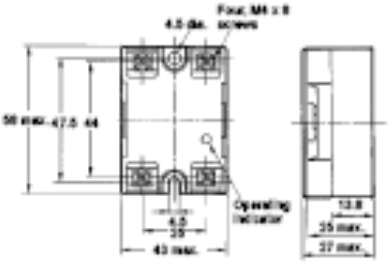
Dimensions

Note: All units are in millimeters unless otherwise indicated.

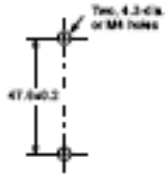
In the case of surface mounting, a 30% derating of the load current is required.

The orientation indicated by the external dimensions is not the correct mounting orientation. When opening mounting holes, refer to the mounting hole dimensions.

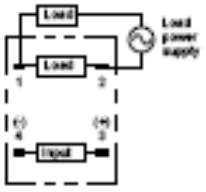
G3NA-205B, G3NA-210B, G3NA-220B, G3NA-410B, G3NA-420B



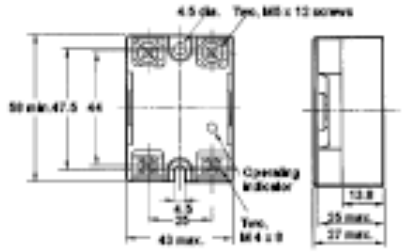
Mounting Holes



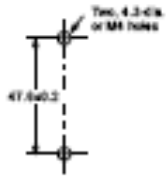
Terminal Arrangement/ Internal Connections (Top View)



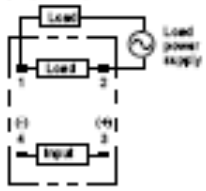
G3NA-240B, G3NA-440B, G3NA-450B



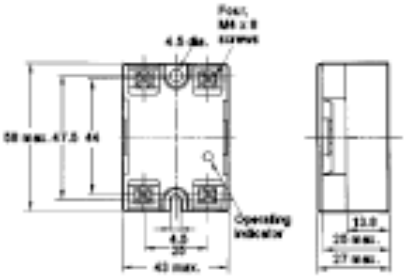
Mounting Holes



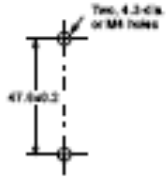
Terminal Arrangement/ Internal Connections (Top View)



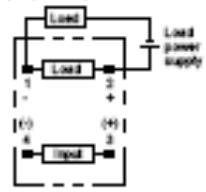
G3NA-D210B



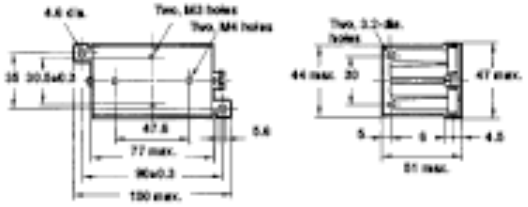
Mounting Holes



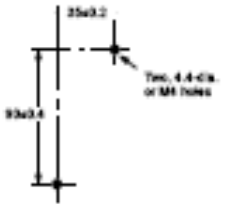
Terminal Arrangement/ Internal Connections (Top View)



Heat Sink
Y92B-N50

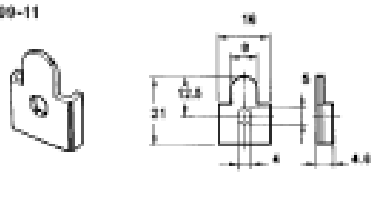


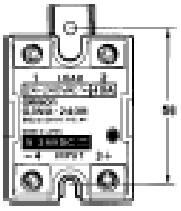
Mounting Holes



Weight: approx. 200 g

R89-11





Use Mounting Bracket R89-11 so that the G3NA-240B can be mounted with the same pitch as that of the G3N-240B.

Precautions

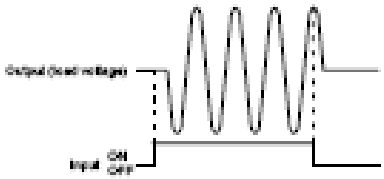
Refer to pages 11 to 19 for general precautions.

Load Connection

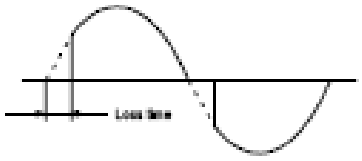
For an AC load, use a power supply rated at 50 or 60 Hz.
The maximum operating frequency is 10 Hz.
The G3NA has a built-in varistor for overvoltage protection.

Zero Cross Function

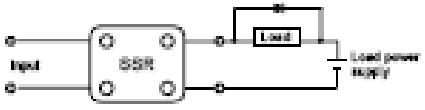
An SSR with a zero cross function operates when an AC load voltage reaches the zero point or its vicinity. This reduces clicking noises when the load is input, and minimizes the influence of an inductive load, such as a lamp, heater, or motor, on the power supply because the inrush current of the load is reduced. This can also minimize the scale of the inrush current protection circuit.



At a low applied voltage, such as 24 VAC, the load current is not fully supplied. When the Unit is switched ON, the voltage required to power the Unit deprives the output signal of the necessary voltage level and thus creates loss time. The lower the load voltage is, the greater the loss time is. This condition, however, will not create any serious problems.



For a DC or L load, a diode should be connected in parallel the load to absorb the counter electromotive force of the load.

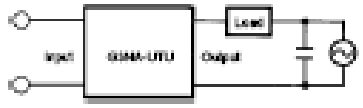


When attaching a heat sink to the G3NA, apply Silicone Grease or equivalent heat conductive grease on the heat sink. (Toshiba Silicon, Shinetsu Silicon, etc.)

Tighten the mounting screws of the heat sink with a torque of 0.78 to 0.98 N • m.

EN55011 Measurement of Mains Terminal Disturbance Voltage

The G3NA-UTU conforms to EN55011 standards when a capacitor is connected to the load power supply as shown in the following circuit diagram.



Recommended Capacitor:
Nissei Denki's MKT-series R40 (1 µF)

The output terminal side of the G3NA-D210B is connected to a built-in diode for protecting the SSR from damage that may result from reverse connection. The SSR, however, cannot withstand one minute or more if the wires are connected in reverse order. Therefore, pay the utmost attention not to make polarity mistakes on the load side.

ALL DIMENSIONS SHOWN ARE IN MILLIMETERS.
To convert millimeters into inches, multiply by 0.03937. To convert grams into ounces, multiply by 0.03527.

APPENDIX G

Half-Effect Linear Current Sensor Datasheet

ACS712

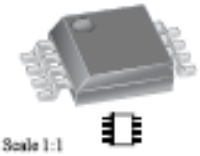
Fully Integrated, Hall Effect-Based Linear Current Sensor IC with 2.1 kVRMS Isolation and a Low-Resistance Current Conductor

Features and Benefits

- Low-noise analog signal path
- Device bandwidth is set via the new FILTER pin
- 5 µs output rise time in response to step input current
- 80 kHz bandwidth
- Total output error 1.5% at T_A = 25°C
- Small footprint, low-profile SOIC8 package
- 1.2 mΩ internal conductor resistance
- 2.1 kVRMS minimum isolation voltage from pins 1-4 to pins 5-8
- 5.0 V, single supply operation
- 66 to 185 mV/A output sensitivity
- Output voltage proportional to AC or DC currents
- Factory-trimmed for accuracy
- Extremely stable output offset voltage
- Nearly zero magnetic hysteresis
- Ratiometric output from supply voltage

TÜV America Certificate Number: U8V 08 05 54214 010

Package: 8 Lead SOIC (suffix LC)



Approximate Scale 1:1

Description

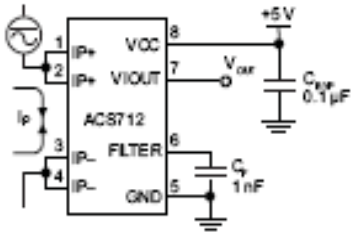
The Allegro® ACS712 provides economical and precise solutions for AC or DC current sensing in industrial, commercial, and communications systems. The device package allows for easy implementation by the customer. Typical applications include motor control, load detection and management, switch-mode power supplies, and overcurrent fault protection. The device is not intended for automotive applications.

The device consists of a precise, low-offset, linear Hall circuit with a copper conduction path located near the surface of the die. Applied current flowing through this copper conduction path generates a magnetic field which the Hall IC converts into a proportional voltage. Device accuracy is optimized through the close proximity of the magnetic signal to the Hall transducer. A precise, proportional voltage is provided by the low-offset, chopper-stabilized BiCMOS Hall IC, which is programmed for accuracy after packaging.

The output of the device has a positive slope (>$V_{IOUT(Q)}$) when an increasing current flows through the primary copper conduction path (from pins 1 and 2, to pins 3 and 4), which is the path used for current sampling. The internal resistance of this conductive path is 1.2 mΩ typical, providing low power loss. The thickness of the copper conductor allows survival of

Continued on the next page...

Typical Application



Application 1. The ACS712 outputs an analog signal, V_{OUT}, that varies linearly with the uni- or bi-directional AC or DC primary sampled current, I_P, within the range specified. C_F is recommended for noise management, with values that depend on the application.

Description (continued)

the device at up to 5× overcurrent conditions. The terminals of the conductive path are electrically isolated from the signal leads (pins 5 through 8). This allows the ACS712 to be used in applications requiring electrical isolation without the use of opto-isolators or other costly isolation techniques.

The ACS712 is provided in a small, surface mount SOIC8 package. The leadframe is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is Pb-free, except for flip-chip high-temperature Pb-based solder balls, currently exempt from RoHS. The device is fully calibrated prior to shipment from the factory.

Selection Guide

Part Number	Packing*	T_A (°C)	Optimized Range, I_P (A)	Sensitivity, $Sens$ (Typ) (mV/A)
ACS712ELCTR-05B-T	Tape and reel, 3000 pieces/reel	−40 to 85	±5	185
ACS712ELCTR-20A-T	Tape and reel, 3000 pieces/reel	−40 to 85	±20	100
ACS712ELCTR-30A-T	Tape and reel, 3000 pieces/reel	−40 to 85	±30	66

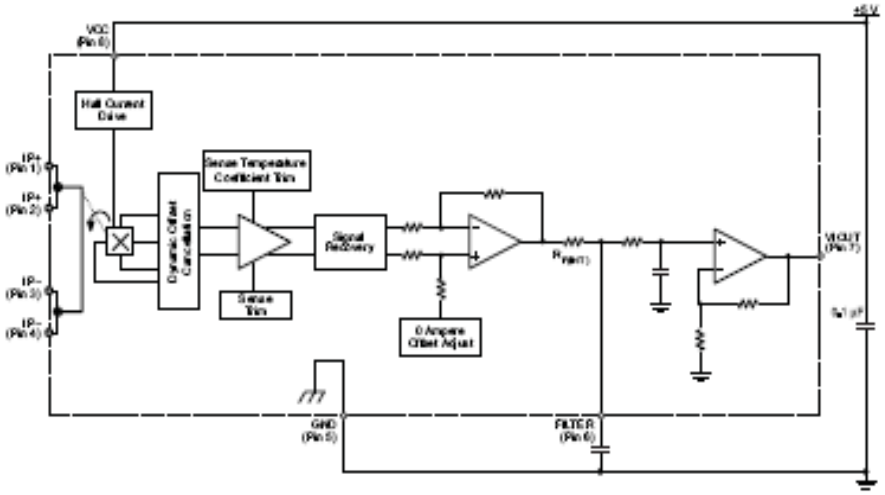
*Contact Allegro for additional packing options.

Absolute Maximum Ratings

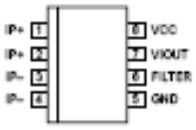
Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		8	V
Reverse Supply Voltage	V_{RCC}		−0.1	V
Output Voltage	V_{IOUT}		8	V
Reverse Output Voltage	V_{RIOUT}		−0.1	V
Reinforced Isolation Voltage	V_{ISO}	Pins 1-4 and 5-8; 60 Hz, 1 minute, T_A=25°C	2100	V
		Voltage applied to leadframe (Ip+ pins), based on IEC 60950	184	V_{peak}
Basic Isolation Voltage	$V_{ISO(bas)}$	Pins 1-4 and 5-8; 60 Hz, 1 minute, T_A=25°C	1500	V
		Voltage applied to leadframe (Ip+ pins), based on IEC 60950	354	V_{peak}
Output Current Source	$I_{IOUT(Source)}$		3	mA
Output Current Sink	$I_{IOUT(Sink)}$		10	mA
Overcurrent Transient Tolerance	I_P	1 pulse, 100 ms	100	A
Nominal Operating Ambient Temperature	T_A	Range E	−40 to 85	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		−65 to 170	°C

Parameter	Specification
Fire and Electric Shock	CAN/CSA-C22.2 No. 60950-1-03 UL 60950-1:2003 EN 60950-1:2001

Functional Block Diagram



Pin-out Diagram



Terminal List Table

Number	Name	Description
1 and 2	IP+	Terminals for current being sampled; fused internally
3 and 4	IP–	Terminals for current being sampled; fused internally
5	GND	Signal ground terminal
6	FILTER	Terminal for external capacitor that sets bandwidth
7	VIOUT	Analog output signal
8	VCC	Device power supply terminal

COMMON OPERATING CHARACTERISTICS[1] over full range of T_A, C_F = 1 nF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Supply Current	I_{CC}	V_{CC} = 5.0 V, output open	–	10	13	mA
Output Capacitance Load	C_{LOAD}	VIOUT to GND	–	–	10	nF
Output Resistive Load	R_{LOAD}	VIOUT to GND	4.7	–	–	kΩ
Primary Conductor Resistance	$R_{PRIMARY}$	T_A = 25°C	–	1.2	–	mΩ
Rise Time	t_r	$I_P = I_P$(max), T_A = 25°C, C_{OUT} = open	–	5	–	µs
Frequency Bandwidth	f	–3 dB, T_A = 25°C; I_P is 10 A peak-to-peak	–	80	–	kHz
Nonlinearity	E_{LIN}	Over full range of I_P	–	1.5	–	%
Symmetry	E_{SYM}	Over full range of I_P	98	100	102	%
Zero Current Output Voltage	$V_{IOUT(Q)}$	Bidirectional; I_P = 0 A, T_A = 25°C	–	$V_{CC} \times 0.5$	–	V
Power-On Time	t_{PO}	Output reaches 90% of steady-state level, T_J = 25°C, 20 A present on leadframe	–	35	–	µs
Magnetic Coupling[2]			–	12	–	G/A
Internal Filter Resistance[3]	$R_{F(INT)}$			1.7		kΩ

[1]Device may be operated at higher primary current levels, I_P, and ambient, T_A, and internal leadframe temperatures, T_A, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.

[2]1G = 0.1 mT.

[3]$R_{F(INT)}$ forms an RC circuit via the FILTER pin.

COMMON THERMAL CHARACTERISTICS[1]

			Min.	Typ.	Max.	Units
Operating Internal Leadframe Temperature	T_A	E range	–40	–	85	°C
					Value	Units
Junction-to-Lead Thermal Resistance[2]	$R_{\theta JL}$	Mounted on the Allegro ASEK 712 evaluation board			5	°C/W
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	Mounted on the Allegro 85-0322 evaluation board, includes the power consumed by the board			23	°C/W

[1]Additional thermal information is available on the Allegro website.

[2]The Allegro evaluation board has 1500 mm^2 of 2 oz. copper on each side, connected to pins 1 and 2, and to pins 3 and 4, with thermal vias connecting the layers. Performance values include the power consumed by the PCB. Further details on the board are available from the Frequently Asked Questions document on our website. Further information about board design and thermal performance also can be found in the Applications Information section of this datasheet.

x05B PERFORMANCE CHARACTERISTICS[1] T_A = −40°C to 85°C, C_F = 1 nF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		−5	–	5	A
Sensitivity	Sens	Over full range of I_P, T_A = 25°C	180	185	190	mV/A
Noise	$V_{NOISE(PP)}$	Peak-to-peak, T_A = 25°C, 185 mV/A programmed Sensitivity, C_F = 47 nF, C_{OUT} = open, 2 kHz bandwidth	–	21	–	mV
Zero Current Output Slope	$\Delta I_{OUT(Q)}$	T_A = −40°C to 25°C	–	−0.26	–	mV/°C
		T_A = 25°C to 150°C	–	−0.08	–	mV/°C
Sensitivity Slope	ΔSens	T_A = −40°C to 25°C	–	0.054	–	mV/A/°C
		T_A = 25°C to 150°C	–	−0.008	–	mV/A/°C
Total Output Error[2]	E_{TOT}	I_P = ±5 A, T_A = 25°C	–	±1.5	–	%

[1]Device may be operated at higher primary current levels, I_P, and ambient temperatures, T_A, provided that the Maximum Junction Temperature, $T_{J(max)}$, is not exceeded.

[2]Percentage of I_P, with I_P = 5 A. Output filtered.

x20A PERFORMANCE CHARACTERISTICS[1] T_A = −40°C to 85°C, C_F = 1 nF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		−20	–	20	A
Sensitivity	Sens	Over full range of I_P, T_A = 25°C	96	100	104	mV/A
Noise	$V_{NOISE(PP)}$	Peak-to-peak, T_A = 25°C, 100 mV/A programmed Sensitivity, C_F = 47 nF, C_{OUT} = open, 2 kHz bandwidth	–	11	–	mV
Zero Current Output Slope	$\Delta I_{OUT(Q)}$	T_A = −40°C to 25°C	–	−0.34	–	mV/°C
		T_A = 25°C to 150°C	–	−0.07	–	mV/°C
Sensitivity Slope	ΔSens	T_A = −40°C to 25°C	–	0.017	–	mV/A/°C
		T_A = 25°C to 150°C	–	−0.004	–	mV/A/°C
Total Output Error[2]	E_{TOT}	I_P = ±20 A, T_A = 25°C	–	±1.5	–	%

[1]Device may be operated at higher primary current levels, I_P, and ambient temperatures, T_A, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.

[2]Percentage of I_P, with I_P = 20 A. Output filtered.

x30A PERFORMANCE CHARACTERISTICS[1] T_A = −40°C to 85°C, C_F = 1 nF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	I_P		−30	–	30	A
Sensitivity	Sens	Over full range of I_P, T_A = 25°C	63	66	69	mV/A
Noise	$V_{NOISE(PP)}$	Peak-to-peak, T_A = 25°C, 66 mV/A programmed Sensitivity, C_F = 47 nF, C_{OUT} = open, 2 kHz bandwidth	–	7	–	mV
Zero Current Output Slope	$\Delta I_{OUT(Q)}$	T_A = −40°C to 25°C	–	−0.35	–	mV/°C
		T_A = 25°C to 150°C	–	−0.08	–	mV/°C
Sensitivity Slope	ΔSens	T_A = −40°C to 25°C	–	0.007	–	mV/A/°C
		T_A = 25°C to 150°C	–	−0.002	–	mV/A/°C
Total Output Error[2]	E_{TOT}	I_P = ±30 A, T_A = 25°C	–	±1.5	–	%

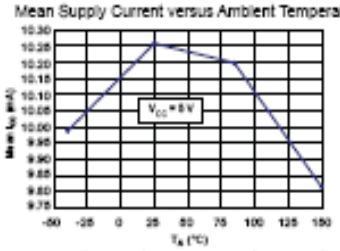
[1]Device may be operated at higher primary current levels, I_P, and ambient temperatures, T_A, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.

[2]Percentage of I_P, with I_P = 30 A. Output filtered.

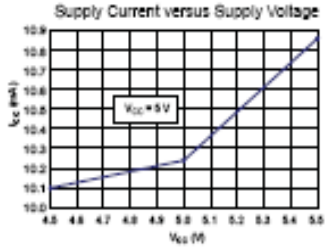
Characteristic Performance

I_P = 5 A, unless otherwise specified

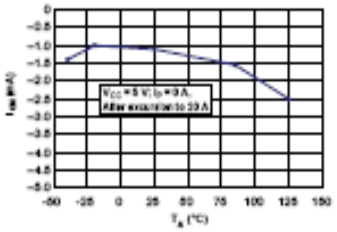
Mean Supply Current versus Ambient Temperature



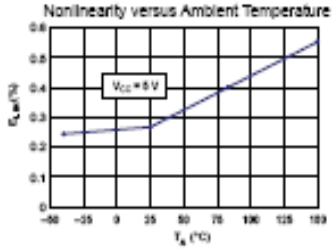
Supply Current versus Supply Voltage



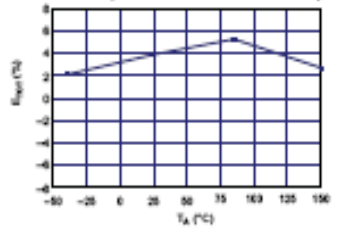
Magnetic Offset versus Ambient Temperature



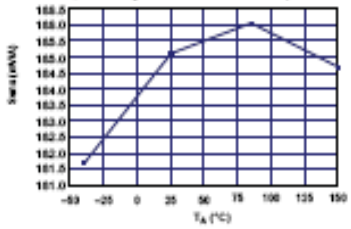
Nonlinearity versus Ambient Temperature



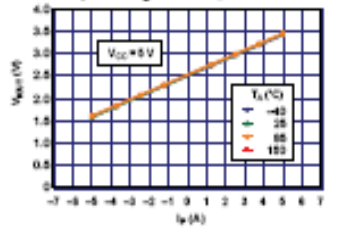
Mean Total Output Error versus Ambient Temperature



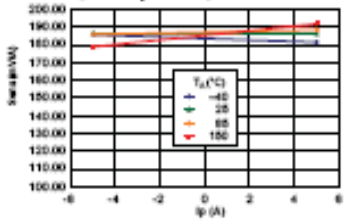
Sensitivity versus Ambient Temperature



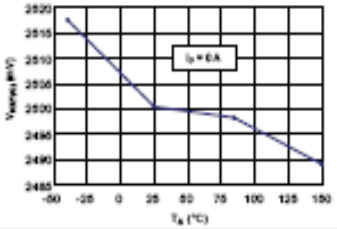
Output Voltage versus Sensed Current



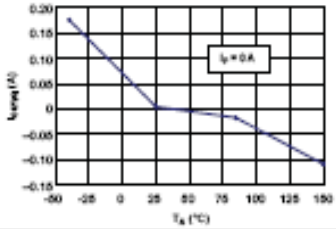
Sensitivity versus Sensed Current



0 A Output Voltage versus Ambient Temperature



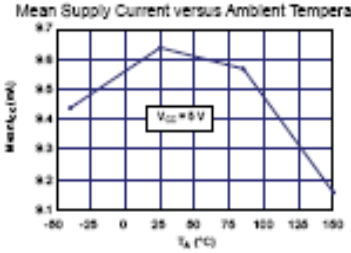
0 A Output Voltage Current versus Ambient Temperature



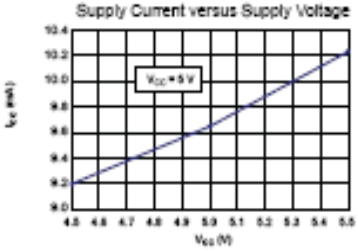
Characteristic Performance

I_P = 20 A, unless otherwise specified

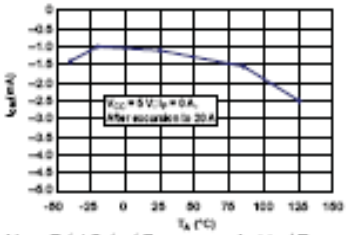
Mean Supply Current versus Ambient Temperature



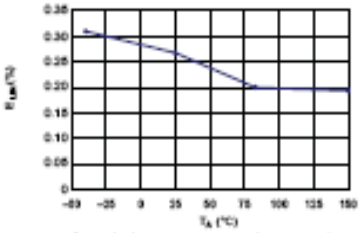
Supply Current versus Supply Voltage



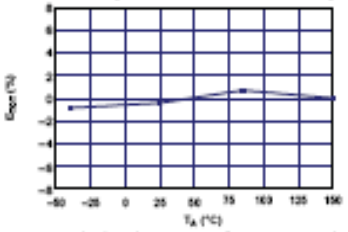
Magnetic Offset versus Ambient Temperature



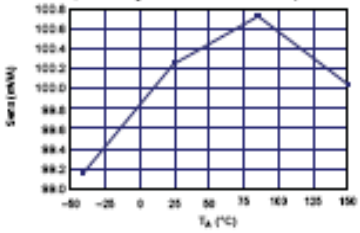
Nonlinearity versus Ambient Temperature



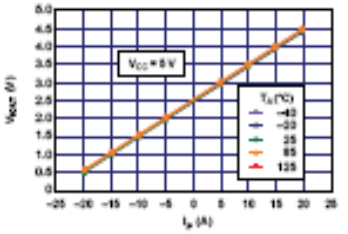
Mean Total Output Error versus Ambient Temperature



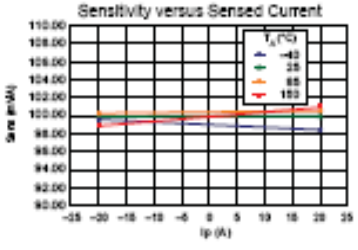
Sensitivity versus Ambient Temperature



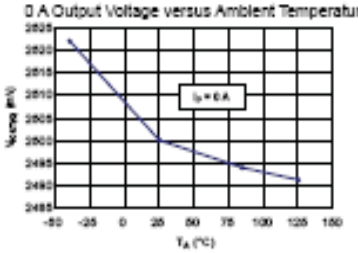
Output Voltage versus Sensed Current



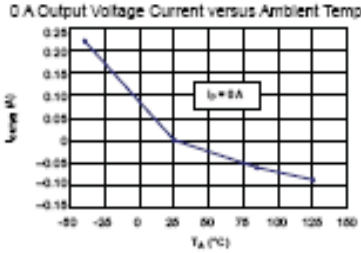
Sensitivity versus Sensed Current



0 A Output Voltage versus Ambient Temperature



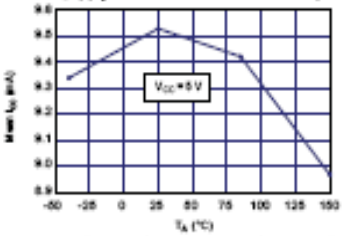
0 A Output Voltage Current versus Ambient Temperature



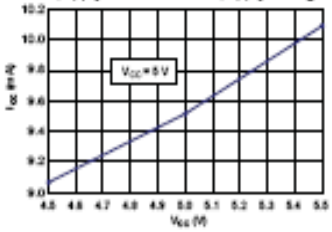
Characteristic Performance

I_P = 30 A, unless otherwise specified

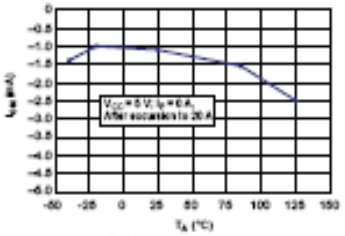
Mean Supply Current versus Ambient Temperature



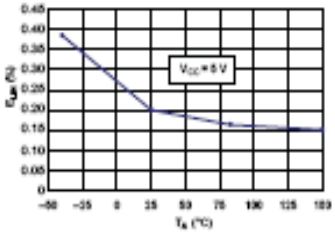
Supply Current versus Supply Voltage



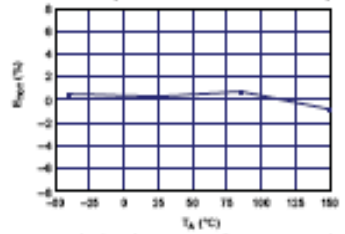
Magnetic Offset versus Ambient Temperature



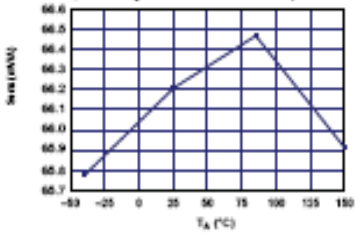
Nonlinearity versus Ambient Temperature



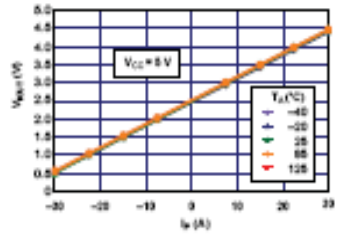
Mean Total Output Error versus Ambient Temperature



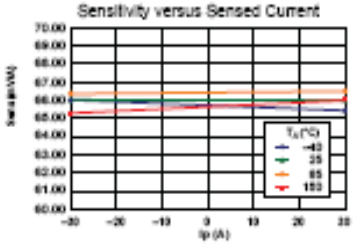
Sensitivity versus Ambient Temperature



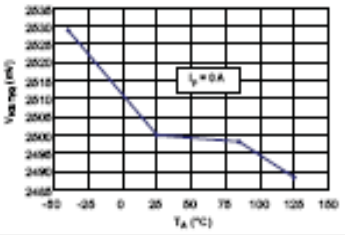
Output Voltage versus Sensed Current



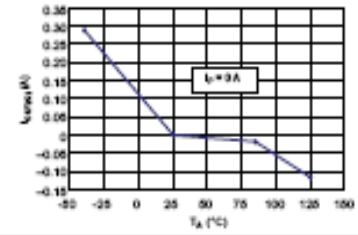
Sensitivity versus Sensed Current



0 A Output Voltage versus Ambient Temperature



0 A Output Voltage Current versus Ambient Temperature



Definitions of Accuracy Characteristics

Sensitivity (Sens). The change in device output in response to a 1A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the full-scale current of the device.

Noise (V_{NOISE}). The product of the linear IC amplifier gain (mV/G) and the noise floor for the Allegro Hall effect linear IC (≈1 G). The noise floor is derived from the thermal and shot noise observed in Hall elements. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

Linearity (E_{LIN}). The degree to which the voltage output from the IC varies in direct proportion to the primary current through its full-scale amplitude. Nonlinearity in the output can be attributed to the saturation of the flux concentrator approaching the full-scale current. The following equation is used to derive the linearity:

$$100\left(1-\left(\frac{\Delta\text{gain}\times\%\text{ sat}\left(V_{IOUT\_full\text{-}scale\ amperes}-V_{IOUT(Q)}\right)}{2\left(V_{IOUT\_half\text{-}scale\ amperes}-V_{IOUT(Q)}\right)}\right)\right)$$

where $V_{IOUT\_full\text{-}scale\ amperes}$ = the output voltage (V) when the sampled current approximates full-scale $\pm I_P$.

Symmetry (E_{SYM}). The degree to which the absolute voltage output from the IC varies in proportion to either a positive or negative full-scale primary current. The following formula is used to derive symmetry:

$$100\left(\frac{V_{IOUT\_+\text{ full-scale amperes}}-V_{IOUT(Q)}}{V_{IOUT(Q)}-V_{IOUT\_-\text{full-scale amperes}}}\right)$$

Quiescent output voltage ($V_{IOUT(Q)}$). The output of the device when the primary current is zero. For a unipolar supply voltage, it nominally remains at $V_{CC}/2$. Thus, V_{CC} = 5 V translates into $V_{IOUT(Q)}$ = 2.5 V. Variation in $V_{IOUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

Electrical offset voltage (V_{OE}). The deviation of the device output from its ideal quiescent value of $V_{CC}/2$ due to nonmagnetic causes. To convert this voltage to amperes, divide by the device sensitivity, Sens.

Accuracy (E_{TOT}). The accuracy represents the maximum deviation of the actual output from its ideal value. This is also known as the total output error. The accuracy is illustrated graphically in the output voltage versus current chart at right.

Accuracy is divided into four areas:

- **0 A at 25°C.** Accuracy at the zero current flow at 25°C, without the effects of temperature.
- **0 A over Δ temperature.** Accuracy at the zero current flow including temperature effects.
- **Full-scale current at 25°C.** Accuracy at the the full-scale current at 25°C, without the effects of temperature.
- **Full-scale current over Δ temperature.** Accuracy at the full-scale current flow including temperature effects.

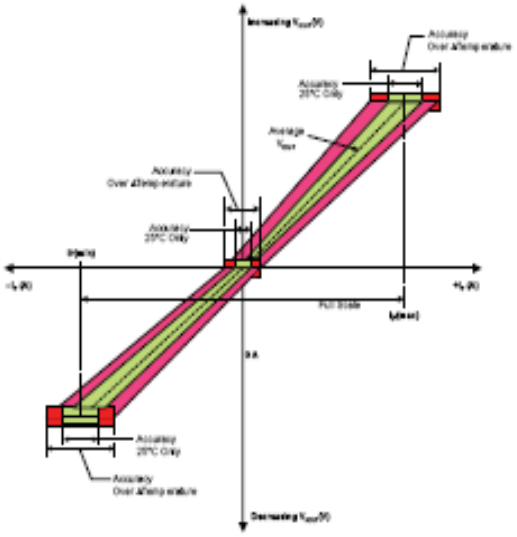
Ratiometry. The ratiometric feature means that its 0 A output, $V_{IOUT(Q)}$, (nominally equal to $V_{CC}/2$) and sensitivity, Sens, are proportional to its supply voltage, V_{CC}. The following formula is used to derive the ratiometric change in 0 A output voltage, $\Delta V_{IOUT(Q)RAT}$ (%).

$$100\left(\frac{V_{IOUT(Q)VCC}/V_{IOUT(Q)5V}}{V_{CC}/5\text{ V}}\right)$$

The ratiometric change in sensitivity, $\Delta Sens_{RAT}$ (%), is defined as:

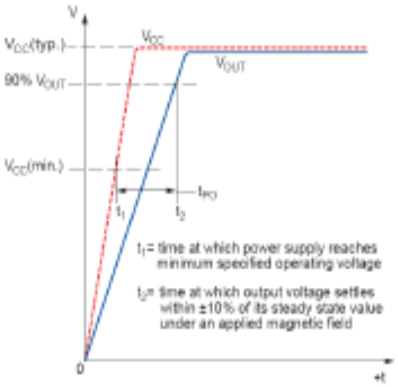
$$100\left(\frac{Sens_{VCC}/Sens_{5V}}{V_{CC}/5\text{ V}}\right)$$

Output Voltage versus Sampled Current
Accuracy at 0 A and at Full-Scale Current

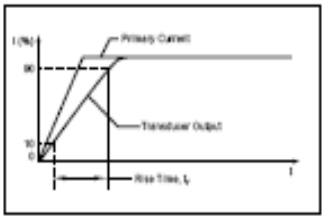


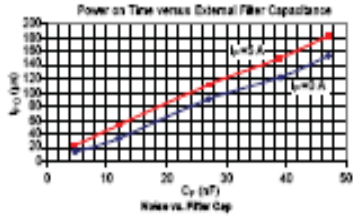
Definitions of Dynamic Response Characteristics

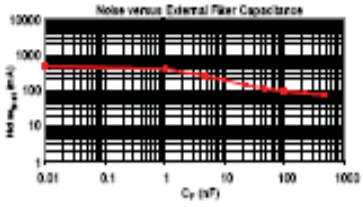
Power-On Time (t_{PO}). When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field. Power-On Time, t_{PO}, is defined as the time it takes for the output voltage to settle within ±10% of its steady state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in the chart at right.

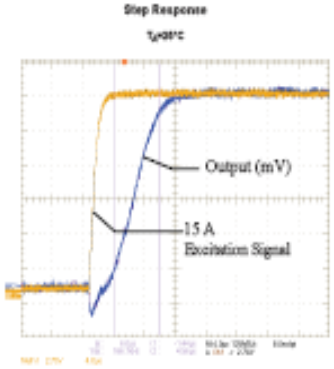


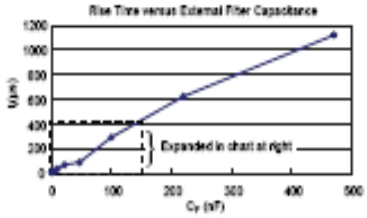
Rise time (t_r). The time interval between a) when the device reaches 10% of its full scale value, and b) when it reaches 90% of its full scale value. The rise time to a step response is used to derive the bandwidth of the device, in which $f(-3\ dB) = 0.35/t_r$. Both t_r and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.



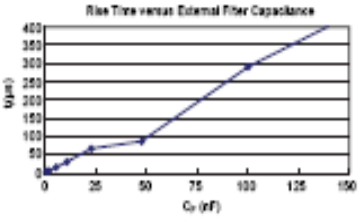








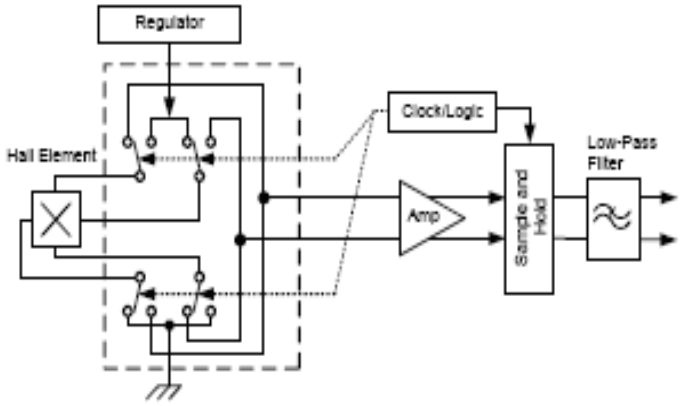
C_F (nF)	t_r (µs)
0	6.6
1	7.7
4.7	17.4
10	32.1
22	68.2
47	88.2
100	291.3
220	623.0
470	1120.0



Chopper Stabilization Technique

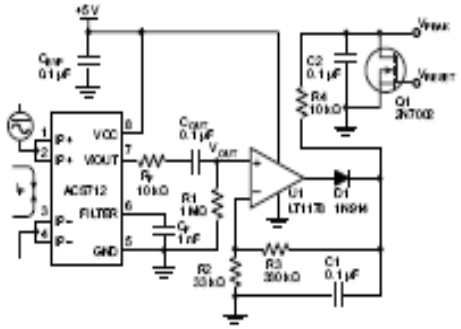
Chopper Stabilization is an innovative circuit technique that is used to minimize the offset voltage of a Hall element and an associated on-chip amplifier. Allegro patented a Chopper Stabilization technique that nearly eliminates Hall IC output drift induced by temperature or package stress effects. This offset reduction technique is based on a signal modulation-demodulation process. Modulation is used to separate the undesired DC offset signal from the magnetically induced signal in the frequency domain. Then, using a low-pass filter, the modulated DC offset is suppressed while the magnetically induced signal passes through the filter. As a result of this chopper stabilization approach, the output voltage from the Hall IC is desensitized to the effects of temperature and mechanical stress. This technique produces devices that have an extremely stable Electrical Offset Voltage, are immune to thermal stress, and have precise recoverability after temperature cycling.

This technique is made possible through the use of a BiCMOS process that allows the use of low-offset and low-noise amplifiers in combination with high-density logic integration and sample and hold circuits.

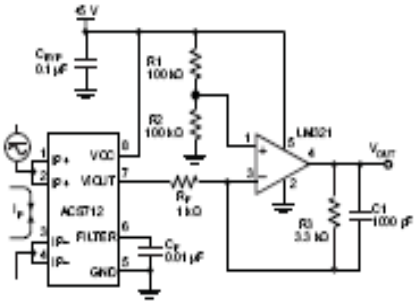


Concept of Chopper Stabilization Technique

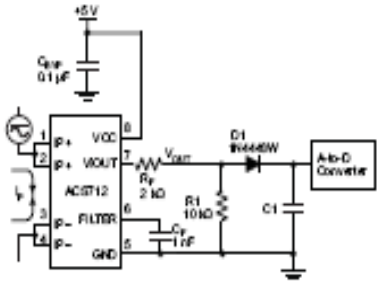
Typical Applications



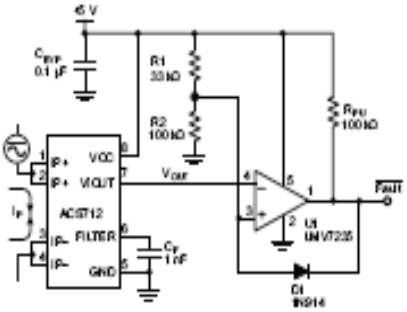
Application 2. Peak Detecting Circuit



Application 3. This configuration increases gain to 610 mV/A (tested using the ACS712ELC-05A).



Application 4. Rectified Output. 3.3 V scaling and rectification application for A-to-D converters. Replaces current transformer solutions with simpler ACS circuit. C1 is a function of the load resistance and filtering desired. R1 can be omitted if the full range is desired.



Application 5. 10 A Overcurrent Fault Latch. Fault threshold set by R1 and R2. This circuit latches an overcurrent fault and holds it until the 5 V rail is powered down.

Improving Sensing System Accuracy Using the FILTER Pin

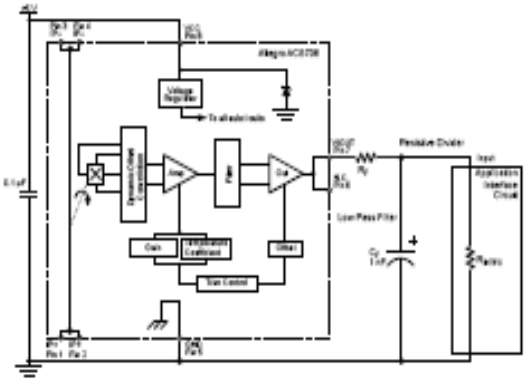
In low-frequency sensing applications, it is often advantageous to add a simple RC filter to the output of the device. Such a low-pass filter improves the signal-to-noise ratio, and therefore the resolution, of the device output signal. However, the addition of an RC filter to the output of a sensor IC can result in undesirable device output attenuation — even for DC signals.

Signal attenuation, ΔV_{ATT}, is a result of the resistive divider effect between the resistance of the external filter, R_F (see Application 6), and the input impedance and resistance of the customer interface circuit, R_{INTFC}. The transfer function of this resistive divider is given by:

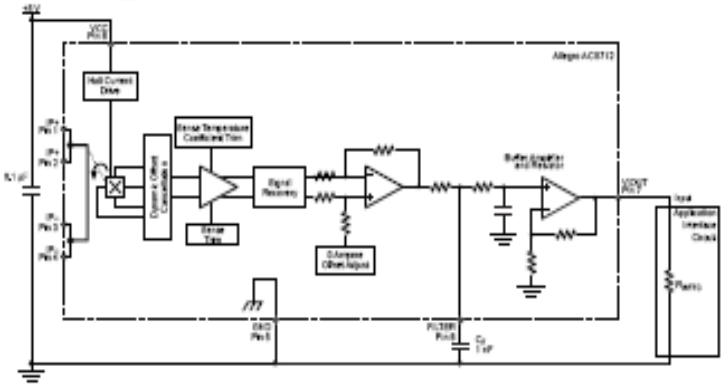
$$\Delta V_{ATT} = V_{IOUT}\left(\frac{R_{INTFC}}{R_F + R_{INTFC}}\right) .$$

Even if R_F and R_{INTFC} are designed to match, the two individual resistance values will most likely drift by different amounts over temperature. Therefore, signal attenuation will vary as a function of temperature. Note that, in many cases, the input impedance, R_{INTFC}, of a typical analog-to-digital converter (ADC) can be as low as 10 kΩ.

The ACS712 contains an internal resistor, a FILTER pin connection to the printed circuit board, and an internal buffer amplifier. With this circuit architecture, users can implement a simple RC filter via the addition of a capacitor, C_F (see Application 7) from the FILTER pin to ground. The buffer amplifier inside of the ACS712 (located after the internal resistor and FILTER pin connection) eliminates the attenuation caused by the resistive divider effect described in the equation for ΔV_{ATT}. Therefore, the ACS712 device is ideal for use in high-accuracy applications that cannot afford the signal attenuation associated with the use of an external RC low-pass filter.

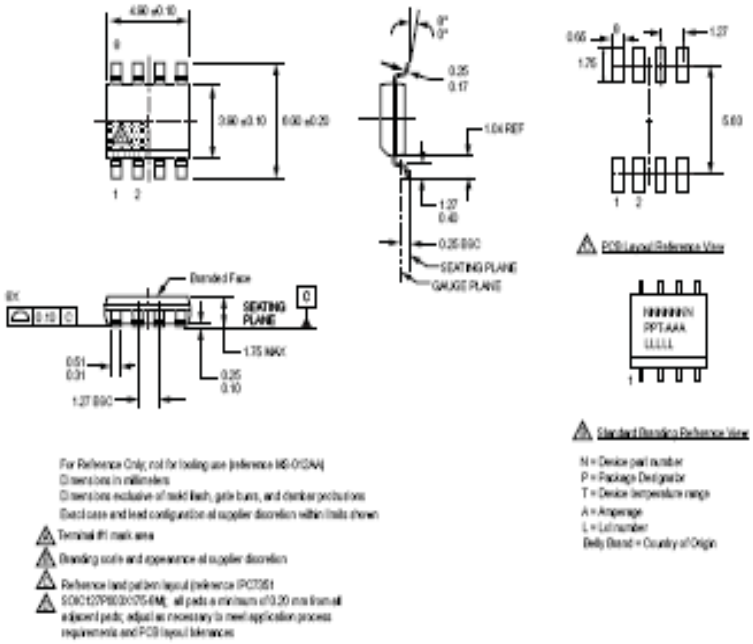


Application 6. When a low pass filter is constructed externally to a standard Hall effect device, a resistive divider may exist between the filter resistor, R_F, and the resistance of the customer interface circuit, R_{INTFC}. This resistive divider will cause excessive attenuation, as given by the transfer function for ΔV_{ATT}.



Application 7. Using the FILTER pin provided on the ACS712 eliminates the attenuation effects of the resistor divider between R_F and R_{INTFC}, shown in Application 6.

Package LC, 8-pin SOIC



APPENDIX F

AR-ELCB Programming

EARTH LEAKAGE CIRCUIT BREAKER WITH AN AUTO RE-CLOSER UNIT PROGRAMMING USING PIC BASIC

```
#include <18F4550.h>
#device adc=8
#use delay(clock=20000000)
#FUSES NOWDT,HS,NOPROTECT,NOBROWNOUT,NOLVP

// LCD STUFF
#define LCD_D0      PIN_B4
#define LCD_D1      PIN_B5
#define LCD_D2      PIN_B6
#define LCD_D3      PIN_B7
#define LCD_RW      PIN_B1
#define LCD_EN      PIN_B3
#define LCD_RS      PIN_B0
#define LINE_1      0x00
#define LINE_2      0x40
#define CLEAR_DISP  0x01
#define DEGREE_SYM  0xdf

void LCD_Init ( void );
void LCD_SetPosition ( unsigned int cX );
void LCD_PutChar ( unsigned int cX );
void LCD_PutCmd ( unsigned int cX );
void LCD_PulseEnable ( void );
void LCD_SetData ( unsigned int cX );

void main()
{byte s1,s2,diff;
 int count;
 count=0;

 delay_ms ( 200 );
 output_low(PIN_B1);
 LCD_Init();
 LCD_SetPosition ( LINE_1 + 4 );
 printf ( LCD_PutChar, "SYAFII");
 LCD_SetPosition ( LINE_2 + 5 );
 printf ( LCD_PutChar, "EC07074");
 delay_ms(3000);
 LCD_SetPosition ( LINE_1 + 1 );
 printf ( LCD_PutChar, "AUTO RECLOSER");
 LCD_SetPosition ( LINE_2 + 5 );
```

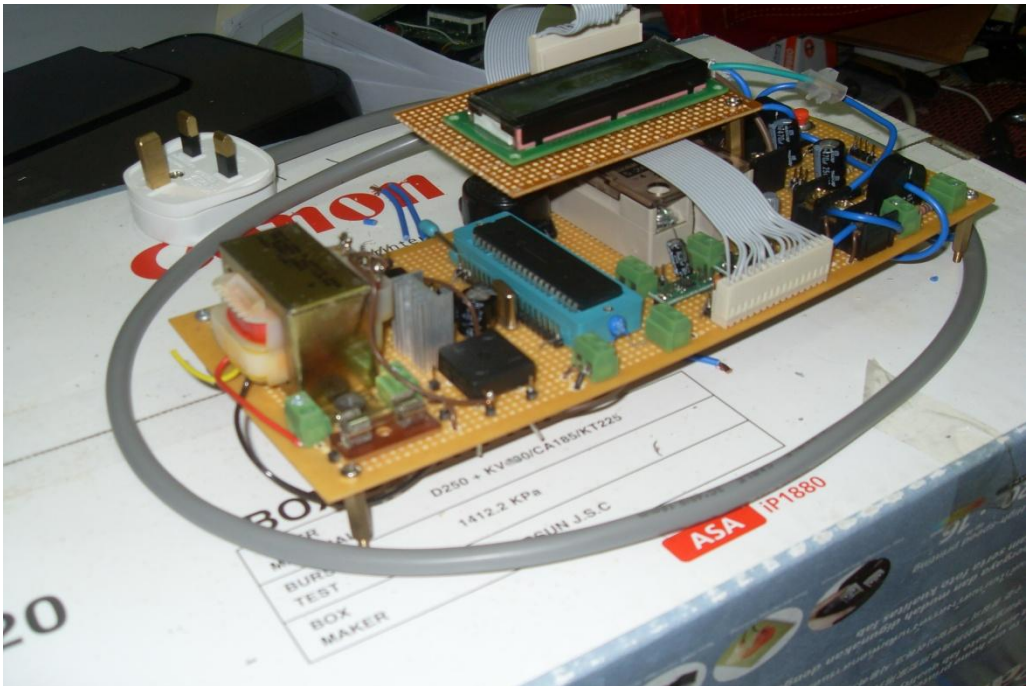
```
printf ( LCD_PutChar, " ELCB     ");
delay_ms(3000);
//adc
setup_adc_ports(AN0_TO_AN1|VSS_VDD);
setup_adc(ADC_CLOCK_DIV_32);

while ( TRUE )
 {
  set_adc_channel(0);
  delay_us(80);
  s1=read_adc();

  set_adc_channel(1);
  delay_us(80);
  s2=read_adc();

  output_high(PIN_B2);

  diff=s2-s1;

  if(diff>1){          //DIFFERENT CURRENT
  output_low(PIN_B2);
  delay_ms(10000);
  output_high(PIN_B2);
  LCD_SetPosition ( LINE_1 + 3 );
  printf ( LCD_PutChar, "TEMPORARY");
  LCD_SetPosition ( LINE_2 + 5 );
  printf ( LCD_PutChar, "FAULT");
  delay_ms(5000);
  count++;}

  LCD_Init();

  if(count>=3)
  {
  while(true)
  {
  output_low(PIN_B2);
  output_high(PIN_D1);
  LCD_SetPosition ( LINE_1 + 3 );
  printf ( LCD_PutChar, "PERMANENT");
  LCD_SetPosition ( LINE_2 + 5 );
  printf ( LCD_PutChar, "FAULT");
  }
  }

 }
```

```
 }

void LCD_Init ( void )
   {
   LCD_SetData ( 0x00 );
   delay_ms ( 200 );      // wait enough time after Vdd rise
   output_low ( LCD_RS );
   LCD_SetData ( 0x03 );   // init with specific nibbles to start 4-bit mode
   LCD_PulseEnable();
   LCD_PulseEnable();
   LCD_PulseEnable();
   LCD_SetData ( 0x02 );   // set 4-bit interface
   LCD_PulseEnable();      // send dual nibbles hereafter, MSN first
   LCD_PutCmd ( 0x2C );    // function set (all lines, 5x7 characters)
   LCD_PutCmd ( 0x0C );    // display ON, cursor off, no blink
   LCD_PutCmd ( 0x01 );    // clear display
   LCD_PutCmd ( 0x06 );    // entry mode set, increment
   }

void LCD_SetPosition ( unsigned int cX )
   {
   // this subroutine works specifically for 4-bit Port A
   LCD_SetData ( swap ( cX ) | 0x08 );
   LCD_PulseEnable();
   LCD_SetData ( swap ( cX ) );
   LCD_PulseEnable();
   }

void LCD_PutChar ( unsigned int cX )
   {
   // this subroutine works specifically for 4-bit Port A
   output_high ( LCD_RS );
   LCD_SetData ( swap ( cX ) );     // send high nibble
   LCD_PulseEnable();
   LCD_SetData ( swap ( cX ) );     // send low nibble
   LCD_PulseEnable();
   output_low ( LCD_RS );
   }

void LCD_PutCmd ( unsigned int cX )
   {
   // this subroutine works specifically for 4-bit Port A
   LCD_SetData ( swap ( cX ) );     // send high nibble
   LCD_PulseEnable();
   LCD_SetData ( swap ( cX ) );     // send low nibble
   LCD_PulseEnable();
   }
```

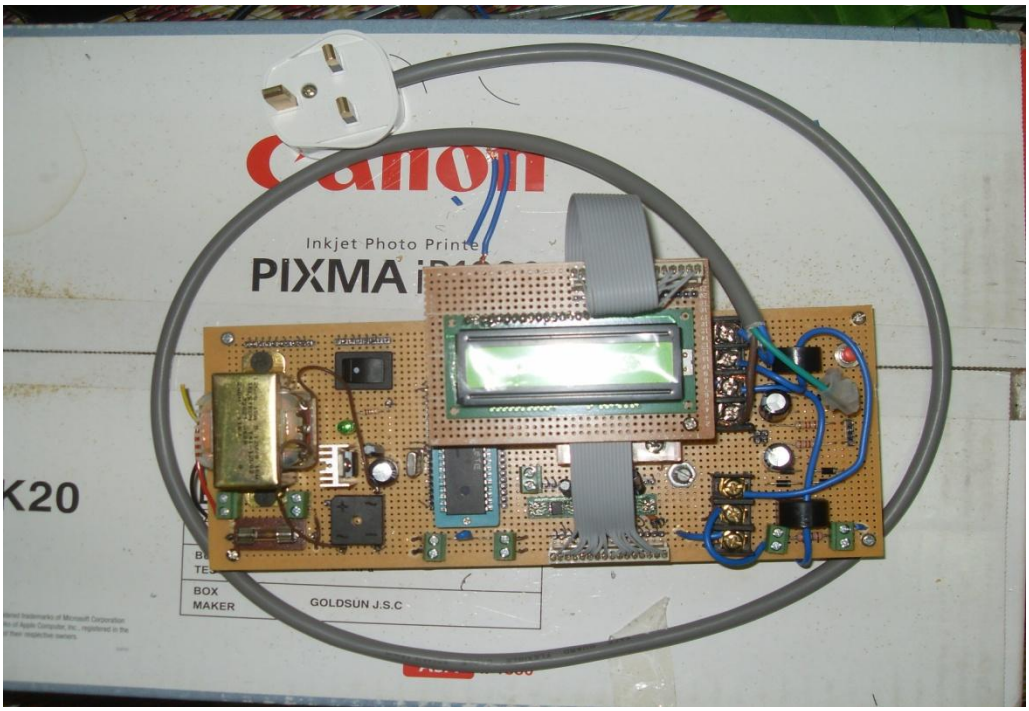
```
void LCD_PulseEnable ( void )
   {
   output_high ( LCD_EN );
   delay_us ( 10 );
   output_low ( LCD_EN );
   delay_ms ( 5 );
   }

void LCD_SetData ( unsigned int cX )
   {
   output_bit ( LCD_D0, cX & 0x01 );
   output_bit ( LCD_D1, cX & 0x02 );
   output_bit ( LCD_D2, cX & 0x04 );
   output_bit ( LCD_D3, cX & 0x08 );
   }
```

APPENDIX G

AR-ELCB HARDWARE PICTURE



FULL VIEW



TOP VIEW

APPENDIX H

Biodata of the Author

AUTHOR'S BIODATA

Muhammad syafi'i bin ali was born on 27th august 1986 in kg.Pantai Merchang,Marang Terengganu.His permanent address is at 265,Kg. Pantai Merchang,21610 Marang Terengganu.He is a youngest brother from seven siblings,He has 5 sister and one brother.His first education is Sekolah Rendah Kebangsaan Merchang.Then he continue secondary education in Sekolah Menengah Kebangsaan Merchang. In secondary school, he takes pure science education and learn some knowledge like biology, physic and chemical. After he completed his studies in pure science course at 2003,he decide to learn and explore knowledge about engineering course. Then he continue study at University Malaysia Pahang in diploma of electrical engineering(electronic industry)course in 2004.Since 2007,he enter to continue with degree of electrical power.He is currently a bachelor student in Electrical Engineering(Power System), faculty of Electrical and Electronics Engineering, University Malaysia Pahang. His research fields are power electronics and power system. He is a student member of the IEM of Malaysia.