18V TO 1000V BOOST CONVERTER

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This thesis is submitted as partial fulfillment of the requirements for the award of the Bachelor of Electrical Engineering (Hons.) (Electronics)

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Date : 23 NOVEMBER 2009

DEDICATION

Specially dedicated to

My beloved father and mother,

To my family and friends

Thanks for all the encouragement and support

ACKNOWLEDGEMENT

First of all, praise to God the most gracious and merciful that I have been able to finish this final year project (PSM) in the mean time.

During this project, I receive contribution and support from many people. In particular, I would like to express my thanks to my supervisor, Encik Abdul Halim bin Mohd Hanafi for his ideas, encouragements, guidances and his kindness to me in order to finish this project.

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Last but not least, I would like to dedicate my appreciation to all my friends who assisted me upon my request and were very helpful with their ideas.

ABSTRACT

Recent advances in semiconductor, magnetic and passive technologies make the switching power supply an ever more popular choice in the power conversion arena today. These supplies offer lightweight, smaller footprints and improved efficiencies over traditional power supplies. The objective of this project is to develop a boost converter which can be operated in many ways in order to obtain the desired output. The operation of power supply circuits was built by using microcontroller and pulse width modulator (PWM) which can produce a PWM as an input from the controller for the boost circuit. This project has been divided into two, using PIC16F877A and using pulse modulator, SG3525AN. The boost topology is used in the circuit for arrangement of the power devices and the other elements. The frequency and period of the pulse width has to be determined first in order to get the 1000V output. C Compiler software is used to program the PIC16F877. For SG3525AN, it will generate the pulse by itself to be supply to the boost circuit. As the result, the direct current (DC) 1000V output voltage remains constant through the time. This boost converter can be used for multipurpose and further research need to be done to complete this circuit to the full potential.

ABSTRAK

Perkembangan teknologi semikonduktor, magnetic dan pasif the membuatkan pembekal kuasa menjadi semakin popular di dalam arena pengubahan kuasa pada hari ini. Pembekal kuasa seperti ini memberikan kelebihan dari segi saiz yang kecil, rekaan yang lebih ringkas dan kecekapan yang lebih bagus berbanding pembekal kuasa tradisional. Objektif untuk projek ini ada untuk menghasilkan “boost converter” yang boleh dikendalikan dengan pelbagai cara untuk mendapatkan keluaran yang dikehendaki. Operasi untuk litar ini dibina menggunakan “microcontroller” and “Pulse Width Modulator” yang akan menghasilkan gelombang sebagai input dari kawalan untuk litar ini. Projek ini dibahagikan kepada dua bahagian, iaitu menggunakan PIC16F877A dan juga SG3525AN. Topologi anjakan untuk litar digunakan dalam susunan alatan kuasa dan elemen yang lain. Frekuensi dan jangka masa gelombang kena ditentukan untuk mendapatkan keluaran sebanyak 1000V. Penggunaan perisian C Compiler turut digunakan untuk membuat program bagi PIC16F877A. Untuk SG3525AN pula, ianya mampu mengeluarkan gelombang semdiri untuk dibekalkan. 1000V dapat dihasilkan. Pembekal kuasa seperti ini boleh digunakan untuk pelbagai kegunaan dan kajian yang lebih mendalam perlu dijalankan agar litar ini bole mencapai keupayaan yang sebenar.

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V	-	Voltage
V_o	-	Voltage Output
V_s	-	Voltage Supply
C	-	Capacitor
D	-	Diode
L	-	Inductor
Ω	-	ohm
PWM	-	Pulse Width Modulator
A	-	Ampere
I	-	Current

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CHAPTER 1

INTRODUCTION

1.1 Overview

The title of this project is 18V to 1000V Boost Converter. This converter also known as the step-up converter that is another switching converter that has the same components as the buck converter, but this converter produces an output voltage greater than the source. For an ideal boost converter has the five basic components, namely a power semiconductor switch, a diode, an inductor a capacitor and a Pulse Width Modulator (PWM) controller. The placement of the inductor, the switch and the diode in the boost converter is the differences of this type of converter compares with the buck converter.

This project is divided into two different methods because this project is mainly to do analysis, comparisons and data collections to determine which method are more reliable, cost savings and high efficiency. For the first method, application of PWM oscillator applied because this oscillator can generate pulse which is 1000V as an output.

The second method is a microcontroller used to control the circuit. The reason for this method is to manipulate the generate pulse that produce by the microcontroller in order to obtain the 1000V output.

1.2 Background

The advent of commercial semiconductor switch in the 1950's represented a major milestone that made Switched-Mode Power Supply (SMPS) such as possible. The SMPS have high efficiency since it can switch turn ON and OFF quickly and have low losses. The major DC to DC converters were developed early 1960s when the switches had become available. The rapid development of this technology has become an advantage for the aerospace industries since the need for small, lightweight and efficient power converters.[10]

Switched systems such as SMPS are a challenge to design since its model depends on whether a switch is opened or closed. R.D. Middlebrook from Caltech in 1977 published the models for DC to DC converters used today. Middlebrook averaged the circuit configurations for each switch state in a technique called state-space averaging. This simplification reduced two systems into one. The new model led to insightful design equations which helped SMPS growth.[10]

1.3 Problem Statement

The increase in demand of power has greatly improved the converter. Even today's car also known as Hybrid Electric Vehicle (HEV) uses electric energy. For example, Toyota Prius HEV. The Toyota Prius HEV contains a motor which utilizes voltages of approximately 500 V. Without a boost converter, the Prius would need nearly 417 cells to power the motor. However, a Prius actually uses only 168 cells and boosts the battery voltage from 202 V to 500 V.

Besides the increase of power demand, an application which is cost savings to build also has been the main issue for this project. Besides being cost savings, this project also must be portable, space savings (small) and easy to be keep.

Lastly, this application must be high efficiency, reliable and long life cycle. Because of user demand, this also has become the main issue and one of the main ideas for this project. User would attract with the end product if it has the above specifications because user tend to buy or use an application which they can rely on for a long time with high efficiency.

1.4 Objectives

Every project must have the objectives to achieve. And these objectives will be the guideline for the completion of this project. For this project, 18V to 1000V boost converter is developed with the listed objectives below:

I. To know the application of the PWM generator.

II. To the input of 18V to 1000V.

III. Application of the Power MOSFET.

IV. Analysis on each system by collecting data.

1.5 Scope of Project

In order to achieve the objectives of the project, there are several scope has been outlined as followed:

I. Using microcontroller.

For this project, PIC16F877A have been selected. The reasons of selection this microcontroller are explain in Chapter 3.

II. Using PWM oscillator.

SG 3525AN have been selected for this project because of the function that this PWM oscillator can provide. More explanations are available in Chapter 3.

III. Application of power MOSFET.

For this project, power MOSFET IRFBG30 has been selected. This power MOSFET is selected because it suitable for this project. Explanation are provide in Chapter 3.

1.6 Outline of Thesis

This thesis consists of five chapters. In the first chapter, this chapter discussed the overall idea of this project is discussed which including objectives of project, problem statement, the scope of this project and outline of this thesis.

Chapter 2 is discuss more on theory and literature review that have been done. It well discusses about the boost converter, basic concept of the converter, PIC 16F877 microcontroller, SG3525A-Pulse Width Modulator Control Circuit, power MOSFET and programming tools used in this project.

Chapter 3 describes the methodology of the hardware and software implementation of this project. The tools, components and software used to accomplish the project also discussed in this chapter.

Chapter 4 presents a discussion of the implementation, result and analysis of the whole project. This chapter also explains the justification of some failure had happen in this project.

Chapter 5 provides the conclusions of the project. There are also several suggestions that can be used for future implementation or upgrading for this project.

CHAPTER 2

THEORY AND LITERATURE REVIEW

2.1 Overview

This chapter includes all the paper works and related research as well as the studies regards to this project. The chapter includes all important studies which have been done previously by other research work. The related works have been referred carefully since some of the knowledge and suggestions from the previous work can be implemented for this project.

Literature review was an ongoing process throughout the whole process of the project. It is very essential to refer to the variety of sources in order to gain more knowledge and skills to complete this project. These sources include reference books, thesis, journals and also the materials obtained from internet.

At the beginning of the project, the basic concept of the boost converter has been well understood. In addition, the function of all the components used in this project such as the microcontroller PIC16F877A, PWM Oscillator SG3525A, and Power MOSFET was explored first before starting the project.

2.2 The Basic Concept of Boost Converter

The boost converter, also known as the step-up converter, is another switching converter that has the same components as the buck converter, but this converter produces an output voltage greater than the source. The ideal boost converter has the five basic components, namely a power semiconductor switch, a diode, an inductor, a capacitor and a PWM controller. The placement of the inductor, the switch and the diode in the boost converter is different from that of the buck converter. The basic circuit of the boost converter is shown in Figure. 2.1.

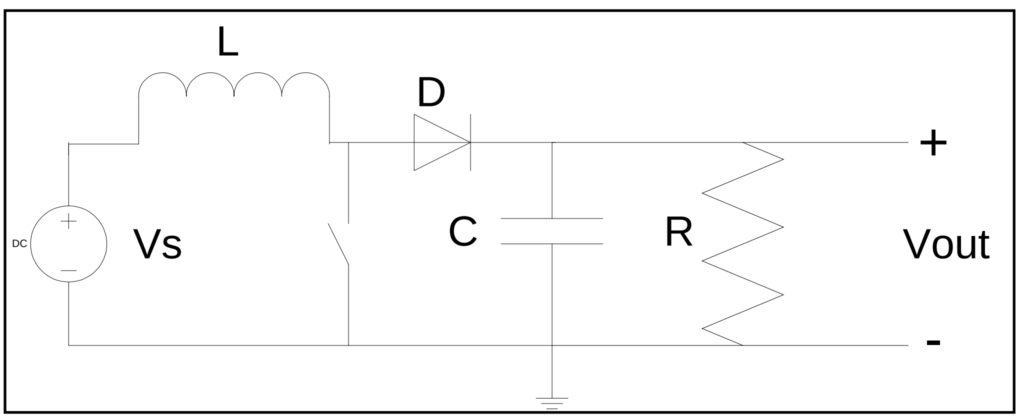


Figure 2.1: Boost Converter Basic Circuit [5]

The operation of the circuit is explained now. The essential control mechanism of the circuit in Figure 2.1 is turning the power semiconductor switch on and off. When the switch is ON, the current through the inductor increases and the energy stored in the inductor builds up. When the switch is off, current through the inductor continues to flow via the diode D, the RC network and back to the source. The inductor is discharging its energy and the polarity of inductor voltage is such that its terminal connected to the diode is positive with respect to its other terminal connected to the source. It can be seen then the capacitor voltage has to be higher than the source voltage and hence this converter is known as the boost converter. It can be seen that the inductor acts like a pump, receiving energy when the switch is closed and transferring it to the RC network when the switch is open. [5]

When the switch is closed, the diode does not conduct and the capacitor sustains the output voltage. The circuit can be split into two parts, as shown in Figure 2.2. As long as the RC time constant is very much larger than the on-period of the switch, the output voltage would remain more or less constant. [5]

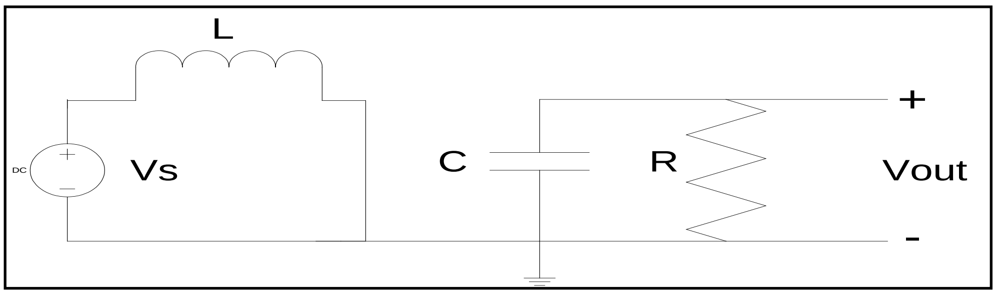


Figure 2.2: Switch Closed State [5]

When the switch is open, the equivalent circuit that is applicable is shown in Figure 2.3. There is a single connected circuit in this case.

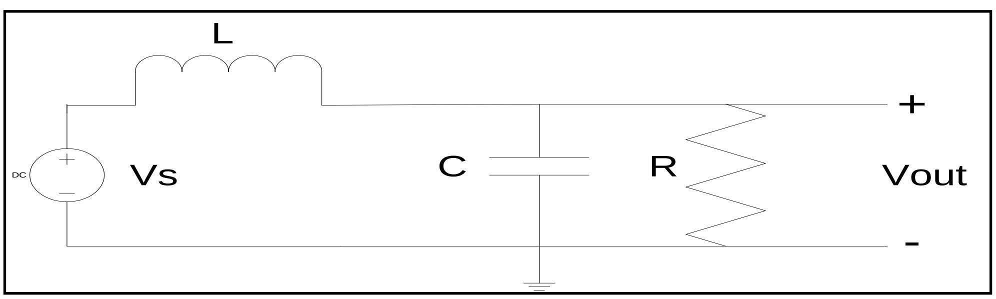


Figure 2.3: Switch Open State [5]

2.3 The Pulse Width Modulation (PWM) Signal

Pulse width modulation (PWM) is a powerful technique for controlling analog circuits with a processor's digital outputs. PWM is employed in a wide variety of applications, ranging from measurement and communications to power control and conversion.

The PWM signal is still digital because, at any given instant of time, the full DC supply is either fully on or fully off. The voltage or current source is supplied to the analog load by means of a repeating series of on and off pulses. The on-time is the time during which the DC supply is applied to the load, and the off-time is the period during which the supply is switched off. [2]

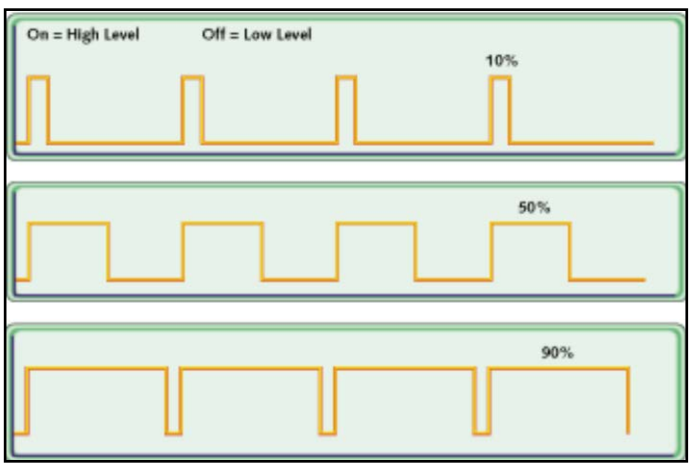


Figure 2.4: PWM signals of varying duty cycles [2]

Figure 2.4 show three different PWM signals. The upper signal shows a PWM output at a 10% duty cycle. That is, the signal is on for 10% of the period and off the other 90%. The middle and bottom show PWM outputs at 50% and 90% duty cycles, respectively. These three PWM outputs encode three different analog signal values, at 10%, 50%, and 90% of the full strength. By controlling analog circuits digitally, system costs and power consumption can be drastically reduced. What's more, many microcontrollers and DSPs already include on-chip PWM controllers, making implementation easy. PWM is economical, space saving, and noise immune.

2.4 Hardware Devices/Components

2.4.1 PIC Microcontroller

PIC is a family of Harvard architecture microcontrollers made by Microchip Technology, derived from the PIC1650 originally developed by General Instrument's Microelectronics Division. The name PIC was originally an acronym for "Programmable Intelligent Computer".

PICs are popular with developers and hobbyists alike due to their low cost, wide availability, large user base, extensive collection of application notes, availability of low cost or free development tools, and serial programming (and reprogramming with flash memory) capability.

The PIC architecture is distinctively minimalist. It is characterized by the following features with separate code and data spaces have a small number of fixed length instructions. Most instructions are single cycle execution (4 clock cycles), with single delay cycles upon branches and skips. Has a single accumulator (W), the use of which (as source operand) is implied (i.e. is not encoded in the op-code). All RAM locations function as registers as both sources 12 and/or destination of math and other functions. Has a hardware stack for storing return addresses also has a fairly small amount of addressable data space (typically 256 bytes), extended through banking. Data space mapped CPU, port, and peripheral registers. The program counter is also mapped into the data space and writable (this is used to synthesize indirect jumps).

Unlike most other CPUs, there is no distinction between "memory" and "register" space because the RAM serves the job of both memory and registers, and the RAM is usually just referred to as the register file or simply as the registers.

2.4.1.1 PIC Family Core Architectural

PIC can be divided into several family cores architectural. There are three main family cores. That is baseline core, mid-range core and high end core.

Baseline core devices is feature a 12-bit wide code memory, and a tiny two level deep call stack. They are represented by PIC10 series, as well as some PIC12and PIC16 devices. Baseline devices are available in 6-pin to 40-pin packages.

Mid-Range core devices is feature a 14-bit wide code memory, and an improved 8 level deep call stack. The instruction set differs very little from the baseline devices, but the increased op-code width allows more memory to be directly addressed. The mid-range core is available in the majority of devices labeled PIC12and PIC16.

High end core devices are 17 series never became popular and has been superseded by the PIC18architecture. It is not recommended for new designs, and may be in limited availability.

Improvements over earlier cores are 16-bit wide op-codes (allowing many new instructions), and a 16 level deep call stack. PIC17 devices were produced in packages from 40 to 68 pins.

2.4.1.2 PIC 16F877A

2.4.1.2.1 Introduction:

PIC16F877A is a small piece of semiconductor integrated circuits. The package type of these integrated circuits is DIP package. DIP stand for Dual Inline Package for semiconductor IC. This package is very easy to be soldered onto the strip board. However using a DIP socket is much easier so that this chip can be plugged and removed from the development board. PIC16F877A have many features which can be use in this project. Table 2.1 provides all the features available on this PIC16F877A. Besides all the features provide, this chip also selected based on several reasons:

i) It support analog to digital conversion.
ii) It size is small and equipped with sufficient output ports
iii) It portability and low current consumption

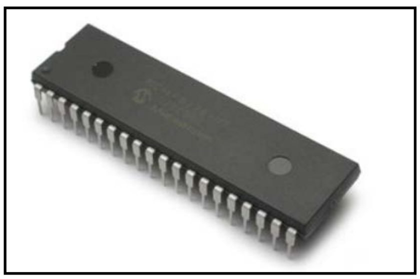


Figure 2.5: PIC 16F877A

Feature	**PIC16F877A**
Operating Frequency	DC – 20 MHz
Program Memory Type	Enhanced Flash
Program Memory Size (bytes)	14336
Data Memory (bytes)	368
EEPROM Data Memory (bytes)	256

Interrupts	15
I/O Ports	Ports A, B, C, D, E
Timers	3
Capture/Compare/PWM modules	2
Serial Communications	MSSP, USART
Parallel Communications	PSP
10-bit Analog-to-Digital Module	8 input channels
Instruction Set	35 Instructions
Resets (and Delays)	POR, BOR(PWRT, OST)

Table 2.1: 40 pin PIC16F877A

2.4.1.2.2 Advantages of PIC 16F877A

There are several advantages of PIC 16F877A if compare to other controller. This chip is easy to buy since it available in market and in demand for the market. .Besides, this chip is inexpensive compare with other controller. Because of the inexpensive value in market, this controller is suitable for low cost development tools

This PIC 16F877A have 33 I/O pins which provides user with more freedom and availability in their project. This controller also has RAM, ROM and peripheral on chip.

2.4.2 Pulse Width Modulator Control Circuit SG3525A

The SG3525A, SG3527A pulse width modulator control circuits offer improved performance and lower external parts count when implemented for controlling all types of switching power supplies. The on–chip +5.1 V reference is trimmed to ±1% and the error amplifier has an input common–mode voltage range that includes the reference voltage, thus eliminating the need for external divider resistors. A sync input to the oscillator enables multiple units to be slaved or a single unit to be synchronized to an external system clock. A wide range of dead time can be programmed by a single resistor connected between the CT and Discharge pins. Figure 2.6 shows the pin connections for this pulse width modulator with the functions of every pin.

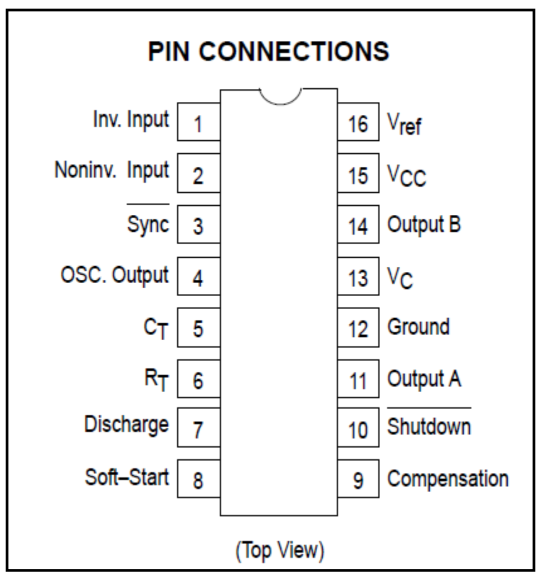


Figure 2.6: Pin Diagram of SG3525A

These devices also feature built–in soft–start circuitry, requiring only an external timing capacitor. A shutdown pin controls both the soft–start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft–start recycle with longer shutdown commands. The under voltage lockout inhibits the outputs and the changing of the soft–start capacitor when VCC is below nominal. The output stages are totem–pole design capable of sinking and sourcing in excess of 200 mA. The output stage of the SG3525A features NOR logic resulting in a low output for an off–state while the SG3527A utilized OR logic which gives a high output when off.

CHAPTER 3

METHODOLOGY

3.1 Overview

This chapter will explain about the methods that will be used to complete the project. Basically, the project will be divided into few parts and it will be executed stage by stage. After the title has been decided, the first thing to do is to have a clear understanding about the whole idea of the project.

Besides, literature review was done on various topics such as the basic knowledge about boost converter, PIC Microcontroller, pulse width modulator, power MOSFET and programming. Moreover, the operation of the technique, the advantages, as well as the details of the component was to be studied before the proceeding to the hardware implementation. The flow chart and block diagram provide in this chapter is method and approaches that need to be taken have been determined to make this project successful.

3.2 Flow Chart on Project Methodology

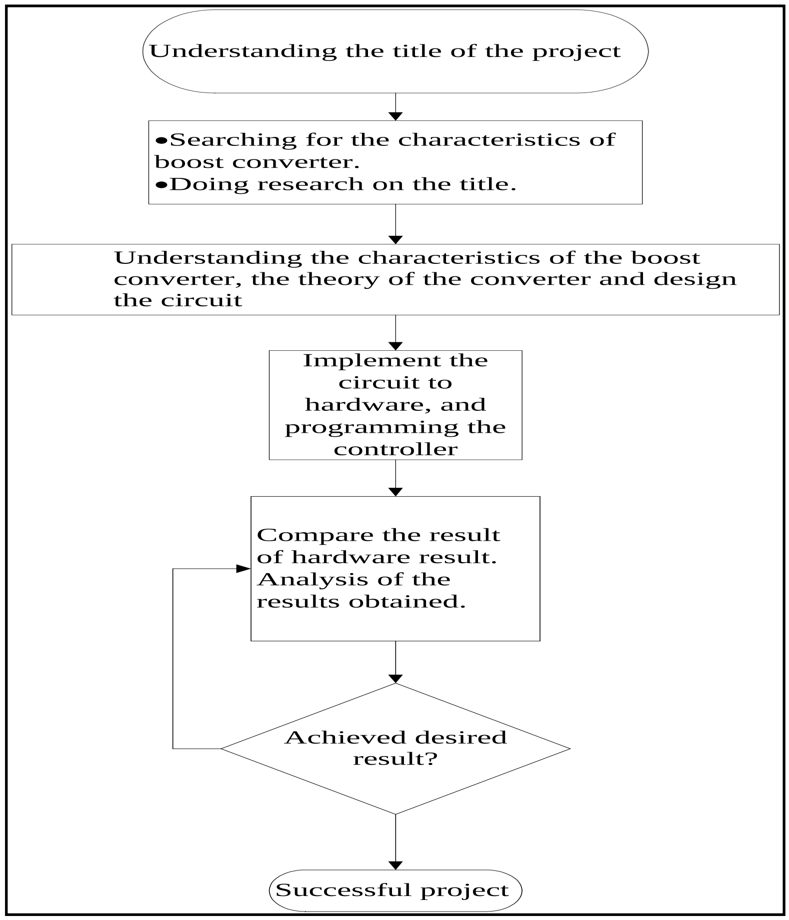


Figure 3.1: Flow Chart on Project Methodology

Figure 3.1 shows the flow chart of this project. It is necessary for every project to have a flow chart because it will be a guideline for the whole project and also the completion of the project. For this project, the first step is to understand the title of project. A better understanding will help in the project. Next step is doing research of this project. Research is an important task because a good research will help the progress of this project and determine the success of it. Once the research is done and information has obtained, then the project can start the next step. With the information and knowledge from the research, the design process can start. Once the designing already completed and satisfied, then the hardware can be build according to the result from the designing. The complete circuit must go through testing and data collected to do comparisons. If the result obtained is satisfied, then the project is successful.

3.3 18V to 1000V Boost Converter Diagram

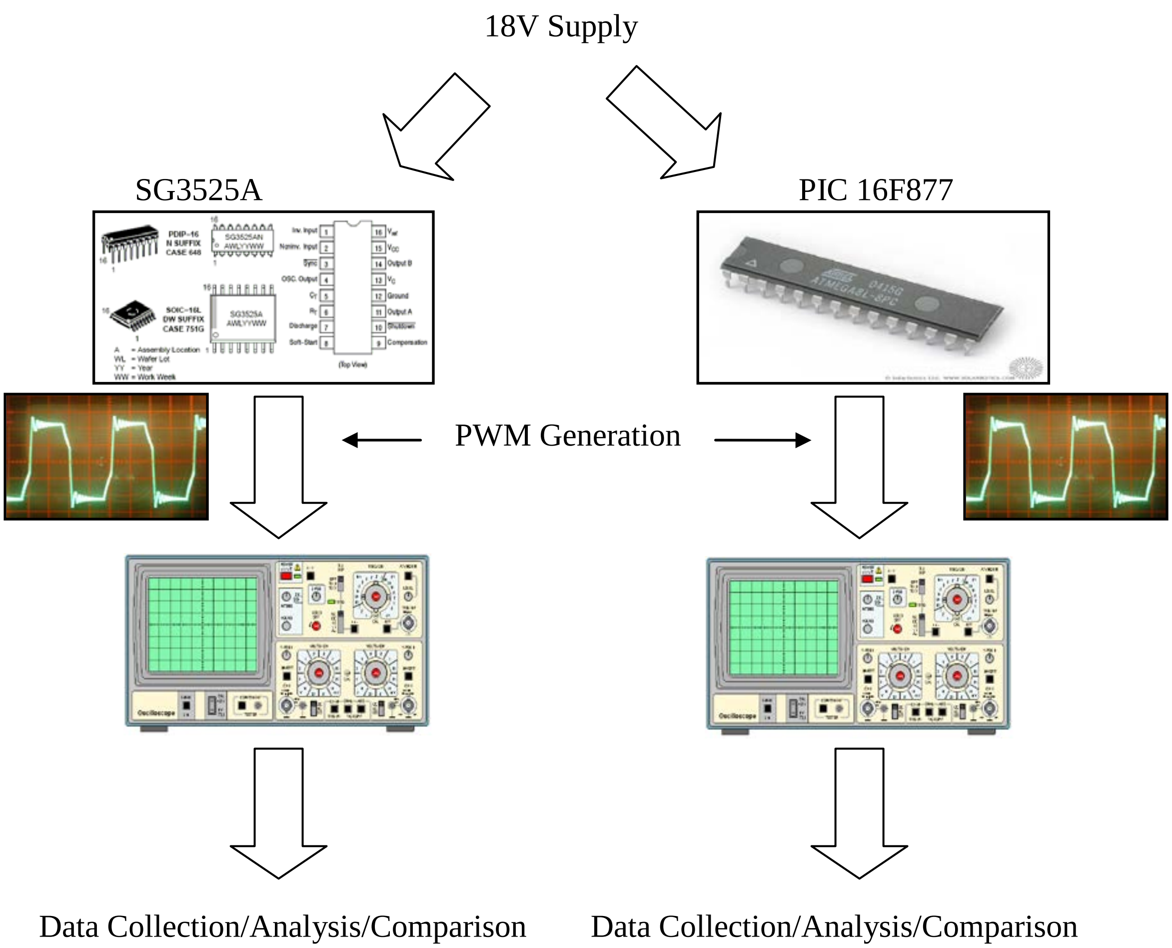


Figure 3.2: 18V to 1000V Boost Converter Diagram

In the previous page show the flow chart of this project. Meanwhile, Figure 3.2 shows the diagram of this project. This diagram helps during the designing, developing and testing the circuit. The diagram shows that this project is divided into two parts or method. Each method uses the same type of application that is using pulse to operate. When the circuit is complete, result will be obtained.

3.4 Circuit Development

3.4.1 PIC Circuit

A PIC microcontroller needs a few setting before it successfully operates. It need to have a master clear reset input, oscillator circuitry and the most important, the voltage supply to be functional. These basic pins are configured as shown in Figure 3.3 and Figure 3.2.

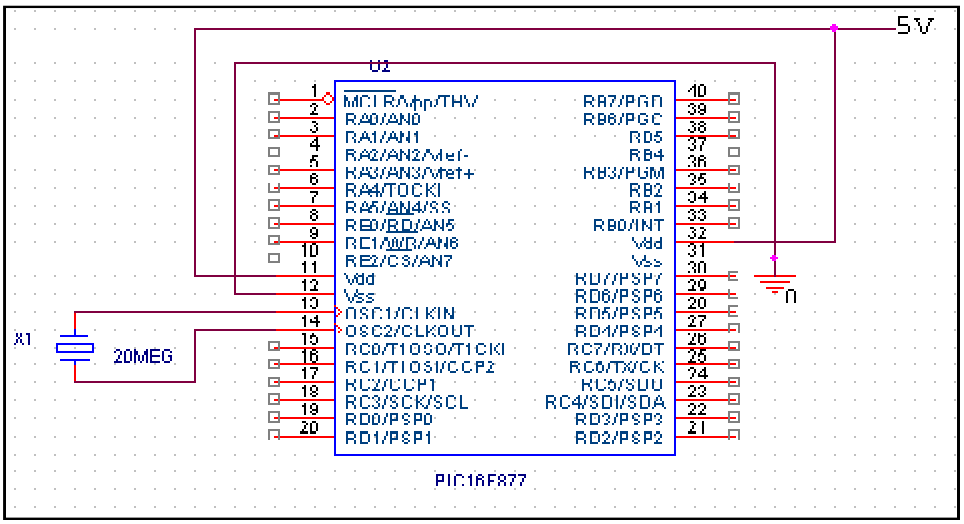


Figure 3.3: Oscillator circuit

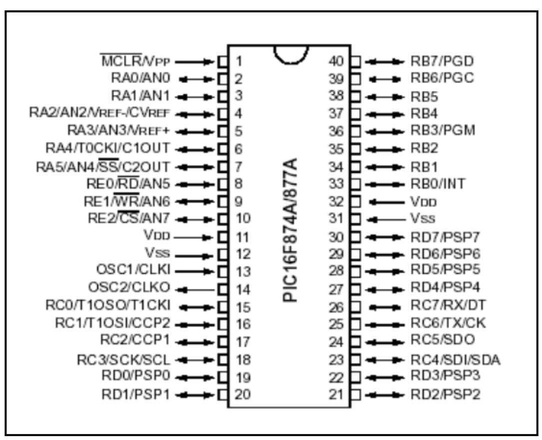


Figure 3.4: Basic pin for PIC16F877A

Basic pin for PIC 16F877A can be shown clearly in Figure 3.4. Master Clear Reset is located at pin 1, V_{dd} or +5V input supply should be connected to both pin 11 and pin 32, V_{ss} or Ground should be connected to both pin 12 and pin 31. While both OSC1 and OSC2 should be connected to pin 13 and pin 14 correctly.

3.4.2 Voltage Regulator 7805 IC

Most digital logic circuits and processors need a 5 volt power supply. LM 7805 voltage regulator IC is used to regulate supply voltage from power supply to 5-volt for microcontroller. From the front side of LM7805, we can see 3 legs or pin. The left pin must be connected to supply voltage in DC. The centre pin must be connected to ground. The right pin is the 5-volt output voltage. A heat sink is required for heat dissipation and can mount at the back of the IC. The voltage regulator IC is shown in Figure 3.5.

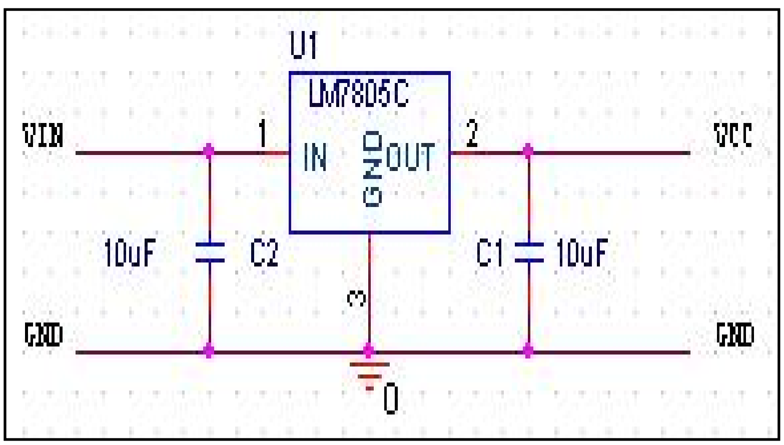
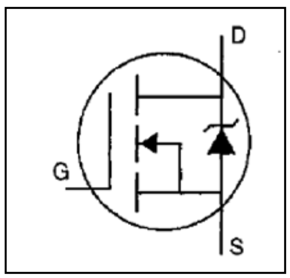


Figure 3.5: Voltage Regulator Circuit.

To provide the steady +5V supply to the PIC Microcontroller, a voltage regulator circuit has been built by using a few component. Two capacitor rated 10uF are used for this circuit and a LM7805 transistor is used to supply 5V for the PIC 16F877A.

3.4.3 Power MOSFET IRFBG30

This power MOSFET as shown in Figure 3.6 can be control by providing it with PWM pulse. This pulse can provide as an input through pin G. It is important to remember that the pulse width of this IRFBG30 is less than 300 microseconds and the duty cycle is less or equal with 2%. Meanwhile pin S is where we connect it to ground. Inside this power MOSFET also is a Zener diode which will avoid the current to flow back. This Zener diode also provides protection for this power MOSFET.



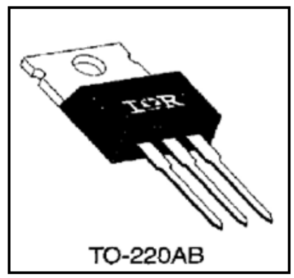


Figure 3.6: Power MOSFET IRGBG30

This power MOSFET has V_{DSS} that can reach up to 1000V with I_D of 3.1A. Meanwhile, the resistance of this power MOSFET is R_{DS} equal to 5.0Ω. This power MOSFET can fit in any applications since it has characteristic of simple drive requirement.

3.4.4 Metallized Polyster Film Capacitor

A capacitor or condenser is a passive electronic component consisting of a pair of conductors separated by a dielectric. Capacitor stores energy and produces a mechanical force between the plates. Besides, capacitors can also block the flow of direct current while allowing alternating current to pass, to filter out interference, to smooth the output of power supplies, and for many other purposes.

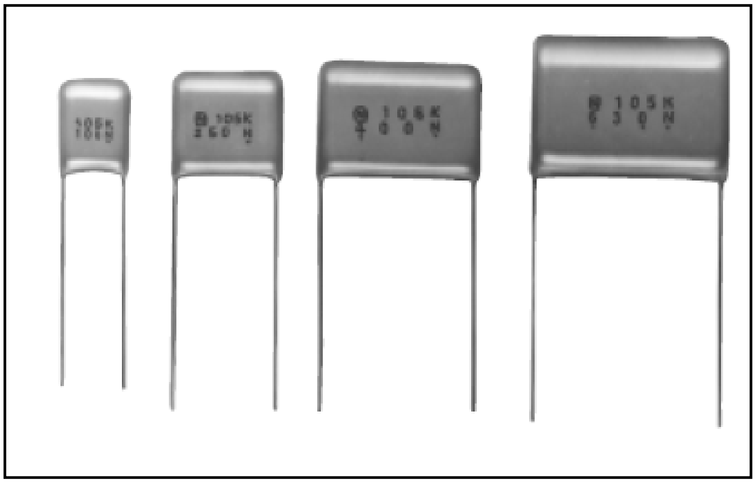


Figure 3.7: Metalized Polyester Film Capacitor

For this project, it is required to use this type of capacitor as shown in Figure 3.7. It has the rating of 1uF with rating voltage of 630V (dc). This capacitor is ECQE(F) type of capacitor. It has a non-inductive construction using metalized Polyster film with flame retardant epoxy resin coating. Other features are self healing property besides the excellent electrical characteristics.

3.4.5 IR2101

The IR2101(S) as shown in Figure 3.8 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

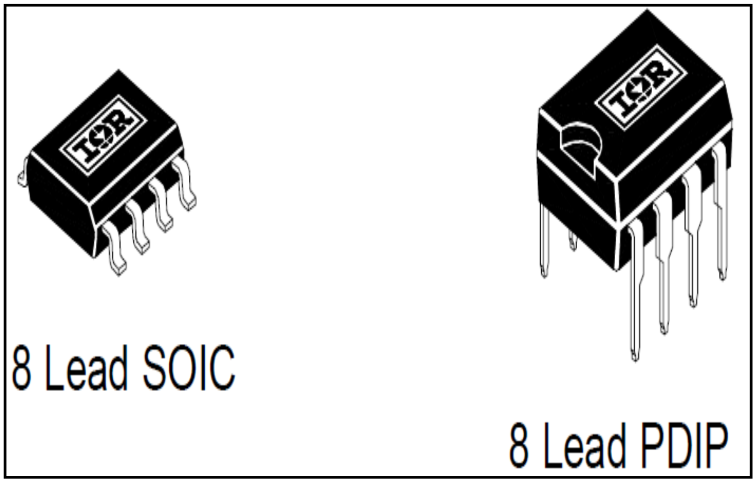


Figure 3.8: Different packaging type of IR2101

For this project, it is necessary to use this IC IR2101 because of the use power MOSFET IRFBG30 which has high switching frequency. A signal is supply through the pin H_{IN} of the IR2101 from the PIC 16F877A. From the IR2101, the pin H_O is then connected to 4N25 before the signal goes to IRFBG30.

3.4.6 4N25

4N25 is an opto-isolator output transistor. This type of opto-isolator is suitable for general purpose switching circuits. Besides, this opto-isolator also capable of handling applications that require interfacing and coupling systems of different potentials and impedances. It also can be use as an I/O interfacing devices. This opto-isolator also can be used as Solid State Relays application.

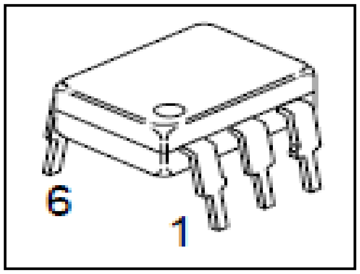


Figure 3.9: Standard Thru Hole type of 4N25

Since the project involve high voltage and low voltage, it is necessary to isolate or separate the two parts. 4N25 is used in the circuit to isolate the high voltage from the low voltage. Figure 3.9 show the diagram of the 4N25 which has been used for this project.

3.5 Programming Development

3.5.1 PWM Mode

In Pulse Width Modulation (PWM) mode is where we need to determine all the require pulse width, period, and duty cycle. Only then programming can be done. The CCPx pin produces up to a 10-bit resolution PWM output. Since the CCPx pin is multiplexed with the PORT data latch, the corresponding TRIS bit must be cleared to make the CCPx pin an output.

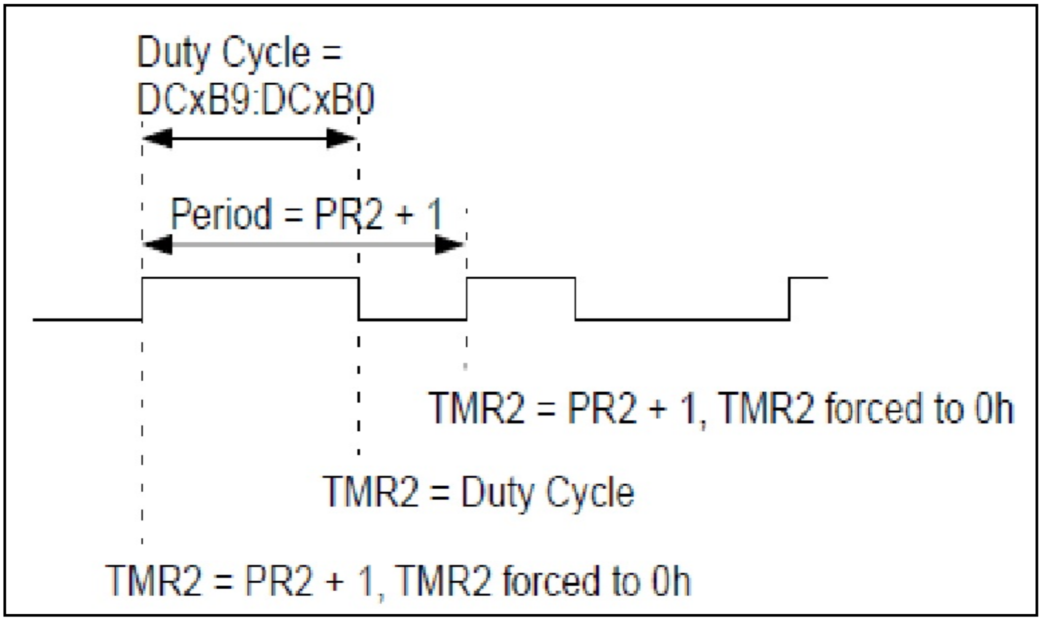


Figure 3.8: PWM Output

One of the requirements for this project is to generate a PWM from the PIC16F877A. This PWM will be connected to IRGBG30 as an input for it to generate enough pulse to produce 1000V. Figure 3.7 shows mathematical equation for the calculations of PWM which will be use in this project.

Before starting with the programming, the frequency of the period must be determined first since the IRFBG30 has its own requirement that it duty cycle of 2% and pulse width of 300us. After some calculations, it has been decide that the PWM frequency is 165 kHz.

Maximum resolution also needs to be determined. Using the equation given, the maximum resolution for this 165 kHz is 6.92 bits. If the PWM duty cycle value is longer than the PWM period, the CCPx pin will not be cleared. This allows a duty cycle of 100%. The minimum resolution (in time) of each bit of the PWM duty cycle depends on the pre-scalar of Timer2.

Once the programming is completed, the CCPx pin is then connected to the IRGBG30 to give the generate PWM as an input to operate the IRGBG30.

3.6 Software Development

3.6.1 C Compiler

C Compiler is program that requires in this project to write the program before burn it into PIC16F877A. C Compiler is based on C language which is a simple way to write a program.

For this project, the command or syntax, **SET_PWM1_DUTY ( ),** is widely use since the project require to generate PWM pulse from the PIC16F877A. This function is only available on devices with CCP/PWM hardware. The parameter value may be an 8 or 16 bit constant or variable.

3.6.2 ORCHAD 9.1 COMPLETE SUITE

ORCHAD 9.1 COMPLETE SUITE is software that can do stimulation and result can be obtained directly. Besides, this software also can be used to design the schematic of the circuit. This software has offer variety of software inside the database which can be used to complete this project.

For this project, this software has been used limited since some of the component for this project didn’t available inside the database of this software. But, in designing the schematic and the circuit drawing, this software has been used widely.

CHAPTER 4

RESULT AND DISCUSSION

4.1 Overview

This chapter will explain about the circuit of every PWM controller that been used in this project. Pictures are provided to explain more on both of circuit and also for better understanding.

This chapter will also explain on the experiments that had been conducted for this project. An experiment is conducted to find out the relationship between PWM and the output voltage for the boost converter. Then, data collection is done to observe the changing in the output voltage when we variable the period and the duty cycle from the PIC16F877A. Several pictures base on each circuit are provided to be use to explain more detail this project. Graph also been provided for a better understanding of this project.

4.2 Circuit Overview

This circuit overview will be divided into two parts since we have 2 different circuits. For the first part we will explain the circuit of the SG3525AN and the second part we will explain on the circuit of PIC6F877A. Pictures been provided for the clear viewing of this project.

4.2.1 Circuit Overview of SG3525AN

For the SG3525AN, a circuit have been successfully been design and solder similar to a PCB board where we solder all the connection and didn't require any wiring. Figure 4.2.1 (a) and Figure 4.2.1 (b) show a complete circuit of the boost converter using SG3525AN after the completion of designing.

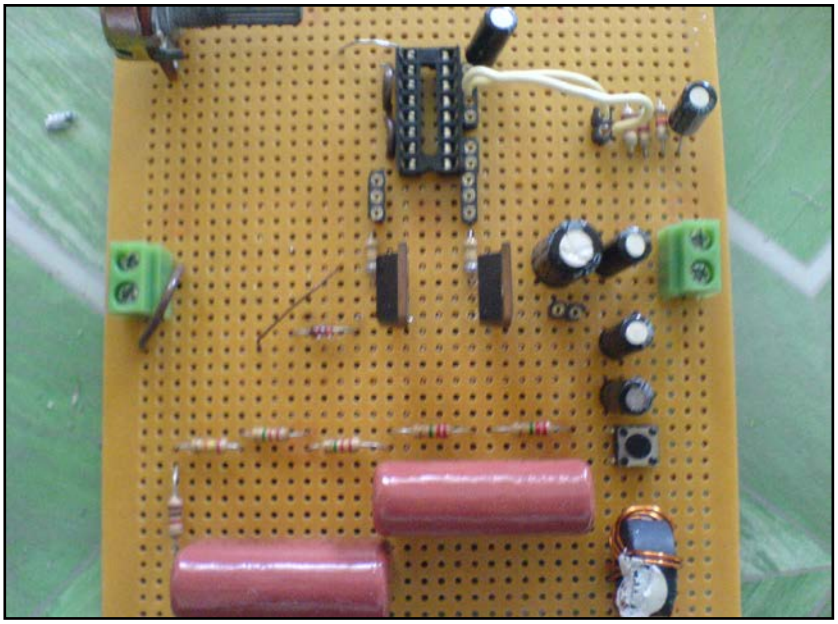


Figure 4.2.1 (a): Top view of the circuit

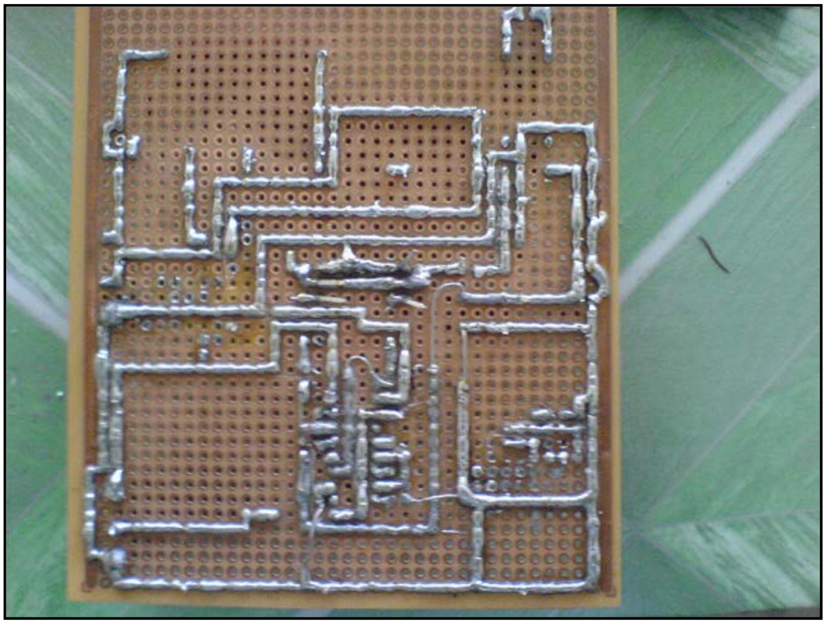


Figure 4.2.1 (b): Bottom view of the circuit

4.2.2 Circuit Overview of PIC6F877A

For the PIC6F877A, a circuit have been successfully been design and solder similar to the previous circuit where the use of wire are able to be reduce. But for the PIC6F877A, the pin connection are connected using the wrapping wire which is suitable for the circuit since it is operate at low voltage and the wrapping wire can stand the it. Figure 4.2.2 (a) and Figure 4.2.2 (b) show a complete circuit of the boost converter using the PIC6F877A after the completion of designing. Meanwhile, Figure 4.2.2 (c) and Figure 4.2.2 (d) show the circuit of PIC16F877.

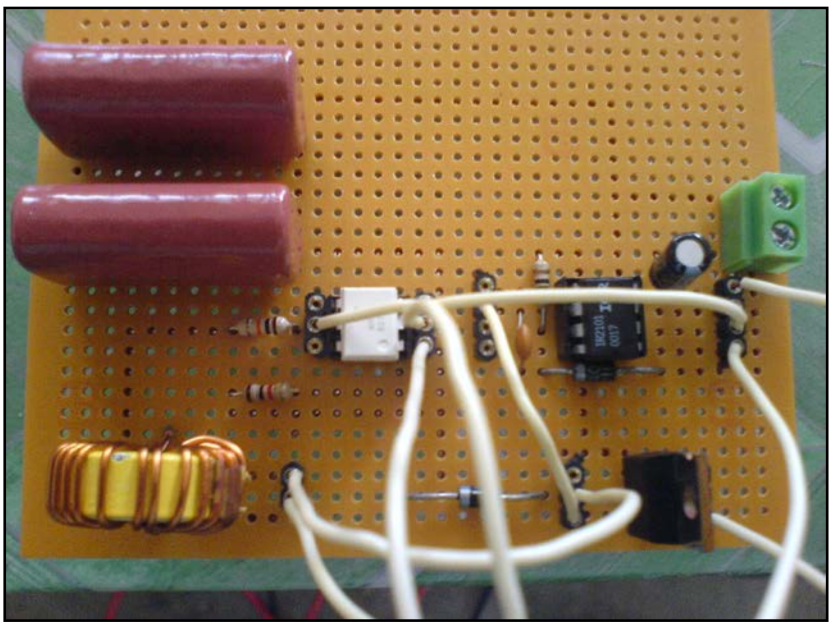


Figure 4.2.2 (a): Top view of the circuit

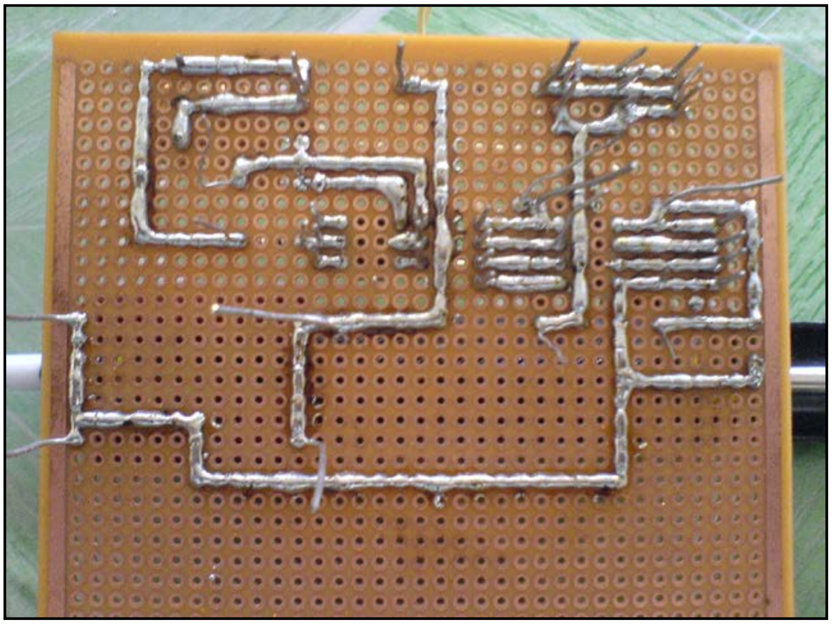


Figure 4.2.2 (b): Bottom view of the circuit

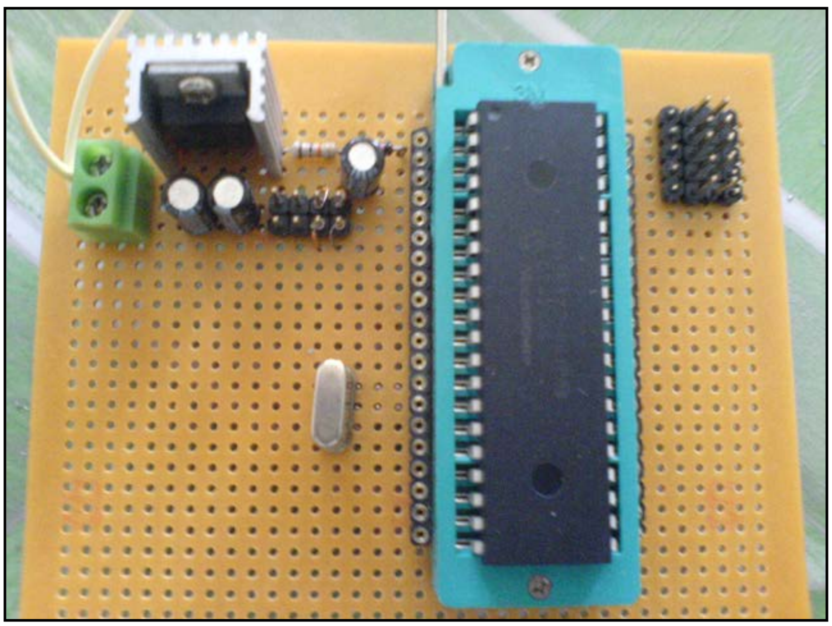


Figure 4.2.2 (c): Top view of the PIC16F877A circuit

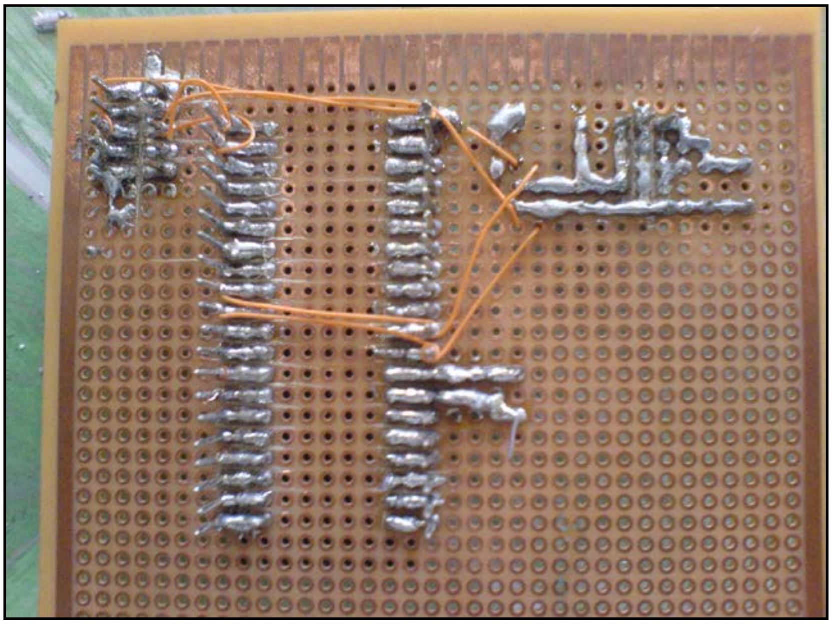


Figure 4.2.2 (c): Bottom view of the PIC16F877A circuit

4.3 Test Result

This test result will be divided into two parts since we have 2 different circuits. For the first part we will explain the circuit of the SG3525AN and the second part we will explain on the circuit of PIC6F877A.

4.3.1 Test Result of SG3525AN

For the testing, the circuit is supply with 18V supply from the power supply. The current value also set to 0.01A which is set for safety purpose and this current value will be manipulate and adjusted by the power supply itself depending on the need of the circuit. Figure 4.3.1 (a) shows the settings of the initial value for this testing.

Figure 4.3.1 (a): Power supply settings

For the test result, the PWM produce by the SG3525AN obtain from pin 11 and pin 14 which are the output for this SG3525AN. Figure 4.3.1 (b) and Figure 4.3.1 (c) show the output produce by both of the output pin.

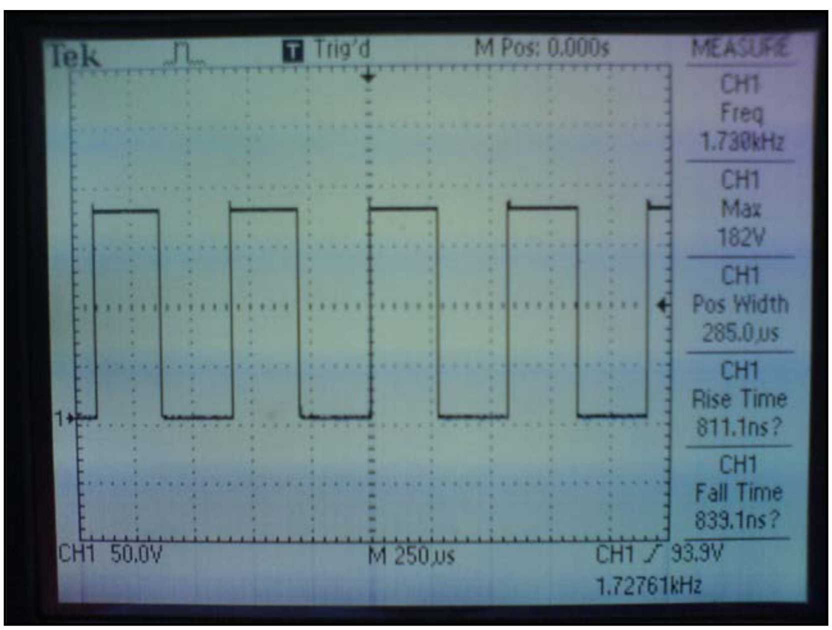


Figure 4.3.1 (b): PWM from pin 11

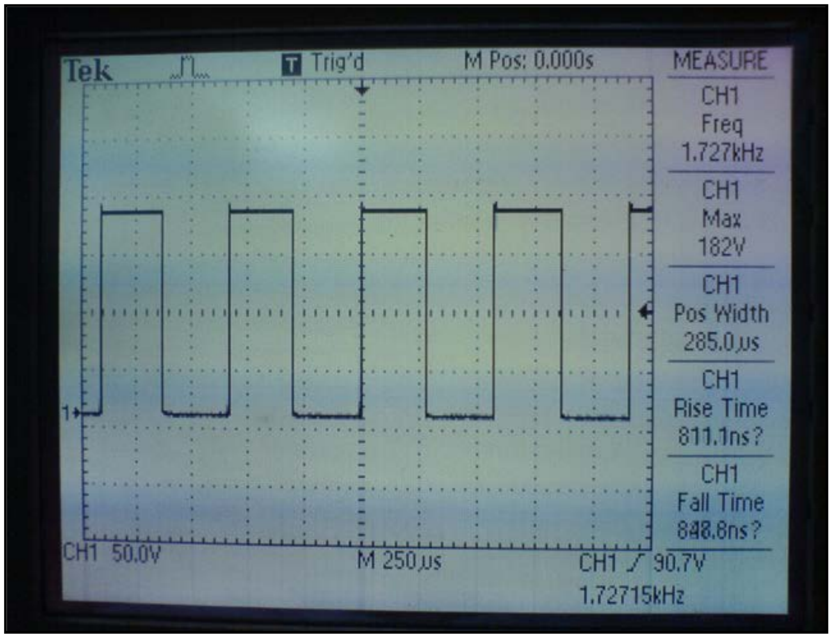


Figure 4.3.1 (c): PWM from pin 14

From both figure, it is clearly show that the PWM from the output pin are similarly the same which will be connected to the Power MOSFET. For both output pins, the frequency produce is 1.727 kHz, which has the same pulse width of 285.0 microseconds.

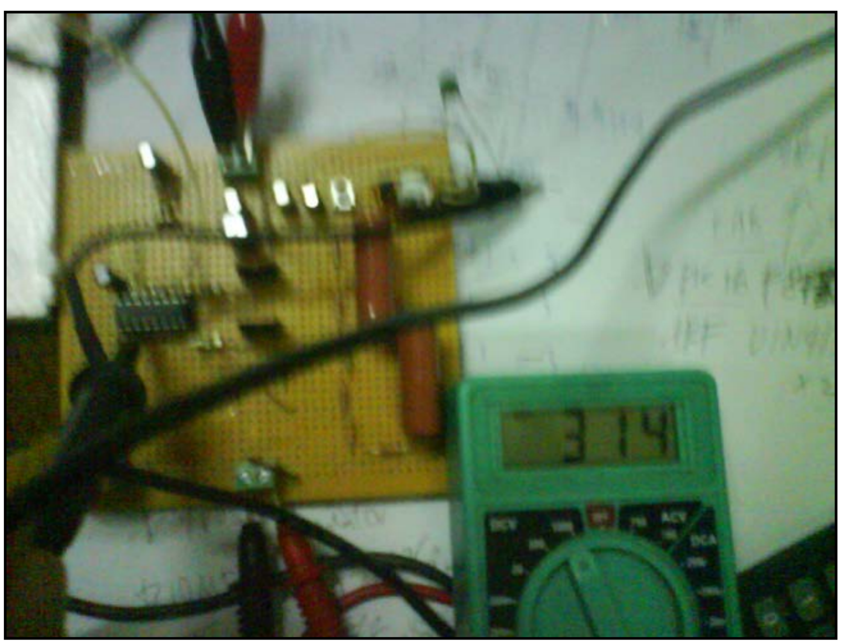


Figure 4.3.1 (d): Output Voltage

For the output voltage, Figure 4.3.1 (d) shows a voltage rated of 314V is produce. This circuit can't be manipulated because the SG3525AN itself will produce the PWM that could generate a pulse to boost the input. Data can't be shown since every variable are control by the SG3525AN.

Although the output didn't reach 1000V, the circuit able to boost the input of 18V to 314V which is 18 times larger than the input. The objective to boost the input achieved.

4.3.2 Test Result of PIC16F877A

Similarly to the previous setting, circuit is supply with 18V supply from the power supply. But for the current value set to 0.31A since some additional application are added to the circuit. Figure 4.3.2 (a) shows the PWM pulse produce by the PIC16F877A which obtain from either pin 16 or pin 17.

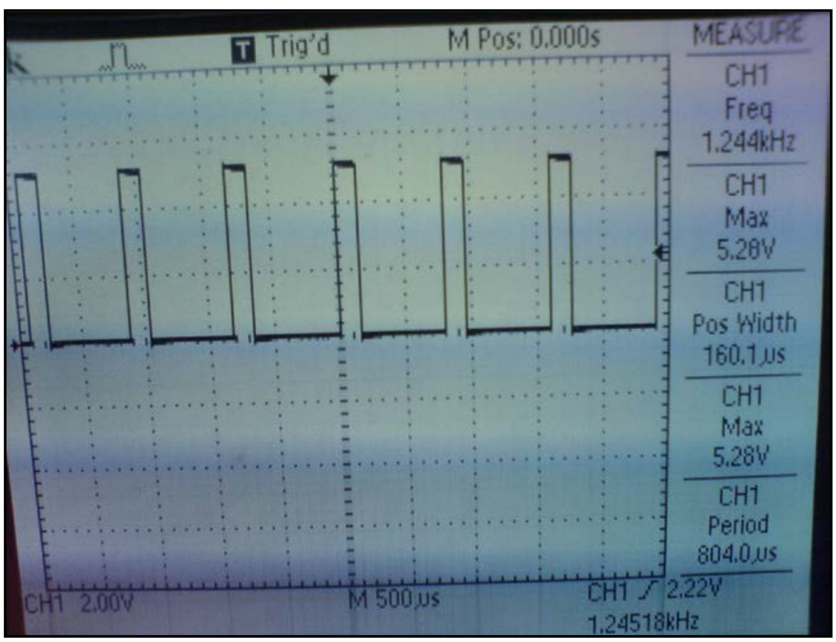


Figure 4.3.2 (a): PWM pulse from PIC16F877A

For the analysis, 3 experiments have been done where the value of period is manipulated and the duty cycle also manipulates to determine which value can produce the target output voltage.

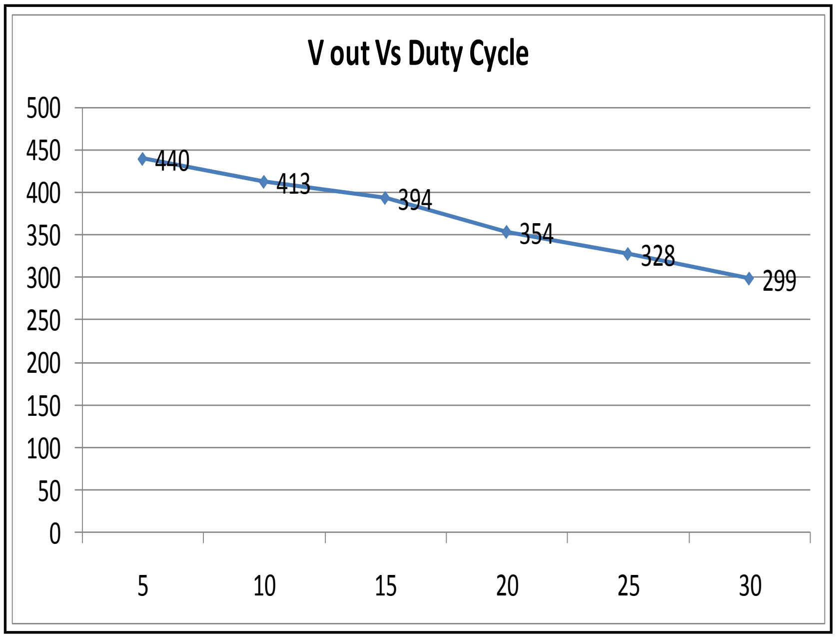
For the first experiment, the period is set to 255 seconds and the duty cycle is varied to different value. Table 4.3.2 (a) shows the result obtain from the experiment.

Period	**Duty Cycle**	**V_{In}**	**V_{Out}**	**I_{In}**	**I_D**
255	5	18.3	440	0.31	0.07
255	10	18.3	413	0.31	0.11
255	15	18.3	394	0.31	0.15
255	20	18.3	354	0.31	0.19
255	25	18.3	328	0.31	0.21
255	30	18.3	299	0.31	0.23

Table 4.3.2 (a): Result of first experiment

The maximum voltage output obtained from this circuit is 440V when period is set to 255seconds and the duty cycle is 5 with V_{In} of 18V and I_{In} of 0.31A. The I_D is 0.07A. Meanwhile, for the minimum voltage output obtained from the experiment is 299V with the same period but different duty cycle (30). The supply voltage and current is the same with the maximum voltage output but for the I_D is 0.23A which is an increase from the initial.

From the result obtained, a graph of V_{out} versus Duty Cycle is plotted. Graph 4.3.2 (a) is plotted using the results obtained from Table 4.3.2 (a).



Graph 4.3.2 (a): Graph for experiment 1

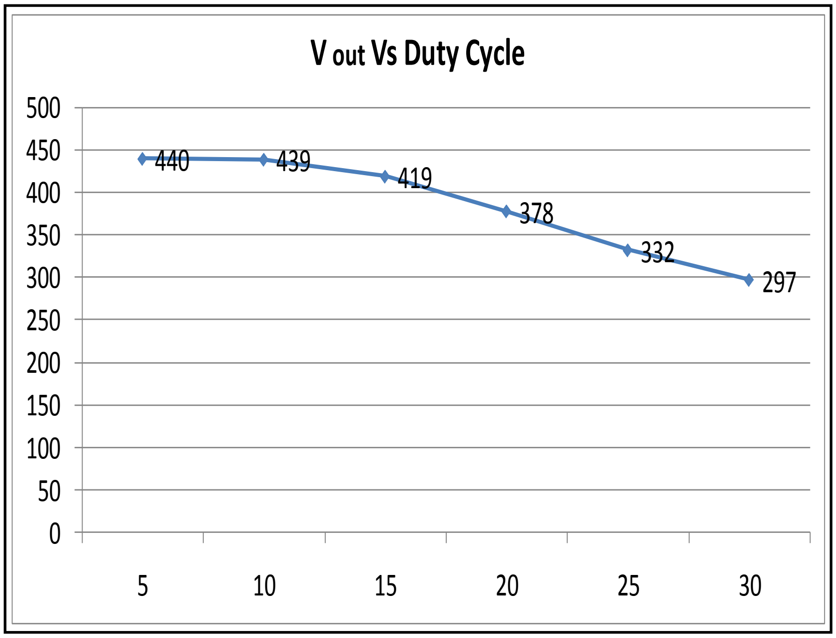
For the second experiment, the period is set to 500 seconds and the duty cycle is varied to different value. Others parameters are fix to the same value as the initial. Table 4.3.2 (b) shows the result obtain from the experiment.

Period	Duty Cycle	V_{In}	V_{Out}	I_{In}	I_D
500	5	18.3	440	0.31	0.07
500	10	18.3	439	0.31	0.12
500	15	18.3	419	0.31	0.17
500	20	18.3	378	0.31	0.19
500	25	18.3	332	0.31	0.22
500	30	18.3	297	0.31	0.24

Table 4.3.2 (b): Result of second experiment

Similarly to the first experiment, the maximum voltage output obtained from this circuit is 440V when period is set to 500 seconds and the duty cycle is 5 with V_{In} of 18V and I_{In} of 0.31A. The I_D is 0.07A. Meanwhile, for the minimum voltage output obtained from the experiment is slightly dropping compare with first experiment that is 297V with the period of 500 seconds but different duty cycle (30). The supply voltage and current is the same with the maximum voltage output but for the I_D, there is increase of it that is from 0.07A to 0.24A.

From the result obtained, a graph of V_{out} versus Duty Cycle is plotted. Graph 4.3.2 (b) is plotted using the results obtained from Table 4.3.2 (b).



Graph 4.3.2 (b): Graph for experiment 2

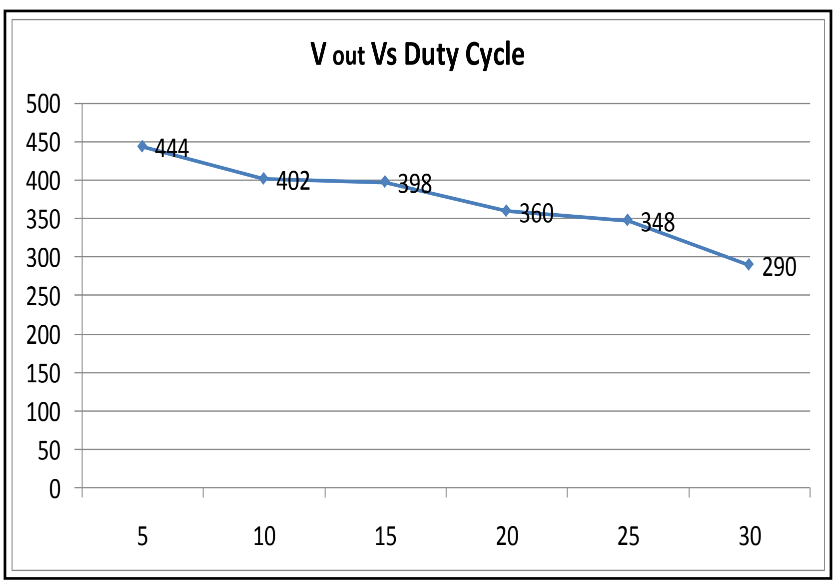
For the third experiment, the period is set to 1000 seconds and the duty cycle is varied to different value. Similarly to the other experiment, the value of V_{in} and I_{in} are the same Table 4.3.2 (c) shows the results obtain from the experiment.

Period	Duty Cycle	V_{In}	V_{Out}	I_{In}	I_D
1000	5	18.3	444	0.31	0.12
1000	10	18.3	402	0.31	0.20
1000	15	18.3	398	0.31	0.24
1000	20	18.3	360	0.31	0.06
1000	25	18.3	348	0.31	0.17
1000	30	18.3	290	0.31	0.25

Table 4.3.2 (c): Result of third experiment

For the third experiment, the maximum voltage output obtained from this circuit is 444V when period is set to 1000 seconds and the duty cycle is 5 with V_{In} of 18V and I_{In} of 0.31A. The I_D is 0.12A which is an increase of value compare to the other experiment. Meanwhile, for the minimum voltage output is 290V with the period of 500 seconds but different duty cycle (30). The supply voltage and current is the same with the maximum voltage output but for the I_D, there is increase to 0.25A.

From the result obtained, a graph of V_{out} versus Duty Cycle is plotted. Graph 4.3.2 (c) is plotted using the results obtained from Table 4.3.2 (c).



Graph 4.3.2 (b): Graph for experiment 3

From the 3 experiment conducted, it is clearly shown that when the duty cycle is increase, the I_D also increase because the signal from the PIC16F877A has increase and triggered the IRGBG30 to produce the higher voltage output. Hence, the inductor “pump” the current from the supply which leads to the increase value of the I_D.

But the voltage value is remain below the target because of the inductor use in this experiment can’t provide an amount which can boost the 18V to 1000V voltage. The inductor can’t store the amount of current which require by the IRGBG30 to boost the input voltage. The increase value of I_D prove that this have affected the boost converter which shows the amount of current needed by the IRGBG30.

Besides, the diode for this experiment also can’t meet the demand that require for the switching frequency of the IRFBG30, in which has affect the output voltage of this boost converter. When the diode already reaching it frequency limit, it will stop the current from flowing through it or reverse the current back.

Other affect such as losses during the current transfer may affect the circuit too. Besides losses during the transfer, the heat dissipation may also affect this project since energy did convert into heat.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

The goal of this project is to design a switching power supply which is able to produce the DC output voltage from 18V to 1000V which operate using the PWM mode only. Due to errors and problems, the 1000V output can't be obtained. But this project shows that using PWM applications, the output voltage can be boost higher than the input voltage. By varying the duty cycle of the PWM, the output voltage can be manipulated depending on the demands and requirement.

The Power MOSFET is similar to the transformer where both can boost the input voltage to the desired output. By only giving the signal that require by the Power MOSFET, this devices can boost the input voltage to the desired output depending on the signal provide by user. This can replace the use of large and conventional transformer.

In conclusion, the switching power supply circuit has been developed in order to produce the output voltage up to 100VDC. The operation of power supply circuits consist of Power MOSFET, inductor, high frequency diode, switcher, PWM controller, and microcontroller. As the result, by adjusting the PWM controller, the PWM pulse produce will give the variable output voltage for the boost converter to boost the input to desired output.

5.2 Recommendation

For this type of converter, it is necessary to use a high current type of diode because once the diode already reaching the limit, it won’t conduct or allow the current flow through.

It is also necessary to use an inductor which can store a high current and energy since the inductor acts as pump for this boost converter.

A better isolation of high voltage side and low voltage side require for this type of project. This is because the high voltage side could affect the other. Besides, this will also help to protect the circuit**.**

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APPENDIX A

MICROCHIP

PIC16F87X

28/40-Pin 8-Bit CMOS FLASH Microcontrollers

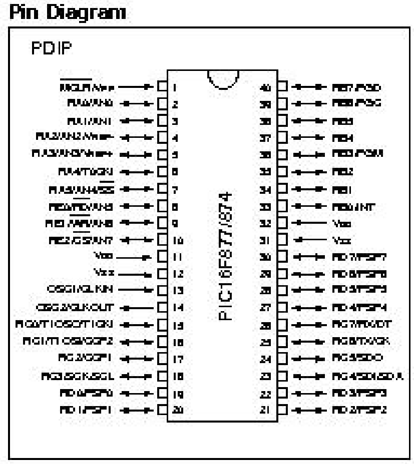
Devices Included in this Data Sheet:

- PIC16F873
- PIC16F874
- PIC16F876
- PIC16F877

Microcontroller Core Features:

- High performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- Up to 8K x 14 words of FLASH Program Memory,
  Up to 368 x 8 bytes of Data Memory (RAM)
  Up to 256 x 8 bytes of EEPROM Data Memory
- Pinout compatible to the PIC16C73B/74B/76/77
- Interrupt capability (up to 14 sources)
- Eight level deep hardware stack
- Direct, indirect and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low power, high speed CMOS FLASH/EEPROM technology
- Fully static design
- In-Circuit Serial Programming™ (ICSP) via two pins
- Single 5V In-Circuit Serial Programming capability
- In-Circuit Debugging via two pins
- Processor read/write access to program memory
- Wide operating voltage range: 2.0V to 5.5V
- High Sink/Source Current: 25 mA
- Commercial, Industrial and Extended temperature ranges
- Low-power consumption:
  - < 0.6 mA typical @ 3V, 4 MHz
  - 20 μA typical @ 3V, 32 kHz
  - < 1 μA typical standby current

Pin Diagram



Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during SLEEP via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
  - Capture is 16-bit, max. resolution is 12.5 ns
  - Compare is 16-bit, max. resolution is 200 ns
  - PWM max. resolution is 10-bit
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI™ (Master mode) and I²C™ (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
- Parallel Slave Port (PSP) 8-bits wide, with external RD, WR and CS controls (40/44-pin only)
- Brown-out detection circuitry for Brown-out Reset (BOR)

Key Features PICmicro™ Mid-Range Reference Manual (DS33023)	PIC16F873	PIC16F874	PIC16F876	PIC16F877
Operating Frequency	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz
RESETS (and Delays)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)
FLASH Program Memory (14-bit words)	4K	4K	8K	8K
Data Memory (bytes)	192	192	368	368
EEPROM Data Memory	128	128	256	256
Interrupts	13	14	13	14
I/O Ports	Ports A,B,C	Ports A,B,C,D,E	Ports A,B,C	Ports A,B,C,D,E
Timers	3	3	3	3
Capture/Compare/PWM Modules	2	2	2	2
Serial Communications	MSSP, USART	MSSP, USART	MSSP, USART	MSSP, USART
Parallel Communications	—	PSP	—	PSP
10-bit Analog-to-Digital Module	5 input channels	8 input channels	5 input channels	8 input channels
Instruction Set	35 instructions	35 instructions	35 instructions	35 instructions

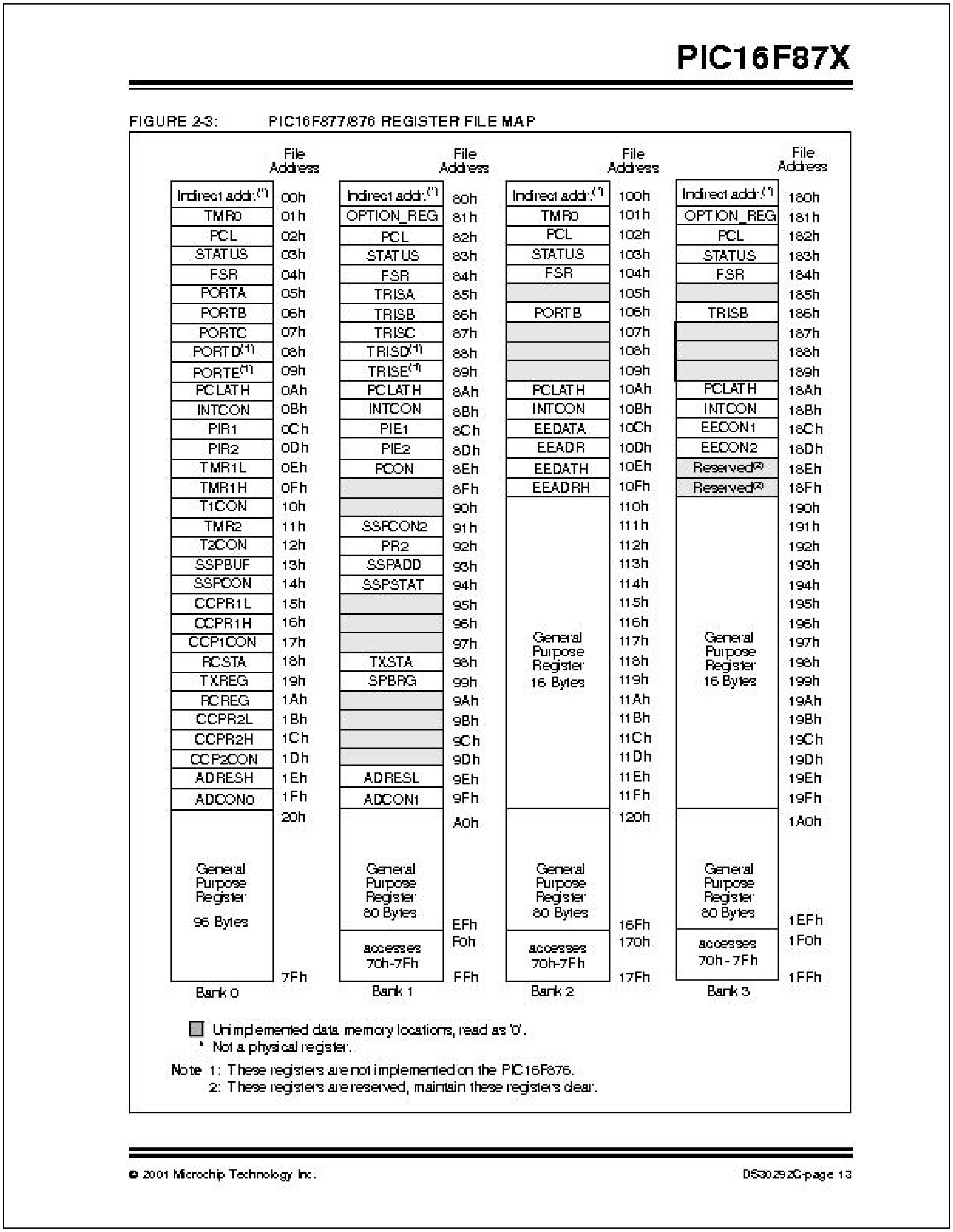


FIGURE 2-3: PIC16F877/876 REGISTER FILE MAP

Bank 0	File Address	Bank 1	File Address	Bank 2	File Address	Bank 3	File Address
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h		107h		187h
PORTD(1)	08h	TRISD(1)	88h		108h		188h
PORTE(1)	09h	TRISE(1)	89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATA	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved(2)	18Eh
TMR1H	0Fh		8Fh	EEADRH	10Fh	Reserved(2)	18Fh
T1CON	10h		90h	General Purpose Register 16 Bytes	110h	General Purpose Register 16 Bytes	190h
TMR2	11h	SSPCON2	91h		111h		191h
T2CON	12h	PR2	92h		112h		192h
SSPBUF	13h	SSPADD	93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1L	15h		95h		115h		195h
CCPR1H	16h		96h		116h		196h
CCP1CON	17h		97h		117h		197h
RCSTA	18h	TXSTA	98h		118h		198h
TXREG	19h	SPBRG	99h		119h		199h
RCREG	1Ah		9Ah		11Ah		19Ah
CCPR2L	1Bh		9Bh		11Bh		19Bh
CCPR2H	1Ch		9Ch		11Ch		19Ch
CCP2CON	1Dh		9Dh		11Dh		19Dh
ADRESH	1Eh	ADRESL	9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
General Purpose Register 96 Bytes	20h	General Purpose Register 80 Bytes	A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h
			EFh		16Fh		1EFh
		accesses 70h-7Fh	F0h	accesses 70h-7Fh	170h	accesses 70h-7Fh	1F0h
	7Fh		FFh		17Fh		1FFh
Bank 0		Bank 1		Bank 2		Bank 3	

Unimplemented data memory locations, read as '0'.
* Not a physical register.

Note 1: These registers are not implemented on the PIC16F876.
2: These registers are reserved, maintain these registers clear.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page:
Bank 1											
80h[3]	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	27
81h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	19
82h[3]	PCL	Program Counter (PC) Least Significant Byte								0000 0000	26
83h[3]	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	18
84h[3]	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	27
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111	29
86h	TRISB	PORTB Data Direction Register								1111 1111	31
87h	TRISC	PORTC Data Direction Register								1111 1111	33
88h[4]	TRISD	PORTD Data Direction Register								1111 1111	35
89h[4]	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction Bits			0000 -111	37
8Ah[1,3]	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000	26
8Bh[3]	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	20
8Ch	PIE1	PSPIE[2]	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	21
8Dh	PIE2	—	(5)	—	EEIE	BCLIE	—	—	CCP2IE	-r-0 0--0	23
8Eh	PCON	—	—	—	—	—	—	$\overline{POR}$	$\overline{BOR}$	---- --qq	25
8Fh	—	Unimplemented								—	—
90h	—	Unimplemented								—	—
91h	SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	68
92h	PR2	Timer2 Period Register								1111 1111	55
93h	SSPADD	Synchronous Serial Port (I^2C mode) Address Register								0000 0000	73, 74
94h	SSPSTAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000 0000	66
95h	—	Unimplemented								—	—
96h	—	Unimplemented								—	—
97h	—	Unimplemented								—	—
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	95
99h	SPBRG	Baud Rate Generator Register								0000 0000	97
9Ah	—	Unimplemented								—	—
9Bh	—	Unimplemented								—	—
9Ch	—	Unimplemented								—	—
9Dh	—	Unimplemented								—	—
9Eh	ADRESL	A/D Result Register Low Byte								xxxx xxxx	116
9Fh	ADCON1	ADFM	—	—	—	PCFG3	PCFG2	PCFG1	PCFG0	0--- 0000	112

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.
2: Bits PSPIE and PSPIF are reserved on PIC16F873/876 devices; always maintain these bits clear.
3: These registers can be addressed from any bank.
4: PORTD, PORTE, TRISD, and TRISE are not physically implemented on PIC16F873/876 devices; read as '0'.
5: PIR2<6> and PIE2<6> are reserved on these devices; always maintain these bits clear.

6.1 Timer1 Operation in Timer Mode

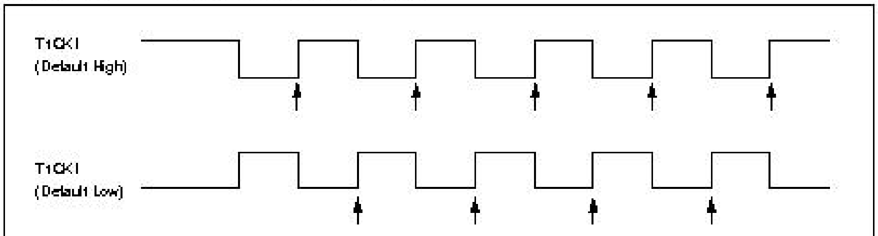
Timer mode is selected by clearing the TMR1CS (T1CON<1>) bit. In this mode, the input clock to the timer is Fosc/4. The synchronize control bit $\overline{\text{T1SYNC}}$ (T1CON<2>) has no effect, since the internal clock is always in sync.

6.2 Timer1 Counter Operation

Timer1 may operate in either a Synchronous, or an Asynchronous mode, depending on the setting of the TMR1CS bit.

When Timer1 is being incremented via an external source, increments occur on a rising edge. After Timer1 is enabled in Counter mode, the module must first have a falling edge before the counter begins to increment.

FIGURE 6-1: TIMER1 INCREMENTING EDGE



Note: Arrows indicate counter increments.

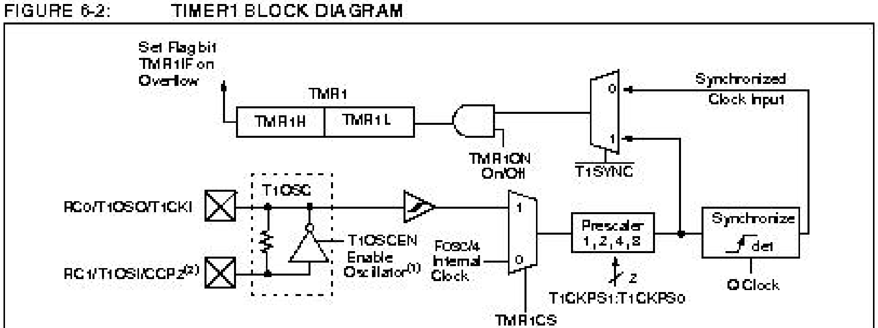
6.3 Timer1 Operation in Synchronized Counter Mode

Counter mode is selected by setting bit TMR1CS. In this mode, the timer increments on every rising edge of clock input on pin RC1/T1OSI/CCP2, when bit T1OSCEN is set, or on pin RC0/T1OSO/T1CKI, when bit T1OSCEN is cleared.

If $\overline{\text{T1SYNC}}$ is cleared, then the external clock input is synchronized with internal phase clocks. The synchronization is done after the prescaler stage. The prescaler stage is an asynchronous ripple-counter.

In this configuration, during SLEEP mode, Timer1 will not increment even if the external clock is present, since the synchronization circuit is shut-off. The prescaler, however, will continue to increment.

FIGURE 6-2: TIMER1 BLOCK DIAGRAM



Note 1: When the T1OSCEN bit is cleared, the inverter is turned off. This eliminates power drain.

8.3 PWM Mode (PWM)

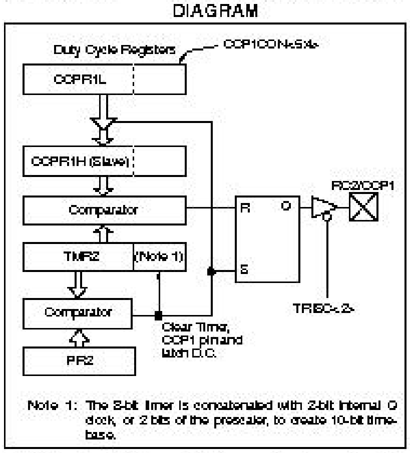
In Pulse Width Modulation mode, the CCPx pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

Note:	Clearing the CCP1CON register will force the CCP1 PWM output latch to the default low level. This is not the PORTC I/O data latch.

Figure 8-3 shows a simplified block diagram of the CCP module in PWM mode.

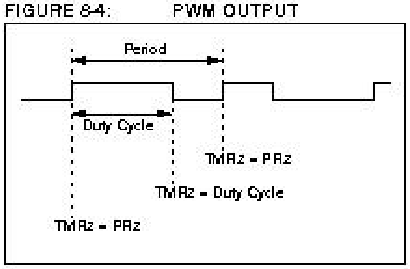
For a step-by-step procedure on how to set up the CCP module for PWM operation, see Section 8.3.3.

FIGURE 8-3: SIMPLIFIED PWM BLOCK DIAGRAM



A PWM output (Figure 8-4) has a time-base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 8-4: PWM OUTPUT



8.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

$$\text{PWM period} = [(PR2) + 1] \cdot 4 \cdot T_{OSC} \cdot (\text{TMR2 prescale value})$$

PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note:	The Timer2 postscaler (see Section 7.1) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

8.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

$$\text{PWM duty cycle} = (CCPR1L:CCP1CON<5:4>) \cdot T_{OSC} \cdot (\text{TMR2 prescale value})$$

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitch-free PWM operation.

When the CCPR1H and 2-bit latch match TMR2, concatenated with an internal 2-bit Q clock, or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

The maximum PWM resolution (bits) for a given PWM frequency is given by the formula:

$$\text{Resolution} = \frac{\log\left(\frac{F_{OSC}}{F_{PWM}}\right)}{\log(2)} \text{ bits}$$

Note:	If the PWM duty cycle value is longer than the PWM period, the CCP1 pin will not be cleared.

8.3.3 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
3. Make the CCP1 pin an output by clearing the TRISC<2> bit.
4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP1 module for PWM operation.

TABLE 8-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12kHz	156.3 kHz	208.3 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFFh	0xFFh	0xFFh	0x3Fh	0x1Fh	0x17h
Maximum Resolution (bits)	10	10	10	8	7	5.5

TABLE 8-4: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, AND TIMER1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh,8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF[1]	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	—	—	—	—	—	—	—	CCP2IF	---- ---0	---- ---0
8Ch	PIE1	PSPIE[1]	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	—	—	—	—	—	—	—	CCP2IE	---- ---0	---- ---0
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	--00 0000	--uu uuuu
15h	CCPR1L	Capture/Compare/PWM Register1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM Register1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
1Bh	CCPR2L	Capture/Compare/PWM Register2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Compare/PWM Register2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by Capture and Timer1.
Note 1: The PSP is not implemented on the PIC16F873/876; always maintain these bits clear.

TABLE 8-5: REGISTERS ASSOCIATED WITH PWM AND TIMER2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh,8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF[1]	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	—	—	—	—	—	—	—	CCP2IF	---- ---0	---- ---0
8Ch	PIE1	PSPIE[1]	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	—	—	—	—	—	—	—	CCP2IE	---- ---0	---- ---0
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
11h	TMR2	Timer2 Module's Register								0000 0000	0000 0000
92h	PR2	Timer2 Module's Period Register								1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/Compare/PWM Register1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM Register1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
1Bh	CCPR2L	Capture/Compare/PWM Register2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Compare/PWM Register2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PWM and Timer2.

Note 1: Bits PSPIE and PSPIF are reserved on the PIC16F873/876; always maintain these bits clear.

8.0 CAPTURE/COMPARE/PWM MODULES

Each Capture/Compare/PWM (CCP) module contains a 16-bit register which can operate as a:

- 16-bit Capture register
- 16-bit Compare register
- PWM Master/Slave Duty Cycle register

Both the CCP1 and CCP2 modules are identical in operation, with the exception being the operation of the special event trigger. Table 8-1 and Table 8-2 show the resources and interactions of the CCP module(s). In the following sections, the operation of a CCP module is described with respect to CCP1. CCP2 operates the same as CCP1, except where noted.

CCP1 Module:

Capture/Compare/PWM Register1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. The special event trigger is generated by a compare match and will reset Timer1.

CCP2 Module:

Capture/Compare/PWM Register2 (CCPR2) is comprised of two 8-bit registers: CCPR2L (low byte) and CCPR2H (high byte). The CCP2CON register controls the operation of CCP2. The special event trigger is generated by a compare match and will reset Timer1 and start an A/D conversion (if the A/D module is enabled).

Additional information on CCP modules is available in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023) and in application note AN594, "Using the CCP Modules" (DS00594).

TABLE 8-1: CCP MODE - TIMER RESOURCES REQUIRED

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

TABLE 8-2: INTERACTION OF TWO CCP MODULES

CCPx Mode	CCPy Mode	Interaction
Capture	Capture	Same TMR1 time-base
Capture	Compare	The compare should be configured for the special event trigger, which clears TMR1
Compare	Compare	The compare(s) should be configured for the special event trigger, which clears TMR1
PWM	PWM	The PWMs will have the same frequency and update rate (TMR2 interrupt)
PWM	Capture	None
PWM	Compare	None

APPENDIX B

Order this document by SG3525A/D

MOTOROLA

SG3525A
SG3527A

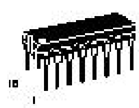
Pulse Width Modulator Control Circuits

The SG3525A, SG3527A pulse width modulator control circuits offer improved performance and lower external parts count when implemented for controlling all types of switching power supplies. The on–chip +5.1 V reference is trimmed to ±1% and the error amplifier has an input common–mode voltage range that includes the reference voltage, thus eliminating the need for external divider resistors. A sync input to the oscillator enables multiple units to be slaved or a single unit to be synchronized to an external system clock. A wide range of deadtime can be programmed by a single resistor connected between the C_T and Discharge pins. These devices also feature built–in soft–start circuitry, requiring only an external timing capacitor. A shutdown pin controls both the soft–start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft–start recycle with longer shutdown commands. The under voltage lockout inhibits the outputs and the changing of the soft–start capacitor when V_{CC} is below nominal. The output stages are totem–pole design capable of sinking and sourcing in excess of 200 mA. The output stage of the SG3525A features NOR logic resulting in a low output for an off–state while the SG3527A utilized OR logic which gives a high output when off.

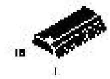
- 8.0 V to 35 V Operation
- 5.1 V ± 1.0% Trimmed Reference
- 100 Hz to 400 kHz Oscillator Range
- Separate Oscillator Sync Pin
- Adjustable Deadtime Control
- Input Undervoltage Lockout
- Latching PWM to Prevent Multiple Pulses
- Pulse–by–Pulse Shutdown
- Dual Source/Sink Outputs: ±400 mA Peak

PULSE WIDTH MODULATOR CONTROL CIRCUITS

SEMICONDUCTOR TECHNICAL DATA

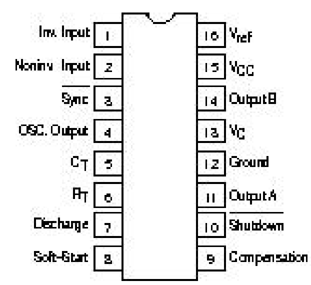


N SUFFIX
PLASTIC PACKAGE
CASE 648

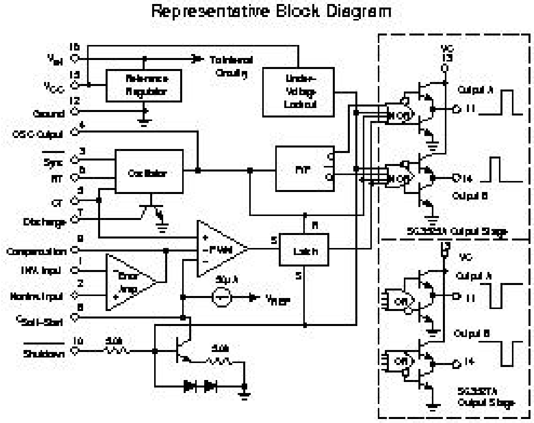


DW SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16L)

PIN CONNECTIONS



Representative Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
SG3525AN	T_A = 0° to +70°C	Plastic DIP
SG3525ADW		SO–16L
SG3527AN		Plastic DIP

Rev 2

SG3525A SG3527A

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs		−0.3 to +5.5	V
Analog Inputs		−0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±500	mA
Reference Output Current	I_{ref}	50	mA
Oscillator Charging Current		5.0	mA
Power Dissipation (Plastic & Ceramic Package) T_A = +25°C (Note 2) T_C = +25°C (Note 3)	P_D	 1000 2000	mW
Thermal Resistance Junction−to−Air	$R_{\theta JA}$	100	°C/W
Thermal Resistance Junction−to−Case	$R_{\theta JC}$	60	°C/W
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Lead Temperature (Soldering, 10 seconds)	T_{Solder}	+300	°C

NOTES: 1. Values beyond which damage may occur.
2. Derate at 10 mW/°C for ambient temperatures above +50°C.
3. Derate at 16 mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	8.0	35	Vdc
Collector Supply Voltage	V_C	4.5	35	Vdc
Output Sink/Source Current (Steady State) (Peak)	I_O	 0 0	 ±100 ±400	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.1	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	kΩ
Oscillator Timing Capacitor	C_T	0.001	0.2	μF
Deadtime Resistor Range	R_D	0	500	Ω
Operating Ambient Temperature Range	T_A	0	+70	°C

APPLICATION INFORMATION

Shutdown Options (See Block diagram, front page)

Since both the compensation and soft−start terminals (Pins 9 and 8) have current source pull−ups, either can readily accept a pull−down signal which only has to sink a maximum of 100 μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn−off signal to the outputs; and a 150 μA current sink begins to discharge the external soft−start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft−start capacitor, thus, allowing, for example, a convenient implementation of pulse−by−pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn−on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

SG3525A SG3527A

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, T_A = T_{low} to T_{high} [Note 4], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (T_J = +25°C)	V_{ref}	5.00	5.10	5.20	Vdc
Line Regulation (+8.0 V ≤ V_{CC} ≤ +35 V)	Reg_{line}	–	10	20	mV
Load Regulation (0 mA ≤ I_L ≤ 20 mA)	Reg_{load}	–	20	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T$	–	20	–	mV
Total Output Variation Includes Line and Load Regulation over Temperature	ΔV_{ref}	4.95	–	5.25	Vdc
Short Circuit Current (V_{ref} = 0 V, T_J = +25°C)	I_{SC}	–	80	100	mA
Output Noise Voltage (10 Hz ≤ f ≤ 10 kHz, T_J = +25°C)	V_n	–	40	200	μV_{rms}
Long Term Stability (T_J = +125°C) (Note 5)	S	–	20	50	mV/khr
OSCILLATOR SECTION (Note 6, unless otherwise noted.)					
Initial Accuracy (T_J = +25°C)		–	±2.0	±6.0	%
Frequency Stability with Voltage (+8.0 V ≤ V_{CC} ≤ +35 V)	$\frac{\Delta f_{osc}}{\Delta V_{CC}}$	–	±1.0	±2.0	%
Frequency Stability with Temperature	$\frac{\Delta f_{osc}}{\Delta T}$	–	±0.3	–	%
Minimum Frequency (R_T = 150 kΩ, C_T = 0.2 μF)	f_{min}	–	50	–	Hz
Maximum Frequency (R_T = 2.0 kΩ, C_T = 1.0 nF)	f_{max}	400	–	–	kHz
Current Mirror (I_{RT} = 2.0 mA)		1.7	2.0	2.2	mA
Clock Amplitude		3.0	3.5	–	V
Clock Width (T_J = +25°C)		0.3	0.5	1.0	μs
Sync Threshold		1.2	2.0	2.8	V
Sync Input Current (Sync Voltage = +3.5 V)		–	1.0	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = +5.1 V)					
Input Offset Voltage	V_{IO}	–	2.0	10	mV
Input Bias Current	I_{IB}	–	1.0	10	μA
Input Offset Current	I_{IO}	–	–	1.0	μA
DC Open Loop Gain (R_L ≥ 10 MΩ)	A_{VOL}	60	75	–	dB
Low Level Output Voltage	V_{OL}	–	0.2	0.5	V
High Level Output Voltage	V_{OH}	3.8	5.6	–	V
Common Mode Rejection Ratio (+1.5 V ≤ V_{CM} ≤ +5.2 V)	CMRR	60	75	–	dB
Power Supply Rejection Ratio (+8.0 V ≤ V_{CC} ≤ +35 V)	PSRR	50	60	–	dB
PWM COMPARATOR SECTION					
Minimum Duty Cycle	DC_{min}	–	–	0	%
Maximum Duty Cycle	DC_{max}	45	49	–	%
Input Threshold, Zero Duty Cycle (Note 6)	V_{th}	0.6	0.9	–	V
Input Threshold, Maximum Duty Cycle (Note 6)	V_{th}	–	3.3	3.6	V
Input Bias Current	I_{IB}	–	0.05	1.0	μA

NOTES: 4. T_{low} = 0° for SG3525A, 3527A T_{high} = +70°C for SG3525A, 3527A
5. Since long term stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
6. Tested at f_{osc} = 40 kHz (R_T = 3.6 kΩ, C_T = 0.01 μF, R_D = 0 Ω).

SG3525A SG3527A

ELECTRICAL CHARACTERISTICS (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit
SOFT–START SECTION					
Soft–Start Current ($V_{shutdown}$ = 0 V)		25	50	80	µA
Soft–Start Voltage ($V_{shutdown}$ = 2.0 V)		–	0.4	0.6	V
Shutdown Input Current ($V_{shutdown}$ = 2.5 V)		–	0.4	1.0	mA
OUTPUT DRIVERS (Each Output, V_{CC} = +20 V)					
Output Low Level (I_{sink} = 20 mA) (I_{sink} = 100 mA)	V_{OL}	 – –	 0.2 1.0	 0.4 2.0	V
Output High Level (I_{source} = 20 mA) (I_{source} = 100 mA)	V_{OH}	 18 17	 19 18	 – –	V
Under Voltage Lockout (V8 and V9 = High)	V_{UL}	6.0	7.0	8.0	V
Collector Leakage, V_C = +35 V (Note 7)	$I_{C(leak)}$	–	–	200	µA
Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	100	600	ns
Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	300	ns
Shutdown Delay (V_{DS} = +3.0 V, C_S = 0, T_J = +25°C)	t_{ds}	–	0.2	0.5	µs
Supply Current (V_{CC} = +35 V)	I_{CC}	–	14	20	mA

NOTE: 7. Applies to SG3525A only, due to polarity of output pulses.

Lab Test Fixture

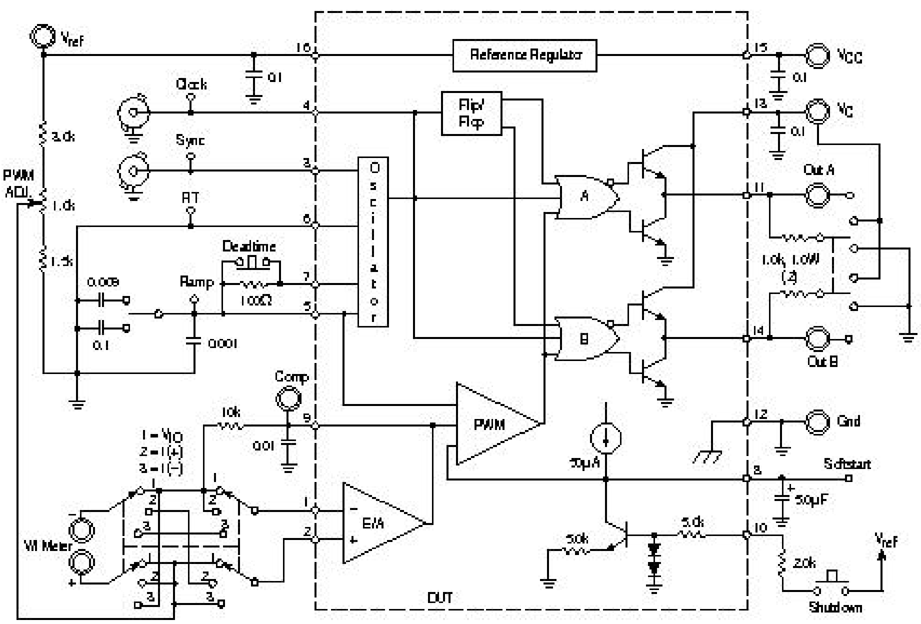


Figure 1. Oscillator Charge Time versus R_T

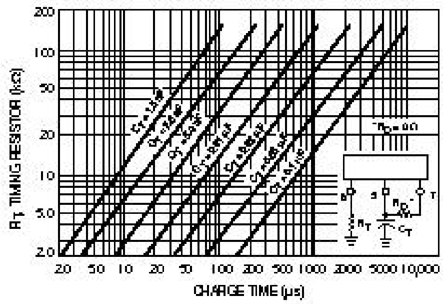


Figure 2. Oscillator Discharge Time versus R_D

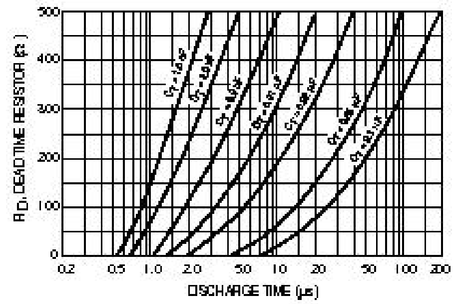


Figure 3. Error Amplifier Open Loop Frequency Response

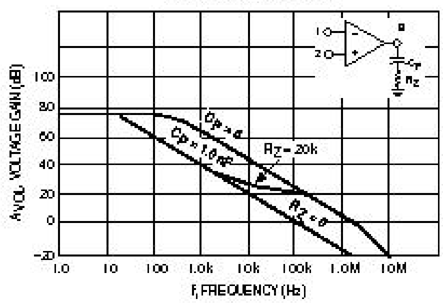


Figure 4. Output Saturation Characteristics (SG3525A)

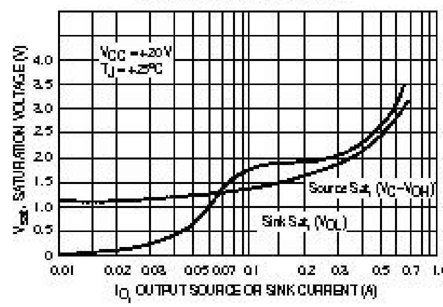


Figure 5. Oscillator Schematic (SG3525A)

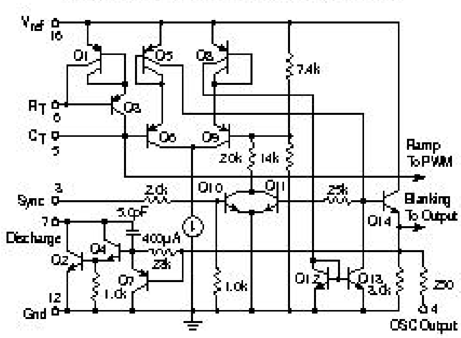


Figure 6. Error Amplifier Schematic (SG3525A)

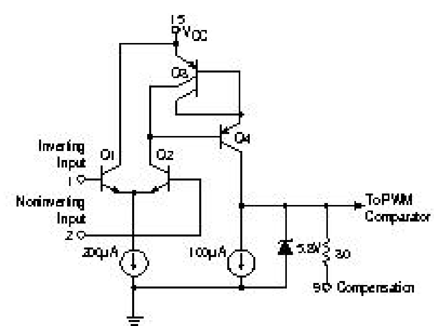


Figure 7. SG3525A Output Circuit
(1/2 Circuit Shown)

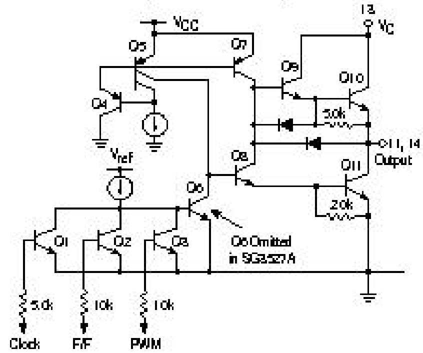
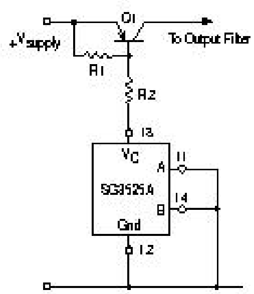
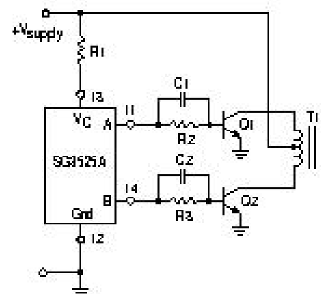


Figure 8. Single–Ended Supply



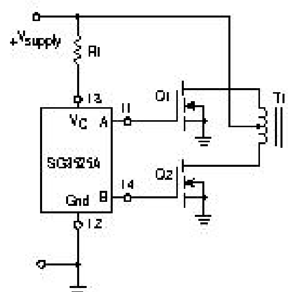
For single–ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem–pole source transistors on alternate oscillator cycles.

Figure 9. Push–Pull Configuration



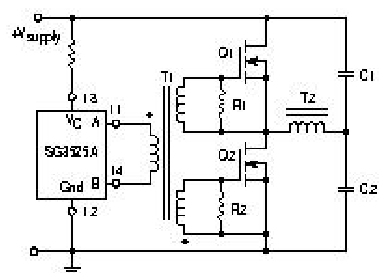
In conventional push–pull bipolar designs, forward base drive is controlled by R1–R3. Rapid turn–off times for the power devices are achieved with speed–up capacitors C1 and C2.

Figure 10. Driving Power FETS



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

Figure 11. Driving Transformers in a Half–Bridge Configuration

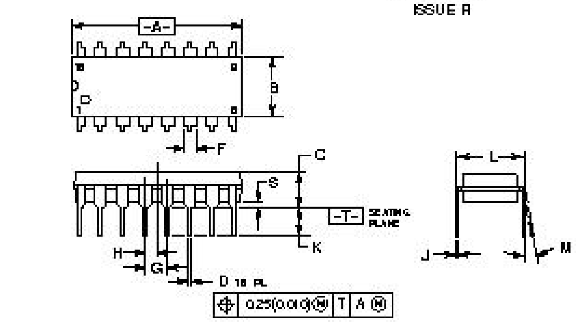


Low power transformers can be driven directly by the SG3525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

SG3525A SG3527A

OUTLINE DIMENSIONS

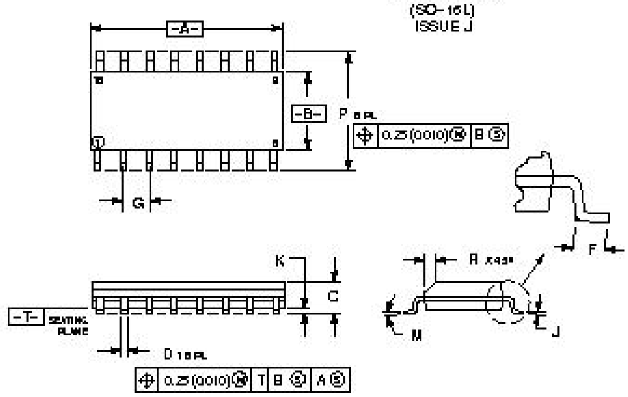
N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC PACKAGE
CASE 751B–05
(SO–16L)
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

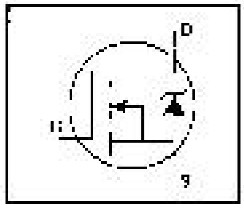
APPENDIX C

International Rectifier PD-9.620A

IRFBG30

HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



V_{DSS} = 1000V

$R_{DS(on)}$ = 5.0Ω

I_D = 3.1A

Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10 V	3.1	
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10 V	2.0	A
I_{DM}	Pulsed Drain Current	12	
P_D @ T_C = 25°C	Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy	260	mJ
I_{AR}	Avalanche Current	3.1	A
E_{AR}	Repetitive Avalanche Energy	13	mJ
dv/dt	Peak Diode Recovery dv/dt	[illegible]	V/ns
T_J	Operating Junction and	-55 to +150	
T_{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf•in (1.1 N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{θJC}$	Junction-to-Case	—	—	1.0	
$R_{θCS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	°C/W
$R_{θJA}$	Junction-to-Ambient			62	

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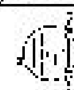
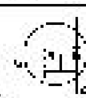
IRFBG30

IOR

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	1000	—	—	V	V_{GS}=0V, I_D= 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		1.4		V/°C	Reference to 25°C, I_D= 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	5.0	Ω	V_{GS}=10V, I_D=1.9A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D= 250µA
g_{fs}	Forward Transconductance	2.1		—	S	V_{DS}=100V, I_D=1.9A ④
I_{DSS}	Drain-to-Source Leakage Current			100	µA	V_{DS}=1000V, V_{GS}=0V
		—		500		V_{DS}=800V, V_{GS}=0V, T_J=125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS}=-20V
Q_g	Total Gate Charge			80		I_D=3.1A
Q_{gs}	Gate-to-Source Charge	—	—	10	nC	V_{DS}=400V
Q_{gd}	Gate-to-Drain ("Miller") Charge		—	42		V_{GS}=10V See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	18	—		V_{DD}=500V
t_r	Rise Time	—	25	—	ns	I_D=3.1A
$t_{d(off)}$	Turn-Off Delay Time	—	88	—		R_G=12Ω
t_f	Fall Time	—	29	—		R_D=170Ω, See Figure 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	600	—		V_{GS}=0V
C_{oss}	Output Capacitance	—	140	—	pF	V_{DS}=25V
C_{rss}	Reverse Transfer Capacitance		50			f=1.0MHz, See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	3.1	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①			12		
V_{SD}	Diode Forward Voltage	—	—	1.8	V	T_J=25°C, I_S=3.1A, V_{GS}=0V ④
t_{rr}	Reverse Recovery Time	—	410	620	ns	T_J=25°C, I_F=3.1A
Q_{rr}	Reverse Recovery Charge	—	1.5	2.0	µC	di/dt=100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

② V_{DD}=50V, starting T_J=25°C, L=57mH, R_G=25Ω, I_{AS}=3.1A (See Figure 12)

③ I_{SD}≤3.1A, di/dt≤40A/µs, V_{DD}≤600, T_J≤150°C

④ Pulse width ≤ 300 µs; duty cycle ≤2%.

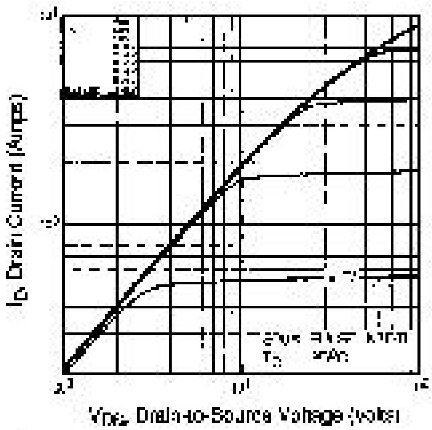


Fig 1. Typical Output Characteristics, T_C=25°C

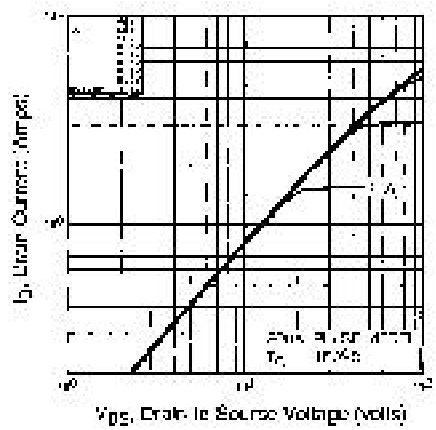


Fig 2. Typical Output Characteristics, T_C=150°C

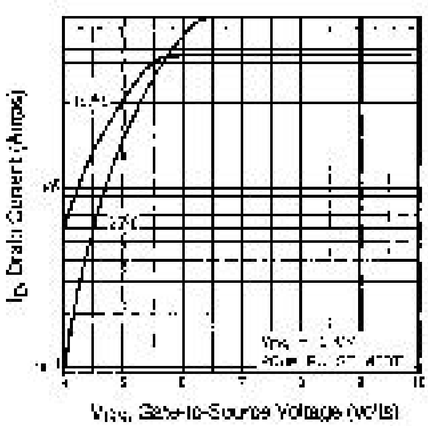


Fig 3. Typical Transfer Characteristics

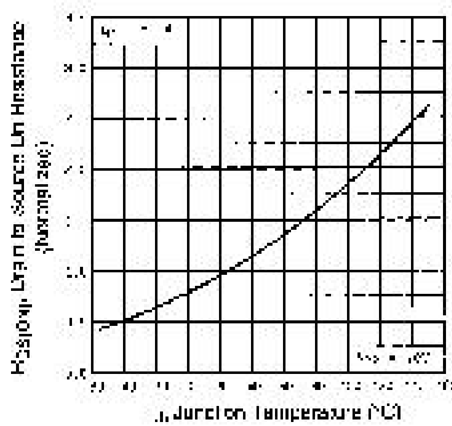


Fig 4. Normalized On-Resistance Vs. Temperature

IRFBG30

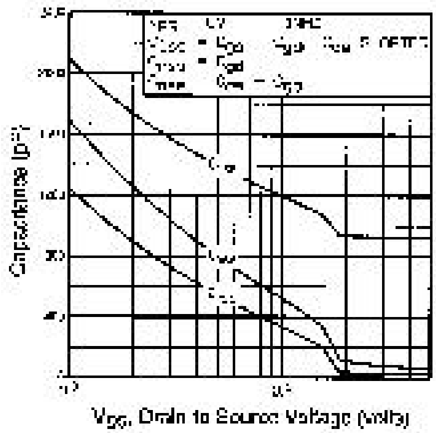


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

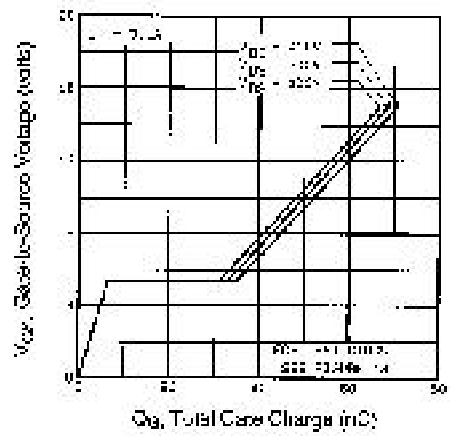


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

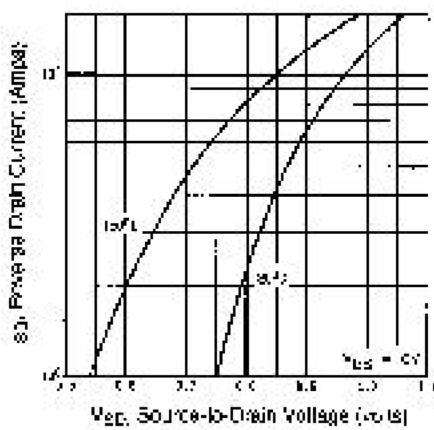


Fig 7. Typical Source-Drain Diode Forward Voltage

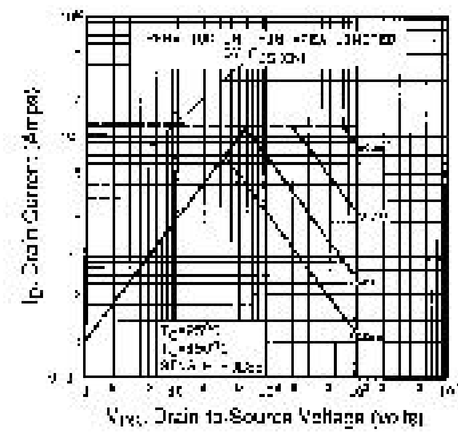


Fig 8. Maximum Safe Operating Area

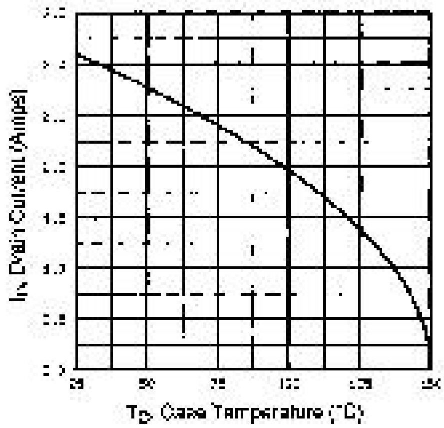


Fig 9. Maximum Drain Current Vs Case Temperature

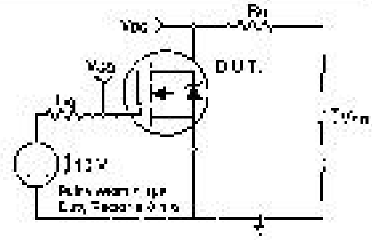


Fig 10a. Switching Time Test Circuit

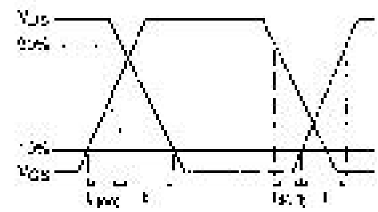


Fig 10b. Switching Time Waveforms

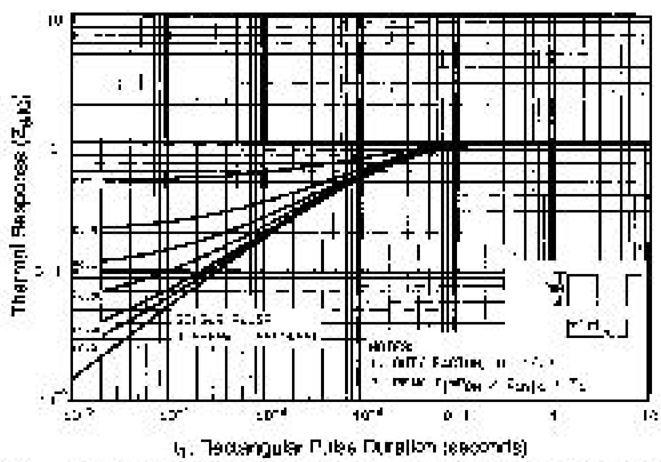


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRFBG30

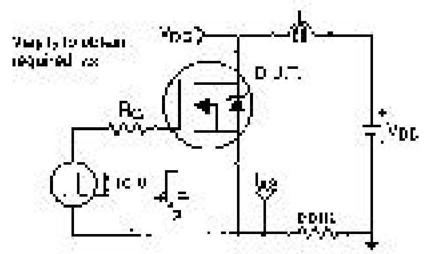


Fig 12a. Unclamped Inductive Test Circuit

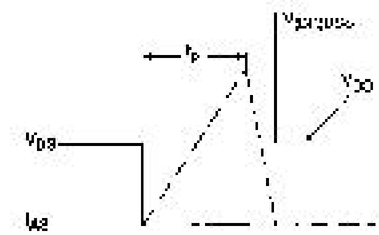


Fig 12b. Unclamped Inductive Waveforms

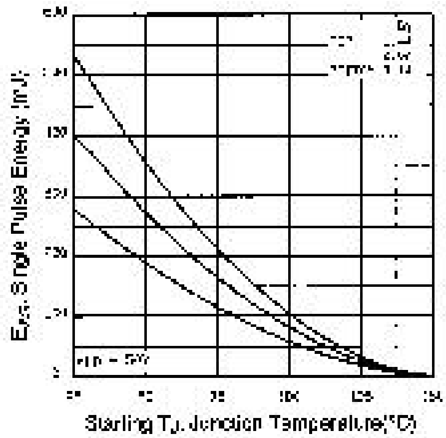


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

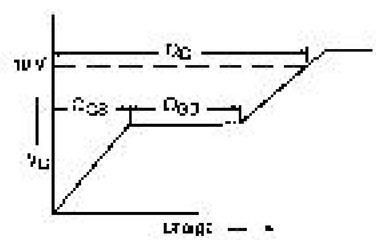


Fig 13a. Basic Gate Charge Waveform

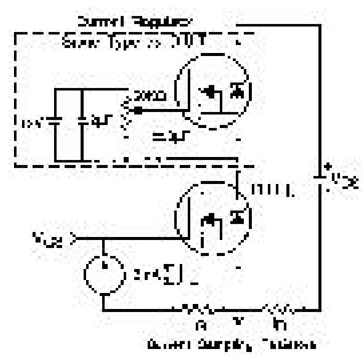


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1505

Appendix B: Package Outline Mechanical Drawing – See page 1509

Appendix C: Part Marking Information – See page 1516

Appendix E: Optional Leadforms – See page 1525

International Rectifier

APPENDIX D

FAIRCHILD
SEMICONDUCTOR™

GlobalOptoisolator™

VDE UL CSA SETI SEMKO DEMKO NEMKO BABT

4N25
4N26
4N27
4N28

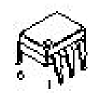
6-Pin DIP Optoisolators Transistor Output

The 4N25, 4N26, 4N27 and 4N28 devices consist of a gallium arsenide infrared emitting diode optically coupled to a monolithic silicon phototransistor detector.

- Most Economical Optoisolator Choice for Medium Speed, Switching Applications
- Meets or Exceeds All JEDEC Registered Specifications
- *To order devices that are tested and marked per VDE 0884 requirements, the suffix "V" must be included at end of part number. VDE 0884 is a test option.*

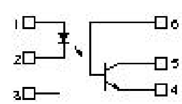
Applications

- General Purpose Switching Circuits
- Interfacing and coupling systems of different potentials and impedances
- I/O Interfacing
- Solid State Relays



STANDARD THRU HOLE

SCHEMATIC



PIN 1. LED ANODE
2. LED CATHODE
3. N.C.
4. EMITTER
5. COLLECTOR
6. BASE

MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Rating	Symbol	Value	Unit
INPUT LED			
Reverse Voltage	V_R	3	Volts
Forward Current — Continuous	I_F	60	mA
LED Power Dissipation @ $T_A = 25°C$ with Negligible Power in Output Detector Derate above 25°C	P_D	120 1.41	mW mW/°C
OUTPUT TRANSISTOR			
Collector–Emitter Voltage	V_{CEO}	30	Volts
Emitter–Collector Voltage	V_{ECO}	7	Volts
Collector–Base Voltage	V_{CBO}	70	Volts
Collector Current — Continuous	I_C	150	mA
Detector Power Dissipation @ $T_A = 25°C$ with Negligible Power in Input LED Derate above 25°C	P_D	150 1.76	mW mW/°C
TOTAL DEVICE			
Isolation Surge Voltage(1) (Peak ac Voltage, 60 Hz, 1 sec Duration)	V_{ISO}	7500	Vac(pk)
Total Device Power Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	250 2.94	mW mW/°C
Ambient Operating Temperature Range	T_A	−55 to +100	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Soldering Temperature (10 sec, 1/16" from case)	T_L	260	°C

1. Isolation surge voltage is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

FAIRCHILD SEMICONDUCTOR

4N25 4N26 4N27 4N28

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Min	Typ(1)	Max	Unit
INPUT LED						
Forward Voltage (I_F = 10 mA)	T_A = 25°C T_A = −55°C T_A = 100°C	V_F	— — —	1.15 1.3 1.05	1.5 — —	Volts
Reverse Leakage Current (V_R = 3 V)		I_R	—	—	100	μA
Capacitance (V = 0 V, f = 1 MHz)		C_J	—	18	—	pF
OUTPUT TRANSISTOR						
Collector–Emitter Dark Current (V_{CE} = 10 V, T_A = 25°C)	4N25,26,27 4N28	I_{CEO}	— —	1 1	50 100	nA
(V_{CE} = 10 V, T_A = 100°C)	All Devices	I_{CEO}	—	1	—	μA
Collector–Base Dark Current (V_{CB} = 10 V)		I_{CBO}	—	0.2	—	nA
Collector–Emitter Breakdown Voltage (I_C = 1 mA)		$V_{(BR)CEO}$	30	45	—	Volts
Collector–Base Breakdown Voltage (I_C = 100 μA)		$V_{(BR)CBO}$	70	100	—	Volts
Emitter–Collector Breakdown Voltage (I_E = 100 μA)		$V_{(BR)ECO}$	7	7.8	—	Volts
DC Current Gain (I_C = 2 mA, V_{CE} = 5 V)		h_{FE}	—	500	—	—
Collector–Emitter Capacitance (f = 1 MHz, V_{CE} = 0)		C_{CE}	—	7	—	pF
Collector–Base Capacitance (f = 1 MHz, V_{CB} = 0)		C_{CB}	—	19	—	pF
Emitter–Base Capacitance (f = 1 MHz, V_{EB} = 0)		C_{EB}	—	9	—	pF
COUPLED						
Output Collector Current (I_F = 10 mA, V_{CE} = 10 V)	4N25,26 4N27,28	I_C (CTR)(2)	2 (20) 1 (10)	7 (70) 5 (50)	— —	mA (%)
Collector–Emitter Saturation Voltage (I_C = 2 mA, I_F = 50 mA)		$V_{CE(sat)}$	—	0.15	0.5	Volts
Turn–On Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_{on}	—	2.8	—	μs
Turn–Off Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_{off}	—	4.5	—	μs
Rise Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_r	—	1.2	—	μs
Fall Time (I_F = 10 mA, V_{CC} = 10 V, R_L = 100 Ω)(3)		t_f	—	1.3	—	μs
Isolation Voltage (f = 60 Hz, t = 1 sec)(4)		V_{ISO}	7500	—	—	Vac(pk)
Isolation Resistance (V = 500 V)(4)		R_{ISO}	10^{11}	—	—	Ω
Isolation Capacitance (V = 0 V, f = 1 MHz)(4)		C_{ISO}	—	0.2	—	pF

1. Always design to the specified minimum/maximum electrical limits (where applicable).
2. Current Transfer Ratio (CTR) = I_C/I_F x 100%.
3. For test circuit setup and waveforms, refer to Figure 11.
4. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

TYPICAL CHARACTERISTICS

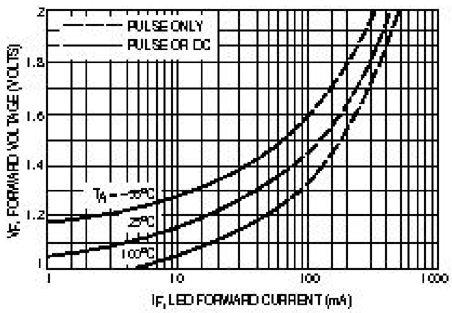


Figure 1. LED Forward Voltage versus Forward Current

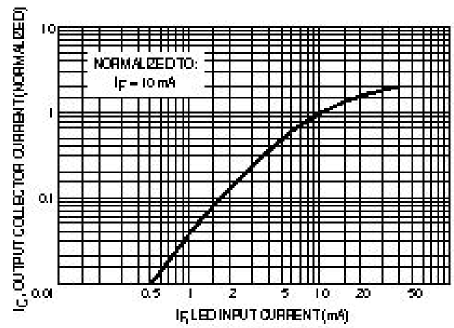


Figure 2. Output Current versus Input Current

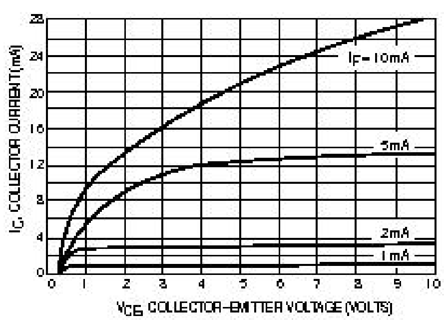


Figure 3. Collector Current versus Collector–Emitter Voltage

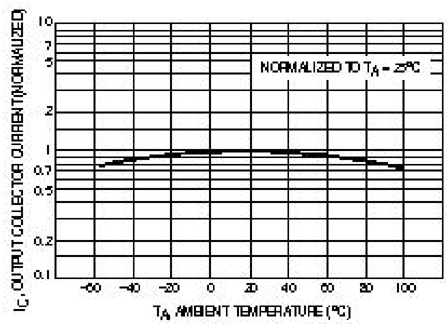


Figure 4. Output Current versus Ambient Temperature

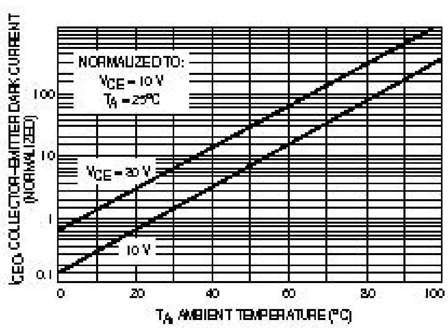


Figure 5. Dark Current versus Ambient Temperature

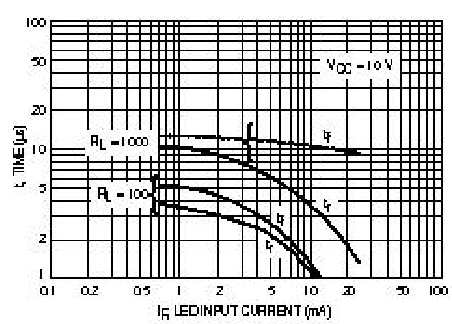


Figure 6. Rise and Fall Times (Typical Values)

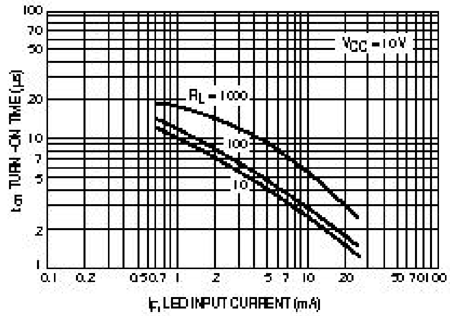


Figure 7. Turn–On Switching Times (Typical Values)

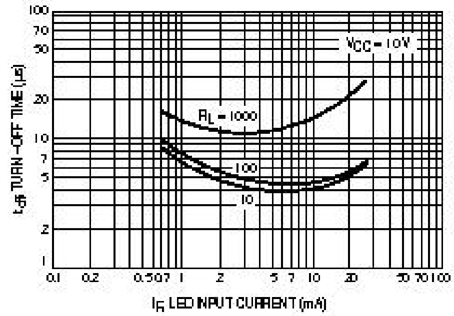


Figure 8. Turn–Off Switching Times (Typical Values)

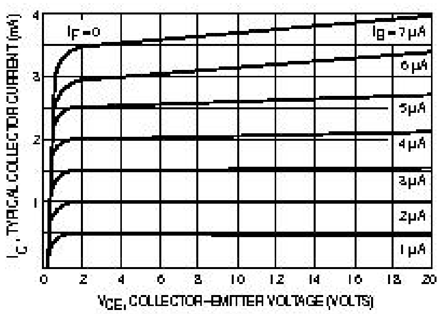


Figure 9. DC Current Gain (Detector Only)

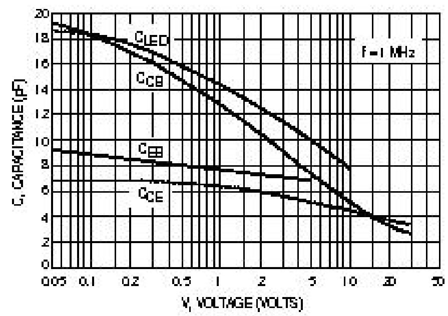


Figure 10. Capacitances versus Voltage

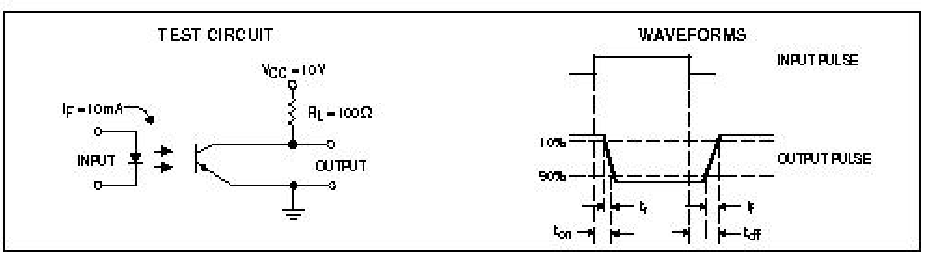
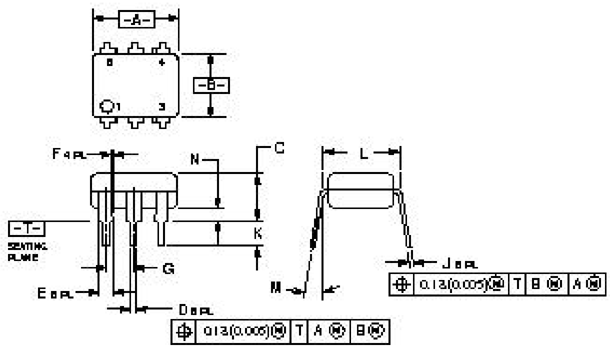


Figure 11. Switching Time Test Circuit and Waveforms

FAIRCHILD SEMICONDUCTOR

4N25 4N26 4N27 4N28

PACKAGE DIMENSIONS

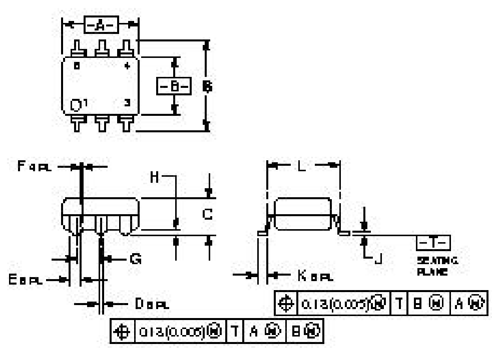


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.100	0.150	2.54	3.81
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.015	0.100	0.38	2.54

STYLE 1:
PIN 1. ANODE
2. CATHODE
3. NC
4. EMITTER
5. COLLECTOR
6. BASE

THRU HOLE



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
H	0.020	0.025	0.51	0.63
J	0.008	0.012	0.20	0.30
K	0.020	0.035	0.51	0.89
L	0.320 BSC		8.13 BSC	
S	0.332	0.390	8.43	9.90

SURFACE MOUNT

APPENDIX E

International
IOR Rectifier

Data Sheet No. PD60043-N

IR2101(S)
IR2102(S)

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout
- 3.3V, 5V, and 15V logic input compatible
- Matched propagation delay for both channels
- Outputs in phase with inputs (IR2101) or out of phase with inputs (IR2102)

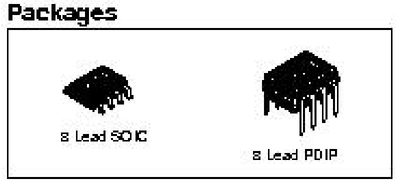
Product Summary

V_{OFFSET}	600V max.
I_O+/-	130 mA / 270 mA
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	160 & 150 ns
Delay Matching	50 ns

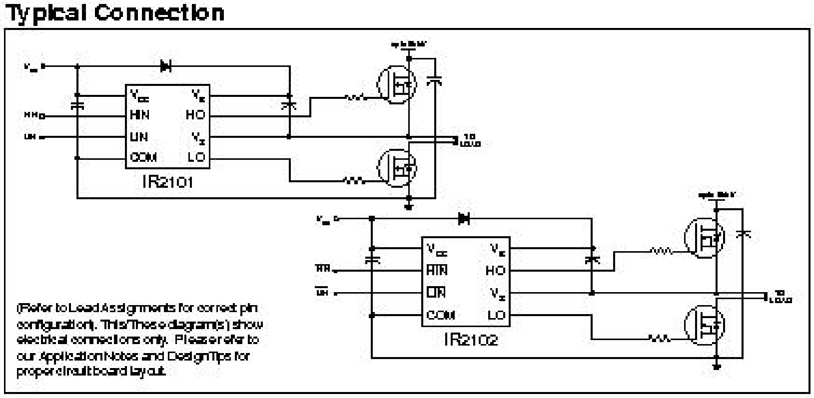
Description

The IR2101(S)/IR2102(S) are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

Packages



Typical Connection



www.irf.com 1

IR2101/IR2102 (S)

International
IOR Rectifier

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage		-0.3	625	V
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side and logic fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN & LIN)		-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable offset supply voltage transient		—	50	V/ns
P_D	Package power dissipation @ $T_A \le +25°C$	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
Rth_{JA}	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

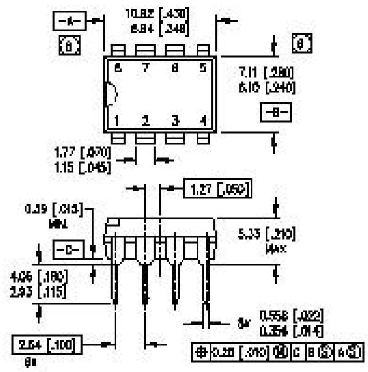
Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15V differential.

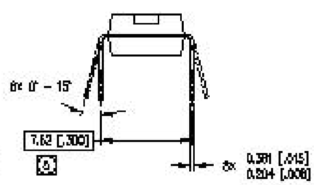
Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage (HIN & LIN) (IR2101) & ($\overline{HIN}$ & $\overline{LIN}$) (IR2102)	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note 1: Logic operational for V_S of -5 to +600V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

Case outlines

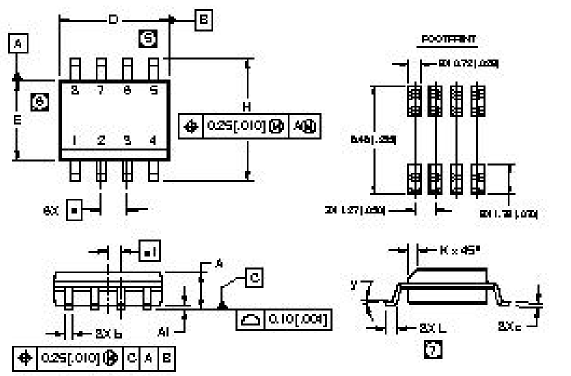


NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-001AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



01-6014
01-3003 01 (MS-001AB)

8 Lead PDIP



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027
01-0021 11 (MS-012AA)

8 Lead SOIC

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105

Data and specifications subject to change without notice. 4/18/2003