THE DEVELOPMENT OF BUCKBOOST CONVERTER FOR DC MOTOR SPEED CONTROL

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DEVELOPMENT OF BUCKBOOST CONVERTER FOR DC MOTOR SPEED CONTROL APPLICATION

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A report submitted as partial fulfillment of the requirements for the award of the degree
of Bachelor of Electrical Engineering (Power System)

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ABSTRACT

In the current century, DC motors plays a vital role in industrial areas. The efficient motor, are motor that be able to control the speed. Motor speed is controller by signal representing from microcontroller, in this project, the power converter for DC motor application is developed. One type of common method is by using Pulse Width Modulation (PWM), to control the speed of DC motor. Rectifiers which converted AC to DC supply and buck/boost converter are used to step up/step down a voltage or current while DC motor used as a load. Supplies to the DC motor are developed and the output is controlled by using PWM. PIC microcontroller is used to generate the PWM wave which can be varied in duty ratio, in order to create another level of DC voltage. This project starts with design circuit of a buck-boost converter using Orcad software and also Proteus 7.6 professional. In addition, hardware prototype has been developed based on the circuit designed. The system performance are evaluated and analyzed in comparison with a simulation results, at the end of this project the motor speed will satisfied the desired speed.

ABSTRAK

Pada abad ini, motor DC memainkan peranan penting dalam industri. Motor yang cekap, adalah motor yang boleh mengendalikan kelajuan. Kelajuan Motor kawalan oleh isyarat yang mewakili dari mikrokontroler, dalam projek ini, penukar kuasa untuk aplikasi motor DC dibangunkan. Salah satu jenis kaedah yang umum adalah dengan menggunakan kaedah Pulse Width Modulation (PWM), untuk mengawal kelajuan motor DC. Rectifier digunakan untuk menukar AC kepada DC dan buck / boost konverter digunakan untuk meningkatkan atau menurungkan voltan atau arus semasa motor DC digunakan sebagai beban. Perlengkapan untuk motor DC dibangunkan dan output dikawal dengan menggunakan PWM. PIC mikrokontroler digunakan untuk menghasilkan gelombang PWM yang boleh berubah-ubah nisbah, dalam rangka mencipta tahap voltan DC yang berbeza. Projek ini bermula dengan rangkaian mewujudkan sebuah konverter buck-boost menggunakan software Orcad dan juga Proteus 7.6 profesional. Selain itu, prototaip peranti keras telah dibangunkan berdasarkan pada rangkaian yang dirancang. Prestasi sistem dinilai dan dianalisis dibandingkan dengan hasil simulasi, pada akhir projek ini kelajuan motor akan memenuhi kelajuan yang dikehendaki.

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CHAPTER 1

INTRODUCTION

1.1 Project Background

This chapter briefly explain about Development of Buck-Boost Converter for DC Motor Speed Control application and its operation. This chapter also will explain the overview of project, objectives, scope of project, problem statement.

1.2 Overview of Project

Motor find the most practical use in our every day life in form of modern gadget device and application. Basically the core of electrical motor is to convert current into mechanical force. Motor have many type even in AC or DC type. Focus on DC motor, to control DC motor, are directly proportional to the supply voltage, so if we reduce the supply voltage from 12 Volts to 6 Volts, the motor will run at half the speed.

In this project, the design of adjustable SMPS regulator voltage is used to supply electrical energy. According to the research made by power supply designer, SMPS is better compare to linear power supply in term of efficiency, size and weight [1]

because the SMPS will regulate the voltage using Pulse-Width Modulation (PWM) technique. For linear power supply, it regulates the voltage or current by wasting excess voltage or current as heat which is very inefficient.

In this project the output voltage of this SMPS used to control the speed of a DC motor with specification 24V and 25W. The switching element in this SMPS will be connected to PIC microcontroller. Various output voltage will be regulated by changing the duty cycles of switching element [3].

1.3 Project Objective

The objective of this project is to;

i. Develop SMPS regulator voltage driving by Pulse Width Modulation (PWM) technique using PIC microcontroller type.
ii. To design SMPS where can be adjustable DC output voltage using Buck-Boost converter that regulate voltage using switching element driven by PWM technique using PIC microcontroller.
    a. Transistor used as switching element in this SMPS, where PWM technique is applied to switch the transistor fully on and fully off.
    b. PIC microcontroller can be programmed to generate various duty cycle based on desired value.
iii. To build a circuit that can control the output voltage which is can step up the voltage or can step down the output voltage.

1.4 Scope Project

i. Analyzing the applications of power electronic in the circuit of DC power supply such as rectifier, snubber circuit, and Dc-Dc buck/boost converter.

ii. PWM is generated using PIC microcontroller.
   - PIC microcontroller can be used to generate PWM, and the programming control duty cycle to be set, than the voltage output can be achieve based value desired.

iii. This project is to develop an adjustable output DC voltage.
   - This SMPS will use PIC microcontroller to generate PWM where it will control the duty cycle of switching. By using this PIC microcontroller, the duty cycle can be adjusted to produce variable output voltage using the Buck-Boost converter topology formula.

1.5 Problem Statement

In the current century, DC motors plays a vital role in industrial areas. DC motors are used widely to a machine, conveyer to produce a production.

Each day DC motor are popular widely used to a certain equipment, to make this motor more reliable:

i. DC-DC converters are required to supply various levels of voltages.

ii. Power supply that can provide energy for long duration usage is needed, in order to extend the lifetime, it is very important to optimize the efficiency of the DC-DC converter, especially the light load efficiency.
iii. The efficiency variation of a PWM synchronous buck-boost converter, are made to minimize the power loss.
iv. Using buck-boost converter also can improve the control speed of DC motor in order to step up or step down the speed desired.
v. Power supply that can be control the output voltage is less in market.

1.6 Thesis Outline

Chapter 1 explains the background of the project, the project objectives, scopes and the problem statement for Buck/boost converter for DC motor speed control application.
The concept of Pulse Width Modulation (PWM) is the major element for the development of
the system.

Chapter 2 is the theory on the key component used in this project. This includes the Power Mosfet, buckboost circuit, and DC motor. It also covers the literature review of these components.

Chapter 3 focuses on the methodologies for the development of the electrical structures and the implementations of microcontroller programming. It gives a brief review on the concept of PWM controller, the electronics structure for hardware development, the calculation involve and the programming for the operation of the systems.

Chapter 4 discusses on the results obtained of throughout the progress. All discussions are concentrating on the result and performance of the Buckboost converter for DC moter speed control application. The discussion is valuable for future development of any system similar to this project.

Chapter 5 is the conclusion for the project. It also discusses the future recommendation to improve the effectiveness, function, application and accuracy of the system. In addition, cost and commercialization sections are elaborated.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

These chapters review the study of DC motors, and explain in detail the operation of Pulse Width Modulation (PWM) control, switching mood power supply (SMPS), rectifier and buck-boost converter. Besides, all the circuit diagram and element that had been used to develop this project will be review in detail.

2.2 DC-DC Converter

2.2.1 Definition

DC to DC converter is an electronic circuit which converts a source of direct current (DC) from one voltage level to another [4].

DC to DC converters are important in portable electronic devices such as cellular phones and laptop computers, which are supplied with power from batteries primarily. Such electronic devices often contain several sub-circuits, each with its own voltage level requirement different from that supplied by the battery or an external supply. Additionally, the battery voltage declines as its stored power is drained. Switched DC to DC converters offer a method to increase voltage from a partially lowered battery voltage thereby saving space instead of using multiple batteries to accomplish the same thing. Most DC to DC converters also regulate the output voltage.

2.3 Switch-Mode Power Supply (SMPS)

A switched-mode power supply (SMPS) is an electronic power supply unit that incorporates a switching regulator in order to provide the required output voltage. An SMPS is actually a power converter that transmits power from a source (e.g., a battery or the electrical power grid) to a load (e.g., a personal computer) with ideally no loss. The function of the converter is to provide a reliable output voltage often at a different level than the input voltage.

SMPS is an electronic power supply unit that incorporates a switching regulator that is an internal control circuit that switches power transistor such as MOSFET rapidly on and off in order to stabilize the output voltage or current. Switching regulators are used as a replacement for the linear regulators when higher efficiency, smaller size and lighter weight are required. This greatly reduces the cooling requirements and allows a much higher power density. [3]

2.4 Pulse-Width Modulation (PWM)

Pulse-Width Modulation (PWM) are use for controlling analog circuits with a processors digital output. PWM uses a square wave whose duty cycle is modulated resulting in the variation of the average value of the waveform. PWM can be used to reduce the total amount of power delivered to a load without losses normally incurred when a power source is limited by resistive means. This is because the average power delivered is proportional to the modulation duty cycle. With a sufficiently high modulation duty cycle (D). With a sufficiently high modulation rate, passive electronic filters can be used to smooth the pulse train and recover an average analog waveform. High frequency PWM power control systems are easily realizable with semiconductor switch. The discrete on/off states of the modulation are used to control the state of the switch which correspondingly controls the voltage across or current through the load. The major advantage of this system is the switch are either off and not conducting any current, or on and have (ideally) no voltage drop across them. The product of the current and the voltage at any given time defines the power dissipated by the switch, thus no power is dissipated by the switch. Realistically, semiconductor switches such as MOSFETs or BJTs are non-ideal switches, but high efficiency controllers can still be build.

2.5 PIC 18F4550 Microcontroller

Many microcontrollers include on-chip PWM units. PIC 18F4550 has two, each of which has a selectable on-time and period. The duty cycle is the ratio of the on-time to the period, the modulating frequency is the inverse of the period. To start PWM operation, the data sheet suggests the software should:

- Set the period in the on-chip timer/ counter that provides the modulating square wave.
- Set the on-time in the PWM control register.
- Set the direction of the PWM output, which is one of the general-purpose I/O pins.
- Star the timer.
- Enable the PWM controller.

The standard PIC18 instruction set adds many enhancements to the previous PICmicro instruction sets, while maintaining an easy migration from these PICmicro instruction sets. Most instructions are a single program memory word (16 bits) but there are four instructions that require two program memory locations.
Each single-word instruction is a 16-bit word divided into an opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into four basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal** operations
- **Control** operations

CHAPTER 3

METHODOLOGY

3.1 Overview

This chapter explains about hardware development such as equipments, procedures and method design for a Buck Boost Converter in Motor. The relevant information is gathered through literature review from previous chapter. This chapter also will cover about designing the buck boost converter, software, part by part circuits and complete circuit. Before looking at the details of all methods below, it is best to begin with brief review of the system design.

3. 2 HARDWARE DEVELOPMENT

3.2.1 System Design

The output voltage of the converter is then varied by using pulse width modulation control which varies the duty cycle of the switch, and then Microcontroller is use to generate the PWM that can control switching of the MOSFET and also use to control the electric energy to operate a variable speed electric motor.

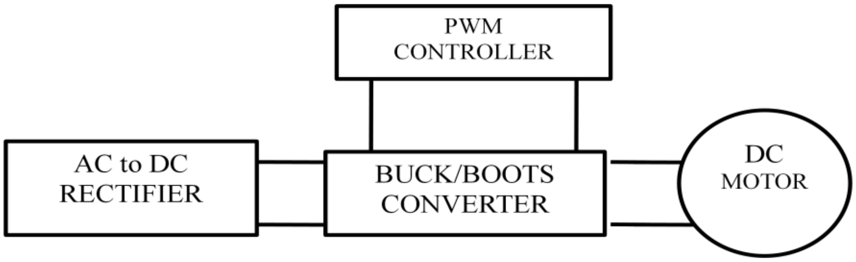


Figure 3.1: Simple Block Diagram

3.2.2 Buck Boost Converter

For the first part in this project are buck boost converter circuit, this circuit is needed in this project to control charging voltage from PV module to rechargeable battery and regulate the output of PV module. The circuit included parts of Buck Boost components such as Power MOSFET (IRFP150N), diode (1N4148), inductor and capacitor, and load resistor. Some of the designs criteria as show as follow:

i. POWER MOSFET (IRFP150N)

As illustrate in Figure 3.2, this power MOSFET has limitations operation in terms of voltage, current and power dissipation. The power absorbed by the gate drive circuitry should not significantly affect the overall efficiency. The power MOSFET current rating is related with the heat dissipated in the devices. This rating will be take in consideration for designing appropriate circuit to protect power MOSFET against high voltage and current, thus cause heat generation. While considering protection of power MOSFET against over voltage, a distinction has to be made between slowly varying over voltage and short time surge. It is about 100Vdc the minimum rating of drain to source breakdown voltage. Gate voltage must be 15-20V higher than the drain voltage. Being a high side switch, such gate voltage would have to be higher than the rail voltage, which is frequently the higher voltage available in the system. Refer APPENDIX for details specification.

The datasheet provided by manufacturers are given in order to ensure the devices neither connected in the specified limits nor exceeded.

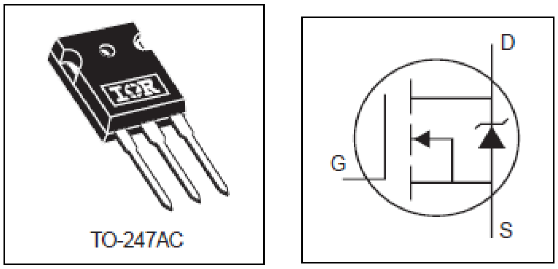


Figure 3.2: IRFP50N terminal pin configuration

ii. CAPACITOR

Except refer to capacitor value and rating of voltage use in system, the capacitor also supposed to be choose with minimum loss because switched power regulators are usually used in high current-performance power supplies. Loss occurs because of its internal series resistance and inductance. Commonly capacitors for switched regulators are chosen based on the equivalent series resistance (ESR).

iii. INDUCTOR

The function on inductor is to store energy and the value is selected to maintain a continuous current mode (CCM) operation as a rated of load (5.6Ω) is decided for this Buck converter. In CCM, current flow continuously in inductor during the entire switching cycle and output inductance selected to limit the peak to peak ripple current flowing. The factors to be considered in selecting the inductor are its peak to peak ripple current (CCM), maximum dc or peak current (not overheat) and maximum operating frequency (maximum core loss is not exceeded, resulting in overheating or saturation).

Design of Buck Boost converter circuit will consider as continuous current operation mode, CCM. The choice of switching frequency and inductance will affect the continuous current in Buck Boost converter design. Just for simple overview about buck boost converter, as the switching frequency increase, it can reduce the size of inductor in order to produce CCM and reduce capacitor size to limit output ripple in Buck Boost converter design.

Here the calculations method and formulas used in order to determine the values of the required components in Buck Boost converter design. This Buck Boost converter circuit is needed to produce an output voltage of 12Vdc from an input of 17.4Vdc.

Step 1: Determine the duty cycle, D to obtain required output voltage.

$$V_{OUT} = - V_{IN} \left(\frac{D}{1-D}\right) \tag{3.1}$$

Where:

D = duty cycle
V_{OUT} = Voltage output
V_{IN} = Voltage input

$$-12 = -17.4 \left(\frac{D}{1-D}\right)$$

$$0.69 = \left(\frac{D}{1-D}\right)$$

$$0.69 - 0.69D = D$$

$D = \underline{0.408}$ @ $\%D = \underline{40.8\%}$

At 0 duty cycle, there will be 0 volts across the load. At 50% duty cycle, the output voltage will have the same magnitude as the input voltage but will be inverted. The maximum duty cycle should be limited to avoid high peak currents and to prevent instability.

Step 2: Select a particular switching frequency (f) and device

Before Buck Boost converter circuit is design, the pulse width modulation (PWM) frequency should be determined. Basically, if the frequency increases, the efficiency of the Buck Boost converter also increases. Thus to choose a suitable PWM frequency for the Buck Boost converter, both of power consumption and the efficiency of the system need to be consider.

It is assumed that the design will use some kind of "Soft Switching", and/or "Low Losses/Non Dissipative Snubbers". Today, for a new, competitive power supply design, just using "Hard Switching" is no longer an option. That choosing the switching frequency must be done at the beginning of a new design, taking in consideration: power level, cooling method, application specifics.

i. Power levels 0-50W: any switching frequency between 100 kHz and 1 MHz may be a good choice, depending of application.
ii. Power levels 50W-500W: best choice would be between 200 kHz and 500 kHz. Use 200 kHz for a higher efficiency and 500 kHz for a higher density and easier filtering.
iii. Power levels 500W-5kW: best choice would be between 100 kHz and 200 kHz. Use 100 kHz for a higher efficiency; otherwise 200 kHz is the best choice.

For the project rating power of solar module is 80W so the switching frequency must in range 200 KHz and 500 KHZ. Assume the switching frequency is 250 KHz for this project.

Step 3: Determine minimum inductor, L_{min} size. The switching frequency and inductor size selected for CCM is f = 250 kHz with load resistor, R_L=5.6Ω

$$L_{min} = \frac{(1-D)^2 R}{2f} \tag{3.2}$$

Where:

L_{min} = Minimum inductor

D = Duty cycle

f = Frequency

R = Resistor

$$L_{min} = \frac{(1-0.632)^2 5.6}{2(250K)}$$

$$= \underline{1.52\mu H}$$

Step 4: To ensure CCM let inductor be 25% greater than minimum inductor value

$$L = 1.25\, L_{min} \tag{3.3}$$

$$= 1.25\,(1.52\mu H)$$

$$= \underline{1.9\mu H}$$

Step 5: The average current and the change in current

$$I_L = \frac{Vo}{R} \tag{3.4}$$

$$I_L = \underline{5A}$$

$$\Delta i_L = \frac{Vin\, DT}{L} \tag{3.5}$$

$$= \frac{(17.4)(0.408)(\frac{1}{250K})}{4.9u} \quad = \underline{5.8\text{A}}$$

Step 6: The maximum inductor current

$$I_{max} = I_L + \frac{\Delta iL}{2} \qquad (3.6)$$

$$= 5 + 5.8/2$$

$$= \underline{7.9\text{A}}$$

Step 7: The minimum inductor current

$$I_{min} = I_L - \frac{\Delta iL}{2} \qquad (3.7)$$

$$= 5 – 5.8/2$$

$$= \underline{2.1\text{A}}$$

Step 8: The capacitor if output ripple not exceed 2%

$$\Delta V_C = 2\% \text{ x } -12$$

$$= 0.24 \text{ V}$$

$$C = \frac{-Vo\ DT}{2\Delta VcR} \qquad (3.8)$$

$$= \frac{-(-12)(0.632)(\frac{1}{250K})}{2(0.24)(5.6)}$$

$$= \underline{11.3\mu\text{F}}$$

Figure 3.3 shows the basic construction of buck boost converter circuit using software OrCAD PSPICE based on calculations.

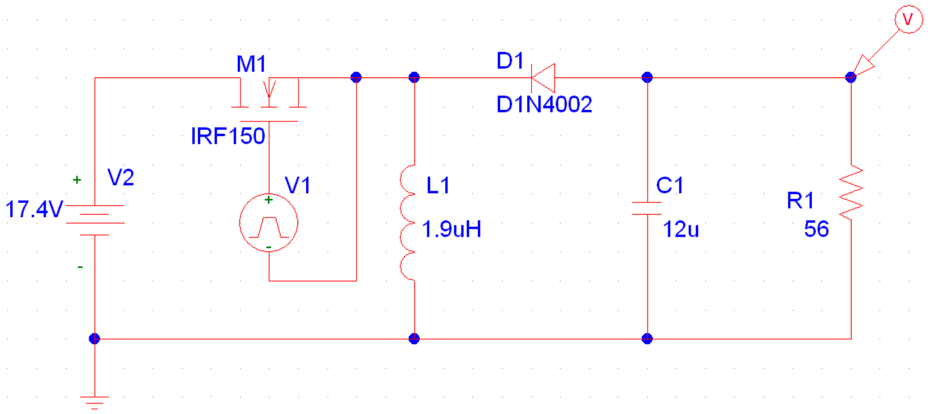


Figure 3.3: OrCAD PSPICE Schematic of Buck Boost Converter.

For this project Buck Boost Converter is use to constant the input voltage of the PV. The basic circuit is shown in Figure 3.3 that can produce the negative output voltage. From the circuit, V2 is the photovoltaic cell and V1 is the pulse generator that use to switching the POWER MOSFETF (M1) for the theoretical, this converter can operate at two conditions other switch OFF or switch ON. When the switching M1 is ON condition current will flow to inductor (L1) and increase the inductor current. After that, if the switching M1 is OFF, the current inductor will be collapse to charge the capacitor (C1). When the switch is turning on back, the capacitor now discharge and supply the voltage to resistor (R1).

The PWM of V1 is adjusted to 250KHZ. The duty cycle, D of the pulse generator V2 will be effect to the output of converter. The output voltage will be same the input voltage if D is 0.5 or 50% of the time switching. The output voltage will be increase if the D is greater than 0.5 and the output voltage will be decrease from input voltage if D is less than 0.5. So, to generate the constant output voltage at variable input voltage PV that must be use PWM to adjust the D automatically using the PIC18F4550 microcontroller.

For the charging battery, voltage must be greater than the voltage of battery. So the output of buck boost converter must be up to 13.8 volts to charging the battery 12 volts. From the simulation PSPICE software, Figure 3.3(a), (b) and (c) showed the graph output from the Buck Boost Converter. In order to vary the output voltage of converter some parameter of MOSFET switching at Pulse generator must be constant.

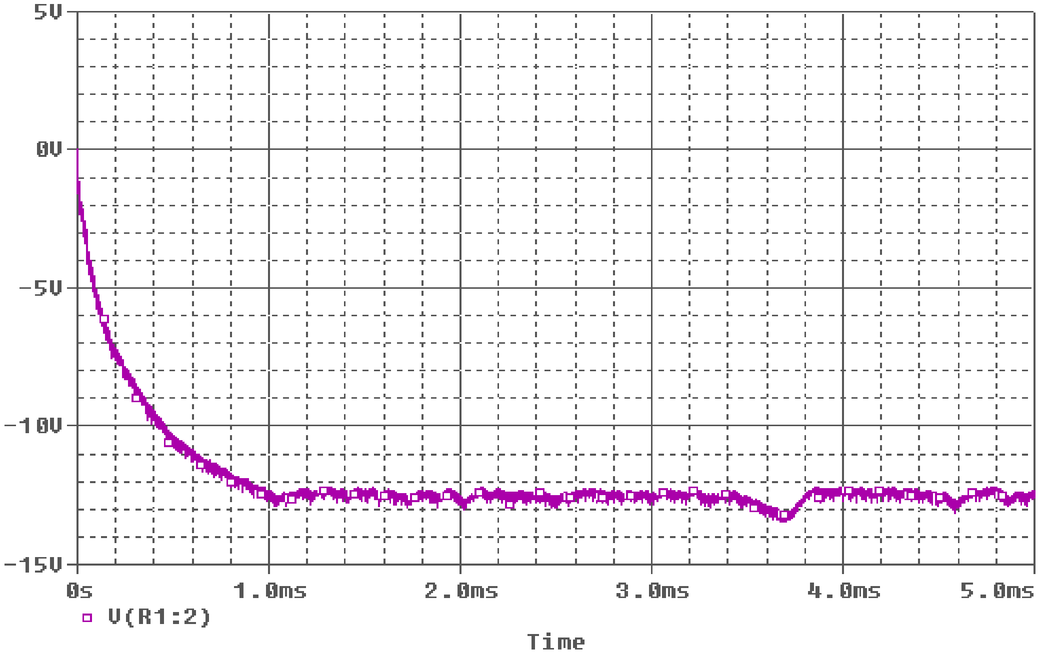


Figure 3.3(a), PSPICE simulation for V_{in} = 17.4 V; V_{out} = 12 V; D = 0.408

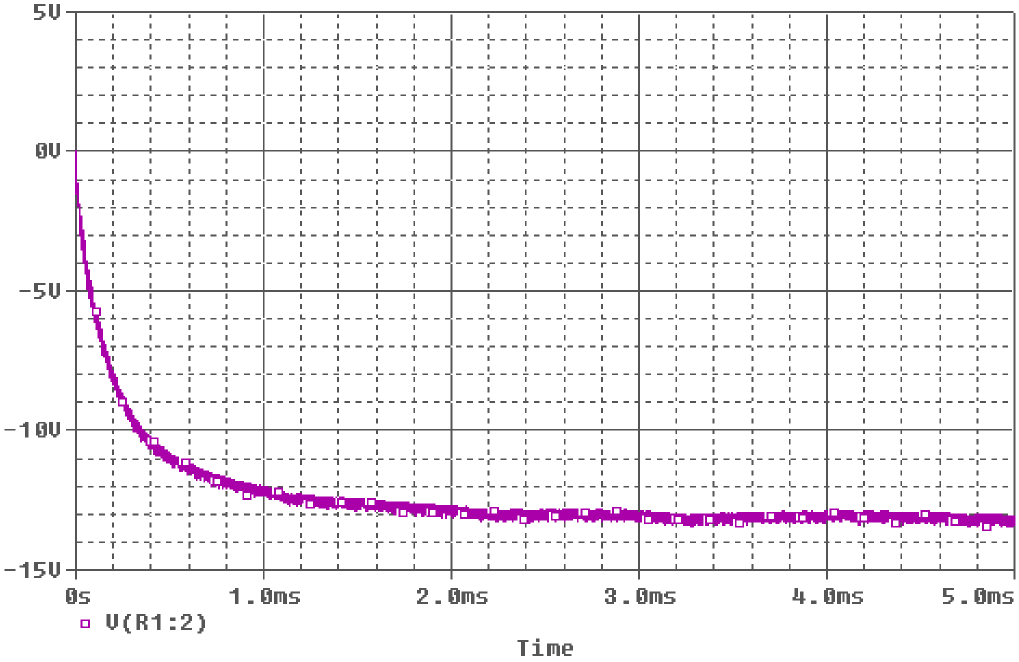


Figure 3.3(b), PSPICE simulation for V_{in} = 15.0 V; V_{out} = 12 V; D = 0.444

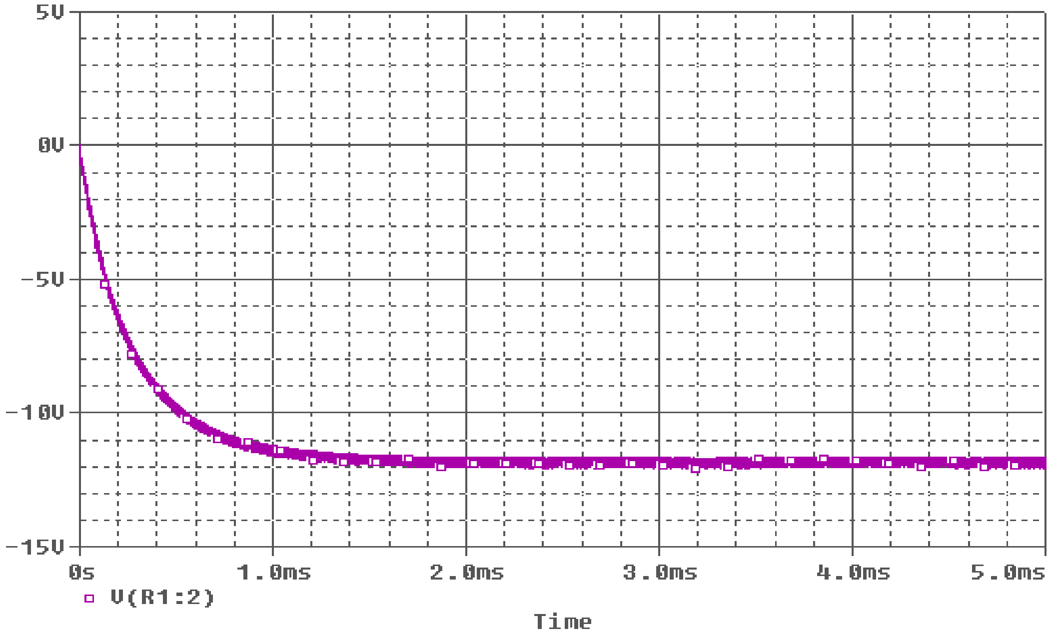


Figure 3.3(c), PSPICE simulation for V_{in} = 10.0 V; V_{out} = 12 V; D = 0.545

3.4 PIC 18F4550 Circuit Design

The second part is a microcontroller circuit. PIC 18F4550 microcontroller is used in this project to control POWER MOSFET switching duty cycle on the Buck Boost converter circuit. PIC 18F4550 has 40 pins. This microcontroller offers the advantages which are very easy to be assembled, can be reprogrammed and erased up to 10,000 times and also an economical price. Therefore it is very good for new product development phase. Figure 3.4 show 40 pin PDIP of PIC 18F4550 microcontroller.

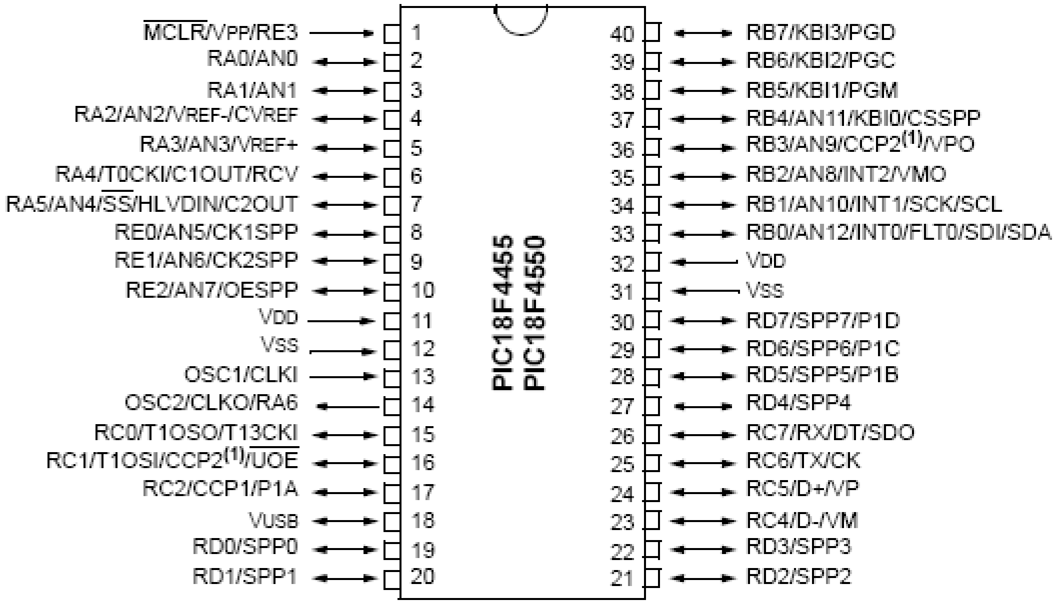


Figure 3.4: 40-Pin PDIP Diagram of PIC 18F4455/18F4550

Before generate PWM signal from PIC18F4550, there are several circuits that is compulsory for the system to function well. It were included the power supply, clock circuit, and reset circuit. Power supply circuit (Figure 3.5) is needed in the basic PIC18F4550 circuitry because 7805 regulator need to regulate the voltage supply of (>6V to 12V) so that the suitable voltage supply will drop at the PIC18F4550 V_{dd} pin12 and make the PIC to functioned.

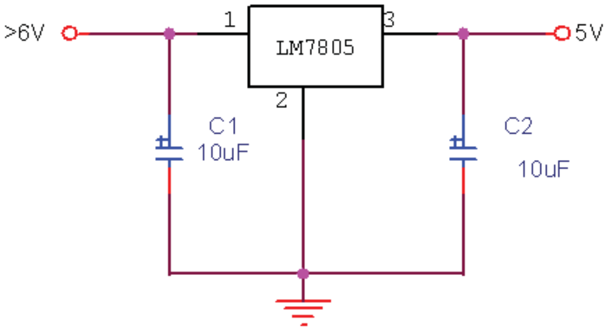


Figure 3.5: PIC 18F4550 power supply circuit

A simple RC circuit (Figure 3.6) is used to produce action-synchronizing clock pulses. 20-MHz resonator is used for the operation clock oscillation by PIC 18F4550. The precision of this oscillation frequency doesn't influence the precision of the clock. The precision of the clock is decided by the precision of the frequency which is inputted to pin13 (OSC1) and pin14 (OSC2).

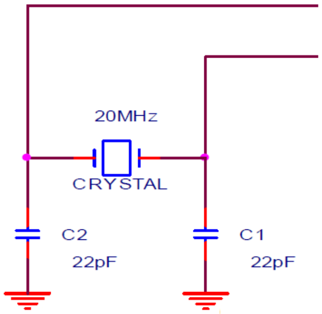


Figure 3.6: PIC 18F4550 clock circuit

Meanwhile, the reset circuit (Figure 3.7) is used so that the program from a known state. It will be reset when the Master Clear (/MCLR) pin is connected to the 0V supply (ground). The PIC has internal circuits to perform this function at power on and the simplest design involve merely connecting the /MCLR pin directly to the positive voltage supply through a resistor to the positive voltage supply. When the power supply is connected, the voltage rise too slowly then this reset function may not work. By having a capacitor, at switch on, the capacitor will discharges. The PIC will be held reset until the voltage /MCLR is above threshold value.

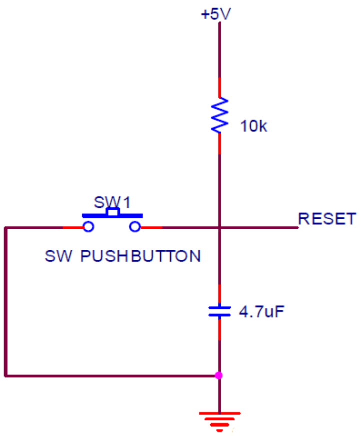
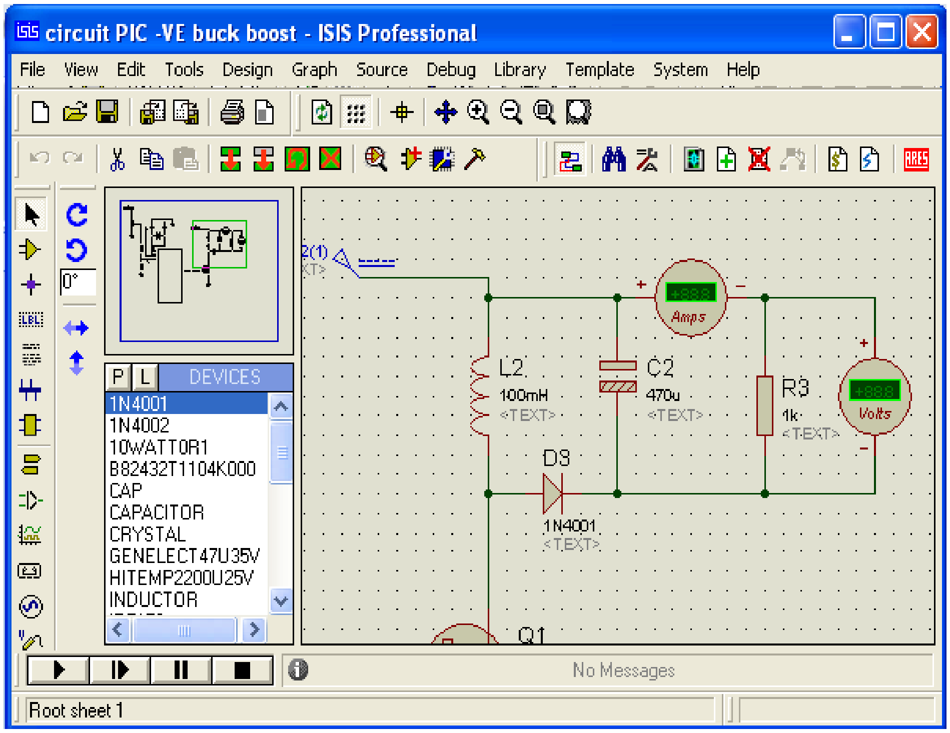


Figure 3.7: PIC 18F4550 reset circuit

3.5 SOFTWARE DEVELOPMENT

3.5.1 Proteus 7 Professional

The Proteus Design Suite is wholly unique in offering the ability to co-simulate both high and low-level micro-controller code in the context of a mixed-mode SPICE circuit simulation. With this Virtual System modeling facility, you can transform your product design cycle, reaping huge rewards in terms of reduced time to market and lower costs of development.



No Messages

Root sheet 1

Figure 3.8, Proteus Virtual System Modeling (VSM)

The Figure 3.8 above shown the Proteus Virtual System Modeling (VSM) combines mixed mode SPICE circuit simulation, animated components and microprocessor models to facilitate co-simulation of complete microcontroller based designs. For the first time ever, it is possible to develop and test such designs before a physical prototype is constructed.

3.3 LIST OF COMPONENT

Table 3.1 shows list component that used in this project.

Table 3.1; List of Component

No	Component	Specification	Quantity	Price
1	Microcontroller	PIC18F4550	1	Rm 25.00
2	Crystal	20MHz	1	Rm 2.50
3	Voltage regulator	LM7805	1	Rm 1.80
4	Power Mosfet	IRF150	1	Rm 5.00
5	Heat Sink	-	3	Rm 1.80
6	Zipper IC	40PIN	1	Rm 2.80
7	Stripe Board	Independent	1	Rm 5.00
8	Reset Button	small	1	Rm 0.50
9	Diode	IN4001	5	Rm 2.50
10	DC motor	12 volts dc motor	1	Rm 85.00
11	Resistor	3k	2	Rm 0.20
12	Resistor	1k	2	Rm 0.20
13	Resistor	10k	2	Rm 0.20
14	Inductor	100mH	2	Rm 1.20
15	Capacitor	4700uF	2	Rm 0.40
		Total Price		Rm134.10

CHAPTER 4

RESULT AND DISCUSSION

4.1 Introduction

This chapter discuss about the result obtained and the limitation of the project. These results include from hardware, software and also the analysis the wave PWM that are be produced. All related result will be show in this chapter.

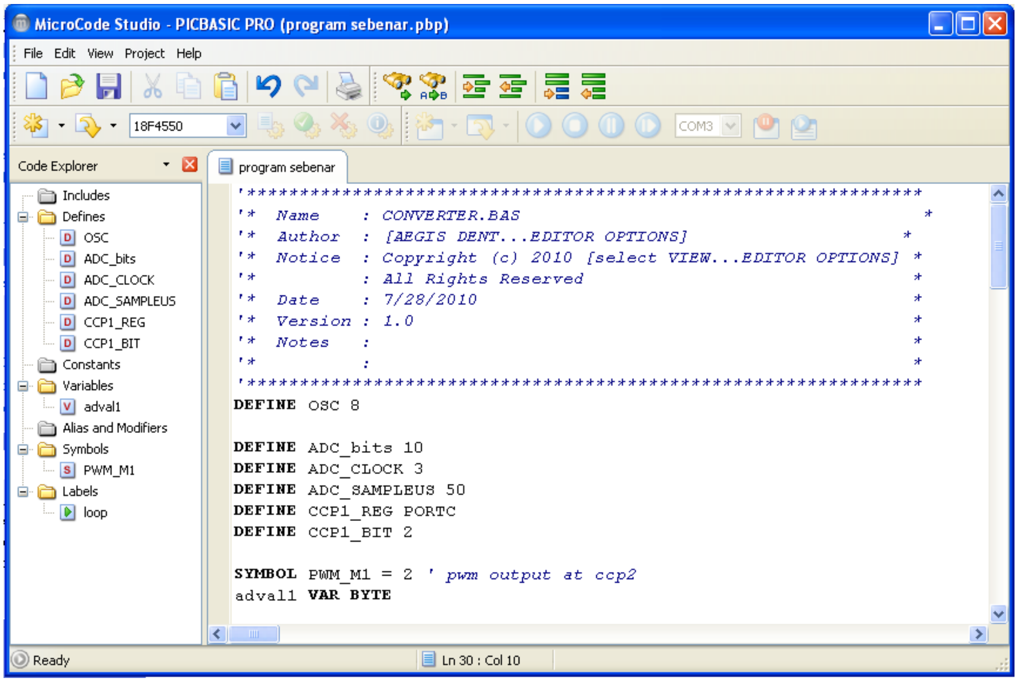
4.2 Software Implementation

For software implementation, MicroCode Studio is software was selected to program microcontroller in assembly language. Besides, Proteus is used to design the circuit and simulate the program that had been created by using Microcode Studio.

4.2.1 MicroCode Studio Software

MicroCode Studio is a powerful, visual Integrated Development Environment (IDE) with In Circuit Debugging (ICD) capability designed specifically for microEngineering Labs PICBASIC and PICBASIC PRO Compiler.

The main editor provides full syntax highlighting of your code with context sensitive keyword help and syntax hints. The code explorer allows to automatically jump to include files, defines, constants, variables, aliases and modifiers, symbols and labels that are contained within source code. Full cut, copy, paste and undo are provided, together with search and replace features.



```
'*****************************************************************
'*  Name    : CONVERTER.BAS                                       *
'*  Author  : [AEGIS DENT...EDITOR OPTIONS]                     *
'*  Notice  : Copyright (c) 2010 [select VIEW...EDITOR OPTIONS] *
'*          : All Rights Reserved                                *
'*  Date    : 7/28/2010                                          *
'*  Version : 1.0                                                *
'*  Notes   :                                                    *
'*          :                                                    *
'*****************************************************************
DEFINE OSC 8

DEFINE ADC_bits 10
DEFINE ADC_CLOCK 3
DEFINE ADC_SAMPLEUS 50
DEFINE CCP1_REG PORTC
DEFINE CCP1_BIT 2

SYMBOL PWM_M1 = 2 ' pwm output at ccp2
adval1 VAR BYTE
```

Figure 4.10: The window of MicroCode Studio.

Figure 4.10 shows the window of MicroCode Studio software. It's easy to set up compiler, assembler and programmer options or can let MicroCode Studio do it built in auto search feature. Compilation and assembler errors can easily be identified and corrected using the error results window. Just click on a compilation error and MicroCode Studio had been automatically take the error line. MicroCode Studio even comes with a serial communications window, allowing debugging and viewing serial output from the microcontroller.

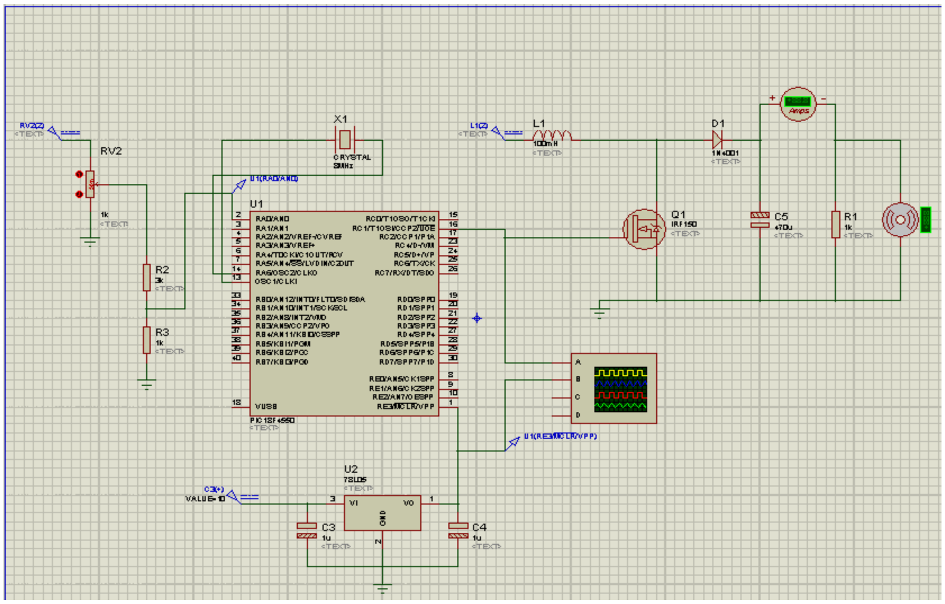


Figure 4.11: Overview by using Proteus software.

4.3 Hardware Development

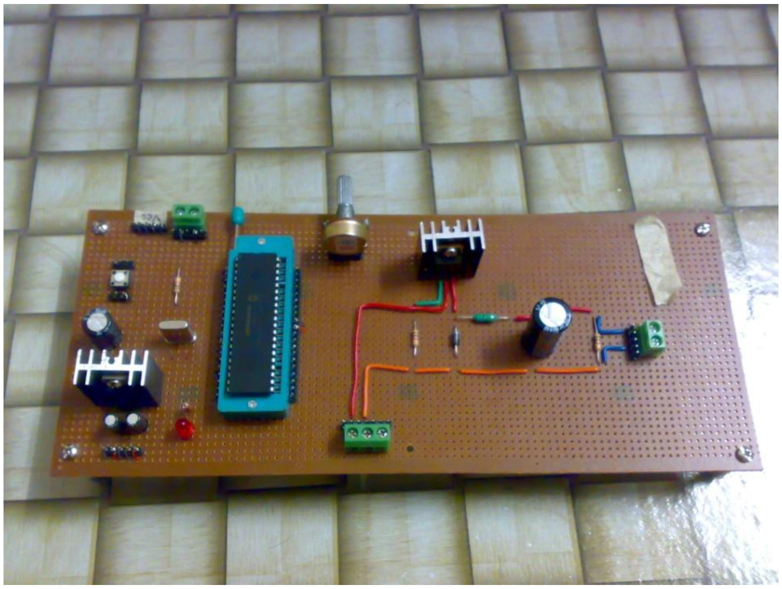


Figure 4.12: Complete Hardware is developed.

4.3.1 Expected Result

Analysis of Duty cycle before fabricating hardware, thus analysis is done by using Proteus software, after hardware finalized, the complete of adjustable PWM be analysis using oscilloscope.

- In the end of the project, SMPS can be controller by PWM technique using PIC controller, where we can get adjustable DC output at the same time control the speed of DC motor.
- Converter have advantages of low voltage stresses, low switch and inductor conduction losses, potential for small inductor size, and the ability to set the output dc voltage arbitrarily.

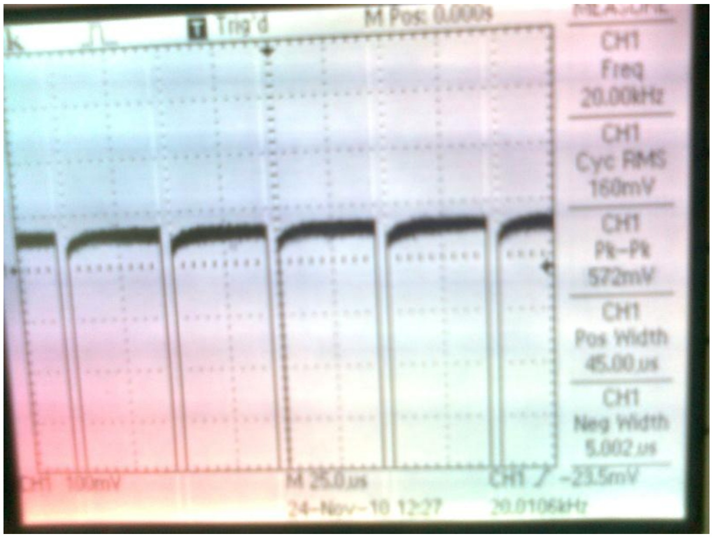


Figure 4.13: Pulse Width Modulation within 80% duty cycle

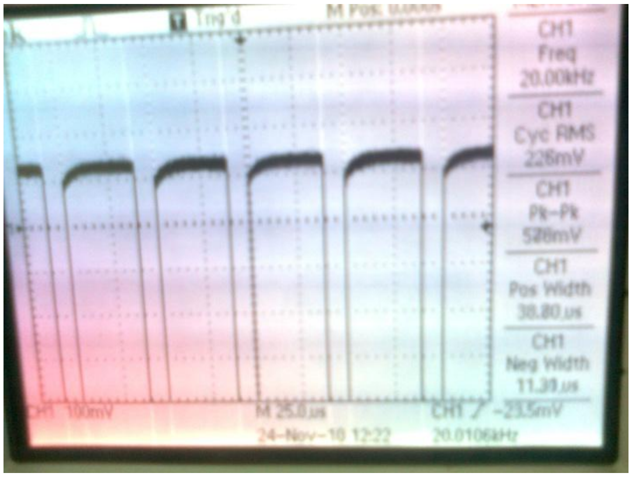


Figure 4.14: Pulse Width Modulation within 60% duty cycle

The complete circuit has been design in Proteus software to determine whether it functions or not using those programming are correct. Hex file from Microcode studio are loaded into PIC 18F4550, and simple drawing has be design like figure 4.11 to generate PWM. The output of the PWM automatically display after running this software, by using potential resistor that use as the analog digital converter, ADC to adjust the voltage detect from the microcontroller.

There are some different PWM that are generate with a different duty cycle, the voltage output will be increase when duty cycle is increase

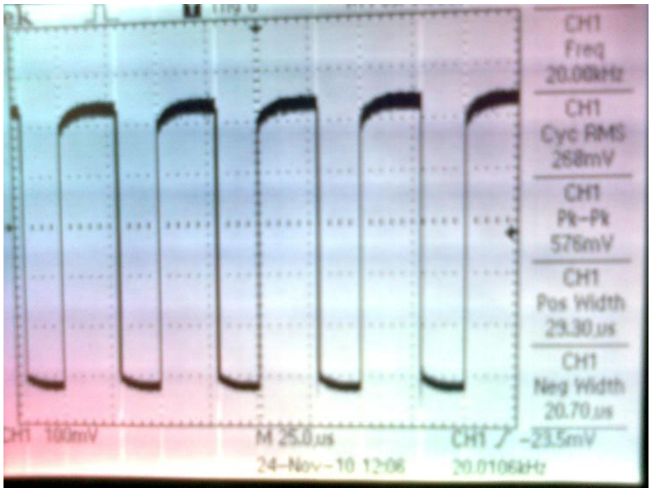


Figure 4.15: Pulse Width Modulation within 50% duty cycle

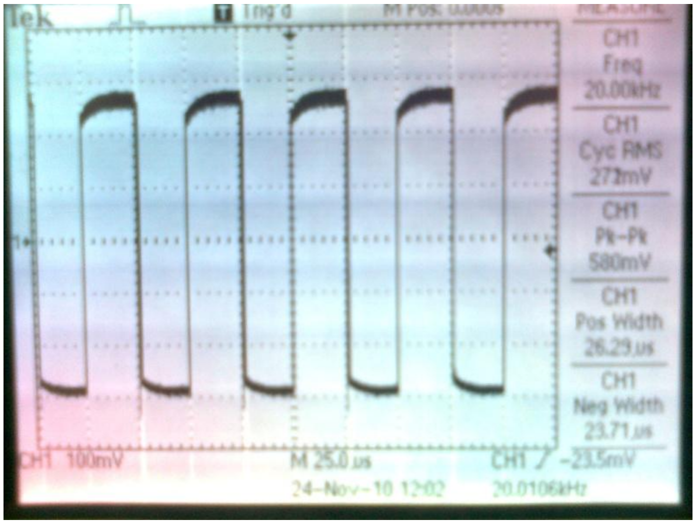


Figure 4.16: Pulse Width Modulation within 40% duty cycle

CHAPTER 5

CONCLUSION

Various tests and experiments are conducted on these modules. The result of these tests have revealed that the system have substance achievement.

5.1 Conclusion

This project has accomplished the main objective where to control DC speed motor by using Pulse Width Modulation (PWM). By using variable resistor, Duty cycle can be control based on PIC programmed.

The converter circuits, rectifier circuits have been discuss in previous chapter and the result shows everything about this project. Microcontroller PIC are play the most important role as medium to control DC output voltage, at the same time get the desired speed motor DC.

Pulse width Modulation (PWM), in this project acts like a brain to this circuit where are controlled with various Duty cycle D, by potential meter. By using voltage divide concept and some coding to PIC 18F4550, it can be done.

5.2 Recommendation

Throughout the development of Buck/boost Converter for DC speed control application, the author has come across several new ideas that will enhance the system. Some of the future work proposes are:

- Using DC driver motor to control the application of motor. This provides an alternative way to point any desired speed motor with interface way.
- Introduced other converter that can be used to forward and reverse the DC motor and not only focus on variable speed only.

REFERENCES

[1].H.W Whittington, B.W Flynn and D.E Macpherson. Switch Mode Power Supplies, McGraw-Hill, 1989.

[2] D.Zhou, "Synthesis of PWM Dc-to-Dc Power Converters," Ph.D, thesis, California Institute of Technology, October 1995.

[3]Severns, R.P, (1985). Modern DC-to-DC Switch Mode Power Converter Cicuits, Van Nostrand Reindhold.

[4] Dong-Kurl Kwak ; Seung-Ho Lee ; Do-Young Jung ; A new buck-boost dc/dc converter of high efficiency by soft switching technique, Power Electronics and Motion Control Conference, 2009. IPEMC '09. IEEE 6th International

[5].Micheal Barr. Embedded System Design: Introduction to pulse Width Modulation, Aug 31, 2001

[6] Application Report: Understanding Buck-Boost Power. Stages In Switch mode Power Supplies, Texas Instruments,1999.

[7] F J Borgum and E B G Nijhof. Inverter Circuit For A PWM Motor Speed Control System. Electronic Components and Application, May 1980

APPENDIX A

(GANNT CHAT)

Gantt chart

	PSM 1													
Task week	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PSM1 briefing	■													
Meeting with SV		■	■	■										
Project proposal draft		■	■	■										
Learning to use Orcad software				■	■	■	■							
Submitting abstract + slide + evaluation form								■	■					
Submitting project progress/summary	■	■	■	■	■	■	■	■	■	■	■	■	■	■
PSM1 seminar									■					
Submitting proposal report + log book + evaluation form													■	■
	PSM 2													
Task week	1	2	3	4	5	6	7	8	9	10	11	12	13	14
Develop circuit design using Orcad software	■	■	■											
Simulating circuit design	■	■	■											
Troubleshooting circuit design using Orcad software	■	■	■											
Developing hardware based on the circuit design				■	■	■	■	■	■	■	■	■		
Testing circuit using oscilloscope and multimeter				■	■	■	■	■	■	■	■	■		
Troubleshooting connections using multimeter				■	■	■	■	■	■	■	■	■	■	
Troubleshooting problems				■	■	■	■	■	■	■	■	■	■	
Submitting project progress/summary	■	■	■	■	■	■	■	■	■	■	■	■	■	■
PSM2 seminar											■	■		
Writing thesis										■	■	■	■	
Submitting thesis													■	■

APPENDIX B

(COODING PWM)

```
Define OSC 8
DEFINE ADC_BITS 8
DEFINE ADC_CLOCK 3
DEFINE ADC_SAMPLEUS 50



OUTPUT PORTC.1
PORTC = 0
D VAR BYTE
C VAR BYTE



ADCON1=%1100

MAIN:
   ADCIN 0,D
   ADCIN 1,C



SELECT CASE D
  CASE is <51
       PORTC.1 = 1
       PAUSE 50
       PORTC.1 = 0
       PAUSE 50
       goto MAIN
  CASE IS <102
```

```
      PORTC.1 = 1
       PAUSE 40
       PORTC.1 = 0
       PAUSE 60
       goto MAIN
   CASE is <153
       PORTC.1 = 1
       PAUSE 30
       PORTC.1 = 0
       PAUSE 70
       goto MAIN
   CASE is <204
       PORTC.1 = 1
       PAUSE 20
       PORTC.1 = 0
       PAUSE 80
       goto MAIN
   CASE is <255
       PORTC.1 = 1
       PAUSE 10
       PORTC.1 = 0
       PAUSE 90
       goto MAIN
END SELECT
goto MAIN
```

APPENDIX C

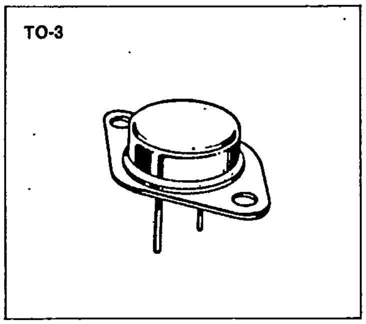
POWER MOSFET (IRF 150)

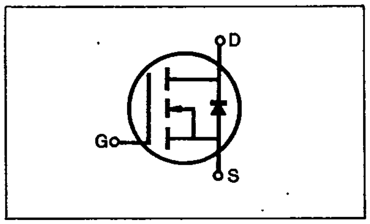
IRF150/151/152/153

N-CHANNEL POWER MOSFETS

FEATURES

- Low $R_{DS(on)}$
- Improved inductive ruggedness
- Fast switching times
- Rugged polysilicon gate cell structure
- Low input capacitance
- Extended safe operating area
- Improved high temperature reliability
- TO-3 package (High current)





PRODUCT SUMMARY

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRF150	100V	0.055Ω	40A
IRF151	60V	0.055Ω	40A
IRF152	100V	0.08 Ω	33A
IRF153	60V	0.08Ω	33A

MAXIMUM RATINGS

Characteristic	Symbol	IRF150	IRF151	IRF152	IRF153	Unit
Drain-Source Voltage (1)	V_{DSS}	100	60	100	60	Vdc
Drain-Gate Voltage (R_{GS}=1.0MΩ) (1)	V_{DGR}	100	60	100	60	Vdc
Gate-Source Voltage	V_{GS}	±20				Vdc
Continuous Drain Current T_C=25°C	I_D	40	40	33	33	Adc
Continuous Drain Current T_C=100°C	I_D	25	25	20	20	Adc
Drain Current—Pulsed (3)	I_{DM}	160	160	132	132	Adc
Gate Current—Pulsed	I_{GM}	±1.5				Adc
Total Power Dissipation @ T_C=25°C Derate above 25°C	P_D	150 1.2				Watts W/°C
Operating and Storage Junction Temperature Range	T_J, Tstg	−55 to 150				°C
Maximum Lead Temp. for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	300				°C

Notes: (1) T_J=25°C to 150°C
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%
(3) Repetitive rating: Pulse width limited by max. junction temperature

ELECTRICAL CHARACTERISTICS (T_C=25°C unless otherwise specified)

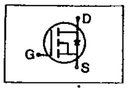
Characteristic	Symbol	Type	Min	Typ	Max	Units	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	IRF150 IRF152	100	—	—	V	V_{GS}=0V
		IRF151 IRF153	60	—	—	V	I_D=250μA
Gate Threshold Voltage	$V_{GS(th)}$	ALL	2.0	—	4.0	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Source Leakage Forward	I_{GSS}	ALL	—	—	100	nA	V_{GS}=20V
Gate-Source Leakage Reverse	I_{GSS}	ALL	—	—	-100	nA	V_{GS}=−20V
Zero Gate Voltage Drain Current	I_{DSS}	ALL	—	—	250	μA	V_{DS}=Max. Rating, V_{GS}=0V
			—	—	1000	μA	V_{DS}=Max. Rating×0.8, V_{GS}=0V, T_C=125°C
On-State Drain-Source Current (2)	$I_{D(on)}$	IRF150 IRF151	40	—	—	A	V_{DS}>$I_{D(on)}$×$R_{DS(on)\ max.}$, V_{GS}=10V
		IRF152 IRF153	33	—	—	A	
Static Drain-Source On-State Resistance (2)	$R_{DS(on)}$	IRF150 IRF151	—	0.04	0.055	Ω	V_{GS}=10V, I_D=20A
		IRF152 IRF153	—	0.06	0.08	Ω	
Forward Transconductance (2)	g_{fs}	ALL	9.0	12.3	—	℧	V_{DS}>$I_{D(on)}$×$R_{DS(on)\ max.}$, I_D=20A
Input Capacitance	C_{iss}	ALL	—	2900	3000	pF	V_{GS}=0V, V_{DS}=25V, f=1.0MHz
Output Capacitance	C_{oss}	ALL	—	1050	1500	pF	
Reverse Transfer Capacitance	C_{rss}	ALL	—	450	500	pF	
Turn-On Delay Time	$t_{d(on)}$	ALL	—	—	35	ns	V_{DD}=0.5BV_{DSS}, I_D=20A, Z_O=4.7Ω (MOSFET switching times are essentially independent of operating temperature.)
Rise Time	t_r	ALL	—	—	100	ns	
Turn-Off Delay Time	$t_{d(off)}$	ALL	—	—	125	ns	
Fall Time	t_f	ALL	—	—	100	ns	
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q_g	ALL	—	72	120	nC	V_{GS}=10V, I_D=50A, V_{DS}=0.8 Max. Rating (Gate charge is essentially independent of operating temperature.)
Gate-Source Charge	Q_{gs}	ALL	—	18	—	nC	
Gate-Drain ("Miller") Charge	Q_{gd}	ALL	—	54	—	nC	

THERMAL RESISTANCE

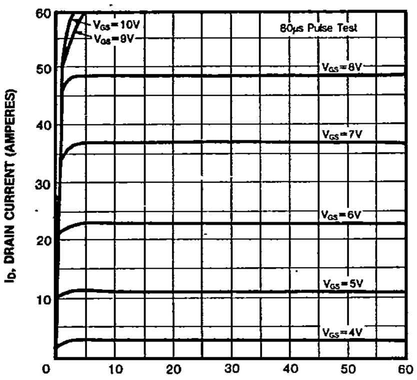
Junction-to-Case	R_{thJC}	ALL	—	—	0.83	K/W	
Case-to-Sink	R_{thCS}	ALL	—	0.1	—	K/W	Mounting surface flat, smooth, and greased
Junction-to-Ambient	R_{thJA}	ALL	—	—	30	K/W	Free Air Operation

Notes: (1) T_J=25°C to 150°C
(2) Pulse test: Pulse width≤300μs, Duty Cycle≤2%
(3) Repetitive rating: Pulse width limited by max. junction temperature

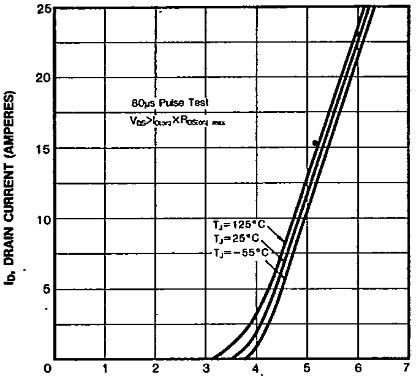
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristic	Symbol	Type	Min	Typ	Max	Units	Test Conditions
Continuous Source Current (Body Diode)	I_S	IRF150 IRF151	—	—	40	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier 
		IRF152 IRF153	—	—	33	A	
Pulse Source Current (Body Diode) (3)	I_{SM}	IRF150 IRF151	—	—	160	A	
		IRF152 IRF153	—	—	132	A	
Diode Forward Voltage (2)	V_{SD}	IRF150 IRF151	—	—	2.5	V	$T_C=25°C$, $I_S=40A$, $V_{GS}=0V$
		IRF152 IRF153	—	—	2.3	V	$T_C=25°C$, $I_S=33A$, $V_{GS}=0V$
Reverse Recovery Time	t_{rr}	ALL	—	600	—	ns	$T_J=150°C$, $I_F=40A$, $dI_F/dt=100A/\mu s$

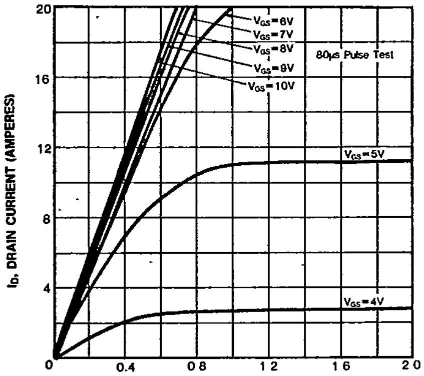
Notes: (1) $T_J=25°C$ to $150°C$ (2) Pulse test: Pulse width$\leq 300\mu s$, Duty Cycle$\leq 2\%$
(3) Repetitive rating: Pulse width limited by max. junction temperature



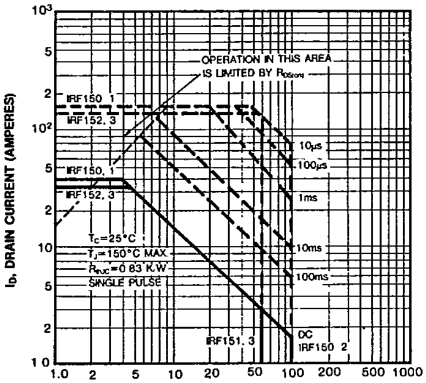
Typical Output Characteristics



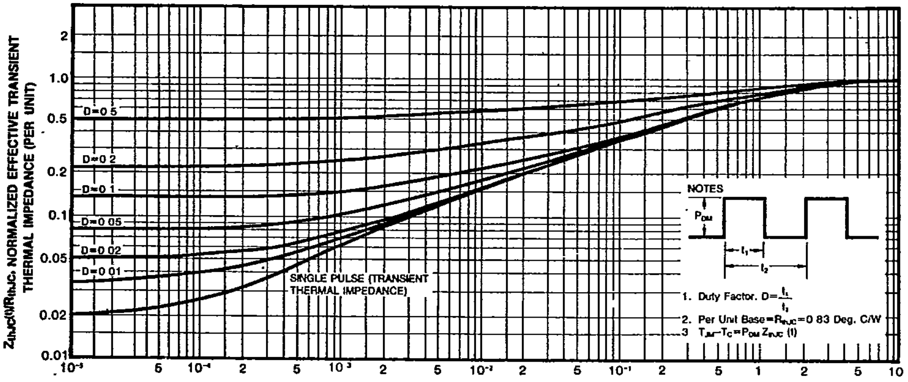
Typical Transfer Characteristics



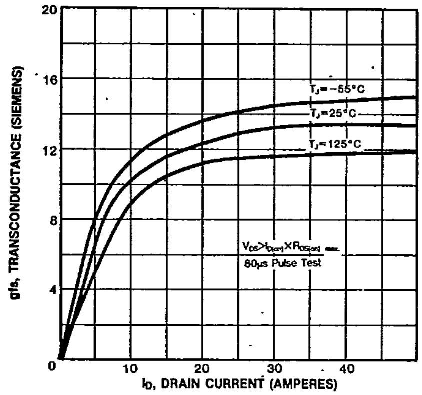
Typical Saturation Characteristics



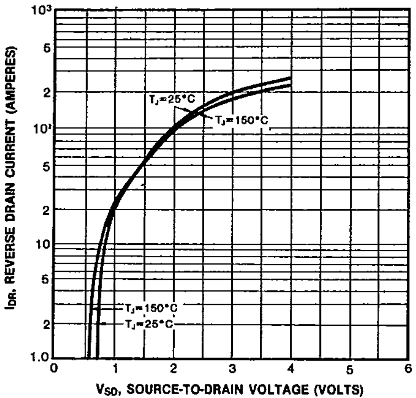
Maximum Safe Operating Area



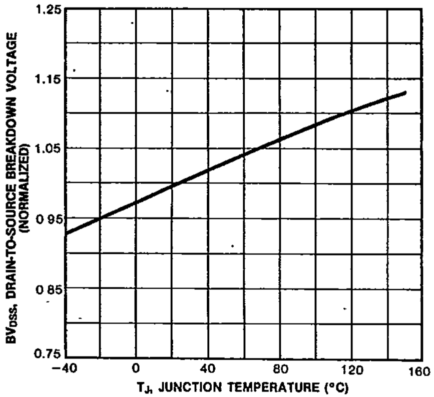
Maximum Effective Transient Thermal Impedance Junction-to-Case Vs. Pulse Duration



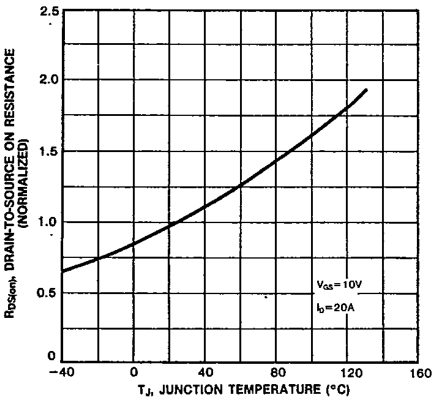
Typical Transconductance Vs. Drain Current



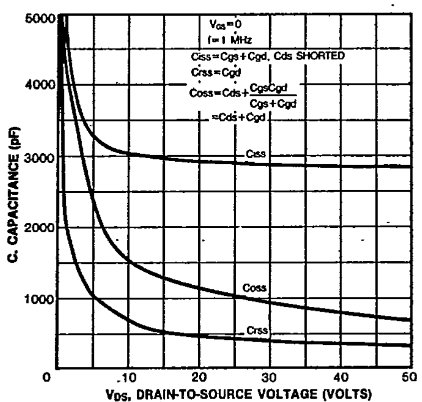
Typical Source—Drain Diode Forward Voltage



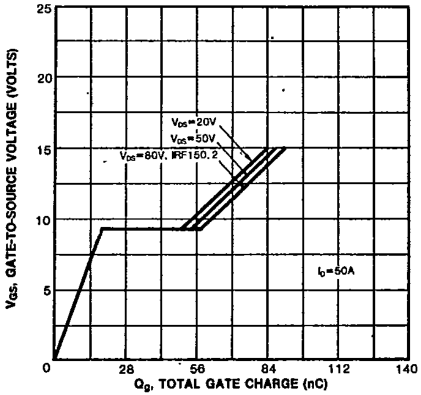
Breakdown Voltage Vs. Temperature



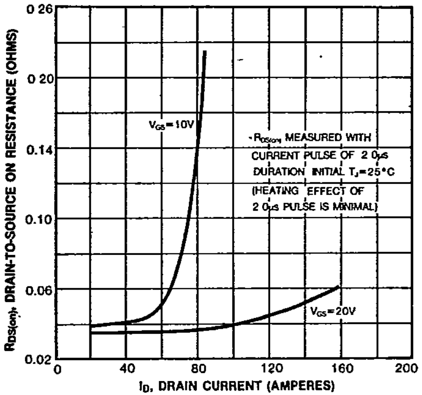
Normalized On-Resistance Vs. Temperature



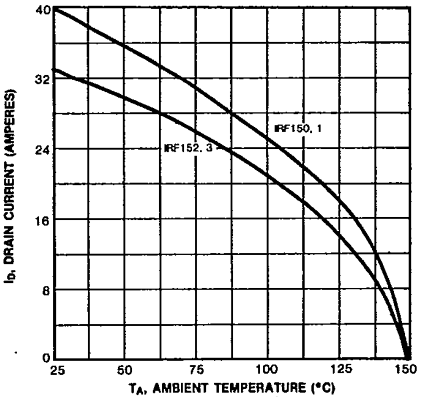
Typical Capacitance Vs. Drain to Source Voltage



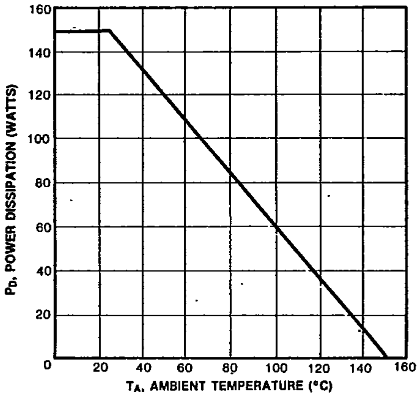
Typical Gate Charge Vs. Gate-To-Source Voltage



Typical On-Resistance Vs. Drain Current



Maximum Drain Current Vs. Case Temperature



Power Vs. Temperature Derating Curve

MICROCHIP

PIC18F2455/2550/4455/4550
Data Sheet

28/40/44-Pin High-Performance, Enhanced Flash USB Microcontrollers with nanoWatt Technology

APPENDIX D

(Datasheet PIC 18F4550)

MICROCHIP

PIC18F2455/2550/4455/4550

28/40/44-Pin High-Performance, Enhanced Flash USB Microcontrollers with nanoWatt Technology

Universal Serial Bus Features:

- USB V2.0 Compliant
- Low Speed (1.5 Mb/s) and Full Speed (12 Mb/s)
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- Supports up to 32 endpoints (16 bidirectional)
- 1-Kbyte dual access RAM for USB
- On-chip USB transceiver with on-chip voltage regulator
- Interface for off-chip USB transceiver
- Streaming Parallel Port (SPP) for USB streaming transfers (40/44-pin devices only)

Power-Managed Modes:

- Run: CPU on, peripherals on
- Idle: CPU off, peripherals on
- Sleep: CPU off, peripherals off
- Idle mode currents down to 5.8 μA typical
- Sleep mode currents down to 0.1 μA typical
- Timer1 oscillator: 1.1 μA typical, 32 kHz, 2V
- Watchdog Timer: 2.1 μA typical
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Four Crystal modes including High Precision PLL for USB
- Two External Clock modes, up to 48 MHz
- Internal oscillator block:
  - 8 user-selectable frequencies, from 31 kHz to 8 MHz
  - User-tunable to compensate for frequency drift
- Secondary oscillator using Timer1 @ 32 kHz
- Dual oscillator options allow microcontroller and USB module to run at different clock speeds
- Fail-Safe Clock Monitor
  - Allows for safe shutdown if any clock stops

Peripheral Highlights:

- High-current sink/source 25 mA/25 mA
- Three external interrupts
- Four Timer modules (Timer0 to Timer3)
- Up to 2 Capture/Compare/PWM (CCP) modules:
  - Capture is 16-bit, max. resolution 6.25 ns ($T_{CY}/16$)
  - Compare is 16-bit, max. resolution 100 ns (T_{CY})
  - PWM output: PWM resolution is 1 to 10-bit
- Enhanced Capture/Compare/PWM (ECCP) module:
  - Multiple output modes
  - Selectable polarity
  - Programmable dead time
  - Auto-Shutdown and Auto-Restart
- Enhanced USART module:
  - LIN bus support
- Master Synchronous Serial Port (MSSP) module supporting 3-wire SPI™ (all 4 modes) and I^{2}C™ Master and Slave modes
- 10-bit, up to 13-channels Analog-to-Digital Converter module (A/D) with programmable acquisition time
- Dual analog comparators with input multiplexing

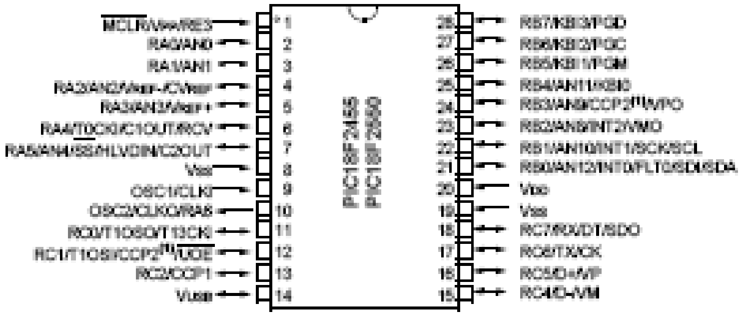
Special Microcontroller Features:

- C compiler optimized architecture with optional extended instruction set
- 100,000 erase/write cycle Enhanced Flash program memory typical
- 1,000,000 erase/write cycle Data EEPROM memory typical
- Flash/Data EEPROM Retention: > 40 years
- Self-programmable under software control
- Priority levels for interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 41 ms to 131s
- Programmable Code Protection
- Single-Supply 5V In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via two pins
- Optional dedicated ICD/ICSP port (44-pin devices only)
- Wide operating voltage range (2.0V to 5.5V)

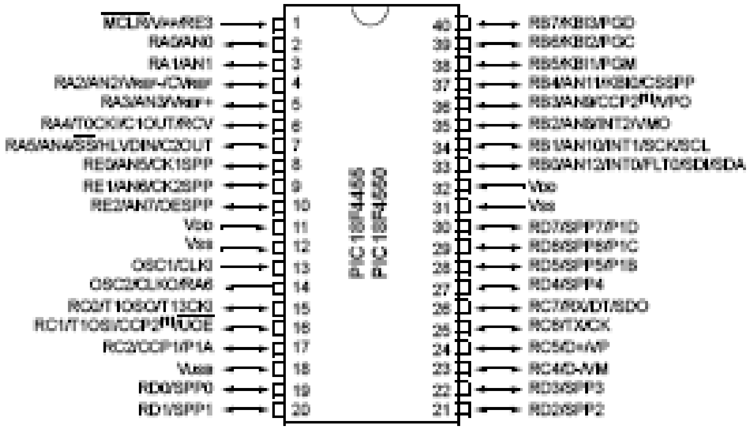
Device	Program Memory		Data Memory		I/O	10-bit A/D (ch)	CCP/ECCP (PWM)	SPP	MSSP		EAUSART	Comparators	Timers 8/16-bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)					SPI™	Master I^{2}C™			
PIC18F2455	24K	12288	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F2550	32K	16384	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F4455	24K	12288	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3
PIC18F4550	32K	16384	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3

Pin Diagrams

28-Pin PDIP, SOIC



40-Pin PDIP



Note 1: RB3 is the alternate pin for CCP2 multiplexing.

TABLE 1-1: DEVICE FEATURES

Features	PIC18F2455	PIC18F2550	PIC18F4455	PIC18F4550
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	24576	32768	24576	32768
Program Memory (Instructions)	12288	16384	12288	16384
Data Memory (Bytes)	2048	2048	2048	2048
Data EEPROM Memory (Bytes)	256	256	256	256
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/ Compare/PWM Modules	0	0	1	1
Serial Communications	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART
Universal Serial Bus (USB) Module	1	1	1	1
Streaming Parallel Port (SPP)	No	No	Yes	Yes
10-bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Comparators	2	2	2	2
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow ($\overline{\text{PWRT}}$, OST), $\overline{\text{MCLR}}$ (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow ($\overline{\text{PWRT}}$, OST), $\overline{\text{MCLR}}$ (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow ($\overline{\text{PWRT}}$, OST), $\overline{\text{MCLR}}$ (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow ($\overline{\text{PWRT}}$, OST), $\overline{\text{MCLR}}$ (optional), WDT
Programmable Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled
Packages	28-pin PDIP 28-pin SOIC	28-pin PDIP 28-pin SOIC	40-pin PDIP 44-pin QFN 44-pin TQFP	40-pin PDIP 44-pin QFN 44-pin TQFP

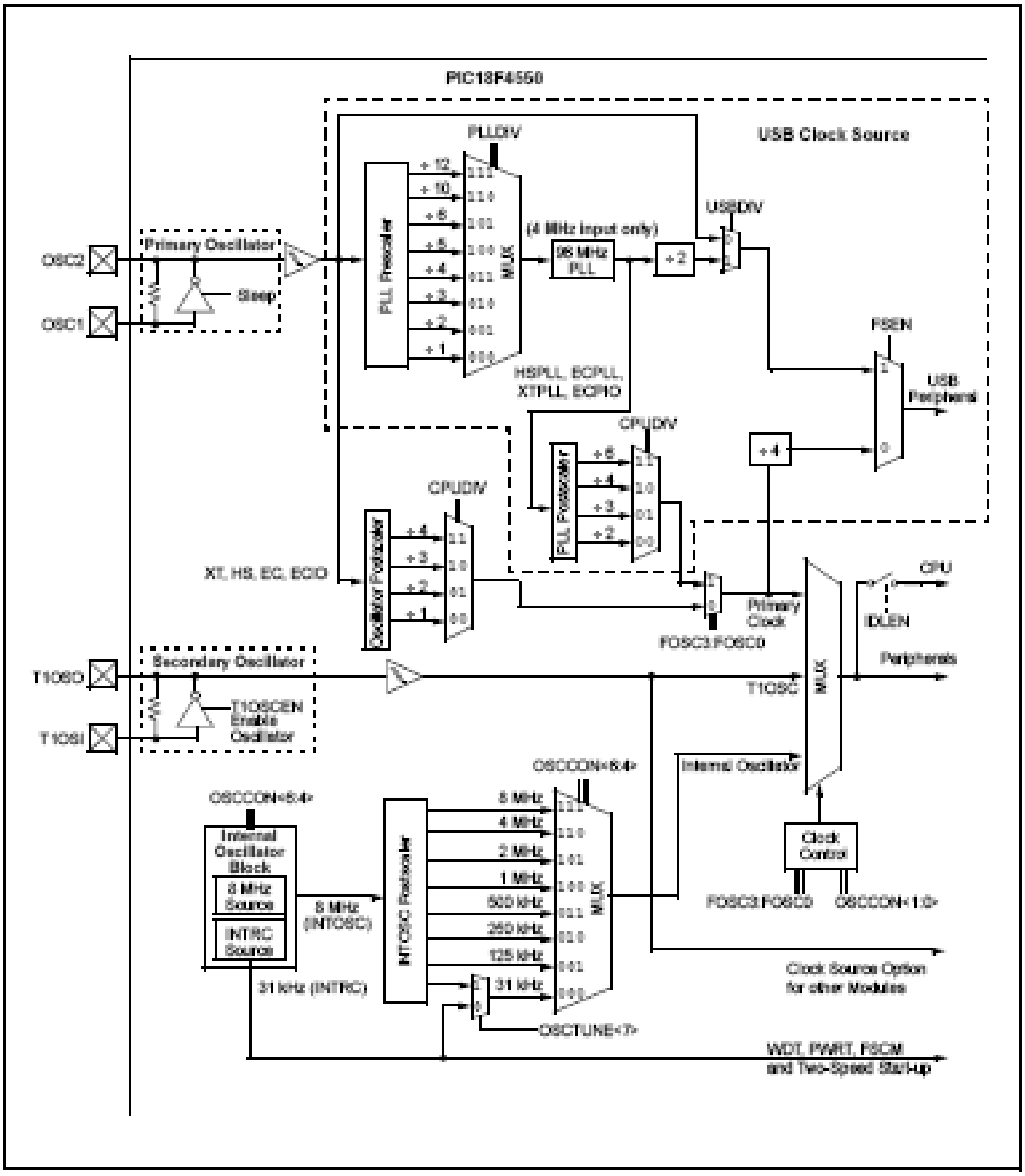
TABLE 1-2: PIC18F2455/2550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	PDIP, SOIC			
				PORTA is a bidirectional I/O port.
RA0/AN0	2			
RA0		I/O	TTL	Digital I/O.
AN0		I	Analog	Analog input 0.
RA1/AN1	3			
RA1		I/O	TTL	Digital I/O.
AN1		I	Analog	Analog input 1.
RA2/AN2/VREF-/CVREF	4			
RA2		I/O	TTL	Digital I/O.
AN2		I	Analog	Analog input 2.
VREF-		I	Analog	A/D reference voltage (low) input.
CVREF		O	Analog	Analog comparator reference output.
RA3/AN3/VREF+	5			
RA3		I/O	TTL	Digital I/O.
AN3		I	Analog	Analog input 3.
VREF+		I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/C1OUT/RCV	6			
RA4		I/O	ST	Digital I/O.
T0CKI		I	ST	Timer0 external clock input.
C1OUT		O	—	Comparator 1 output.
RCV		I	TTL	External USB transceiver RCV input.
RA5/AN4/$\overline{\text{SS}}$/HLVDIN/C2OUT	7			
RA5		I/O	TTL	Digital I/O.
AN4		I	Analog	Analog input 4.
$\overline{\text{SS}}$		I	TTL	SPI™ slave select input.
HLVDIN		I	Analog	High/Low-Voltage Detect input.
C2OUT		O	—	Comparator 2 output.
RA6	—	—	—	See the OSC2/CLKO/RA6 pin.

Legend:
TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
O = Output
CMOS = CMOS compatible input or output
I = Input
P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX configuration bit is cleared.
2: Default assignment for CCP2 when CCP2MX configuration bit is set.

FIGURE 2-1: PIC18F2455/2550/4455/4550 CLOCK DIAGRAM



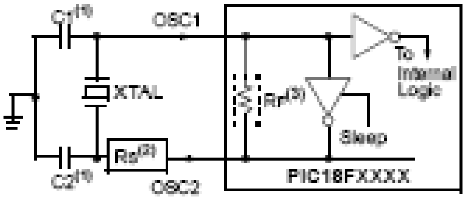
2.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In HS, HSPLL, XT and XTPLL Oscillator modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation. Figure 2-2 shows the pin connections.

The oscillator design requires the use of a parallel cut crystal.

Note: Use of a series cut crystal may give a frequency out of the crystal manufacturer's specifications.

FIGURE 2-2: CRYSTAL/CERAMIC RESONATOR OPERATION (XT, HS OR HSPLL CONFIGURATION)



Note 1: See Table 2-1 and Table 2-2 for initial values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.
3: RF varies with the oscillator mode chosen.

TABLE 2-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Typical Capacitor Values Used:			
Mode	**Freq**	**OSC1**	**OSC2**
XT	4.0 MHz	33 pF	33 pF
HS	8.0 MHz 16.0 MHz	27 pF 22 pF	27 pF 22 pF

Capacitor values are for design guidance only.

These capacitors were tested with the resonators listed below for basic start-up and operation. **These values are not optimized.**

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.

See the notes following Table 2-2 for additional information.

Resonators Used:
4.0 MHz
8.0 MHz
16.0 MHz

TABLE 2-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Crystal Freq	Typical Capacitor Values Tested:	
		C1	C2
XT	4 MHz	27 pF	27 pF
HS	4 MHz	27 pF	27 pF
	8 MHz	22 pF	22 pF
	20 MHz	15 pF	15 pF

Capacitor values are for design guidance only.

These capacitors were tested with the crystals listed below for basic start-up and operation. **These values are not optimized.**

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.

See the notes following this table for additional information.

Crystals Used:
4 MHz
8 MHz
20 MHz

Note 1: Higher capacitance increases the stability of oscillator but also increases the start-up time.

2: When operating below 3V VDD, or when using certain ceramic resonators at any voltage, it may be necessary to use the HS mode or switch to a crystal oscillator.

3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.

4: Rs may be required to avoid overdriving crystals with low drive level specification.

5: Always verify oscillator performance over the VDD and temperature range that is expected for the application.

An internal postscaler allows users to select a clock frequency other than that of the crystal or resonator. Frequency division is determined by the CPUDIV configuration bits. Users may select a clock frequency of the oscillator frequency, or 1/2, 1/3 or 1/4 of the frequency.

An external clock may also be used when the microcontroller is in HS Oscillator mode. In this case, the OSC2/CLKO pin is left open (Figure 2-3).

3.5.4 EXIT WITHOUT AN OSCILLATOR START-UP DELAY

Certain exits from power-managed modes do not invoke the OST at all. There are two cases:

- PRI_IDLE mode where the primary clock source is not stopped; and
- the primary clock source is not any of the XT or HS modes.

In these instances, the primary clock source either does not require an oscillator start-up delay, since it is already running (PRI_IDLE), or normally does not require an oscillator start-up delay (EC and any internal oscillator modes). However, a fixed delay of interval TCSD following the wake event is still required when leaving Sleep and Idle modes to allow the CPU to prepare for execution. Instruction execution resumes on the first clock cycle following this delay.

TABLE 3-2: EXIT DELAY ON WAKE-UP BY RESET FROM SLEEP MODE OR ANY IDLE MODE (BY CLOCK SOURCES)

Microcontroller Clock Source		Exit Delay	Clock Ready Status Bit (OSCCON)
Before Wake-up	**After Wake-up**		
Primary Device Clock (PRI_IDLE mode)	XT, HS	None	OSTS
	XTPLL, HSPLL		
	EC		
	INTOSC(3)		IOFS
T1OSC or INTRC(1)	XT, HS	TOST(4)	OSTS
	XTPLL, HSPLL	TOST + t_{rc}(4)	
	EC	TCSD(2)	
	INTOSC(2)	TIOBST(5)	IOFS
INTOSC(3)	XT, HS	TOST(5)	OSTS
	XTPLL, HSPLL	TOST + t_{rc}(4)	
	EC	TCSD(2)	
	INTOSC(2)	None	IOFS
None (Sleep mode)	XT, HS	TOST(4)	OSTS
	XTPLL, HSPLL	TOST + t_{rc}(4)	
	EC	TCSD(2)	
	INTOSC(2)	TIOBST(5)	IOFS

Note 1: In this instance, refers specifically to the 31 kHz INTRC clock source.

2: TCSD (parameter 38, Table 28-12) is a required delay when waking from Sleep and all Idle modes and runs concurrently with any other required delays (see **Section 3.4 "Idle Modes"**).

3: Includes both the INTOSC 8 MHz source and postscaler derived frequencies.

4: TOST is the Oscillator Start-up Timer period (parameter 32, Table 28-12). t_{rc} is the PLL lock time-out (parameter F12, Table 28-9); it is also designated as TPLL.

5: Execution continues during TIOBST (parameter 39, Table 28-12), the INTOSC stabilization period.