DEVELOPMENT OF MICROHYDRO GENERATOR SYSTEM

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JUDUL: **DEVELOPMENT OF MICROHYDRO GENERATOR SYSTEM**

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Faculty of Electrical & Electronics Engineering
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NOVEMBER, 2010

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Date : 30 NOVEMBER 2010

Specially dedicated to my beloved family

To My beloved Mother and Dad

And those people who have guided and inspired me throughout my journey of education

Thanks for everything...

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ABSTRACT

The chief sources of energy used for the generation of electrical energy are water, fuels and nuclear energy. Micro-Hydro Generator Systems (MHGS) converts potential energy of water into electricity. It is a clean source of energy. Hydro electric power plants generate from few kW to thousands of MW. It can be classified as Micro Hydro power system for the generating capacity less than 100kW. Micro hydro can provide alternative renewable energy sources especially in areas with small rivers or stream flowing. Other renewable energy source, such as solar and wind, can be used to produce electrical power. The choice of energy source depends on several factors, including availability, economic and energy and power requirements. Micro hydro power is almost always more cost-effective than any other form of renewable power. Micro hydro designates projects with power output of less than 500W. This project is also using a Programmable Interface Controller (PIC) and power electronic components in designing hardware. In the end of the project, the proposed micro hydro-generator work properly as designed and produce output power as high as 500W or more and can be used for lighting, bulk, and battery charge and electronics devices.

ABSTRAK

Sumber utama tenaga yang digunakan untuk penjanaan tenaga elektrik adalah air, bahan api dan tenaga nuklear. Sistem penjanaan kuasa mikro hidro adalah sistem menukar tenaga keupayaan air kepada tenaga elektrik. Ini merupakan sumber tenaga bersih. Tenaga penjanaan air elektrik menghasilkan dari beberapa kW ribuan kepada MW. Hal ini boleh diklasifikasikan sebagai sistem tenaga elektrik Mikro hidro untuk kapasiti menghasilkan kurang dari 100kW. Mikro hidro dapat menyediakan sumber tenaga alternatif terbaru terutama di daerah-daerah dengan air sungai kecil atau air sungai yang mengalir. Selain itu, sumber tenaga yang boleh diperbaharui ialah seperti solar dan angin, boleh digunakan untuk menghasilkan tenaga elektrik. Pemilihan sumber tenaga bergantung pada beberapa faktor, termasuk yang sedia ada, ekonomi dan tenaga dan keperluan kuasa. Kuasa Mikro hidro hampir selalu lebih jimat berbanding daripada bentuk lain dari tenaga yang boleh diperbaharui. Projek Mikro hidro ini direkabentuk supaya dapat menghasilkan kuasa lebih kurang dari 500W. Projek ini juga menggunakan komponen (PIC) pengawal mikro dan skematik elektronik dalam perancangan. Pada akhir projek, dicadangkan sistem penjana mikro-hidro dapat bekerja dengan baik seperti yang dirancang dan menghasilkan kuasa keluaran setinggi 500W atau lebih dan boleh digunakan untuk pencahayaan, lampu rumah, dan pengecas bateri dan barangan elektronik.

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D,d	-	Diameter
AC	-	Alternating Current
DC	-	Direct Current
A	-	Ampere
V	-	Volt
W	-	Watt
Pth	-	Theoretical water power output in W
Q	-	Usable flow rate in m^3/s
H	-	Gross head in m
G	-	Gravitational constant (9.8 m/s^2)
m	-	meter
mm	-	millimeter
sq	-	square
km	-	kilometer
VDC	-	Voltage Direct Current
ADC	-	Voltage Alternate Current
Hz	-	Hertz

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1 Project Background

Micro-Hydro Generator Systems (MHGS) convert the energy of moving water into electricity. Generator systems convert from mechanical to electrical energy. This project is to develop a Micro-Hydro generator system using battery based system to generate power. The battery based system that we will use is Lead-acid deep cycle batteries. This battery can be charge and discharge system. The prime mover of this project is water that means source of water pressure from a present water tank, pipes and to turn a turbine then the turbine spins an alternator and electricity is produces to charge the battery. Then an alternator converts the mechanical energy from the turbine into electrical energy. Many other components may be in a system, but it all begins with the energy already within the moving water. Other renewable energy source, such as solar and wind, can be used to produce electrical power. The choice of energy source depends

on several factors, including availability, economic and energy and power requirements. Micro hydro power is almost always more cost-effective than any other form of renewable power. Micro hydro designates projects with power output of less than 100 kW. This project is also using a Programmable Interface Controller (PIC) and power electronic components in designing hardware. In the end of the project, the proposed micro hydro-generator will work properly as designed and will produce output power as high as 1kW or more and can be used for lighting, bulk, and battery charger and electronics devices.

1.2 Problem Statements

Hydro generator system in market is huge and high cost and no micro hydro generator in the market.

1.3 Objectives of Project

The objectives of this project are:

i. To produce electricity using renewable source of energy.
ii. To implement the use of Programmable Intelligent Circuit (PIC) and Power Electronics switch in designing hardware.
iii. To provide clean, environmentally friendly electricity in rural communities.

1.4 Scope of project

The scope of this project is:

i. To develop of Micro-Hydro Generator System using automotive alternator.
ii. Using PIC 16F877 microcontroller as a control circuit.
iii. Produce output power at least 500W

1.5 Literature Review

Micro hydro power was once the world's prominent source of mechanical power for manufacturing. Micro hydro is making a comeback for electricity generation in homes. This system of the Micro hydro can be divide by two is Battery base systems and AC- Direct System.[1].

The battery base system is power can be supplied by a micro hydro system in two ways. In a battery-based system, power is generated at a level equal to the average demand and stored in batteries. Batteries can supply power as needed at levels much higher than that generated and during times of low demand the excess can be stored. If enough energy is available from the water, an AC-direct system can generate power as alternating current (AC). This system typically requires a much higher power level than the battery-based system. The input voltage to the batteries in a battery-based system commonly ranges from 12 to 48 Volts DC. If the transmission distance is not great then 12 Volts is often high enough. A 24 Volt system is used if the power level or transmission distance is greater. If all of the loads are inverter-powered the battery voltage is independent of the inverter output voltage and voltages of 48 or 120 may be used to overcome long transmission distances. Although batteries and inverters can be

specified for these voltages, it is common to convert the high voltage back down to 12 or 24 Volts (battery voltage) using transformers or solid state converters.[1]

Most battery-based systems use an automotive alternator. If selected carefully, and rewound when appropriate, the alternator can achieve very good performance. A rheostat can be installed in the field circuit to maximize the output. Rewound alternators can be used even in the 100–200 Volt range.[1]

Micro hydro power is best where water supply is continuously available. Where supply is seasonal it may still be cost effective to install micro hydro as a stand-alone system. This will depend on whether the cost of installing the system is offset by the savings made during the period when the creek is flowing. Another renewable system, or a generator, will be required when water is not available.[2]

1.6 Thesis Outline

This report contains 5 chapters which is every chapter have its own purpose. After viewing the entire chapter in this report, hopefully the viewer can understand the whole system design for this project.

Chapter 1 describe on the background of the project, problem statement, objectives, scope of the project and the literature review that referred to in the development of micro hydro generator system.

Chapter 2 is focused to the theory of the Micro Hydro Generator System (MHGS) where it described about operation of MHGS and measuring of head, flow and potential power. This chapter also include why we need to use MHGS.

Chapter 3 elaborated more on the method of micro hydro generator system. Besides it also describe the functions of each components used in the system and operation such as alternator, battery, charger controller, inverter and ballast load.

Chapter 4 present about result and discussion while in development process. The result of this project is also accompanied by the discussion for each problem statement.

Lastly in Chapter 5, in this chapter the conclusion has been made for the project from the whole aspect and there are also suggestions to improve the micro hydro generator system in the future, in case for the commercialization.

CHAPTER 2

MICRO-HYDRO GENERATOR SYSTEM (MHGS)

2.1 Introduction

This chapter explains about a theory of Micro Hydro Generator System (MHGS) included operation of MHGS, measuring of head, flow rate and potential power produces so that the reader will get a clear idea how the MHGS is working. To achieve that first we need to study more about MHGS and doing more research about the MHGS operation. This chapter also includes overview of Micro Hydropower potential in Malaysia.

2.2 Operation of MHGS

A Micro Hydro Generator System (MHGS) convert the energy of moving water into electricity. Instead, a portion of a stream or river is temporarily diverted into a pipe system and to the micro-hydro turbine and generator. It is then returned to its source. Because of this these types of system have far less impact on the environment than large scale hydro schemes. Micro hydro generator systems use the force of running water to turn turbine blades, which spin a shaft connected to a generator. These systems are best suited to rural sites, and can be set up wherever water falls from a higher lever to a lower level, such as a waterfall, hillside, stream, or where a reservoir discharges into a river. The type of turbine required will depend on the ‘head' (the vertical fall) and the flow rate of the water. There are two basic of turbines such as impulse and reaction. These turbines are more details explanation in Chapter 3.

2.2.1 Measuring of Head

Generally, the distance the water falls depends on the steepness of the terrain the water is moving across, or the height of a dam the water is stored behind. The farther the water falls, the more power it has. In fact, the power of falling water is ‘directly proportional’ to the distance it falls. In other words, water falling twice as far has twice as much as energy. It is important to note we are only talking about the vertical distance the water falls. The distance the water travels horizontally is consequential only in expense of the system and friction losses. Head is usually measured in ‘feet’.

2.2.2 Measuring of Flow Rate

More water falling through the turbine will produce more power. The amount of water available depends on the volume of water at the source. Power is also ‘directly proportional’ to river flow, or flow volume. A river with twice the amount of flowing water as another river can produce twice as much energy. This is also effect of choice a size of pipelines. Flow volume is usually measured in ‘gallons per minute’, or ‘GPM’.

2.2.3 Measuring of Potential Power

The amount of power available from a micro hydro generator system is directly related to the flow rate, head and the force of gravity. Once we have determined the usable flow rate (the amount of flow we can divert for power generation) and the available head for our particular site, we can calculate the amount of electrical power we can expect to generate. This is calculated using the following equation:

Pth = Q x H x **g**
Pth = Theoretical power output in kW
Q = Usable flow rate in m3/s
H = Gross head in m
g = Gravitational constant (9.8 m/s2)

2.3 Overview of Micro Hydropower Potential in Malaysia

Malaysia comprises of two distinct region which are West Malaysia covering Peninsula Malaysia and East Malaysia covering North Borneo. In total, both regions cover land area of 330 000 sq. km in which 58% is lowland areas and 42% is highland areas [ ]. The highland areas in Malaysia are created by numbers of well known ranges. In Peninsula Malaysia, the highland areas are created by ranges such as Titiwangsa, Tahan, Bintang, Kledang, and Pantai Timur. Barisan Titiwangsa range is the main range which is considered as the backbone of Peninsula. In Sarawak, the highland areas were created mainly by Tama Abu, Iran and Kapuas Hulu ranges. In Sabah the highland areas were created by Crocker, Maitland and Brassey. With average rainfall of 2540 mm in Peninsula, 2630 mm in Sabah and 3850 mm in Sarawak, Malaysia bless with abundant streams and rivers flowing from the highland areas created by these ranges [ ]. Combinations of highland area with huge river networks promise Malaysia with a lot of micro hydropower potential. Figure 2.3 shows the map of Peninsular Malaysia.

Figure 2.3 Map of Peninsular Malaysia

2.4 Advantages of MHGS

The advantages of MHGS is efficient energy, meaning that it only takes a small amount of flow or a drop as low as two feet to generate electricity with micro hydro. Electricity can be delivered as far as a mile away to the location where it is being used. Secondly, reliable electricity source, meaning that hydro produce a continuous supply of electrical energy in comparison to other small-scale renewable technologies. Lastly, the advantage of MHGS is no reservoir required, meaning that the water passing through the generator is directed back into the stream with relatively little impact on the surrounding ecology.

2.5 Disadvantages of MHGS

The disadvantages of MHGS is suitable site characteristic required, meaning that factor to consider are distance from the power source to the location where energy is required, stream size and balance system component like inverter, batteries and controller. Second disadvantage is energy expansion not possible, meaning that the size and flow of small streams may restrict future site expansion as the power demand increases. Lastly, environmental impact, meaning that the ecological impact of small-scale hydro is minimal, however the low-level environment effect must be taken into consideration before construction begins.

2.5 Summary

From this Chapter 2, we can see that before we develop the Micro Hydro Generator System (MHGS), we must know to measure of head and flow rate. That is important to calculate output power of the system. Besides that, we also know for the long term, why we need to use MHGS this is because it can be more economical and also may be that we are interested in helping to protect the environment. In this chapter also explain about advantages and disadvantages of using MHGS.

CHAPTER 3

DEVELOPMENT OF MICRO HYDRO GENERATOR SYSTEM (MHGS)

3.1 Introduction

This chapter explains about how to develop of Micro Hydro Generator System with used battery based system. This chapter also will include project flow, flow chart, block diagram to develop Micro Hydro Generator system used battery based system. It also will cover about based component of MHGS, hardware and software implementation.

3.2 Hardware Development

This project

3.2.1 Mechanical System Design

3.2.2 Electrical System Design

3.3 Basic Components of MHGS

This project is using battery based system so basic components to develop of micro hydro generator system is turbine, alternator, battery, charger controller and inverter.

3.3.1 Alternator

Alternator which has a built in rectifier to convert the generated AC signal to a DC signal**.** The specified turbines which convert mechanical energy into electrical energy use an alternator that outputs a DC signal**.** The DC signal is then sent to the battery where, along with the batteries a monitor will be needed this way you can determine how much electricity the turbine is generating, the consumption of that energy and battery capacity. Based on figure 3.3

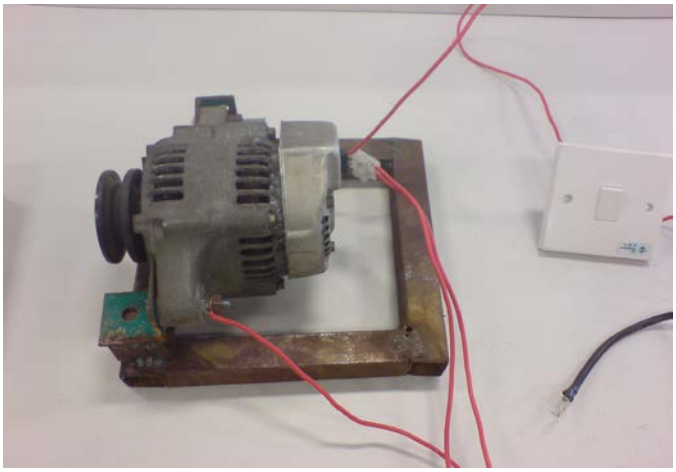


Figure 3.3 Automotive Alternator

3.3.2 Battery

Deep cycle batteries are best to use for any renewable energy system. Batteries Lead-acid deep cycle batteries are usually used in hydro system. Deep cycle batteries are designed to withstand repeated charge and discharge cycles. The amount of batteries you use in your Micro-Hydro system will depend on your needs. The input voltage to the batteries in a battery based system commonly ranges from 12 to 48 Volts DC View our battery section to see how to calculate your needs.

3.3.3 Charge Controller

A charge controller is connected with the battery operation to prevent overcharging of the batteries. In the event of a power outage excess electricity could be produced and the charge controller would absorb the excess energy to protect the batteries. Hydro systems with lead-acid batteries require protection from overcharge and over-discharge.

3.3.4 Inverter

A battery bank does not enable users to live with all the conveniences of modern living, as most appliances use high voltage AC (alternating current) while batteries can supply only DC (direct current). Inverters are used to convert DC to AC so that stored battery power may be used as needed by appliances and other loads. Modern inverters are available in virtually any wattage capacity, in recreational and commercial grades, in a variety of DC voltages, and with the220-240VAC, 50 Hz output for the rest of the world and 120VAC 60 Hz output for North American applications.

3.3.5 Ballast Load

A ballast load takes the excess energy produced that is no longer needed to keep the batteries charged, and diverts it to a waste load. Most of the time, we will find dump loads consisting of water heater elements or air heaters. A ballast load is a very important component to the system.

3.3.6 Turbines

Turbines are commonly used today to power micro generator system. The moving water strikes the turbine blades, much like a waterwheel, to spin a shaft. But turbines are more compact in relation to their energy output than waterwheels. There also have fewer gears and require less material for construction. Low head, low flow turbines may be difficult to find, and may have to be custom-made. There are two general types of turbines like impulse and reaction.

3.3.6.1 Impulse Turbine

Impulse turbines, which have the least complex design, are most commonly used for high-head micro hydro system. The most common types of impulse turbines include the Pelton wheel and the Turgo wheel. That mean, the Pelton wheel uses the concept of jet to create energy. Pelton wheel turbines are also available in various sizes and operate best under low-flow and high-head condition. Another impulse turbine is Turgo impulse wheel is an upgraded version of the Pelton. The size of Turgo is half the size of the Pelton. Turgo wheel moves twice as fast. It is also needs few or no gears and good reputation for trouble-free operation. The Turgo can operate under low flow condition but requires a medium or high head.

3.3.6.2 Reaction Turbine

Reaction turbines, which are highly efficient, depend on pressure rather than velocity to produce energy. All blades of the reaction turbine maintain constant contact with the water. These turbines are often used in large-scale hydropower sites. Because of their complexity and high cost, reaction turbines aren't usually used for micro hydropower projects. An exception is the propeller turbine, which comes in many different designs and works much like a boat's propeller. Propeller turbines have three to six usually fixed blades set at different angles aligned on the runner. The bulb, tubular, and Kaplan tubular are variations of the propeller turbine. The Kaplan turbine, which is a highly adaptable propeller system, can be used for micro hydro sites.

3.4 Software Implementation

3.4.1 MicroCode Studio (PBP) Compiler

3.4.2 UP00B PIC USB Programmer

3.4.3 Programming the PIC 16F877 Microcontroller

3.5 Summary

The concept and method development of MHGS have been described in this chapter. Flow chart is very important before start the project. All the components of this

project must check specification and test. In Chapter 4 present more detail about result and discussion.

CHAPTER 4

RESULT AND DISCUSSION

4.1 Introduction

This chapter explains about result and discussion for test automotive alternator with AC motor. This chapter also will discuss about data collection by using Tachometer for measure speed of motor and digital multimeter for measure voltage at alternator.

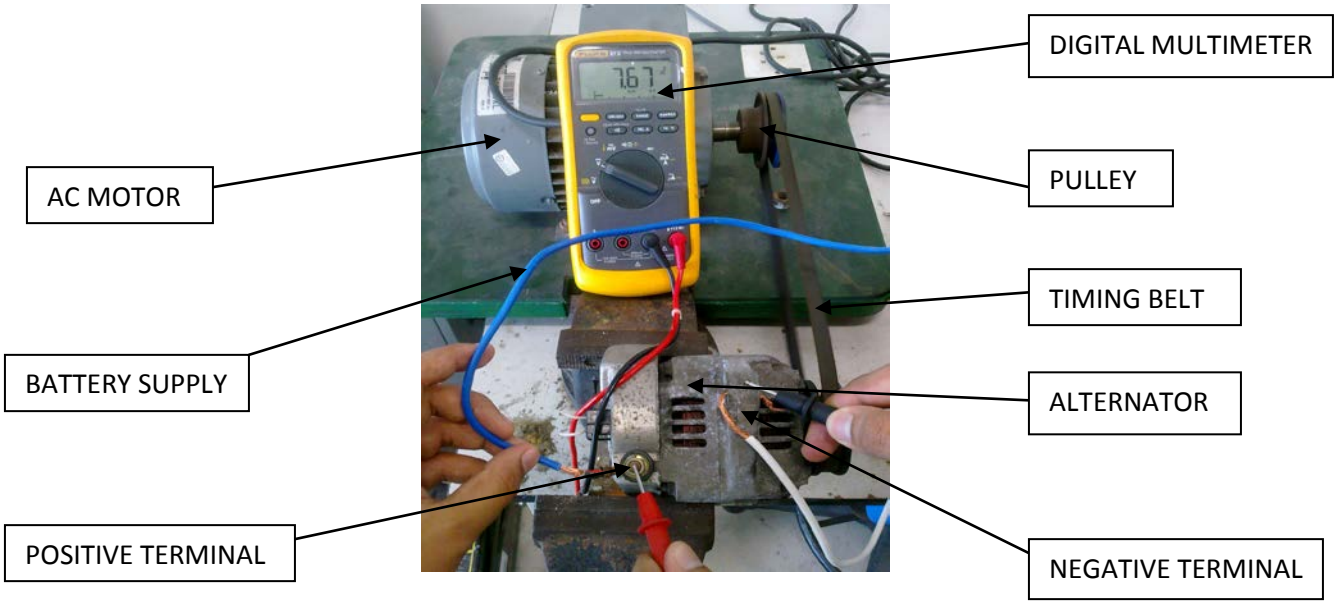
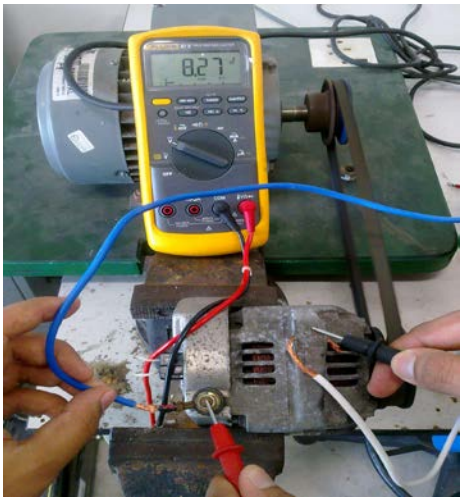


Figure 3: Testing Alternator using AC motor

4.2 Alternator Output

Based on Figure 3 (a), (b), (c), (d) alternator used is automotive alternator with specification speed is 1800 rpm, voltage is 14.0 VDC and current is 45A. The specification of AC motor is 1380 rpm and connected inverter to control their speed. We also used timing belt to joined alternator and AC motor.

Figure 3 (a)



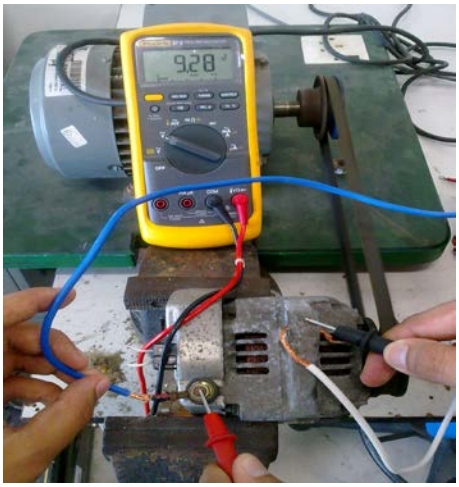


Figure 3 (b)

Figure 3 (c)

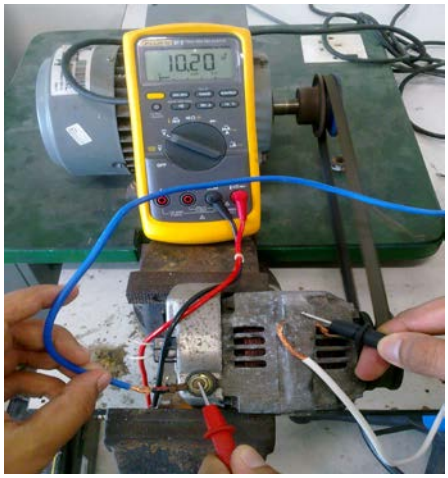


Figure 3 (d)

Figure 4: Inverter control speed

Figure 5: Tachometer measured speed motor (RPM)

Figure 6: Battery lead acid

Table 1: Data Collection

FREQUENCY (Hz)	SPEED (RPM)	VOLTAGE DC (V)
20	500	1.4
30	1036	4.3
40	1399	7.75
50	1679	10.35

Based on the Table 1 is data collection using alternator and AC motor. We control the frequency of using inverter ADLEEPOWER. It is also control the speed AC motor. We also used Tachometer to measure speed of alternator and digital Multimeter to measure voltage at alternator. We see on the table, we know that when speed increase, voltage of alternator also increase. We can't get 14 V because we used AC Motor that speed RPM of AC motor is 1380 RPM. We refer the specification of Alternator to produce 14 V, the speed of alternator must 1800 RPM. So the speed of alternator is effect of Voltage. We also know that the voltage alternator must be higher than voltage of battery for charge the battery.

4.3 Charge Controller Circuit

4.4 Liquid Crystal Display (LCD) Circuit

4.5 Project Results

4.6 Summary

The preminalary result and discussion of data collection of alternator concept have been described in this chapter. The most important thing is to make sure that alternator can be function to charge the battery. The next Chapter is

CHAPTER 5

CONCLUSION

5.1 Introduction

As a conclusion, the system is not difficult to operate and maintain. This project is almost always more cost-effective than any other form of renewable power. The proposed Micro- Hydro Generator System (MHGS) will work properly as designed and will produce output power as high as 1kW or more and can be used for lighting, bulk, and battery charge and electronics devices. Another thing, the advantage of using Micro hydro system is to protect the environment and also non polluting energy source that has provided reliable power in the past and is one of the most promising renewable energy sources for the future. Lastly, for long term this project, in case for the commercialization especially in Malaysia.

5.2 Future Development

5.3 Costing and Commercialization

5.3.1 Costing

5.3.2 Commercialization

5.4 Conclusion

CHAPTER 1

INTRODUCTION

1.1 Project Background

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electronic components in designing hardware. In the end of the project, the proposed micro hydro-generator can work properly as designed and produce output power as high as 500W or more and can be used for lighting, bulk, and battery charger and electronics devices.

1.2 Problem Statements

Hydro generator system in market is huge and high cost and no micro hydro generator in the market. The problem also is less use of renewable energy source that convenient to supply for load. Difficulty to get data, meaning that lot of data have to be assumed because of there is no real site to survey, to make the calculations on site and to collect all the data needed and any more.

1.3 Objectives of Project

The objectives of this project are:

i. To produce electricity using renewable source of energy.
ii. To implement the use of Programmable Intelligent Circuit (PIC) and Power Electronics switch in designing hardware.
iii. To provide clean, environmentally friendly electricity in rural communities.

1.4 Scope of project

The scope of this project is:

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1.5 Literature Review

Micro hydro power was once the world's prominent source of mechanical power for manufacturing. Micro hydro is making a comeback for electricity generation in homes. This system of the Micro hydro can be divide by two is Battery base systems and AC- Direct System [1].

The battery base system is power can be supplied by a micro hydro system in two ways. In a battery-based system, power is generated at a level equal to the average demand and stored in batteries. Batteries can supply power as needed at levels much higher than that generated and during times of low demand the excess can be stored. If enough energy is available from the water, an AC-direct system can generate power as alternating current (AC). This system typically requires a much higher power level than the battery-based system. The input voltage to the batteries in a battery-based system commonly ranges from 12 to 48 Volts DC. If the transmission distance is not great then 12 Volts is often high enough. A 24 Volt system is used if the power level or transmission distance is greater. If all of the loads are inverter-powered the battery voltage is independent of the inverter output voltage and voltages of 48 or 120 may be used to overcome long transmission distances. Although batteries and inverters can be

specified for these voltages, it is common to convert the high voltage back down to 12 or 24 Volts (battery voltage) using transformers or solid state converters.[1]

Most battery-based systems use an automotive alternator. If selected carefully, and rewound when appropriate, the alternator can achieve very good performance. A rheostat can be installed in the field circuit to maximize the output. Rewound alternators can be used even in the 100–200 Volt range.[1]

Micro hydro power is best where water supply is continuously available. Where supply is seasonal it may still be cost effective to install micro hydro as a stand-alone system. This will depend on whether the cost of installing the system is offset by the savings made during the period when the creek is flowing. Another renewable system, or a generator, will be required when water is not available.[2]

1.6 Thesis Outline

This report contains 5 chapters which is every chapter have its own purpose. After viewing the entire chapter in this report, hopefully the viewer can understand the whole system design for this project.

Chapter 1 describe on the background of the project, problem statement, objectives, scope of the project and the literature review that referred to in the development of Microhydro Generator System (MHGS).

Chapter 2 is focused to the theory of the Microhydro Generator System (MHGS) where it described about operation of MHGS and measuring of head, flow and potential

power. In this chapter also include about theory overview of Micro hydropower potential in Malaysia. Lastly, this chapter also includes advantages and disadvantages of MHGS.

Chapter 3 elaborated more on the method of micro hydro generator system. Besides it also describe the hardware development that divide by two design which is mechanical system design and electrical system design. This chapter also include the functions of each components used in the system and operation such as alternator, battery, charger controller, inverter, load and turbine.

Chapter 4 presents the data and experimental about result and discussion while in development process. The results of this project are also accompanied by the discussion for each problems statement and reflect to the objective of this project.

Lastly in Chapter 5, in this chapter the conclusion has been made for the project from the whole aspect and there are also suggestions to improve the micro hydro generator system in the future, in case for the costing and commercialization.

CHAPTER 2

MICRO-HYDRO GENERATOR SYSTEM (MHGS)

2.1 Introduction

This chapter explains about a theory of Micro Hydro Generator System (MHGS) included operation of MHGS, measuring of head, flow rate and potential power produces so that the reader will get a clear idea how the MHGS is working. To achieve that first we need to study more about MHGS and doing more research about the MHGS operation. This chapter also includes overview of Micro Hydropower potential in Malaysia.

2.2 Operation of MHGS

A Micro Hydro Generator System (MHGS) convert the energy of moving water into electricity. Instead, a portion of a stream or river is temporarily diverted into a pipe system and to the micro hydro turbine and generator. It is then returned to its source.

Because of this these types of system have far less impact on the environment than large scale hydro schemes. Micro hydro generator systems use the force of running water to turn turbine blades, which spin a shaft connected to a generator. These systems are best suited to rural sites, and can be set up wherever water falls from a higher lever to a lower level, such as a waterfall, hillside, stream, or where a reservoir discharges into a river. The type of turbine required will depend on the ‘head' (the vertical fall) and the flow rate of the water. There are two basic of turbines such as impulse and reaction. These turbines are more details explanation in Chapter 3.

2.2.1 Measuring of Head

Generally, the distance the water falls depends on the steepness of the terrain the water is moving across, or the height of a dam the water is stored behind. The farther the water falls, the more power it has. In fact, the power of falling water is ‘directly proportional’ to the distance it falls. In other words, water falling twice as far has twice as much as energy. It is important to note we are only talking about the vertical distance the water falls. The distance the water travels horizontally is consequential only in expense of the system and friction losses. Head is usually measured in ‘feet’.

2.2.2 Measuring of Flow Rate

More water falling through the turbine will produce more power. The amount of water available depends on the volume of water at the source. Power is also ‘directly proportional’ to river flow, or flow volume. A river with twice the amount of flowing

water as another river can produce twice as much energy. This is also effect of choice a size of pipelines. Flow volume is usually measured in ‘gallons per minute’, or ‘GPM’.

2.2.3 Measuring of Potential Power

The amount of power available from a micro hydro generator system is directly related to the flow rate, head and the force of gravity. Once we have determined the usable flow rate (the amount of flow we can divert for power generation) and the available head for our particular site, we can calculate the amount of electrical power we can expect to generate. This is calculated using the following equation [2]:

Pth = Q x H x **g**
Pth = Theoretical water power output in W
Q = Usable flow rate in m^3/s
H = Gross head in m
g = Gravitational constant (9.8 m/s^2)

2.3 Overview of Micro Hydropower Potential in Malaysia

Malaysia comprises of two distinct regions which are West Malaysia covering Peninsula Malaysia and East Malaysia covering North Borneo. In total, both regions cover land area of 330 000 sq. km in which 58% is lowland areas and 42% is highland areas [5]. The highland areas in Malaysia are created by numbers of well known ranges. In Peninsula Malaysia, the highland areas are created by ranges such as Titiwangsa,

Tahan, Bintang, Kledang, and Pantai Timur. Barisan Titiwangsa range is the main range which is considered as the backbone of Peninsula. In Sarawak, the highland areas were created mainly by Tama Abu, Iran and Kapuas Hulu ranges. In Sabah the highland areas were created by Crocker, Maitland and Brassey. With average rainfall of 2540 mm in Peninsula, 2630 mm in Sabah and 3850 mm in Sarawak, Malaysia bless with abundant streams and rivers flowing from the highland areas created by these ranges [6]. Combinations of highland area with huge river networks promise Malaysia with a lot of micro hydropower potential. Figure 2.3 shows the map of Peninsular Malaysia.

Figure 2.3 Map of Peninsular Malaysia

2.4 Advantages of MHGS

The advantages of MHGS is efficient energy, meaning that it only takes a small amount of flow or a drop as low as two feet to generate electricity with micro hydro. Electricity can be delivered as far as a mile away to the location where it is being used. Secondly, reliable electricity source, meaning that hydro produce a continuous supply of electrical energy in comparison to other small-scale renewable technologies. Lastly, the advantage of MHGS is no reservoir required, meaning that the water passing through the generator is directed back into the stream with relatively little impact on the surrounding ecology.

2.5 Disadvantages of MHGS

The disadvantages of MHGS is suitable site characteristic required, meaning that factor to consider are distance from the power source to the location where energy is required, stream size and balance system component like inverter, batteries and controller. Second disadvantage is energy expansion not possible, meaning that the size and flow of small streams may restrict future site expansion as the power demand increases. Lastly, environmental impact, meaning that the ecological impact of small-scale hydro is minimal, however the low-level environment effect must be taken into consideration before construction begins.

2.5 Summary

From this Chapter 2, we can see that before we develop the Micro Hydro Generator System (MHGS), we must know to measure of head and flow rate include the pipes. That is important to calculate output power of the system. Besides that, we also know overview of micro hydropower potential in Malaysia that means suitable to install of micro hydropower depend on land area. In this chapter also explain about advantages and disadvantages of using MHGS.

CHAPTER 3

DEVELOPMENT OF MICROHYDRO GENERATOR SYSTEM (MHGS)

3.1 Introduction

This chapter explains about how to develop of Micro Hydro Generator System. This chapter also will include hardware development system which is this system can divide by two design to develop Microhydro Generator system used battery based system. It also will cover about basic component of MHGS such as alternator, battery, charge controller, power inverter, ballast load and turbine. The hardware and software implementation also include about MicroCode Studio (PBP) Compiler, UP00B PIC USB Programmer device.

3.2 Hardware Development

The main project development of Microhydro Generator System (MHGS) is hardware development. The hardware developments are included the mechanical system design and electrical system design.

3.2.1 Mechanical System Design

From this mechanical System design, Figure 3.1 shows that block diagram of Microhydro Generator System (MHGS). This system is included the prime mover as renewable source of energy is water. This project is used impeller turbine. The turbine and generator is connected to the battery. This project is used alternator that functions to charge the battery. The system charging of battery, voltage at generator must higher than voltage at battery. This project also used lead acid battery is rating voltage and current is 12V 45AH. The Lead-acid batteries require protection from overcharge and over-discharge. The charge controller in this project is operated that to prevent overcharging of the batteries. The ballast load in this system takes the excess energy produced that is no longer needed to keep the batteries charged, and diverts it to a waste load. This system also used power inverter that functions convert from DC to AC voltage.

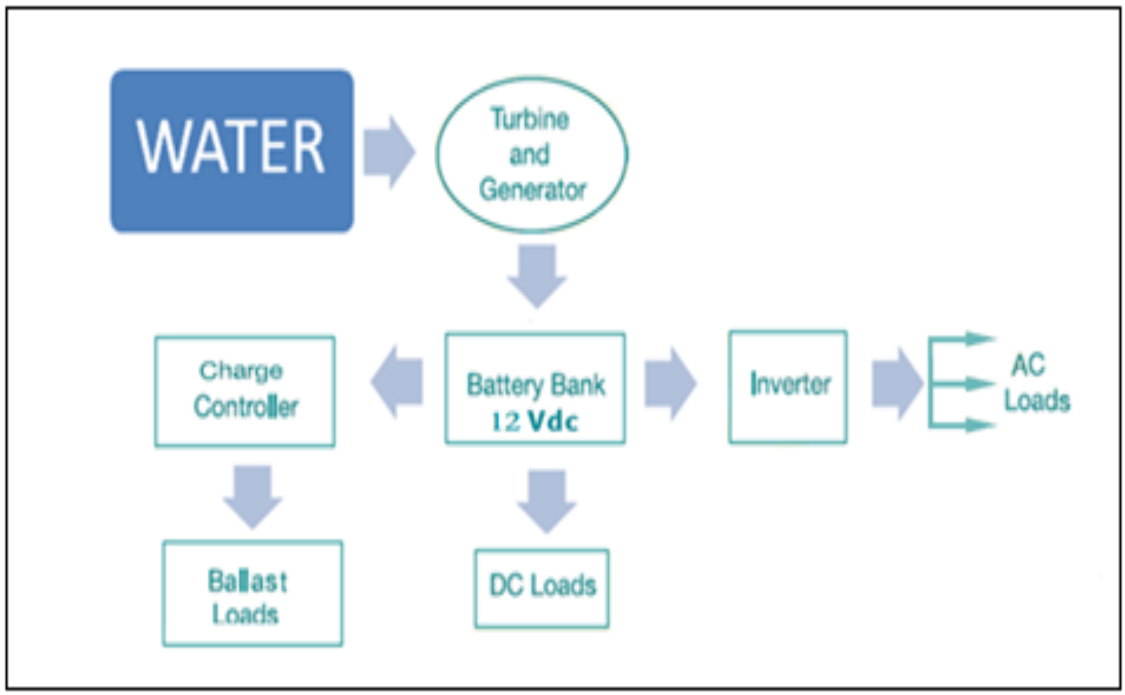


Figure 3.1: Block Diagram of Microhydro Generator System (MHGS)

Figure 3.2 show that the hardware system of MHGS. The design is used impeller as a turbine. The gear is connected by shaft at impeller turbine to rotate the alternator using gear. In micro hydro system, water turns a wheel to rotate a turbine connected alternator using gearing concept and produce electricity. These projects want to more rotate and high speed to charge the battery. The concept of charging system, when the charging system's output is greater than that needed by the vehicle, it sends current into the battery to maintain the batter's state of charge.

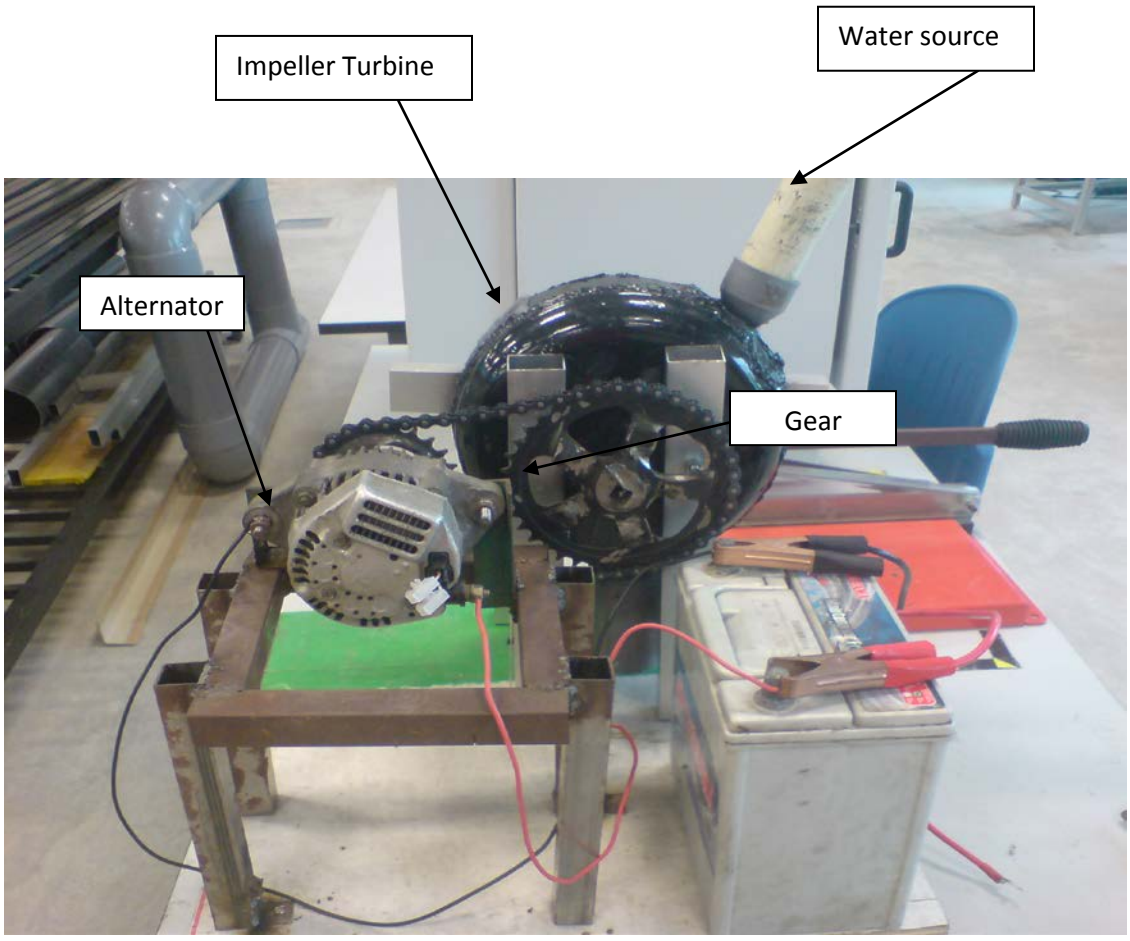


Figure 3.2: Hardware System of MHGS

Figure 3.3 show that this operation system of MHGS using AC Motor. Before we installed at turbine, we must test using the AC Motor. Alternator is connected at the AC Motor to charge the battery. The power inverter is connected at lead-acid batteries to convert voltage from 12VDC to 220VAC. Power inverters are used to convert DC to AC so that stored battery power may be used as needed by appliances and other loads. The multi-meter at this figure is function to measure range of the voltage at lead-acid batteries. Voltage increase when speed of alternator is increase.

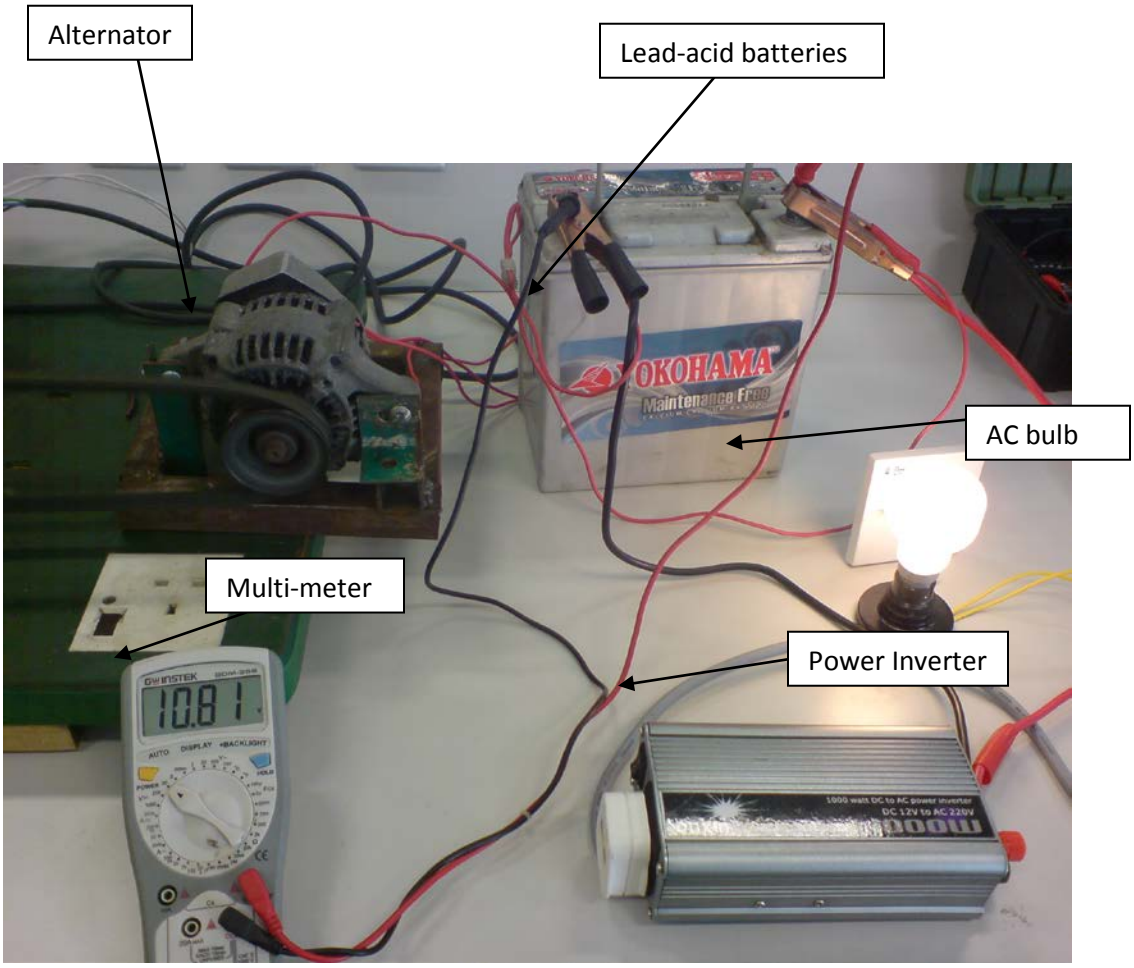


Figure 3.3: Operation System of MHGS using AC Motor

3.2.2 Electrical System Design

The second part of this project is electrical system design. Figure 3.4 show that the circuit charge controller. This project is used PIC 18F4550 as microcontroller. The components for whole this circuit is used such as LCD display, crystal, resistor, capacitor, transistor, LM7805, relay 5V, LED and DC motor 12V. The LCD is used to display rating voltage at the battery. The LED green, yellow and red as signal for this system. This circuit is operation base on voltage supply. When battery low, LCD can display Battery Charging and LED Red is shown.

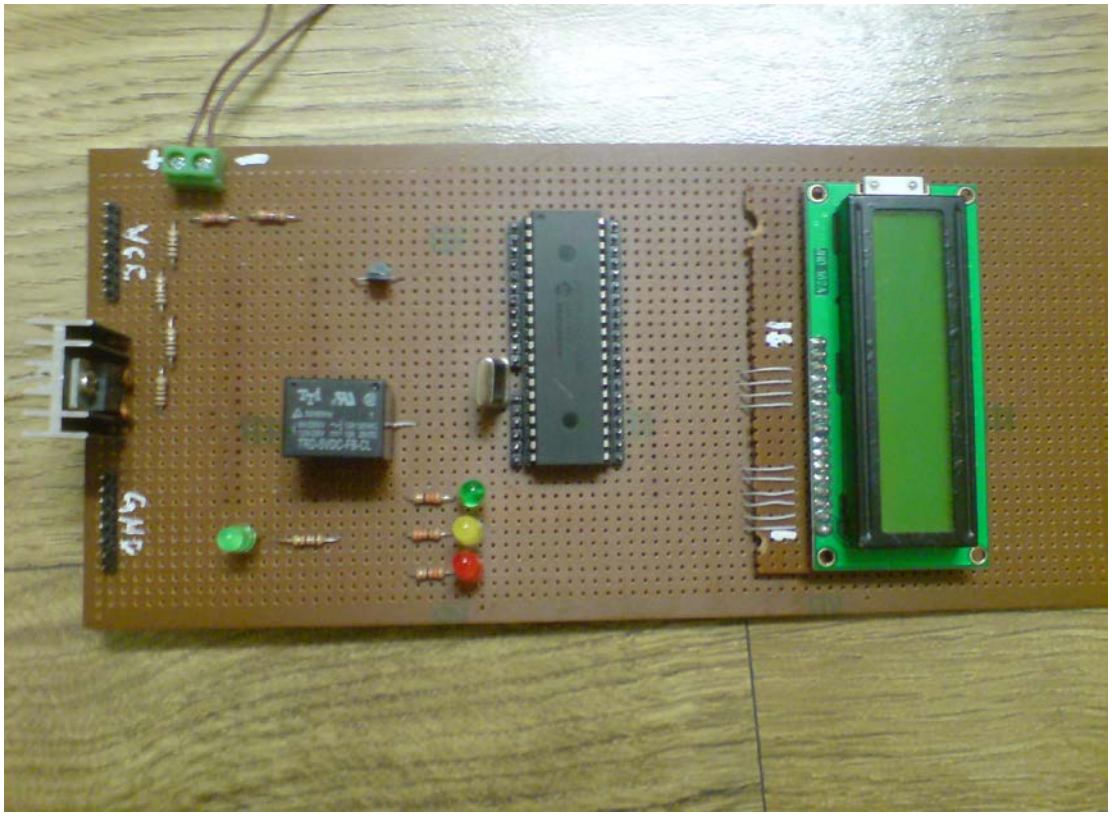


Figure 3.4: Circuit charge controller using PIC18F4550

3.3 Basic Components of MHGS

This project is using battery based system so basic components to develop of Microhydro Generator System (MHGS) is turbine, alternator, battery, charger controller, ballast load, power inverter and turbine. This topic can explain more detail about the function for each component.

3.3.1 Alternator

An alternator differs from a dc motor in that it contains no permanent magnet. Figure 3.5 shows that alternator which has a built in rectifier to convert the generated AC signal to a DC signal**.** The specified turbines which convert mechanical energy into electrical energy use an alternator that outputs a DC signal**.** The DC signal is then sent to the battery where, along with the batteries a monitor will be needed this way you can determine how much electricity the turbine is generating, the consumption of that energy and battery capacity.

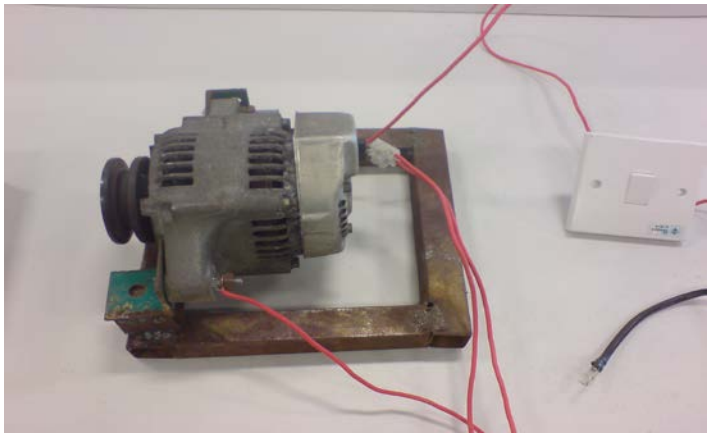


Figure 3.5: Automotive Alternator

3.3.2 Battery

Deep cycle batteries are best to use for any renewable energy system. Figure 3.6 show that, Batteries Lead-acid deep cycles are usually used in hydro system. Deep cycle batteries are designed to withstand repeated charge and discharge cycles. The amount of batteries in Micro-Hydro system will depend on our needs. The input voltage to the batteries in a battery based system commonly ranges from 12 to 48 Volts DC.

Figure 3.6: Lead-acid batteries

3.3.3 Charge Controller

A charge controller is connected with the battery operation to prevent overcharging of the batteries. In the event of a power outage excess electricity could be produced and the charge controller would absorb the excess energy to protect the batteries. Hydro systems with lead-acid batteries require protection from overcharge and over-discharge.

3.3.4 Inverter

A battery bank does not enable users to live with all the conveniences of modern living, as most appliances use high voltage AC (alternating current) while batteries can supply only DC (direct current). Figure 3.7 show that inverters are used to convert DC to AC so that stored battery power may be used as needed by appliances and other loads. This power inverter is 1000W capacity to the load. Modern inverters are available in virtually any wattage capacity, in recreational and commercial grades, in a variety of DC voltages, and with the220-240VAC, 50 Hz output for the rest of the world and 120VAC 60 Hz output for North American applications.

Figure 3.7: Inverter

3.3.5 Ballast Load

A ballast load takes the excess energy produced that is no longer needed to keep the batteries charged, and diverts it to a waste load. Most of the time, we will find dump

loads consisting of water heater elements or air heaters. A ballast load is a very important component to the system.

3.3.6 Turbines

Turbines are commonly used today to power micro generator system. The moving water strikes the turbine blades, much like a waterwheel, to spin a shaft. But turbines are more compact in relation to their energy output than waterwheels. There also have fewer gears and require less material for construction. Low head, low flow turbines may be difficult to find, and may have to be custom-made [3]. There are two general types of turbines like impulse and reaction. Figure 3.8 show that the waterwheel is part of this system. This waterwheel has diameter 0.15m and 12 blades.

Figure 3.8: Waterwheel

3.3.6.1 Impulse Turbine

Impulse turbines, which have the least complex design, are most commonly used for high-head micro hydro system. The most common types of impulse turbines include the Pelton wheel and the Turgo wheel. That mean, the Pelton wheel uses the concept of jet to create energy. Pelton wheel turbines are also available in various sizes and operate best under low-flow and high-head condition. Another impulse turbine is Turgo impulse wheel is an upgraded version of the Pelton. The size of Turgo is half the size of the Pelton. Turgo wheel moves twice as fast. It is also needs few or no gears and good reputation for trouble-free operation. The Turgo can operate under low flow condition but requires a medium or high head.

3.3.6.2 Reaction Turbine

Reaction turbines, which are highly efficient, depend on pressure rather than velocity to produce energy. All blades of the reaction turbine maintain constant contact with the water. These turbines are often used in large-scale hydropower sites. Because of their complexity and high cost, reaction turbines aren't usually used for micro hydropower projects. An exception is the propeller turbine, which comes in many different designs and works much like a boat's propeller. Propeller turbines have three to six usually fixed blades set at different angles aligned on the runner. The bulb, tubular, and Kaplan tubular are variations of the propeller turbine. The Kaplan turbine, which is a highly adaptable propeller system, can be used for micro hydro sites [4].

Figure 3.9 show that, Impulse and reaction turbine are two most widely used methods of obtaining energy from water, there is another version which is a hybrid of two. Called a Crossflow turbine, it converts energy from both the kinetic energy of water flow and the pressure loss of the flow. It does this by performing the flow, at the entrance of the turbine, into a rectangular jet and forcing this jet onto the blades of the turbine. The orientation of the turbine axis is perpendicular to the flow, and the turbine itself is hollow. Therefore, after the flow has struck the blades of the turbine, it falls through the center axis and strikes the blade again on the bottom side of the turbine. This imparts a loss of pressure in the flow and thus imparts more energy into the turbine [2].

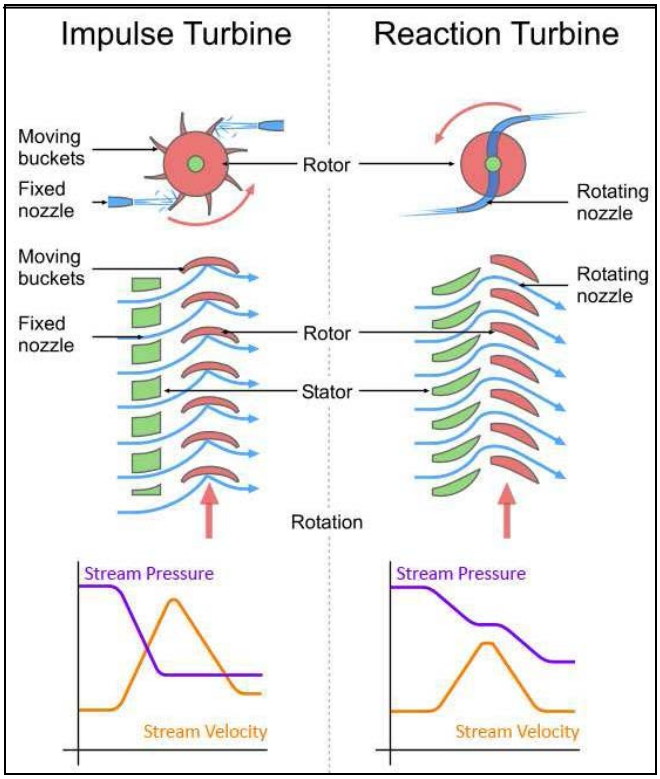


Figure 3.9: Comparisons of Impulse and Reaction Turbine

3.4 Software Implementation

This section will discuss about software which has been implemented in this project which are MicroCode Studio PicBasic Pro (PBP) Compiler for programming PIC18F4550, Proteus 7 Profesional for designing the circuit and simulation for the programming and also UP00B PIC USB Programmer for writing the programming language into the PIC18F4550

3.4.1 MicroCode Studio (PBP) Compiler

MicroCode Studio is a powerful, visual Integrated Development Environment (IDE) with In Circuit Debugging (ICD) capability designed specifically for microEngineering Labs PICBASIC™ and PICBASIC PRO™ compiler.

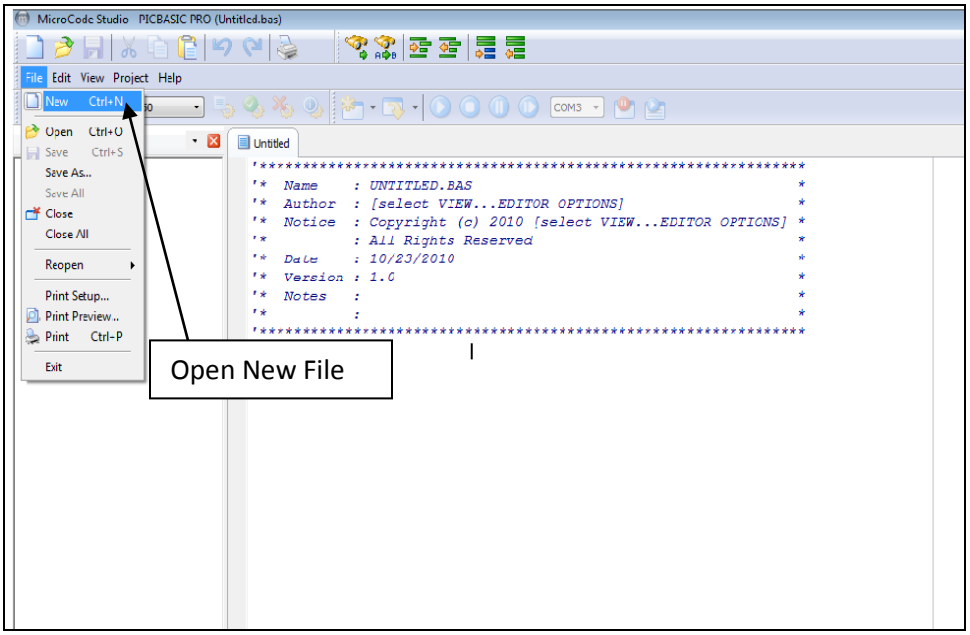
The main editor provides full syntax highlighting of your code with context sensitive keyword help and syntax hints. The code explorer allows you to automatically jump to include files, defines, constants, variables, aliases and modifiers, symbols and labels, which are contained within your source code. Full cut, copy, paste and undo is provided, together with search and replace features.

- Full syntax highlighting of your source code
- Quickly jump to include files, symbols, defines, variables and labels using the code explorer window
- Identify and correct compilation and assembler errors
- View serial output from your microcontroller
- Keyword based context sensitive help
- Support for MPASM

Below is the step to use the using MicroCode Studio software in charge controller and display LCD:

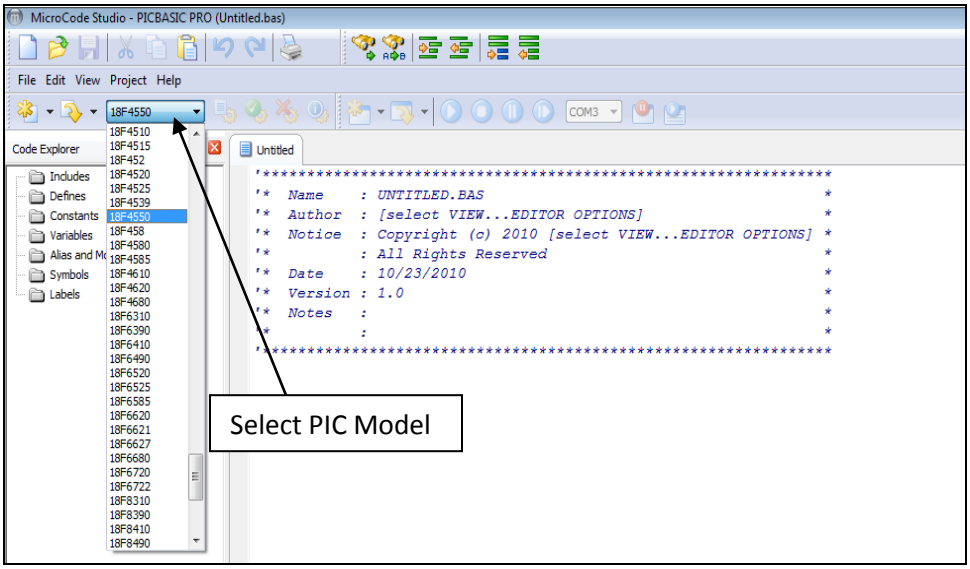
Step 1: Opening New File

The first step to use the Microcode Studio is open the new file to create the program.



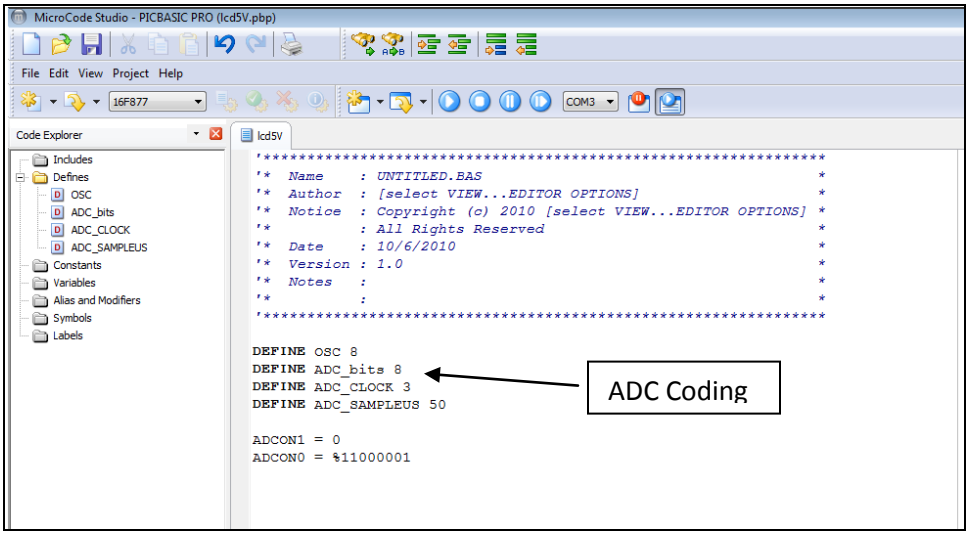
Step 2: Selecting PIC Model

The second step is selecting the PIC model to use.



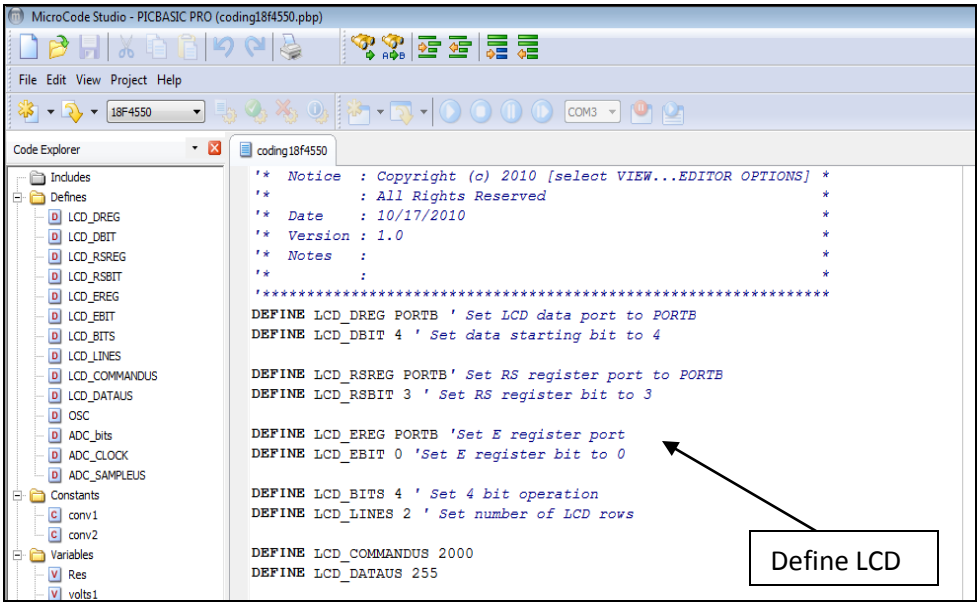
Step 3: ADC Coding

After open the new file and select the PIC model, the third step is write the ADC coding.

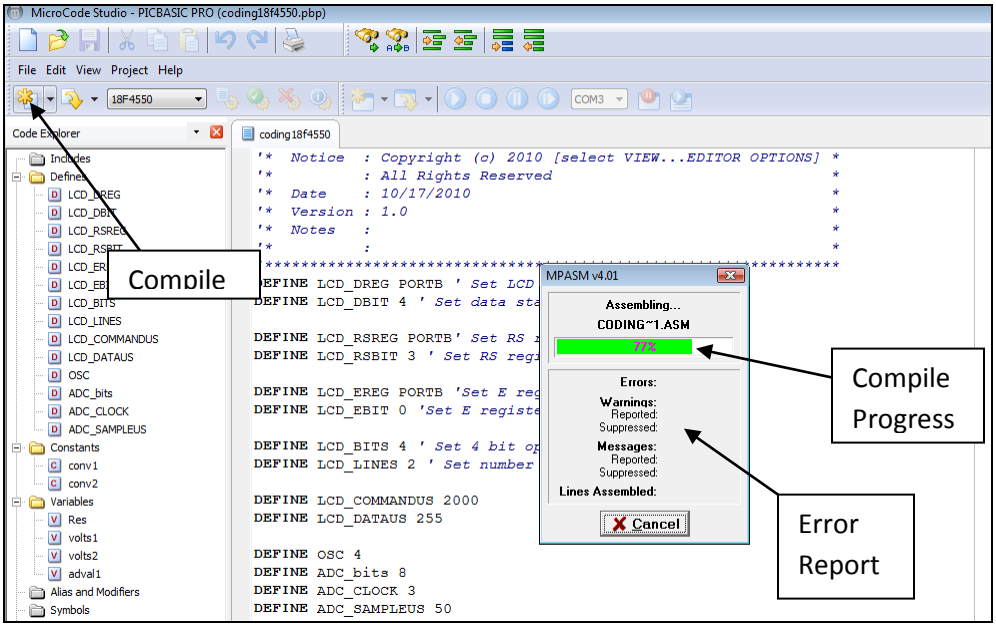


Step 4: Define Variable & LCD Display

The fourth step is before start the all program we must define variable and declare instruction LCD display



Step 6: Compile Program & Error Checking



After all steps are done, the PIC is ready to write by using UP00B PIC USB Programmer.

3.4.2 UP00B PIC USB Programmer

UP00B is the enhanced version of UP00A. As PIC MCU is gaining its popularity in market for student and hobbyist, more low cost and user friendly programmer is needed. Previous USB PIC Programmer, UP00A is obsolete because it cannot support Windows Vista, fail to program many new PIC MCU, further the firmware is not upgradeable. Hence, UP00B is now introduced to you! It comes with two ZIP sockets to offer program loading to 8 pin, 18 pin, 28 pin and 40 pin PIC MCU (8 bit) by using Microchip PICKit2 software. It offers a low cost yet convenience USB PIC Programmer to user. Loading program to PIC MCU will be as easy as 1, 2, 3. It has been designed with capabilities and features as below:

- USB powered, no extra power needed to load program
- Two ZIF sockets (20 pins and 40 pins) to ease program loading process
- Support most 8pin, 18pin, 28pin and 40pin PDIP 8 bit PIC MCU
- Support windows XP and Vista
- Support Intel and AMD based system
- Support Laptop and desktop PC

Package Including:

- 1 USB Programmer UP00B
- 1 USB Cable (B type)
- 1 Software Installation and User’s Manual CD Rom

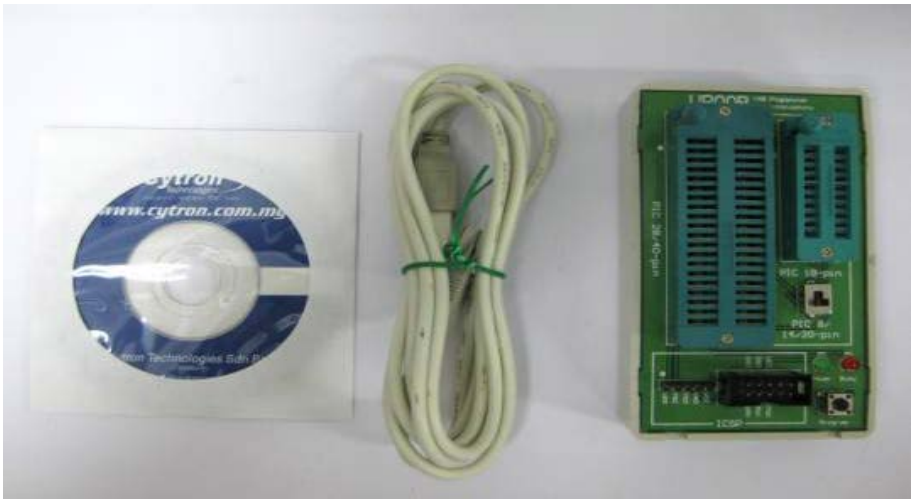


Figure 3.10: CYTRON USB Programmer

3.4.2.1 Board Layout

Table 3.1 Function of Board Layout Identified

Label	Function
A	ZIF Socket 20 pins
B	ZIF Socket 40 pins
C	Switch selector for PIC pins of ZIF Socket 20 pins
D	Busy LED
E	Power LED
F	Program Button
G	Connector for ICSP

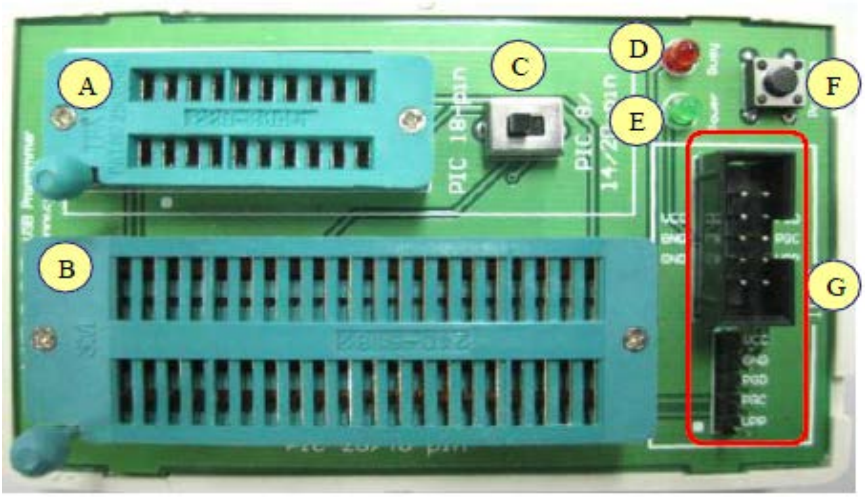


Figure 3.11: Board Layout USB Programmer UP00B

3.4.2.2 Installation (Software)

The programmer software for UP00B is Microchip PICkit 2 Programmer software. This is simple instructions, the following section will guide user to install this software.

1. Place UP00B CD in to computer or laptop CD drive.
2. Browse to folder “UP00B setup”.
3. Double click “setup” to run the installation wizard.

3.4.2.3 Plugging the Microcontroller

40-pin Microcontroller

- Plug in the microcontroller at the ZIF Socket 40 pin (indicated on the board) and push the toggle as shown.

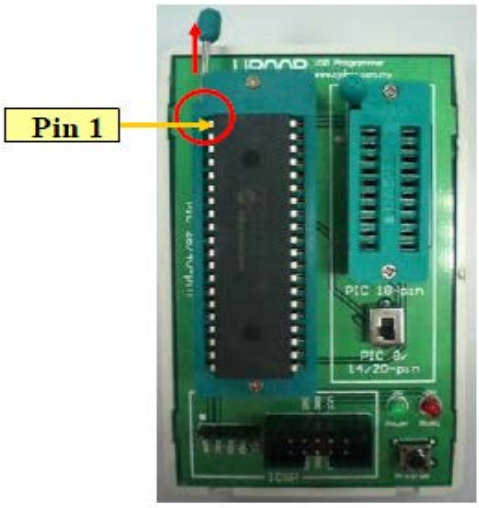
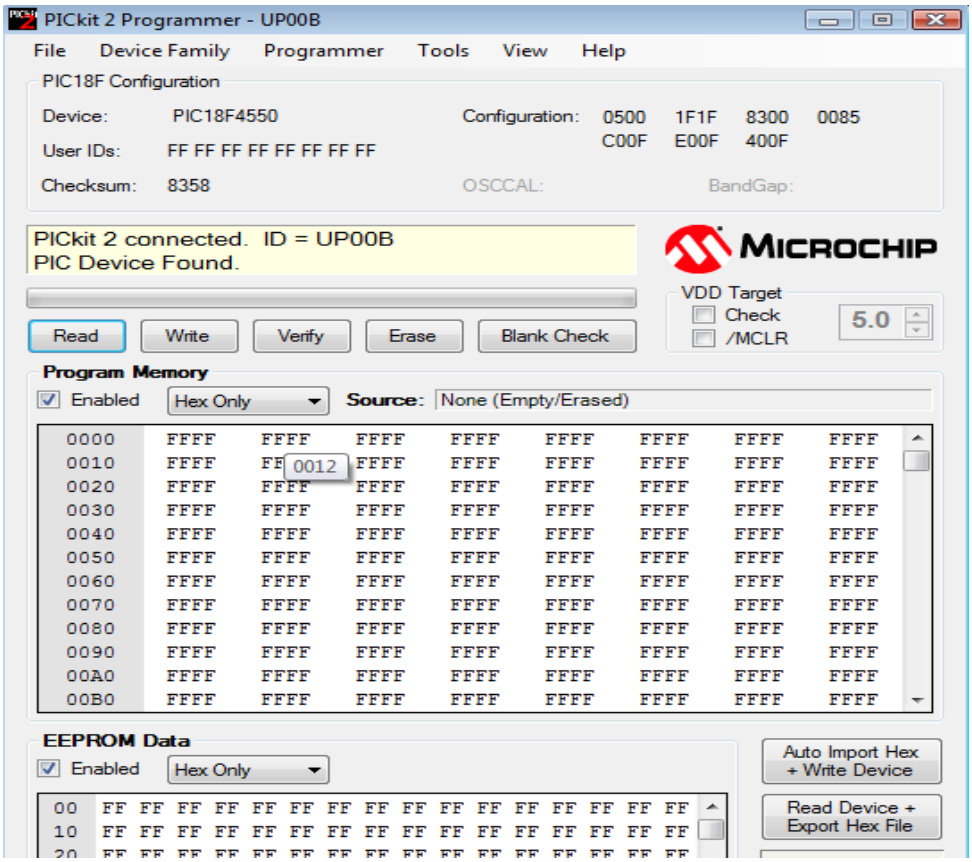


Figure 3.12: Plug-in 40-pin Microcontroller

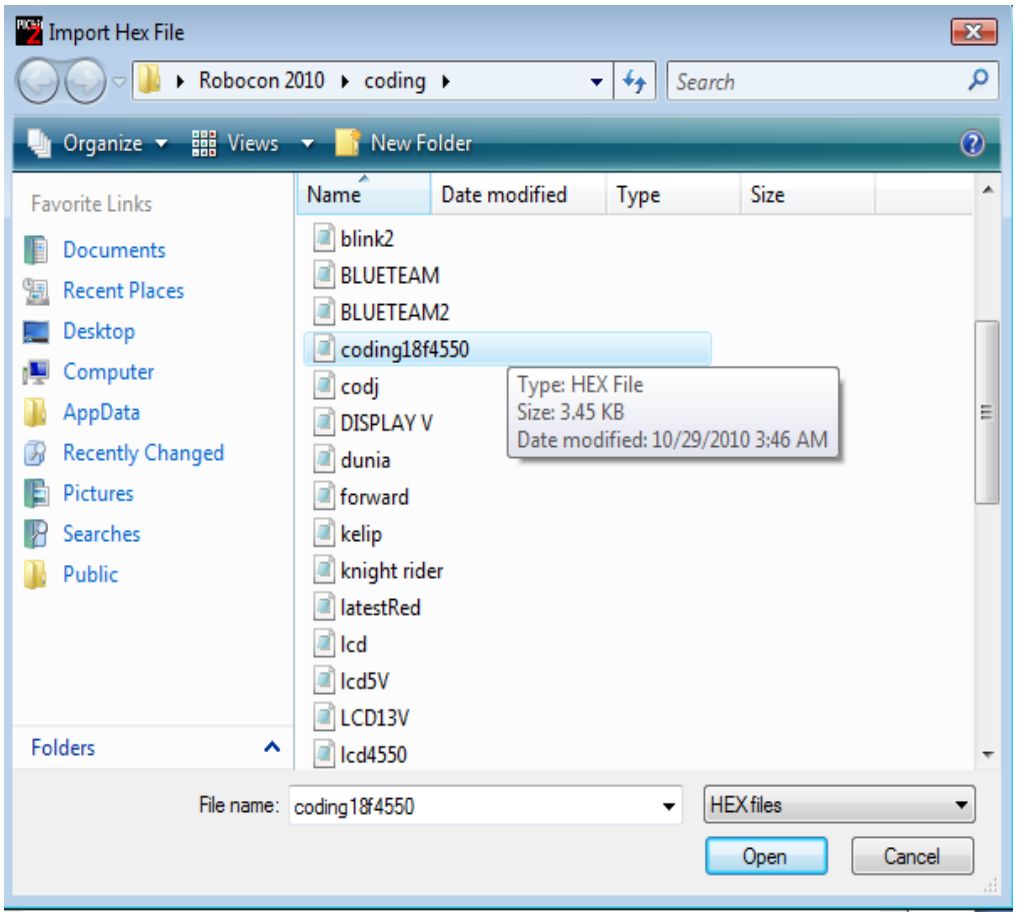
3.4.2.4 Program the PIC Microcontroller

To start writing the C-language in PIC18F4550, first run PICkit 2 Programmer software.

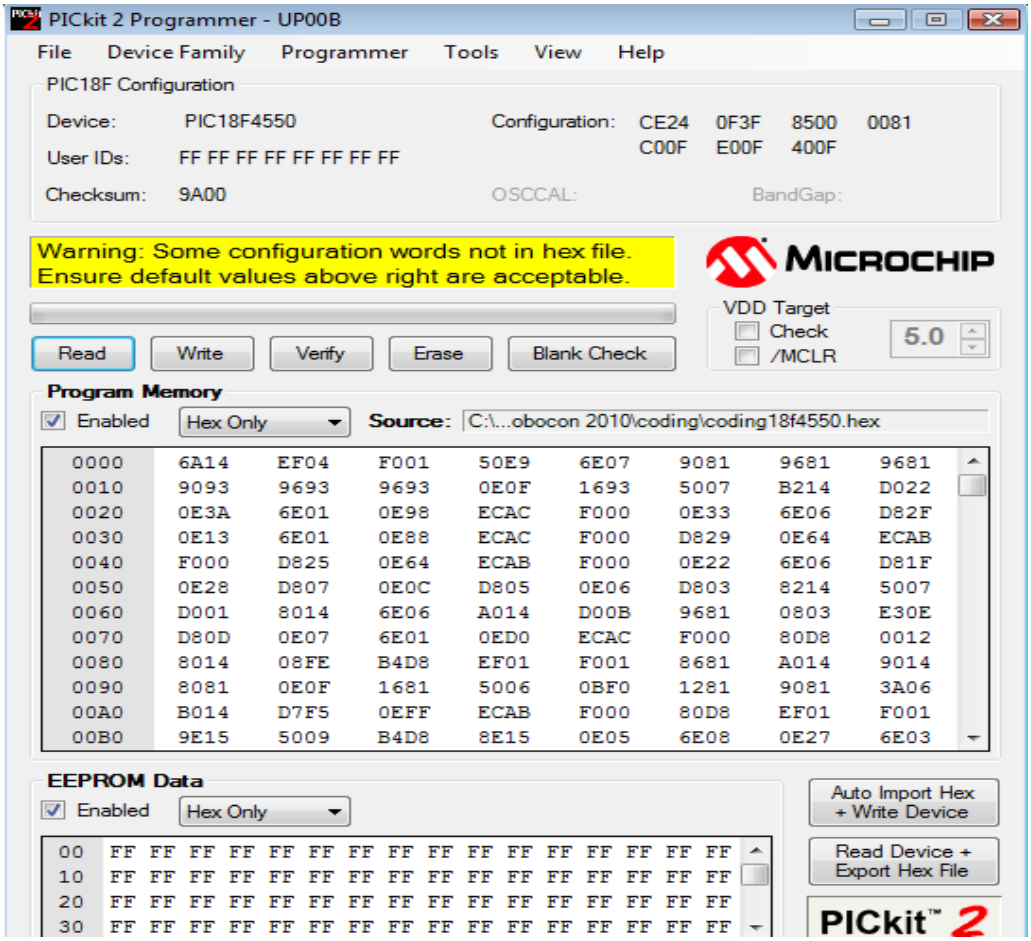
1. By clicking the icon shown, the programmer will detect the type of PIC on the Programmer.


PICkit 2 Programmer - UP00B
File
Device Family
Programmer
Tools
View
Help
PIC18F Configuration
Device: PIC18F4550
Configuration: 0500 1F1F 8300 0085 C00F E00F 400F
User IDs: FF FF FF FF FF FF FF FF
Checksum: 8358
OSCCAL:
BandGap:
PICkit 2 connected. ID = UP00B
PIC Device Found.
MICROCHIP
VDD Target
Check
/MCLR
5.0
Read
Write
Verify
Erase
Blank Check
Program Memory
Enabled
Hex Only
Source: None (Empty/Erased)
0000 FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
0010 FFFF FF 0012 FFFF FFFF FFFF FFFF FFFF FFFF
0020 FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
0030 FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
0040 FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
0050 FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
0060 FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
0070 FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
0080 FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
0090 FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
00A0 FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
00B0 FFFF FFFF FFFF FFFF FFFF FFFF FFFF FFFF
EEPROM Data
Enabled
Hex Only
00 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
10 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
Auto Import Hex + Write Device
Read Device + Export Hex File

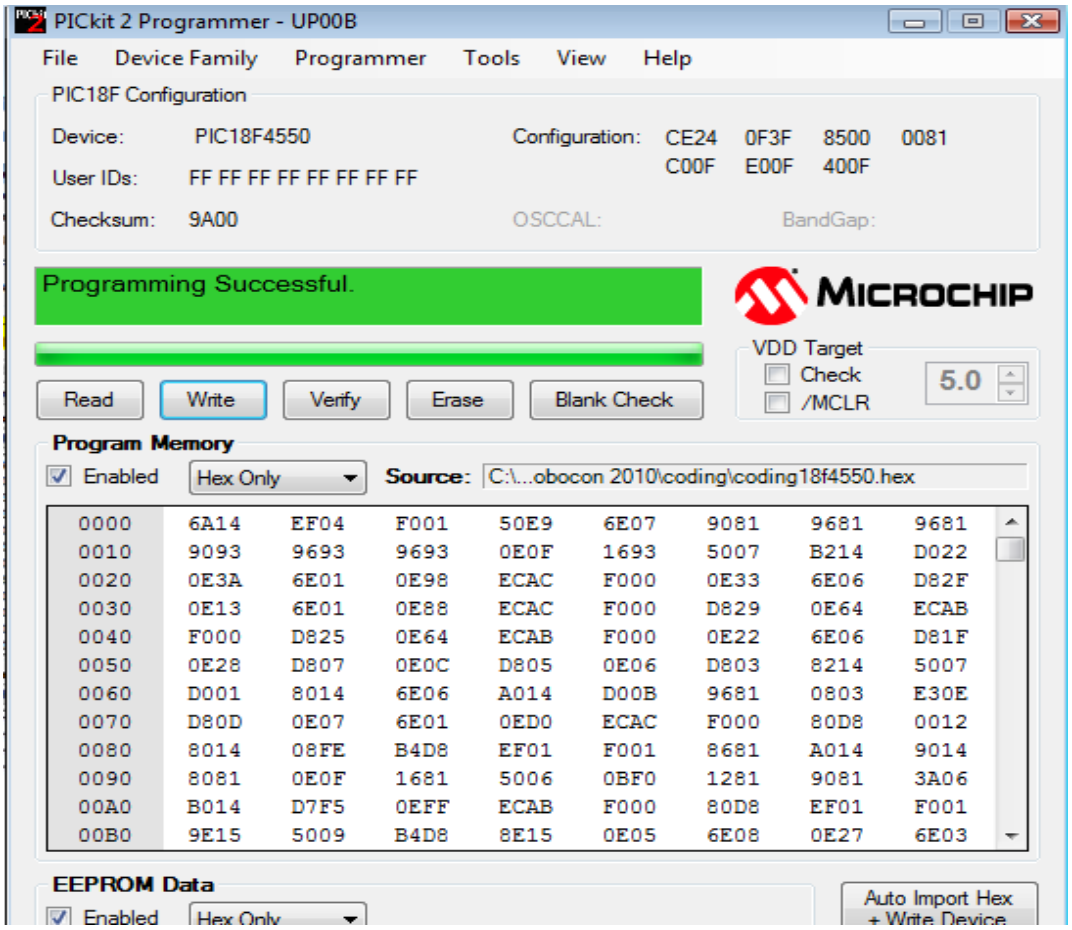
2. To write Hex code to PICkit 2 we must first open the hex file. By clicking the icon shown, choose the coding to burn at PICkit 2.



3. Then, icon showed the hex code.



4. After that, click write to check the programming is successful. When it is completed, the icon will show the Programming successful then the PIC18F4550 is ready to be plug out.



3.5 Summary

The concept and method development of MHGS have been described in this chapter. All the components of this project must check specification and test. Make sure all the components can be function before installed. All the circuit in this project will be controlled by PIC18F4550 microcontroller which acts as the processor in this project. It is very important to implement the hardware stage by stage so that it will be easy to troubleshoot if there's a problem. The most important thing is to make sure that the PIC18F4550 microcontroller can constantly operate and functioning so that it will keep all circuits runs. Next, in chapter 4 present more detail about result and discussion.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Introduction

In this chapter explains about results and discussion for whole development of Microhydro Generator System (MHGS) process will be describe. The result will be discussed in this chapter is for the data collection of automotive alternator with using AC motor and also using Tachometer to measure the speed rotation. This chapter also will discuss about charge controller for the system. The calculation in this chapter is depend on the result of data collection of automotive alternator. It depends on water pressure and rotation of speed to generate power for this system. The important of this project is generate more power using pressure water to produce electricity can achieve the objectives of this project. Every discussion and analysis stated in this chapter also for the whole system problem, the better solution need to come-up in order to overcome every flaw and problem of this MHGS.

4.2 Alternator Output

Alternator is mechanical energy is transferred from the engine to the alternator by a grooved drive belt on a pulley arrangement. Through electromagnetic induction, the alternator changes this mechanical energy into electrical energy. The alternating current generated is converted into direct current (DC) by the rectifier, a set of diode which allow current to pass in only one direction. The alternator output test check the ability of the alternator to deliver its rated output of voltage and current. Output current and voltage should meet the specifications of the alternator. From the experimental result is data collection of alternator output using AC motor, frequency controller and tachometer to measure rotation speed of alternator.

Table 4.1: Alternator speed without battery

Frequency Controller, Hz	Speed without battery, RPM
0	0
20	250.4
25	284.4
30	367.9
35	389.5
40	441.1
45	534.7
50	611.1

Table 4.1 shows that the measurement of rotation speeds without battery using frequency controller. The minimum rotation speed of alternator is 250.4 rpm and maximum at frequency 50Hz is 611.1 rpm. The rotation of alternator is high when without tap battery because the amature no voltage produce.

Table 4.2: Alternator speed using battery

Frequency Controller	**Speed using battery, RPM**
0	0
20	210.4
25	268.8
30	353.9
35	370.3
40	400.3
45	480.5
50	550.6

From the table 4.2 show that frequency controller and speed using battery. The experiment is to measure of rotation speed using battery. The minimum rotation speed of alternator is 250.4 rpm and maximum at frequency 50Hz is 611.1 rpm. The different without battery and using battery is speed. The battery supplies current to energize the alternator. During charging, the battery changes electrical energy from the alternator into chemical energy. When used the battery the alternator produce voltage at amature.

Table 4.3: Alternator output current

Frequency Controller	Rotation Speed of Alternator, RPM	Current, A
0	0	0
20	250.4	0.1
25	284.4	0.1
30	367.9	0.2
35	389.5	0.2
40	441.1	0.3
45	534.7	0.3
50	611.1	0.4

Table 4.3 shows that the alternator output current is measured used multi-meter and tachometer. The data is collected using frequency controller as control the speed of AC motor. When increase the frequency controller so the current produce is high. The rotation of alternator is effect of produce current.

4.3 Water Power Output

Water power output can measure by using this formula and 0.6 is efficiency of water power.

Pth = Q x H x **g x 0.6**
Pth = Theoretical water power output in W
Q = Usable flow rate in m3/s
H = Gross head in m
g = Gravitational constant (9.8 m/s2)

Table 4.4: Theoretical of Water Power Output in Watt

Water Power Output, W	**Usable flow rate in m^3/s, Q**	**Gross head, m**
58.8	10	1
176.4	15	2
352.8	20	3
588.0	25	4
882.0	30	5

Table 4.4 show that theoretical calculation of water power output in Watt. Flow rate and gross head is effect to produce water power. The power formula demonstrates that a site with high head might only need a small flow while a site with a high flow might only need a small head. While a micro hydro unit can operate with as little as two metres of head, most units used in domestic situations will require at least ten metres head. Designing and installing the pipe work for a site with less than ten metres head can be very difficult.

4.3 Charge Controller Circuit

Figure 4.1, show that, the charge controller circuit where it used PIC18F4550 as controller using simulation of Proteus 7 Professional. The circuit function when detect voltage at battery. Figure 4.1 show that LCD display voltage at battery and LED show colour green when voltage full. If voltage full higher 12V relay is functioning to run motor. That mean signal of voltage is higher than 12V. Transistors amplify current, for example we can be used to amplify the small output current from a logic IC so that it can operate a lamp, relay or other high current device.

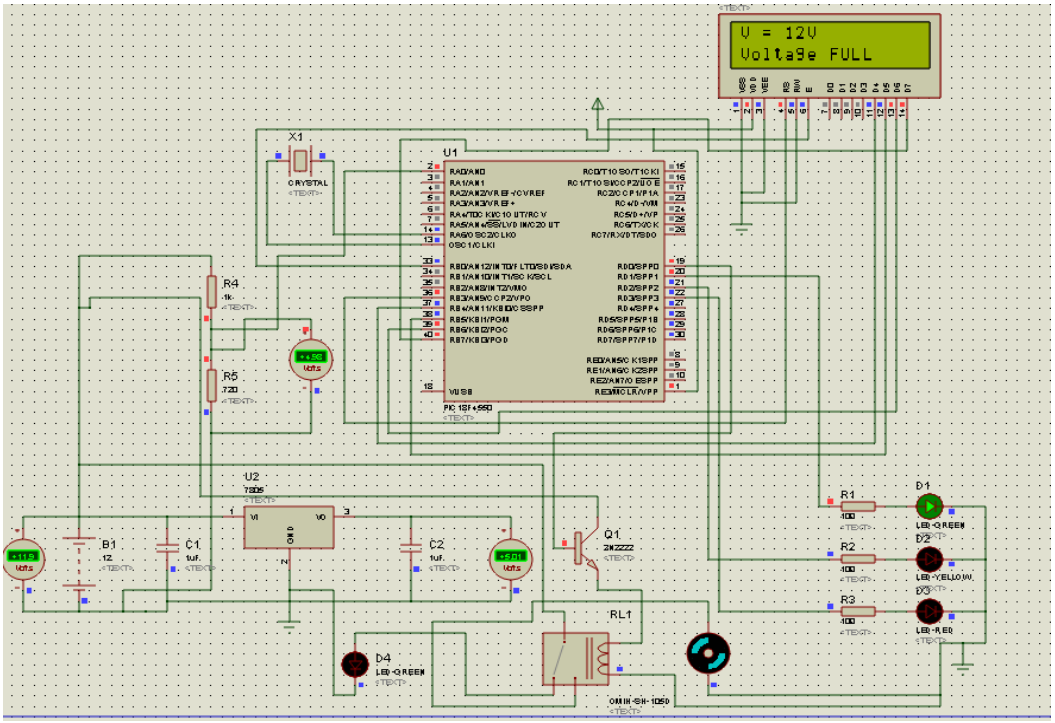


Figure 4.1: Voltage full at 12V using simulation

Figure 4.2 shows the hardware test using DC power. Figure 4.2 show that LCD display 13V and 100% when DC Power supply is 13V and current is 0.09A, meaning that the voltage is full. The programming can be program to show the percentage of charging battery and display at LCD.

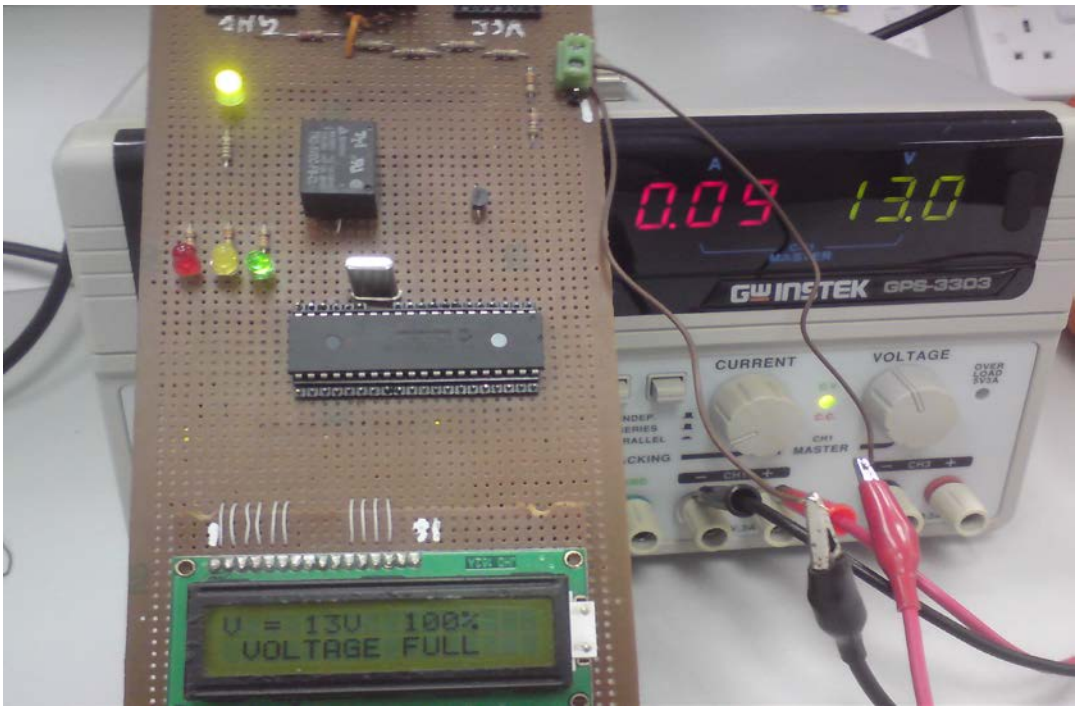


Figure 4.2: Voltage full at 13V and 100% using Power DC supply

Figure 4.3 show that, we can see when voltage is 7V, then the LCD display voltage low and the LED Yellow is on show that voltage is low by using simulation.

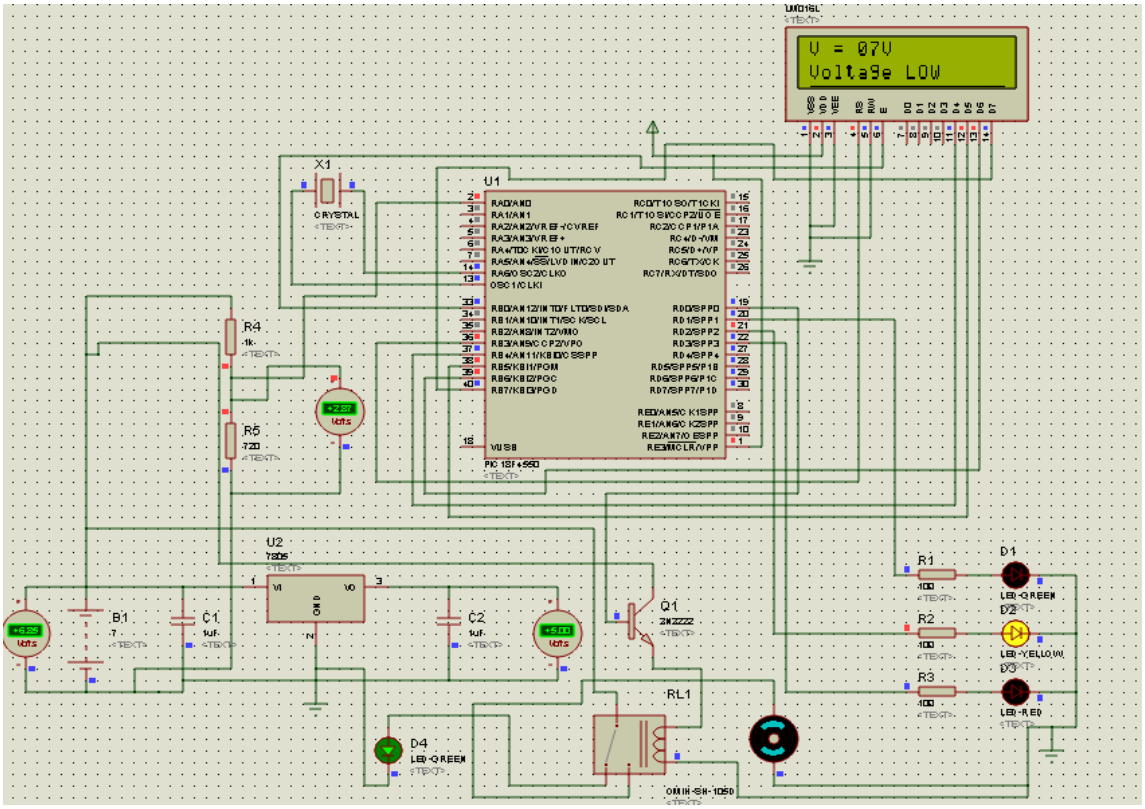


Figure 4.3: Voltage low at 7V using simulation

Figure 4.4 using DC power supply 11V and current is 0.07A then LCD display voltage 12V and percentage is 60% meaning that voltage is low. The voltage is different from simulation this is because hardware has voltage drop.

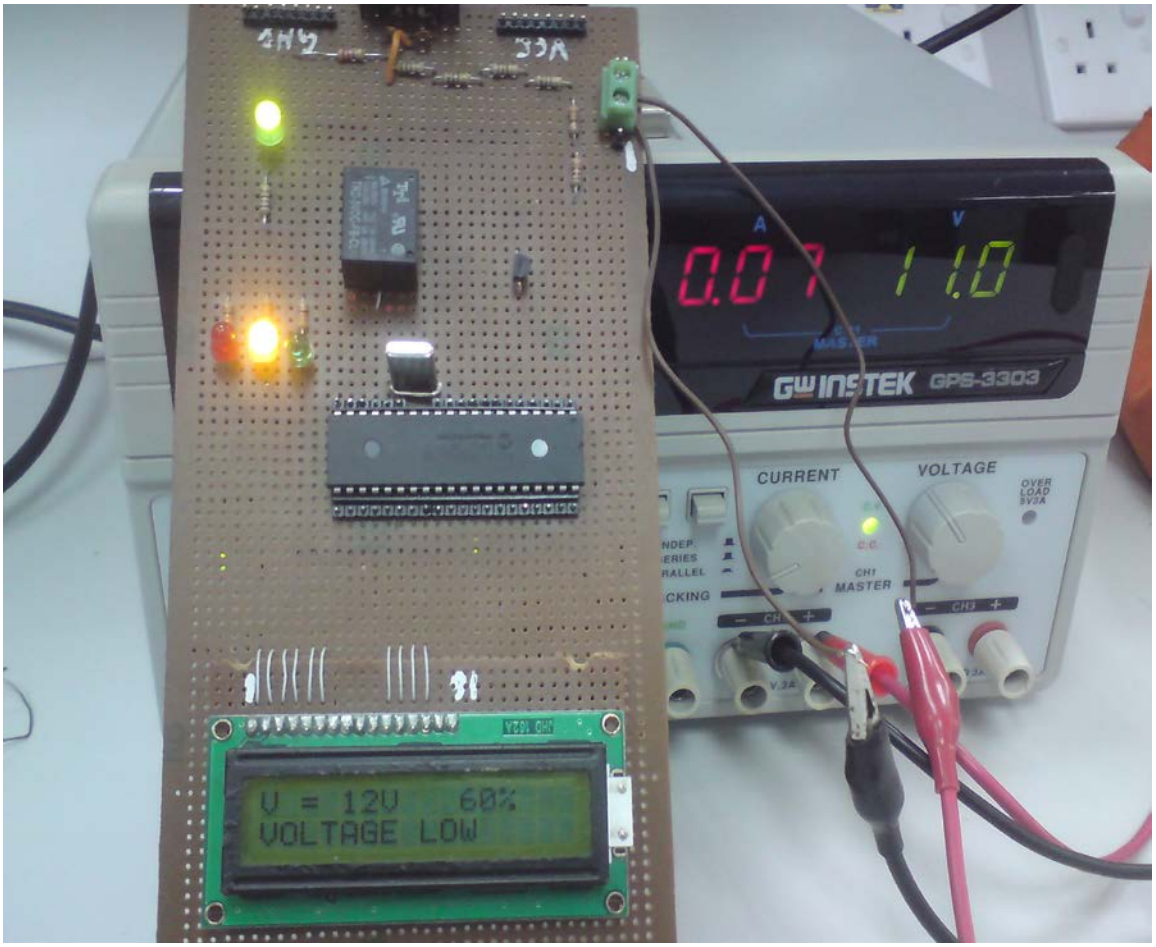


Figure 4.4: Voltage low at 12V and 60%

Figure 4.5 show that, when voltage is 4V, then the LCD display battery charging and the LED Red is on show that battery start charging and the voltage is different from simulation this is because hardware has voltage drop.

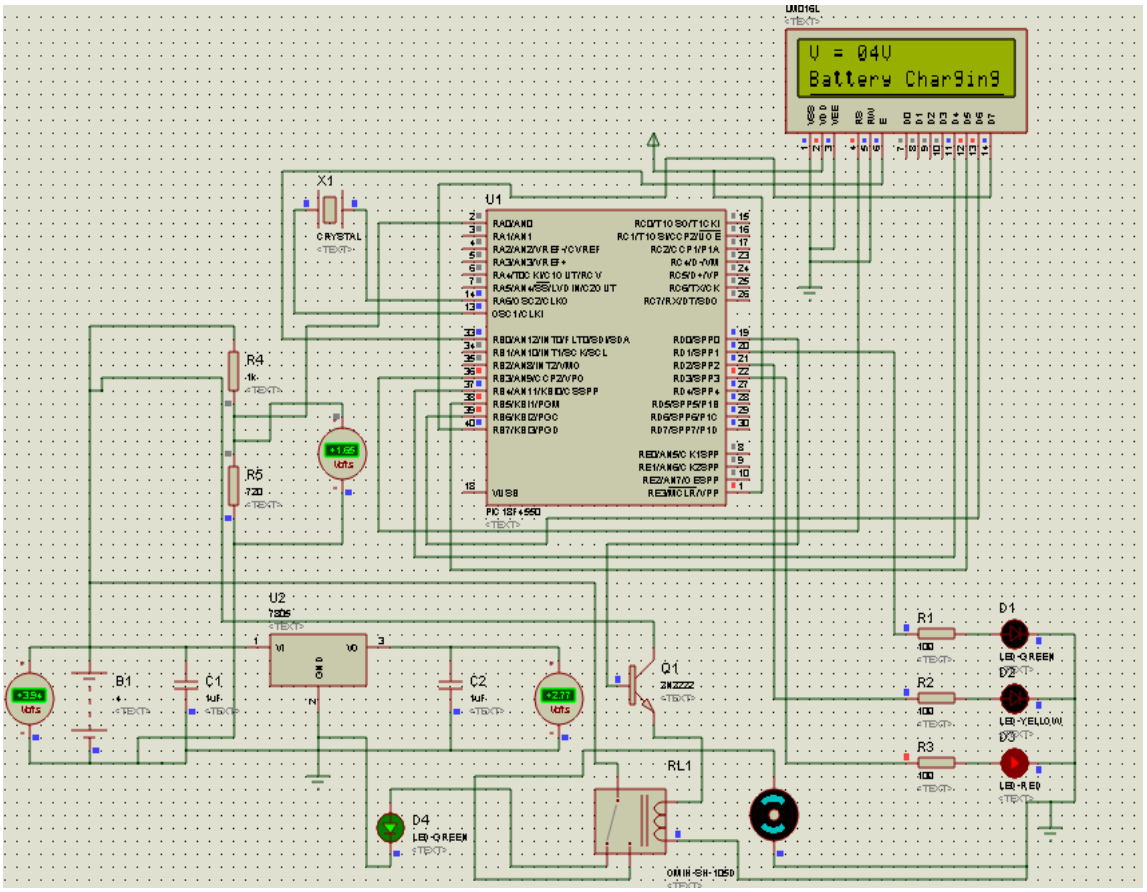


Figure 4.5: Battery charging at 4V using simulation

Figure 4.6 using DC power supply 8.1V and current is 0.06A then LCD display voltage 9V and percentage is 30% meaning that battery is start charging. The LED Red is show that signal battery in start charging.

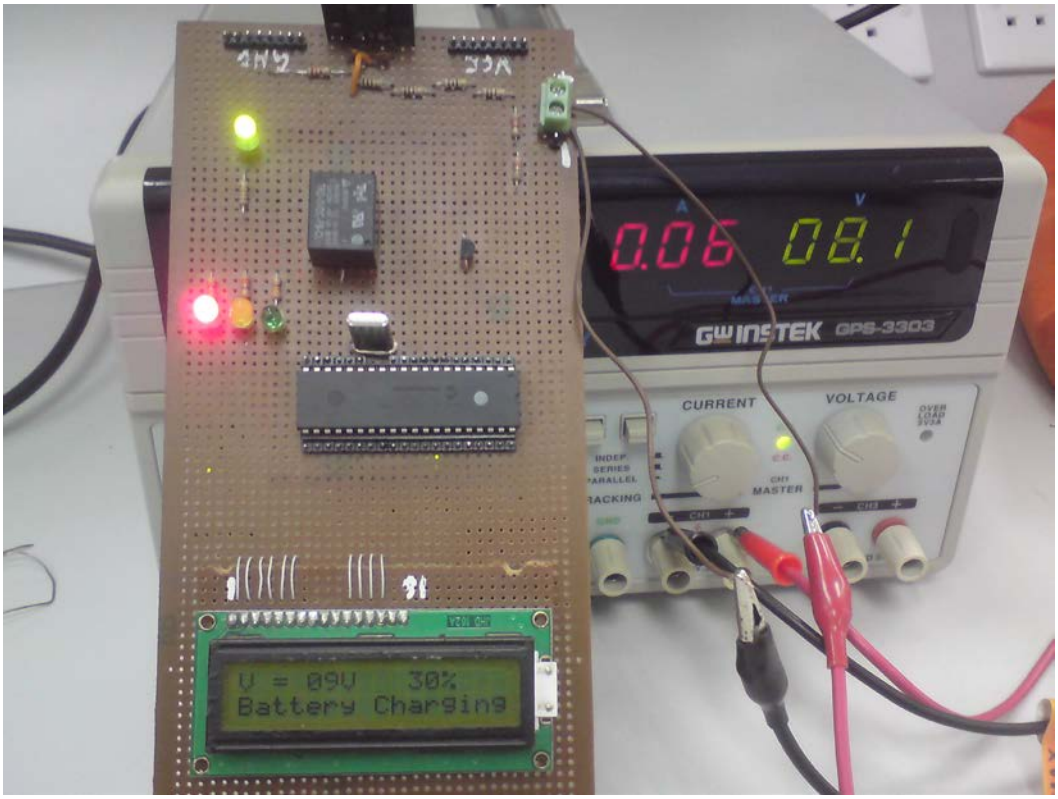


Figure 4.6: Battery start charging at voltage 9V and 30%

4.6 Summary

According to the results and discussions in this project, there are some important things that could be consider in order completing the whole MHGS, it is the sensitivity of this system. The speed is very important to generate power and produce electricity. This project also wants to high pressure of water to rotate the turbine very fast. The theoretical or water power output is depend on flow rate and gross head. Before we install the system, we must measure the gross head and flow rate. The suitable place to install this system at high mountain.

CHAPTER 5

CONCLUSION

5.1 Conclusion

As a conclusion, this project is almost always more cost-effective than any other form of renewable power. The objectives of the development of Microhydro Generator System (MHGS) were successfully fulfilled. Which are first by designing the hardware of mechanical part of turbine by using gear bicycle which can be operated. This project that utilized the use of PIC microcontroller, for charge controller and display voltage rating via LCD display circuit has successfully integrated between each other. In this chapter also include the future development. The combination of analog electronics knowledge, autotronics knowledge, Microprocessor knowledge, power electronic knowledge and individual self skilled method to create the new circuit is important in order to make this project success. Lastly, for long term this project, in case for the commercialization especially in Malaysia.

5.2 Recommendation

The recommendation of this project is for next improvement process the student must study the Microhydro Generator System (MHGS) in detailed and make sure to understand and a new upgrade can be done to make the MHGS more effective and generate more power. Before install the system make sure to measure the pressure of water and high of head. Other than that, choose of turbine is effect of the system. In designing the hardware and circuit device is very important to effective of this project. The last future recommend that can be done is to design of MHGS is produce more electricity and reduce the cost of construction.

5.3 Costing and Commercialization

This part will describe the parts and overall cost of fabricating the development of Microhydro Generator System (MHGS). This part also will explain the commercialization of project.

5.3.1 Costing

Table 5.1 shows the cost of the component and the total cost. The total cost of the development of Microhydro Generator System is RM347.45. It is due to the changing of component in the development process, besides there were the components that do not function and need to be replaced during the hardware circuit designing. The cost stated above is for the hardware and electric and electronic components that used and involve in this project.

Table 5.1: The cost of components

Device	**Qty**	**Model**	**Manufacture**	**Unit cost(RM)**	**Extendedcost (RM)**
Alternator	1	Kancil		55.00	55.00
Turbine	1			10.00	10.00
Shaft	1			6.00	6.00
Power Inverter	1			220.00	220.00
Pipe	1			3.00	3.00
Resistor	8	330,100, 1K Ohm	Cytron	0.04,0.07	0.38
Transistor	2	2N2222	Cytron	0.20	0.40
LED	3		Cytron	0.12	0.36
Crystal	1	4MHz	Cytron	0.12	0.12
Stripe board	1		Cytron	5.00	5.00
Heat sink	1		Cytron	0.65	0.65
Capacitor	2	0.1uF	Cytron	0.12	0.24
Diode 12V	2		Cytron	0.30	0.60
LM7805	1		Cytron	0.70	0.70
PIC	1	18F4550	Microchip	30.00	30.00
LCD	1	2X16 JHD16A		15.00	15.00
				Total	347.45

5.3.2 Commercialization

This project can be commercialize by built the new Microhydro Generator System (MHGS) that follow the feature that have been recommended in the suggestion section, it is due to the target cost of the recommended Microhydro Generator System is more cheaper than this new invention one. The new microhydro generator system has the higher commercialize value because it can solve

REFERENCES

[1] Micro Hydro Power in the Nineties by *Paul Cunningham & Barbara Atkinson in May 1998*

[2] Micro-Hydro Power: A guide for development workers. P Fraenkel, O.Paish, V.Bokalders, A Harvey, A.Brown, R Edwards. Intermediate Technology Publishing

[3] Adam Harvey. Andy Brown. Priyantha Hemsfachi and Allcn lniwsiii."Micro Hydro Design Manual" */nlrrnrrdiutr T~clrrroiug~. Puhiicuiions. United Kingdon!.* 1993.

[4] Allen R. Invenin. "Micro Hydropower Sourcebook" *n'REC.4 lrrlernafioi~uFl oroidaiioir. Uiiiied Siaier. 1986.*

[5] Philip Hurst, '*Rainforest Politics, Ecological Destruction in South-East Asia'*, Zeds Books, London. 1990.

[6] Ministry of Science, Technology and the Environment, '*Assessment of Biological Diversity in Malaysia'*, 1997.

APPENDIX A

Charging System of Alternator

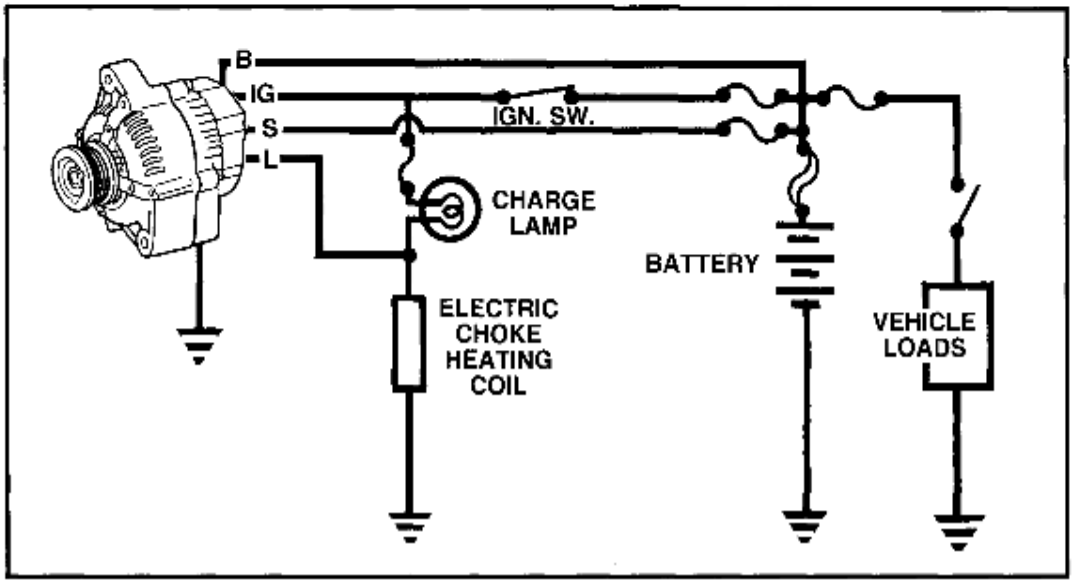
CHARGING SYSTEMS

General

The charging system converts mechanical energy into electrical energy when the engine is running. This energy is needed to operate the loads in the vehicle's electrical system. When the charging system's output is greater than that needed by the vehicle, it sends current into the battery to maintain the battery's state of charge. Proper diagnosis of charging system problems requires a thorough understanding of the system components and their operation.

Operation

When the engine is running, battery power energizes the charging system and engine power drives it. The charging system then generates electricity for the vehicle's electrical systems. At low speeds with some electrical loads "on" (e.g., lights and window defogger), some battery current may still be needed. But, at high speeds, the charging system supplies all the current needed by the vehicle. Once those needs are taken care of, the charging system then sends current into the battery to restore its charge.



Toyota Charging Systems

Typical charging system components include:

IGNITION SWITCH
When the ignition switch is in the ON position, battery current energizes the alternator.

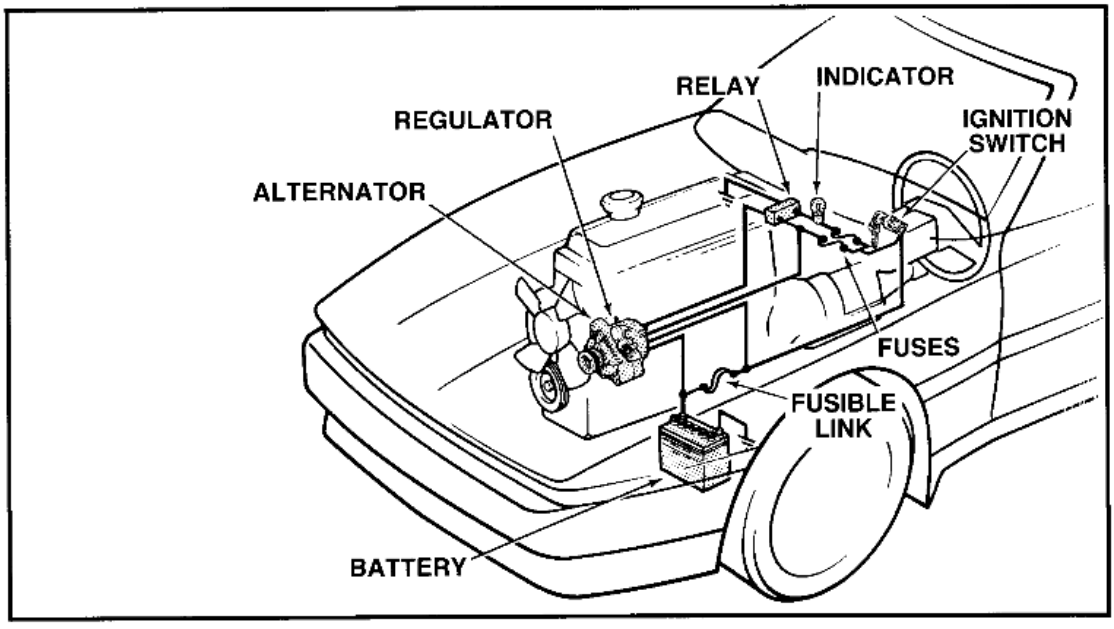
ALTERNATOR
Mechanical energy is transferred from the engine to the alternator by a grooved drive belt on a pulley arrangement. Through electromagnetic induction, the alternator changes this mechanical energy into electrical energy. The alternating current generated is converted into direct current by the rectifier, a set of diodes which allow current to pass in only one direction.

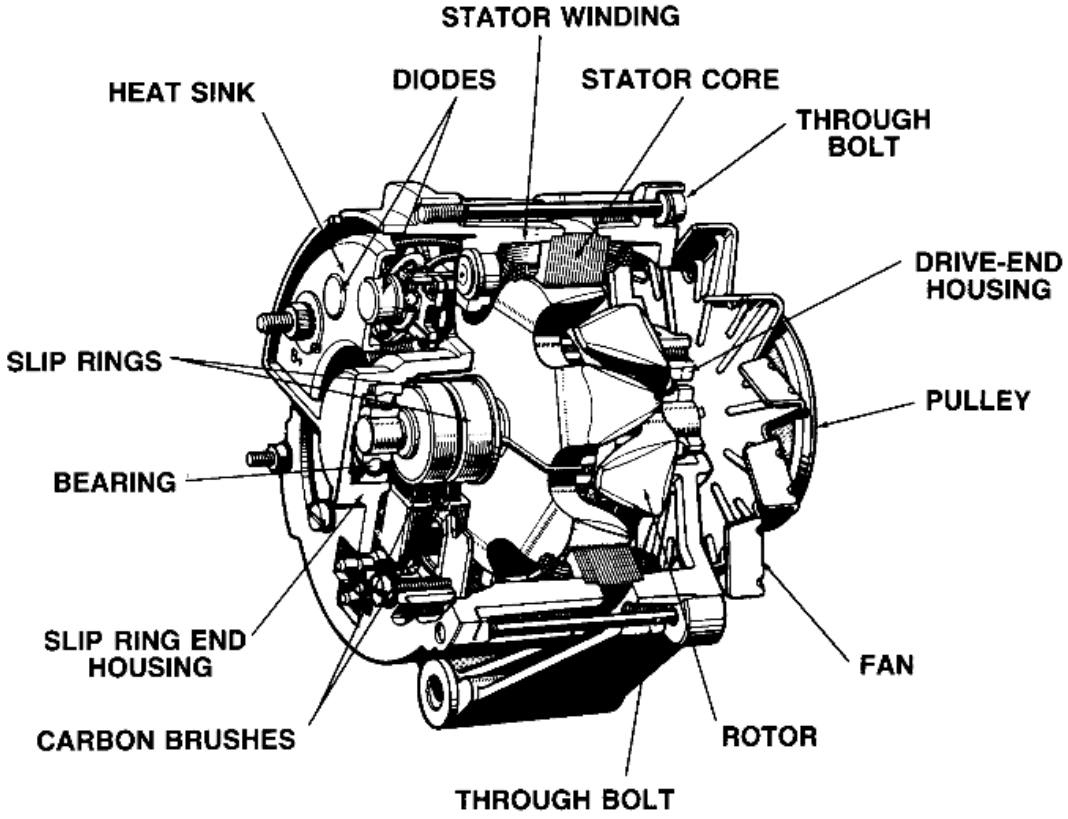
VOLTAGE REGULATOR
Without a regulator, the alternator will always operate at its highest output. This may damage certain components and overcharge the battery. The regulator controls the alternator output to prevent overcharging or undercharging. On older models, this is a separate electromechanical component which uses a coil and contact points to open and close the circuit to the alternator. On most models today, this is a built-in electronic device.

BATTERY
The battery supplies current to energize the alternator. During charging, the battery changes electrical energy from the alternator into chemical energy. The battery's active materials are restored. The battery also acts as a "shock absorber" or voltage stabilizer in the system to prevent damage to sensitive components in the vehicle's electrical system.

INDICATOR
The charging indicator device most commonly used on Toyotas is a simple ON/OFF warning lamp. It is normally off. It lights when the ignition is turned "on" for a check of the lamp circuit. And, it lights when the engine is running if the charging system is undercharging. A voltmeter is used on current Supra and Celica models to indicate system voltage ... it is connected in parallel with the battery. An ammeter in series with the battery was used on older Toyotas.

FUSING
A fusible link as well as separate fuses are used to protect
circuits in the charging system.



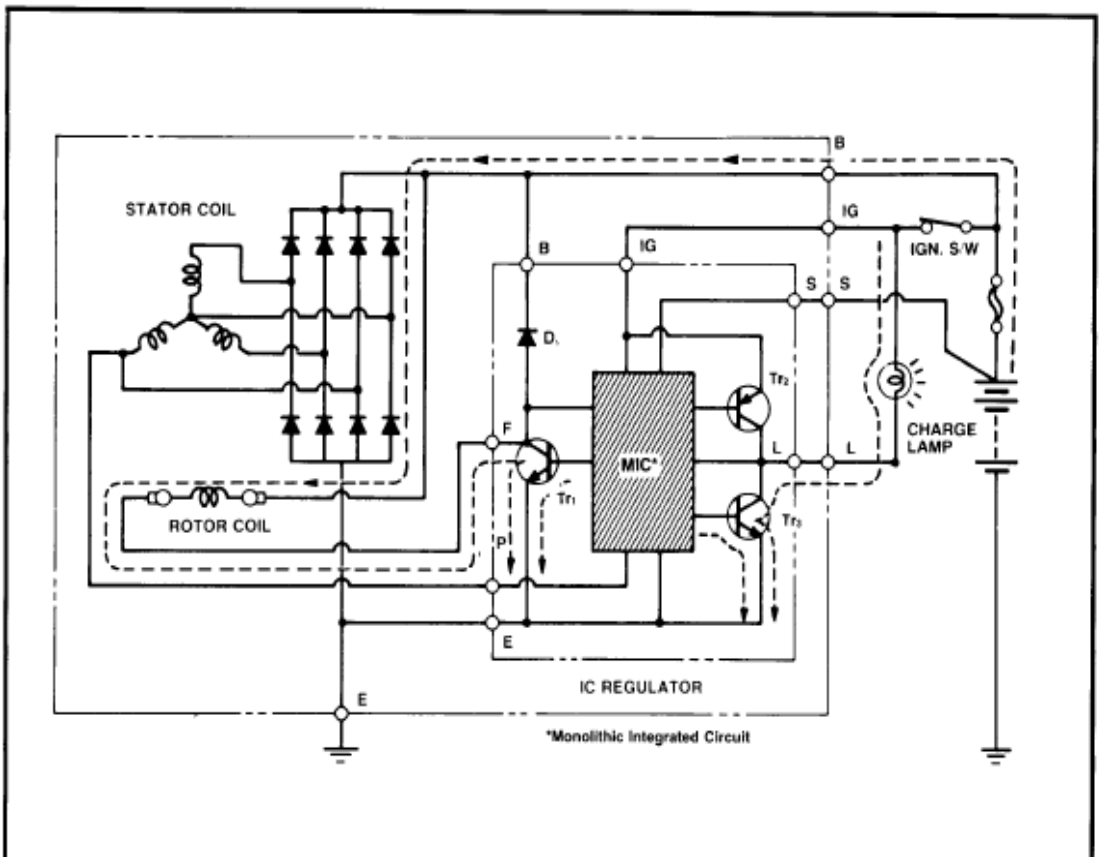

STATOR WINDING
HEAT SINK
DIODES
STATOR CORE
THROUGH BOLT
DRIVE-END HOUSING
SLIP RINGS
PULLEY
BEARING
SLIP RING END HOUSING
FAN
CARBON BRUSHES
ROTOR
THROUGH BOLT

Alternator Operation

GENERAL

The operation of the Toyota compact, high-speed alternator is shown in the following circuit diagrams.

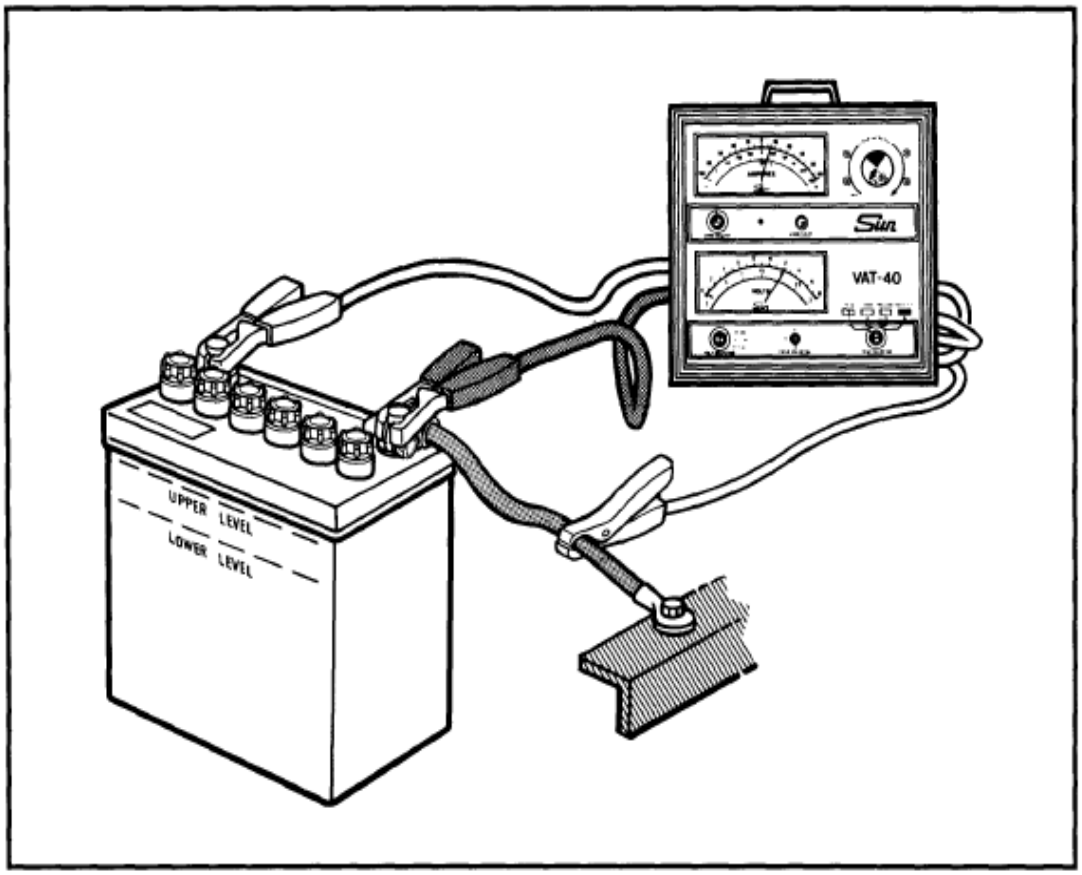
IGNITION ON, ENGINE STOPPED



ALTERNATOR OUTPUT TEST

The alternator output test checks the ability of the alternator to deliver its rated output of voltage and current. This test should be performed whenever an overcharging or undercharging problem is suspected. Output current and voltage should meet the specifications of the alternator. If not, the alternator or regulator (IC or external) may require replacement.

A Sun VAT-40 tester, similar testers, or a separate voltmeter and ammeter can be used. Toyota repair manuals detail the testing procedures with an ammeter and voltmeter. Follow the manufacturer's instructions when using special testers, although most are operated similarly. The following steps outline a typical procedure for performing the alternator output test using a Sun VAT-40:



Charging Without Load

1. Prepare the tester:

- Rotate the Load Increase control to OFF,
- Check each meter's mechanical zero. Adjust, if necessary.
- Connect the tester Load Leads to the battery terminals; RED to positive, BLACK to negative.
- Set Volt Selector to INT 18V.
- Set Test Selector to #2 CHARGING.
- Adjust ammeter to read ZERO using the electrical Zero Adjust control.
- Connect the clamp-on Amps Pickup around the battery ground (-) cables.

2. Turn the ignition switch to "ON" (engine not running) and read the amount of discharge on the ammeter. This is a base reading for current the alternator must supply for ignition and accessories **before** it can provide current to charge the battery.

NOTE: The reading should be about six amps.

3. Start the engine and adjust the speed to about 2000 rpm. Some models may require a different speed setting.

4. After about 3-4 minutes, read the ammeter and voltmeter. Add this ammeter reading and the reading found in step 2 (engine not running).

NOTE: The total current should be less than 10 amps. If it is more, the alternator may still be charging the battery. Once the battery is fully charged, you should get specified results.

The voltage should be within the specs for the alternator. This is usually between 13 and 15 volts. Refer to the appropriate repair manual. If the voltage is more than specified, replace the regulator. If the voltage is less than specified, ground the alternator field terminal "F" and check the voltmeter reading. This bypasses the regulator, so do not exceed the specified test speed. If the reading is still less than specified, check the alternator.

5. Remove ground from terminal "F."

Charging With Load

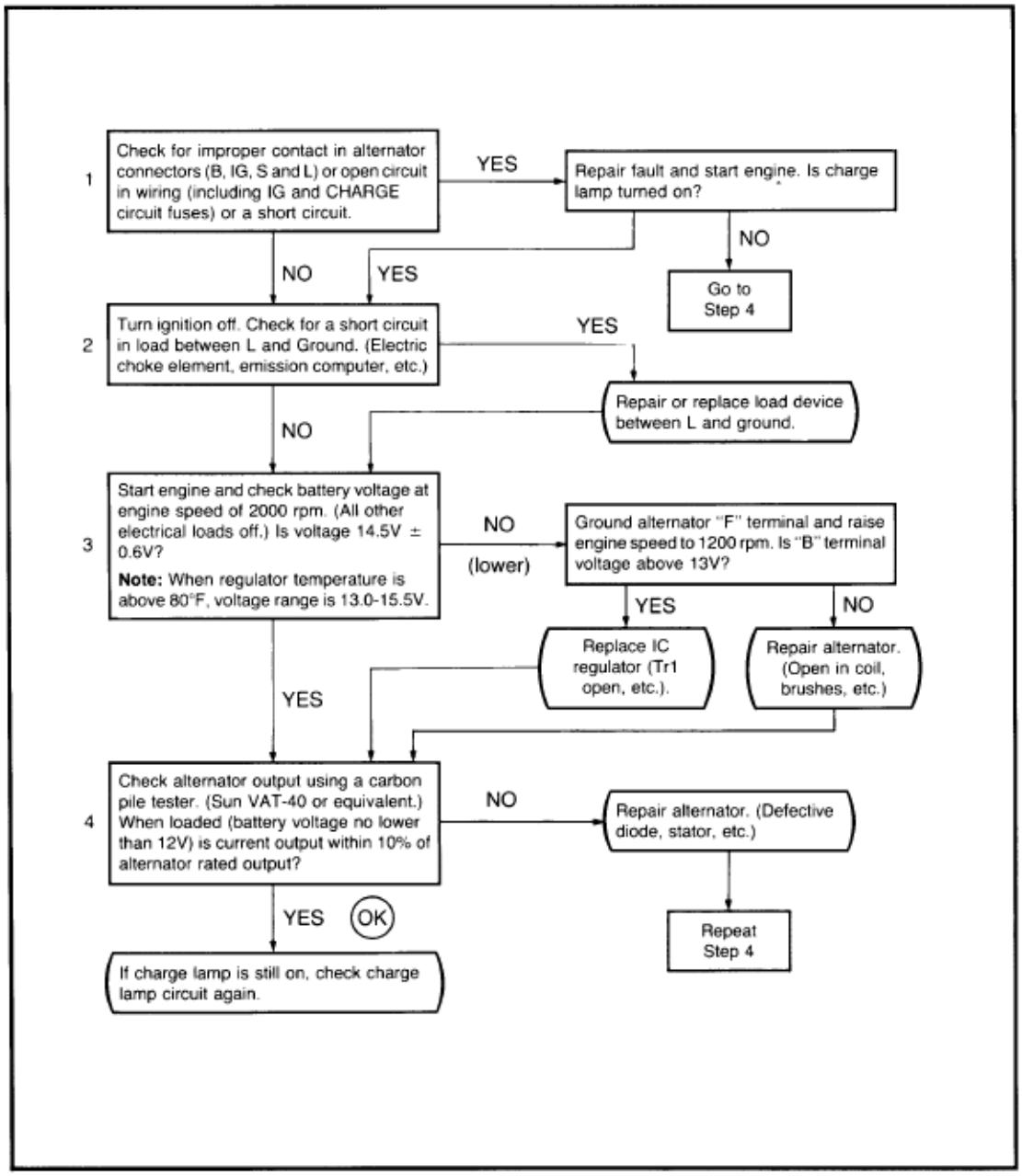
6. With the engine running at specified speed, adjust the Load Increase control to obtain the highest ammeter reading possible without causing the voltage to drop lower than 12 volts.

7. Read the ammeter.

NOTE: The reading should be within 10% of the alternator's rated output. If it is less, the alternator requires further testing or replacement.

TROUBLESHOOTING THE COMPACT, HIGH-SPEED ALTERNATOR.

Check Battery First!



APPENDIX B

Micro Hydro Potential in West Malaysia

Micro Hydro Potential in West Malaysia

Bil	State	No. of Sites	Total estimated available power (kW)
1	Johor	12	1687.9
2	Negeri Sembilan	17	848
3	Malacca	0	0
4	Selangor	2	343.8
5	Pahang	26	4835.1
6	Perak	34	9945.9
7	Kedah	5	496.7
8	Penang	0	0
9	Perlis	0	0
10	Kelantan	10	1420
11	Terengganu	3	829.9
			20407.3

Bil	Stream Name	Site Location	Available head,m	Catchment Area,km^2	Annual Flowrate,m^3/s	Available Power,kW	Possible Energy Demand
Bentong							
1	Sg.Tampik	Kg.Ceringing Hulu,Janda Baik	110	2	0.11	71.2	Alternative off – grid connection
2	Sg. Sum Sum	Kg. Sum Sum,Janda Baik	160	1	0.05	47.1	Alternative off grid connection
3	Sg.Leba	Orang Asli village of Kg. Sg.Leba	180	5	0.13	137.7	Off grid generation

Temerloh							
6	Sg.Galung	Orang asli Kg. Mentuh,Jenderak	80	4	0.1	47.1	Off grid generation
7	Sg.Rangit	Pusat latihan Gajah Kuala Gandah	120	5	0.13	91.8	Alternative off grid connection
Kuantan							
8	Sg.Jerangkang	Jerangkang waterfall	240	8	0.25	353.2	Alternative Off grid generation
Kuala Lipis							
9	Sg.Sempar	Orang asli Kg.Titum,Hulu Jelai	100	6	0.28	164.8	Off grid generation
10	Sg.Senuh	Orang asli Kg. Kuala Besuk,Hulu Jelai	80	3	0.14	65.9	Off grid generation
11.	Sg.Betau	Orang asli Kg.Cerung,Hulu Jelai	120	6	0.28	197.8	Off grid generation
12	Sg. Sinderut	Orang asli Kg.Sinderut,Hulu Jelai	240	8	0.32	452.1	Off grid generation
13	Sg. Rungak	Orang asli Kg.Shean,Hulu Jelai	140	6	0.28	230.7	Off grid generation

Rompin							
14	Sg. Air Besar	Kg.Tekek,Tioman island	260	3	0.126	192.8	Off grid generation
15	Sg.Lalang	Kg.Lalang, Tioman island	160	4	0.17	160.1	Off grid generation
16.	Sg.Paya	Kg.Paya, Tioman island	160	2	0.08	75.3	Off grid generation
17.	Sg.Nipah and Sg.Seriah	Tg.Nipah, Tioman island	120	7	0.29	204.8	Off grid generation
18.	Sg.Keliling	Kg.Juara, Tioman island	120	4	0.17	120.1	Off grid generation
19.	Sg.Mentawak	Kg.Juara, Tioman island	220	5	0.21	272	Off grid generation
20.	Sg.Asah	Kg. Asah, Tioman island	120	3	0.13	91.8	Off grid generation
21.	Sg.Raya	Kg.Mukut, Tioman island	160	6	0.25	235.4	Off grid generation
Cameron Highland							
22.	Sg. Terisu	Pos Terisu,orang asli settlement	80	10	0.43	202.5	Alternative off grid connection
23.	Sg.Menlock	Kg.Teji,Pos Telanuk,Ringlet	200	11	0.64	753.4	Off-grid connection
24.	Sg.Bertik	Kg.Rening,Ringlet	80	5	0.29	136.6	Off-grid connection
25.	Sg.Cai	Kg.Renglas,Pos Telanuk,Ringlet	100	7	0.41	241.3	Off-grid Connection
26.	Sg.Kelow	Pos Mensun,Ringlet	120	7	0.41	289.6	Off-grid Connection

APPENDIX C

PIC18F4550 Microcontroller and Addressing Modes

MICROCHIP **PIC18F2455/2550/4455/4550**

28/40/44-Pin, High-Performance, Enhanced Flash, USB Microcontrollers with nanoWatt Technology

Universal Serial Bus Features:

- USB V2.0 Compliant
- Low Speed (1.5 Mb/s) and Full Speed (12 Mb/s)
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- Supports up to 32 Endpoints (16 bidirectional)
- 1-Kbyte Dual Access RAM for USB
- On-Chip USB Transceiver with On-Chip Voltage Regulator
- Interface for Off-Chip USB Transceiver
- Streaming Parallel Port (SPP) for USB streaming transfers (40/44-pin devices only)

Power-Managed Modes:

- Run: CPU on, peripherals on
- Idle: CPU off, peripherals on
- Sleep: CPU off, peripherals off
- Idle mode currents down to 5.8 µA typical
- Sleep mode currents down to 0.1 µA typical
- Timer1 Oscillator: 1.1 µA typical, 32 kHz, 2V
- Watchdog Timer: 2.1 µA typical
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Four Crystal modes, including High Precision PLL for USB
- Two External Clock modes, up to 48 MHz
- Internal Oscillator Block:
  - 8 user-selectable frequencies, from 31 kHz to 8 MHz
  - User-tunable to compensate for frequency drift
- Secondary Oscillator using Timer1 @ 32 kHz
- Dual Oscillator options allow microcontroller and USB module to run at different clock speeds
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if any clock stops

Peripheral Highlights:

- High-Current Sink/Source: 25 mA/25 mA
- Three External Interrupts
- Four Timer modules (Timer0 to Timer3)
- Up to 2 Capture/Compare/PWM (CCP) modules:
  - Capture is 16-bit, max. resolution 5.2 ns (TCY/16)
  - Compare is 16-bit, max. resolution 83.3 ns (TCY)
  - PWM output: PWM resolution is 1 to 10-bit
- Enhanced Capture/Compare/PWM (ECCP) module:
  - Multiple output modes
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
- Enhanced USART module:
  - LIN bus support
- Master Synchronous Serial Port (MSSP) module supporting 3-wire SPI (all 4 modes) and I^2C™ Master and Slave modes
- 10-bit, up to 13-channel Analog-to-Digital Converter module (A/D) with Programmable Acquisition Time
- Dual Analog Comparators with Input Multiplexing

Special Microcontroller Features:

- C Compiler Optimized Architecture with optional Extended Instruction Set
- 100,000 Erase/Write Cycle Enhanced Flash Program Memory typical
- 1,000,000 Erase/Write Cycle Data EEPROM Memory typical
- Flash/Data EEPROM Retention: > 40 years
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 41 ms to 131s
- Programmable Code Protection
- Single-Supply 5V In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via two pins
- Optional dedicated ICD/ICSP port (44-pin devices only)
- Wide Operating Voltage Range (2.0V to 5.5V)

Device	Program Memory		Data Memory		I/O	10-Bit A/D (ch)	CCP/ECCP (PWM)	SPP	MSSP		EAUSART	Comparators	Timers 8/16-Bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)					SPI	Master I^2C™			
PIC18F2455	24K	12288	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F2550	32K	16384	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F4455	24K	12288	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3
PIC18F4550	32K	16384	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3

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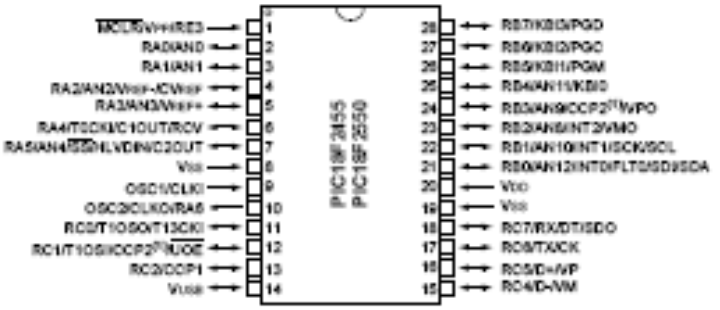
Pin Diagrams

28-Pin PDIP, SOIC



40-Pin PDIP

Note 1: RB3 is the alternate pin for CCP2 multiplexing.

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TABLE 1-1: DEVICE FEATURES

Features	PIC18F2455	PIC18F2550	PIC18F4455	PIC18F4550
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	24576	32768	24576	32768
Program Memory (Instructions)	12288	16384	12288	16384
Data Memory (Bytes)	2048	2048	2048	2048
Data EEPROM Memory (Bytes)	256	256	256	256
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/ Compare/PWM Modules	0	0	1	1
Serial Communications	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART
Universal Serial Bus (USB) Module	1	1	1	1
Streaming Parallel Port (SPP)	No	No	Yes	Yes
10-Bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Comparators	2	2	2	2
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT
Programmable Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled
Packages	28-pin PDIP 28-pin SOIC	28-pin PDIP 28-pin SOIC	40-pin PDIP 44-pin QFN 44-pin TQFP	40-pin PDIP 44-pin QFN 44-pin TQFP

TABLE 1-2: PIC18F2455/2550 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	PDIP, SOIC			
MCLR/VPP/RE3	1			Master Clear (input) or programming voltage (input).
MCLR		I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP		P		Programming voltage input.
RE3		I	ST	Digital input.
OSC1/CLKI	9			Oscillator crystal or external clock input.
OSC1		I	Analog	Oscillator crystal input or external clock source input.
CLKI		I	Analog	External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)
OSC2/CLKO/RA6	10			Oscillator crystal or clock output.
OSC2		O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO		O	—	In select modes, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6		I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

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TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTA is a bidirectional I/O port.
RA0/AN0	2	19	19			
RA0				I/O	TTL	Digital I/O.
AN0				I	Analog	Analog input 0.
RA1/AN1	3	20	20			
RA1				I/O	TTL	Digital I/O.
AN1				I	Analog	Analog input 1.
RA2/AN2/VREF-/CVREF	4	21	21			
RA2				I/O	TTL	Digital I/O.
AN2				I	Analog	Analog input 2.
VREF-				I	Analog	A/D reference voltage (low) input.
CVREF				O	Analog	Analog comparator reference output.
RA3/AN3/VREF+	5	22	22			
RA3				I/O	TTL	Digital I/O.
AN3				I	Analog	Analog input 3.
VREF+				I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/C1OUT/RCV	6	23	23			
RA4				I/O	ST	Digital I/O.
T0CKI				I	ST	Timer0 external clock input.
C1OUT				O	—	Comparator 1 output.
RCV				I	TTL	External USB transceiver RCV input.
RA5/AN4/$\overline{SS}$/HLVDIN/C2OUT	7	24	24			
RA5				I/O	TTL	Digital I/O.
AN4				I	Analog	Analog input 4.
$\overline{SS}$				I	TTL	SPI slave select input.
HLVDIN				I	Analog	High/Low-Voltage Detect input.
C2OUT				O	—	Comparator 2 output.
RA6	—	—	—	—	—	See the OSC2/CLKO/RA6 pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the $\overline{ICPRT}$ Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the $\overline{DEBUG}$ Configuration bit is cleared.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/AN12/INT0/FLT0/SDI/SDA	33	9	8			
RB0				I/O	TTL	Digital I/O.
AN12				I	Analog	Analog Input 12.
INT0				I	ST	External Interrupt 0.
FLT0				I	ST	Enhanced PWM Fault Input (ECCP1 module).
SDI				I	ST	SPI data in.
SDA				I/O	ST	I^2C™ data I/O.
RB1/AN10/INT1/SCK/SCL	34	10	9			
RB1				I/O	TTL	Digital I/O.
AN10				I	Analog	Analog Input 10.
INT1				I	ST	External Interrupt 1.
SCK				I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL				I/O	ST	Synchronous serial clock input/output for I^2C mode.
RB2/AN8/INT2/VMO	35	11	10			
RB2				I/O	TTL	Digital I/O.
AN8				I	Analog	Analog Input 8.
INT2				I	ST	External Interrupt 2.
VMO				O	—	External USB transceiver VMO output.
RB3/AN9/CCP2/VPO	36	12	11			
RB3				I/O	TTL	Digital I/O.
AN9				I	Analog	Analog Input 9.
CCP2(1)				I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
VPO				O	—	External USB transceiver VPO output.
RB4/AN11/KBI0/CSSPP	37	14	14			
RB4				I/O	TTL	Digital I/O.
AN11				I	Analog	Analog Input 11.
KBI0				I	TTL	Interrupt-on-change pin.
CSSPP				O	—	SPP chip select control output.
RB5/KBI1/PGM	38	15	15			
RB5				I/O	TTL	Digital I/O.
KBI1				I	TTL	Interrupt-on-change pin.
PGM				I/O	ST	Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC	39	16	16			
RB6				I/O	TTL	Digital I/O.
KBI2				I	TTL	Interrupt-on-change pin.
PGC				I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	40	17	17			
RB7				I/O	TTL	Digital I/O.
KBI3				I	TTL	Interrupt-on-change pin.
PGD				I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

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TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTC is a bidirectional I/O port.
RC0/T1OSO/T13CKI	15	34	32			
RC0				I/O	ST	Digital I/O.
T1OSO				O	—	Timer1 oscillator output.
T13CKI				I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2/ $\overline{UOE}$	16	35	35			
RC1				I/O	ST	Digital I/O.
T1OSI				I	CMOS	Timer1 oscillator input.
CCP2(2)				I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
$\overline{UOE}$				O	—	External USB transceiver $\overline{OE}$ output.
RC2/CCP1/P1A	17	36	36			
RC2				I/O	ST	Digital I/O.
CCP1				I/O	ST	Capture 1 input/Compare 1 output/PWM 1 output.
P1A				O	TTL	Enhanced CCP1 PWM output, channel A.
RC4/D-/VM	23	42	42			
RC4				I	TTL	Digital input.
D-				I/O	—	USB differential minus line (input/output).
VM				I	TTL	External USB transceiver VM input.
RC5/D+/VP	24	43	43			
RC5				I	TTL	Digital input.
D+				I/O	—	USB differential plus line (input/output).
VP				I	TTL	External USB transceiver VP input.
RC6/TX/CK	25	44	44			
RC6				I/O	ST	Digital I/O.
TX				O	—	EUSART asynchronous transmit.
CK				I/O	ST	EUSART synchronous clock (see RX/DT).
RC7/RX/DT/SDO	26	1	1			
RC7				I/O	ST	Digital I/O.
RX				I	ST	EUSART asynchronous receive.
DT				I/O	ST	EUSART synchronous data (see TX/CK).
SDO				O	—	SPI data out.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels; I = Input
O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the $\overline{ICPRT}$ Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the $\overline{DEBUG}$ Configuration bit is cleared.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTD is a bidirectional I/O port or a Streaming Parallel Port (SPP). These pins have TTL input buffers when the SPP module is enabled.
RD0/SPP0	19	38	38			
RD0				I/O	ST	Digital I/O.
SPP0				I/O	TTL	Streaming Parallel Port data.
RD1/SPP1	20	39	39			
RD1				I/O	ST	Digital I/O.
SPP1				I/O	TTL	Streaming Parallel Port data.
RD2/SPP2	21	40	40			
RD2				I/O	ST	Digital I/O.
SPP2				I/O	TTL	Streaming Parallel Port data.
RD3/SPP3	22	41	41			
RD3				I/O	ST	Digital I/O.
SPP3				I/O	TTL	Streaming Parallel Port data.
RD4/SPP4	27	2	2			
RD4				I/O	ST	Digital I/O.
SPP4				I/O	TTL	Streaming Parallel Port data.
RD5/SPP5/P1B	28	3	3			
RD5				I/O	ST	Digital I/O.
SPP5				I/O	TTL	Streaming Parallel Port data.
P1B				O	—	Enhanced CCP1 PWM output, channel B.
RD6/SPP6/P1C	29	4	4			
RD6				I/O	ST	Digital I/O.
SPP6				I/O	TTL	Streaming Parallel Port data.
P1C				O	—	Enhanced CCP1 PWM output, channel C.
RD7/SPP7/P1D	30	5	5			
RD7				I/O	ST	Digital I/O.
SPP7				I/O	TTL	Streaming Parallel Port data.
P1D				O	—	Enhanced CCP1 PWM output, channel D.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels; I = Input
O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the $\overline{\text{DEBUG}}$ Configuration bit is cleared.

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TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTE is a bidirectional I/O port.
RE0/AN5/CK1SPP	8	25	25			
RE0				I/O	ST	Digital I/O.
AN5				I	Analog	Analog input 5.
CK1SPP				O	—	SPP clock 1 output.
RE1/AN6/CK2SPP	9	26	26			
RE1				I/O	ST	Digital I/O.
AN6				I	Analog	Analog input 6.
CK2SPP				O	—	SPP clock 2 output.
RE2/AN7/OESPP	10	27	27			
RE2				I/O	ST	Digital I/O.
AN7				I	Analog	Analog input 7.
OESPP				O	—	SPP output enable output.
RE3	—	—	—	—	—	See $\overline{MCLR}$/VPP/RE3 pin.
VSS	12, 31	6, 30, 31	6, 29	P	—	Ground reference for logic and I/O pins.
VDD	11, 32	7, 8, 28, 29	7, 28	P	—	Positive supply for logic and I/O pins.
VUSB	18	37	37	O	—	Internal USB 3.3V voltage regulator output.
NC/ICCK/ICPGC(3)	—	—	12			No Connect or dedicated ICD/ICSP™ port clock.
ICCK				I/O	ST	In-Circuit Debugger clock.
ICPGC				I/O	ST	ICSP programming clock.
NC/ICDT/ICPGD(3)	—	—	13			No Connect or dedicated ICD/ICSP port clock.
ICDT				I/O	ST	In-Circuit Debugger data.
ICPGD				I/O	ST	ICSP programming data.
NC/$\overline{ICRST}$/ICVPP(3)	—	—	33			No Connect or dedicated ICD/ICSP port Reset.
$\overline{ICRST}$				I	—	Master Clear (Reset) input.
ICVPP				P	—	Programming voltage input.
NC/ICPORTS(3)	—	—	34	P	—	No Connect or 28-pin device emulation.
ICPORTS						Enable 28-pin device emulation when connected to VSS.
NC	—	13	—	—	—	No Connect.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the $\overline{DEBUG}$ Configuration bit is cleared.

5.2 PIC18 Instruction Cycle

5.2.1 CLOCKING SCHEME

The microcontroller clock input, whether from an internal or external source, is internally divided by four to generate four non-overlapping quadrature clocks (Q1, Q2, Q3 and Q4). Internally, the program counter is incremented on every Q1; the instruction is fetched from the program memory and latched into the Instruction Register (IR) during Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 5-3.

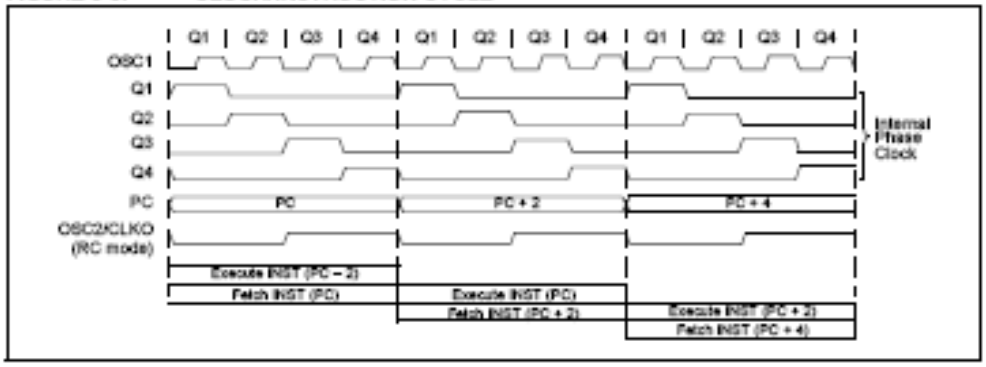
5.2.2 INSTRUCTION FLOW/PIPELINING

An "Instruction Cycle" consists of four Q cycles: Q1 through Q4. The instruction fetch and execute are pipelined in such a manner that a fetch takes one instruction cycle, while the decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 5-3).

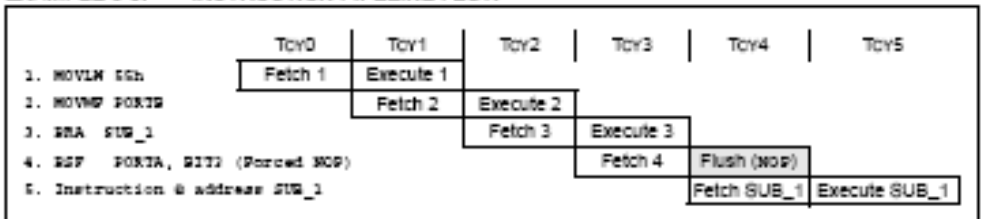
A fetch cycle begins with the Program Counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 5-3: CLOCK/INSTRUCTION CYCLE



EXAMPLE 5-3: INSTRUCTION PIPELINE FLOW



Note: All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

APPENDIX D

Programming of Charge Controller

```
DEFINE OSC 4

define ADC_bits 8

define ADC_CLOCK 3

DEFINE ADC_SAMPLEUS 50


DEFINE LCD_DREG PORTB ' Set LCD data port to PORTB

DEFINE LCD_DBIT 4 ' Set data starting bit to 4

DEFINE LCD_RSREG PORTB' Set RS register port to PORTB

DEFINE LCD_RSBIT 3 ' Set RS register bit to 3

DEFINE LCD_EREG PORTB 'Set E register port

DEFINE LCD_EBIT 0 'Set E register bit to 0

DEFINE LCD_BITS 4 ' Set 4 bit operation

DEFINE LCD_LINES 2 ' Set number of LCD rows

define LCD_COMMANDUS 2000

DEFINE LCD_DATAUS 255


''START GREETING''

PAUSE 1000

LCDOUT $FE,2,"    VOLTAGE  "

lcdout $FE,$C0, "    DETECTED   "

PAUSE 3000

LCDOUT $FE,1 'LCD CLEAR


LED var PORTD
```

```
OUTPUT PORTD.1

OUTPUT PORTD.2

OUTPUT PORTD.3

output PORTB.0

output PORTB.3

output PORTB.4

output PORTB.5

output PORTB.6

output PORTB.7


'i var byte

'j VAR BYTE


Res1 var word

Res var word

volts1 var word

volts2 var word



conv1 con 19

conv2 con 61
```

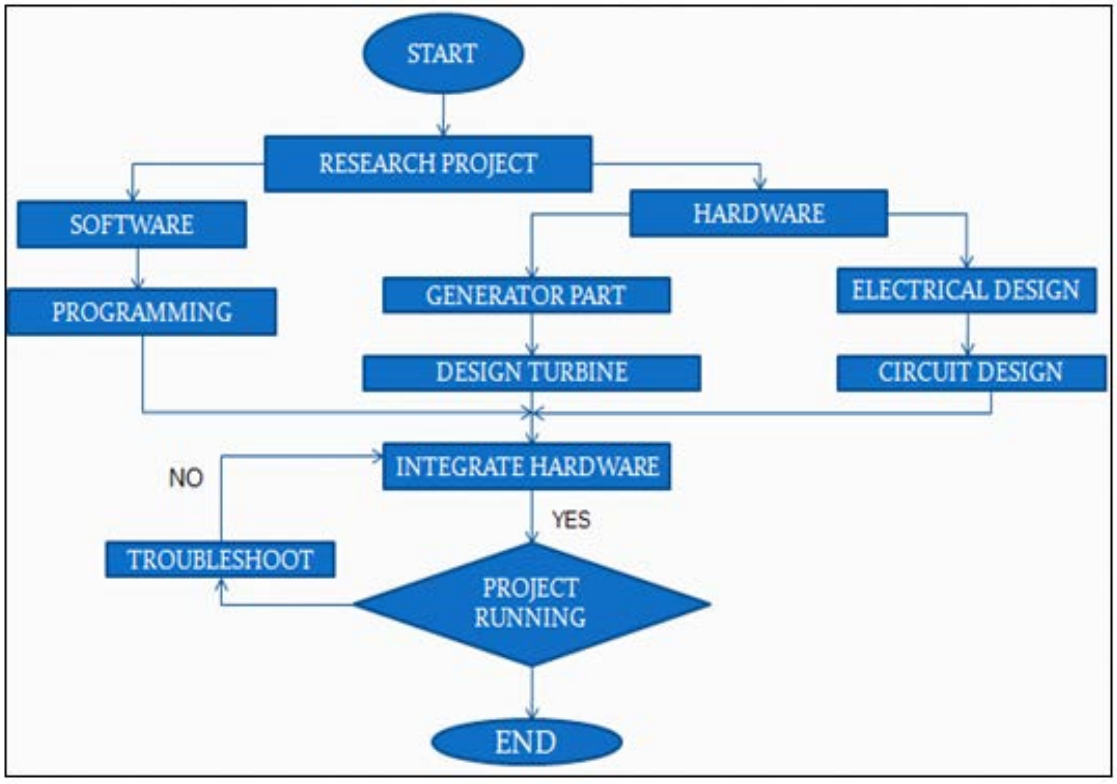
```
ADCON1 = %1110 'setting AN0 as analogue input
Pause 1000

ADCIN 0, res 'ANO -> Res
'ADCIN 1, RES1




LOOP:


if ( rES < 228) then
'    lcdout $FE,1
   lcdout $FE,2, "         30%"
          Lcdout $FE,$C0, "Battery Charging"
   PAUSE 1000
   HIGH PORTD.3  'RED LIGHT
   LOW PORTD.1
   LOW PORTD.2
   GOTO LOOP1
   pause 2000
   GOTO LOOP
endif
```

```
if  (RES => 255) theN
   lcdout $FE,1
   lcdout $FE,2, "        100% "
   lcdout $FE,$C0, " VOLTAGE FULL "
   PAUSE 1000
   HIGH PORTD.1 'GREEN LIGHT
   LOW PORTD.2
   LOW PORTD.3
   GOTO LOOP1
   pause 2000
   goto loop
ENDIF


LOOP2:
if  ( 229 <= RES <= 244) then
   lcdout $FE,1
   lcdout $FE,2, "         60%"
   Lcdout $FE,$C0, "VOLTAGE LOW"
   PAUSE 1000
   HIGH PORTD.2 'YELLOW LIGHT
   LOW PORTD.1
   LOW PORTD.3
   GOTO LOOP1
```

```
   pause 2000
   GOTO LOOP
endif

GOTO LOOP



ADCIN 0,RES
LOOP1:

Volts1 = Res / conv1
Volts2 = Res / Conv2
Volts2 = Volts2 / 100
Volts1 = volts1 + volts2
LCDOUT $FE,2,"V = " ,dec2 volts1, "V"
pause 1000
'goto loop



end
```

APPENDIX E

Flow Chart


START
RESEARCH PROJECT
SOFTWARE
HARDWARE
PROGRAMMING
GENERATOR PART
ELECTRICAL DESIGN
DESIGN TURBINE
CIRCUIT DESIGN
INTEGRATE HARDWARE
NO
YES
TROUBLESHOOT
PROJECT RUNNING
END

REFERENCES

1 Mitja Koprivsek, *Development Trend of Residual Current Circuit Breakers, IEC 1008-1- Residual current operated circuit breakers,* grad. Eng. Of el. Eng. ETI d.d. Izlake. 2004

2 SABS 767 - *Earth Leakage Protection Units,* 1982

3 "Elektron*", ELECTRICAL SHOCK AND FIRE HAZARD PROTECTION CONQUERING THE LIMITATIONS.* September 1993.

4 Alvarion. *Lightning Protection*. (1-21) October 2005

5 Indo asian fusegear ltd. *Stopshock Residual Current Circuit Breaker*. (1-8) 2000

6 Suruhanjaya Tenaga. *Prohibition on The Use Of Voltage Operand Earth Leakage Circuit Breaker (ELCB).* Tuesday, 13 March 2007

APPENDIX A

AR-ELCB Programming

EARTH LEAKAGE CIRCUIT BREAKER WITH AN AUTO RE-CLOSER UNIT PROGRAMMING USING PICBASIC (MICROCODE STUDIO)

```
DEFINE OSC 20

DEFINE LCD_DREG PORTB
DEFINE LCD_DBIT 4
DEFINE LCD_RSREG PORTB
DEFINE LCD_RSBIT 3
DEFINE LCD_EREG PORTB
DEFINE LCD_EBIT 0
DEFINE LCD_BITS 4
DEFINE LCD_LINES 2
DEFINE LCD_COMMANDUS 2000
DEFINE LCD_DATAUS 255

' Define ADCIN parameters
Define ADC_BITS 8 ' Set number of bits in result
Define ADC_CLOCK 3 ' Set clock source (3=rc)
Define ADC_SAMPLEUS 50 ' Set sampling time in uS

data1 var byte
i var byte
j var byte
adcon1=$0e
trisa= %00111111
trisb= %00100000
trisd= %00000000


   main:
```

```
    pause 1000
    lcdout $fe,$80+4, "Tarmizi"
    lcdout $fe,$c0+4, "EC 05004"

    pause 1000
    lcdout $fe,1

    lcdout $fe,$80+1, "ELCB with Auto"
    lcdout $fe,$c0+1, "Re-Closer Unit"

    pause 1000
    lcdout $fe,1

    i=0
    j=0
loop:
       adcin 0,data1

       if data1>$40 then
          low portb.2
          HIGH Portd.1
          lcdout $fe,1
          lcdout $fe,$80+2, "Protection Off"
          lcdout $fe,$c0, "Fault:Overcurent"
          pause 1000
          i=i+1
          if i=3 then goto stop1

       else

          high portb.2
```

```
                low portd.1
                lcdout $fe,1
                lcdout $fe,$80+2, "Protection ON"
                lcdout $fe,$c0+2, "Fault: None"
                pause 1000
                j=j+1
                if j>5 then i=0
'               count portd.2,5000,timer1
'               if timer1>5000 then i=0

           endif

    goto loop
stop1:
end
```

APPENDIX B

PIC18F4550 Microcontroller, Addressing Modes, and Instruction Set

PIC18F4550 MICROCONTROLLER, ADDRESSING MODES AND INSTRUCTION SET

MICROCHIP **PIC18F2455/2550/4455/4550**

28/40/44-Pin, High-Performance, Enhanced Flash, USB Microcontrollers with nanoWatt Technology

Universal Serial Bus Features:

- USB V2.0 Compliant
- Low Speed (1.5 Mb/s) and Full Speed (12 Mb/s)
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- Supports up to 32 Endpoints (16 bidirectional)
- 1-Kbyte Dual Access RAM for USB
- On-Chip USB Transceiver with On-Chip Voltage Regulator
- Interface for Off-Chip USB Transceiver
- Streaming Parallel Port (SPP) for USB streaming transfers (40/44-pin devices only)

Power-Managed Modes:

- Run: CPU on, peripherals on
- Idle: CPU off, peripherals on
- Sleep: CPU off, peripherals off
- Idle mode currents down to 5.8 µA typical
- Sleep mode currents down to 0.1 µA typical
- Timer1 Oscillator: 1.1 µA typical, 32 kHz, 2V
- Watchdog Timer: 2.1 µA typical
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Four Crystal modes, including High Precision PLL for USB
- Two External Clock modes, up to 48 MHz
- Internal Oscillator Block:
  - 8 user-selectable frequencies, from 31 kHz to 8 MHz
  - User-tunable to compensate for frequency drift
- Secondary Oscillator using Timer1 @ 32 kHz
- Dual Oscillator options allow microcontroller and USB module to run at different clock speeds
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if any clock stops

Peripheral Highlights:

- High-Current Sink/Source: 25 mA/25 mA
- Three External Interrupts
- Four Timer modules (Timer0 to Timer3)
- Up to 2 Capture/Compare/PWM (CCP) modules:
  - Capture is 16-bit, max. resolution 5.2 ns (TCY/16)
  - Compare is 16-bit, max. resolution 83.3 ns (TCY)
  - PWM output: PWM resolution is 1 to 10-bit
- Enhanced Capture/Compare/PWM (ECCP) module:
  - Multiple output modes
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
- Enhanced USART module:
  - LIN bus support
- Master Synchronous Serial Port (MSSP) module supporting 3-wire SPI (all 4 modes) and I^2C™ Master and Slave modes
- 10-bit, up to 13-channel Analog-to-Digital Converter module (A/D) with Programmable Acquisition Time
- Dual Analog Comparators with Input Multiplexing

Special Microcontroller Features:

- C Compiler Optimized Architecture with optional Extended Instruction Set
- 100,000 Erase/Write Cycle Enhanced Flash Program Memory typical
- 1,000,000 Erase/Write Cycle Data EEPROM Memory typical
- Flash/Data EEPROM Retention: > 40 years
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 41 ms to 131s
- Programmable Code Protection
- Single-Supply 5V In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via two pins
- Optional dedicated ICD/ICSP port (44-pin devices only)
- Wide Operating Voltage Range (2.0V to 5.5V)

Device	Program Memory		Data Memory		I/O	10-Bit A/D (ch)	CCP/ECCP (PWM)	SPP	MSSP		EAUSART	Comparators	Timers 8/16-Bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)					SPI	Master I^2C™			
PIC18F2455	24K	12288	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F2550	32K	16384	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F4455	24K	12288	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3
PIC18F4550	32K	16384	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3

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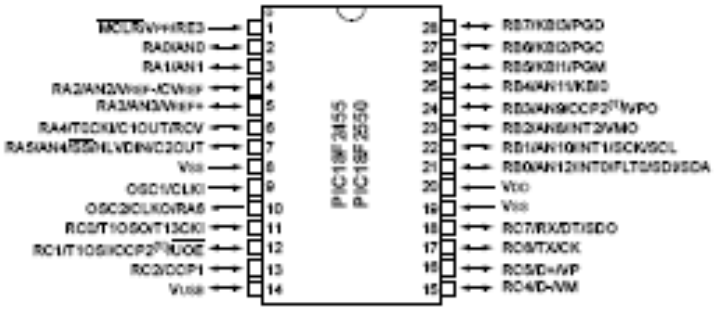
Pin Diagrams

28-Pin PDIP, SOIC



40-Pin PDIP

Note 1: RB3 is the alternate pin for CCP2 multiplexing.

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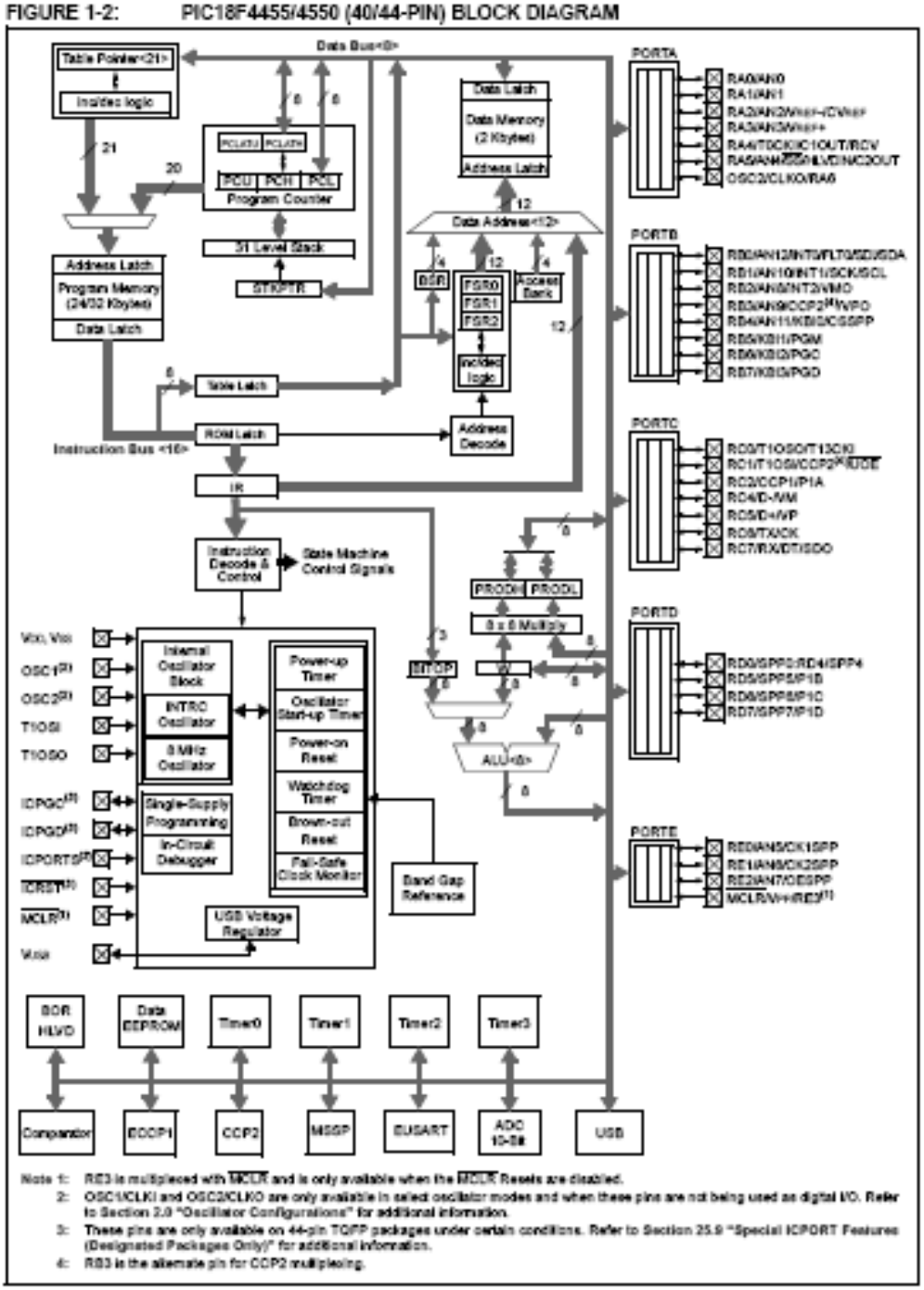
TABLE 1-1: DEVICE FEATURES

Features	PIC18F2455	PIC18F2550	PIC18F4455	PIC18F4550
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	24576	32768	24576	32768
Program Memory (Instructions)	12288	16384	12288	16384
Data Memory (Bytes)	2048	2048	2048	2048
Data EEPROM Memory (Bytes)	256	256	256	256
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/ Compare/PWM Modules	0	0	1	1
Serial Communications	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART
Universal Serial Bus (USB) Module	1	1	1	1
Streaming Parallel Port (SPP)	No	No	Yes	Yes
10-Bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Comparators	2	2	2	2
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT
Programmable Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled
Packages	28-pin PDIP 28-pin SOIC	28-pin PDIP 28-pin SOIC	40-pin PDIP 44-pin QFN 44-pin TQFP	40-pin PDIP 44-pin QFN 44-pin TQFP

FIGURE 1-2: PIC18F4455/4550 (40/44-PIN) BLOCK DIAGRAM



Note 1: RE3 is multiplexed with MCLR and is only available when the MCLR Resets are disabled.
2: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. Refer to Section 2.0 "Oscillator Configurations" for additional information.
3: These pins are only available on 44-pin TQFP packages under certain conditions. Refer to Section 25.9 "Special ICPORT Features (Designated Packages Only)" for additional information.
4: RB3 is the alternate pin for CCP2 multiplexing.

TABLE 1-2: PIC18F2455/2550 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	PDIP, SOIC			
$\overline{MCLR}$/VPP/RE3	1			Master Clear (input) or programming voltage (input).
$\overline{MCLR}$		I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP		P		Programming voltage input.
RE3		I	ST	Digital input.
OSC1/CLKI	9			Oscillator crystal or external clock input.
OSC1		I	Analog	Oscillator crystal input or external clock source input.
CLKI		I	Analog	External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)
OSC2/CLKO/RA6	10			Oscillator crystal or clock output.
OSC2		O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO		O	—	In select modes, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6		I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

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TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
MCLR/VPP/RE3	1	18	18			Master Clear (Input) or programming voltage (Input).
MCLR				I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP				P		Programming voltage input.
RE3				I	ST	Digital input.
OSC1/CLKI	13	32	30			Oscillator crystal or external clock input.
OSC1				I	Analog	Oscillator crystal input or external clock source input.
CLKI				I	Analog	External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)
OSC2/CLKO/RA6	14	33	31			Oscillator crystal or clock output.
OSC2				O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO				O	—	In RC mode, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6				I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels; I = Input
O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.
2: Default assignment for CCP2 when CCP2MX Configuration bit is set.
3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

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TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTA is a bidirectional I/O port.
RA0/AN0	2	19	19			
RA0				I/O	TTL	Digital I/O.
AN0				I	Analog	Analog input 0.
RA1/AN1	3	20	20			
RA1				I/O	TTL	Digital I/O.
AN1				I	Analog	Analog input 1.
RA2/AN2/VREF-/CVREF	4	21	21			
RA2				I/O	TTL	Digital I/O.
AN2				I	Analog	Analog input 2.
VREF-				I	Analog	A/D reference voltage (low) input.
CVREF				O	Analog	Analog comparator reference output.
RA3/AN3/VREF+	5	22	22			
RA3				I/O	TTL	Digital I/O.
AN3				I	Analog	Analog input 3.
VREF+				I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/C1OUT/RCV	6	23	23			
RA4				I/O	ST	Digital I/O.
T0CKI				I	ST	Timer0 external clock input.
C1OUT				O	—	Comparator 1 output.
RCV				I	TTL	External USB transceiver RCV input.
RA5/AN4/$\overline{SS}$/HLVDIN/C2OUT	7	24	24			
RA5				I/O	TTL	Digital I/O.
AN4				I	Analog	Analog input 4.
$\overline{SS}$				I	TTL	SPI slave select input.
HLVDIN				I	Analog	High/Low-Voltage Detect input.
C2OUT				O	—	Comparator 2 output.
RA6	—	—	—	—	—	See the OSC2/CLKO/RA6 pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/AN12/INT0/ FLT0/SDI/SDA	33	9	8			
RB0				I/O	TTL	Digital I/O.
AN12				I	Analog	Analog input 12.
INT0				I	ST	External interrupt 0.
FLT0				I	ST	Enhanced PWM Fault input (ECCP1 module).
SDI				I	ST	SPI data in.
SDA				I/O	ST	I^2C™ data I/O.
RB1/AN10/INT1/SCK/ SCL	34	10	9			
RB1				I/O	TTL	Digital I/O.
AN10				I	Analog	Analog input 10.
INT1				I	ST	External interrupt 1.
SCK				I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL				I/O	ST	Synchronous serial clock input/output for I^2C mode.
RB2/AN8/INT2/VMO	35	11	10			
RB2				I/O	TTL	Digital I/O.
AN8				I	Analog	Analog input 8.
INT2				I	ST	External interrupt 2.
VMO				O	—	External USB transceiver VMO output.
RB3/AN9/CCP2/VPO	36	12	11			
RB3				I/O	TTL	Digital I/O.
AN9				I	Analog	Analog input 9.
CCP2(1)				I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
VPO				O	—	External USB transceiver VPO output.
RB4/AN11/KBI0/CSSPP	37	14	14			
RB4				I/O	TTL	Digital I/O.
AN11				I	Analog	Analog input 11.
KBI0				I	TTL	Interrupt-on-change pin.
CSSPP				O	—	SPP chip select control output.
RB5/KBI1/PGM	38	15	15			
RB5				I/O	TTL	Digital I/O.
KBI1				I	TTL	Interrupt-on-change pin.
PGM				I/O	ST	Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC	39	16	16			
RB6				I/O	TTL	Digital I/O.
KBI2				I	TTL	Interrupt-on-change pin.
PGC				I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	40	17	17			
RB7				I/O	TTL	Digital I/O.
KBI3				I	TTL	Interrupt-on-change pin.
PGD				I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

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TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTC is a bidirectional I/O port.
RC0/T1OSO/T13CKI	15	34	32			
RC0				I/O	ST	Digital I/O.
T1OSO				O	—	Timer1 oscillator output.
T13CKI				I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2/ UOE	16	35	35			
RC1				I/O	ST	Digital I/O.
T1OSI				I	CMOS	Timer1 oscillator input.
CCP2(2)				I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
$\overline{UOE}$				O	—	External USB transceiver $\overline{OE}$ output.
RC2/CCP1/P1A	17	36	36			
RC2				I/O	ST	Digital I/O.
CCP1				I/O	ST	Capture 1 input/Compare 1 output/PWM 1 output.
P1A				O	TTL	Enhanced CCP1 PWM output, channel A.
RC4/D-/VM	23	42	42			
RC4				I	TTL	Digital input.
D-				I/O	—	USB differential minus line (input/output).
VM				I	TTL	External USB transceiver VM input.
RC5/D+/VP	24	43	43			
RC5				I	TTL	Digital input.
D+				I/O	—	USB differential plus line (input/output).
VP				I	TTL	External USB transceiver VP input.
RC6/TX/CK	25	44	44			
RC6				I/O	ST	Digital I/O.
TX				O	—	EUSART asynchronous transmit.
CK				I/O	ST	EUSART synchronous clock (see RX/DT).
RC7/RX/DT/SDO	26	1	1			
RC7				I/O	ST	Digital I/O.
RX				I	ST	EUSART asynchronous receive.
DT				I/O	ST	EUSART synchronous data (see TX/CK).
SDO				O	—	SPI data out.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the $\overline{ICPRT}$ Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the $\overline{DEBUG}$ Configuration bit is cleared.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTD is a bidirectional I/O port or a Streaming Parallel Port (SPP). These pins have TTL input buffers when the SPP module is enabled.
RD0/SPP0	19	38	38			
RD0				I/O	ST	Digital I/O.
SPP0				I/O	TTL	Streaming Parallel Port data.
RD1/SPP1	20	39	39			
RD1				I/O	ST	Digital I/O.
SPP1				I/O	TTL	Streaming Parallel Port data.
RD2/SPP2	21	40	40			
RD2				I/O	ST	Digital I/O.
SPP2				I/O	TTL	Streaming Parallel Port data.
RD3/SPP3	22	41	41			
RD3				I/O	ST	Digital I/O.
SPP3				I/O	TTL	Streaming Parallel Port data.
RD4/SPP4	27	2	2			
RD4				I/O	ST	Digital I/O.
SPP4				I/O	TTL	Streaming Parallel Port data.
RD5/SPP5/P1B	28	3	3			
RD5				I/O	ST	Digital I/O.
SPP5				I/O	TTL	Streaming Parallel Port data.
P1B				O	—	Enhanced CCP1 PWM output, channel B.
RD6/SPP6/P1C	29	4	4			
RD6				I/O	ST	Digital I/O.
SPP6				I/O	TTL	Streaming Parallel Port data.
P1C				O	—	Enhanced CCP1 PWM output, channel C.
RD7/SPP7/P1D	30	5	5			
RD7				I/O	ST	Digital I/O.
SPP7				I/O	TTL	Streaming Parallel Port data.
P1D				O	—	Enhanced CCP1 PWM output, channel D.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels; I = Input
O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.
2: Default assignment for CCP2 when CCP2MX Configuration bit is set.
3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the $\overline{\text{DEBUG}}$ Configuration bit is cleared.

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TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTE is a bidirectional I/O port.
RE0/AN5/CK1SPP	8	25	25			
RE0				I/O	ST	Digital I/O.
AN5				I	Analog	Analog input 5.
CK1SPP				O	—	SPP clock 1 output.
RE1/AN6/CK2SPP	9	26	26			
RE1				I/O	ST	Digital I/O.
AN6				I	Analog	Analog input 6.
CK2SPP				O	—	SPP clock 2 output.
RE2/AN7/OESPP	10	27	27			
RE2				I/O	ST	Digital I/O.
AN7				I	Analog	Analog input 7.
OESPP				O	—	SPP output enable output.
RE3	—	—	—	—	—	See $\overline{MCLR}$/VPP/RE3 pin.
VSS	12, 31	6, 30, 31	6, 29	P	—	Ground reference for logic and I/O pins.
VDD	11, 32	7, 8, 28, 29	7, 28	P	—	Positive supply for logic and I/O pins.
VUSB	18	37	37	O	—	Internal USB 3.3V voltage regulator output.
NC/ICCK/ICPGC(3)	—	—	12			No Connect or dedicated ICD/ICSP™ port clock.
ICCK				I/O	ST	In-Circuit Debugger clock.
ICPGC				I/O	ST	ICSP programming clock.
NC/ICDT/ICPGD(3)	—	—	13			No Connect or dedicated ICD/ICSP port clock.
ICDT				I/O	ST	In-Circuit Debugger data.
ICPGD				I/O	ST	ICSP programming data.
NC/$\overline{ICRST}$/ICVPP(3)	—	—	33			No Connect or dedicated ICD/ICSP port Reset.
$\overline{ICRST}$				I	—	Master Clear (Reset) input.
ICVPP				P	—	Programming voltage input.
NC/ICPORTS(3)	—	—	34	P	—	No Connect or 28-pin device emulation.
ICPORTS						Enable 28-pin device emulation when connected to VSS.
NC	—	13	—	—	—	No Connect.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

2.0 OSCILLATOR CONFIGURATIONS

2.1 Overview

Devices in the PIC18F2455/2550/4455/4550 family incorporate a different oscillator and microcontroller clock system than previous PIC18F devices. The addition of the USB module, with its unique requirements for a stable clock source, make it necessary to provide a separate clock source that is compliant with both USB low-speed and full-speed specifications.

To accommodate these requirements, PIC18F2455/2550/4455/4550 devices include a new clock branch to provide a 48 MHz clock for full-speed USB operation. Since it is driven from the primary clock source, an additional system of prescalers and postscalers has been added to accommodate a wide range of oscillator frequencies. An overview of the oscillator structure is shown in Figure 2-1.

Other oscillator features used in PIC18 enhanced microcontrollers, such as the Internal oscillator block and clock switching, remain the same. They are discussed later in this chapter.

2.1.1 OSCILLATOR CONTROL

The operation of the oscillator in PIC18F2455/2550/4455/4550 devices is controlled through two Configuration registers and two control registers. Configuration registers, CONFIG1L and CONFIG1H, select the oscillator mode and USB prescaler/postscaler options. As Configuration bits, these are set when the device is programmed and left in that configuration until the device is reprogrammed.

The OSCCON register (Register 2-2) selects the Active Clock mode; it is primarily used in controlling clock switching in power-managed modes. Its use is discussed in **Section 2.4.1 "Oscillator Control Register"**.

The OSCTUNE register (Register 2-1) is used to trim the INTRC frequency source, as well as select the low-frequency clock source that drives several special features. Its use is described in **Section 2.2.6.2 "OSCTUNE Register"**.

2.2 Oscillator Types

PIC18F2455/2550/4455/4550 devices can be operated in twelve distinct oscillator modes. In contrast with previous PIC18 enhanced microcontrollers, four of these modes involve the use of two oscillator types at once. Users can program the FOSC3:FOSC0 Configuration bits to select one of these modes:

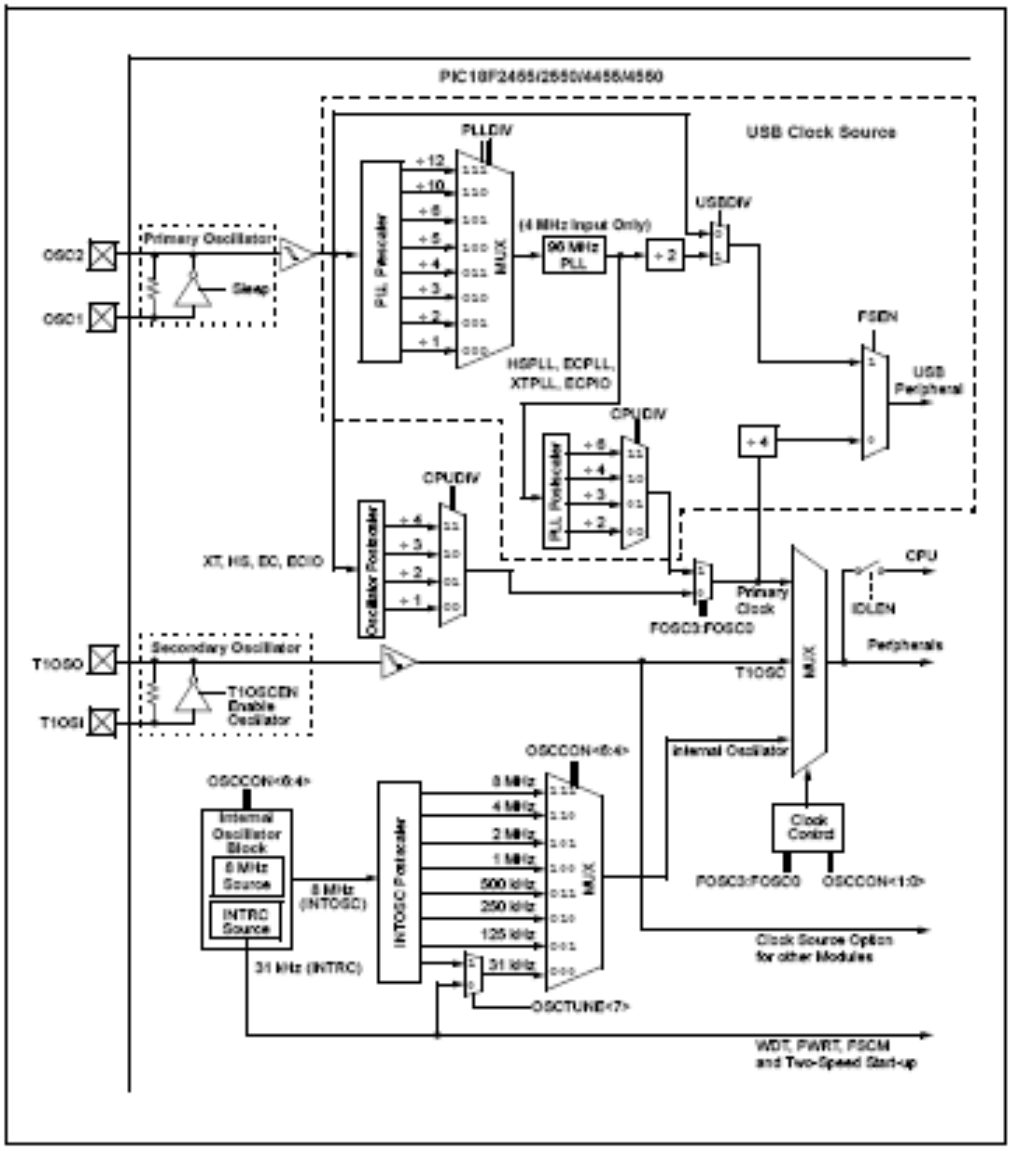
1. XT Crystal/Resonator
2. XTPLL Crystal/Resonator with PLL enabled
3. HS High-Speed Crystal/Resonator
4. HSPLL High-Speed Crystal/Resonator with PLL enabled
5. EC External Clock with Fosc/4 output
6. ECIO External Clock with I/O on RA6
7. ECPLL External Clock with PLL enabled and Fosc/4 output on RA6
8. ECPIO External Clock with PLL enabled, I/O on RA6
9. INTHS Internal Oscillator used as microcontroller clock source, HS Oscillator used as USB clock source
10. INTXT Internal Oscillator used as microcontroller clock source, XT Oscillator used as USB clock source
11. INTIO Internal Oscillator used as microcontroller clock source, EC Oscillator used as USB clock source, digital I/O on RA6
12. INTCKO Internal Oscillator used as microcontroller clock source, EC Oscillator used as USB clock source, Fosc/4 output on RA6

2.2.1 OSCILLATOR MODES AND USB OPERATION

Because of the unique requirements of the USB module, a different approach to clock operation is necessary. In previous PIC® devices, all core and peripheral clocks were driven by a single oscillator source; the usual sources were primary, secondary or the internal oscillator. With PIC18F2455/2550/4455/4550 devices, the primary oscillator becomes part of the USB module and cannot be associated to any other clock source. Thus, the USB module must be clocked from the primary clock source; however, the microcontroller core and other peripherals can be separately clocked from the secondary or internal oscillators as before.

Because of the timing requirements imposed by USB, an internal clock of either 6 MHz or 48 MHz is required while the USB module is enabled. Fortunately, the microcontroller and other peripherals are not required to run at this clock speed when using the primary oscillator. There are numerous options to achieve the USB module clock requirement and still provide flexibility for clocking the rest of the device from the primary oscillator source. These are detailed in **Section 2.3 "Oscillator Settings for USB"**.

FIGURE 2-1: PIC18F2455/2550/4455/4550 CLOCK DIAGRAM



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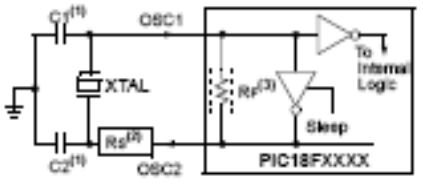
2.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In HS, HSPLL, XT and XTPLL Oscillator modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation. Figure 2-2 shows the pin connections.

The oscillator design requires the use of a parallel cut crystal.

Note:	Use of a series cut crystal may give a frequency out of the crystal manufacturer's specifications.

FIGURE 2-2: CRYSTAL/CERAMIC RESONATOR OPERATION (XT, HS OR HSPLL CONFIGURATION)



Note 1: See Table 2-1 and Table 2-2 for initial values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.
3: RF varies with the oscillator mode chosen.

TABLE 2-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Typical Capacitor Values Used:			
Mode	**Freq**	**OSC1**	**OSC2**
XT	4.0 MHz	33 pF	33 pF
HS	8.0 MHz	27 pF	27 pF
	16.0 MHz	22 pF	22 pF

Capacitor values are for design guidance only.

These capacitors were tested with the resonators listed below for basic start-up and operation. **These values are not optimized.**

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.

See the notes following Table 2-2 for additional information.

Resonators Used:
4.0 MHz
8.0 MHz
16.0 MHz

TABLE 2-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Osc Type	Crystal Freq	Typical Capacitor Values Tested:	
		C1	**C2**
XT	4 MHz	27 pF	27 pF
HS	4 MHz	27 pF	27 pF
	8 MHz	22 pF	22 pF
	20 MHz	15 pF	15 pF

Capacitor values are for design guidance only.

These capacitors were tested with the crystals listed below for basic start-up and operation. **These values are not optimized.**

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.

See the notes following this table for additional information.

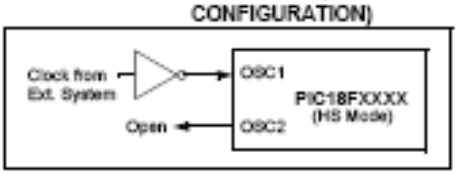
Crystals Used:
4 MHz
8 MHz
20 MHz

Note 1:	Higher capacitance increases the stability of oscillator but also increases the start-up time.
2:	When operating below 3V VDD, or when using certain ceramic resonators at any voltage, it may be necessary to use the HS mode or switch to a crystal oscillator.
3:	Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
4:	RS may be required to avoid overdriving crystals with low drive level specification.
5:	Always verify oscillator performance over the VDD and temperature range that is expected for the application.

An internal postscaler allows users to select a clock frequency other than that of the crystal or resonator. Frequency division is determined by the CPUDIV Configuration bits. Users may select a clock frequency of the oscillator frequency, or 1/2, 1/3 or 1/4 of the frequency.

An external clock may also be used when the microcontroller is in HS Oscillator mode. In this case, the OSC2/CLKO pin is left open (Figure 2-3).

FIGURE 2-3: EXTERNAL CLOCK INPUT OPERATION (HS OSC CONFIGURATION)

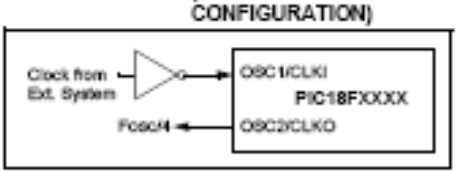


2.2.3 EXTERNAL CLOCK INPUT

The EC, ECIO, ECPLL and ECPIO Oscillator modes require an external clock source to be connected to the OSC1 pin. There is no oscillator start-up time required after a Power-on Reset or after an exit from Sleep mode.

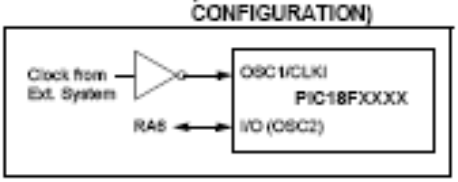
In the EC and ECPLL Oscillator modes, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic. Figure 2-4 shows the pin connections for the EC Oscillator mode.

FIGURE 2-4: EXTERNAL CLOCK INPUT OPERATION (EC AND ECPLL CONFIGURATION)



The ECIO and ECPIO Oscillator modes function like the EC and ECPLL modes, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6). Figure 2-5 shows the pin connections for the ECIO Oscillator mode.

FIGURE 2-5: EXTERNAL CLOCK INPUT OPERATION (ECIO AND ECPIO CONFIGURATION)



The internal postscaler for reducing clock frequency in XT and HS modes is also available in EC and ECIO modes.

2.2.4 PLL FREQUENCY MULTIPLIER

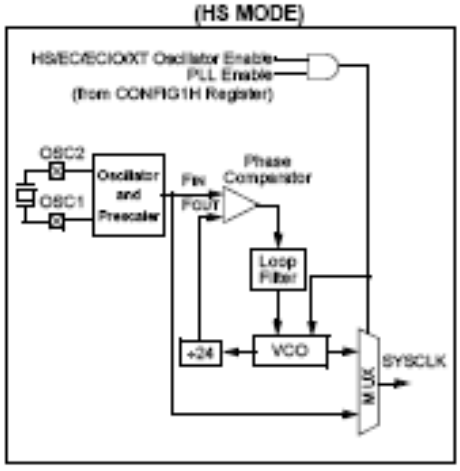
PIC18F2455/2550/4455/4550 devices include a Phase Locked Loop (PLL) circuit. This is provided specifically for USB applications with lower speed oscillators and can also be used as a microcontroller clock source.

The PLL is enabled in HSPLL, XTPLL, ECPLL and ECPIO Oscillator modes. It is designed to produce a fixed 96 MHz reference clock from a fixed 4 MHz input. The output can then be divided and used for both the USB and the microcontroller core clock. Because the PLL has a fixed frequency input and output, there are eight prescaling options to match the oscillator input frequency to the PLL.

There is also a separate postscaler option for deriving the microcontroller clock from the PLL. This allows the USB peripheral and microcontroller to use the same oscillator input and still operate at different clock speeds. In contrast to the postscaler for XT, HS and EC modes, the available options are 1/2, 1/3, 1/4 and 1/6 of the PLL output.

The HSPLL, ECPLL and ECPIO modes make use of the HS mode oscillator for frequencies up to 48 MHz. The prescaler divides the oscillator input by up to 12 to produce the 4 MHz drive for the PLL. The XTPLL mode can only use an input frequency of 4 MHz which drives the PLL directly.

FIGURE 2-6: PLL BLOCK DIAGRAM (HS MODE)



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4.0 RESET

The PIC18F2455/2550/4455/4550 devices differentiate between various kinds of Reset:

a) Power-on Reset (POR)
b) MCLR Reset during normal operation
c) MCLR Reset during power-managed modes
d) Watchdog Timer (WDT) Reset (during execution)
e) Programmable Brown-out Reset (BOR)
f) RESET Instruction
g) Stack Full Reset
h) Stack Underflow Reset

This section discusses Resets generated by MCLR, POR and BOR and covers the operation of the various start-up timers. Stack Reset events are covered in **Section 6.1.2.4 "Stack Full and Underflow Resets"**. WDT Resets are covered in **Section 25.2 "Watchdog Timer (WDT)"**.

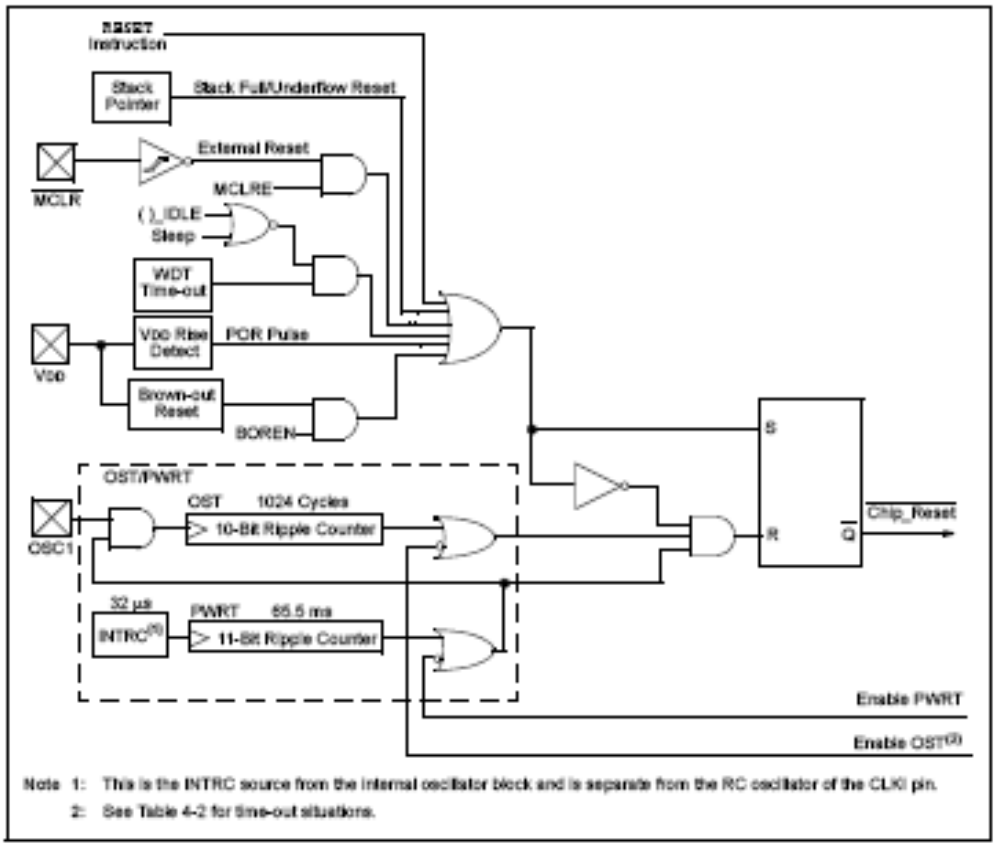
A simplified block diagram of the on-chip Reset circuit is shown in Figure 4-1.

4.1 RCON Register

Device Reset events are tracked through the RCON register (Register 4-1). The lower five bits of the register indicate that a specific Reset event has occurred. In most cases, these bits can only be cleared by the event and must be set by the application after the event. The state of these flag bits, taken together, can be read to indicate the type of Reset that just occurred. This is described in more detail in **Section 4.6 "Reset State of Registers"**.

The RCON register also has control bits for setting interrupt priority (IPEN) and software control of the BOR (SBOREN). Interrupt priority is discussed in **Section 9.0 "Interrupts"**. BOR is covered in **Section 4.4 "Brown-out Reset (BOR)"**.

FIGURE 4-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: This is the INTRC source from the internal oscillator block and is separate from the RC oscillator of the CLKI pin.
2: See Table 4-2 for time-out situations.

4.2 Master Clear Reset (MCLR)

The MCLR pin provides a method for triggering an external Reset of the device. A Reset is generated by holding the pin low. These devices have a noise filter in the MCLR Reset path which detects and ignores small pulses.

The MCLR pin is not driven low by any internal Resets, including the WDT.

In PIC18F2455/2550/4455/4550 devices, the MCLR input can be disabled with the MCLRE Configuration bit. When MCLR is disabled, the pin becomes a digital input. See **Section 10.5 "PORTE, TRISE and LATE Registers"** for more information.

4.3 Power-on Reset (POR)

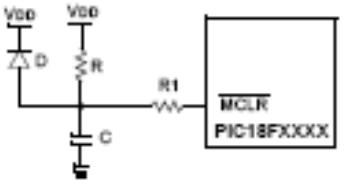
A Power-on Reset pulse is generated on-chip whenever VDD rises above a certain threshold. This allows the device to start in the initialized state when VDD is adequate for operation.

To take advantage of the POR circuitry, tie the MCLR pin through a resistor (1 kΩ to 10 kΩ) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset delay. A minimum rise rate for VDD is specified (parameter D004, **Section 28.1 "DC Characteristics"**). For a slow rise time, see Figure 4-2.

When the device starts normal operation (i.e., exits the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

POR events are captured by the POR bit (RCON<1>). The state of the bit is set to '0' whenever a POR occurs; it does not change for any other Reset event. POR is not reset to '1' by any hardware event. To capture multiple events, the user manually resets the bit to '1' in software following any POR.

FIGURE 4-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



Note 1: External Power-on Reset circuit is required only if the VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

2: R < 40 kΩ is recommended to make sure that the voltage drop across R does not violate the device's electrical specification.

3: R1 ≥ 1 kΩ will limit any current flowing into MCLR from external capacitor C, in the event of MCLR/VPP pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

5.0 MEMORY ORGANIZATION

There are three types of memory in PIC18 enhanced microcontroller devices:

- Program Memory
- Data RAM
- Data EEPROM

As Harvard architecture devices, the data and program memories use separate busses; this allows for concurrent access of the two memory spaces. The data EEPROM, for practical purposes, can be regarded as a peripheral device, since it is addressed and accessed through a set of control registers.

Additional detailed information on the operation of the Flash program memory is provided in **Section 6.0 "Flash Program Memory"**. Data EEPROM is discussed separately in **Section 7.0 "Data EEPROM Memory"**.

5.1 Program Memory Organization

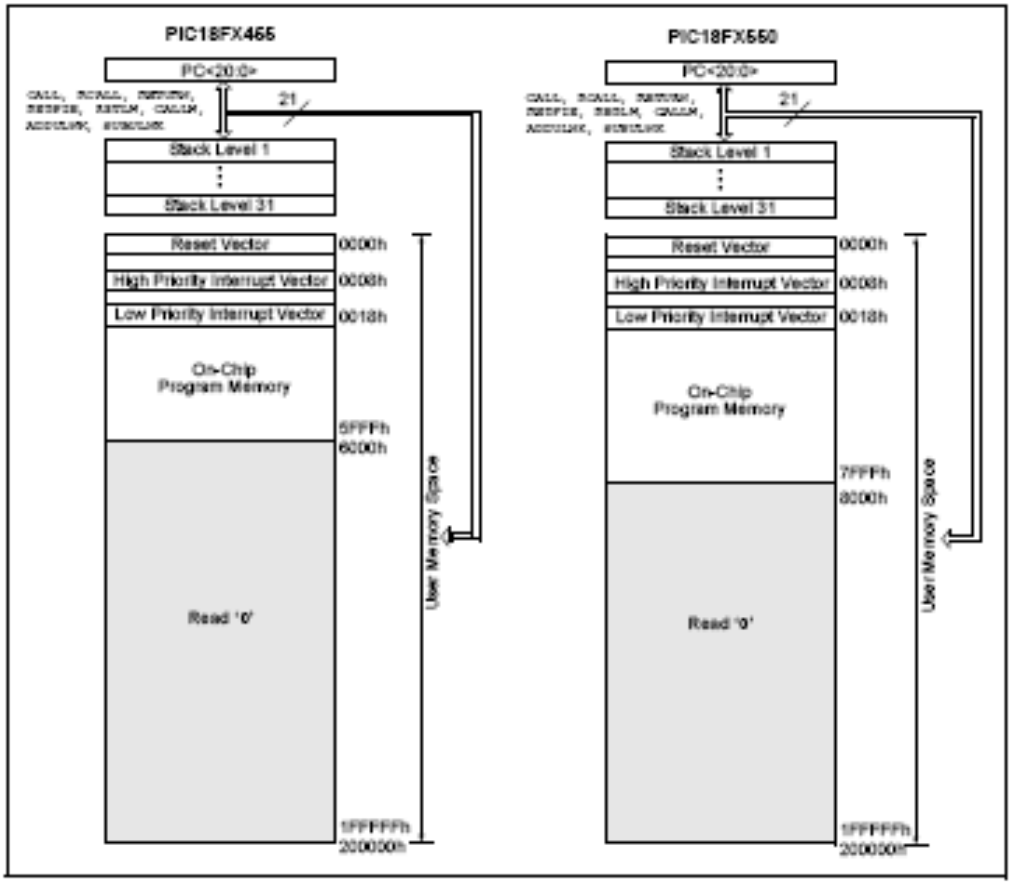
PIC18 microcontrollers implement a 21-bit program counter which is capable of addressing a 2-Mbyte program memory space. Accessing a location between the upper boundary of the physically implemented memory and the 2-Mbyte address will return all '0's (a NOP instruction).

The PIC18F2455 and PIC18F4455 each have 24 Kbytes of Flash memory and can store up to 12,288 single-word instructions. The PIC18F2550 and PIC18F4550 each have 32 Kbytes of Flash memory and can store up to 16,384 single-word instructions.

PIC18 devices have two interrupt vectors. The Reset vector address is at 0000h and the interrupt vector addresses are at 0008h and 0018h.

The program memory maps for PIC18FX455 and PIC18FX550 devices are shown in Figure 5-1.

FIGURE 5-1: PROGRAM MEMORY MAP AND STACK FOR PIC18F2455/2550/4455/4550 DEVICES



5.1.1 PROGRAM COUNTER

The Program Counter (PC) specifies the address of the instruction to fetch for execution. The PC is 21 bits wide and is contained in three separate 8-bit registers. The low byte, known as the PCL register, is both readable and writable. The high byte, or PCH register, contains the PC<15:8> bits; it is not directly readable or writable. Updates to the PCH register are performed through the PCLATH register. The upper byte is called PCU. This register contains the PC<20:16> bits; it is also not directly readable or writable. Updates to the PCU register are performed through the PCLATU register.

The contents of PCLATH and PCLATU are transferred to the program counter by any operation that writes PCL. Similarly, the upper two bytes of the program counter are transferred to PCLATH and PCLATU by an operation that reads PCL. This is useful for computed offsets to the PC (see **Section 5.1.4.1 "Computed GOTO"**).

The PC addresses bytes in the program memory. To prevent the PC from becoming misaligned with word instructions, the Least Significant bit of PCL is fixed to a value of '0'. The PC increments by 2 to address sequential instructions in the program memory.

The CALL, RCALL and GOTO program branch instructions write to the program counter directly. For these instructions, the contents of PCLATH and PCLATU are not transferred to the program counter.

5.1.2 RETURN ADDRESS STACK

The return address stack allows any combination of up to 31 program calls and interrupts to occur. The PC is pushed onto the stack when a CALL or RCALL instruction is executed or an interrupt is Acknowledged. The PC value is pulled off the stack on a RETURN, RETLW or a RETFIE instruction. PCLATU and PCLATH are not affected by any of the RETURN or CALL instructions.

The stack operates as a 31-word by 21-bit RAM and a 5-bit Stack Pointer, STKPTR. The stack space is not part of either program or data space. The Stack Pointer is readable and writable and the address on the top of the stack is readable and writable through the Top-of-Stack Special Function Registers. Data can also be pushed to, or popped from the stack, using these registers.

A CALL type instruction causes a push onto the stack. The Stack Pointer is first incremented and the location pointed to by the Stack Pointer is written with the contents of the PC (already pointing to the instruction following the CALL). A RETURN type instruction causes a pop from the stack. The contents of the location pointed to by the STKPTR are transferred to the PC and then the Stack Pointer is decremented.

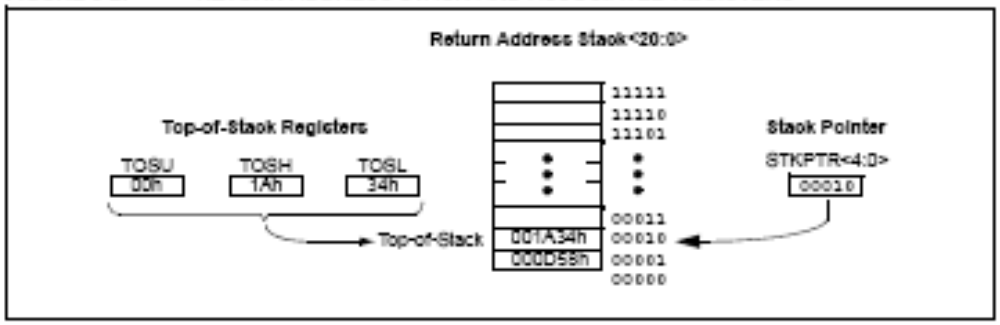
The Stack Pointer is initialized to '00000' after all Resets. There is no RAM associated with the location corresponding to a Stack Pointer value of '00000'; this is only a Reset value. Status bits indicate if the stack is full, has overflowed or has underflowed.

5.1.2.1 Top-of-Stack Access

Only the top of the return address stack (TOS) is readable and writable. A set of three registers, TOSU:TOSH:TOSL, hold the contents of the stack location pointed to by the STKPTR register (Figure 5-2). This allows users to implement a software stack if necessary. After a CALL, RCALL or interrupt, the software can read the pushed value by reading the TOSU:TOSH:TOSL registers. These values can be placed on a user-defined software stack. At return time, the software can return these values to TOSU:TOSH:TOSL and do a return.

The user must disable the global interrupt enable bits while accessing the stack to prevent inadvertent stack corruption.

FIGURE 5-2: RETURN ADDRESS STACK AND ASSOCIATED REGISTERS



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5.2 PIC18 Instruction Cycle

5.2.1 CLOCKING SCHEME

The microcontroller clock input, whether from an internal or external source, is internally divided by four to generate four non-overlapping quadrature clocks (Q1, Q2, Q3 and Q4). Internally, the program counter is incremented on every Q1; the instruction is fetched from the program memory and latched into the instruction Register (IR) during Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 5-3.

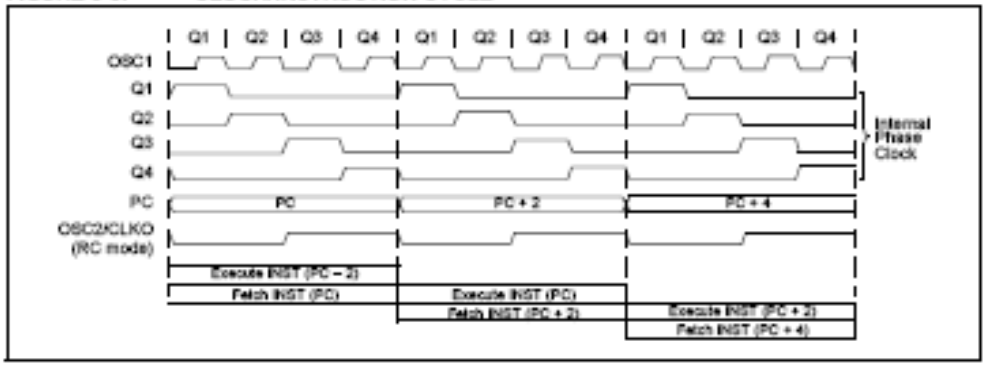
5.2.2 INSTRUCTION FLOW/PIPELINING

An "Instruction Cycle" consists of four Q cycles: Q1 through Q4. The instruction fetch and execute are pipelined in such a manner that a fetch takes one instruction cycle, while the decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 5-3).

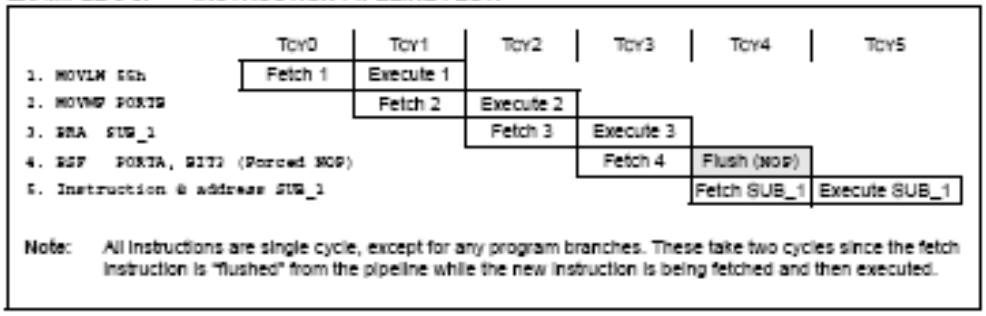
A fetch cycle begins with the Program Counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 5-3: CLOCK/INSTRUCTION CYCLE



EXAMPLE 5-3: INSTRUCTION PIPELINE FLOW



Note: All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

5.2.3 INSTRUCTIONS IN PROGRAM MEMORY

The program memory is addressed in bytes. Instructions are stored as two bytes or four bytes in program memory. The Least Significant Byte of an instruction word is always stored in a program memory location with an even address (LSb = 0). To maintain alignment with instruction boundaries, the PC increments in steps of 2 and the LSb will always read '0' (see Section 6.1.1 "Program Counter").

Figure 5-4 shows an example of how instruction words are stored in the program memory.

The CALL and GOTO instructions have the absolute program memory address embedded into the instruction. Since instructions are always stored on word boundaries, the data contained in the instruction is a word address. The word address is written to PC<20:1>, which accesses the desired byte address in program memory. Instruction #2 in Figure 5-4 shows how the instruction, GOTO 0006h, is encoded in the program memory. Program branch instructions, which encode a relative address offset, operate in the same manner. The offset value stored in a branch instruction represents the number of single-word instructions that the PC will be offset by. Section 28.0 "Instruction Set Summary" provides further details of the instruction set.

FIGURE 5-4: INSTRUCTIONS IN PROGRAM MEMORY

Program Memory Byte Locations →

			LSB = 1	LSB = 0	Word Address ↓
					000000h
					000002h
					000004h
					000006h
Instruction 1:	MOVLW	055h	0Fh	55h	000008h
Instruction 2:	GOTO	0006h	EFh	03h	00000Ah
			F0h	00h	00000Ch
Instruction 3:	MOVFF	123h, 456h	C1h	23h	00000Eh
			F4h	56h	000010h
					000012h
					000014h

5.2.4 TWO-WORD INSTRUCTIONS

The standard PIC18 instruction set has four two-word instructions: CALL, MOVFF, GOTO and LSFR. In all cases, the second word of the instructions always has '1111' as its four Most Significant bits; the other 12 bits are literal data, usually a data memory address.

The use of '1111' in the 4 MSbs of an instruction specifies a special form of NOP. If the instruction is executed in proper sequence, immediately after the first word, the data in the second word is accessed and used by the instruction sequence. If the first word is skipped for some reason and the second word is executed by itself, a NOP is executed instead. This is necessary for cases when the two-word instruction is preceded by a conditional instruction that changes the PC. Example 5-4 shows how this works.

Note:	See Section 6.5 "Program Memory and the Extended Instruction Set" for information on two-word instruction in the extended instruction set.

EXAMPLE 5-4: TWO-WORD INSTRUCTIONS

CASE 1:

Object Code	Source Code		
0110 0110 0000 0000	TSTFSZ	REG1	; is RAM location 0?
1100 0001 0010 0011	MOVFF	REG1, REG2	; No, skip this word
1111 0100 0101 0110			; Execute this word as a NOP
0010 0100 0000 0000	ADDWF	REG1	; continue code

CASE 2:

Object Code	Source Code		
0110 0110 0000 0000	TSTFSZ	REG1	; is RAM location 0?
1100 0001 0010 0011	MOVFF	REG1, REG2	; Yes, execute this word
1111 0100 0101 0110			; 2nd word of instruction
0010 0100 0000 0000	ADDWF	REG1	; continue code

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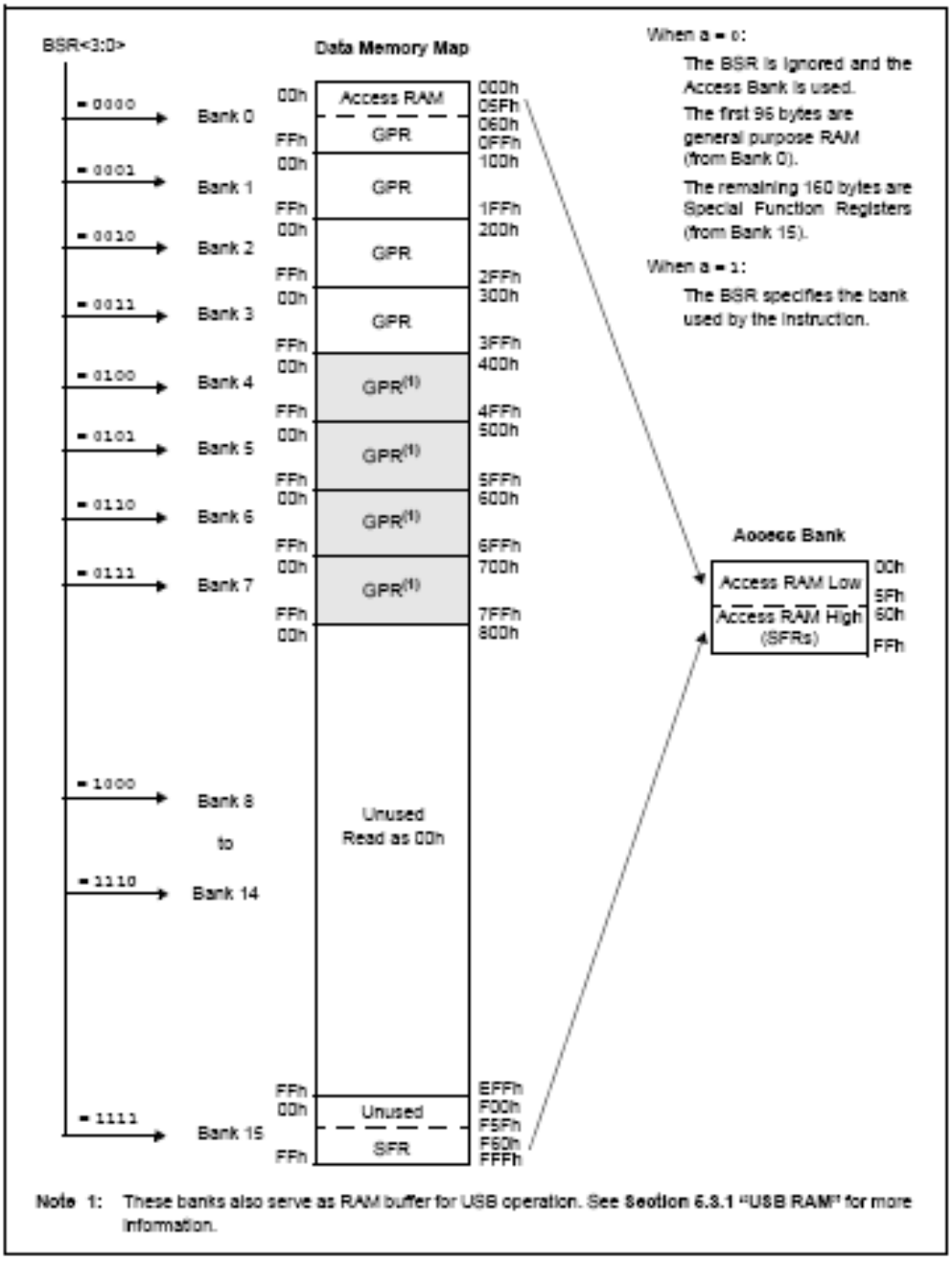
FIGURE 5-5: DATA MEMORY MAP FOR PIC18F2455/2550/4455/4550 DEVICES



Note 1: These banks also serve as RAM buffer for USB operation. See Section 6.3.1 "USB RAM" for more information.

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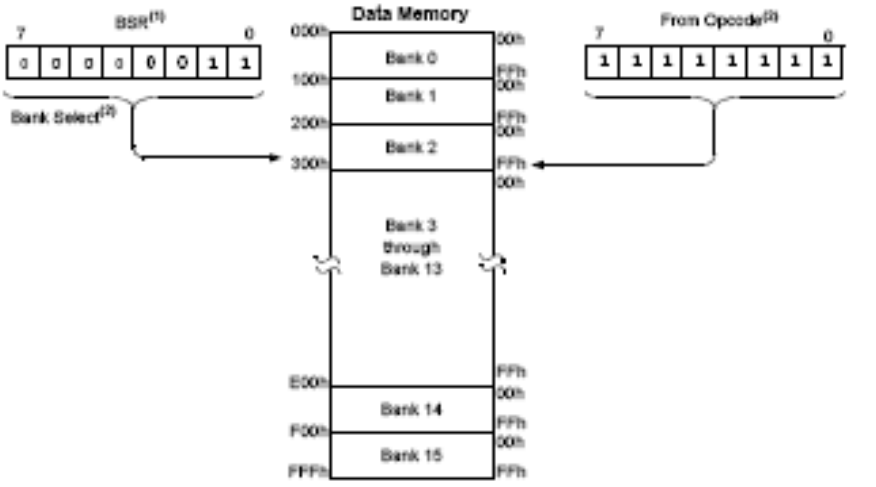
FIGURE 5-6: USE OF THE BANK SELECT REGISTER (DIRECT ADDRESSING)



Note 1: The Access RAM bit of the instruction can be used to force an override of the selected bank (BSR<3:0>) to the registers of the Access Bank.

2: The MOVFF instruction embeds the entire 12-bit address in the instruction.

5.3.3 ACCESS BANK

While the use of the BSR, with an embedded 8-bit address, allows users to address the entire range of data memory, it also means that the user must always ensure that the correct bank is selected. Otherwise, data may be read from or written to the wrong location. This can be disastrous if a GPR is the intended target of an operation but an SFR is written to instead. Verifying and/or changing the BSR for each read or write to data memory can become very inefficient.

To streamline access for the most commonly used data memory locations, the data memory is configured with an Access Bank, which allows users to access a mapped block of memory without specifying a BSR. The Access Bank consists of the first 96 bytes of memory (000h-5Fh) in Bank 0 and the last 160 bytes of memory (60h-FFh) in Block 15. The lower half is known as the "Access RAM" and is composed of GPRs. The upper half is where the device's SFRs are mapped. These two areas are mapped contiguously in the Access Bank and can be addressed in a linear fashion by an 8-bit address (Figure 5-5).

The Access Bank is used by core PIC18 instructions that include the Access RAM bit (the 'a' parameter in the instruction). When 'a' is equal to '1', the instruction uses the BSR and the 8-bit address included in the opcode for the data memory address. When 'a' is '0', however, the instruction is forced to use the Access Bank address map; the current value of the BSR is ignored entirely.

Using this "forced" addressing allows the instruction to operate on a data address in a single cycle without updating the BSR first. For 8-bit addresses of 60h and above, this means that users can evaluate and operate on SFRs more efficiently. The Access RAM below 60h is a good place for data values that the user might need to access rapidly, such as immediate computational results or common program variables. Access RAM also allows for faster and more code efficient context saving and switching of variables.

The mapping of the Access Bank is slightly different when the extended instruction set is enabled (XINST Configuration bit = 1). This is discussed in more detail in **Section 5.6.3 "Mapping the Access Bank in Indexed Literal Offset Mode"**.

5.3.4 GENERAL PURPOSE REGISTER FILE

PIC18 devices may have banked memory in the GPR area. This is data RAM which is available for use by all instructions. GPRs start at the bottom of Bank 0 (address 000h) and grow upwards towards the bottom of the SFR area. GPRs are not initialized by a Power-on Reset and are unchanged on all other Resets.

10.0 I/O PORTS

Depending on the device selected and features enabled, there are up to five ports available. Some pins of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

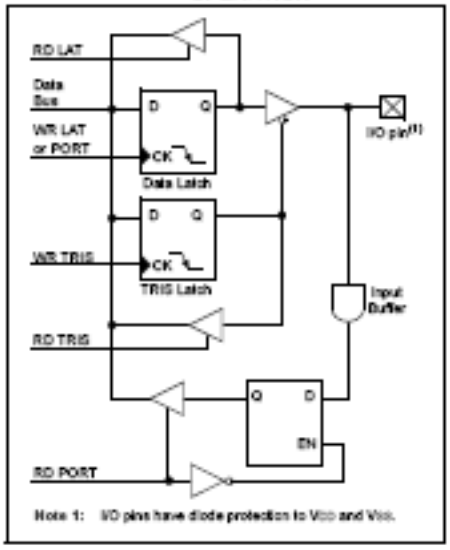
Each port has three registers for its operation. These registers are:

- TRIS register (data direction register)
- PORT register (reads the levels on the pins of the device)
- LAT register (output latch)

The Data Latch register (LATA) is useful for read-modify-write operations on the value driven by the I/O pins.

A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 10-1.

FIGURE 10-1: GENERIC I/O PORT OPERATION



Note 1: I/O pins have diode protection to VDD and VSS.

10.1 PORTA, TRISA and LATA Registers

PORTA is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins; writing to it will write to the port latch.

The Data Latch register (LATA) is also memory mapped. Read-modify-write operations on the LATA register read and write the latched output value for PORTA.

The RA4 pin is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA6 pin is multiplexed with the main oscillator pin; it is enabled as an oscillator or I/O pin by the selection of the main oscillator in Configuration Register 1H (see **Section 25.1 "Configuration Bits"** for details). When not used as a port pin, RA6 and its associated TRIS and LAT bits are read as '0'.

RA4 is also multiplexed with the USB module; it serves as a receiver input from an external USB transceiver. For details on configuration of the USB module, see **Section 17.2 "USB Status and Control"**.

Several PORTA pins are multiplexed with analog inputs, the analog VREF+ and VREF- inputs and the comparator voltage reference output. The operation of pins RA5 and RA3:RA0 as A/D converter inputs is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register 1).

Note:	On a Power-on Reset, RA5 and RA3:RA0 are configured as analog inputs and read as '0'. RA4 is configured as a digital input.

All other PORTA pins have TTL input levels and full CMOS output drivers.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE 10-1: INITIALIZING PORTA

```
CLRF    PORTA   ; Initialize PORTA by
                ; clearing output
                ; data latches
CLRF    LATA    ; Alternate method
                ; to clear output
                ; data latches
MOVLW   0Fh     ; Configure A/D
MOVWF   ADCON1  ; for digital inputs
MOVLW   07h     ; Configure comparators
MOVWF   CMCON   ; for digital input
MOVLW   0CFh    ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISA   ; Set RA<3:0> as inputs
                ; RA<5:4> as outputs
```

TABLE 10-1: PORTA I/O SUMMARY

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RA0/AN0	RA0	0	OUT	DIG	LATA<0> data output; not affected by analog input.
		1	IN	TTL	PORTA<0> data input; disabled when analog input enabled.
	AN0	1	IN	ANA	A/D input channel 0 and Comparator C1- input. Default configuration on POR; does not affect digital output.
RA1/AN1	RA1	0	OUT	DIG	LATA<1> data output; not affected by analog input.
		1	IN	TTL	PORTA<1> data input; reads '0' on POR.
	AN1	1	IN	ANA	A/D input channel 1 and Comparator C2- input. Default configuration on POR; does not affect digital output.
RA2/AN2/ VREF-/CVREF	RA2	0	OUT	DIG	LATA<2> data output; not affected by analog input. Disabled when CVREF output enabled.
		1	IN	TTL	PORTA<2> data input. Disabled when analog functions enabled; disabled when CVREF output enabled.
	AN2	1	IN	ANA	A/D input channel 2 and Comparator C2+ input. Default configuration on POR; not affected by analog output.
	VREF-	1	IN	ANA	A/D and comparator voltage reference low input.
	CVREF	x	OUT	ANA	Comparator voltage reference output. Enabling this feature disables digital I/O.
RA3/AN3/ VREF+	RA3	0	OUT	DIG	LATA<3> data output; not affected by analog input.
		1	IN	TTL	PORTA<3> data input; disabled when analog input enabled.
	AN3	1	IN	ANA	A/D input channel 3 and Comparator C1+ input. Default configuration on POR.
	VREF+	1	IN	ANA	A/D and comparator voltage reference high input.
RA4/T0CKI/ C1OUT/RCV	RA4	0	OUT	DIG	LATA<4> data output; not affected by analog input.
		1	IN	ST	PORTA<4> data input; disabled when analog input enabled.
	T0CKI	1	IN	ST	Timer0 clock input.
	C1OUT	0	OUT	DIG	Comparator 1 output; takes priority over port data.
	RCV	x	IN	TTL	External USB transceiver RCV input.
RA5/AN4/$\overline{SS}$/ HLVDIN/C2OUT	RA5	0	OUT	DIG	LATA<5> data output; not affected by analog input.
		1	IN	TTL	PORTA<5> data input; disabled when analog input enabled.
	AN4	1	IN	ANA	A/D input channel 4. Default configuration on POR.
	$\overline{SS}$	1	IN	TTL	Slave select input for SSP (MSSP module).
	HLVDIN	1	IN	ANA	High/Low-Voltage Detect external trip point input.
	C2OUT	0	OUT	DIG	Comparator 2 output; takes priority over port data.
OSC2/CLKO/ RA6	OSC2	x	OUT	ANA	Main oscillator feedback output connection (all XT and HS modes).
	CLKO	x	OUT	DIG	System cycle clock output (Fosc/4); available in EC, ECPLL and INTCKO modes.
	RA6	0	OUT	DIG	LATA<6> data output. Available only in ECIO, ECPIO and INTIO modes; otherwise, reads as '0'.
		1	IN	TTL	PORTA<6> data input. Available only in ECIO, ECPIO and INTIO modes; otherwise, reads as '0'.

Legend: OUT = Output, IN = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option)

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10.2 PORTB, TRISB and LATB Registers

PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

The Data Latch register (LATB) is also memory mapped. Read-modify-write operations on the LATB register read and write the latched output value for PORTB.

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit, RBPU (INTCON2<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Note:	On a Power-on Reset, RB4:RB0 are configured as analog inputs by default and read as '0'; RB7:RB5 are configured as digital inputs. By programming the Configuration bit, PBADEN (CONFIG3H<1>), RB4:RB0 will alternatively be configured as digital inputs on POR.

Four of the PORTB pins (RB7:RB4) have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur. Any RB7:RB4 pin configured as an output is excluded from the interrupt-on-change comparison. The pins are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are ORed together to generate the RB Port Change Interrupt with Flag bit, RBIF (INTCON<0>).

The interrupt-on-change can be used to wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB (except with the `MOVFF (ANY), PORTB` instruction). This will end the mismatch condition.

b) Clear flag bit, RBIF.

A mismatch condition will continue to set flag bit, RBIF. Reading PORTB will end the mismatch condition and allow flag bit, RBIF, to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

Pins, RB2 and RB3, are multiplexed with the USB peripheral and serve as the differential signal outputs for an external USB transceiver (TRIS configuration). Refer to **Section 17.2.2.2 "External Transceiver"** for additional information on configuring the USB module for operation with an external transceiver.

RB4 is multiplexed with CSSPP, the chip select function for the Streaming Parallel Port (SPP) – TRIS setting. Details of its operation are discussed in **Section 18.0 "Streaming Parallel Port"**.

EXAMPLE 10-2: INITIALIZING PORTB

```
CLRF    PORTB   ; Initialize PORTB by
                ; clearing output
                ; data latches
CLRF    LATB    ; Alternate method
                ; to clear output
                ; data latches
MOVLW   0Eh     ; Set RB<4:0> as
MOVWF   ADCON1  ; digital I/O pins
                ; (required if config bit
                ; PBADEN is set)
MOVLW   0CFh    ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISB   ; Set RB<3:0> as inputs
                ; RB<5:4> as outputs
                ; RB<7:6> as inputs
```


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TABLE 10-3: PORTB I/O SUMMARY (CONTINUED)

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RB6/KBI2/ PGC	RB6	0	OUT	DIG	LATB<6> data output.
		1	IN	TTL	PORTB<6> data input; weak pull-up when $\overline{\text{RBPU}}$ bit is cleared.
	KBI2	1	IN	TTL	Interrupt-on-pin change.
	PGC	x	IN	ST	Serial execution (ICSP™) clock input for ICSP and ICD operation.(3)
RB7/KBI3/ PGD	RB7	0	OUT	DIG	LATB<7> data output.
		1	IN	TTL	PORTB<7> data input; weak pull-up when $\overline{\text{RBPU}}$ bit is cleared.
	KBI3	1	IN	TTL	Interrupt-on-pin change.
	PGD	x	OUT	DIG	Serial execution data output for ICSP and ICD operation.(3)
		x	IN	ST	Serial execution data input for ICSP and ICD operation.(3)

Legend: OUT = Output, IN = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, I^2C/SMB = I^2C/SMBus input buffer, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option)

Note 1: Configuration on POR is determined by PBADEN Configuration bit. Pins are configured as analog inputs when PBADEN is set and digital inputs when PBADEN is cleared.

2: Alternate pin assignment for CCP2 when CCP2MX = 0. Default assignment is RC1.

3: All other pin functions are disabled when ICSP™ or ICD operation is enabled.

4: 40/44-pin devices only.

TABLE 10-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	54
LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	54
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	54
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
INTCON2	$\overline{\text{RBPU}}$	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RBIP	51
INTCON3	INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF	51
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	52
SPPCON(1)	—	—	—	—	—	—	SPPOWN	SPPEN	55
SPPCFG(1)	CLKCFG1	CLKCFG0	CSEN	CLK1EN	WS3	WS2	WS1	WS0	55
UCON	—	PPBRST	SE0	PKTDIS	USBEN	RESUME	SUSPND	—	55

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTB.

Note 1: These registers are unimplemented on 28-pin devices.

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TABLE 10-3: PORTB I/O SUMMARY (CONTINUED)

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RB6/KBI2/ PGC	RB6	0	OUT	DIG	LATB<6> data output.
		1	IN	TTL	PORTB<6> data input; weak pull-up when RBPU bit is cleared.
	KBI2	1	IN	TTL	Interrupt-on-pin change.
	PGC	x	IN	ST	Serial execution (ICSP™) clock input for ICSP and ICD operation.(3)
RB7/KBI3/ PGD	RB7	0	OUT	DIG	LATB<7> data output.
		1	IN	TTL	PORTB<7> data input; weak pull-up when RBPU bit is cleared.
	KBI3	1	IN	TTL	Interrupt-on-pin change.
	PGD	x	OUT	DIG	Serial execution data output for ICSP and ICD operation.(3)
		x	IN	ST	Serial execution data input for ICSP and ICD operation.(3)

Legend: OUT = Output, IN = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, I^2C/SMB = I^2C/SMBus input buffer, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option)

Note 1: Configuration on POR is determined by PBADEN Configuration bit. Pins are configured as analog inputs when PBADEN is set and digital inputs when PBADEN is cleared.

2: Alternate pin assignment for CCP2 when CCP2MX = 0. Default assignment is RC1.

3: All other pin functions are disabled when ICSP™ or ICD operation is enabled.

4: 40/44-pin devices only.

TABLE 10-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	54
LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	54
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	54
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RBIP	51
INTCON3	INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF	51
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	52
SPPCON(1)	—	—	—	—	—	—	SPPOWN	SPPEN	55
SPPCFG(1)	CLKCFG1	CLKCFG0	CSEN	CLK1EN	WS3	WS2	WS1	WS0	55
UCON	—	PPBRST	SE0	PKTDIS	USBEN	RESUME	SUSPND	—	55

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTB.

Note 1: These registers are unimplemented on 28-pin devices.

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21.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) converter module has 10 inputs for the 28-pin devices and 13 for the 40/44-pin devices. This module allows conversion of an analog input signal to a corresponding 10-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 21-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 21-2, configures the functions of the port pins. The ADCON2 register, shown in Register 21-3, configures the A/D clock source, programmed acquisition time and justification.

REGISTER 21-1: ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS3:CHS0:** Analog Channel Select bits

0000 = Channel 0 (AN0)
0001 = Channel 1 (AN1)
0010 = Channel 2 (AN2)
0011 = Channel 3 (AN3)
0100 = Channel 4 (AN4)
0101 = Channel 5 (AN5)(1,2)
0110 = Channel 6 (AN6)(1,2)
0111 = Channel 7 (AN7)(1,2)
1000 = Channel 8 (AN8)
1001 = Channel 9 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
1100 = Channel 12 (AN12)
1101 = Unimplemented(2)
1110 = Unimplemented(2)
1111 = Unimplemented(2)

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

When ADON = 1:
1 = A/D conversion in progress
0 = A/D Idle

bit 0 **ADON:** A/D On bit

1 = A/D converter module is enabled
0 = A/D converter module is disabled

Note 1: These channels are not implemented on 28-pin devices.
2: Performing a conversion on unimplemented channels will return a floating input measurement.

REGISTER 21-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0(1)	R/W(1)	R/W(1)	R/W(1)
—	—	VCFG0	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **VCFG0:** Voltage Reference Configuration bit (V_{REF-} source)
1 = V_{REF-} (AN2)
0 = V_{SS}

bit 4 **VCFG0:** Voltage Reference Configuration bit (V_{REF+} source)
1 = V_{REF+} (AN3)
0 = V_{DD}

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits:

PCFG3: PCFG0	AN12	AN11	AN10	AN9	AN8	AN7(2)	AN6(2)	AN5(2)	AN4	AN3	AN2	AN1	AN0
0000(1)	A	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A	A
0011	D	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	D	A	A	A	A	A	A	A	A	A
0111(1)	D	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input D = Digital I/O

Note 1: The POR value of the PCFG bits depends on the value of the PBADEN Configuration bit. When PBADEN = 1, PCFG<3:0> = 0000; when PBADEN = 0, PCFG<3:0> = 0111.
2: AN5 through AN7 are available only on 40/44-pin devices.

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The analog reference voltage is software selectable to either the device's positive and negative supply voltage (V_{DD} and V_{SS}) or the voltage level on the RA3/AN3/V_{REF+} and RA2/AN2/V_{REF-}/CVREF pins.

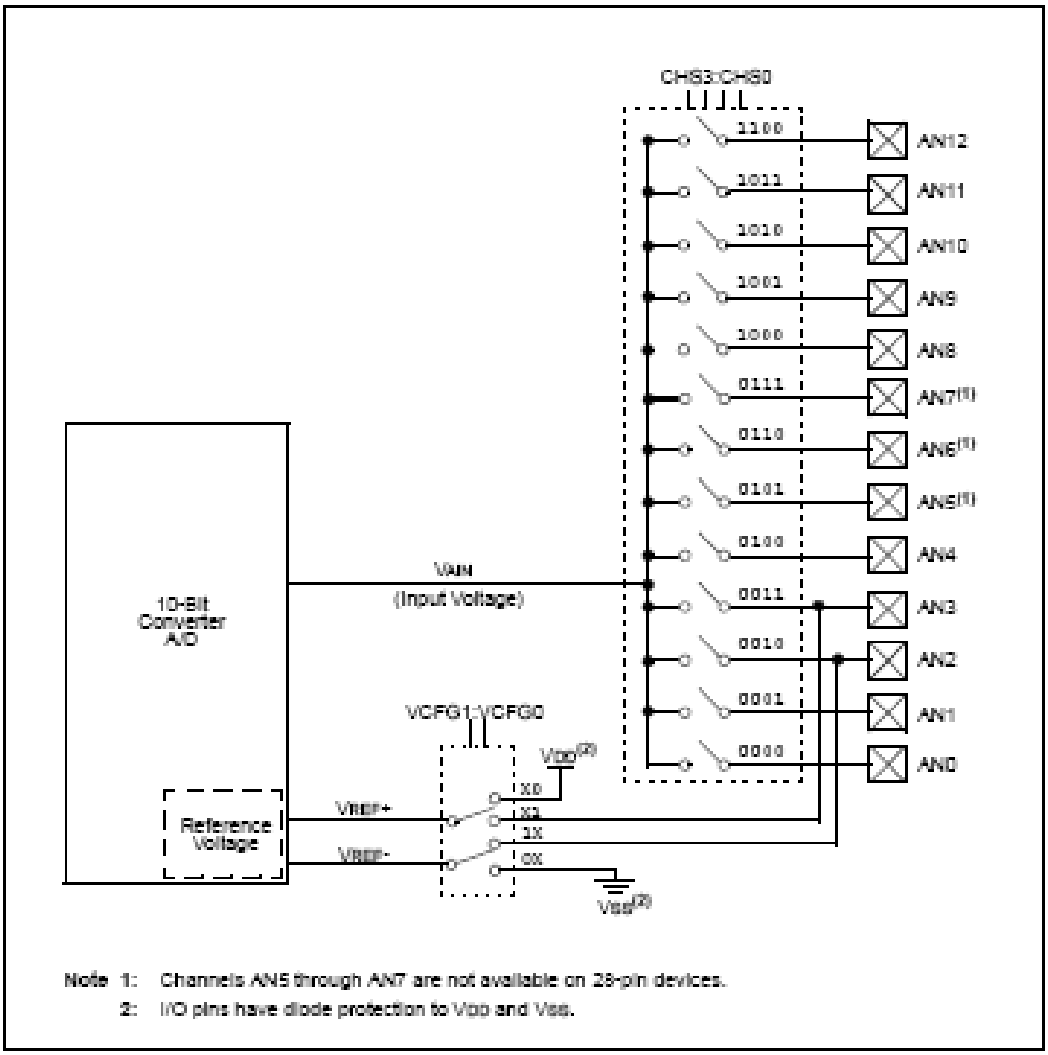
The A/D converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0 register) is cleared and A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 21-1.

FIGURE 21-1: A/D BLOCK DIAGRAM



Note 1: Channels AN5 through AN7 are not available on 28-pin devices.
2: I/O pins have diode protection to V_{DD} and V_{SS}.

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APPENDIX C

LM358 Op-Amp Datasheet

LM158,A-LM258,A
LM358,A

LOW POWER DUAL OPERATIONAL AMPLIFIERS

- INTERNALLY FREQUENCY COMPENSATED
- LARGE DC VOLTAGE GAIN: 100dB
- WIDE BANDWIDTH (unity gain): 1.1MHz (temperature compensated)
- VERY LOW SUPPLY CURRENT/OP (500µA) ESSENTIALLY INDEPENDENT OF SUPPLY VOLTAGE
- LOW INPUT BIAS CURRENT: 20nA (temperature compensated)
- LOW INPUT OFFSET VOLTAGE: 2mV
- LOW INPUT OFFSET CURRENT: 2nA
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE POWER SUPPLY VOLTAGE
- LARGE OUTPUT VOLTAGE SWING 0V TO (Vcc - 1.5V)

N
DIP8
(Plastic Package)

D & S
SO8 & miniSO8
(Plastic Micropackage)

P
TSSOP8
(Thin Shrink Small Outline Package)

DESCRIPTION

These circuits consist of two independent, high gain, internally frequency compensated which were designed specifically to operate from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op-amp circuits which now can be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with the standard +5V which is used in logic systems and will easily provide the required interface electronics without requiring any additional power supply.

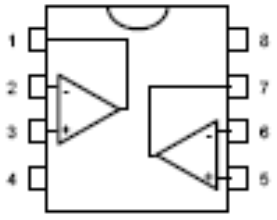
Inthe linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

ORDER CODE

Part Number	Temperature Range	Package			
		N	S	D	P
LM158,A	-55°C, +125°C	•		•	•
LM258,A	-40°C, +105°C	•		•	•
LM358,A	0°C, +70°C	•	•	•	•
Example : LM258N					

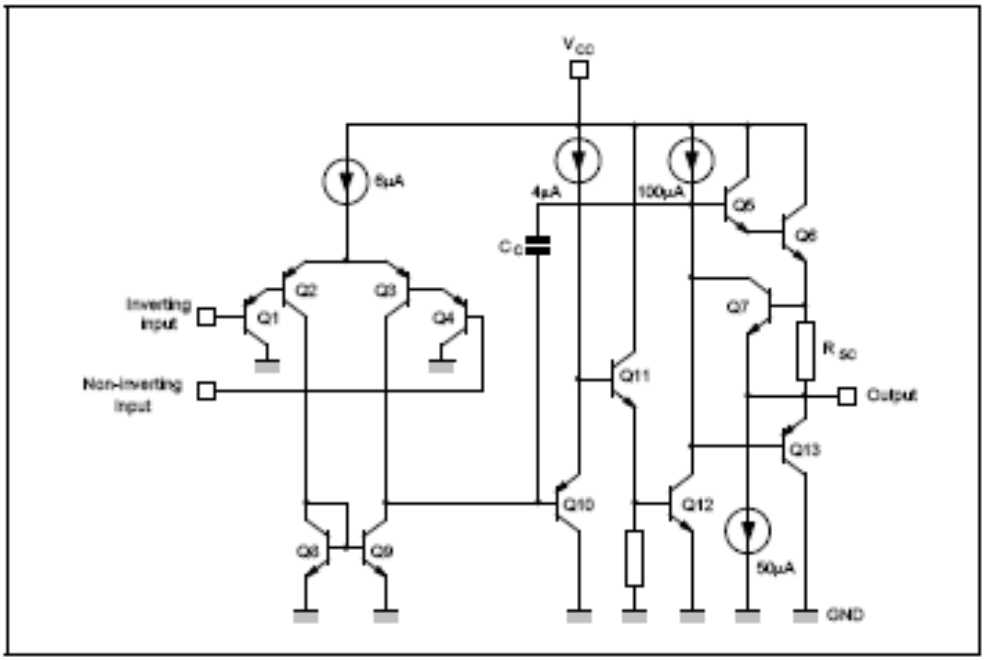
N = Dual In Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)
S = Small Outline Package (miniSO) only available in Tape & Reel (DT)
P = Thin Shrink Small Outline Package (TSSOP) - only available in Tape &Reel (PT)

PIN CONNECTIONS (top view)



1 - Output 1
2 - Inverting Input
3 - Non-Inverting Input
4 - V_{CC}^-
5 - Non-Inverting Input 2
6 - Inverting Input 2
7 - Output 2
8 - V_{CC}^+

SCHEMATIC DIAGRAM (1/2 LM158)



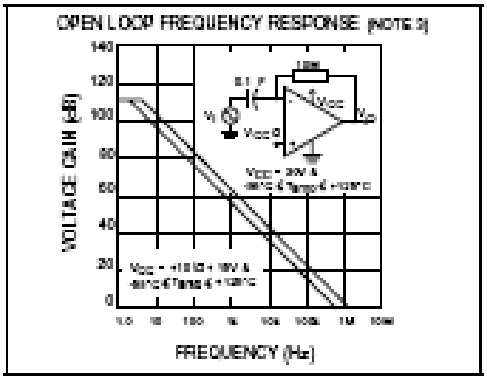
ABSOLUTE MAXIMUM RATINGS

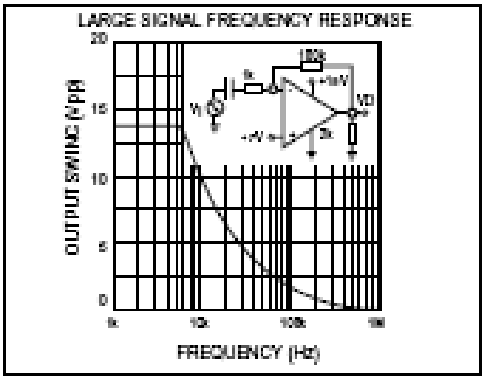
Symbol	Parameter	LM158,A	LM258,A	LM358,A	Unit
V_{CC}	Supply voltage	+/-16 or 32			V
V_i	Input Voltage	-0.3 to +32			V
V_{id}	Differential Input Voltage	+32			V
P_{tot}	Power Dissipation [1]	500			mW
	Output Short-circuit Duration [2]	Infinite			
I_{in}	Input Current [3]	50			mA
T_{oper}	Operating Free-air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to +150			°C

1. Power dissipation must be considered to ensure maximum junction temperature (Tj) is not exceeded.
2. Short-circuits from the output to V_{CC} can cause excessive heating if V_{CC} > 15V. The maximum output current is approximately 40mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuit on all amplifiers.
3. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diodes clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. this transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time duration than an input is driven negative.
This is not destructive and normal output will set up again for input voltage higher than -0.3V.

Symbol	Parameter	LM158A-LM258A LM358A			LM158-LM258 LM358			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	High Level Output Voltage (V_{CC}* = 30V) T_{amb} = +25°C R_L = 2kΩ $T_{min} \le T_{amb} \le T_{max}$ T_{amb} = +25°C R_L = 10kΩ $T_{min} \le T_{amb} \le T_{max}$	26 26 27 27	27 28 		26 26 27 27	27 28 		V
V_{OL}	Low Level Output Voltage (R_L = 10kΩ) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		5	20 20		5	20 20	mV
SR	Slew Rate V_{CC} = 15V, V_i = 0.5 to 3V, R_L = 2kΩ, C_L = 100pF, unity Gain	0.3	0.6		0.3	0.6		V/µs
GBP	Gain Bandwidth Product V_{CC} = 30V, f =100kHz,V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF	0.7	1.1		0.7	1.1		MHz
THD	Total Harmonic Distortion f = 1kHz, A_V = 20dB, R_L = 2kΩ, V_o = $2V_{pp}$, C_L = 100pF, V_O = 2Vpp		0.02			0.02		%
e_n	Equivalent Input Noise Voltage f = 1kHz, R_s = 100Ω, V_{CC} = 30V		55			55		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input Offset Voltage Drift		7	15		7	30	µV/°C
DI_{io}	Input Offset Current Drift		10	200		10	300	pA/°C
V_{o1}/V_{o2}	Channel Separation - note 4) 1kHz ≤ f ≤ 20kHZ		120			120		dB

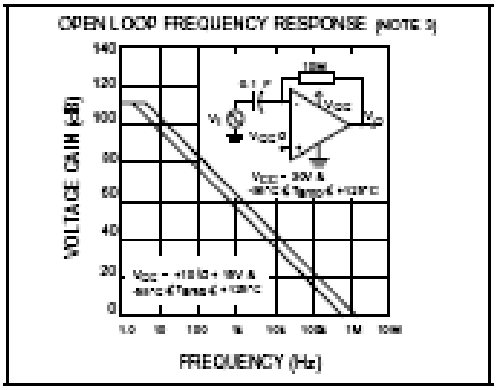
1. V_o = 1.4V, R_s = 0Ω, 5V < V_{CC}* < 30V, 0 < V_{ic} < V_{CC}* - 1.5V
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC}* - 1.5V, but either or both inputs can go to +32V without damage.
4. Due to the proximity of external components insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

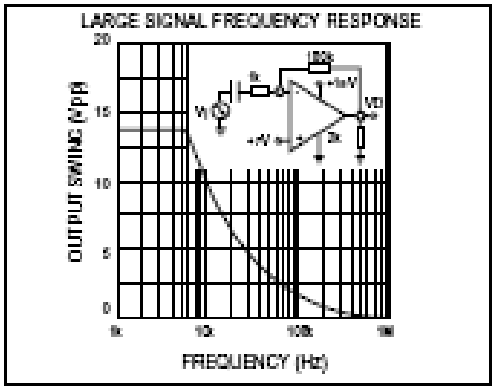


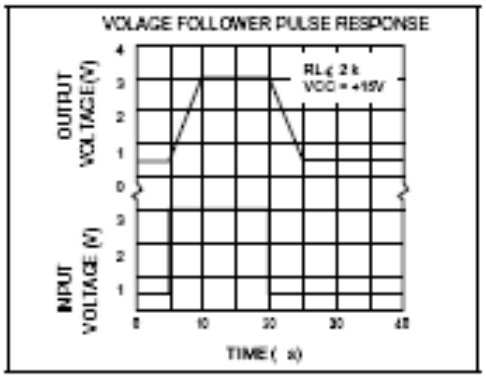


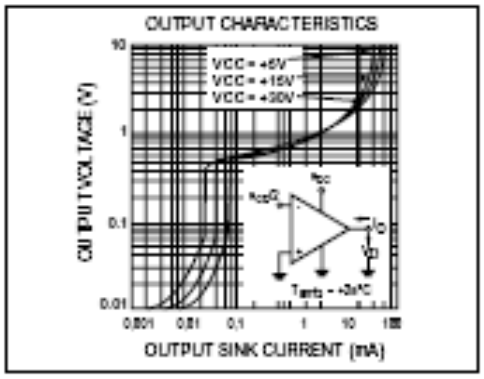
Symbol	Parameter	LM158A-LM258A LM358A			LM158-LM258 LM358			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	High Level Output Voltage (V_{CC}+ = 30V) T_{amb} = +25°C R_L = 2kΩ $T_{min} \le T_{amb} \le T_{max}$ T_{amb} = +25°C R_L = 10kΩ $T_{min} \le T_{amb} \le T_{max}$	26 26 27 27	27 28 		26 26 27 27	27 28 		V
V_{OL}	Low Level Output Voltage (R_L = 10kΩ) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		5	20 20		5	20 20	mV
SR	Slew Rate V_{CC} = 15V, V_i = 0.5 to 3V, R_L = 2kΩ, C_L = 100pF, unity Gain	0.3	0.6		0.3	0.6		V/µs
GBP	Gain Bandwidth Product V_{CC} = 30V, f =100kHz,V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF	0.7	1.1		0.7	1.1		MHz
THD	Total Harmonic Distortion f = 1kHz, A_V = 20dB, R_L = 2kΩ, V_o = 2V_{pp}, C_L = 100pF, V_O = 2Vpp		0.02			0.02		%
e_n	Equivalent Input Noise Voltage f = 1kHz, R_s = 100Ω, V_{CC} = 30V		55			55		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input Offset Voltage Drift		7	15		7	30	µV/°C
DI_{io}	Input Offset Current Drift		10	200		10	300	pA/°C
V_{o1}/V_{o2}	Channel Separation - note 4) 1kHz ≤ f ≤ 20kHZ		120			120		dB

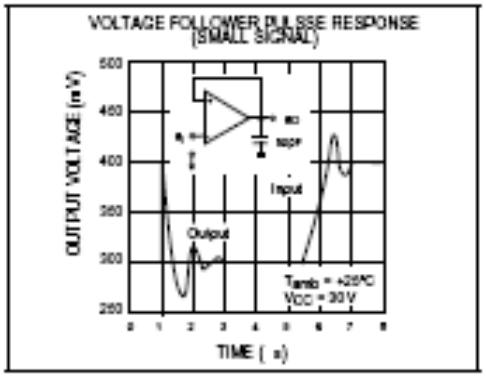
1. V_o = 1.4V, R_s = 0Ω, 5V < V_{CC}+ < 30V, 0 < V_{ic} < V_{CC}+ - 1.5V
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC}+ - 1.5V, but either or both inputs can go to +32V without damage.
4. Due to the proximity of external components insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

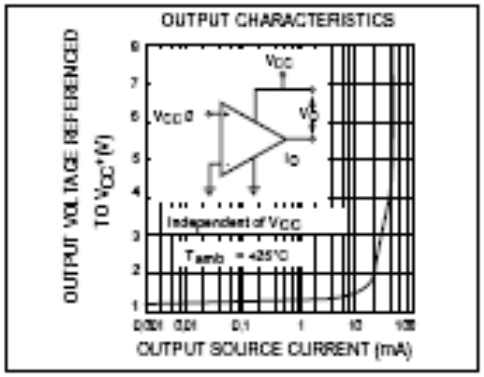


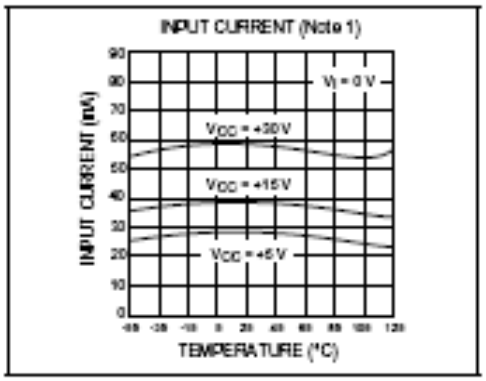


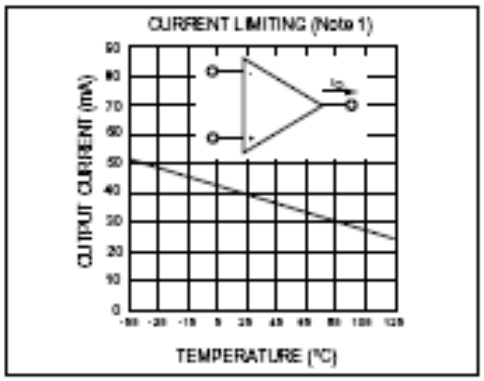

VOLAGE FOLLOWER PULSE RESPONSE
OUTPUT VOLTAGE(V)
INPUT VOLTAGE (V)
RL ≥ 2 k
VCC = +15V
TIME (s)

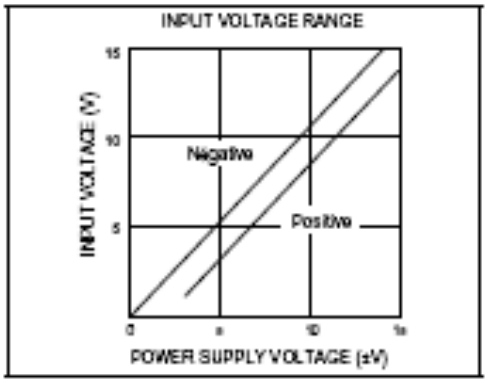

OUTPUT CHARACTERISTICS
VCC = +5V
VCC = +15V
VCC = +30V
OUTPUT VOLTAGE (V)
OUTPUT SINK CURRENT (mA)

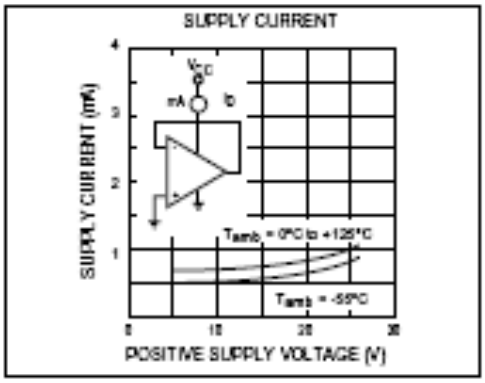

VOLTAGE FOLLOWER PULSE RESPONSE
(SMALL SIGNAL)
OUTPUT VOLTAGE (mV)
Input
Output
Tamb = +25°C
VCC = 30V
TIME (s)

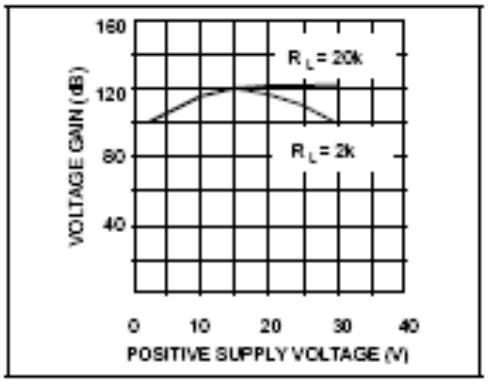

OUTPUT CHARACTERISTICS
OUTPUT VOLTAGE REFERENCED TO VCC+ (V)
Independent of VCC
Tamb = +25°C
OUTPUT SOURCE CURRENT (mA)

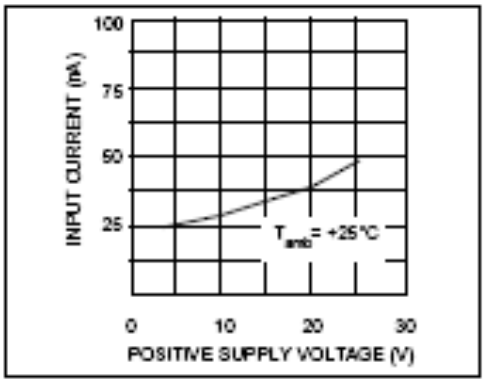

INPUT CURRENT (Note 1)
INPUT CURRENT (nA)
VI = 0 V
VCC = +30V
VCC = +15V
VCC = +5V
TEMPERATURE (°C)

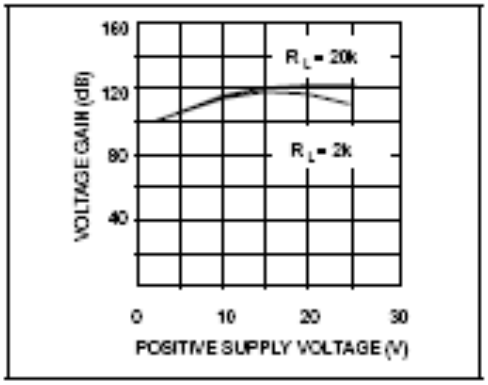

CURRENT LIMITING (Note 1)
OUTPUT CURRENT (mA)
TEMPERATURE (°C)

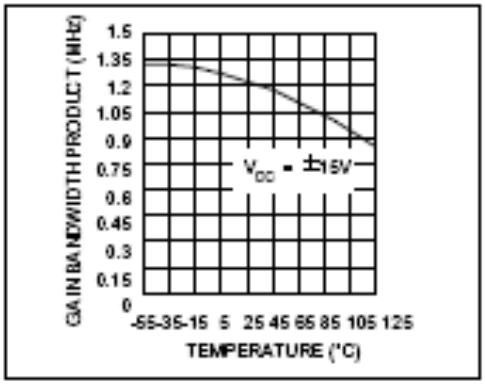

INPUT VOLTAGE RANGE
INPUT VOLTAGE (V)
Negative
Positive
POWER SUPPLY VOLTAGE (±V)

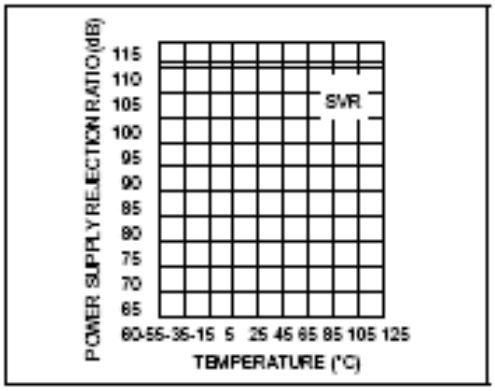

SUPPLY CURRENT
SUPPLY CURRENT (mA)
Tamb = 0°C to +125°C
Tamb = -55°C
POSITIVE SUPPLY VOLTAGE (V)

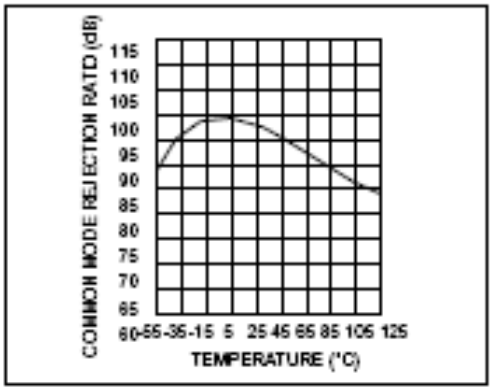

VOLTAGE GAIN (dB)
RL = 20k
RL = 2k
POSITIVE SUPPLY VOLTAGE (V)


INPUT CURRENT (nA)
Tamb = +25°C
POSITIVE SUPPLY VOLTAGE (V)


VOLTAGE GAIN (dB)
RL = 20k
RL = 2k
POSITIVE SUPPLY VOLTAGE (V)

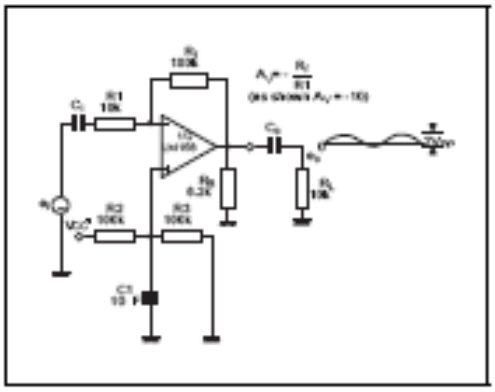

GAIN BANDWIDTH PRODUCT (MHz)
VCC = ±15V
TEMPERATURE (°C)



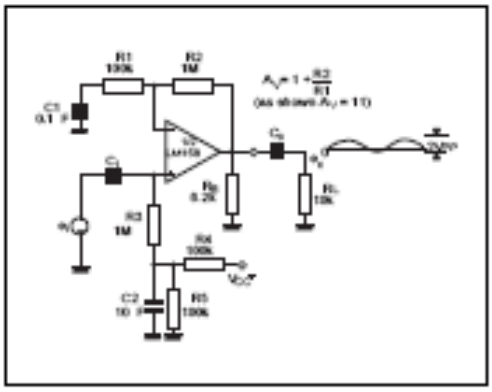


TYPICAL APPLICATIONS (single supply voltage) V_{cc} = +5V_{dc}

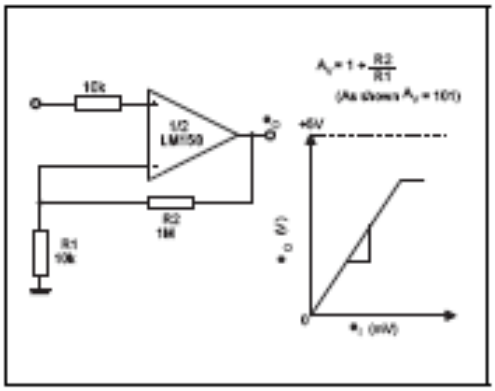
AC COUPLED INVERTING AMPLIFIER



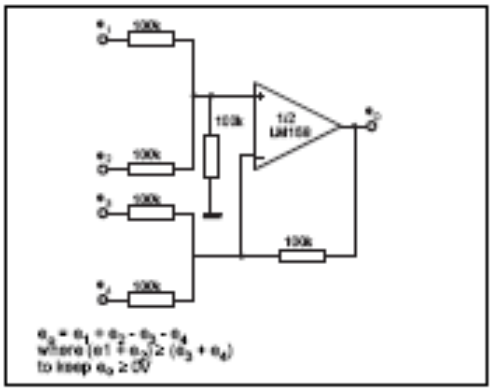
AC COUPLED NON-INVERTING AMPLIFIER



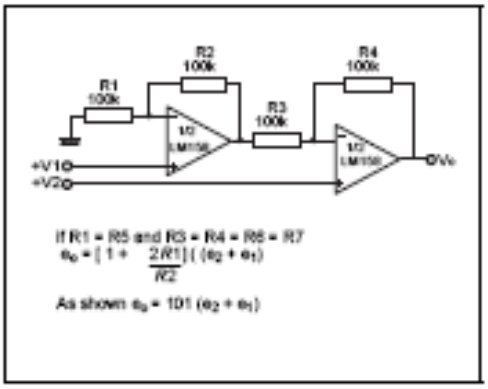
NON-INVERTING DC AMPLIFIER



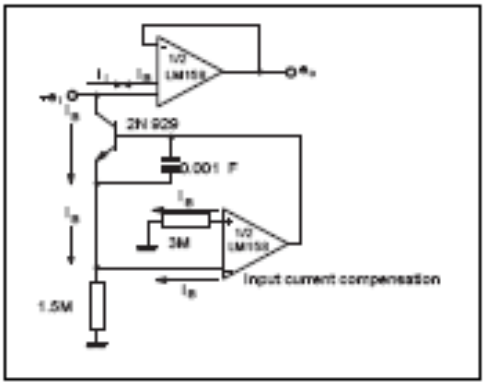
DC SUMMING AMPLIFIER



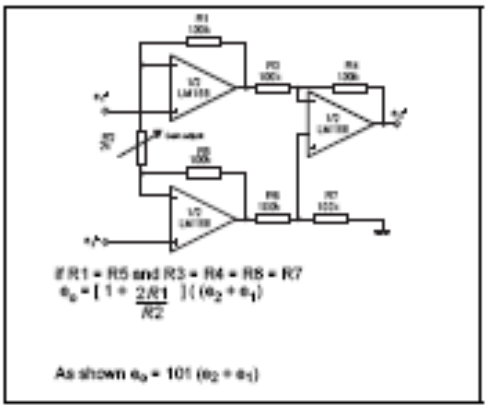
HIGH INPUT Z, DC DIFFERENTIAL AMPLIFIER



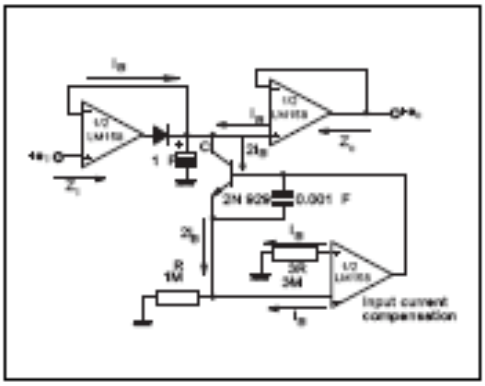
USING SYMMETRICAL AMPLIFIERS TO REDUCE INPUT CURRENT



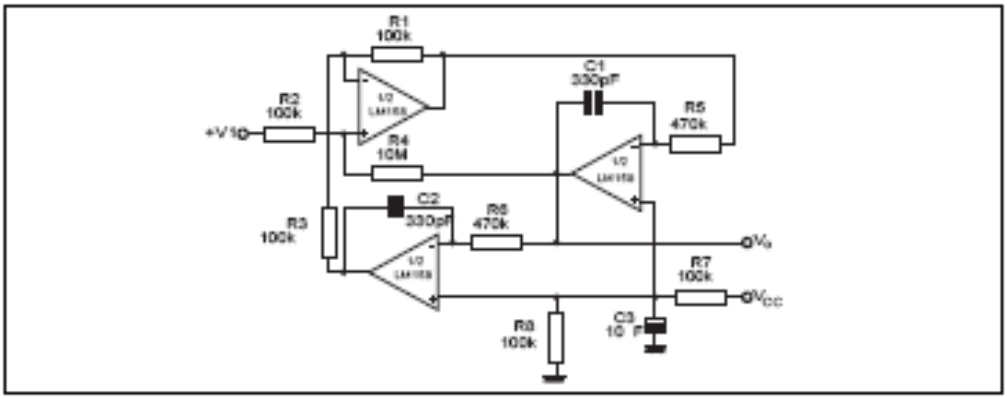
HIGH INPUT Z ADJUSTABLE GAIN DC INSTRUMENTATION AMPLIFIER



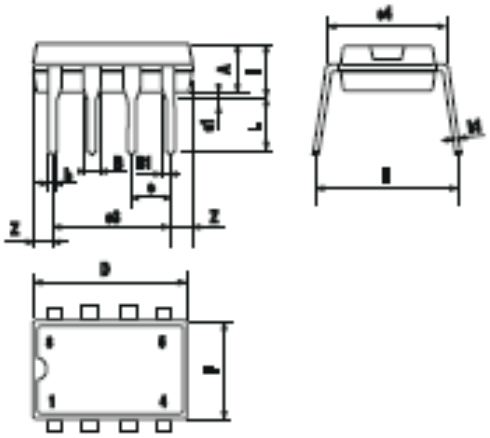
LOW DRIFT PEAK DETECTOR



ACTIVE BAND-PASS FILTER



PACKAGE MECHANICAL DATA
8 PINS - PLASTIC DIP



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

APPENDIX D

LM7805 Voltage Regulator Datasheet

FAIRCHILD
SEMICONDUCTOR®

March 2008

LM78XX/LM78XXA
3-Terminal 1A Positive Voltage Regulator

Features

- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

General Description

The LM78XX series of three terminal positive regulators are available in the TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

Ordering Information

Product Number	Output Voltage Tolerance	Package	Operating Temperature
LM7805CT	±4%	TO-220	-40°C to +125°C
LM7806CT			
LM7808CT			
LM7809CT			
LM7810CT			
LM7812CT			
LM7815CT			
LM7818CT			
LM7824CT			
LM7805ACT	±2%		0°C to +125°C
LM7806ACT			
LM7808ACT			
LM7809ACT			
LM7810ACT			
LM7812ACT			
LM7815ACT			
LM7818ACT			
LM7824ACT			

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Block Diagram

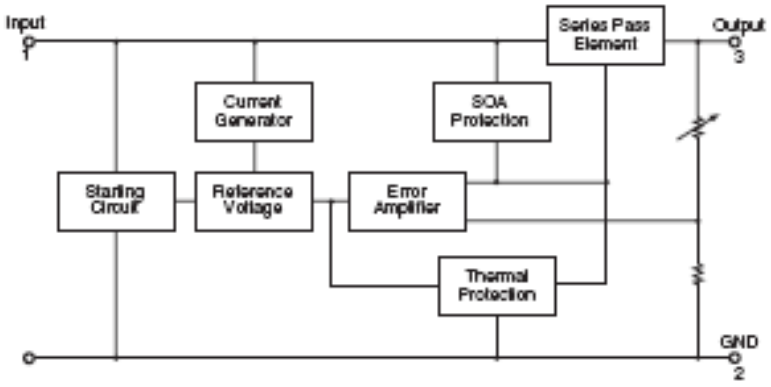


Figure 1.

Pin Assignment

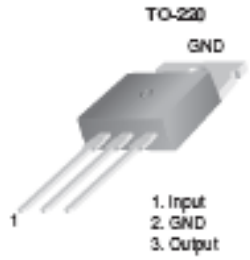


Figure 2.

Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Symbol	Parameter		Value	Unit
V_I	Input Voltage	V_O = 5V to 18V	35	V
		V_O = 24V	40	V
$R_{\theta JC}$	Thermal Resistance Junction-Cases (TO-220)		5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction-Air (TO-220)		65	°C/W
T_{OPR}	Operating Temperature Range	LM78xx	-40 to +125	°C
		LM78xxA	0 to +125	
T_{STG}	Storage Temperature Range		-65 to +150	°C

Electrical Characteristics (LM7805)

Refer to the test circuits. -40°C < T_J < 125°C, I_O = 500mA, V_I = 10V, C_I = 0.1µF, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_J = +25°C		4.8	5.0	5.2	V
		5mA ≤ I_O ≤ 1A, P_O ≤ 15W, V_I = 7V to 20V		4.75	5.0	5.25	
Regline	Line Regulation[1]	T_J = +25°C	V_O = 7V to 25V	–	4.0	100	mV
			V_I = 8V to 12V	–	1.6	50.0	
Regload	Load Regulation[1]	T_J = +25°C	I_O = 5mA to 1.5A	–	9.0	100	mV
			I_O = 250mA to 750mA	–	4.0	50.0	
I_Q	Quiescent Current	T_J = +25°C		–	5.0	8.0	mA
ΔI_Q	Quiescent Current Change	I_O = 5mA to 1A		–	0.03	0.5	mA
		V_I = 7V to 25V		–	0.3	1.3	
$\Delta V_O/\Delta T$	Output Voltage Drift[2]	I_O = 5mA		–	-0.8	–	mV/°C
V_N	Output Noise Voltage	f = 10Hz to 100kHz, T_A = +25°C		–	42.0	–	µV/V_O
RR	Ripple Rejection[2]	f = 120Hz, V_O = 8V to 18V		62.0	73.0	–	dB
V_{DROP}	Dropout Voltage	I_O = 1A, T_J = +25°C		–	2.0	–	V
r_O	Output Resistance[2]	f = 1kHz		–	15.0	–	mΩ
I_{SC}	Short Circuit Current	V_I = 35V, T_A = +25°C		–	230	–	mA
I_{PK}	Peak Current[2]	T_J = +25°C		–	2.2	–	A

Notes:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.
2. These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7805A) (Continued)

Refer to the test circuits. $0°C < T_J < 125°C$, $I_O = 1A$, $V_I = 10V$, $C_I = 0.33\mu F$, $C_O = 0.1\mu F$, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_O	Output Voltage	$T_J = +25°C$		4.9	5.0	5.1	V
		$I_O = 5mA$ to 1A, $P_O \leq 15W$, $V_I = 7.5V$ to 20V		4.8	5.0	5.2	
Regline	Line Regulation[19]	$V_I = 7.5V$ to 25V, $I_O = 500mA$		–	5.0	50.0	mV
		$V_I = 8V$ to 12V		–	3.0	50.0	
		$T_J = +25°C$	$V_I = 7.3V$ to 20V	–	5.0	50.0	
			$V_I = 8V$ to 12V	–	1.5	25.0	
Regload	Load Regulation[19]	$T_J = +25°C$, $I_O = 5mA$ to 1.5A		–	9.0	100	mV
		$I_O = 5mA$ to 1A		–	9.0	100	
		$I_O = 250mA$ to 750mA		–	4.0	50.0	
I_Q	Quiescent Current	$T_J = +25°C$		–	5.0	6.0	mA
ΔI_Q	Quiescent Current Change	$I_O = 5mA$ to 1A		–	–	0.5	mA
		$V_I = 8V$ to 25V, $I_O = 500mA$		–	–	0.8	
		$V_I = 7.5V$ to 20V, $T_J = +25°C$		–	–	0.8	
$\Delta V_O/\Delta T$	Output Voltage Drift[20]	$I_O = 5mA$		–	-0.8	–	mV/°C
V_N	Output Noise Voltage	$f = 10Hz$ to 100kHz, $T_A = +25°C$		–	10.0	–	$\mu V/V_O$
RR	Ripple Rejection[20]	$f = 120Hz$, $I_O = 500mA$, $V_I = 8V$ to 18V		–	68.0	–	dB
V_{DROP}	Dropout Voltage	$I_O = 1A$, $T_J = +25°C$		–	2.0	–	V
r_O	Output Resistance[20]	$f = 1kHz$		–	17.0	–	mΩ
I_{SC}	Short Circuit Current	$V_I = 35V$, $T_A = +25°C$		–	250	–	mA
I_{PK}	Peak Current[20]	$T_J = +25°C$		–	2.2	–	A

Notes:

19. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

20. These parameters, although guaranteed, are not 100% tested in production.

Typical Performance Characteristics

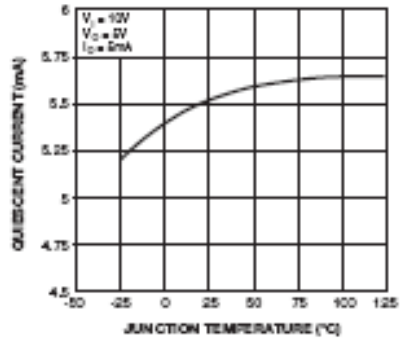


Figure 3. Quiescent Current

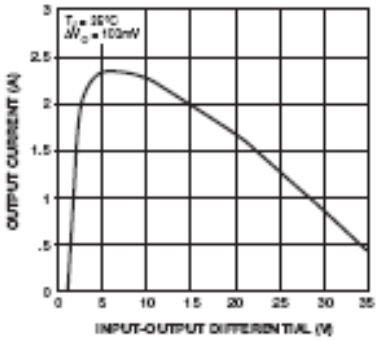


Figure 4. Peak Output Current

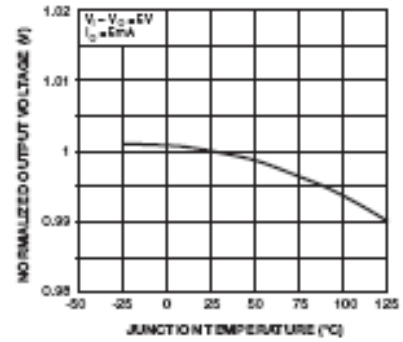


Figure 5. Output Voltage

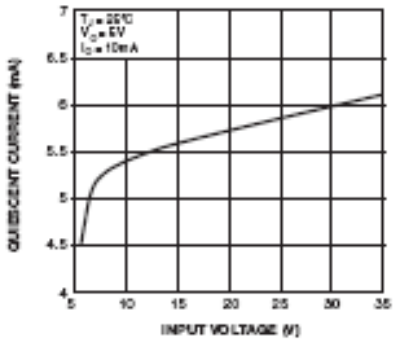


Figure 6. Quiescent Current

Typical Applications

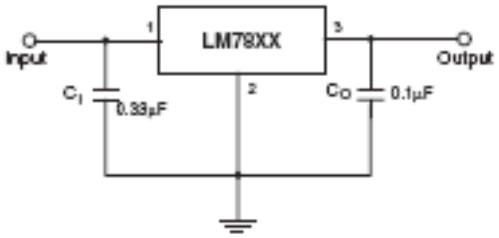


Figure 7. DC Parameters

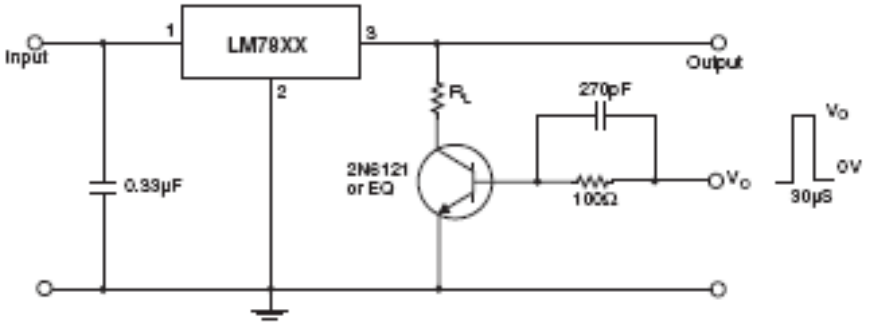


Figure 8. Load Regulation

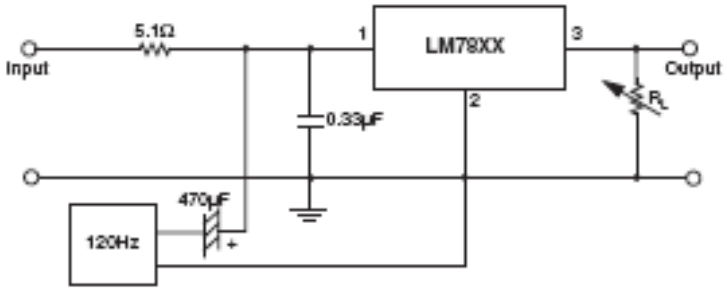


Figure 9. Ripple Rejection

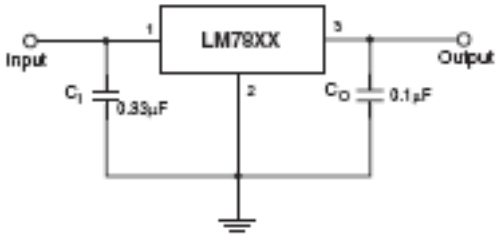
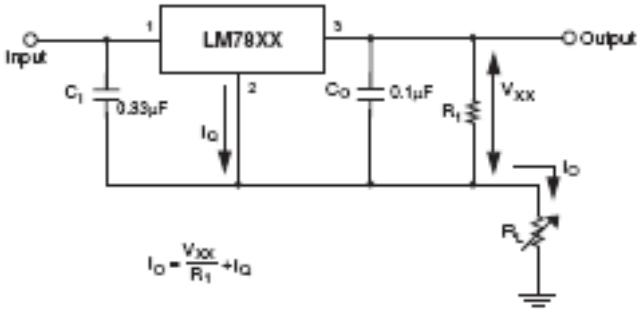


Figure 10. Fixed Output Regulator



Notes:
1. To specify an output voltage, substitute voltage value for "XX." A common ground is required between the input and the output voltage. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.
2. C_I is required if regulator is located an appreciable distance from power supply filter.
3. C_O improves stability and transient response.

Figure 11.

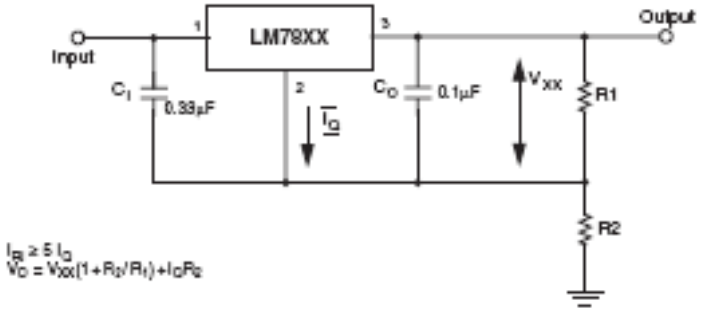
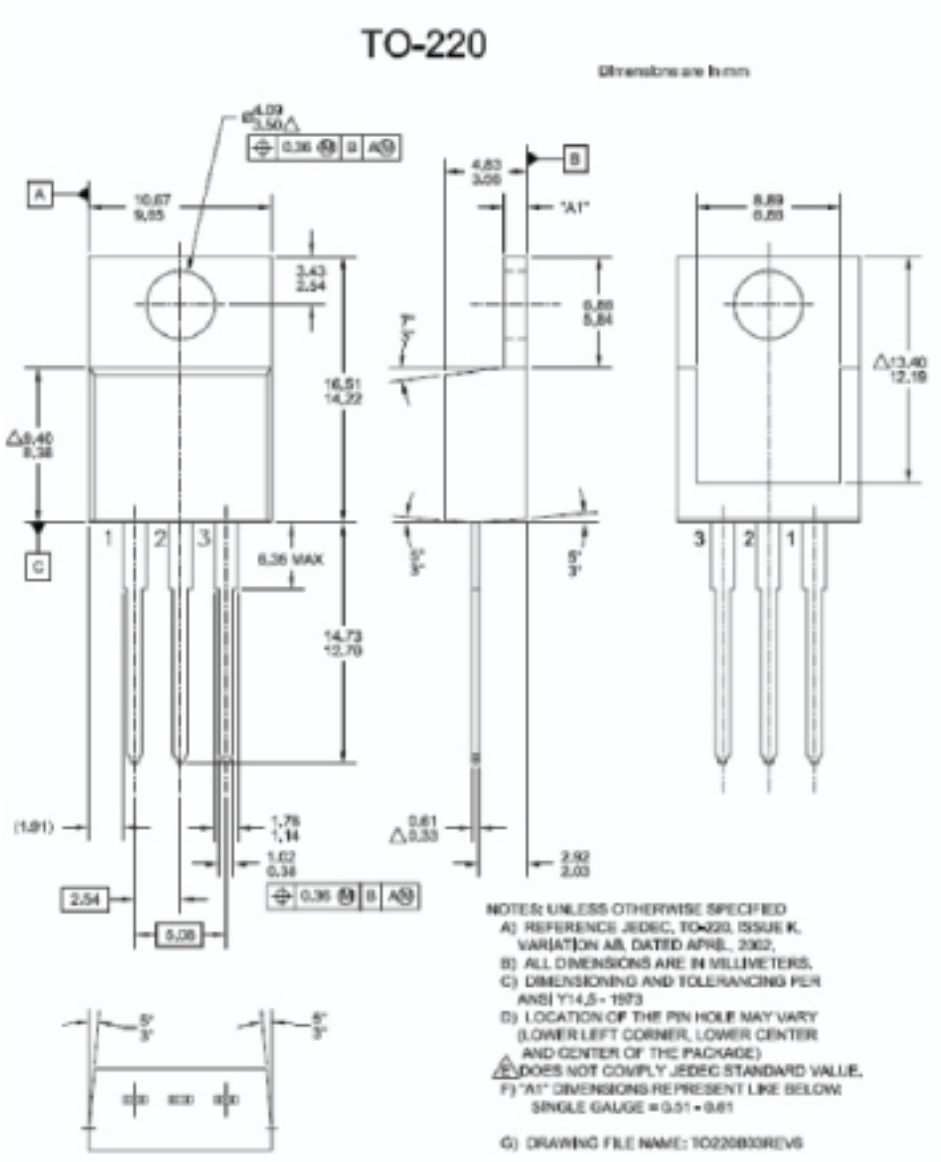


Figure 12. Circuit for Increasing Output Voltage

Mechanical Dimensions

Dimensions in millimeters



APPENDIX E

JHD162A Series Datasheet

JHD162A SERIES

• ..... DISPLAY CONTENT= 16 CHAR x 2ROW

CHAR. DOTS= 5 x 8

DRIVING MODE= 1/16D

AVAILABLE TYPES= =

TN= STN(YELLOW GREEN= GREY= B/W)

REFLECTIVE= WITH EL OR LED BACKLIGHT

EL/100VAC= 400HZ

LED/4.2VDC

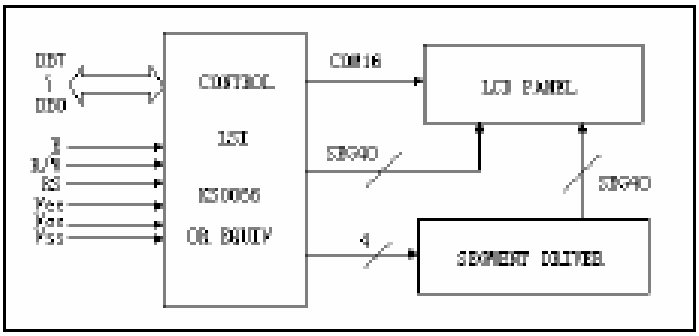
• .....

Parameter	Symbol	Testing Criteria	Standard Values			Unit
			Min.	Typ.	Max	
Supply voltage	Vcc-Vss	-	4.5	5.0	5.5	V
Input high voltage	VIH	-	2.2	-	Vcc	V
Input low voltage	VIL	-	-0.3	-	0.6	V
Output high voltage	VOH	-I0=0.2mA	2.4	-	-	V
Output low voltage	VOL	I0L=1.2mA	-	-	0.4	V
Operating voltage	Icc	Vcc=5.0V	-	1.5	3.0	mA

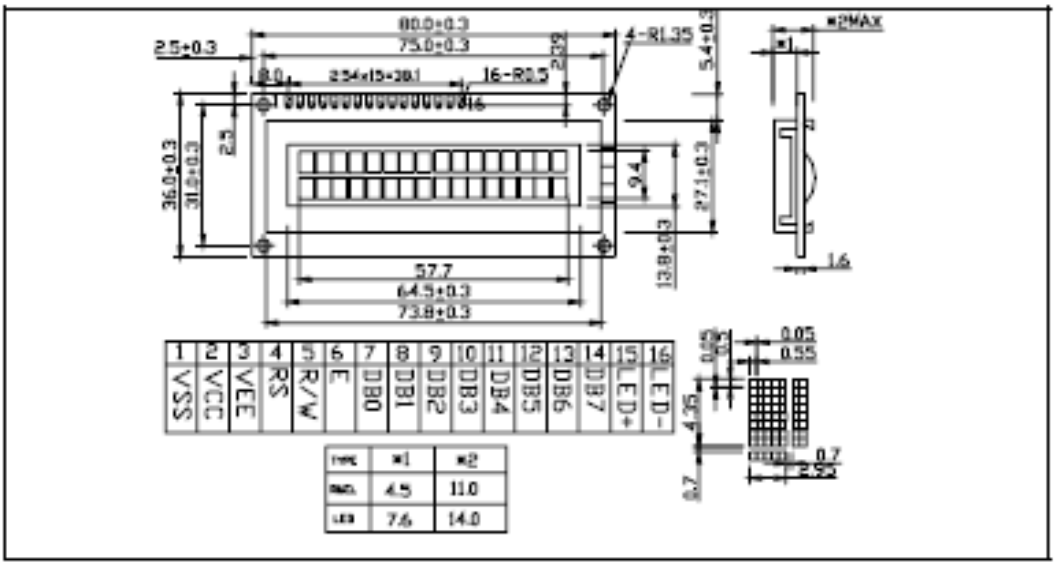
..

..

• .....



• .....



	4.5	11.0
	7.6	14.0

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
VSS	V_{CC}	V_{EE}	RS	R/W	E	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	LED+	LED-

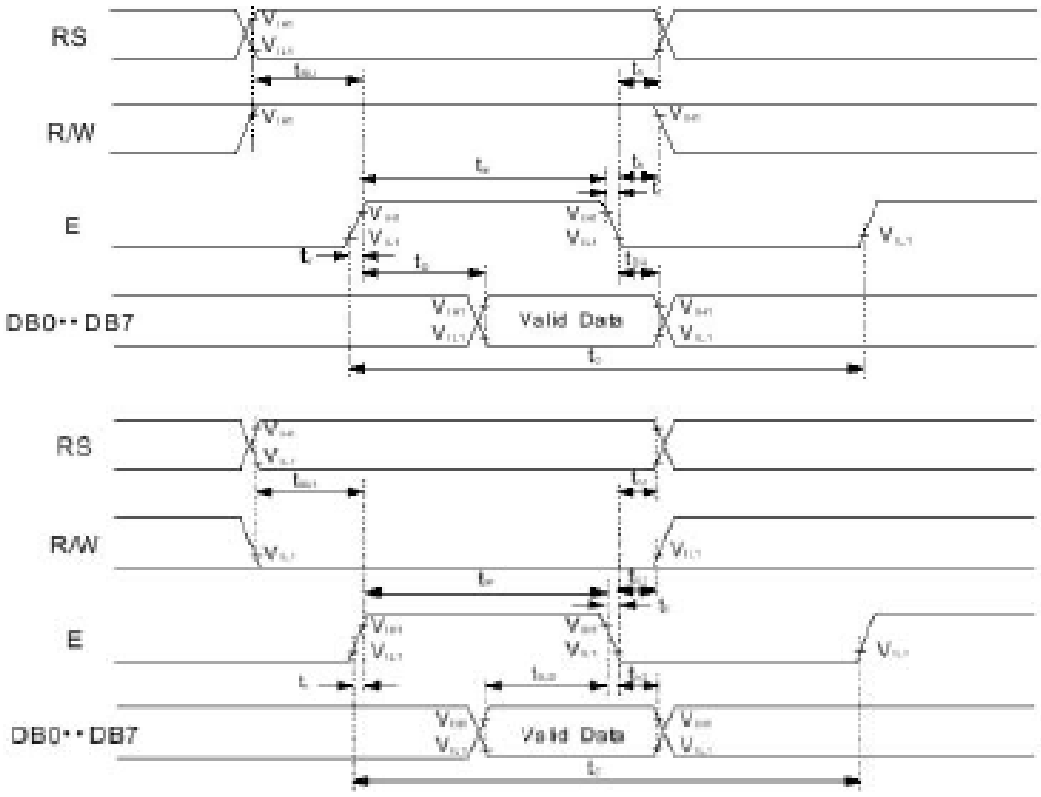
AC Characteristics Read Mode Timing Diagram

Table 12. AC Characteristics (V_{DD} = 4.5V ~ 5.5V, Ta = -30 ~ +85°C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode (Refer to Fig-6)	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu1	40	-	-	
	R/W and RS Hold Time	t_{H1}	10	-	-	
	Data Setup Time	tsu2	80	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode (Refer to Fig-7)	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu	40	-	-	
	R/W and RS Hold Time	t_H	10	-	-	
	Data Output Delay Time	t_D	-	-	120	
	Data Hold Time	t_{DH}	5	-	-	

Table 13. AC Characteristics (V_{DD} =2.7V ~ 4.5V, Ta = -30 ~ +85°C)

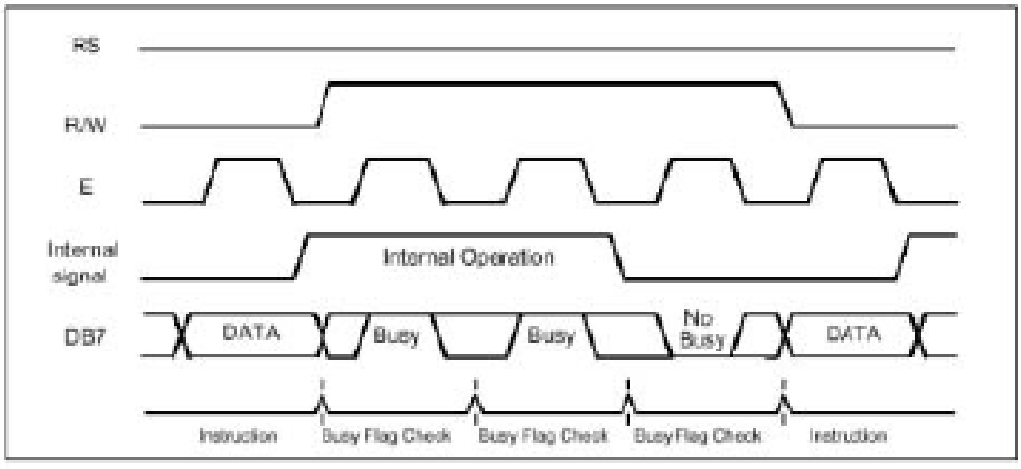
Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode (Refer to Fig-6)	E Cycle Time	tc	1000	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu1	60	-	-	
	R/W and RS Hold Time	t_{H1}	20	-	-	
	Data Setup Time	tsu2	195	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode (Refer to Fig-7)	E Cycle Time	tc	1000	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu	60	-	-	
	R/W and RS Hold Time	t_H	20	-	-	
	Data Output Delay Time	t_D	-	-	360	
	Data Hold Time	t_{DH}	5	-	-	

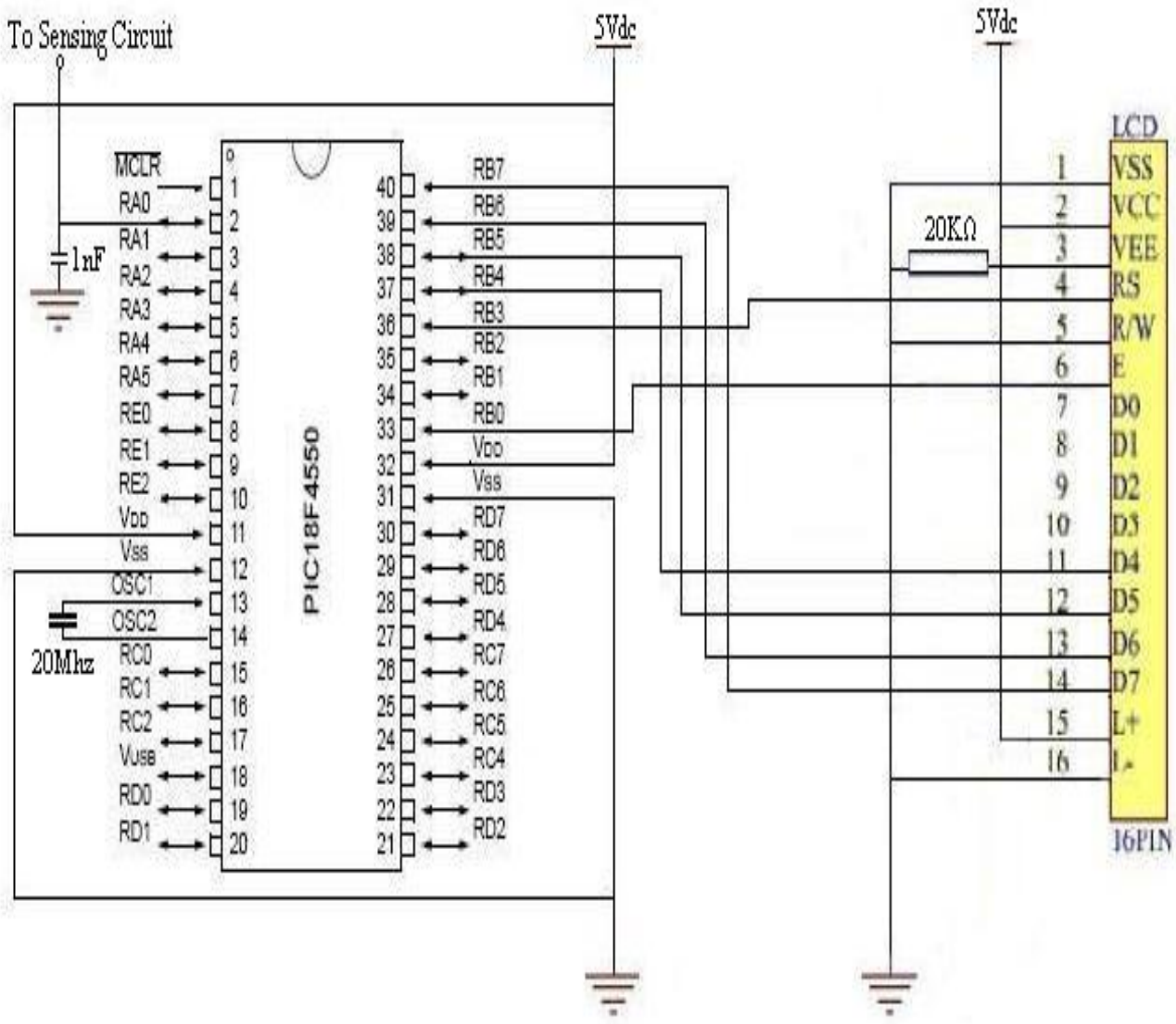


Write Mode Timing Diagram

Timing

1) Interface with 8-bit MPU
When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7.
Example of timing sequence is shown below.




To Sensing Circuit
5Vdc
5Vdc
LCD
PIC18F4550
MCLR
RA0
RA1
RA2
RA3
RA4
RA5
RE0
RE1
RE2
VDD
VSS
OSC1
OSC2
RC0
RC1
RC2
VUSB
RD0
RD1
RB7
RB6
RB5
RB4
RB3
RB2
RB1
RB0
VDD
VSS
RD7
RD6
RD5
RD4
RC7
RC6
RC5
RC4
RD3
RD2
1nF
20Mhz
20KΩ
VSS
VCC
VEE
RS
R/W
E
D0
D1
D2
D3
D4
D5
D6
D7
L+
16PIN

APPENDIX F

Omron G3NA-240B Solid State Relay

OMRON

Solid-state Relay

G3NA

A Wide Range of Models with 5- to 40-A Output Currents and Up to 480-VAC/200-VDC Output Voltages

- All models feature the same compact dimensions to provide a uniform mounting pitch.
- Built-in varistor effectively absorb external surges.
- Operation indicator (red LED) enables monitoring operation.
- Protective cover for greater safety.
- Standard models approved by UL/CSA and -UTU models by VDE (TÜV).

Ordering Information

Isolation	Zero cross function	Indicator	Rated output load (Applicable output load)	Rated input voltage	Model
Phototriac	Yes	Yes	5 A at 24 to 240 VAC* (19 to 264 VAC)	5 to 24 VDC	G3NA-205B
Photocoupler				100 to 120 VAC	
				200 to 240 VAC	
Phototriac			10 A at 24 to 240 VAC* (19 to 264 VAC)	5 to 24 VDC	G3NA-210B
Photocoupler				100 to 120 VAC	
				200 to 240 VAC	
			10 A at 200 to 480 VAC* (180 to 528 VAC)	5 to 24 VDC	G3NA-410B
				100 to 240 VAC	
	—		10 A at 5 to 200 VDC* (4 to 220 VDC)	5 to 24 VDC	G3NA-D210B
				100 to 240 VAC	
Phototriac	Yes		20 A at 24 to 240 VAC* (19 to 264 VAC)	5 to 24 VDC	G3NA-220B
Photocoupler				100 to 120 VAC	
				200 to 240 VAC	
			20 A at 200 to 480 VAC* (180 to 528 VAC)	5 to 24 VDC	G3NA-420B
				100 to 240 VAC	
Phototriac			40 A at 24 to 240 VAC* (19 to 264 VAC)	5 to 24 VDC	G3NA-240B
Photocoupler				100 to 120 VAC	
				200 to 240 VAC	
			40 A at 200 to 480 VAC* (180 to 528 VAC)	5 to 24 VDC	G3NA-440B
				100 to 240 VAC	
			50 A at 200 to 480 VAC* (180 to 528 VAC)	5 to 24 VDC	G3NA-450B

*Loss time increases under 75 VAC. (Refer to page 148.)

Note: When ordering a TÜV-approved model, add "-UTU" to the model number as shown below.
Example: G3NA-210B-UTU

■ Accessories (Order Separately)

Heat Sink

The following heat sinks are thin and can be DIN-track mounted (except Y92B-P250).
See *Dimensions* for details.

Model	Applicable SSR
Y92B-N50	G3NA-205B, G3NA-210B, G3NA-D210B, G3NA-410B, G3NE-205T(L), G3NE-210T(L)
Y92B-N100	G3NA-220B, G3NA-420B, G3NE-220T(L)
Y92B-N150	G3NA-240B, G3NA-440B
Y92B-P250	G3NA-450B

Low-cost Models

Model	Applicable SSR
Y92B-A100	G3NA-205B, G3NA-210B, G3NA-D210B, G3NA-220B, G3NA-410B, G3NA-420B
Y92B-A150N	G3NA-240B, G3NA-440B
Y92B-A250	G3NA-440B

Mounting Bracket

Used to mount the G3NA with a mounting dimension of 56 mm.

Model	Applicable SSR
R99-11	G3NA-240B, G3NA-440B

See *Dimensions* for details. (Refer to page 148.)

Specifications

■ Ratings

Input (Ambient Temperature: 25°C)

Model	Rated voltage	Operating voltage	Impedance	Voltage level	
				Must operate voltage	Must release voltage
G3NA-2□□B	5 to 24 VDC	4 to 32 VDC	7 mA max.*	4 VDC max.	1 VDC min.
	100 to 120 VAC	75 to 132 VAC	36 kΩ±20%	75 VAC max.**	20 VAC min.**
	200 to 240 VAC	150 to 264 VAC	72 kΩ±20%	150 VAC max.**	40 VAC min.**
G3NA-4□□B	5 to 24 VDC	4 to 32 VDC	5 mA max.*	4 VDC max.	1 VDC min.
G3NA-D210B	100 to 240 VAC	75 to 264 VAC	72 kΩ±20%	75 VAC max.	20 VAC min.

Note: The input impedance is measured at the maximum value of the rated supply voltage (for example, with the model rated at 100 to 120 VAC, the input impedance is measured at 120 VAC).
*With constant current input circuit system. The impedance for the G3NA-□□□B-UTU is 15 mA max.
**Refer to the *Engineering Data* for further details.

Output

Model	Applicable load				
	Rated load voltage	Load voltage range	Load current		Inrush current
			With heat sink*	Without heat sink	
G3NA-205B	24 to 240 VAC	19 to 264 VAC	0.1 to 5 A	0.1 to 3 A	60 A (60 Hz, 1 cycle)
G3NA-210B			0.1 to 10 A	0.1 to 4 A	150 A (60 Hz, 1 cycle)
G3NA-410B	200 to 480 VAC	180 to 528 VAC	0.2 to 10 A	0.2 to 4 A	
G3NA-220B	24 to 240 VAC	19 to 264 VAC	0.1 to 20 A	0.1 to 4 A	220 A (60 Hz, 1 cycle)
G3NA-420B	200 to 480 VAC	180 to 528 VAC	0.2 to 20 A	0.2 to 4 A	
G3NA-240B	24 to 240 VAC	19 to 264 VAC	0.1 to 40 A	0.1 to 6 A	440 A (60 Hz, 1 cycle)
G3NA-440B	200 to 480 VAC	180 to 528 VAC	0.2 to 40 A	0.2 to 6 A	
G3NA-450B	200 to 480 VAC	180 to 528 VAC	0.2 to 50 A	0.2 to 6 A	
G3NA-D210B	5 to 200 VDC	4 to 220 VDC	0.1 to 10 A	0.1 to 4 A	20 A (10 ms)

*When OMRON's heat sink (refer to the accessories) or a heat sink of specified size is used.

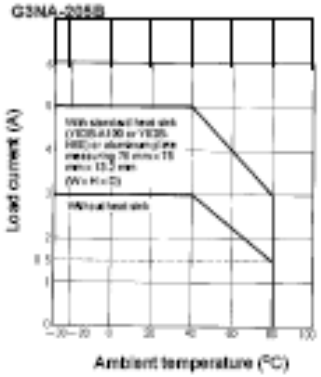
■ Characteristics

Item	G3NA-205B, -210B, -220B	G3NA-240B	G3NA-410B, -420B, -440B, -450B	G3NA-D210B
Operate time	1/2 of load power source cycle + 1 ms max. (DC input) 3/2 of load power source cycle + 1 ms max. (AC input)			1 ms max. (DC input) 30 ms max. (AC input)
Release time	1/2 of load power source cycle + 1 ms max. (DC input) 3/2 of load power source cycle + 1 ms max. (AC input)			5 ms max. (DC input) 30 ms max. (AC input)
Output ON voltage drop	1.6 V (RMS) max.		1.6 V (RMS) max.	1.5 V max.
Leakage current	5 mA max. (at 100 VAC) 10 mA max. (at 200 VAC)		10 mA max. (at 200 VAC) 20 mA max. (at 400 VAC)	5 mA max. (at 200 VDC)
Insulation resistance	100 MΩ min. (at 500 VDC)			
Dielectric strength	2,500 VAC, 50/60 Hz for 1 min			
Vibration resistance	Malfunction: 10 to 55 Hz, 1.5-mm double amplitude			
Shock resistance	Malfunction: 1,000 m/s^2			
Ambient temperature	Operating: −30°C to 80°C (with no icing or condensation) Storage: −30°C to 100°C (with no icing or condensation)			
Approved standards	UL508 File No.E84562/CSA C22.2 (No.0, No.14) File No.LR35535 TÜV R9151660 (EN60950)			
Ambient humidity	Operating: 45% to 85%			
Weight	Approx. 80 g	Approx. 70 g	Approx. 80 g	Approx. 70 g

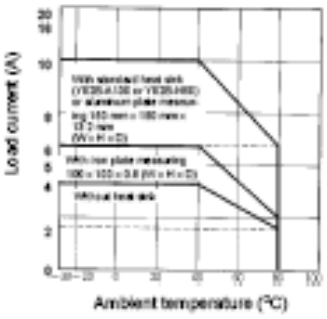
Engineering Data

Load Current vs. Ambient Temperature Characteristics

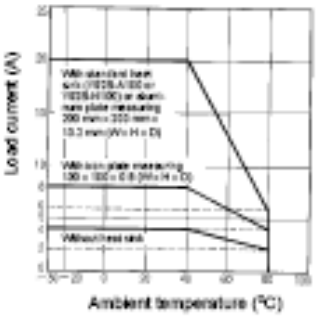
G3NA-205B



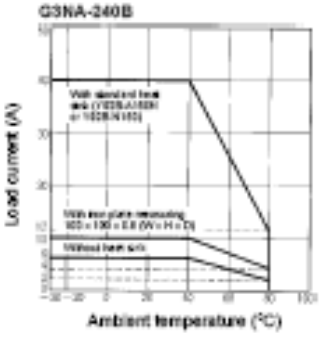
G3NA-210B/410B



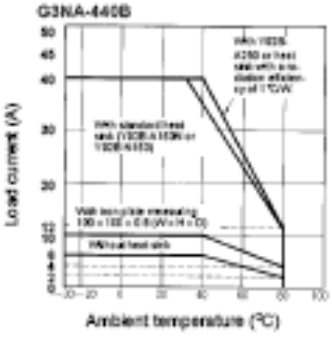
G3NA-220B/420B



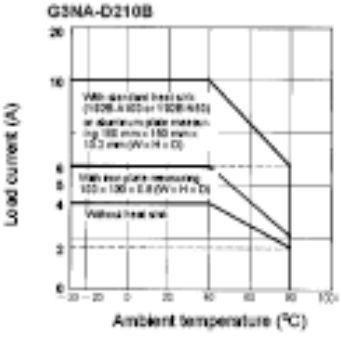
G3NA-240B



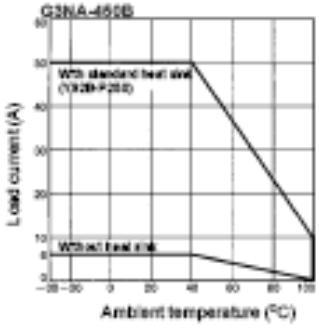
G3NA-440B



G3NA-D210B



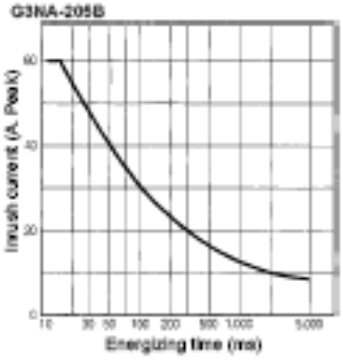
G3NA-450B



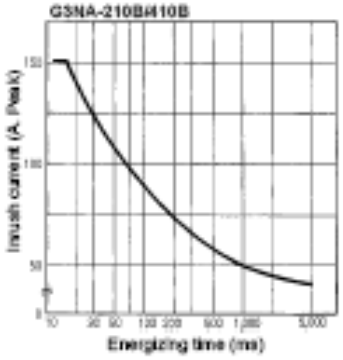
Inrush Current Resistivity

Non-repetitive (Keep the inrush current to half the rated value if it occurs repetitively.)

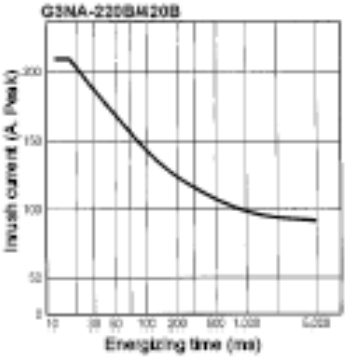
G3NA-205B



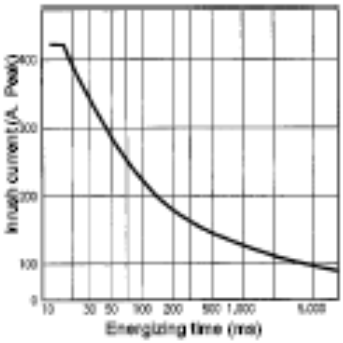
G3NA-210B/410B



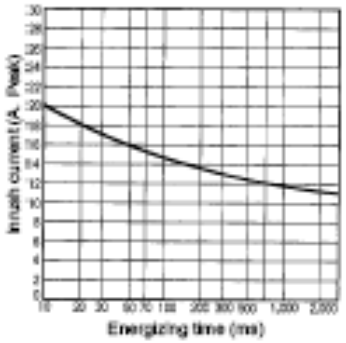
G3NA-220B/420B



G3NA-240B/440B/450B

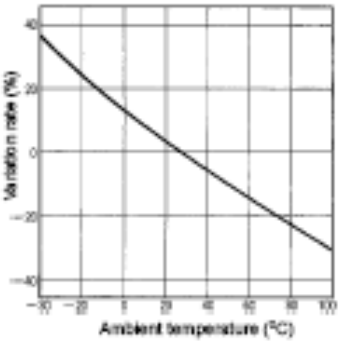


G3NA-D210B



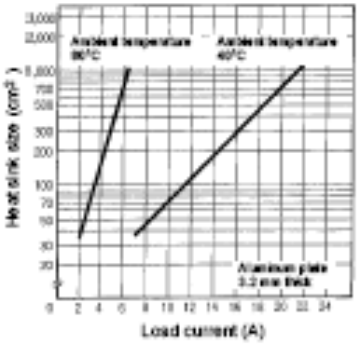
Temperature Characteristics (with Must Operate Voltage and Must Release Voltage)

G3NA-2□□B AC Input



Heat Sink Size vs. Load Current

G3NA-220B



Note: The heat sink size refers to the combined area of the sides of the heat sink that radiate heat. For example, when a current of 15 A is allowed to flow through the SSR at 40°C, the graph shows that the heat sink size is about 450 cm². Therefore, if the heat sink is square, one side of the heat sink must be 15 cm ($15^2 \times 2 = 450$) or longer.

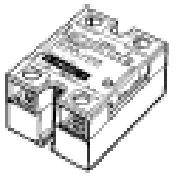
Dimensions

Note: All units are in millimeters unless otherwise indicated.

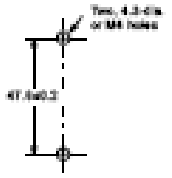
In the case of surface mounting, a 30% derating of the load current is required.

The orientation indicated by the external dimensions is not the correct mounting orientation. When opening mounting holes, refer to the mounting hole dimensions.

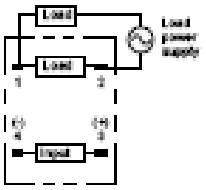
G3NA-205B, G3NA-210B, G3NA-220B, G3NA-410B, G3NA-420B



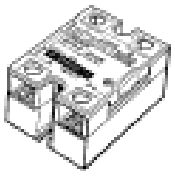
Mounting Holes

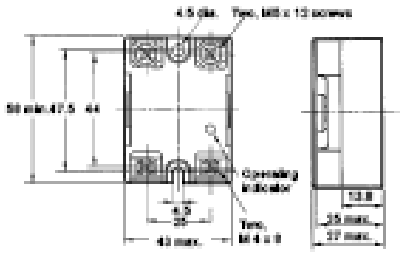


Terminal Arrangement/ Internal Connections (Top View)

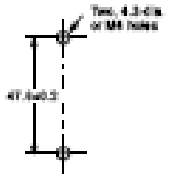


G3NA-240B, G3NA-440B, G3NA-450B

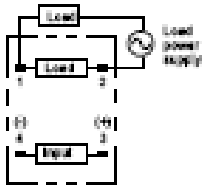




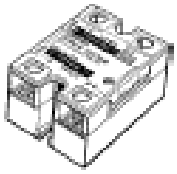
Mounting Holes



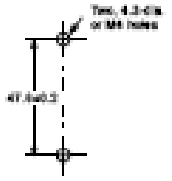
Terminal Arrangement/ Internal Connections (Top View)



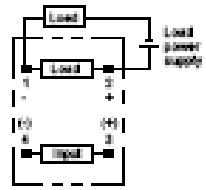
G3NA-D210B



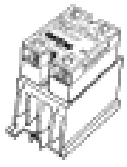
Mounting Holes



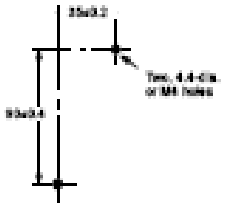
Terminal Arrangement/ Internal Connections (Top View)



Heat Sink
Y92B-N50

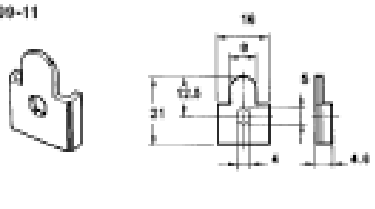


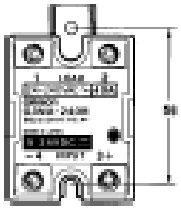
Mounting Holes



Weight: approx. 200 g

R89-11





Use Mounting Bracket R89-11 so that the G3NA-240B can be mounted with the same pitch as that of the G3N-240B.

Precautions

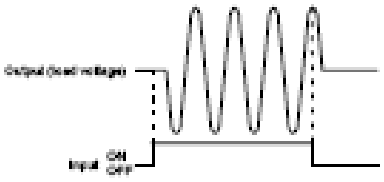
Refer to pages 11 to 19 for general precautions.

Load Connection

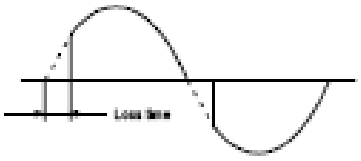
For an AC load, use a power supply rated at 50 or 60 Hz.
The maximum operating frequency is 10 Hz.
The G3NA has a built-in varistor for overvoltage protection.

Zero Cross Function

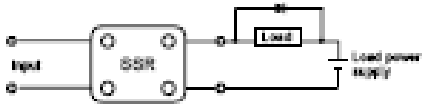
An SSR with a zero cross function operates when an AC load voltage reaches the zero point or its vicinity. This reduces clicking noises when the load is input, and minimizes the influence of an inductive load, such as a lamp, heater, or motor, on the power supply because the inrush current of the load is reduced. This can also minimize the scale of the inrush current protection circuit.



At a low applied voltage, such as 24 VAC, the load current is not fully supplied. When the Unit is switched ON, the voltage required to power the Unit deprives the output signal of the necessary voltage level and thus creates loss time. The lower the load voltage is, the greater the loss time is. This condition, however, will not create any serious problems.



For a DC or L load, a diode should be connected in parallel the load to absorb the counter electromotive force of the load.

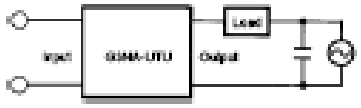


When attaching a heat sink to the G3NA, apply Silicone Grease or equivalent heat conductive grease on the heat sink. (Toshiba Silicon, Shinetsu Silicon, etc.)

Tighten the mounting screws of the heat sink with a torque of 0.78 to 0.98 N • m.

EN55011 Measurement of Mains Terminal Disturbance Voltage

The G3NA-UTU conforms to EN55011 standards when a capacitor is connected to the load power supply as shown in the following circuit diagram.



Recommended Capacitor:
Nissei Denki's MKT-series R40 (1 μF)

The output terminal side of the G3NA-D210B is connected to a built-in diode for protecting the SSR from damage that may result from reverse connection. The SSR, however, cannot withstand one minute or more if the wires are connected in reverse order. Therefore, pay the utmost attention not to make polarity mistakes on the load side.

ALL DIMENSIONS SHOWN ARE IN MILLIMETERS.
To convert millimeters into inches, multiply by 0.03937. To convert grams into ounces, multiply by 0.03527.

APPENDIX G

AR-ELCB Hardware Picture

Figure A1: Auto Re-closer ELCB with casing

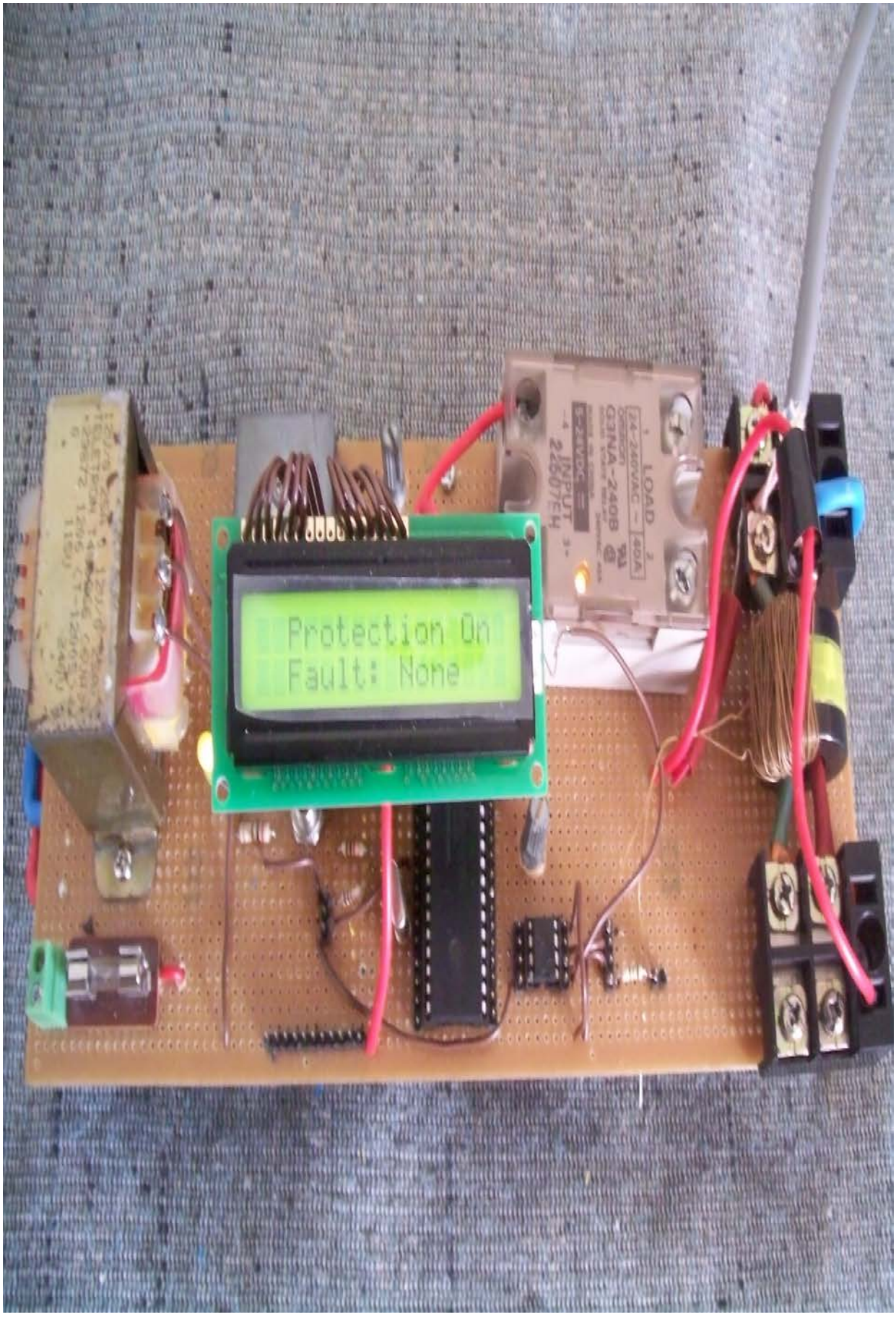

Protection On
Fault: None

Figure A2: Auto Re-closer ELCB without casing

APPENDIX H

Biodata of the Author

AUTHOR'S BIODATA

Mohd Tarmizi bin Rahim was born on 10th September 1985 in Muadzam Shah, Pahang. His permanent address is at 226, Felda Keratong 9, 26700 Muadzam Shah, Pahang. He is an youngest brother from six siblings, he has one brother and four sister. His first education is Sekolah Rendah Perantau Damai. After 5 year searching for knowledge there, he enter his secondary education at Sekolah Mengah Perantau Damai. Soon after three year there, he got an opportunity to advance his study to technical school which are Sekolah Menengah Teknik Dungun. He completed his studies there in Electrical Engineering course at 2003. Then he has been accepted to study in Science physics course at Pahang Matriculation College from 9 May 2004 until 14 April 2005. He is currently (2009) a Bachelor's student in the Electrical Engineering (Power System), faculty of Electrical and Electronics Engineering, University Malaysia Pahang. His research fields are power electronics and power system. He is a student member of the IEM of Malaysia.