DEVELOPMENT OF SPEED CONTROLLER FOR INVERTER FED INDUCTION MOTOR

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This thesis is submitted as partial fulfillment of the requirements for the award of the Bachelor Degree of Electrical Engineering (Power System)

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DISEMBER 2010

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To my beloved mother, father, and brothers

"I hereby acknowledge that the scope and quality of this thesis is qualified for the award of the Bachelor Degree of Electrical Engineering (Power System)"

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Date : _____

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In the name of ALLAH, Most Generous and Most Merciful

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ABSTRACT

Normally variable speed control was performed by some type of d.c. motor. Today, the development of power semiconductors has resulted in the utilization of inverter circuits for variable speed control of induction motor. This project is to develop the application of inverter which can control the speed of induction motor by using PI controller. Inverters are circuit that convert DC to AC. The function of inverter is to create an AC voltage by using a DC voltage source, the voltage source that used DC voltage commonly batteries. Pulse Width Modulation (PWM) technique is considered as one solution for harmonic reduction and increasing the motor efficiency. Previous study regarding the performance on the traditional Pulse Width Modulation (PWM) inverter is carried out and it was found that the performance is not ideal. Therefore an improvement on the traditional PWM inverter is carried out by inserting a Proportional Integral (PI) controller to regulate and stabilize the output voltage of the inverter. This work was applied close-loop variable speed drive for single-phase induction motor using voltage control. The proposed drive system is simulated using Matlab/ Simulink, its results were compared with the hardware experimental results. The simulation and laboratory results proved that the drive system could be used for the speed control of a single phase induction motor with wide speed range.

ABSTRAK

Biasanya kawalan kelajuan boleh laras dilakukan oleh beberapa jenis dc motor. Sekarang ini, perkembangan semikonduktor kuasa telah mengakibatkan penggunaan litar penyongsang untuk kawalan kelajuan boleh laras projek motor aruhan. Ini adalah untuk mengembangkan aplikasi penyongsang yang boleh mengawal kelajuan motor aruhan dengan menggunakan teknik PWM. Penyongsang adalah litar yang menukarkan DC ke AC. Fungsi penyongsang adalah untuk menghasilkan voltan AC dengan menggunakan sumber voltan DC, sumber voltan yang digunakan oleh voltan DC biasanya bateri. Kaedah permodulatan lebar denyut (PLD) dianggap sebagai salah satu penyelesaian untuk mengurangkan harmonik dan meningkatkan kecekapan motor. Kajian tentang ciri-ciri dan prestasi sesebuah penyongsang tradisi telah dibuat dan didapati prestasinya tidak begitu memuaskan. Justeru pengawal PI telah digunakan dalam Pemodulatan Lebar Denyut (PWM) penyongsang bagi mengawal dan menstabilkan voltan keluaran penyongsang. Kerja ini mengaplikasikan kawalan kelajuan boleh laras gelung tertutup untuk motor aruhan satu fasa menggunakan kaedah kawalan voltan. Sistem pemacu yang telah dicadangkan telah disimulasikan menggunakan Matlab /Simulink. Keputusannya telah dibandingkan dengan hasil yang diperolehi melalui kaedah eksperimen menggunakan perkakasan yang sebenar. Keputusan simulasi dan eksperimen di dalam makmal membuktikan bahawa sistem pemacu tersebut boleh digunakan untuk mengawal kelajuan motor aruhan satu fasa dengan julat kelajuan yang lebih besar.

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S - Apparent power

V - Voltage

Vo - Output voltage

Vin - Input voltage

Vdc - DC supply voltage

Vrms - rms voltage

Vref - Reference voltage

I - Current

Io - Output current

Iin - Input current

Irms - rms current

R - Resistor

f - Switching frequency

fLC - Cut-off frequency

ma - Modulation index

mf - Modulation frequency

L - Inductor

C - Capacitor

PWM - Pulse Width Modulation

THD - Total harmonic distortion

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1 Background

This chapters are mainly discuss about application of inverter and advantages of the PWM inverter and also the development inverter by using PI controller. The problem, objectives, scopes, methodology and thesis outline also presented in this chapter.

1.2 Overview of the Project

Inverters are circuits that convert direct current (DC) to alternating current (AC). Usually inverters are used to transfer power from a DC source to an AC load. Inverters are mainly used in application such as adjustable-speed AC motor drives, uninterruptible power supply (UPS), and AC appliances run from an automobile battery.

Although inverters are used to convert DC to AC, the output of the inverters usually contains very high total harmonics distortion (THD). Hence measures used to reduce the THD at the output become the concern of the development of inverters.

PWM inverters are members of the inverter family. PWM inverters are favorable in many inverter circuits because PWM inverters manage to eliminate harmonics in a relatively easier way as compare to traditional square-wave inverters. The main advantage of PWM inverter is to shift all the harmonics into a much higher frequency, causing the filter design become easier than the square-wave inverters.

In order to successfully produce output with low THD, a unipolar switching scheme is employed in design of PWM inverter. Besides a linear PI controller is proposed to stabilize the voltage at the output.

1.3 Problem Statement

PWM inverters usually contain higher THD before the filtering process. However, PWM inverters shift the harmonics into higher frequency hence a relatively easier filter can be designed i.e. the cut-off frequency can be placed in the range of kHz hence allowing the components size of LC filter become smaller. Due to rapid development of modern technologies, the control methods that are used in PWM inverters can be categorized into 3 groups, which are model based, non-model based, and mix-based. PI controller being the model-based controller is used in stabilizing the output voltage of the PWM inverters.

1.4 Objectives of the Project

I. To develop inverter for single phase induction motor applications that can generate variable voltages
II. To enhance the performance of a typical PWM inverter using PI controller.
III. Design circuit and analyze the switching characteristics of pulse width modulated inverter.

1.5 The scopes of the Project.

After intensively reviewed on the single-phase unipolar inverter, there are many issues need to be tackled in order to achieve a preliminary objective. The scopes of this thesis are used for the guideline of the project. The project scopes are as follows:

I. Read all significant references and analyse the literature reviews about the operation of inverter, operation of PWM, driver circuit, power circuit.

II. Design a simulation circuit by using MATLAB/SIMULINK software part by part according to the theories and methods that gain from the literature review. Then simulated and analysis the output waveform.

III. Construct the circuit on breadboard based on collected data from simulation part and literature reviews.

1.6 Methodology

The procedure of the analysis is the important factor to ensure that project is completely done as expected, because it is necessary to have an efficient plan and it will help to guide into the target to achieve the objective. There are two parts of study in this project. The first part is simulation part and the second part is experimental part.

1.7 Thesis Outline

Chapter 1 discuss on the background of the project, objectives, scope of the project, methodology and also the thesis outline.

Chapter 2 focuses on literature reviews of this project based on journals and other references.

Chapter 3 mainly discuss on the system design of the project. Details on the progress of the project are explained in this chapter.

Chapter 4 presents the results of the project. The discussion focused on the result based on the experiment.

Chapter 5 concludes overall about the project. Obstacle faces and future recommendation are also discussed in this chapter.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In this chapter, the overview and theories of several fields involve in this dissertation is discussed. These concepts will further help us to understand the upcoming discussion on PWM inverter and its implementation. This chapter also attempts to give brief explanations and elucidate the control theory of PWM inverter. Theory and the operation of the PWM inverter with linear PI controller are discussed in this chapter. Last but not least, a brief review is done on the different controller for PWM inverter.

2.2 AC Motor and Loads

An inverter is an electronic device which inverts DC energy (the type of energy found in batteries) into AC energy. Household appliances such as refrigerators, TVs, lighting, stereos, computer etc., all run off of AC electricity [1]. An AC motor is an electric motor that is driven by an alternating current. The motor is connected to the mains through an AC switch. The AC voltage varies across the motor in phase control mode by means of a microcontroller, which sets the triggering time. The application of AC motor load is refrigerators, TVs, lighting, computer and washing machines power tools and food processors.

Besides that, small single-phase AC motor are usually used to power mechanical clocks, audio turn tables, and tape drives; formerly they were also much used in accurate timing instruments such as strip-chart recorders or telescope drive mechanisms[1]

2.2 Unipolar PWM inverter

Pulse Width Modulation (PWM) provides a way to decrease the THD of the output signal. In PWM, the amplitude of the output voltage can be controlled with the modulating waveforms. For a PWM inverter, it required a reference signal (usually a sinusoidal signal) and a carrier signal (a triangular wave that controls the switching frequency). The operation of a unipolar PWM inverter is first comparing the reference voltage (Vref) to a reference triangular waveform (Vtri). The principle is shown in Figure 2.1 below [2].

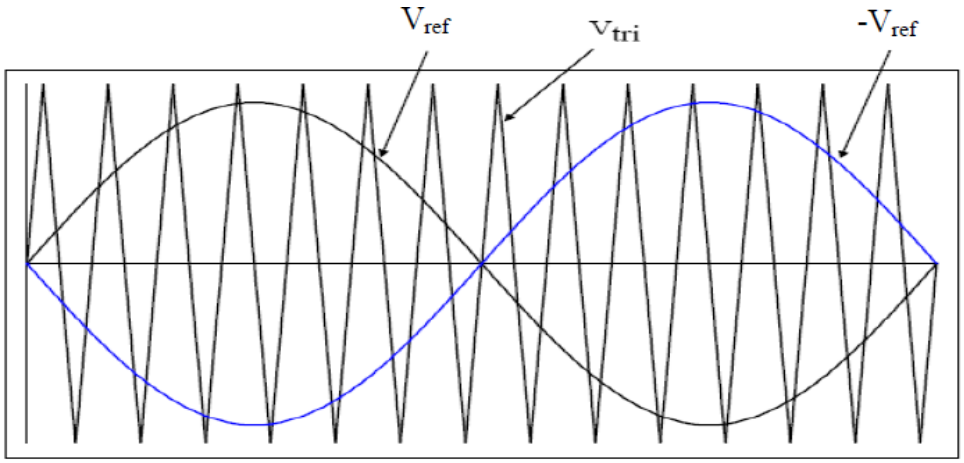

Figure 2.1: Basic PWM Principle of Operation

Based on Figure 2.1, ma = 0.9 where ma is the ratio of peak control voltage to peak triangle voltage that is ——. The logic is used to operate the four switches in the H-Bridge configuration of Figure 2.2 is as follows [2]:

i. Vref > Vtri , close switch A+, open switch A– , so voltage Va = Vdc
ii. Vref < Vtri , open switch A+, close switch A– , so voltage Va = 0
iii. –Vref > Vtri , close switch B+, open switch B– , so voltage Vb = Vdc
iv. –Vref< Vtri , open switch B+, close switch B– , so voltage Vb = 0

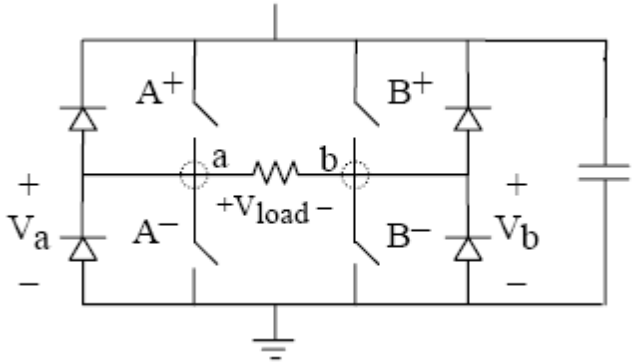

Figure 2.2: Four MOSFET Switches (A+, A-, B+, B-) Configured as an H-Bridge

The resulting voltage across the load (Vab) under unipolar switching scheme is shown in Figure 2.3 below. [2]

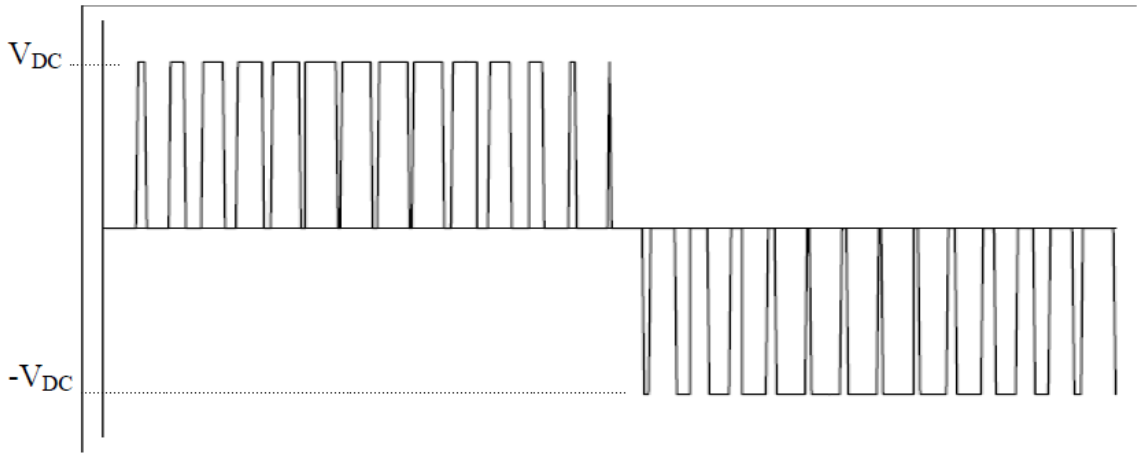

Figure 2.3: Load voltage at ma = 0.9

The output voltage shown in Figure 2.3 before filtering contains very high THD. Hence a filter has to be designed to eliminate the harmonics at the output signal. For unipolar PWM inverter, the harmonics only exist in the order of 2mf, 4mf, 6mf and others, where modulation frequency, =——., where ftri is the frequency of triangular signal and fref is the frequency of the sinusoidal signal respectively. Since in most application, high switching frequency around 20 kHz is employed in PWM inverter, thus the harmonics are all shift to very high frequency allowing the design of LC filter becoming easier.

2.3 Total Harmonic Distortion (THD)

Total Harmonic Distortion is a term that is used to quantify the non-sinusoidal property of a waveform. Smaller THD allows the components in a loudspeaker, amplifier or microphone or other equipment to produce a more accurate reproduction in electronics and audio media [3]. Since the objective of the inverter is to use a DC voltage as input source to supply a load requiring AC voltage and current, the quality of the AC output can be described in THD terms. Table 2.1 shows the Normalized Fourier Coefficient Vn/Vdc for unipolar PWM inverter. [6]

Table 2.1: Normalized Fourier Coefficient Vn/Vdc for Unipolar PWM Inverter.

ma	1.0	0.9	0.8	0.7	0.6	0.5	0.4	0.3	0.2	0.1
n = 1	1.00	0.90	0.80	0.70	0.60	0.50	0.40	0.30	0.20	0.10
n = 2mf±1	0.18	0.25	0.31	0.35	0.37	0.36	0.33	0.27	0.19	0.10
n = 2mf±3	0.21	0.18	0.14	0.10	0.07	0.04	0.02	0.01	0.00	0.00

2.4 State Space Inverter Model

PWM inverter is non-linear in nature due to the existence of the solid state switches. Hence both linearization and averaging of the PWM are the initial steps before designing suitable controller for the inverter. Referring to Figure 2.4 below, with the assumption of switching frequency is more than 10 kHz, the PWM inverter can be represented by a DC voltage source, Va with a value of Vcont * KPWM where KPWM = Vdc/Vtri. By choosing the inductor current, iL and output voltage, Vout as the system

variables, the state space model of the equivalent circuit can be formed as shown in Figure 2.5. The state-space inverter model shown in Figure 2.5 is the basic to develop a controller for the PWM inverter.

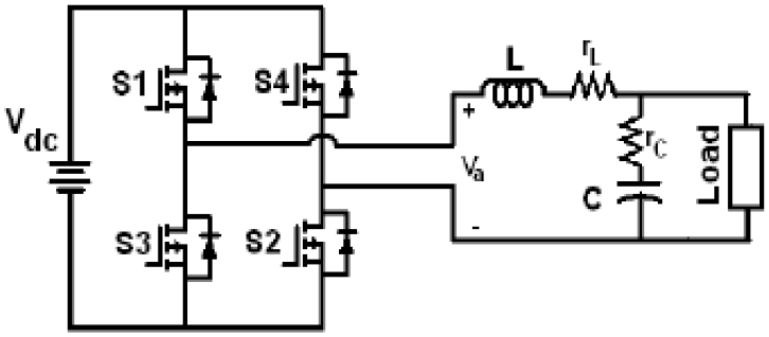

Figure 2.4: Typical Single Phase Inverter Circuit

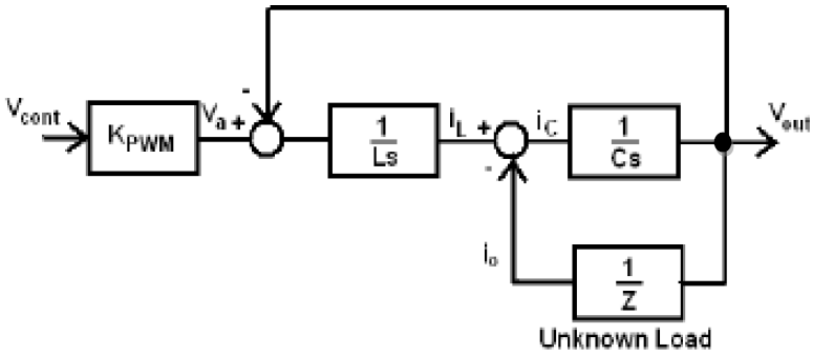

Figure 2.5: State-Space Inverter Model Block Diagram

2.5 Linear PI Controller

The controller for PWM inverter can be categorized into 3 groups which are model-based, non-model based and mix based [1]. Figure 2.6 shows the types of controller available in PWM inverter.

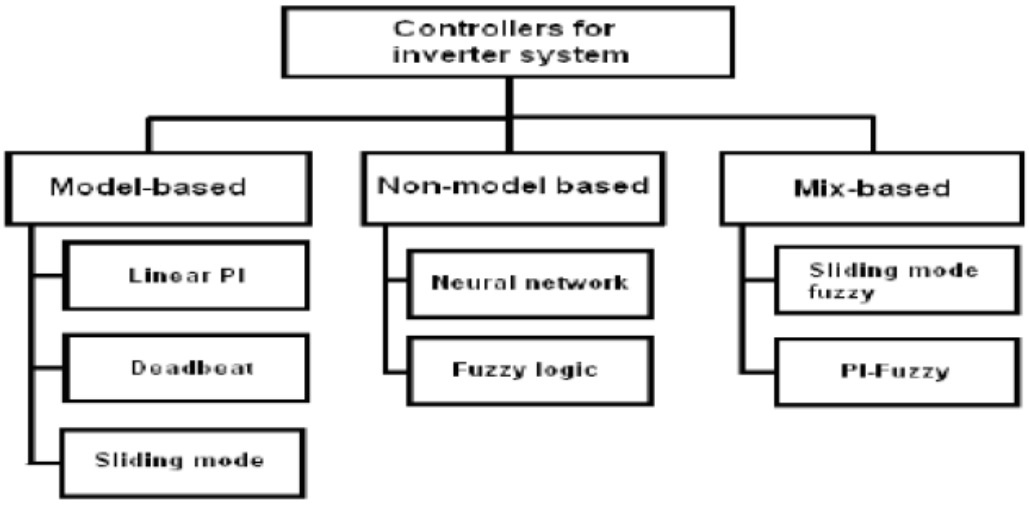

Figure 2.6: Classification of Controllers for PWM Inverter

Among the prominent model-based controller that has been used to regulate an inverter system is the Linear PI controller [1]. PI controller is simple to understand as well as to implement. However the PI controller can only produce excellent performance under limited operating range (i.e. load variation within a close neighborhood of the operating point).

Usually in PI controller, the most popular tuning method is the frequency response analysis. The main advantage of this method is that it provides a graphical approach to the system stability and performance while tuning the PI controller. Under this method, Bode diagram is used to determine the gain margin, phase margin and the stability of the system. In most power converters application, the phase margin is chosen to be around 45° to 60° to ensure that there is less oscillation for the transient dynamics [1]. The gain margin however is chosen to be wide enough to provide the fastest dynamic response.

2.6 Feed-Forward PI Controller

Besides the linear PI controller, there is also non-linear PI controller being used in PWM inverter. The non-linear PI controller also known as feed-forward controller is actually derived from the linear PI controller. Figure 2.7 shows the feed-forward controller block diagram. [3]

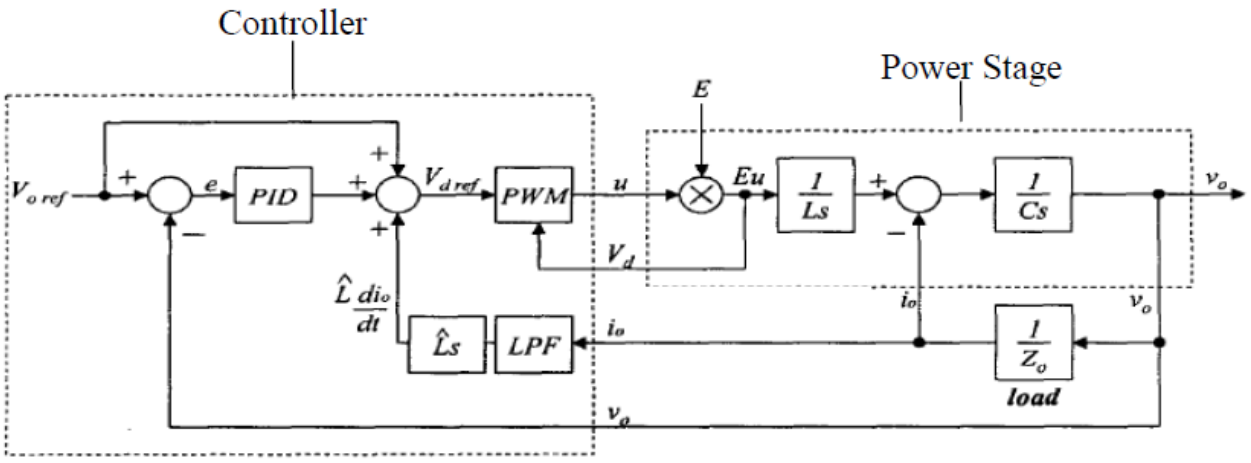

Figure 2.7: Block Diagram of the Feed-Forward Control Scheme

Feed-Forward control scheme is an improvement for a voltage feedback PI controller. The advantages of feed-forward control scheme are having fast transient response, low THD sine wave output voltage, fixed switching frequency and high robustness against load and side step changes.

In feed-forward control scheme, a multi-loop control structure involving the voltage loop and current loop is employed [3]. In this control structure, options can be made either to choose inductor current or capacitor current as the feedback current loop. If the inductor current is chosen, various decoupling methods (feed-forward loop) can be applied, which eliminates the load effect and hence enhance the controller robustness. Figure 2.8 below shows the multi-loop feed-forward control scheme.

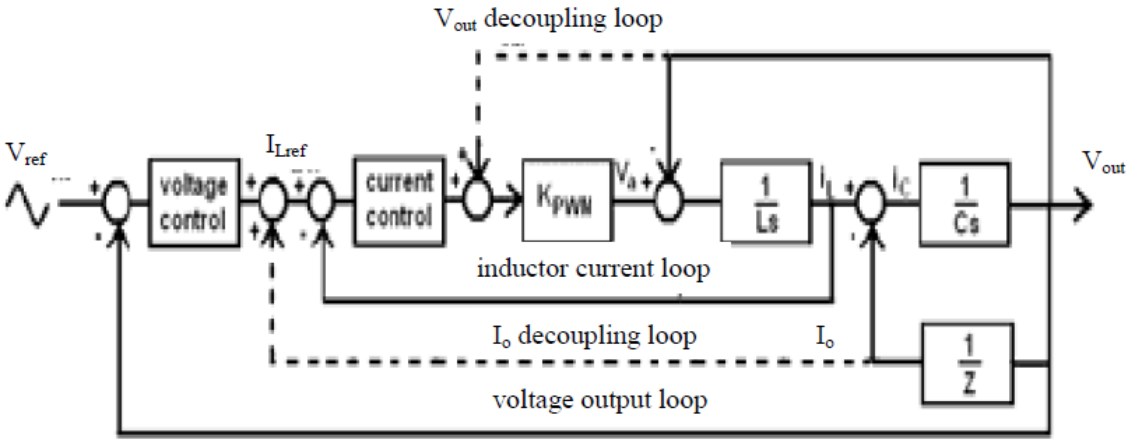

Figure 2.8: Multi-Loop Feed-Forward Control Scheme

2.7 Development in PWM Controller

Due to the rapid development of modern technology, the analog controller for PWM inverter is being replaced by digital controller. The most common digital controller for PWM inverter is based on digital signal processing (DSP) and the controller is known as deadbeat controller [5]. The advantage of deadbeat controller is the output THD can be less than 1% in present of unknown load. However the theory of deadbeat controller is harder and the controller is hard to develop as compare to the PI controller. Besides, Fuzzy Logic Controller (FLC) has been widely applied on inverters through various control schemes. FLC can be used in either direct control scheme, feed forward compensator along with other linear controllers and as a gain scheduler for a PI controller. FLC has the advantage of high degree of freedom in tuning the control parameters causing it easily modified and can be tuned to approximate different kinds of linear or nonlinear controllers. However, FLC suffers from lack of standard design procedure and long design time cycle.

Next, due to development of AC drives, AC PI controllers have become the concern among other controllers recently. The advantages of AC PI controller are it can eliminate the steady state control error completely and is able to apply in high power PWM inverter. However the AC PI controllers are sensitive to fluctuation of the loading and electric network. Figure 2.9 shows the simplified control system diagram for the AC regulator. [4]

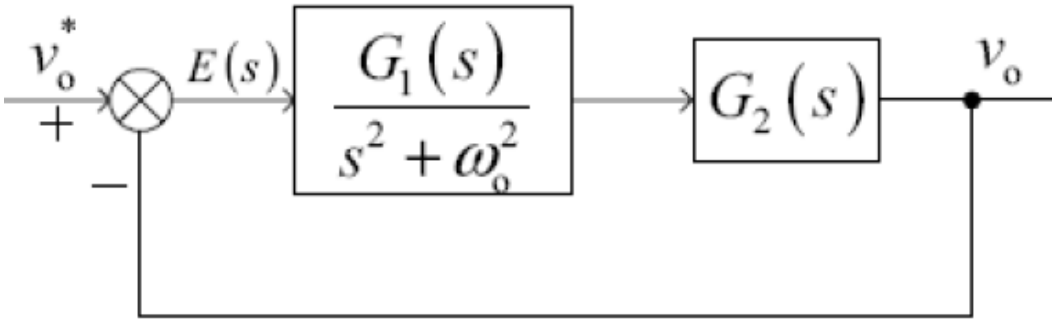

Figure 2.9: Simplified Control System Diagram

CHAPTER 3

PROJECT DEVELOPMENT

3.1 Introduction

This section provides the details on the development of PWM inverter in term of software. MATLAB software is used to model the whole system of the PWM inverter as well as to design a suitable PI controller for the PWM inverter. Steps used to implement the PWM inverter is discussed in details in this chapter. Preliminary outcomes of the project is discussed in this chapter as well.

3.2 Methodology

The development methodology of the project can be divided into 4 major categories. They are:

i. Background Study
ii. Software Development
iii. Hardware Development
iv. Testing and Improvement

3.2.1 Background Study

The basic concept of inverter has to be studied first before choosing a suitable controller for the inverter. Next the performances of a PWM inverter need to be understood by studying the switching scheme of the PWM inverter and the application of PWM inverter. Several articles regarding the PWM inverter are read through in order to know the recent development of PWM inverter and its application in industry.

3.2.2 Software Development

An inverter is an electrical device that converts direct current (DC) to alternating current (AC); the resulting AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits. Figure 3.1 below shows the basic configuration of the inverter circuit.

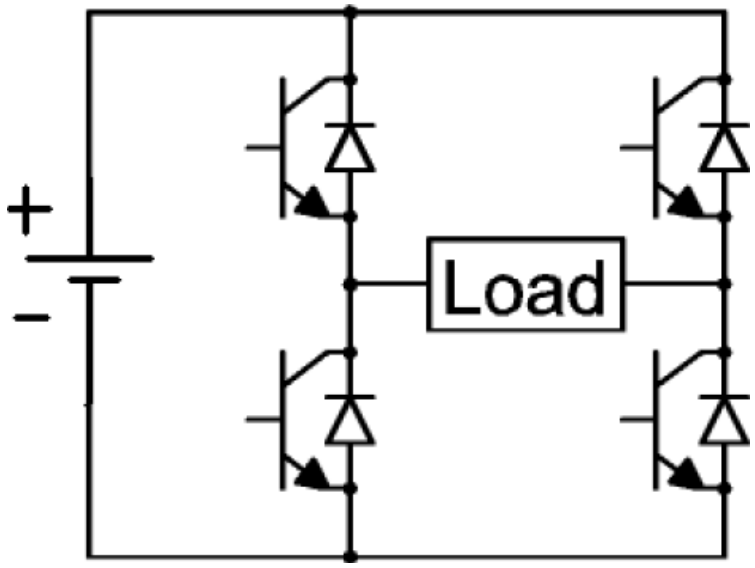

Figure 3.1: Basic Configuration of an Inverter

The output of the inverter is a square wave which contains lots of harmonics. Hence a low pass filter is usually installed at the output side to filter all the unwanted harmonics in order to obtain a pure sinusoidal output wave. In this case, PWM inverter is used because it is able to shift the harmonics into a higher frequency hence making the low pass filter becoming easier to design. The PWM inverter is modeled using MATLAB and the configuration of the PWM inverter is shown in Figure 3.2 below.

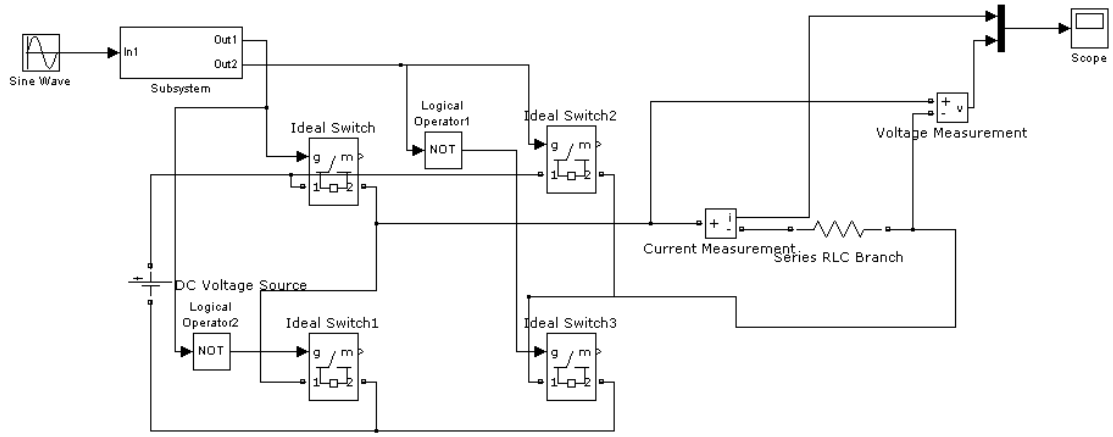

Figure 3.2: PWM Configuration in MATLAB

The switching scheme that is employed in this PWM inverter is the unipolar switching scheme. By referring to Figure 2.1 and Figure 2.2, the switching scheme of a unipolar PWM inverter can be modeled as shown in Figure 3.3 below. Both relational operators act as comparator whereby sine wave from Figure 3.2 is compared with the triangular signal. If the magnitude of the sine wave is higher than the triangular signal, it will produce an output of logic 1 and vice versa. Gain of -1 is used to invert the sine wave signal before comparing with the triangular signal.

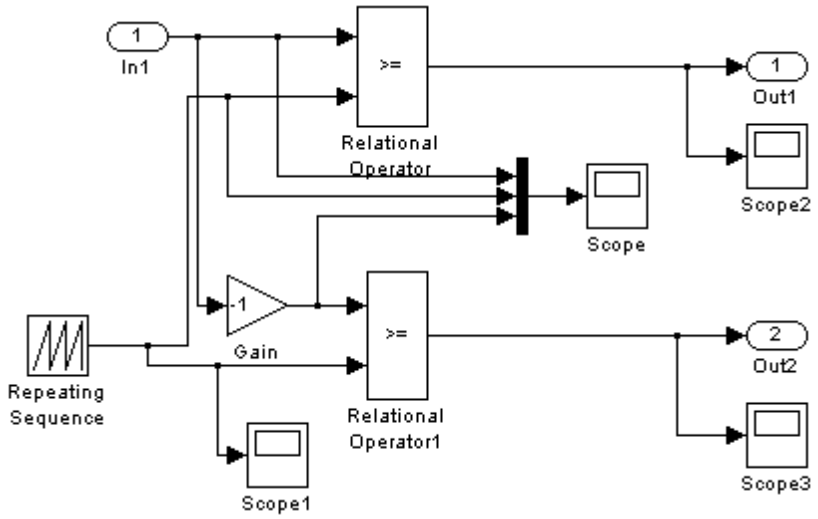

Figure 3.3: Unipolar Switching Model

The result of the PWM inverter before filtered (Pin a-b as in Figure 3.2) is shown in Figure 3.4 below. It can be observed that the output voltage is an AC square wave and the output current is in sinusoidal waveform. In this case, DC supply voltage of 15 V, mf = 200 and ma = 1 are used. Both the output voltage and output current contain very high THD. Hence a filter has to be designed in order to filter all the unwanted harmonics.

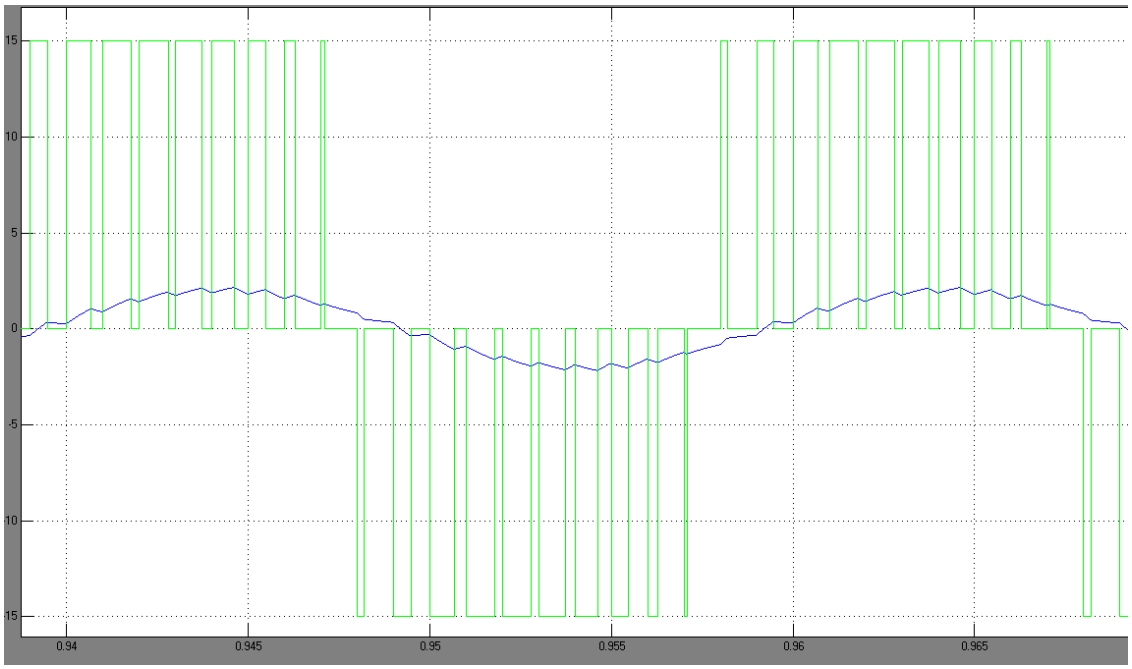

Figure 3.4: Output of PWM Inverter Before Filtered

3.2.3 Data Analysis

This subsection will further discuss the effect of modulation index toward the output signal. As described earlier, modulation index, ma is the ratio between sinusoidal magnitudes against the triangular magnitude. By altering the value of modulation index, different output magnitude can be obtained. The input DC voltage is 12 V with switching frequency of 10 kHz. Four different cases with ma equals to 1.0, 0.8, 0.5 and 1.2 are simulated and the results of inverter output voltages are shown in Figure 3.6, Figure 3.7, Figure 3.8 and Figure 3.9 respectively whereby the circuit of PWM inverter is shown in Figure 3.5.

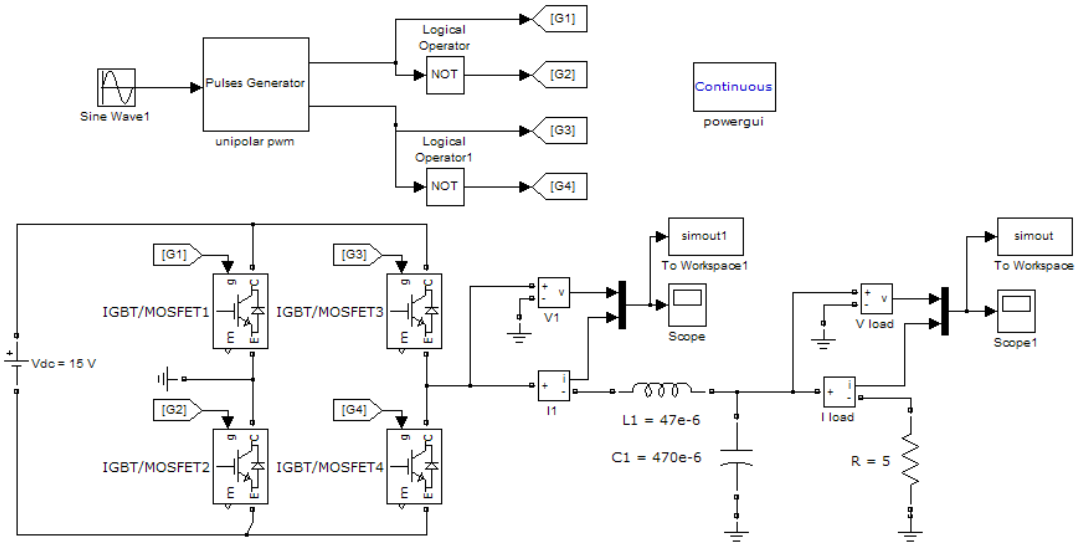

Figure 3.5: PWM Inverter

1. $M_{a=}1.0$

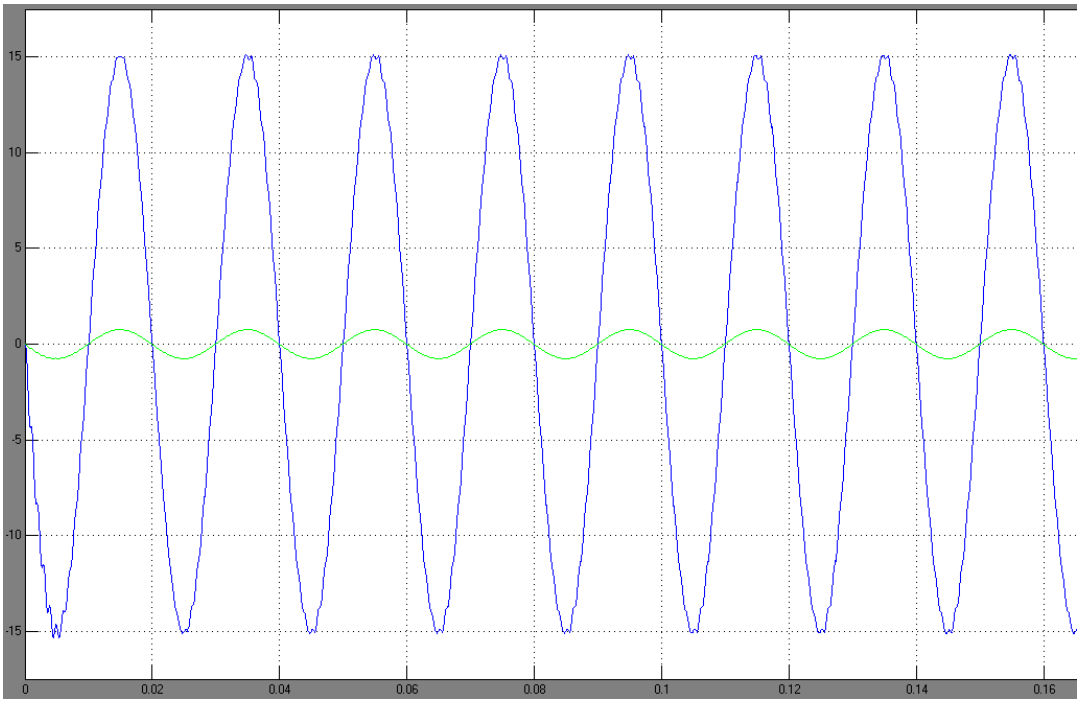

Figure 3.6: Output Voltage at ma = 1.0

2. $M_{a=}0.8$

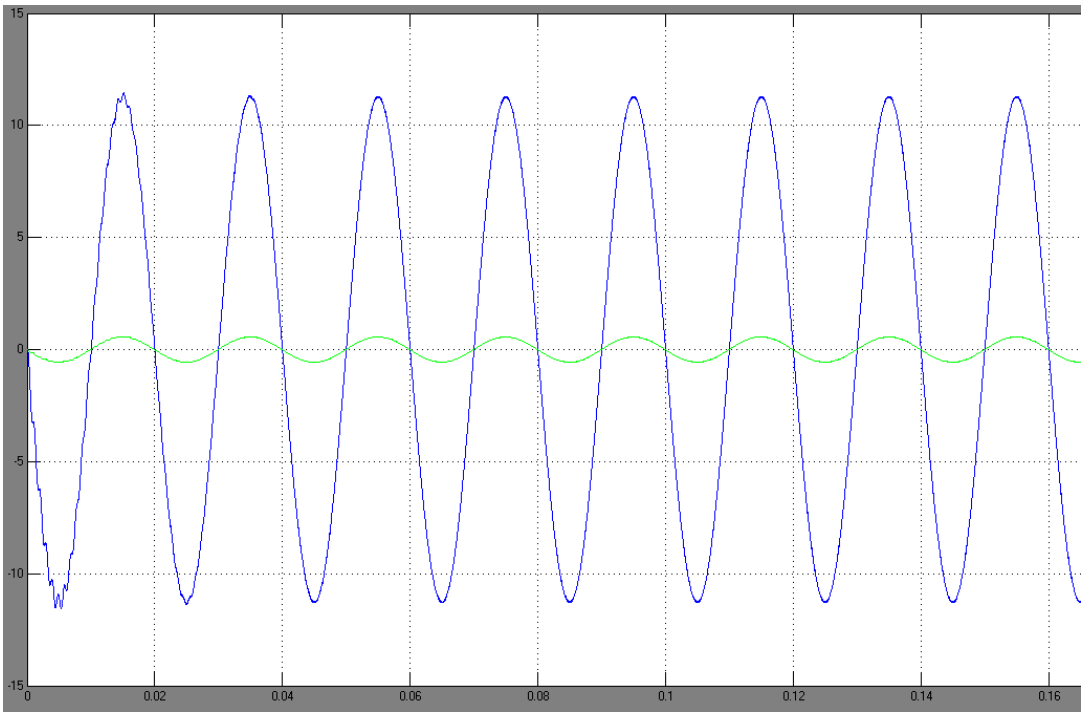

Figure 3.7: Output Voltage at ma = 0.8

3. Ma = 0.5

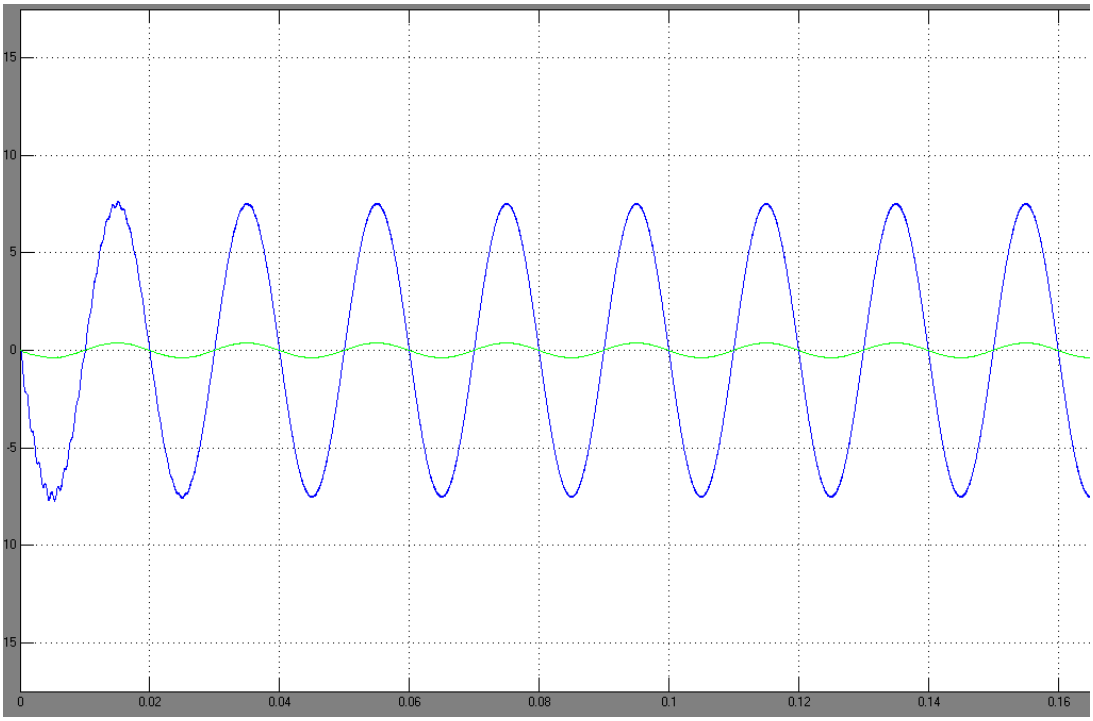

Figure 3.8: Output Voltage at ma = 0.5

4. Ma = 1.2

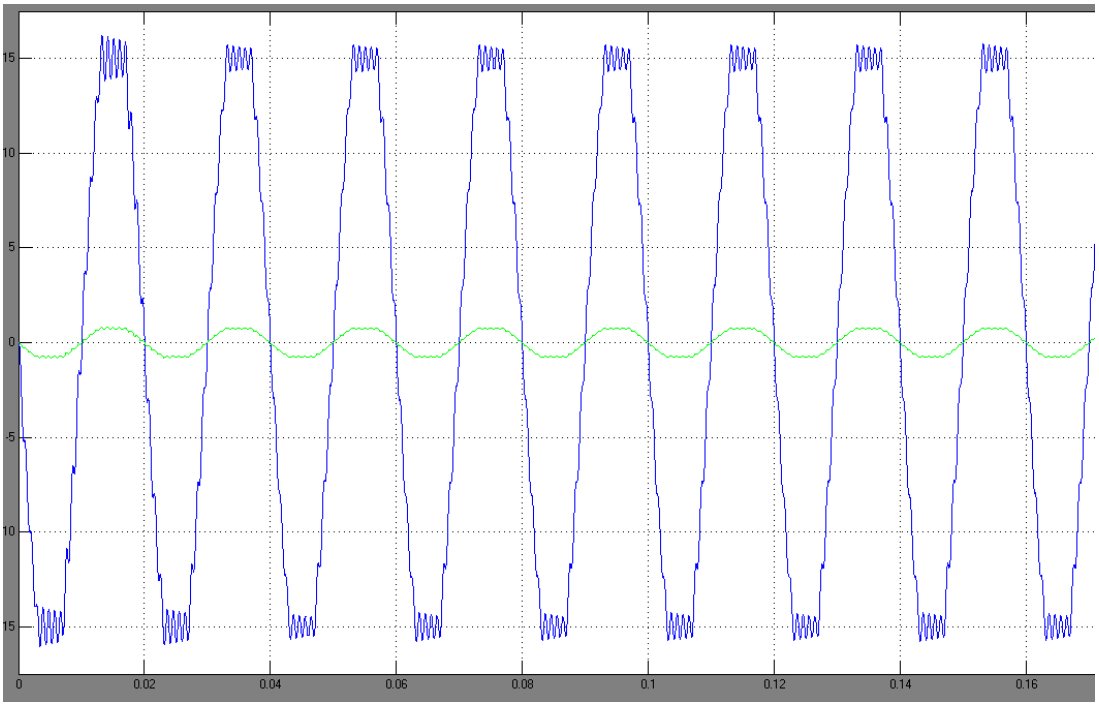

Figure 3.9: Output Voltage at ma = 1.2

The plots shown in Figure 3.5 to Figure 3.8 are summarized in Table 3.1 below:

Table 3.1: Modulation Index and Output Magnitude with VDC = 15V

Modulation index, ma	Theoretical value (Vo = maVdc)	Output magnitude, Vo
1.2	N/A	22
1.0	15	21
0.8	12	12
0.5	6	6

It is clearly shown in Table 3.1 that the output magnitude is depending on the modulation index m_a. The lower the modulation index, the lower the magnitude value is. The formula to calculate the output magnitude is given as Vo = ma Vdc. This formula is valid only when ma is less than 1.0. This is because when ma is greater than 1, the output magnitude is increased but it increases nonlinearly, hence the value of output magnitude cannot be calculated when ma > 1. By controlling the modulation index (varied the sinusoidal magnitude), the desired output voltage can be obtained.

3.2.4 Design Specification

After knowing the performance of the PWM inverter, the specification of PWM inverter is calculated and the PWM inverter circuit is refined with the appropriate values. In order to design a PWM inverter, first the DC input of the inverter is fixed at

15 V and the peak output voltage, Vop is fixed at 12 V with output peak current of Iop = 2.4 A. The load is a computer load (R load) and switching frequency is chosen to be 20 kHz. The calculation is shown in the steps below

i. Determine the R load:

$$= \frac{}{} = \frac{}{} = 5\ \Omega$$

ii. Determine modulation index, m_a:

$$= {}_a$$

$${}_a = \frac{}{} = 0.80$$

iii. Determine modulation frequency, m_f:

$${}_f = \frac{}{} = \frac{}{} = 200$$

iv. Determine inductance L and capacitance C:

$$= \frac{}{}$$

Assume the cut-off frequency fLC = 1 kHz, choose the capacitance value to be C = 470 μF hence the inductance can be calculated using the formula above, L = 53.89 μH, hence choose L = 47 μH. v. Determine the rms output voltage and current after filter:

$$= \frac{}{} = 8.49$$

$$= \frac{}{} = 1.70$$

The specification of the PWM inverter is summarized as shown in Table 3.2 below:

Table 3.2 Specification of the PWM Inverter Output

Vdc	15 V
Vop	12 V
Vorms	8.49 Vrms
Iop	2.4 A
Iorms	1.70 Arms
Switching Frequency, f	10 kHz
Modulation index (ma)	0.80
Modulation frequency (mf)	200
L	47 μH
C	470 μF
R	5 Ω

3.2.5 Small Signal Analysis

In order to determine the value of PI controller, small signal analysis is required. Figure 3.10 below shows the block diagram of the small signal model of the PWM inverter that is used to determine the value of Kp and KI. Figure 3.11 shows the Bode plot of the system. From Figure 3.11, it is shown that the phase margin (when gain = 0) is equal to 45° at frequency 1000 rad/s. The Kp and KI values at this phase margin are respectively 0.1 and 0.01respectively The small signal model requires linearization and

averaging of the PWM inverter. Linearization and averaging technique are needed because the PWM inverter is not a linear component. By linearization and averaging technique, the PWM inverter can be modeled as Vdc/Vtri. To analyze the model, open loop system is required to design a suitable controller for the system.

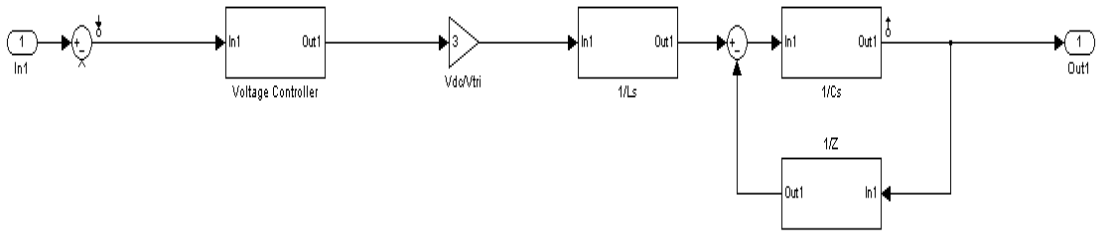

Figure 3.10: Small Signal Model for PWM Inverter

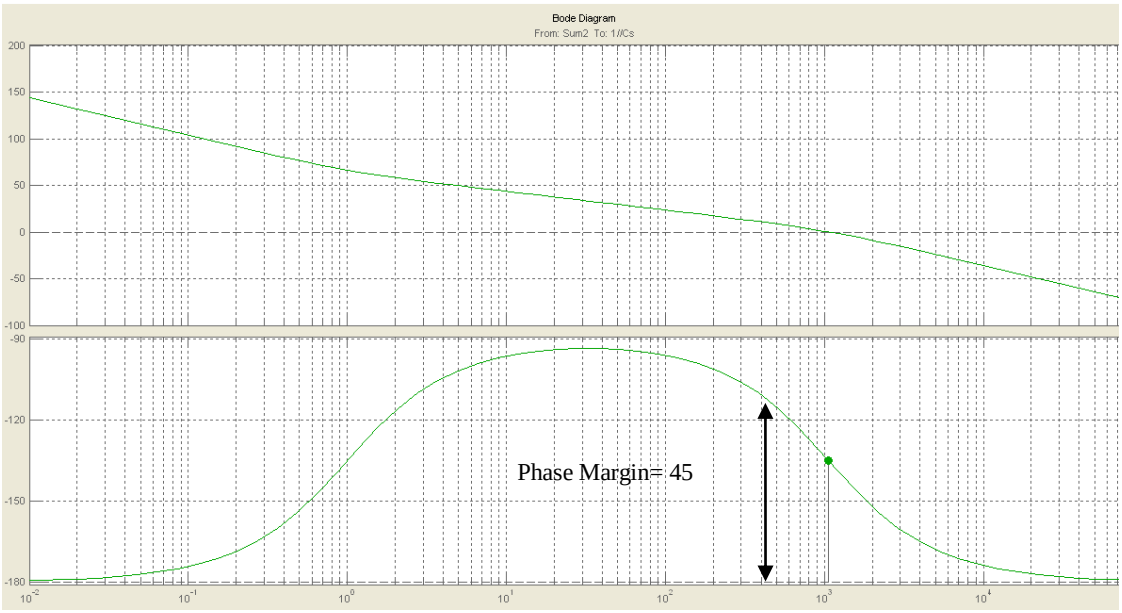

Figure 3.11: Bode Plot of the Small Signal Model

After successfully select the Kp and KI values, the system performances is now analyze through large signal model which is shown in Figure 3.12. The result of the PWM inverter output voltage is shown in Figure 3.13 and the THD results of the PWM inverter are shown in Figure 3.14

3.2.6 Large Signal Analysis

In large signal analysis, first the PWM inverter is tested in open loop condition that is without the feedback. Simulations are carried out to determine the inverter output voltage and its total harmonic distortion (THD). Referring to Figure 3.13, that is the output of the PWM inverter whereby the measurement is taken at pin a-b and it is clearly shown that that the peak output voltage is 12V. Figure 3.12 shows the large signal model of the PWM inverter. The THD of the inverter is shown in Figure 3.14.

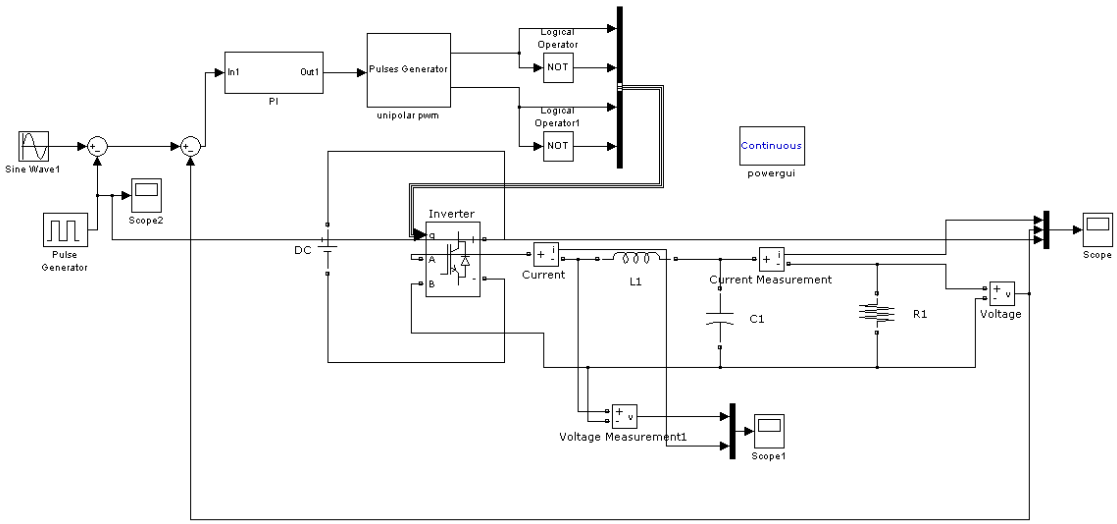

Figure 3.12: Large Signal Model of PWM Inverter

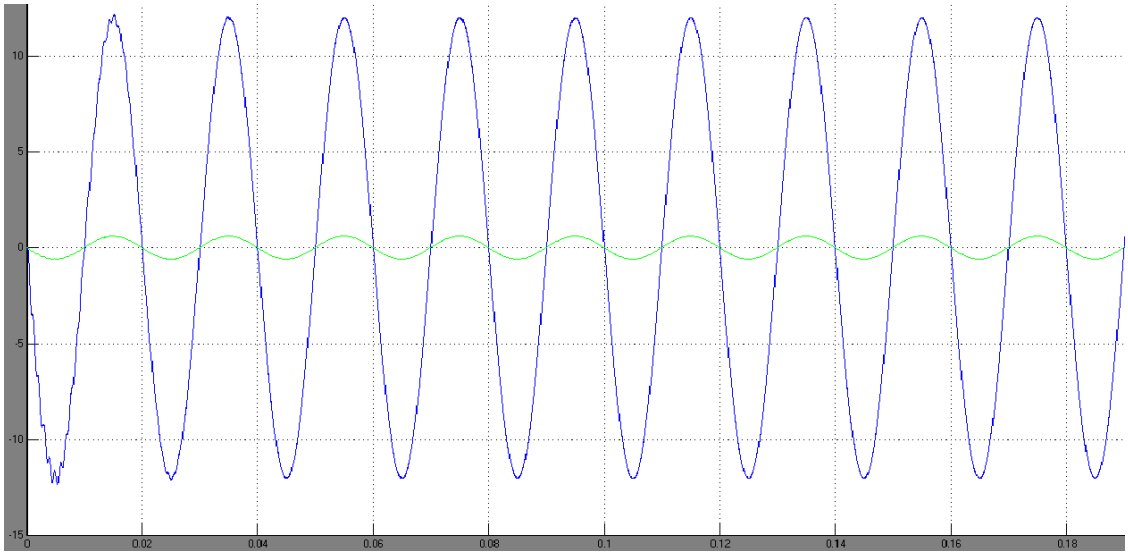

Figure 3.13: PWM Inverter Output Waveform at Pin a-b

Figure 3.14 (a) and Figure 3.14 (b) show the THD at 2mf and 4mf respectively whereby measurement is taken at Pin c-d. Figure 3.14 (c) shows the THD after filtered. For unipolar PWM inverter, the magnitude of frequency spectrum at 2mf (40 kHz) and 4mf (80 kHz) is zero. Hence the results shown in Figure 3.14 (a) and Figure 3.14 (b) are valid.

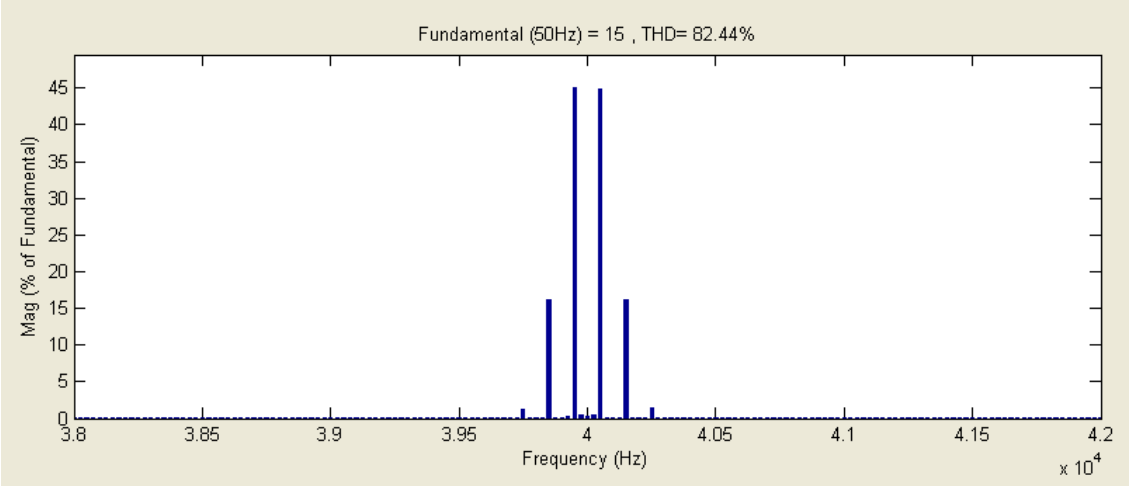

Figure 3.14 (a): Harmonic at 2mf

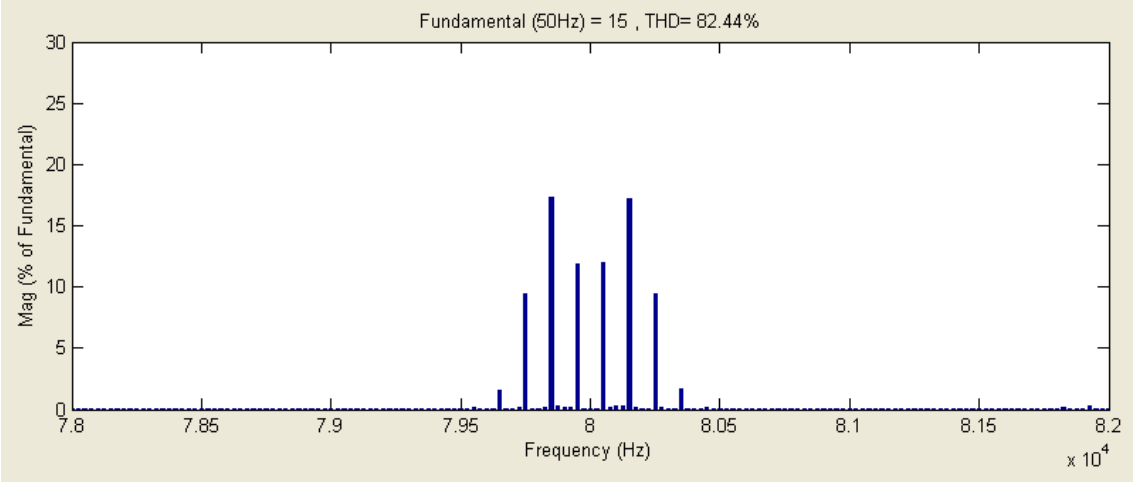

Figure 3.14 (b): Harmonic at 4mf

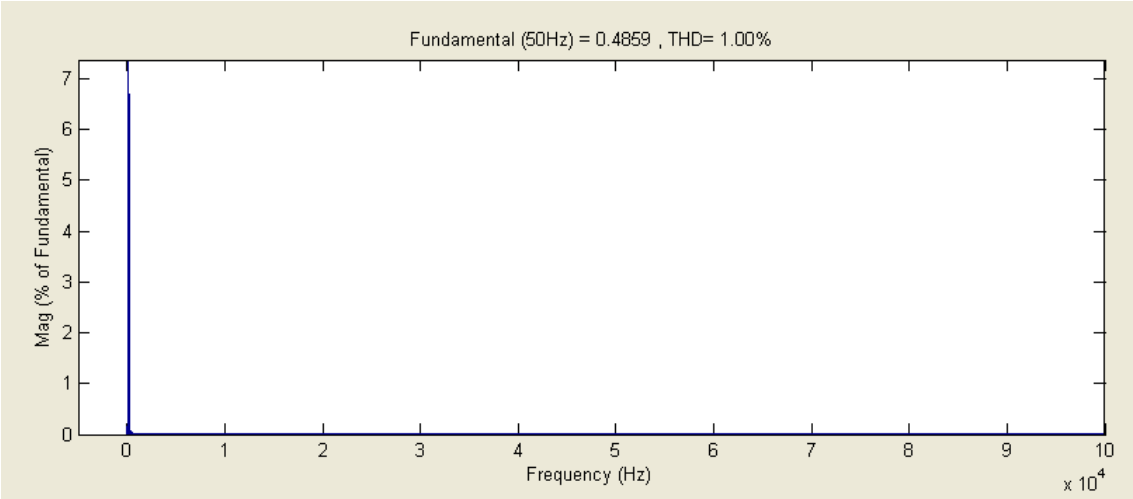

Figure: 3.14 (c): THD after Filtered

Figure 3.14: THD of the PWM Inverter (a) Before Filter at 2 mf (b) Before Filter at 4mf (c) After Filtered

The simulation results shown verified that the performance of PWM inverter is similar to that the theory part, that is the THD of the inverter after filtered is less than 5%, hence a sinusoidal waveform is obtained at the output.

3.2.7 Controller Analysis

In order to verify the performance of the inverter, a disturbance is introduced at the input side. A sinusoidal signal is imposed at the input side to analyze the performance of the controller that is the ability or time taken of the controller to recover from disturbance. Figure 3.15 shows the circuit with a disturbance signal at the input side and Figure 3.16 shows the result of the test. Figure 3.17 shows the change in input signal towards the performance of the controller by introducing a 2 V disturbance to the inverter at time, t = 0.2 second. Figure 3.18 shows the circuit to test the performance of the controller when load is changed at t = 0.2 seconds and Figure 3.19 shows the performance's result of the controller if the load is changed at t = 0.2 second.

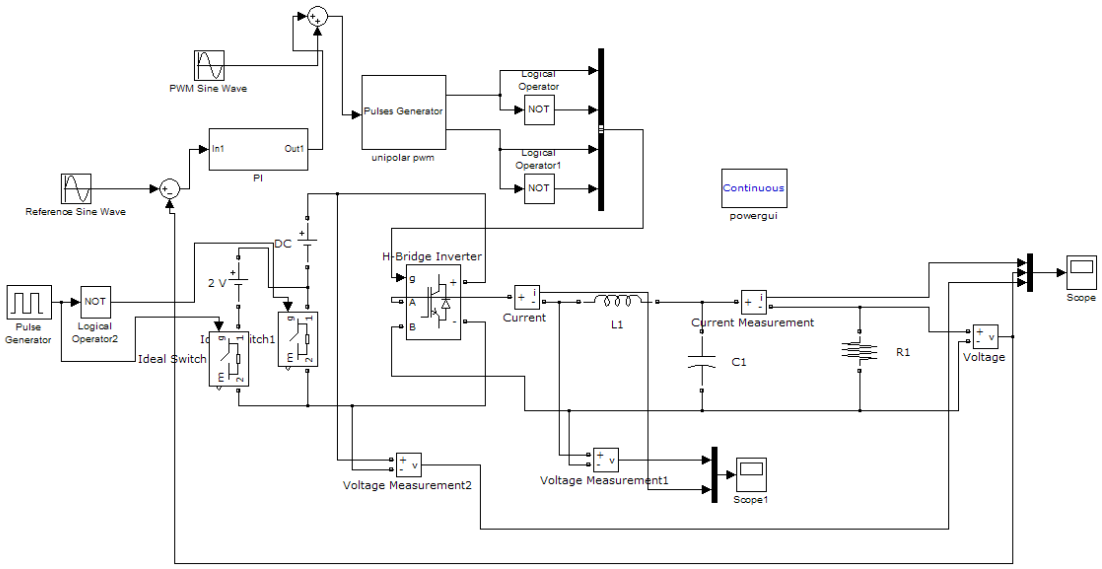

Figure 3.15: Input Disturbance Testing Circuit

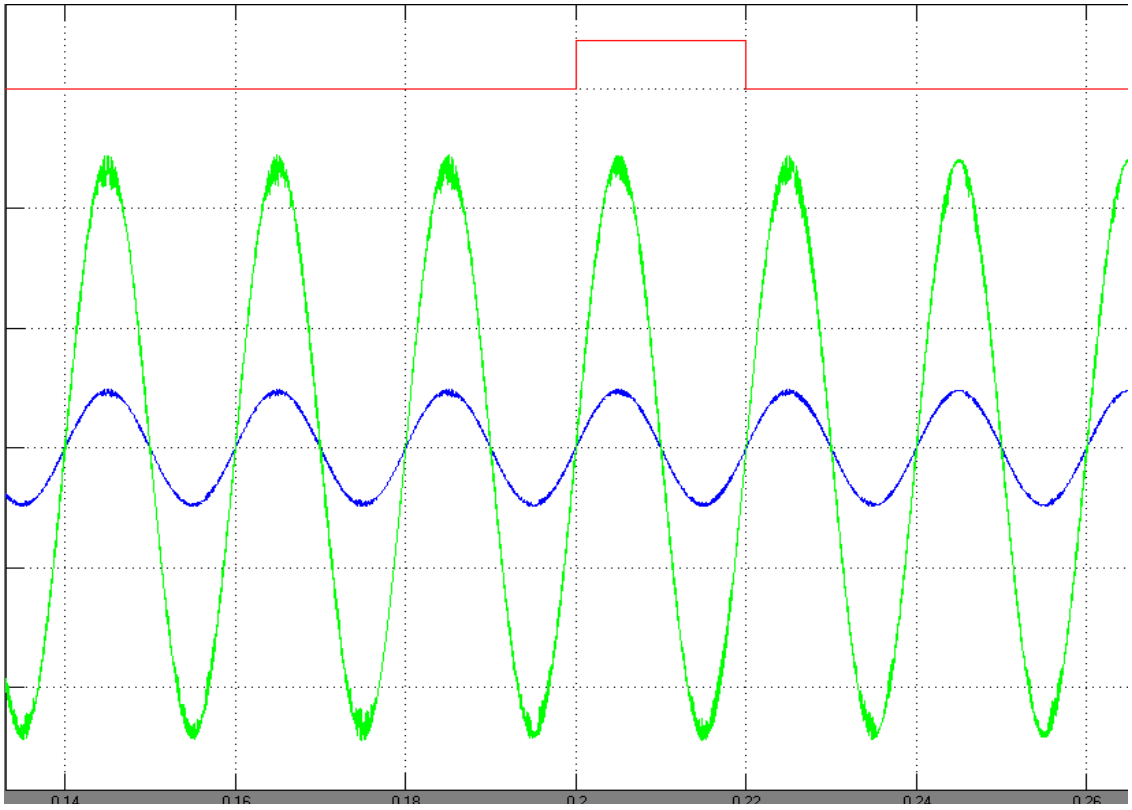

Figure 3.16: Performance of the Controller

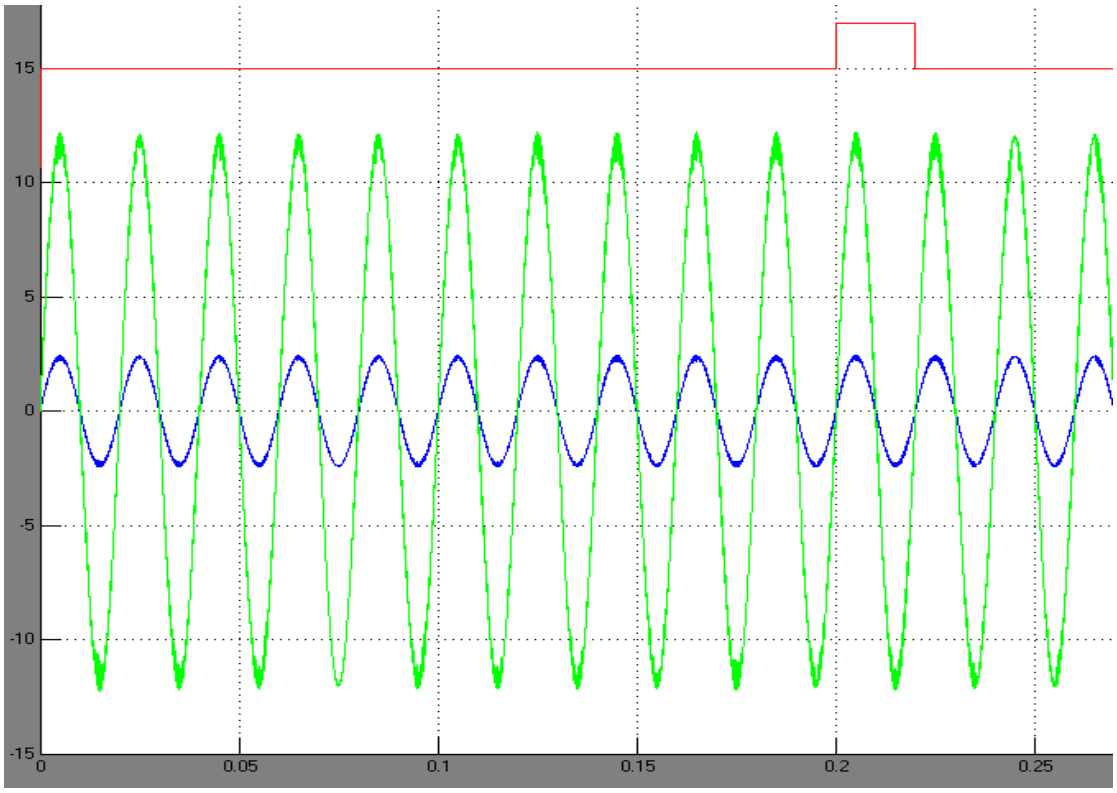

Figure 3.17: Performance of Controller When Reference Signal Changes at t = 0.2s

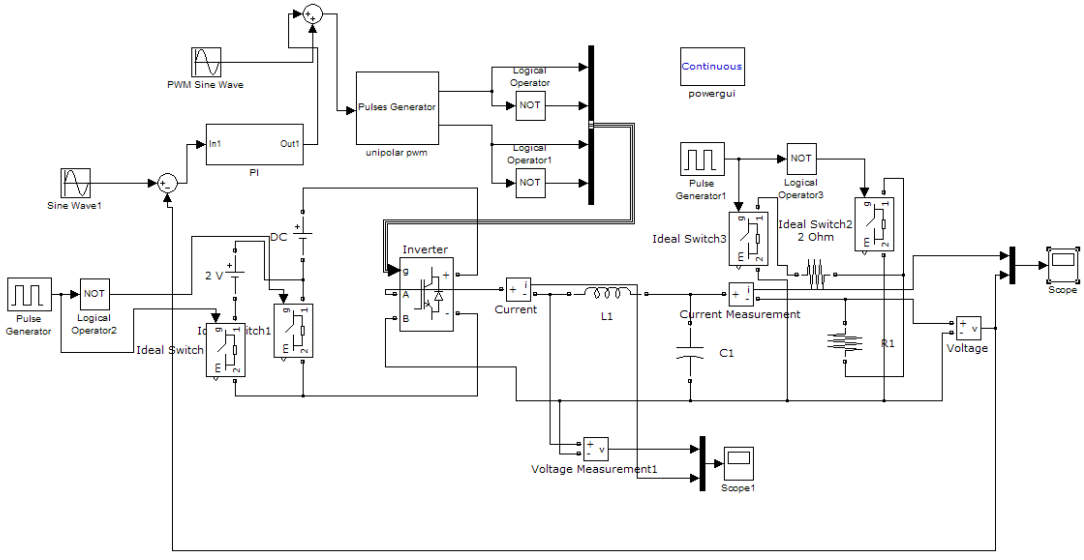

Figure 3.18: Load Change Testing Circuit

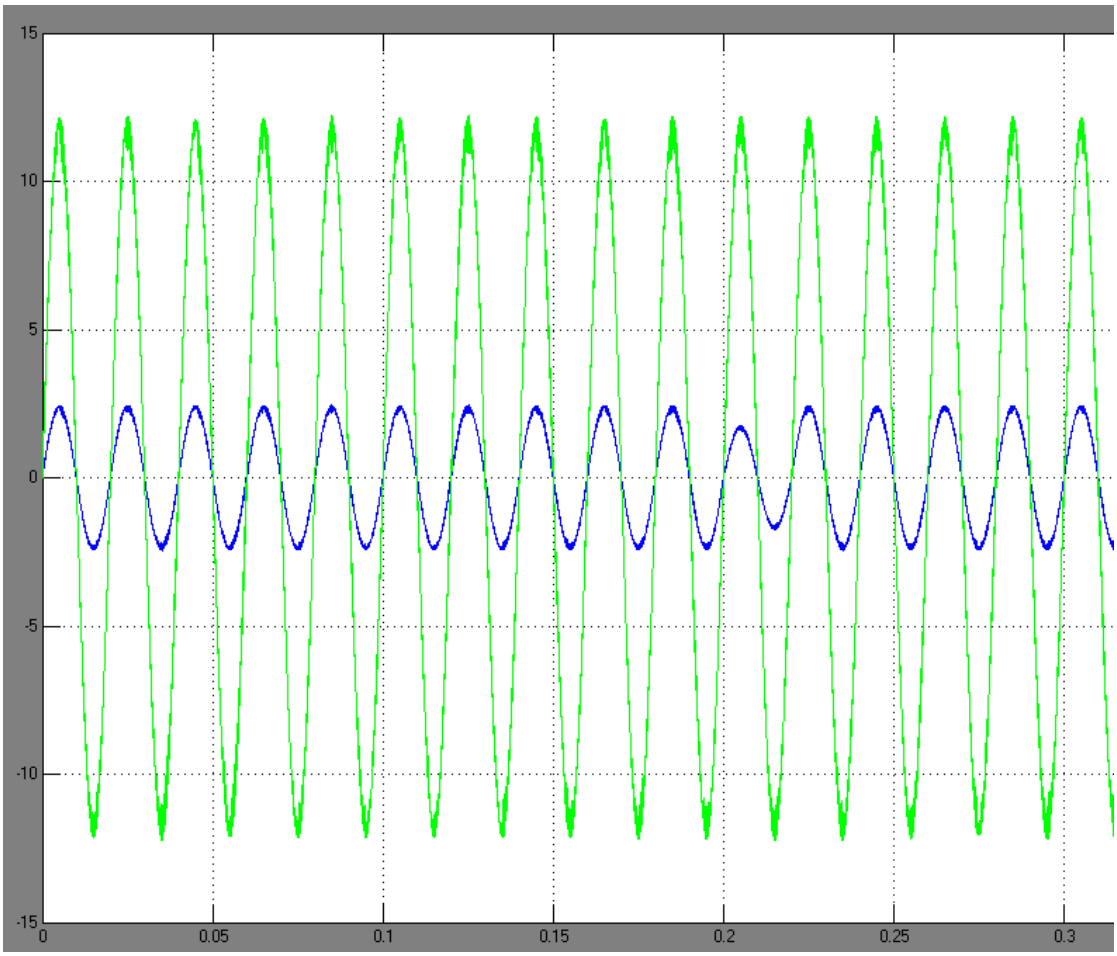

Figure 3.19: Performance of Controller due to a 2 Ω Increased in Load

3.3 Summary

A closed loop voltage controlled PWM inverter is successfully developed. The performance of the PI controller is tested by introducing disturbances into the system. However the PI controller has certain limitations. For the PI controller to work in optimum condition, the input disturbance cannot exceed 2 V and the interrupting time must within 0.5 seconds. The longer the interrupting time, the longer the time is needed for the output voltage signal to become stable.

3.4 Hardware Development

This section provides the details on the hardware development of the PWM inverter. Components selection and design specification is discussed in this section. The design is spread into 2 parts, which are the PWM driver part and inverter part.

3.4.1 PWM and Driver Design

The PWM generator is initially designed base on Figure 4.1. However, the configuration is modified and the actual configuration of the PWM and driver circuit is shown in Figure 4.2. Table 4.1 shows the specification of the PWM and driver design.

Table 3.3 Data Specification of PWM and Driver Design

Parameter / Component		Value
Resistor	R1	100 Ω
	R2	10 kΩ
	R3	3 kΩ
	R4	1.5 kΩ
Rheostat	R5	5 kΩ
Capacitor	C1	10 nF
	C2	10 nF
	C3	100 nF
	C4	100 nF
	C5	100 nF
	C6	100 nF
	C7	100 nF
Frequency	f	12.5 kHz
Supply Voltage	Vcc	15 Vdc
Output Voltage	Vout	12 Vdc
PWM Generator	SG 3525	N/A
Driver	TC 4427	N/A

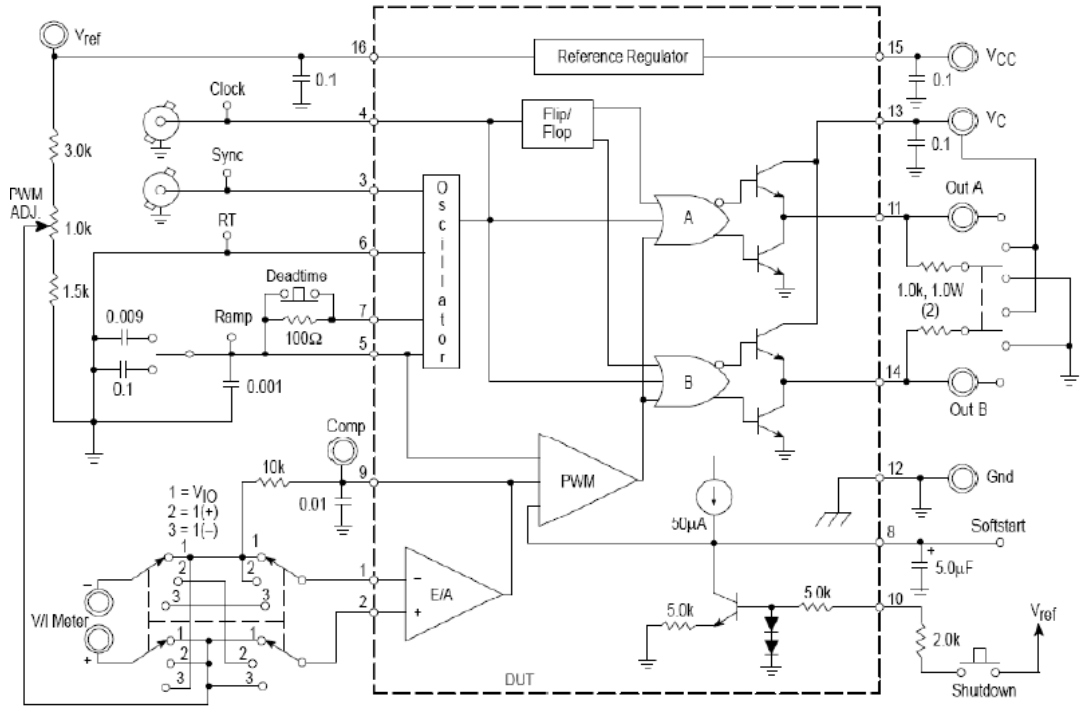

Figure 3.20: Lab Text Fixture of SG 3525

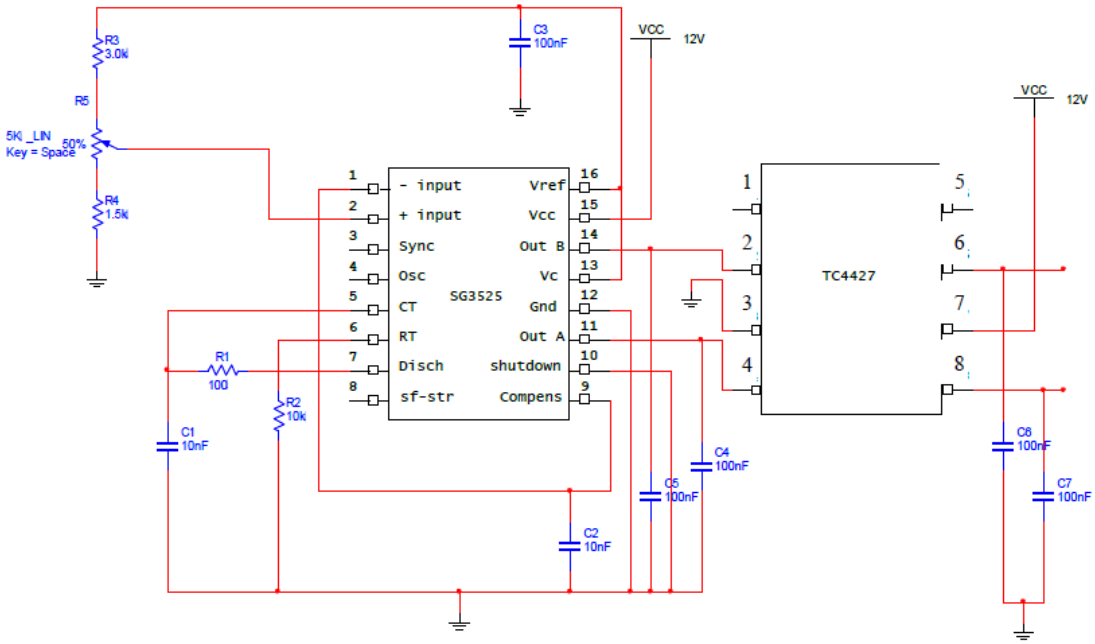

Figure 3.21: PWM and Driver Circuit

Component SG3525 is the PWM generator that generates a square wave signal to turn on and off the MOSFET. I.C. TC 4427 is the driver that amplified the current from the output signal of SG3525 in order to effectively turn on and off the MOSFET. The important components in designing the above circuit are R1, R2 and C1 which can set the dead time and frequency of the driver system. Based on the data sheet of SG 3525, the value of R1, R2 and C1 is determined through the graphs that shown in Figure 3.22 and Figure 3.23 respectively.

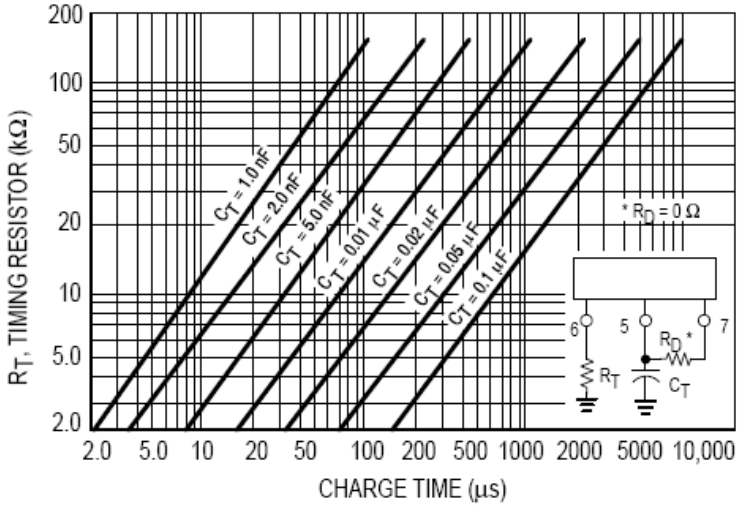

Figure 3.22: Oscillator Charge Time versus RT

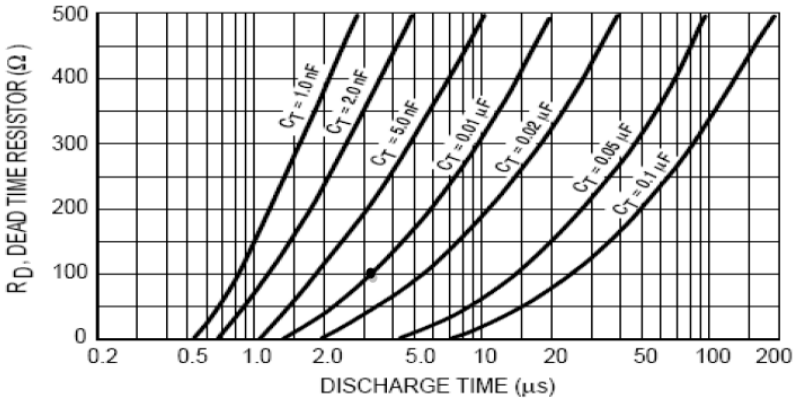

Figure 3.23: Oscillator Discharge Time versus RD

Based on Figure 3.22, the value of resistor R1 is chosen to be 10kΩ and C1 is chosen to be 0.01μF or 10nF. From Figure 3.23, dead time is determined by the intersection point of RD and CT or in this case R2 and C1. The discharge time determine its dead time. For a dead time of 3μsec, the resistor value R2 is chosen to be 100 Ω. The frequency of the PWM generator is determined from Figure 3.22 that is the intersection point of resistor R1 and capacitor C1. In this case the frequency is around 10 kHz. The actual frequency and dead time is shown in chapter 4. The resistor R3 and R4 and rheostat R5 are mainly used to determine the duty cycle of the SG 3525 output signal. To successfully design the desired duty cycle of the output signal, a 5kΩ rheostat (R5) is used and is tuned to the maximum duty cycle of 49%. The duty cycle of SG 3525 can be increased up to 99% by connecting both the output (pin 11 and pin 14) together as shown in Figure 3.24, however a duty cycle of 49% is chosen because the output signal is used to turn on the MOSFET later. For example, if the duty cycle is 70%, the inverter will results in a 70% positive voltage and 30% negative voltage in 1 complete cycle.

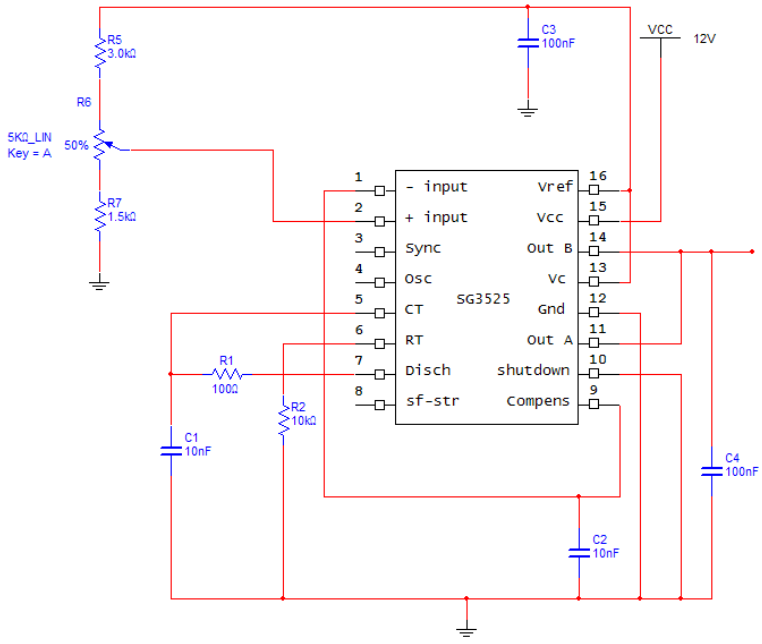

Figure 3.24: Configuration of SG 3525 to Produce Duty Cycle Up to 99%

IC TC 4427 is used to amplify the current IG that is used to turn on the MOSFET later in the inverter. Both output from SG 3525 are directly fed into TC 4427 as shown in Figure 3.21. Since TC 4427 has 2 non-inverting outputs, hence there will be no additional work from inverting the output back. Figure 3.26 shows the I.C. configuration of TC 4427. The design of TC 4427 is initially based on Figure 3.25. The configuration is then modified and the final configuration of both IC (SG 3525 and TC 4427) is as shown in Figure 3.21.

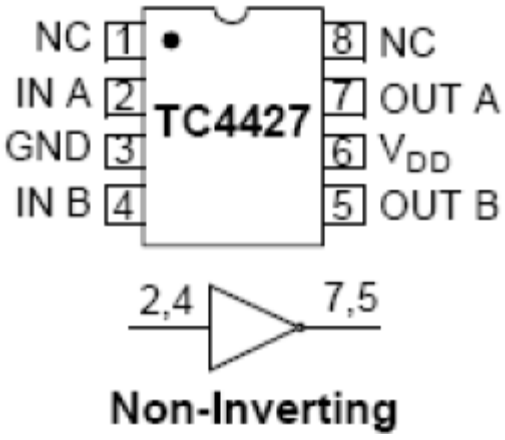

Figure 3.25: I.C. Pin TC 4427

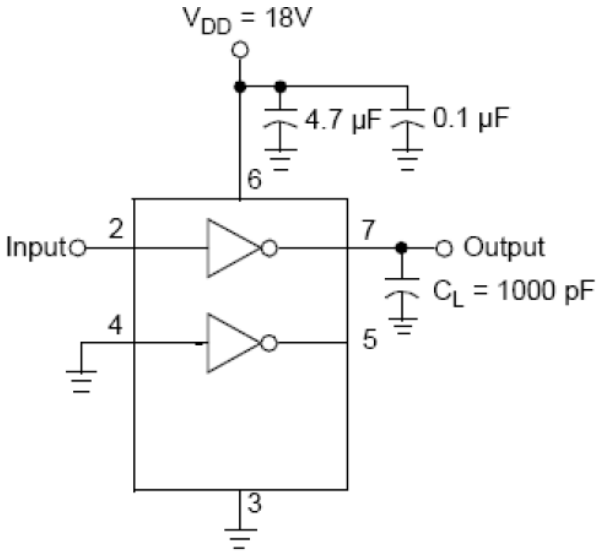

Figure 3.26: Initial Configuration of TC 4427

3.4.2 Inverter Power Circuit Design

Next, for the inverter power circuit configuration, it consists of 4 MOSFET, 4 X 1.5 Ω resistors, an inductor of 47 μH, a capacitor of 470 μF and a R-load of 5 Ω as shown in Figure 4.9 and Table 4.2. The inductor and capacitor serve as the filter which is used to filter out the current and voltage harmonics in order to produce a smooth sinusoidal signal. Meanwhile the resistor 1.5 Ω is used to stabilize the gate current IG. In the design of inverter, IRF 540 is the chosen MOSFET due to its small VGS (on) and low ID (on) as shown in Table 3.5. The voltage and current rating for the MOSFET are shown in Table 3.6.

Table 3.4: Data Specification for Inverter

Parameter		Value
Resistor	R1	1.5 Ω, 5 W
	R2	1.5 Ω, 5 W
	R3	1.5 Ω, 5 W
	R4	1.5 Ω, 5 W
Capacitor	C1	470 μF
Inductor	L1	47 μH
R-Load	R5	5 Ω, 25 W
MOSFET	IRF 540	Refer Table 4.4

Table 3.5: Electrical Characteristic of MOSFET Device IRF 540

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250$ μA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10$ V $I_D = 11$ A		0.055	0.077	Ω

Table 3.6 Ratings of MOSFET Device IRF 540

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRF540	100 V	<0.077 Ω	22 A

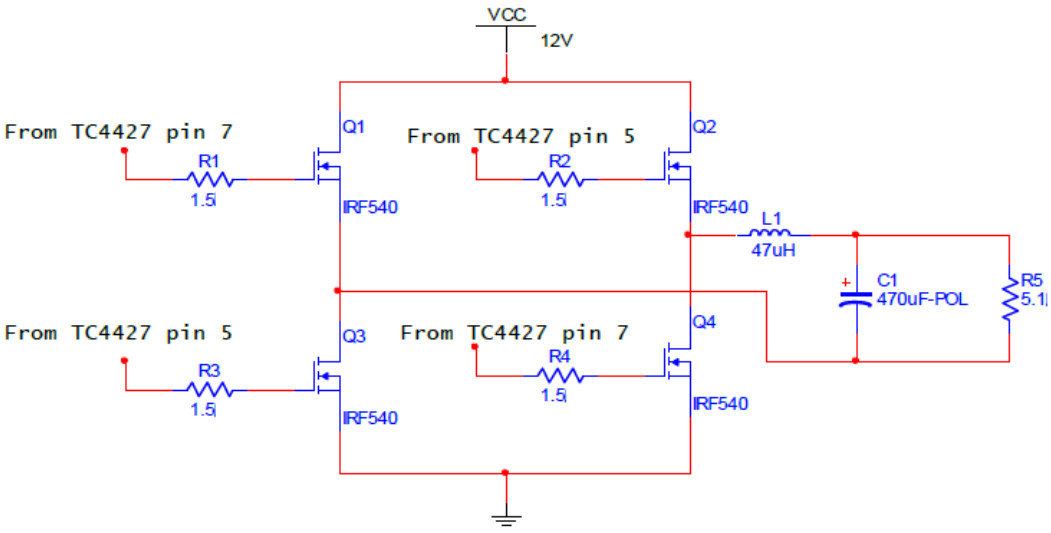

Figure 3.27: Inverter Configuration

CHAPTER 4

RESULT AND ANALYSIS

4.1 Result from SG 3525

The output of SG 3525 is a square wave with magnitude 12 V. However the output magnitude can be varied by altering the supply voltage to the I.C SG 3525. Besides by changing the value of resistor R5, the duty cycle of the output signal will be changed. Figure 4.1 shows the dead time of the system, Figure 4.2 shows the output voltage at different duty cycle, and Figure 4.3 shows the result of output voltage at different supply voltage. (Notes: blue signal refers to the output voltage signal at pin 11 and green signal refers to the output voltage signal at pin 14).

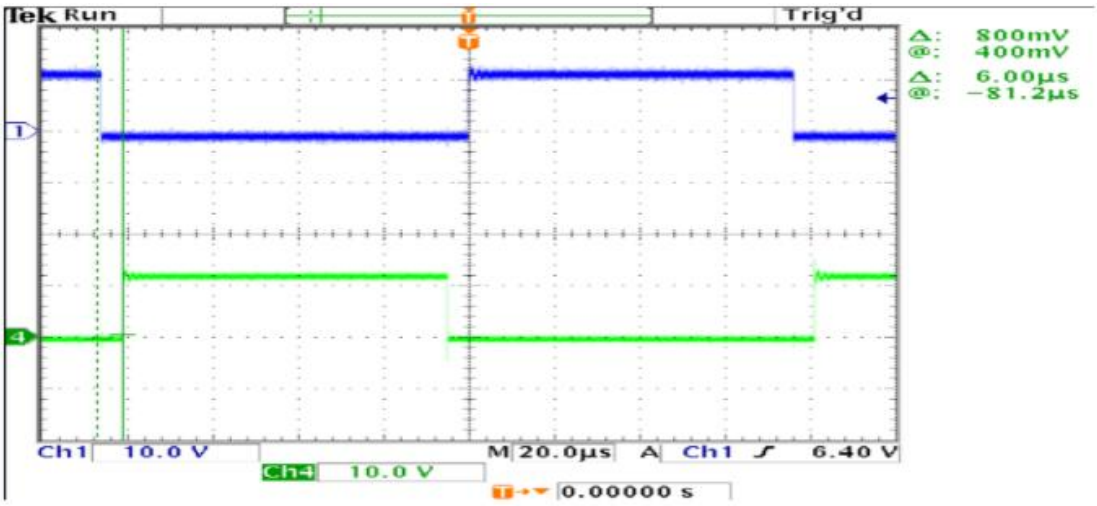

Figure 4.1: Dead Time from SG 3525

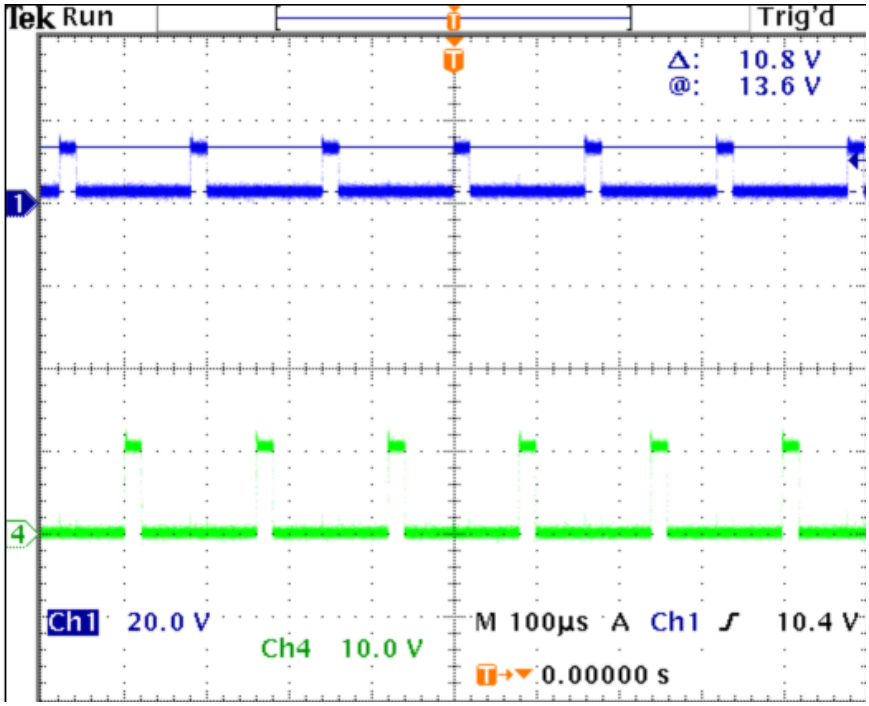

Figure 4.2 (a): Duty Cycle = 10 %

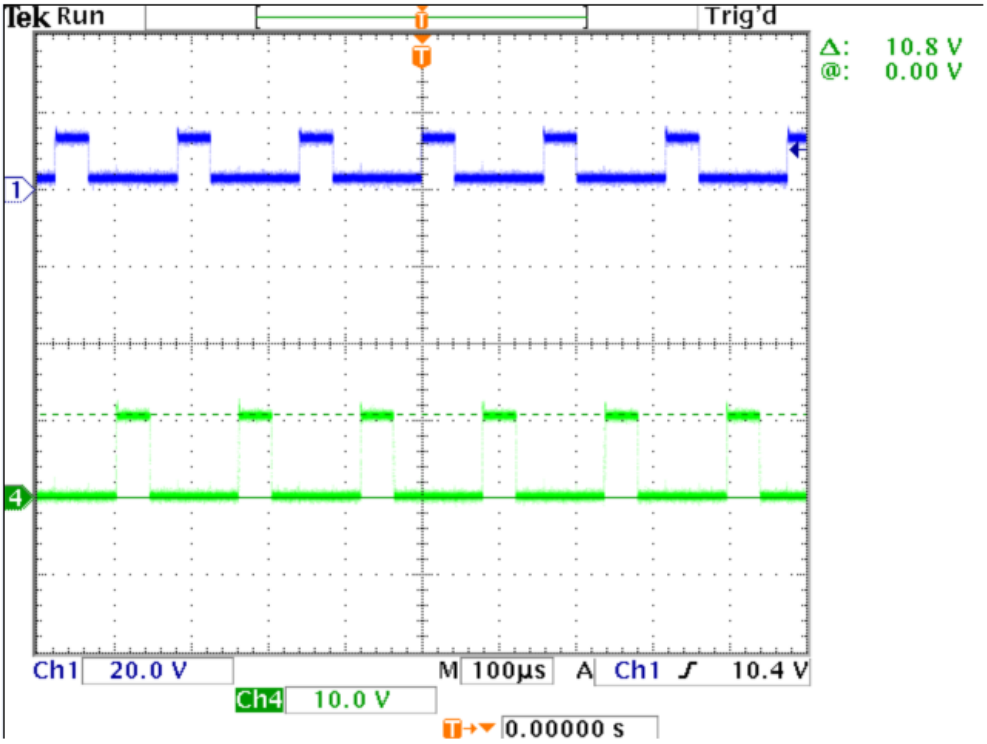

Figure 4.2 (b): Duty Cycle = 20 %

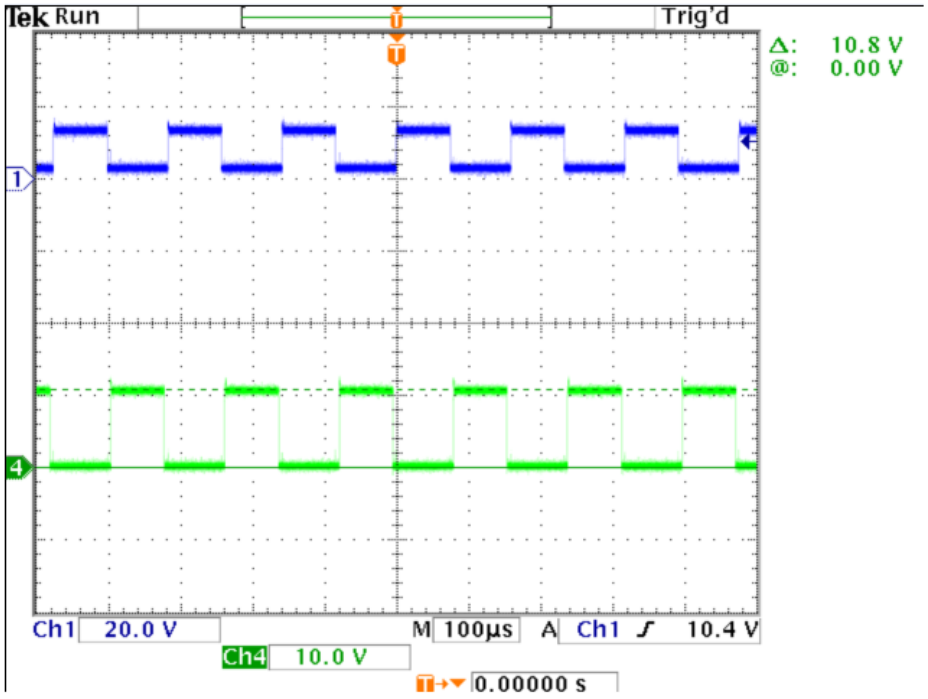

Figure 4.2 (c): Duty Cycle = 48 %

Figure 4.2: Voltage Output Waveform at Different Duty Cycle

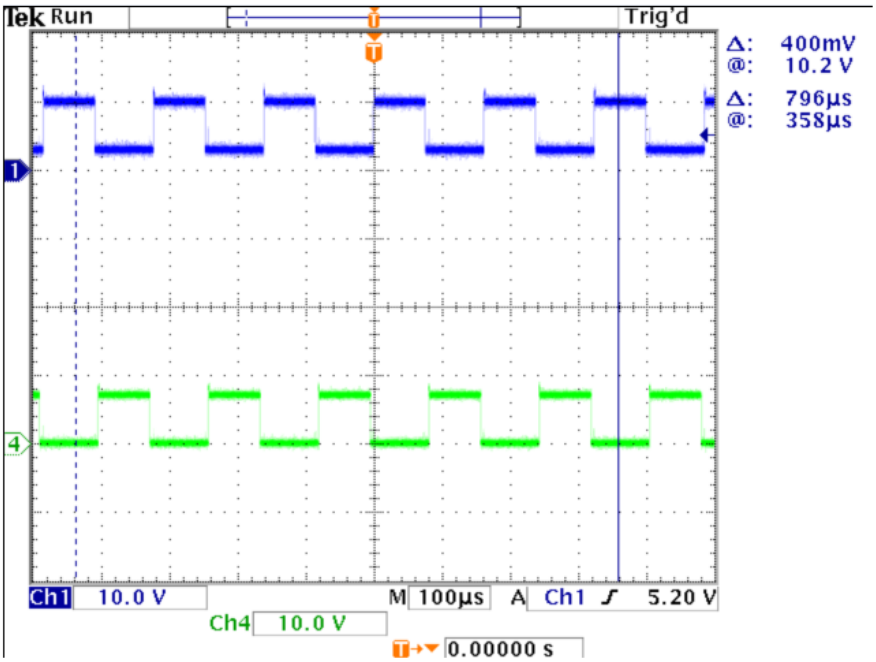

Figure 4.3 (a): Input Voltage = 10 V

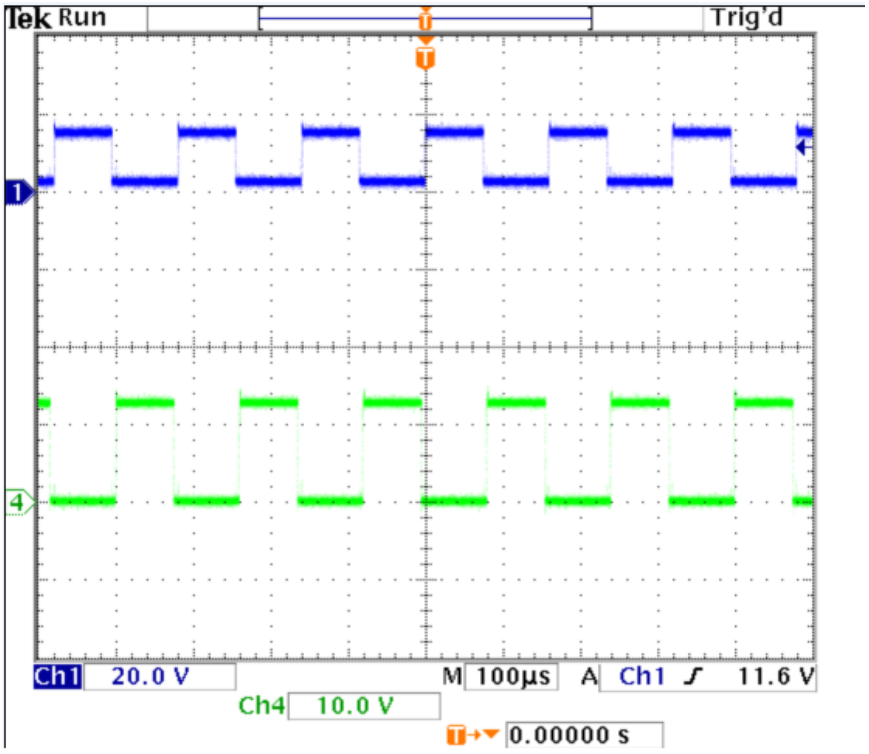

Figure 4.3(b): Input Voltage = 14 V

Figure 4.3: Output Signal at Different Supply Voltage

From plot in Figure 4.1, the actual dead time is 6 μs whereby the design dead time is 3μs. This is due to the components that used in the real circuit is not in ideal value that is all components are with its own tolerance. Besides that, the actual frequency is determined as:

$$= \frac{}{} = 10$$

However the designed frequency is 12.5 kHz. This is due to the tolerance of components in the actual circuit and the frequency obtained from the data sheet of SG 3525 only serves as a reference during the design phase.

In this design, a duty cycle of 48% is used due to reasons stated below:

i. If more than 48 %, 2 SG 3525 will be used and it will make the circuit very complex.
ii. A 48 % duty cycle is good enough to turn the MOSFET on.

4.2 Result from TC 4427

TC 4427 is a driver that is used to amplify the current so that it can turn the MOSFET on and off properly. The output of TC 4427 is shown in Figure 4.4.

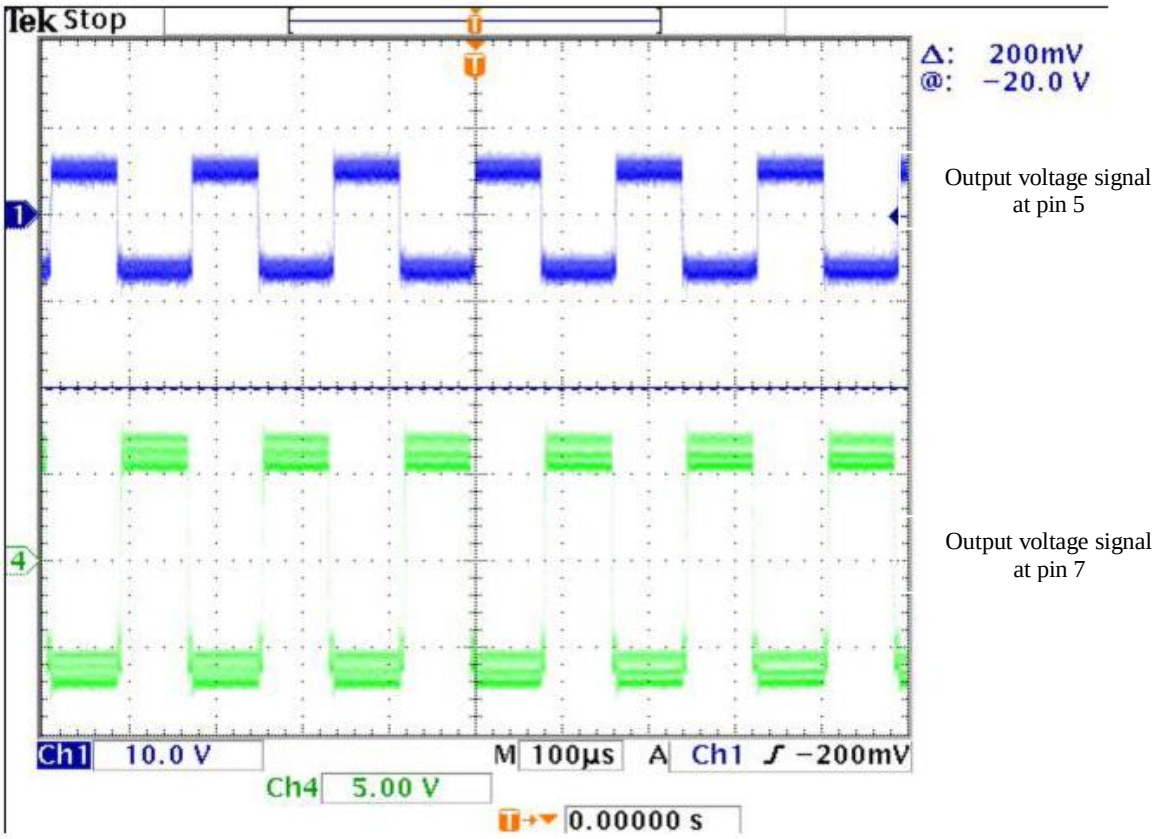

Figure 4.4: Output from TC 4427

Plot in Figure 4.4 clearly shows that there is noise at the output of TC 4427. This noise may be due to probe problem and connection problem such as components are not properly soldered and number of jumpers used in the circuit.

The output voltage of the TC 4427 is also depends on the I.C. supply voltage. In this case a supply of 12 V is used and the output voltage is around 10 V which is sufficient to turn the MOSFET on.

4.3 Result from Inverter

The output signal from TC 4427 is fed into the VGS terminal of 4 MOSFETs inverter as shown in Figure 4.5. Voltage is measured across the load and is shown in Figure 4.7

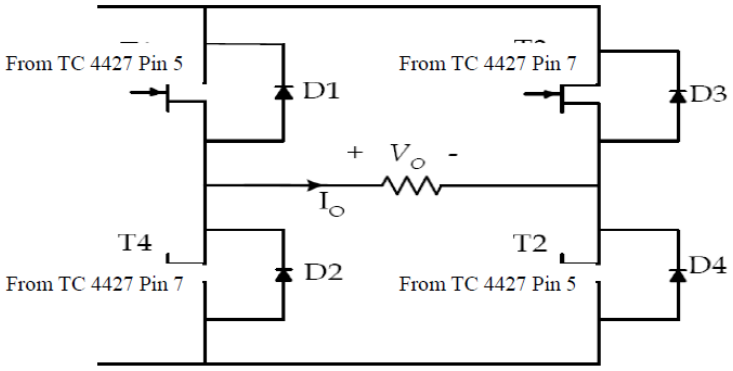

Figure 4.5: A Typical Inverter Configuration

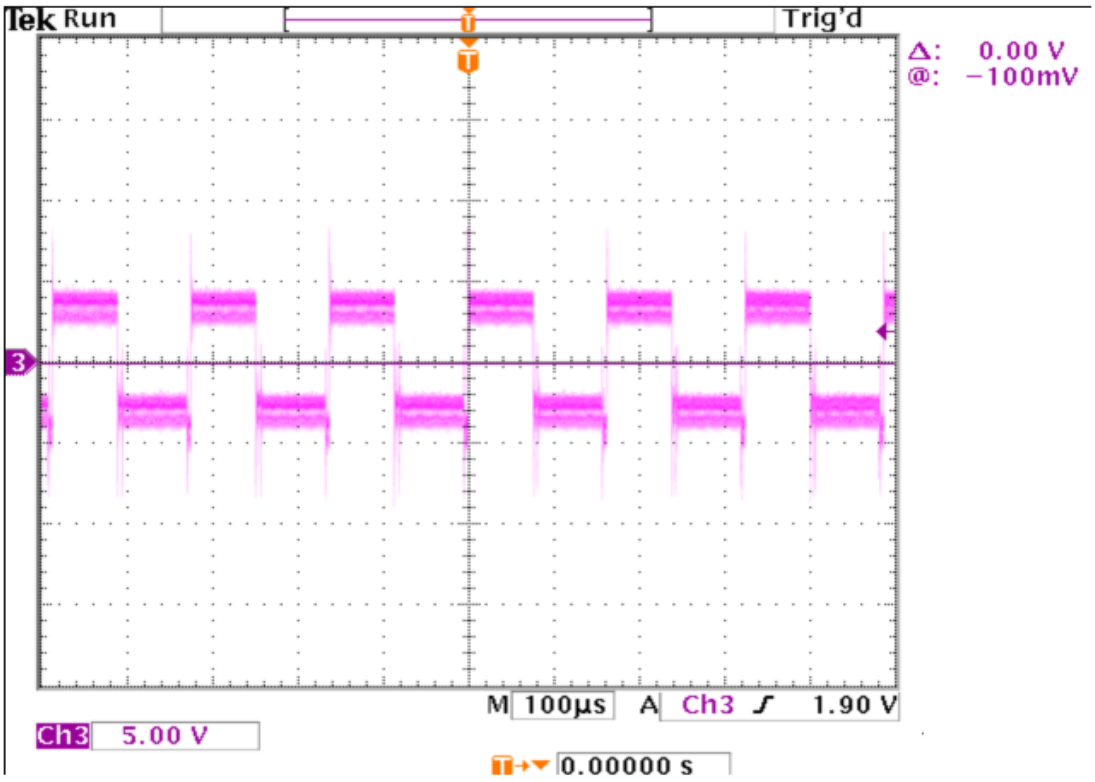

Figure 4.6: Voltage across R-Load

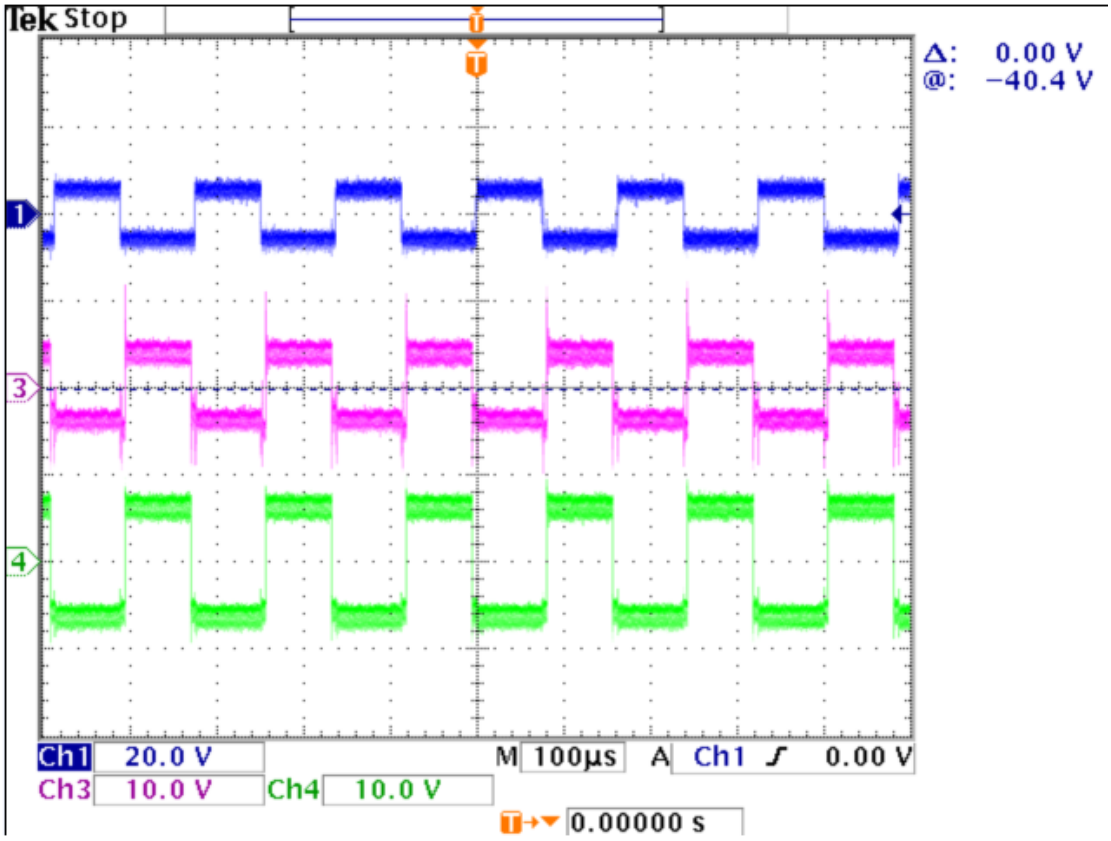

Figure 4.7: Voltage Signal from TC 4427 and Across Load

The output signal across the load is around ±5 V which is relatively low when compared to the desired output of 10 Vac. This is due to the reason that the higher the voltage across the load, the more current is required. In this design, a 5 Ω, 10 W resistor is used as a load. Hence the current required to produce a maximum voltage of 12 V will be calculated as follow:

$$= - = 2.4$$

The current of 2.4 A is very high and will cause damage to the MOSFET because the ID(on) for this MOSFET is around 2.5 A to 3.0 A as shown in Figure 4.8. By referring to Figure 4.8, when the MOSFET is turn on, VDS = 0V and ID = IDSS which

is around 2.5 to 3 Ampere. Therefore, with a 5 Ω load, it is risky to produce a 12 V output base on the specification of MOSFET IRF 540. Besides with such an amount of current, the MOSFET will be very hot and heat sink is required to dissipate the heat and to protect the MOSFET from being damaged. To overcome this problem, a bigger load can be used such as replacing the 5 Ω load with a 10 Ω load because it will caused the current I(on) to become smaller hence the MOSFET will be protected from being damage.

To overcome this problem, a bigger load can be used such as replacing the 5 Ω load with a 10 Ω load because it will caused the current $I_{(on)}$ to become smaller hence the MOSFET will be protected from being damage. Another solution is to use another MOSFET such as IRF 740 with a very high $I_{D(on)}$ of 10 Ampere. The data sheet of IRF 740 is provided in the Appendix section.

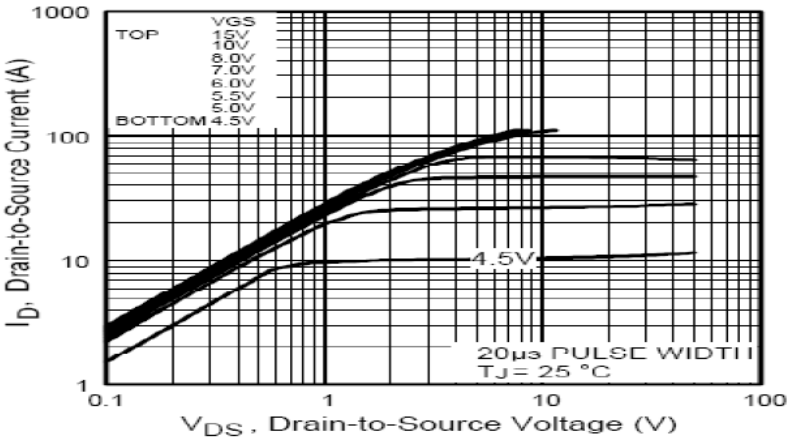

Figure 4.8: Characteristic of MOSFET IRF 540

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

This project is split into 2 major parts that is the software and hardware parts. The PWM inverter is first developed using MATLAB software. During the software development process, the PWM inverter is first designed in open loop condition. The characteristic and performance of an open loop inverter is studied and it was found that the performance for an open loop inverter is not ideal. Hence a close loop inverter has to be designed by feedback the inverter output to the controller. In designing the close loop system, PI controller was selected and reducing the steady state error of the inverter output. The performance of the PI controller was tested by introducing disturbance at the input in order to realize the time taken for the output signal becoming stable. Throughout the process, voltage signal for the PWM inverter was successfully controlled and the PI controller works well. The objective of the project is achieved in the software part.

The next part of the project is the hardware development of the PWM inverter. During the hardware development process, the inverter is developed in open loop

condition and the performance is tested. The PWM inverter consist of a PWM and driver controller circuit with SG 3525 and TC 4427 being the 2 most important integrated circuit(IC) whereby SG 3525 served as the PWM generator and TC 4427 served as the driver. However since the development of filter is not successful, the objective of developing the hardware is not completely achieved. However same results on the open loop system were successfully obtained. The filter needs to be refined in order to yield desired results.

5.2 Recommendation

For further refine purpose, the voltage controlled PWM inverter can be improved in 3 aspects:

i. Select a suitable capacitor that can successfully filtered out the voltage harmonics in order to produce a smooth sinusoidal waveform.

ii. A feedback for the PWM inverter is needed by introducing a PI controller to the inverter at the hardware part.

iii. Design a current controller for the PWM inverter once the voltage controller is successfully developed.

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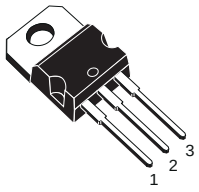
IRF540

N-CHANNEL 100V - 0.055 Ω - 22A TO-220
LOW GATE CHARGE STripFET™ II POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRF540	100 V	<0.077 Ω	22 A

- TYPICAL $R_{DS}(on)$ = 0.055Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- LOW GATE CHARGE
- APPLICATION ORIENTED CHARACTERIZATION



TO-220

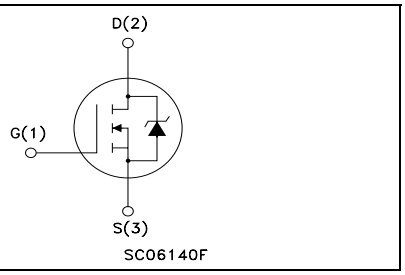
DESCRIPTION

This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements.

APPLICATIONS

- HIGH-EFFICIENCY DC-DC CONVERTERS
- UPS AND MOTOR CONTROL

INTERNAL SCHEMATIC DIAGRAM



Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
IRF540	IRF540&	TO-220	TUBE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	100	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	100	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain Current (continuous) at T_C = 25°C	22	A
I_D	Drain Current (continuous) at T_C = 100°C	15	A
I_{DM}(•)	Drain Current (pulsed)	88	A
P_{tot}	Total Dissipation at T_C = 25°C	85	W
	Derating Factor	0.57	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	9	V/ns
E_{AS} (2)	Single Pulse Avalanche Energy	220	mJ
T_{stg}	Storage Temperature	-55 to 175	°C
T_j	Max. Operating Junction Temperature		

(•) Pulse width limited by safe operating area.

1) I_{SD} ≤22A, di/dt ≤300A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$
(2) Starting T_j = 25 °C, I_D = 12A, V_{DD} = 30V

NEW DATASHEET ACCORDING TO PCN DSG/CT/1C16 MARKING: IRF540 &

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	1.76	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	Typ	300	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	100			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 11 A		0.055	0.077	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS} =25 V I_D = 11 A		20		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		870 125 52		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 50 V I_D = 12 A R_G = 4.7 Ω V_{GS} = 10 V (Resistive Load, Figure 3)		60 45		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}= 80 V I_D= 22 A V_{GS}= 10V		30 6 10	41	nC nC nC

SWITCHING OFF

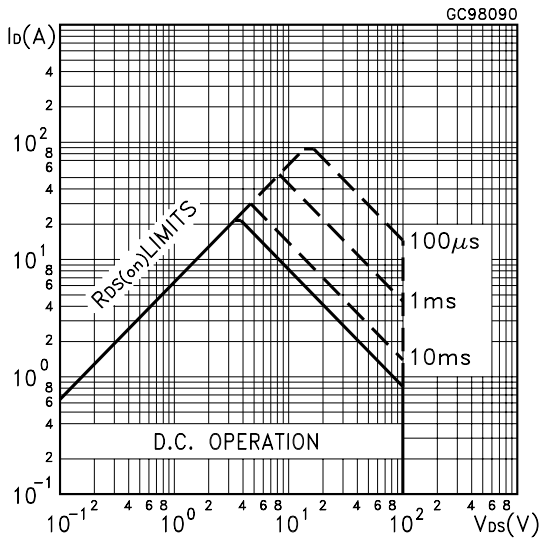
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD} = 50 V I_D = 12 A R_G = 4.7Ω, V_{GS} = 10 V (Resistive Load, Figure 3)		50 20		ns ns

SOURCE DRAIN DIODE

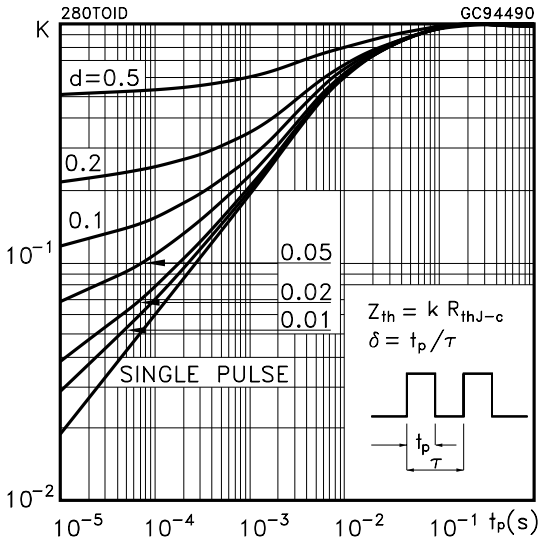
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				22 88	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 22 A V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 22 A di/dt = 100A/µs V_{DD} = 30 V T_j = 150°C (see test circuit, Figure 5)		100 375 7.5		ns nC A

(*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(•)Pulse width limited by safe operating area.

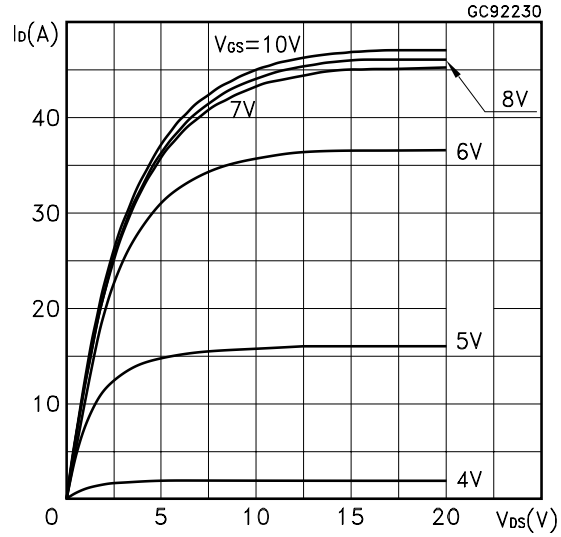
Safe Operating Area



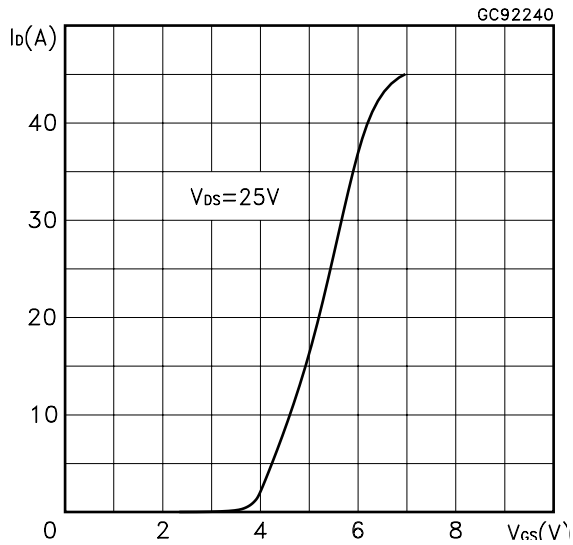
Thermal Impedance



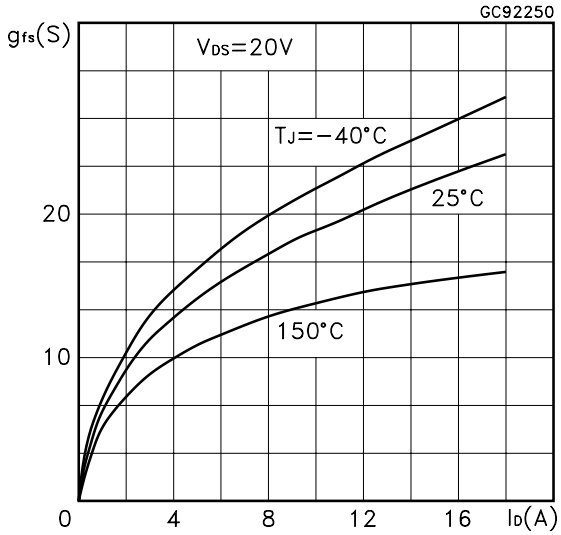
Output Characteristics



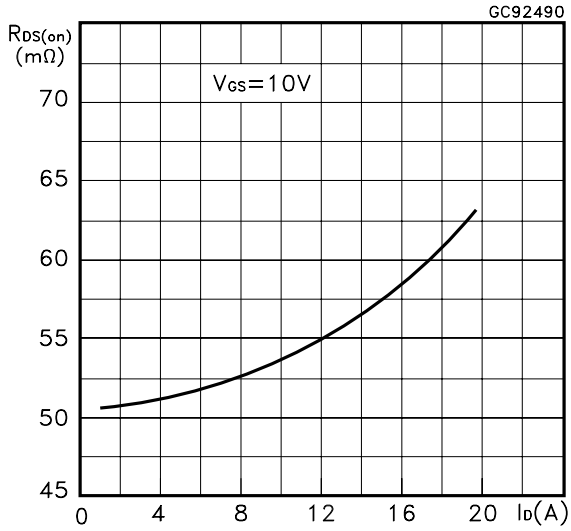
Transfer Characteristics



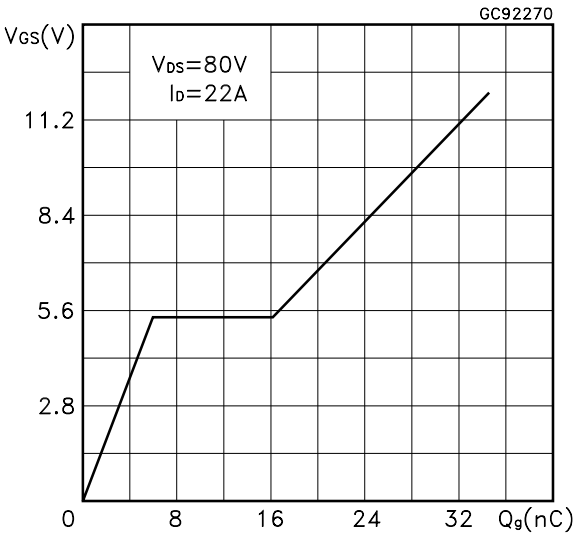
Transconductance



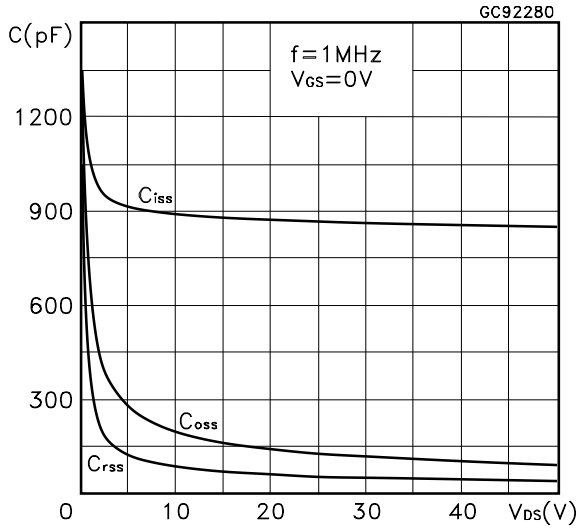
Static Drain-source On Resistance



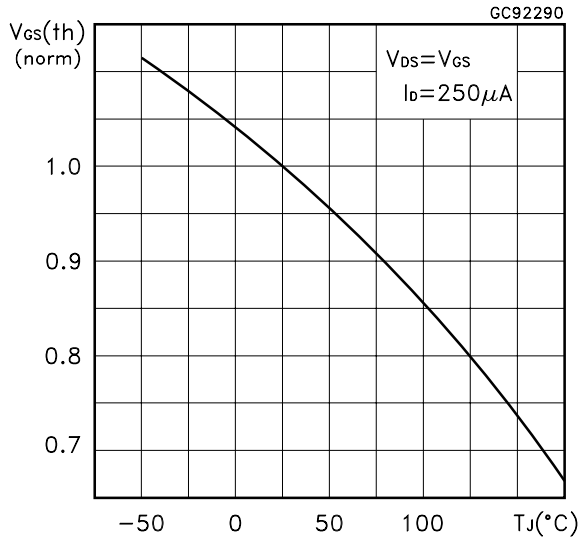
Gate Charge vs Gate-source Voltage



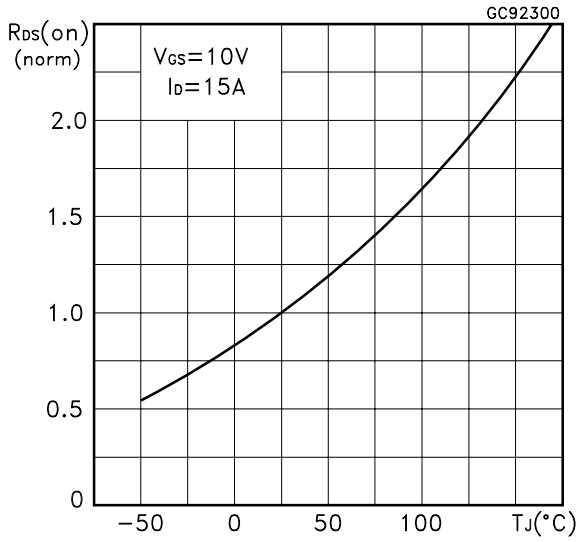
Capacitance Variations



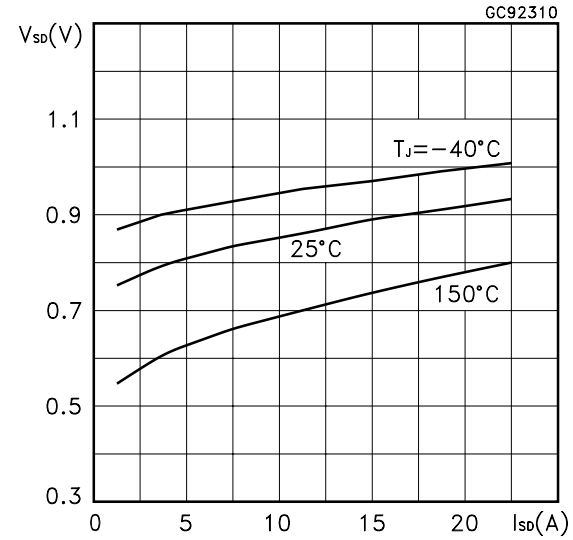
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



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Normalized Breakdown Voltage vs Temperature

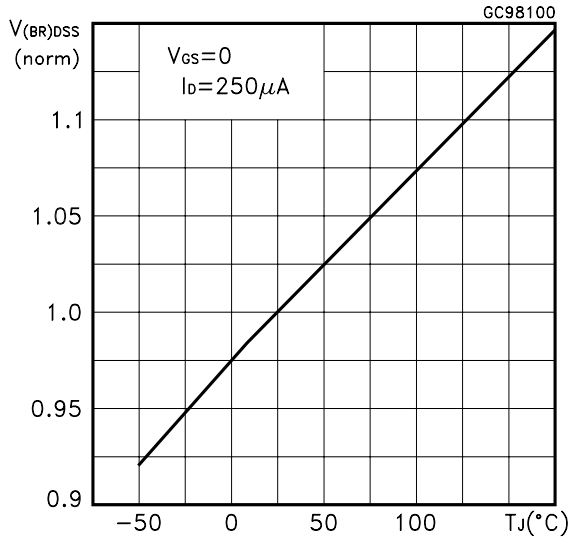

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Fig. 1: Unclamped Inductive Load Test Circuit

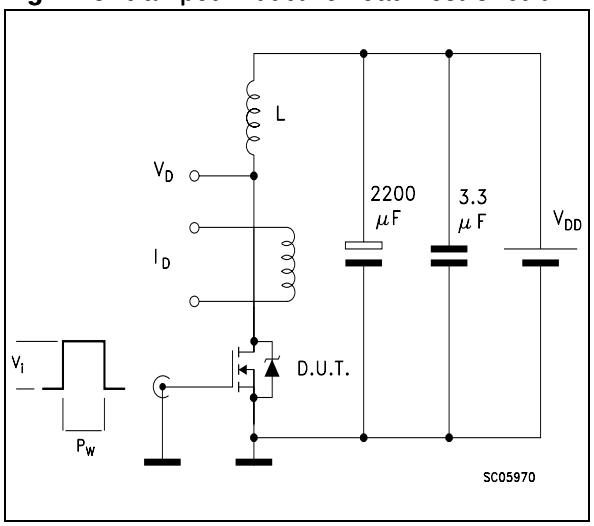


Fig. 2: Unclamped Inductive Waveform

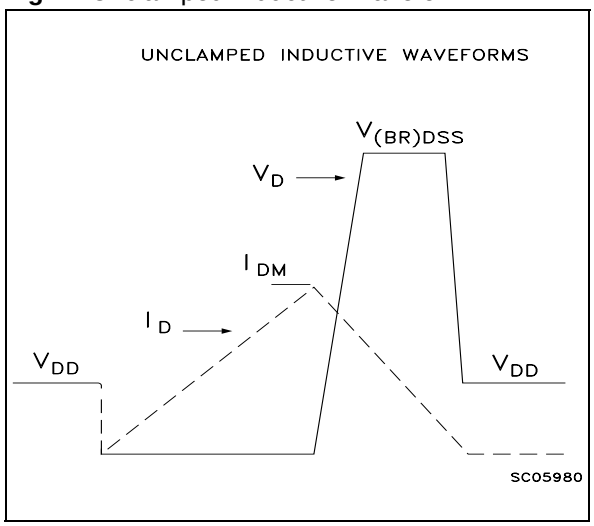


Fig. 3: Switching Times Test Circuits For Resistive Load

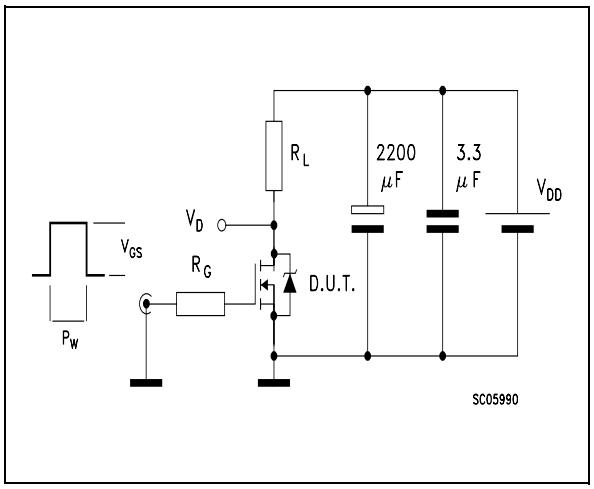


Fig. 4: Gate Charge test Circuit

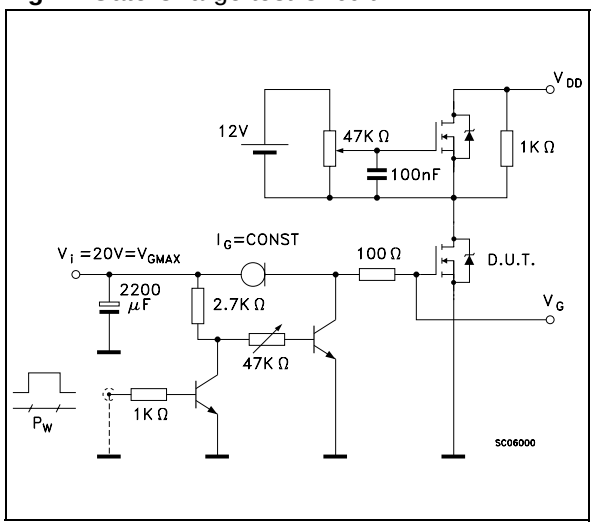
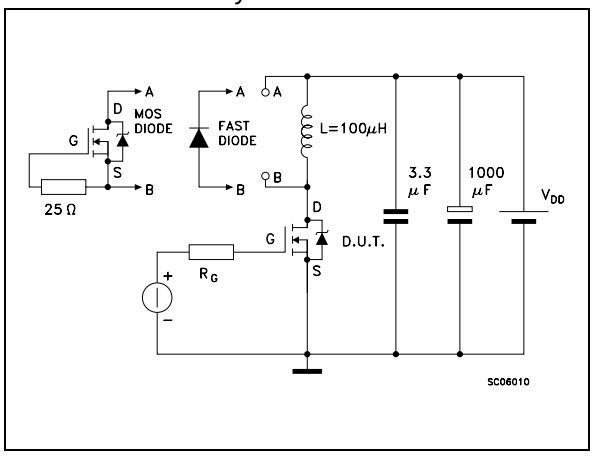
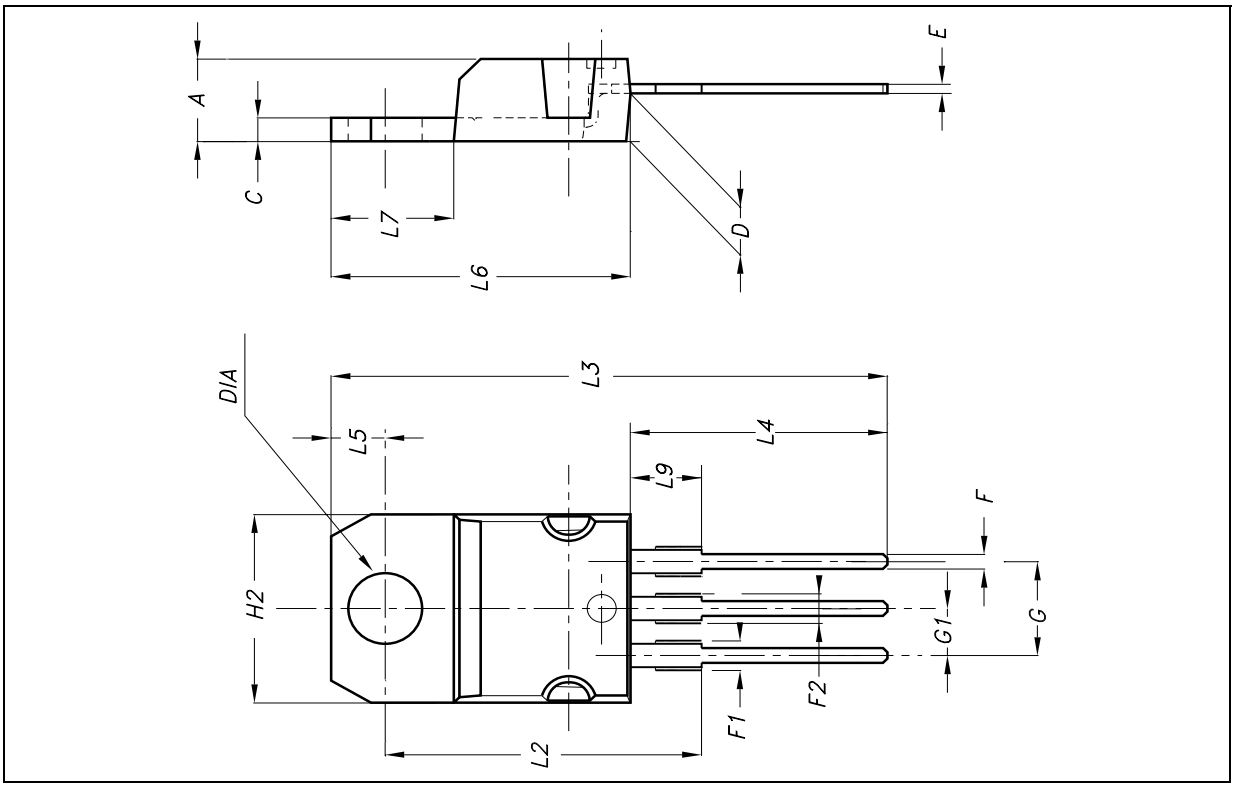


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-220 MECHANICAL DATA

DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.40		2.70	0.094		0.106
H2	10		10.40	0.393		0.409
L2		16.40			0.645	
L3		28.90			1.137	
L4	13		14	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.20		6.60	0.244		0.260
L9	3.50		3.93	0.137		0.154
DIA	3.75		3.85	0.147		0.151



MOTOROLA

SG3525A
SG3527A

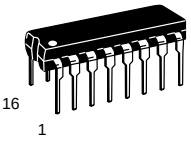
Pulse Width Modulator Control Circuits

PULSE WIDTH MODULATOR CONTROL CIRCUITS

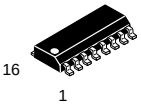
SEMICONDUCTOR TECHNICAL DATA

The SG3525A, SG3527A pulse width modulator control circuits offer improved performance and lower external parts count when implemented for controlling all types of switching power supplies. The on–chip +5.1 V reference is trimmed to ±1% and the error amplifier has an input common–mode voltage range that includes the reference voltage, thus eliminating the need for external divider resistors. A sync input to the oscillator enables multiple units to be slaved or a single unit to be synchronized to an external system clock. A wide range of deadtime can be programmed by a single resistor connected between the C_T and Discharge pins. These devices also feature built–in soft–start circuitry, requiring only an external timing capacitor. A shutdown pin controls both the soft–start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft–start recycle with longer shutdown commands. The under voltage lockout inhibits the outputs and the changing of the soft–start capacitor when V_{CC} is below nominal. The output stages are totem–pole design capable of sinking and sourcing in excess of 200 mA. The output stage of the SG3525A features NOR logic resulting in a low output for an off–state while the SG3527A utilized OR logic which gives a high output when off.

- 8.0 V to 35 V Operation
- 5.1 V ± 1.0% Trimmed Reference
- 100 Hz to 400 kHz Oscillator Range
- Separate Oscillator Sync Pin
- Adjustable Deadtime Control
- Input Undervoltage Lockout
- Latching PWM to Prevent Multiple Pulses
- Pulse–by–Pulse Shutdown
- Dual Source/Sink Outputs: ±400 mA Peak

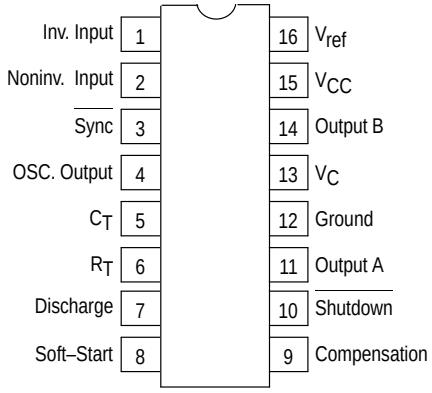


N SUFFIX
PLASTIC PACKAGE
CASE 648



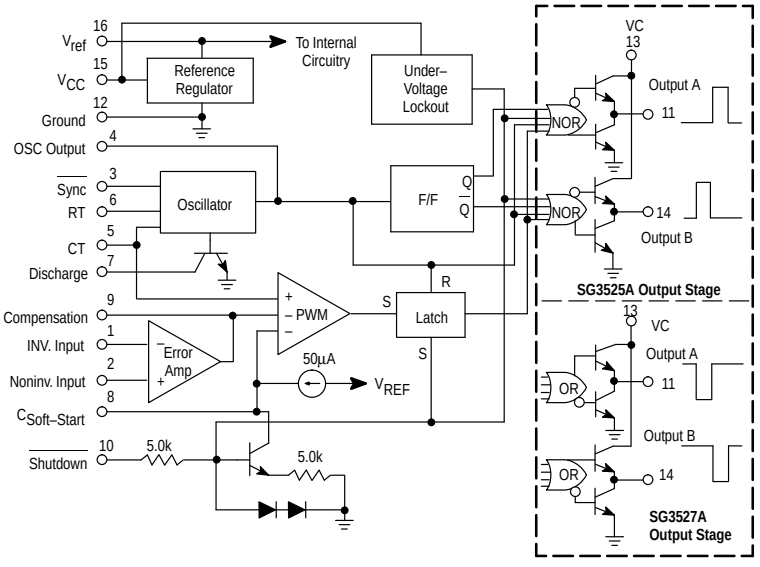
DW SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO–16L)

PIN CONNECTIONS



(Top View)

Representative Block Diagram



ORDERING INFORMATION

Device	Operating Temperature Range	Package
SG3525AN	T_A = 0° to +70°C	Plastic DIP
SG3525ADW		SO–16L
SG3527AN		Plastic DIP

MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	+40	Vdc
Collector Supply Voltage	V_C	+40	Vdc
Logic Inputs		–0.3 to +5.5	V
Analog Inputs		–0.3 to V_{CC}	V
Output Current, Source or Sink	I_O	±500	mA
Reference Output Current	I_{ref}	50	mA
Oscillator Charging Current		5.0	mA
Power Dissipation (Plastic & Ceramic Package) T_A = +25°C (Note 2) T_C = +25°C (Note 3)	P_D	 1000 2000	mW
Thermal Resistance Junction–to–Air	$R_{\theta JA}$	100	°C/W
Thermal Resistance Junction–to–Case	$R_{\theta JC}$	60	°C/W
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Lead Temperature (Soldering, 10 seconds)	T_{Solder}	+300	°C

NOTES: 1. Values beyond which damage may occur.
2. Derate at 10 mW/°C for ambient temperatures above +50°C.
3. Derate at 16 mW/°C for case temperatures above +25°C.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	8.0	35	Vdc
Collector Supply Voltage	V_C	4.5	35	Vdc
Output Sink/Source Current (Steady State) (Peak)	I_O	 0 0	 ±100 ±400	mA
Reference Load Current	I_{ref}	0	20	mA
Oscillator Frequency Range	f_{osc}	0.1	400	kHz
Oscillator Timing Resistor	R_T	2.0	150	kΩ
Oscillator Timing Capacitor	C_T	0.001	0.2	μF
Deadtime Resistor Range	R_D	0	500	Ω
Operating Ambient Temperature Range	T_A	0	+70	°C

APPLICATION INFORMATION

Shutdown Options (See Block diagram, front page)

Since both the compensation and soft–start terminals (Pins 9 and 8) have current source pull–ups, either can readily accept a pull–down signal which only has to sink a maximum of 100 μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn–off signal to the outputs; and a 150 μA current sink begins to discharge the external soft–start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft–start capacitor, thus, allowing, for example, a convenient implementation of pulse–by–pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn–on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

ELECTRICAL CHARACTERISTICS (V_{CC} = +20 Vdc, $T_A = T_{low}$ to T_{high} [Note 4], unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (T_J = +25°C)	V_{ref}	5.00	5.10	5.20	Vdc
Line Regulation (+8.0 V ≤ V_{CC} ≤ +35 V)	Reg_{line}	–	10	20	mV
Load Regulation (0 mA ≤ I_L ≤ 20 mA)	Reg_{load}	–	20	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T$	–	20	–	mV
Total Output Variation Includes Line and Load Regulation over Temperature	ΔV_{ref}	4.95	–	5.25	Vdc
Short Circuit Current (V_{ref} = 0 V, T_J = +25°C)	I_{SC}	–	80	100	mA
Output Noise Voltage (10 Hz ≤ f ≤ 10 kHz, T_J = +25°C)	V_n	–	40	200	μV_{rms}
Long Term Stability (T_J = +125°C) (Note 5)	S	–	20	50	mV/khr
OSCILLATOR SECTION (Note 6, unless otherwise noted.)					
Initial Accuracy (T_J = +25°C)		–	±2.0	±6.0	%
Frequency Stability with Voltage (+8.0 V ≤ V_{CC} ≤ +35 V)	$\frac{\Delta f_{osc}}{D\ V_{CC}}$	–	±1.0	±2.0	%
Frequency Stability with Temperature	$\frac{\Delta f_{osc}}{D\ T}$	–	±0.3	–	%
Minimum Frequency (R_T = 150 kΩ, C_T = 0.2 μF)	f_{min}	–	50	–	Hz
Maximum Frequency (R_T = 2.0 kΩ, C_T = 1.0 nF)	f_{max}	400	–	–	kHz
Current Mirror (I_{RT} = 2.0 mA)		1.7	2.0	2.2	mA
Clock Amplitude		3.0	3.5	–	V
Clock Width (T_J = +25°C)		0.3	0.5	1.0	μs
Sync Threshold		1.2	2.0	2.8	V
Sync Input Current (Sync Voltage = +3.5 V)		–	1.0	2.5	mA
ERROR AMPLIFIER SECTION (V_{CM} = +5.1 V)					
Input Offset Voltage	V_{IO}	–	2.0	10	mV
Input Bias Current	I_{IB}	–	1.0	10	μA
Input Offset Current	I_{IO}	–	–	1.0	μA
DC Open Loop Gain (R_L ≥ 10 MΩ)	A_{VOL}	60	75	–	dB
Low Level Output Voltage	V_{OL}	–	0.2	0.5	V
High Level Output Voltage	V_{OH}	3.8	5.6	–	V
Common Mode Rejection Ratio (+1.5 V ≤ V_{CM} ≤ +5.2 V)	CMRR	60	75	–	dB
Power Supply Rejection Ratio (+8.0 V ≤ V_{CC} ≤ +35 V)	PSRR	50	60	–	dB
PWM COMPARATOR SECTION					
Minimum Duty Cycle	DC_{min}	–	–	0	%
Maximum Duty Cycle	DC_{max}	45	49	–	%
Input Threshold, Zero Duty Cycle (Note 6)	V_{th}	0.6	0.9	–	V
Input Threshold, Maximum Duty Cycle (Note 6)	V_{th}	–	3.3	3.6	V
Input Bias Current	I_{IB}	–	0.05	1.0	μA

NOTES: 4. T_{low} = 0° for SG3525A, 3527A T_{high} = +70°C for SG3525A, 3527A
5. Since long term stability cannot be measured on each device before shipment, this specification is an engineering estimate of average stability from lot to lot.
6. Tested at f_{osc} = 40 kHz (R_T = 3.6 kΩ, C_T = 0.01 μF, R_D = 0Ω).

ELECTRICAL CHARACTERISTICS (Continued)

Characteristics	Symbol	Min	Typ	Max	Unit
SOFT–START SECTION					
Soft–Start Current ($V_{shutdown}$ = 0 V)		25	50	80	μA
Soft–Start Voltage ($V_{shutdown}$ = 2.0 V)		–	0.4	0.6	V
Shutdown Input Current ($V_{shutdown}$ = 2.5 V)		–	0.4	1.0	mA
OUTPUT DRIVERS (Each Output, V_{CC} = +20 V)					
Output Low Level (I_{sink} = 20 mA) (I_{sink} = 100 mA)	V_{OL}	 – –	 0.2 1.0	 0.4 2.0	V
Output High Level (I_{source} = 20 mA) (I_{source} = 100 mA)	V_{OH}	 18 17	 19 18	 – –	V
Under Voltage Lockout (V8 and V9 = High)	V_{UL}	6.0	7.0	8.0	V
Collector Leakage, V_C = +35 V (Note 7)	$I_{C(leak)}$	–	–	200	μA
Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	100	600	ns
Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	300	ns
Shutdown Delay (V_{DS} = +3.0 V, C_S = 0, T_J = +25°C)	t_{ds}	–	0.2	0.5	μs
Supply Current (V_{CC} = +35 V)	I_{CC}	–	14	20	mA

NOTE: 7. Applies to SG3525A only, due to polarity of output pulses.

Lab Test Fixture

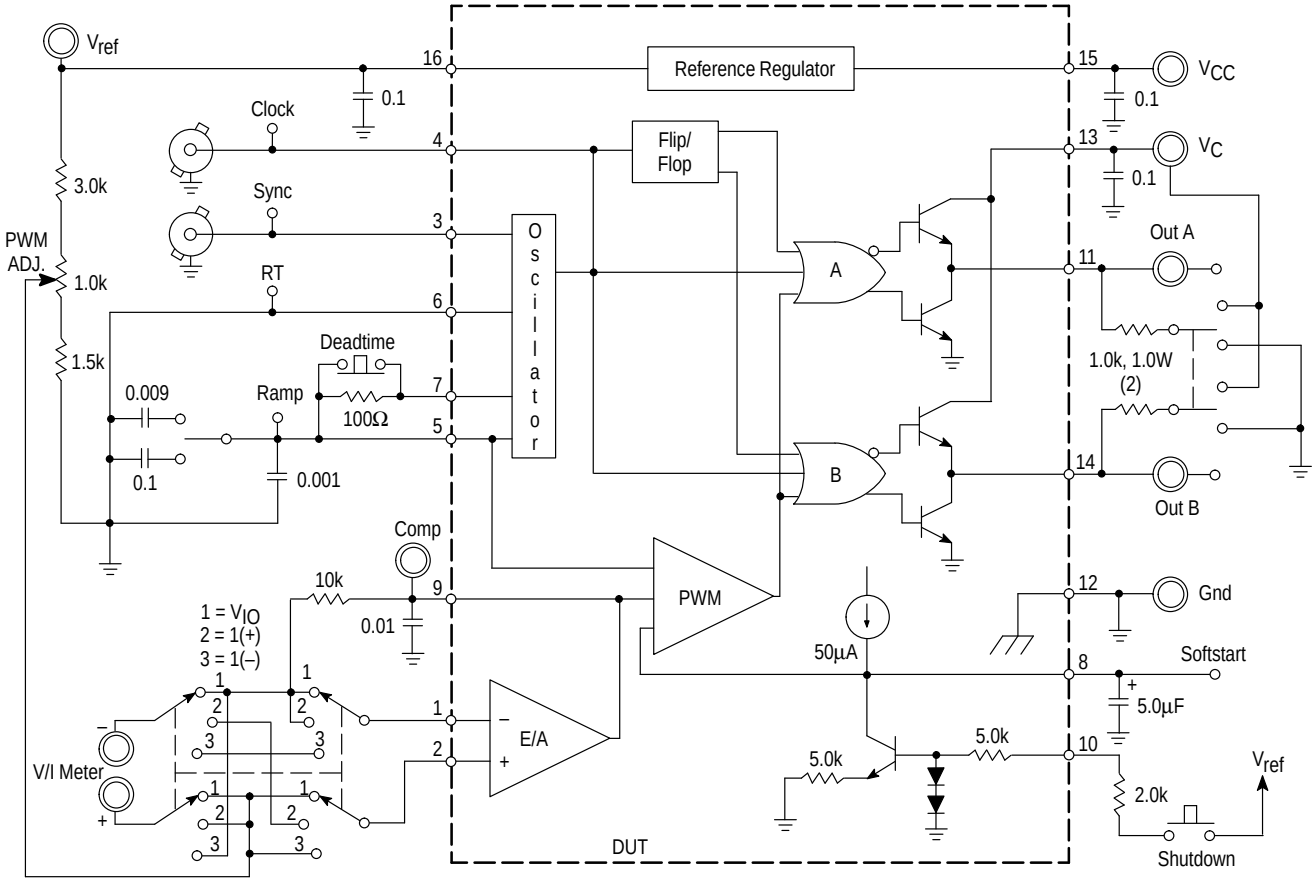


Figure 1. Oscillator Charge Time versus R_T

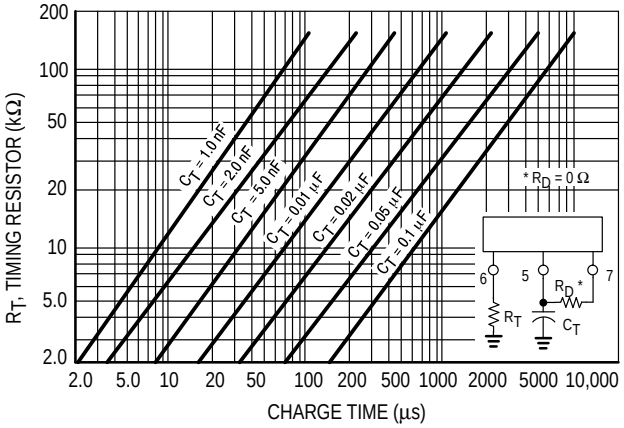


Figure 2. Oscillator Discharge Time versus R_D

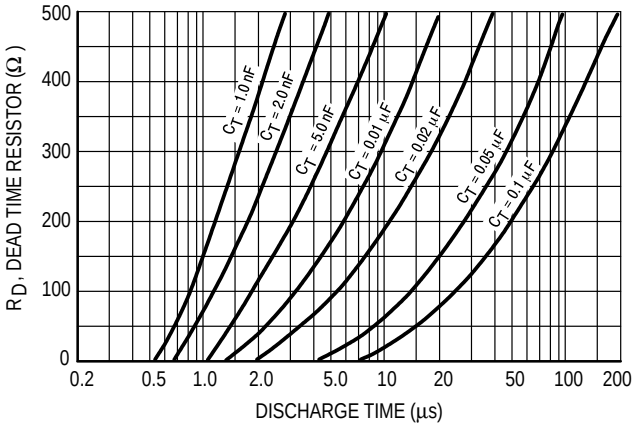


Figure 3. Error Amplifier Open Loop Frequency Response

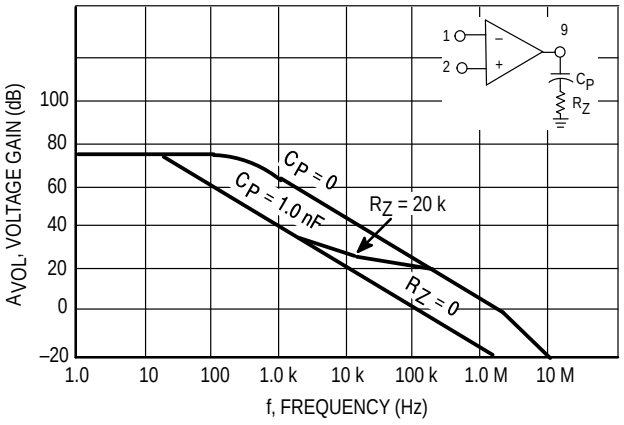


Figure 4. Output Saturation Characteristics (SG3525A)

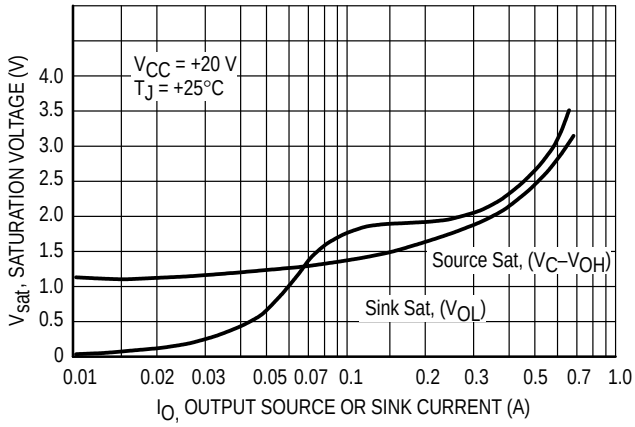


Figure 5. Oscillator Schematic (SG3525A)

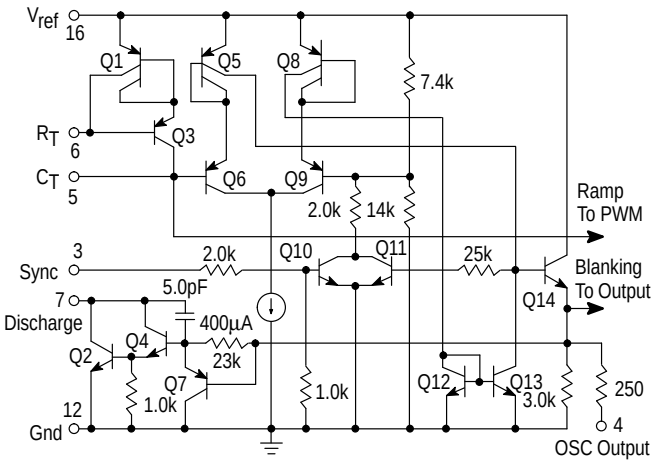


Figure 6. Error Amplifier Schematic (SG3525A)

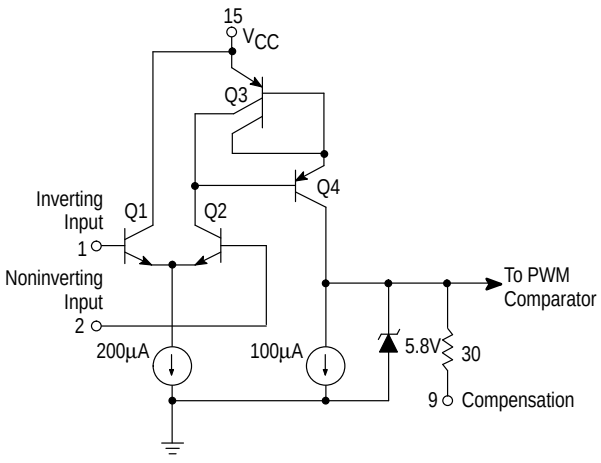


Figure 7. SG3525A Output Circuit
(1/2 Circuit Shown)

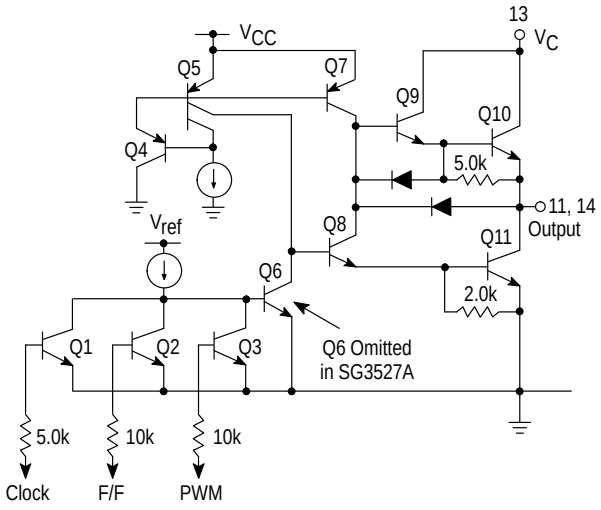
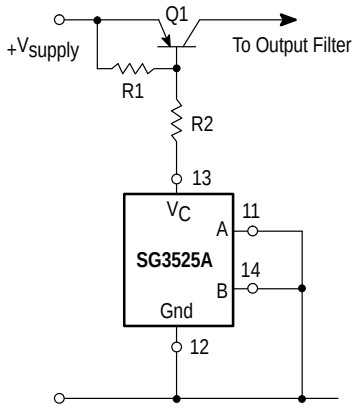
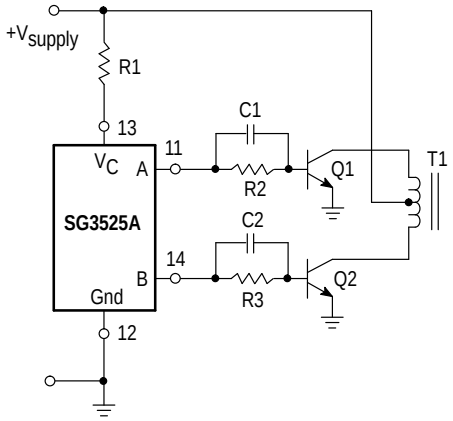


Figure 8. Single–Ended Supply



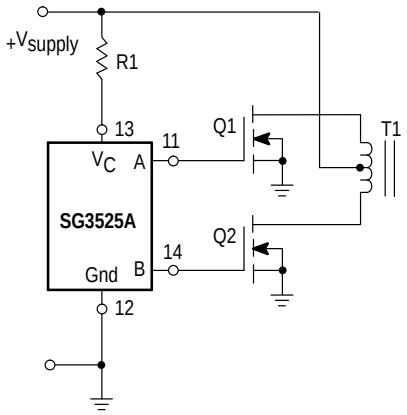
For single–ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem–pole source transistors on alternate oscillator cycles.

Figure 9. Push–Pull Configuration



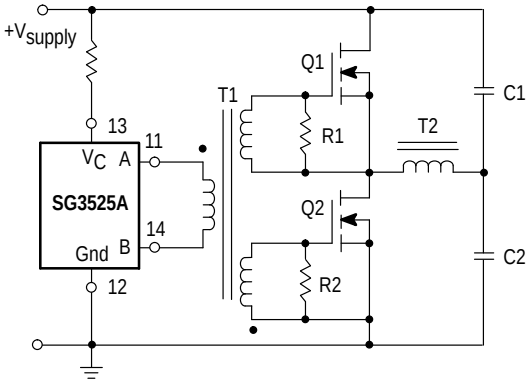
In conventional push–pull bipolar designs, forward base drive is controlled by R1–R3. Rapid turn–off times for the power devices are achieved with speed–up capacitors C1 and C2.

Figure 10. Driving Power FETS



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

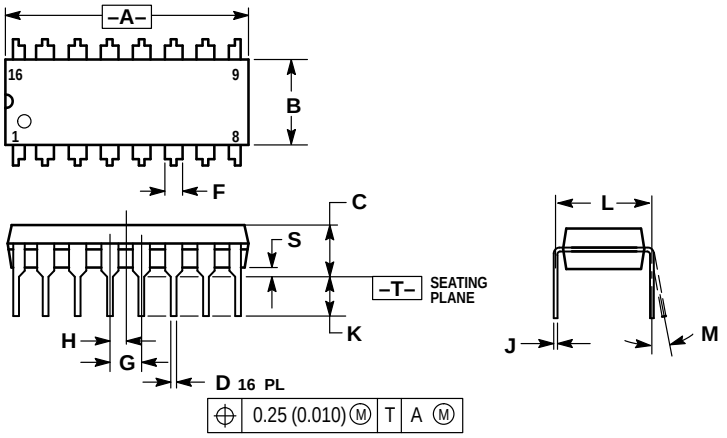
Figure 11. Driving Transformers in a Half–Bridge Configuration



Low power transformers can be driven directly by the SG3525A. Automatic reset occurs during deadtime, when both ends of the primary winding are switched to ground.

OUTLINE DIMENSIONS

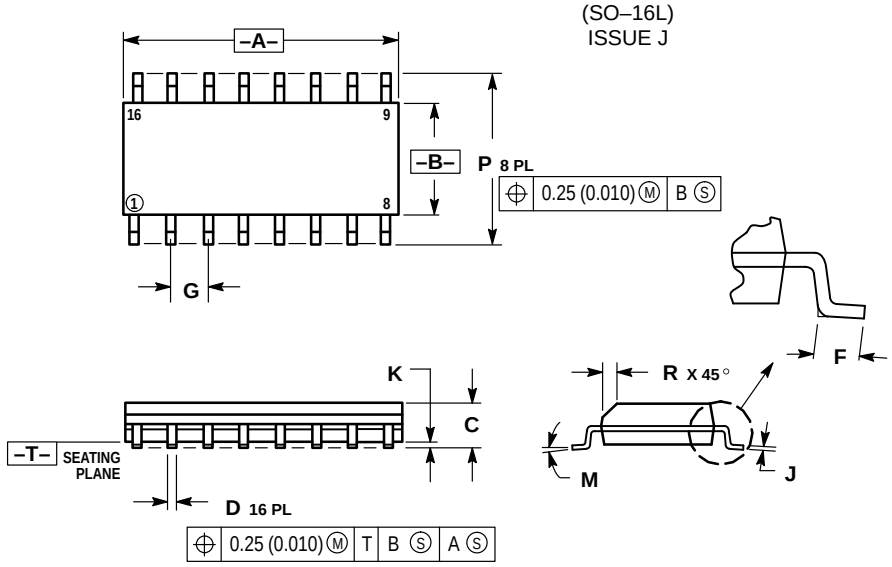
N SUFFIX
PLASTIC PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

DW SUFFIX
PLASTIC PACKAGE
CASE 751B–05
(SO–16L)
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

TC4426/TC4427/TC4428

1.5A Dual High-Speed Power MOSFET Drivers

Features:

- High Peak Output Current – 1.5A
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- High Capacitive Load Drive Capability – 1000 pF in 25 ns (typ.)
- Short Delay Times – 40 ns (typ.)
- Matched Rise and Fall Times
- Low Supply Current:
  - With Logic '1' Input – 4 mA
  - With Logic '0' Input – 400 µA
- Low Output Impedance – 7Ω
- Latch-Up Protected: Will Withstand 0.5A Reverse Current
- Input Will Withstand Negative Inputs Up to 5V
- ESD Protected – 4 kV
- Pin-compatible with the TC426/TC427/TC428
- Space-saving 8-Pin MSOP and 8-Pin 6x5 DFN Packages

Applications:

- Switch Mode Power Supplies
- Line Drivers
- Pulse Transformer Drive

General Description:

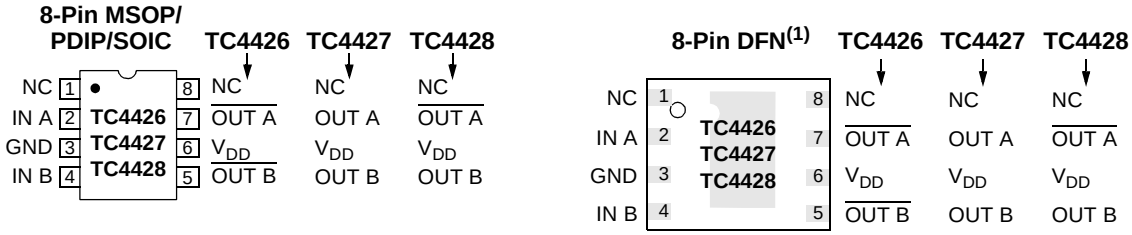
The TC4426/TC4427/TC4428 are improved versions of the earlier TC426/TC427/TC428 family of MOSFET drivers. The TC4426/TC4427/TC4428 devices have matched rise and fall times when charging and discharging the gate of a MOSFET.

These devices are highly latch-up resistant under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (of either polarity) occurs on the ground pin. They can accept, without damage or logic upset, up to 500 mA of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against Electrostatic Discharge (ESD) up to 4 kV.

The TC4426/TC4427/TC4428 MOSFET drivers can easily charge/discharge 1000 pF gate capacitances in under 30 ns. These devices provide low enough impedances in both the on and off states to ensure the MOSFET's intended state will not be affected, even by large transients.

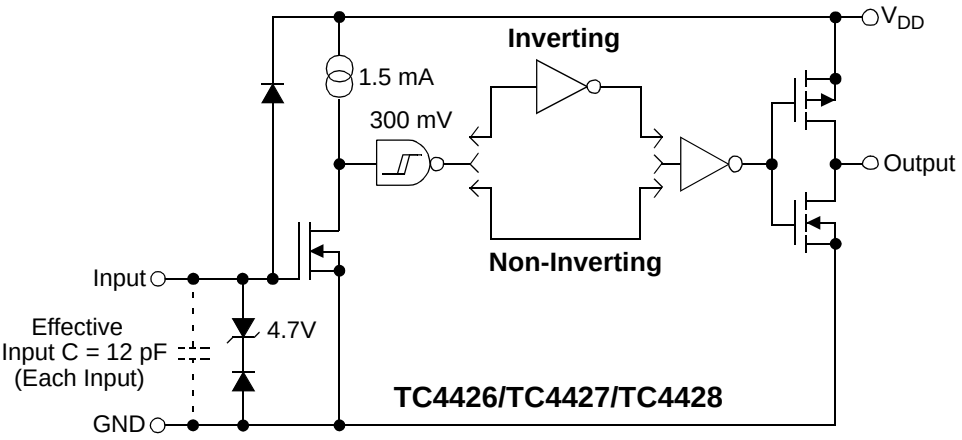
Other compatible drivers are the TC4426A/TC4427A/TC4428A family of devices. The TC4426A/TC4427A/TC4428A devices have matched leading and falling edge input-to-output delay times, in addition to the matched rise and fall times of the TC4426/TC4427/TC4428 devices.

Package Types



Note 1: Exposed pad of the DFN package is electrically isolated.

Functional Block Diagram



Note 1: TC4426 has two inverting drivers, while the TC4427 has two non-inverting drivers. The TC4428 has one inverting and one non-inverting driver.

2: Ground any unused driver input.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage ..... +22V

Input Voltage, IN A or IN B
..... (V_{DD} + 0.3V) to (GND – 5V)

Package Power Dissipation ($T_A \leq 70°C$)
DFN ..... **Note 3**
MSOP ..... 340 mW
PDIP ..... 730 mW
SOIC ..... 470 mW

Storage Temperature Range ..... -65°C to +150°C

Maximum Junction Temperature ..... +150°C

† Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

PIN FUNCTION TABLE

Name	Function
NC	No Connection
IN A	Input A
GND	Ground
IN B	Input B
OUT B	Output B
V_{DD}	Supply Input
OUT A	Output A
NC	No Connection

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, T_A = +25ºC with 4.5V $\leq V_{DD} \leq$ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic ‘1’, High Input Voltage	V_{IH}	2.4	—	—	V	**Note 2**
Logic ‘0’, Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	-1.0	—	+1.0	µA	$0V \leq V_{IN} \leq V_{DD}$
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance	R_O	—	7	10	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	1.5	—	A	V_{DD} = 18V
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	> 0.5	—	A	Duty cycle ≤ 2%, t ≤ 300 µs V_{DD} = 18V
Switching Time (Note 1)						
Rise Time	t_R	—	19	30	ns	**Figure 4-1**
Fall Time	t_F	—	19	30	ns	**Figure 4-1**
Delay Time	t_{D1}	—	20	30	ns	**Figure 4-1**
Delay Time	t_{D2}	—	40	50	ns	**Figure 4-1**
Power Supply						
Power Supply Current	I_S	— —	— —	4.5 0.4	mA	V_{IN} = 3V (Both inputs) V_{IN} = 0V (Both inputs)

Note 1: Switching times ensured by design.

2: For V temperature range devices, the V_{IH} (Min) limit is 2.0V.

3: Package power dissipation is dependent on the copper pad area on the PCB.

DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE)

Electrical Specifications: Unless otherwise noted, over operating temperature range with 4.5V ≤ V_{DD} ≤ 18V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	—	—	V	**Note 2**
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	-10	—	+10	µA	0V ≤ V_{IN} ≤ V_{DD}
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance	R_O	—	9	12	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	1.5	—	A	V_{DD} = 18V
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	>0.5	—	A	Duty cycle ≤ 2%, t ≤ 300 µs V_{DD} = 18V
Switching Time (Note 1)						
Rise Time	t_R	—	—	40	ns	**Figure 4-1**
Fall Time	t_F	—	—	40	ns	**Figure 4-1**
Delay Time	t_{D1}	—	—	40	ns	**Figure 4-1**
Delay Time	t_{D2}	—	—	60	ns	**Figure 4-1**
Power Supply						
Power Supply Current	I_S	— —	— —	8.0 0.6	mA	V_{IN} = 3V (Both inputs) V_{IN} = 0V (Both inputs)

Note 1: Switching times ensured by design.

2: For V temperature range devices, the V_{IH} (Min) limit is 2.0V.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with 4.5V ≤ V_{DD} ≤ 18V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range (C)	T_A	0	—	+70	°C	
Specified Temperature Range (E)	T_A	-40	—	+85	°C	
Specified Temperature Range (V)	T_A	-40	—	+125	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 8L-6x5 DFN	θ_{JA}	—	33.2	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	206	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	—	125	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	155	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25ºC with 4.5V ≤ V_{DD} ≤ 18V.

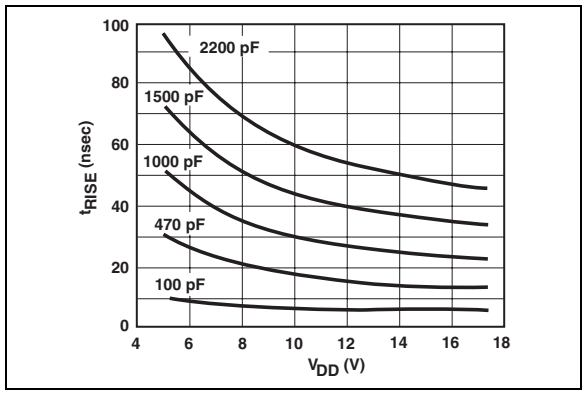


FIGURE 2-1: *Rise Time vs. Supply Voltage.*

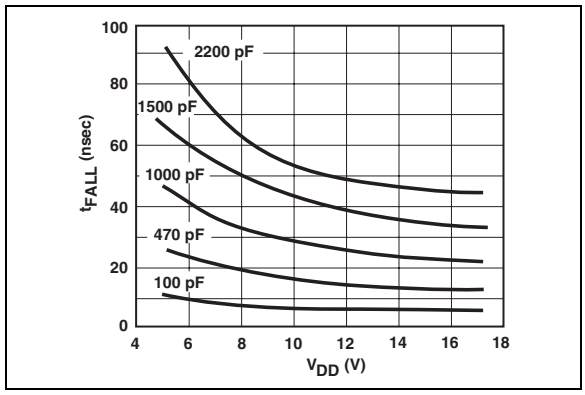


FIGURE 2-4: *Fall Time vs. Supply Voltage.*

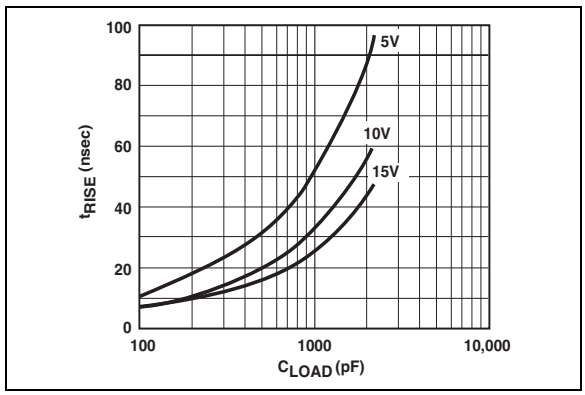


FIGURE 2-2: *Rise Time vs. Capacitive Load.*

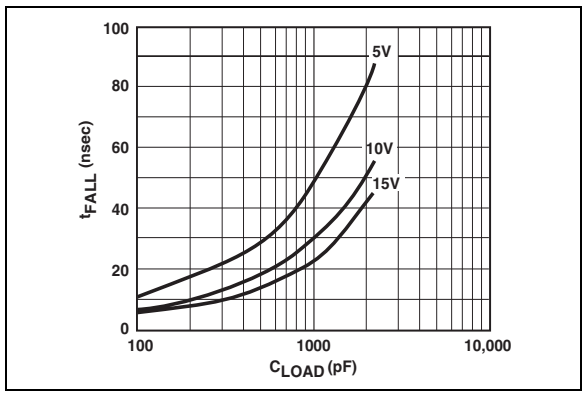


FIGURE 2-5: *Fall Time vs. Capacitive Load.*

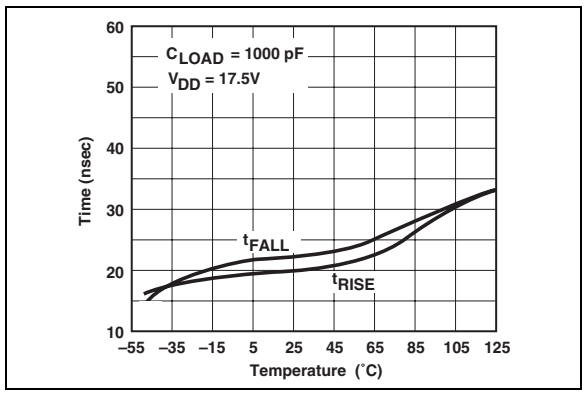


FIGURE 2-3: *Rise and Fall Times vs. Temperature.*

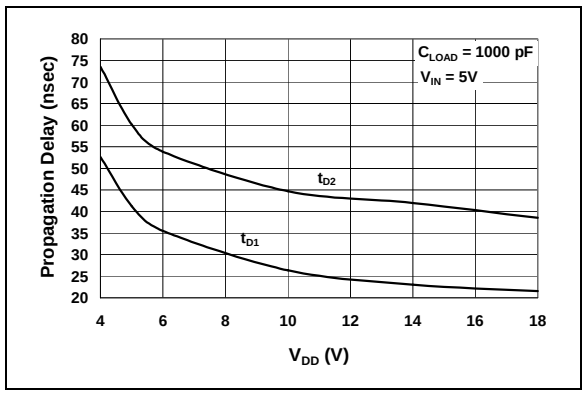


FIGURE 2-6: *Propagation Delay Time vs. Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25ºC with 4.5V ≤ V_{DD} ≤ 18V.

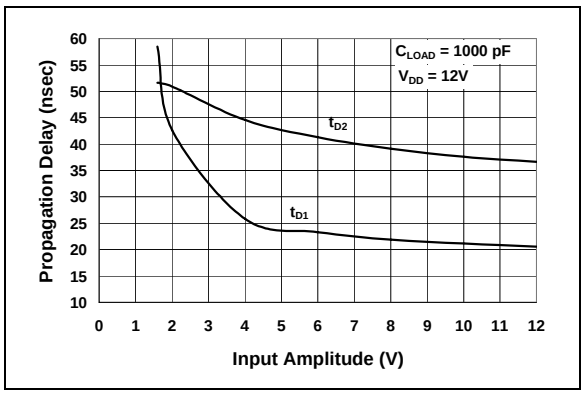


FIGURE 2-7: *Propagation Delay Time vs. Input Amplitude.*

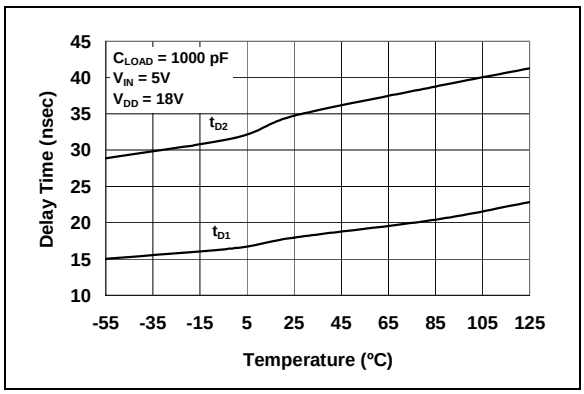


FIGURE 2-10: *Propagation Delay Time vs. Temperature.*

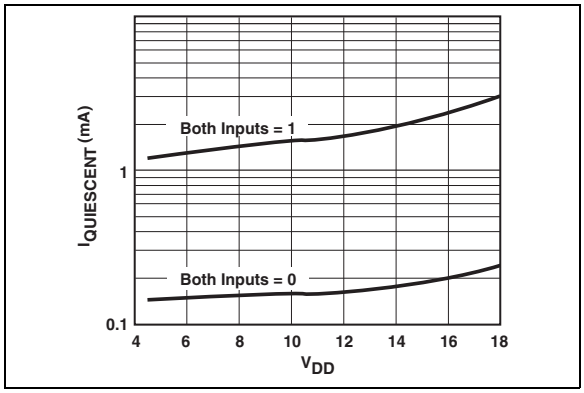


FIGURE 2-8: *Supply Current vs. Supply Voltage.*

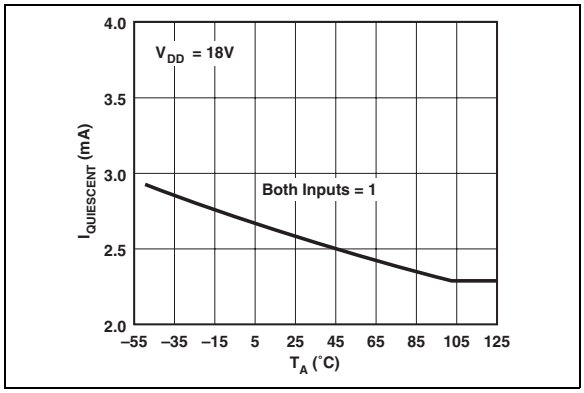


FIGURE 2-11: *Supply Current vs. Temperature.*

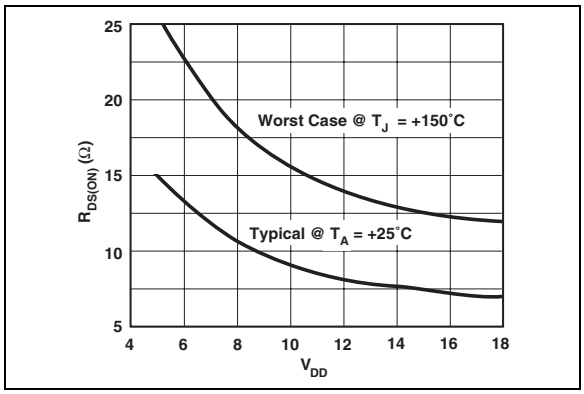


FIGURE 2-9: *Output Resistance (R_{OH}) vs. Supply Voltage.*

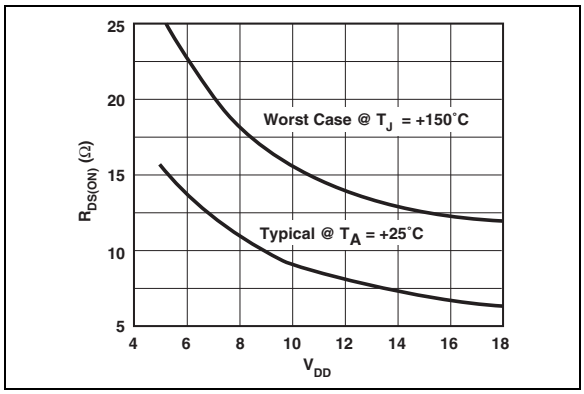


FIGURE 2-12: *Output Resistance (R_{OL}) vs. Supply Voltage.*

Note: Unless otherwise indicated, T_A = +25ºC with 4.5V ≤ V_{DD} ≤ 18V.

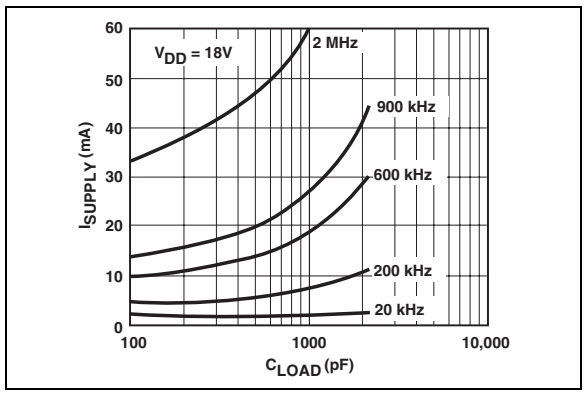


FIGURE 2-13: *Supply Current vs. Capacitive Load.*

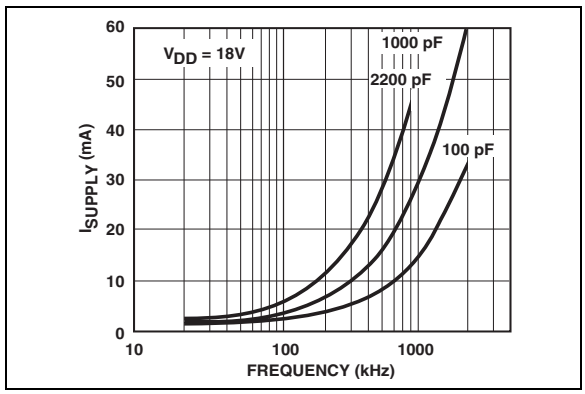


FIGURE 2-16: *Supply Current vs. Frequency.*

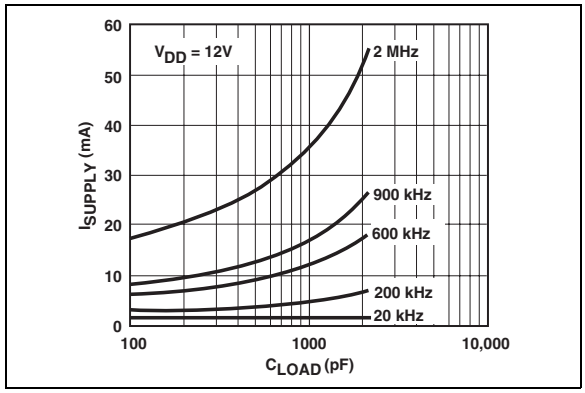


FIGURE 2-14: *Supply Current vs. Capacitive Load.*

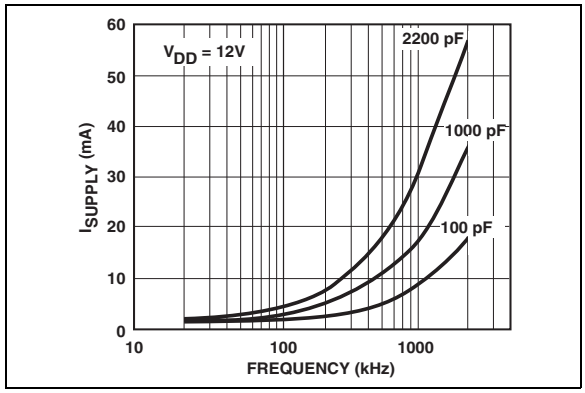


FIGURE 2-17: *Supply Current vs. Frequency.*

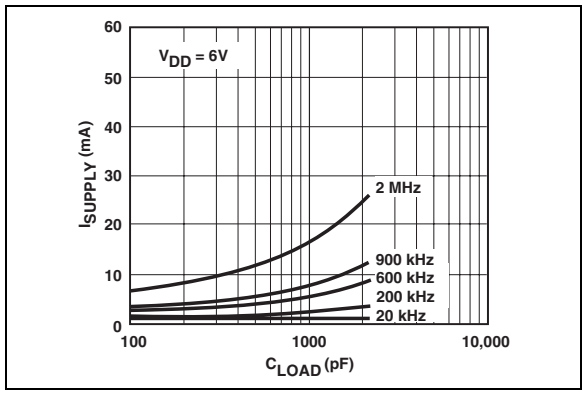


FIGURE 2-15: *Supply Current vs. Capacitive Load.*

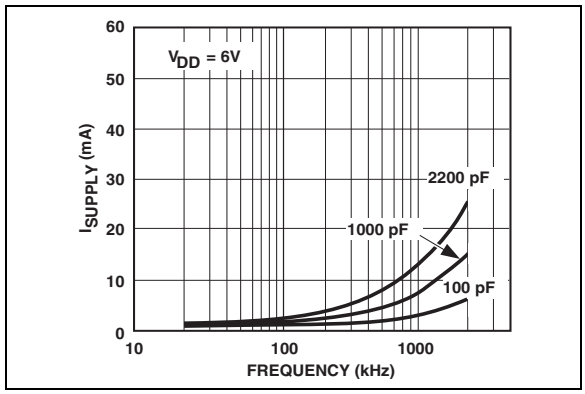
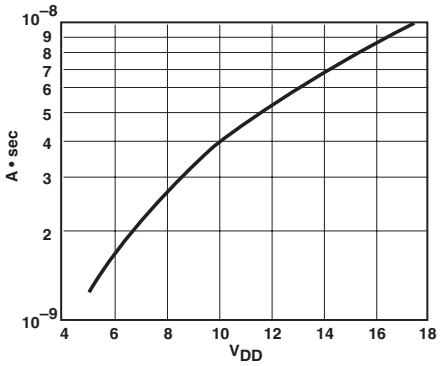


FIGURE 2-18: *Supply Current vs. Frequency.*

Note: Unless otherwise indicated, T_A = +25ºC with 4.5V ≤ V_{DD} ≤ 18V.



Note: The values on this graph represent the loss seen by both drivers in a package during one complete cycle. For a single driver, divide the stated values by 2. For a single transition of a single driver, divide the stated value by 4.

FIGURE 2-19: *Crossover Energy vs. Supply Voltage.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE (1)

8-Pin PDIP/ MSOP/SOIC	8-Pin DFN	Symbol	Description
1	1	NC	No connection
2	2	IN A	Input A
3	3	GND	Ground
4	4	IN B	Input B
5	5	OUT B	Output B
6	6	V_{DD}	Supply input
7	7	OUT A	Output A
8	8	NC	No connection
—	PAD	NC	Exposed Metal Pad

Note 1: Duplicate pins must be connected for proper operation.

3.1 Inputs A and B

MOSFET driver inputs A and B are high-impedance, TTL/CMOS compatible inputs. These inputs also have 300 mV of hysteresis between the high and low thresholds that prevents output glitching even when the rise and fall time of the input signal is very slow.

3.2 Ground (GND)

Ground is the device return pin. The ground pin(s) should have a low-impedance connection to the bias supply source return. High peak currents will flow out the ground pin(s) when the capacitive load is being discharged.

3.3 Output A and B

MOSFET driver outputs A and B are low-impedance, CMOS push-pull style outputs. The pull-down and pull-up devices are of equal strength, making the rise and fall times equivalent.

3.4 Supply Input (V_{DD})

The V_{DD} input is the bias supply for the MOSFET driver and is rated for 4.5V to 18V with respect to the ground pin. The V_{DD} input should be bypassed with local ceramic capacitors. The value of these capacitors should be chosen based on the capacitive load that is being driven. A value of 1.0 µF is suggested.

3.5 Exposed Metal Pad

The exposed metal pad of the 6x5 DFN package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane or other copper plane on a printed circuit board, to aid in heat removal from the package.

4.0 APPLICATIONS INFORMATION

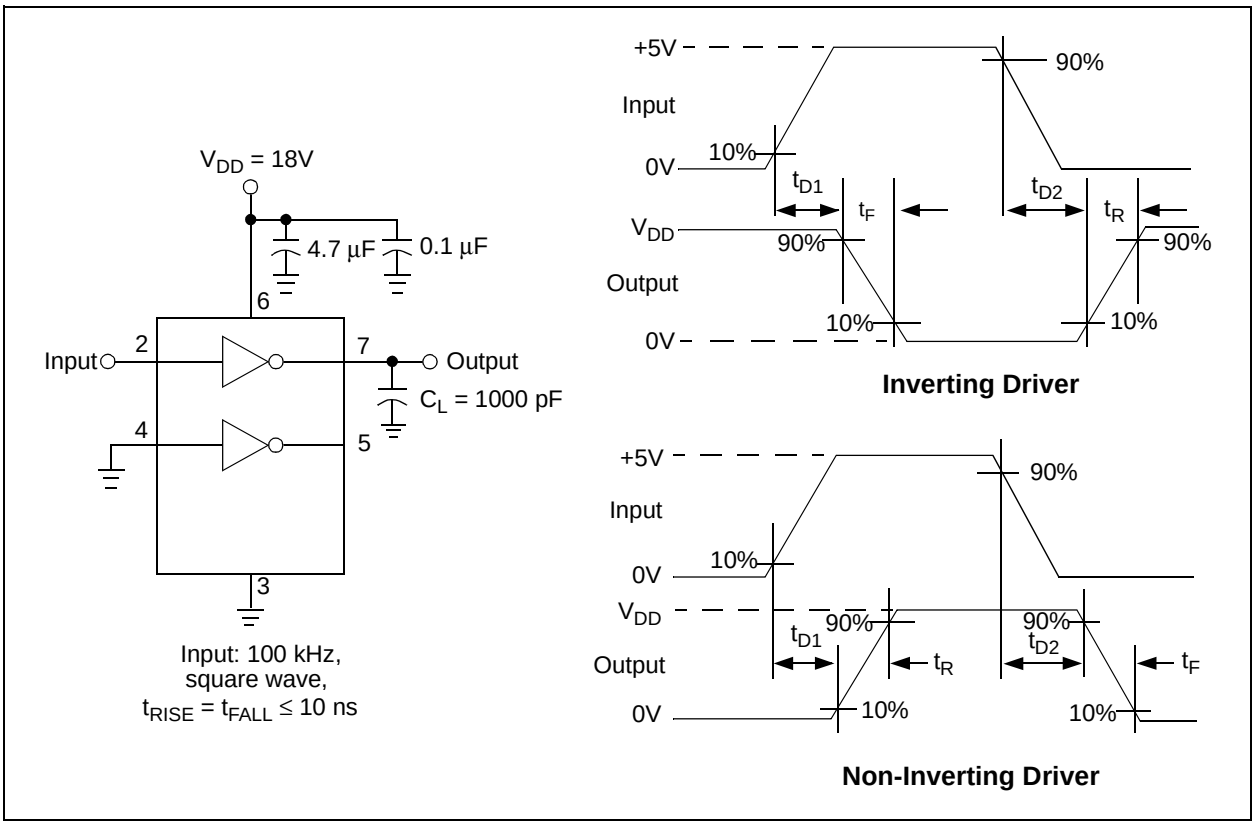
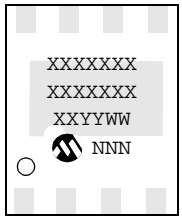


FIGURE 4-1: *Switching Time Test Circuit.*

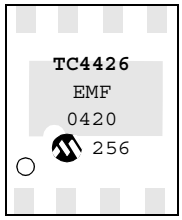
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

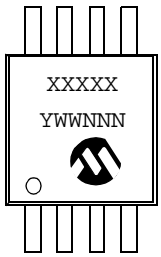
8-Lead DFN



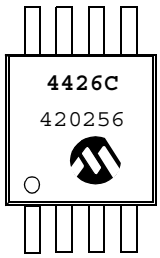
Example:



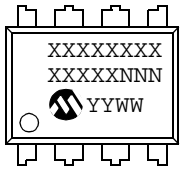
8-Lead MSOP



Example:



8-Lead PDIP (300 mil)



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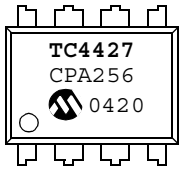
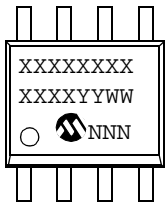


8-Lead SOIC (150 mil)



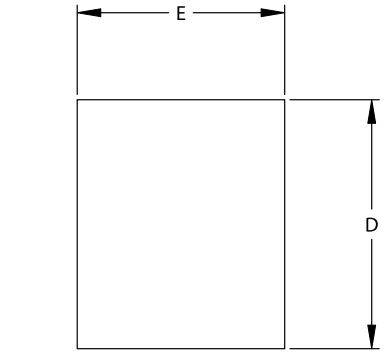
Example:

Legend:	XX...X	Customer specific information*
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

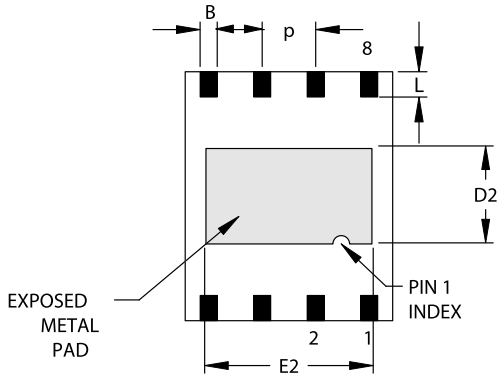
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard device marking consists of Microchip part number, year code, week code, and traceability code.

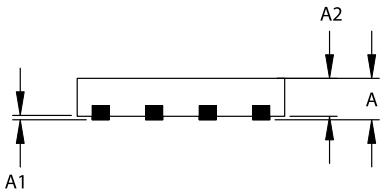
8-Lead Plastic Dual Flat No Lead Package (MF) 6x5 mm Body (DFN-S) – Saw Singulated

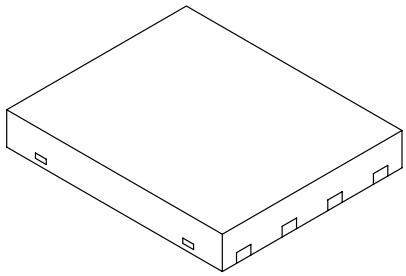


TOP VIEW



BOTTOM VIEW





Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p	.050 BSC			1.27 BSC		
Overall Height	A	.033	.035	.037	0.85	0.90	0.95
Package Thickness	A2	.031	.035	.037	0.80	0.89	0.95
Standoff	A1	.000	.0004	.002	0.00	0.01	0.05
Base Thickness	A3	.007	.008	.009	0.17	0.20	0.23
Overall Length	E	.195	.197	.199	4.95	5.00	5.05
Exposed Pad Length	E2	.152	.157	.163	3.85	4.00	4.15
Overall Width	D	.234	.236	.238	5.95	6.00	6.05
Exposed Pad Width	D2	.089	.091	.093	2.25	2.30	2.35
Lead Width	B	.014	.016	.019	0.35	0.40	0.47
Lead Length	L	.024		.026	0.60		0.65

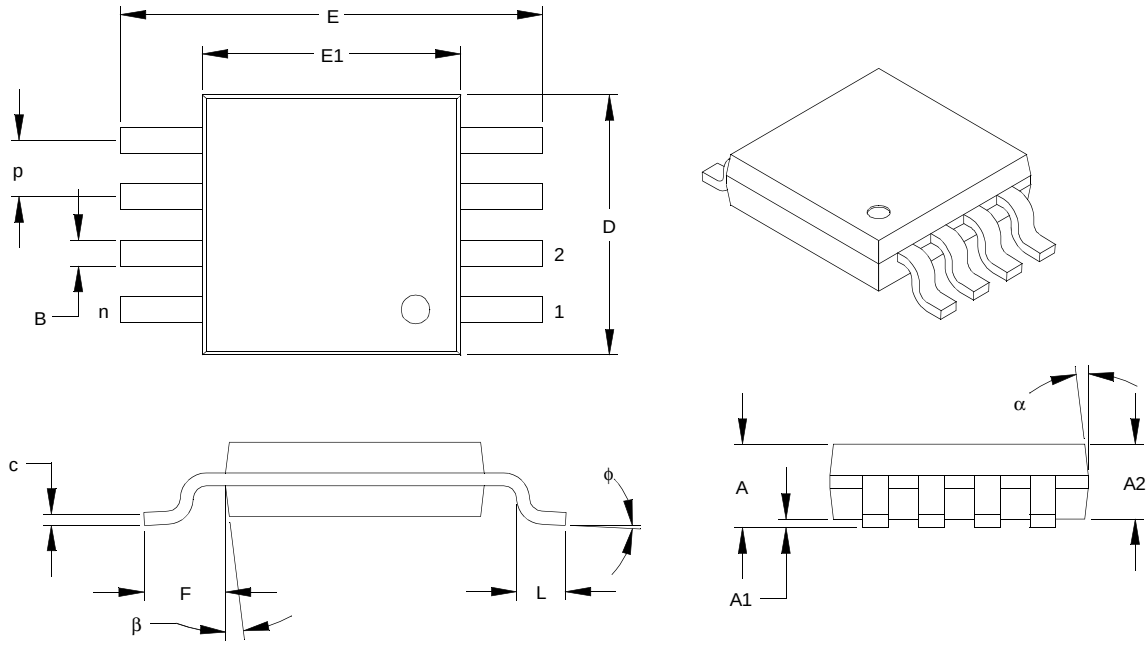
Notes:

JEDEC equivalent: MO-220

Drawing No. C04-122

Revised 11/3/03

8-Lead Plastic Micro Small Outline Package (MS) (MSOP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 BSC			4.90 BSC	
Molded Package Width	E1		.118 BSC			3.00 BSC	
Overall Length	D		.118 BSC			3.00 BSC	
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF			0.95 REF	
Foot Angle	φ	0°	-	8°	0°	-	8°
Lead Thickness	c	.003	.006	.009	0.08	-	0.23
Lead Width	B	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°	5°	-	15°

***** Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

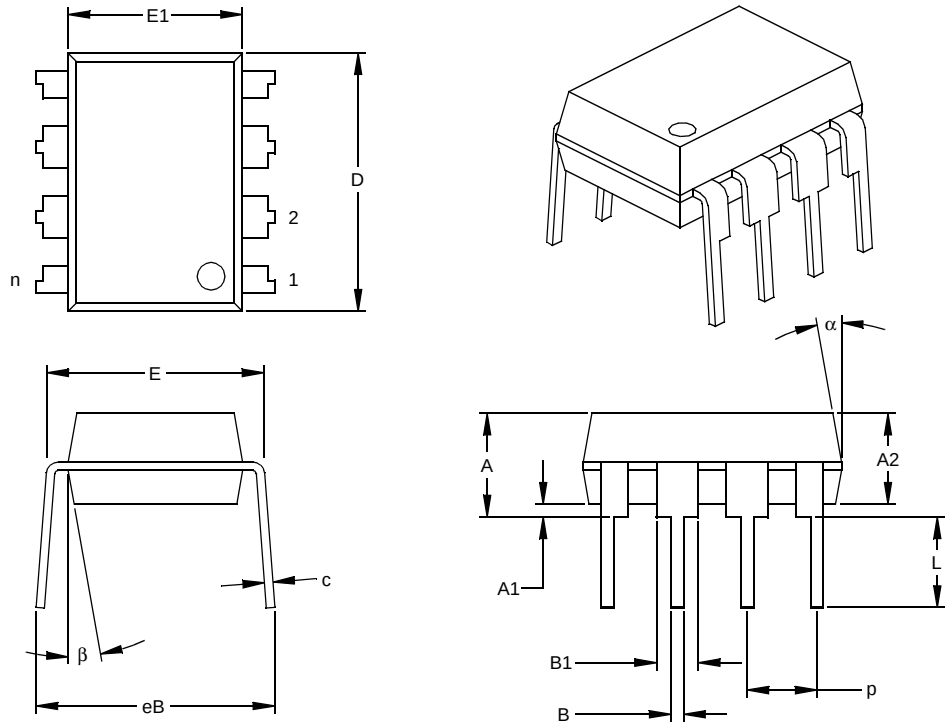
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
See ASME Y14.5M

REF: Reference Dimension, usually without tolerance, for information purposes only.
See ASME Y14.5M

JEDEC Equivalent: MO-187 Revised 07-21-05

Drawing No. C04-111

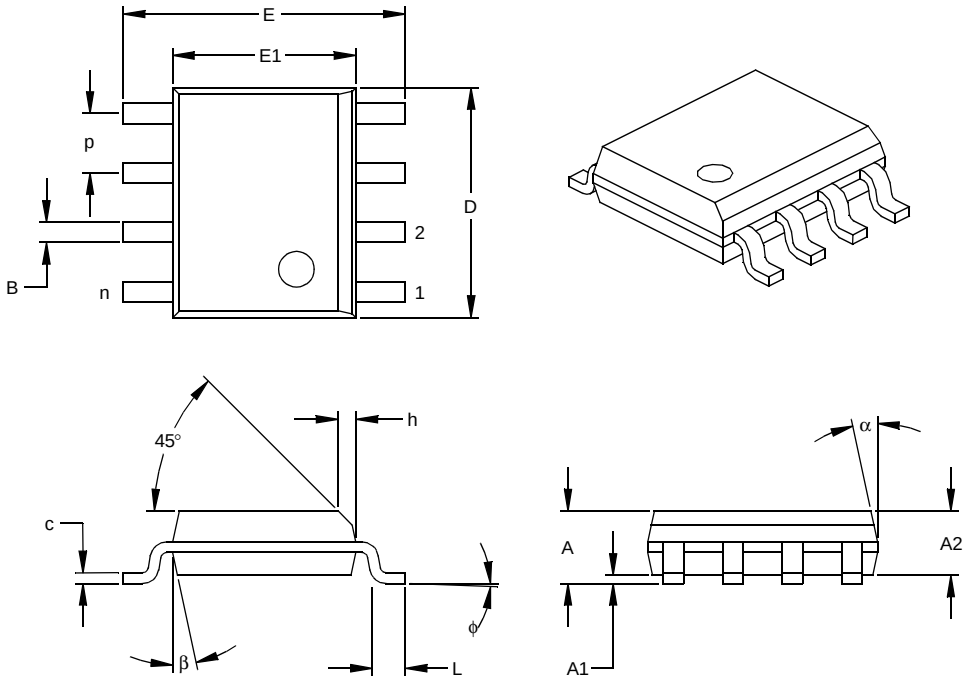
8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

***** Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

***** Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	XX	XXX	X
Device	Temperature Range	Package	Tape & Reel	PB Free

Device:	TC4426:	1.5A Dual MOSFET Driver, Inverting
	TC4427:	1.5A Dual MOSFET Driver, Non-Inverting
	TC4428:	1.5A Dual MOSFET Driver, Complementary
Temperature Range:	C =	0°C to +70°C (PDIP and SOIC only)
	E =	-40°C to +85°C
	V =	-40°C to +125°C
Package:	MF =	Dual, Flat, No-Lead (6X5 mm Body), 8-lead
	MF713 =	Dual, Flat, No-Lead (6X5 mm Body), 8-lead (Tape and Reel)
	OA =	Plastic SOIC, (150 mil Body), 8-lead
	OA713 =	Plastic SOIC, (150 mil Body), 8-lead (Tape and Reel)
	PA =	Plastic DIP (300 mil Body), 8-lead
	UA =	Plastic Micro Small Outline (MSOP), 8-lead
	UA713 =	Plastic Micro Small Outline (MSOP), 8-lead (Tape and Reel)

Examples:

a) TC4426COA: 1.5A Dual Inverting MOSFET driver, 0°C to +70°C SOIC package.

b) TC4426EUA: 1.5A Dual Inverting MOSFET driver, -40°C to +85°C. MSOP package.

c) TC4426EMF: 1.5A Dual Inverting MOSFET driver, -40°C to +85°C, DFN package.

a) TC4427CPA: 1.5A Dual Non-Inverting MOSFET driver, 0°C to +70°C PDIP package.

b) TC4427EPA: 1.5A Dual Non-Inverting MOSFET driver, -40°C to +85°C PDIP package.

a) TC4428COA713: 1.5A Dual Complementary MOSFET driver, 0°C to +70°C, SOIC package, Tape and Reel.

b) TC4428EMF: 1.5A Dual Complementary, MOSFET driver, -40°C to +85°C DFN package.

Sales and Support

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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ISO/TS 16949:2002

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