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Nano-Dimensional Properties of Si-FinFET Transistor Based on I_{ON}/I_{OFF} Ratio and Subthreshold Swing (SS)

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ABSTRACT

This paper presents design the optimal channel dimensions for Silicon Fin Feld Effect Transistor (Si-FinFET) for improvement electrical characteristic of Si-FinFET depending on the electrical characteristics of the channel (I_{ON}/I_{OFF}, SS, V_T, DIBL). The MuGFET simulation tool has been using to investigate the electrical characteristics of Si-FinFET. The current voltage characteristics has been simulating with different dimensions channel (length, width and oxide thickness). The best channel dimensions of Si-FinFET observed based on electrical characteristics at the working voltage V_{DD} range of 0-5 V. Note that the results with the scaling channel dimensions. Depending on I_{ON}/I_{OFF} ratio higher value, and nearest SS to the ideal SS, the best scaling channel dimensions (K) will be K=0.25 at V_{DD}=5 V and K=0.25 at V_{DD}=0.5 V.

1. Introduction

Electronic engineering has played an important role in the development of science and knowledge, and most importantly in the evolution of integrated circuit manufacturing (ICs) [1, 2].

Many new field effect transistor (FET) structures have been extensively explored given that the metal oxide semiconductor FET (MOSFET) technology (Fig. 1) [3]. As the transistor approaches the effect of the MOSFET from the scaling limits, the adverse consequences arising from short channel effects become increasingly important. Many new FET structures are being explored on a large scale. One of these FETs was the FinFET, this transistor structure has attracted widespread interest from researchers in the fields of industry and academic studies of semiconductors [2].

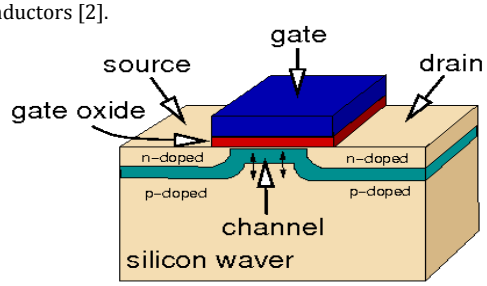

Fig. 1 Metal-oxide field-effect transistor (MOSFET)

FinFET technology takes name from the fact that the FET structure used looks like a set of fins when viewed this form of gate structure provides improved electrical control over the channel conduction and it helps reduce leakage current levels and overcomes some other short-channel effects.

To minimize channel dimensions in the FinFET design (Fig. 2), there is a need to simulate the characterization of FinFET behaviour and assist in decision-making. Over the past decade, there have been many researches focused on manufacturing FINFETs with different nanometres such as semiconductor materials, insulation materials, and various manufacturing techniques [4]. that have been developed to predict the performance of FIN electronic devices, such as diodes, transistors, capacitors and resistors, with Nano-dimensions have recently become popular in the electronics industry due to their extremely small electronic circuits [5-7].

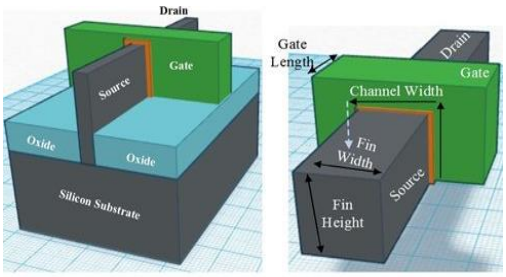

Fig. 2 FinFET structure

The performance of new devices, which may correspond to a wide array of new applications, will likely depend on the nano-dimensional characteristics of such devices. The chip generation of these relatively new and powerful electronic devices with ultra-small transistors may be even regarded more trustable when new findings from future research are consolidated. However, the new nano-dimensional FET designs and structures are still considered novel technologies and thus necessitate further study and improvement, and they require further innovations despite the limitations in the field of MOSFET science. Electronic device simulation has become increasingly important in understanding the physics behind the structures of new devices. Thus, simulation tools are adopted in this research for the analysis and evaluation of the performance limits of Si FinFET structures. Experimental work can be supported by simulation tools to further explore the development of MuGFETs for nano-dimensional characterization [8]. Simulation tools can also help identify device strengths, weaknesses, and retrenchment costs and illustrate the extensibility of these devices in the nm range [8, 9].

2. Experimental Methods

In this research, MuGFET is used as the simulation tool to investigate the characteristics of the FinFET transistor. The output characteristic curves of the transistor under different conditions and with different parameters are considered.

The effects of variable values, namely, gate length, width and oxide thickness on the Si FinFET transistor are determined based on the I–V characteristics derived from the simulation. The MuGFET [10] simulation tool used for the FET with Nano-dimensional structure is developed and designed by Purdue University (USA).

MuGFET can select either PADRE or PROPHET for simulation, in which both simulates are developed by Bell Laboratories. PROPHET is a partial

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differential equation profiler for one, two or three dimensions, whereas PADRE is a device-oriented simulator for 2D or 3D devices with arbitrary geometry. The software can generate useful characteristic FET curves for engineers, especially to fully explain the underlying physics of FETs. MuGFET can also provide self-consistent solutions to poison and drift-diffusion equations [3]. In this research, the Id–Vg characteristics of Si-FinFET at the temperature of 300 K are simulated with the parameters in Table 1.

Table 1 The parameter used in this research

Parameters	Value
Channel length (L)	(5, 10, 15, 20 and 40) nm
Channel width (W)	(5, 10, 12, 15 and 20) nm
Oxide thickness (T_{OX})	(1.5, 2.5, 5 and 7) nm
Scaling factor (K)	(0.25, 0.5, 0.75 and 1.00)
channel concentration p -type	10^{16} cm^{-3}
channel concentration N -type	10^{19} cm^{-3}

3. Results and Discussion

3.1 Channel Length Characteristics Results

The scaling down of channel length L and its effect on the characteristics of Si-FinFET have been study. The simulation of transfer characteristics (drain current I_d –gate voltage V_g) have been down with different channel lengths (L), channel width (W), and oxide thicknesses (T_{ox}). The limitation parameters were used to find the optimal channel dimensions were I_{ON}/I_{OFF} ratio (where I_{OFF} is an I_d at OFF state at V_g = 0 V and I_{ON} is an I_d at ON state at V_g = 1V), and subthreshold swing (SS) and the threshold voltage (V_T) and drain-induced barrier lowering (DIBL).

Fig. 3 shows the I_{ON}/I_{OFF} ratio with the channel length of 5, 10, 15, 20, and 40 nm, and at W = 5 nm and T_{ox} = 2.5 nm, the I_{ON} /I_{OFF} increased up to more than 10^8 for increasing L from 5 to 40 nm for V_{DD}=5 V, and for V_{DD} = 0.5 V, the maximum value for I_{ON}/I_{OFF} were more than10^7 at L=40 nm. It is notice that, for L range from 5 to 20 nm the highest I_{ON}/I_{OFF} happen for V_{DD}=0.5 V, while for 20 to 40 nm L range highest I_{ON}/I_{OFF} happen for V_{DD} = 5 V.

Fig. 4 presents the channel length characteristics of (SS) of the FinFET, in this results the channel length were 5, 10, 15, 20, and 40 nm, the W = 5 nm and Tox = 2.5 nm. This figure illustrates that the SS started with 77.7 mV/dec at L = 15 nm which is the furthest value from the ideal SS (59.5 mV/dec), and then decreases with increasing the channel length, at L=40 nm, the nearest value to the ideal SS (60.6 mV/dec) where happen.

Fig. 5 presents the channel length characteristics of threshold voltage (V_T), and drain-induced barrier lowering (DIBL) of the FinFET. V_T increased linearly with increasing the channel length, where V_T = 0.65 V at the higher channel length of 40 nm and V_T = 0.25 V at the lowest channel length of 5 nm. Finally, the DIBL decreased as channel length increased until it reached 7.8 mV/V at length of channel = 40 nm.

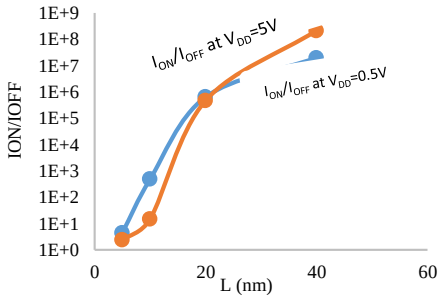

Fig. 3 I_{ON}/I_{OFF} ratio with channel length of Si-FinFET

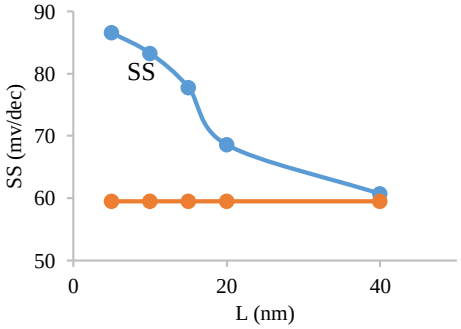

Fig. 4 SS with channel length of Si-FinFET

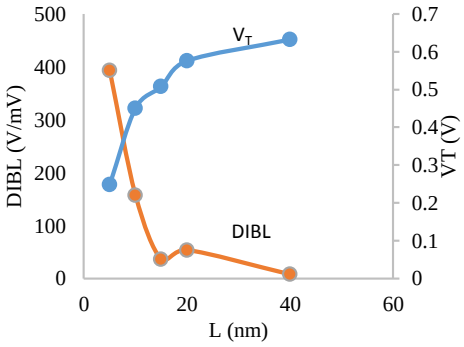

Fig. 5 V_T and DIBL with channel length of Si-FinFET

3.2 Channel Width Characteristic Results

The scaling down of channel width W and its effect on the characteristics of Si FinFET have been study. Fig. 6 shows the I_{ON}/I_{OFF} ratio with the channel width of 5, 10, 15 and 20 nm, and at L= 40 nm and T_{ox} = 2.5 nm, with increasing W from 5 to 20 nm. The value of I_{ON}/I_{OFF} decreased to 10^3 at V_{DD} = 5 V and W = 20 nm, and for V_{DD} = 0.5 V the I_{ON} /I_{OFF} decreased to 10^4 at W = 20 nm. It is notice that, for W range from 5 to 12 nm the highest I_{ON}/I_{OFF} happen for V_{DD} = 5V, while for 12 to 20 nm W range highest I_{ON}/I_{OFF} happen for V_{DD} = 0.5V. Fig. 7 presents the channel with characteristics of subthreshold swing (SS) of the FinFET, in this results the channel width were 5, 10, 15 and 20 nm, the L = 40 nm and T_{ox} = 2.5 nm. This figure illustrates that the SS started with 60.65 mV/dec at W = 5 nm which is the closest value from the ideal SS (95.5 mV/dec), and increases with increasing the channel width, until it reaches the highest value (75.69mV/dec) at W = 20 nm.

Fig. 8 presents the channel width characteristics of threshold voltage (V_T), and drain-induced barrier lowering (DIBL) of the FinFET. V_T decreased with increasing the channel width, where V_T = 0.63 V at the higher channel with of 5nm and V_T = 0.47 V at the lowest channel with of 20 nm. Finally, the DIBL increased as channel width increased until it reached 69.3 mV/V at width of channel=20nm.

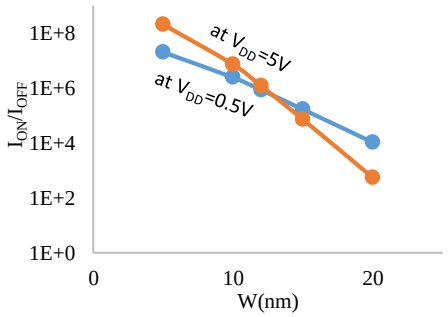

Fig. 6 I_{ON}/I_{OFF} with channel width of Si-FinFET

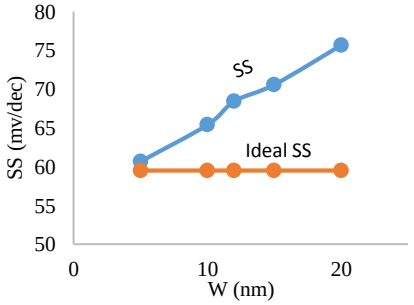

Fig. 7 SS with channel width of Si-FinFET

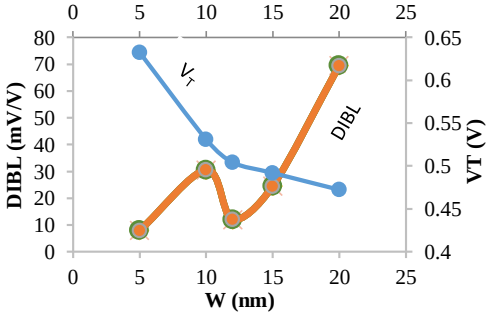

Fig. 8 V_T, DIBL with channel width of Si-FinFET

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3.3 Channel Oxide Thickness Characteristics

The scaling down of channel oxide thickness and its effect on the characteristics of Si FinFET have been study. Fig. 9 shows the I_{ON}/I_{OFF} ratio with the channel oxide thickness of 1.5, 2.5, 5 and 7 nm, and at L=40 nm and W=5 nm, for increasing T_{OX} from 1.5 to 7 nm. The maximum value for I_{ON}/I_{OFF} (more than 10^7) at V_{DD}=5 V happen at T_{OX}=1.5 nm and after that decreased to about 10^2 at T_{OX} = 7 nm, and for V_{DD} = 0.5 V the I_{ON}/I_{OFF} highest value (more than10^6) at W= 1.5 nm and the decrease to 10^3 at T_{OX}= 7 nm.

Fig. 10 presents the channel with characteristics of subthreshold swing (SS) of the FinFET, in this results the channel oxide thickness were 1.5, 2.5, 5 and 7 nm, the L = 40 nm and W = 12 nm. This figure illustrates that the SS started with 62.85 mV/dec at T_{OX} = 1.5 nm which is the closest value to the ideal SS (59.5 mV/dec), and then increased with increasing the channel oxide thickness, until it reached to highest value (106 mV/dec) at T_{OX}=7 nm.

Fig. 11 presents the channel oxide thickness characteristics of threshold voltage (V_T), and drain-induced barrier lowering (DIBL) of the FinFET. V_T increased with increasing the channel oxide thickness, where V_T = 0.49 V at T_{OX} = 1.5 nm. and V_T = 0.53 V at channel oxide thickness of 7nm Finally, the DIBL increased from 5.49 mv/v to 99.3 mV/V, while the T_{OX} increased from 1.5 nm to 7 nm respectienly.

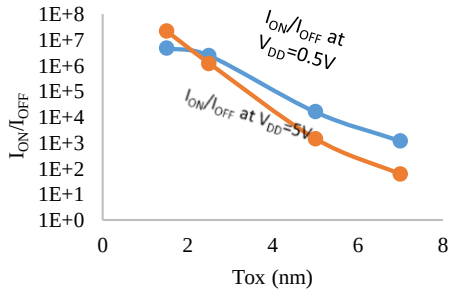

Fig. 9 I_{ON}/I_{OFF} with oxide thickness of Si-FinFET

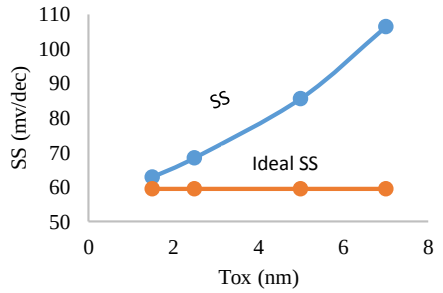

Fig. 10 SS with oxide thickness of Si-FinFET

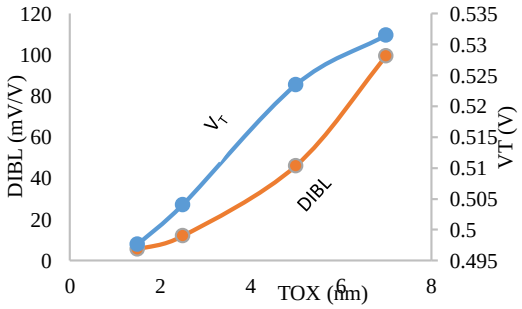

Fig. 11 V_T, DIBL with channel oxide thickness of Si-FinFET

3.4 Dimensions Scaling Factor (K) Characteristics

The scaling down of channel dimensions and its effect on the characteristics of Si FinFET has been simulate using the same voltage range in all other simulations. The length, width and thickness will be scale-down by a factor (K). While K = 0.25 represent the minimal dimensions value, and K=1 represents the original value. Table 2 represent the dimensions of Si-FinFET and its K value. Table 2 shows the parameters that used with condition scaling factor K.

Table 2 The parameter used with condition scaling factor K

K	L (nm)	W (nm)	T_{OX} (nm)
0.25	5	2.5	0.625
0.5	10	5	1.5
0.75	20	10	3
1.00	40	20	6

Fig. 12 shows the I_{ON}/I_{OFF} ratio with the scaling factor K from 0.25 to1, the highest value of I_{ON}/I_{OFF} (more than 10^8) happen at scaling factor K = 0.75 at V_{DD} = 5 V, and for V_{DD}=0.5 V, the maximum value for I_{ON}/I_{OFF} (more than10^7) also happen at K= 0.7. For K more the 0.75 the I_{ON}/I_{OFF} decreased significantly.

Fig. 13 presents the scaling factor K characteristics of subthreshold swing (SS) for Si FinFET, this figure illustrates that the furthest SS from the ideal SS (59.5 mV/dec) with 85.6 mV/dec happen at K=1. At K = 0.25 the nearest value to the ideal SS (62.2 mV/dec) were happen. So, with increase K, SS increased significantly.

Fig. 14 presents the scaling factor K characteristics of threshold voltage (V_T), and drain-induced barrier lowering (DIBL) of the Si FinFET where V_T = 0.74 V (the higher value) happen at K = 0.5, and V_T = 0.49 V at the lowest value at K = 1. Finally, the DIBL the value ranges from 45 to 50 mV/V until it reached 49.99 mV/V at K=0.25.

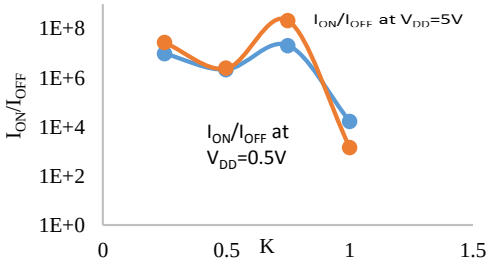

Fig. 12 I_{ON}/I_{OFF} with scaling factor (K) of Si-FinFET

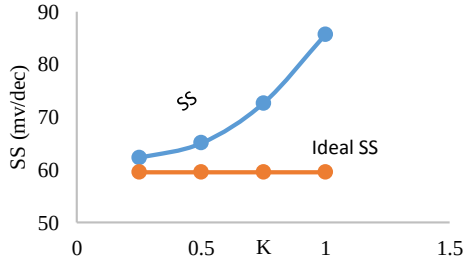

Fig. 13 SS with scaling factor (K) of Si-FinFET

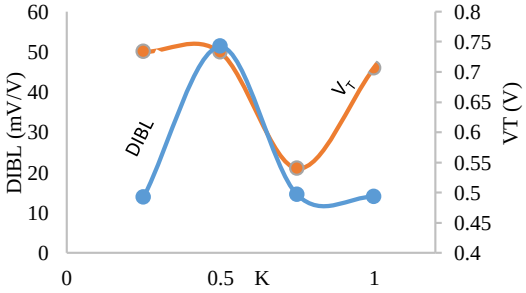

Fig. 14 V_T and DIBL with scaling factor (K) of Si-FinFET

4. Conclusion

The effects of channel dimensions (length, width, and oxide thickness) on electric characteristics of Si-FinFET are studied, the MuGFET have been used as a simulation tool. Highest I_{ON}/I_{OFF} ratio and nearest SS to the ideal value were used as parameters to evaluate the best dimensions of Si-FinFET. Depending on results, the higher L (=40 nm), the lower W (=5 nm), and the lower T_{OX} (=1.5) nm, are the optimal dimensions for Si-FinFET. For scaling factor (K), the optimal value of was at K=0.25, at this value K represent the lower dimensions of transistor.

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