Temperature Sensitivity of Silicon Nanowire Transistor Based on Channel Length

Hani Taha AlAriqi [1], Waheb A. Jabbar[1,*], Yasir Hashim[2], and Hadi Bin Manap[1]

[1]*Faculty of Engineering Technology, Universiti Malaysia Pahang, 26300 Gambang, Kuantan, Pahang, Malaysia*
[2]*Computer Engineering Department, Faculty of Engineering, Ishik University, Erbil-Kurdistan, Iraq*

*waheb@ieee.org

***Abstract*— This paper investigates the temperature sensitivity of Silicon Nanowire Transistor (SiNWT) depends on the gate length, and also presents the possibility of using it as a Nano- temperature sensor. The MuGFET simulation tool was used to investigate temperature characteristics of the nanowire. Current-voltage characteristics with different values of temperature and with different length of the Nano wire gate (L_g = 25, 45, 65, 85 and 105 nm), were simulated. MOS diode mode connection suggested to measure the temperature sensitivity of SiNWT. The final results show that the best temperature sensitivity of SiNWT based in largest ΔI occurred at working voltage V_{DD} range 1 V to 3.5 V, depends on channel length range 25 nm to 85 nm and beyond the temperature sensitivity will be constant even the channel length increased up to 105 nm.**

Keywords— SiNWT; temperature sensitivity, channel length

I. INTRODUCTION

Due to the scaling of the complementary metal-oxide-silicon (CMOS) did not track the constant-field scaling principle accurately because of non-scaling factors- the threshold voltage of the metal oxide semiconductor field effect transistor (MOSFET)'s Vth- designers are looking for creating more sophisticated integrated circuits via using more transistors per chip. This limitation caused device the dereliction by high-field effects. More than the latest roughly 4 decades, experts and researchers had increased the intricacy of integrated circuits IC's thru further five orders of stages [1, 2]. That incredible reaching has changed the world. The downsizing of transistors to the nm region means to find out and investigating in the field of nanoscale materials and nanoscience as well. The nanometer has been as significant to science as the micrometer was in the previous century [3].

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) approaches its down-scaling limits, many new FET structures are being extensively explored. One of these FETs was the Si-Nanowire FET (SiNWFET) (Fig. 1). This transistor structure has attracted wide attention from researchers in academic and in semiconductor industry fields as well [4-6].

The remaining part of this paper is organized as follows: The next section presents an overview about Nanowire technology. Section III introduces adopted methods of this research. The results and discussions are presented in Section IV. Finally, paper is concluded in Section V.

II. THE NANOWIRE TECHNOLOGY

A nanowire is an extremely thin wire identical material or configuration with a length on a demand of some nanometer s (nm) or more less.it is also a nanostructure, with the span of the demand of a nanometer (10^{-9} meters). Then again, nanowires can be defined as tool that have a thickness or diameter controlled to tens of nanometers or less and an unconfined length. Numerous diverse types of nanowires exist, including metallic such as Ni, Pt, Au, etc., semiconducting such as Si, InP, GaN, etc., and insulating like SiO2, T iO2. The nanowires could be used in the near future to link ever tinier components into very small circuits. Using nanotechnology, such constituents led to create out of chemical combinations [7, 8].

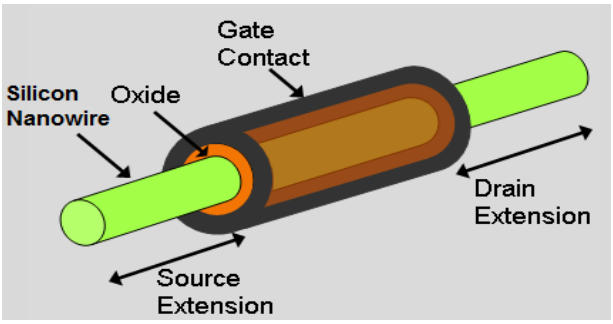

Fig. 1. SiNWT structure

Apparently, the subsumed electronics applications - that is, for use within equipment- are the best example for using the semiconductor temperature sensor [9]. The transistor based temperature sensors are designed depending on the temperature characteristics of current-voltage curves of the Nanowire transistor [10-13]. The bipolar transistor can be used as a temperature sensor by connecting the base and collector together. This will use a transistor in diode mode. While the transistor in MOSFET structures can be used as a temperature sensor by connecting the gate with either source or drain (Fig. 2). Electronic devices in Nano dimension like diodes, transistors, capacitors and resistors appealing,

particularly the attention to the electronics industry due to the drive for ever-smaller electronic circuits.

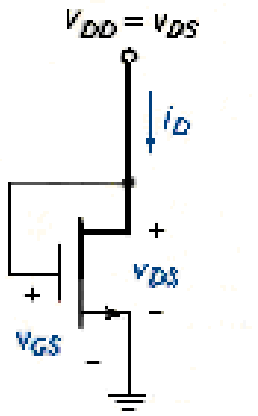

Fig. 2. MOSFET as a temperature sensor (Vg = Vd = V_{DD})

The performance of these new devices, with a wide array of the additional applications, will depend on the characteristics of these devices in Nano-dimensions. A new more powerful electronics device's chips generation with ultra-small transistors could be more trustable in the future after more finds and detection too, by researchers for these tiny structures. The designing of Field Effect Transistors in Nano dimensions with new structures is still a technology understudying and improving as well as that requires further innovations before the challenging state of the MOSFETs Science.

III. Research Methodology

Simulation tools of electronic devices have become increasingly important to understand the physics behind the structures of new devices [8]. Simulation tools can also help identify device strengths, weaknesses, and retrenchment costs and illustrate the extensibility of these devices in the nm range. Consequently, MuGFET simulator is utilized in this research for the analysis and performance evaluation of GaAs-FinFET structure's dimensions. Experimental work can be supported by simulation tools to further explore the development of MuGFET for Nano-dimensional characterization. MuGFET is used to investigate the characteristics of the FinFET transistor. The output characteristic curves of the transistor under different conditions and with different parameters are considered.

Simulation tool (MuGFET) can choose either PADRE or PROPHET simulate and both simulates are developed in Bell Laboratories. PROPHET is a partial differential equation profiler for 1, 2, or 3 dimensions. PADRE is a device-oriented simulator for 2D or 3D device with arbitrary geometry [8]. This software provides many useful characteristic curves for FETs for engineers and for deeply understanding Physics. The MuGFET simulation tool also provides self-consistent solutions to the Poisson and drift-diffusion equation [8]. MuGFET is used to simulate the motion of transport objects in the calculation of the characteristics for Nanowire [14].

IV. Results and Discussion

Firstly, the Id-Vg characteristics of Nanowire at a temperature (250, 275, 300, 325, 350, 375, 400, 425 and 450 K°) were simulated with the following parameters Channel width = 30 nm, Channel concentration (P-type) = 10^{16} cm^{-3}, Source and Drain lengths = 50 nm, Source and Drain concentration (N-type) = 10^{19} cm^{-3}, and Oxide thickness = 2.5 nm. The gate length values will be (L_g = 25, 45, 65, 85 and 105 nm).

Table I. Simulation Parameters

Parameters	value
Channel length (L)	(5, 10, 15, 20, 25, 30, 35, 40 and 45) nm
Channel diameter (D)	5 nm
Oxide thickness (T_{OX})	2.5 nm
channel concentration p -type	10^{16} cm^{-3}
channel concentration N -type	10^{19} cm^{-3}

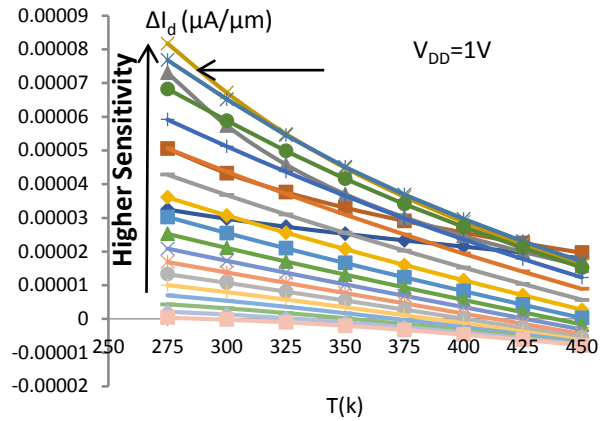

Fig. 3. ΔId-Temperature characteristics of SiNWT at Lg = 25 nm

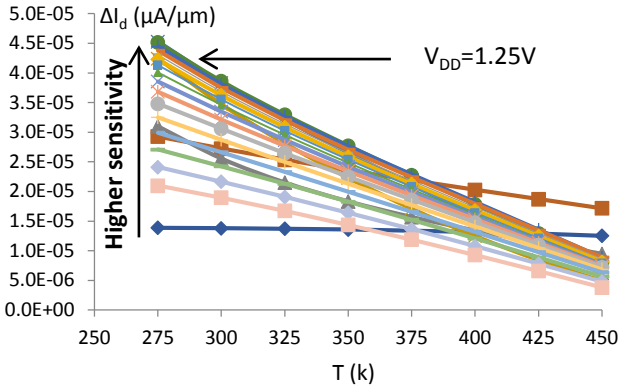

Fig. 4. ΔId-Temperature characteristics of SiNWT at Lg = 45 nm

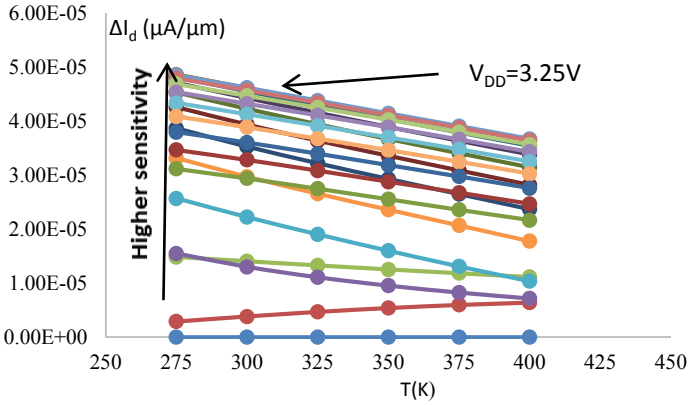

Fig. 5. ΔI_d-Temperature characteristics of SiNWT at Lg = 65 nm

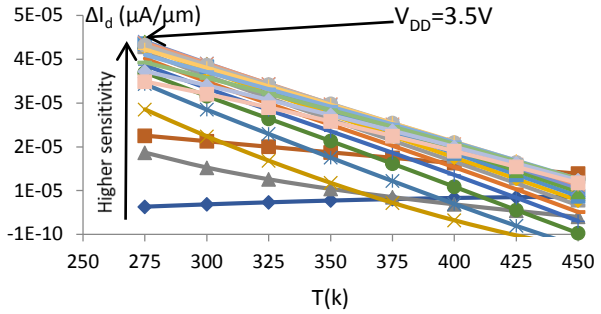

Fig. 6. ΔI_d-Temperature characteristics of SiNWT at Lg = 85 nm

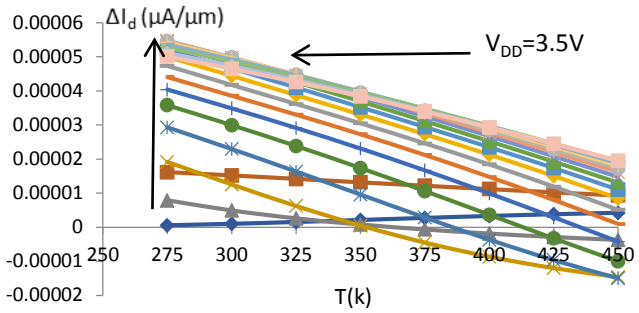

Fig. 7. ΔI_d-Temperature characteristics of SiNWT at Lg = 105 nm

Figures 8, 9, 10, 11 and 12 show the change of ΔI with increasing V_{DD} at (T = 250, 275, 300, 325, 350, 375, 400, 425 and 450 K°) at L_g = 25, 45, 65, 85, and 105 nm respectively, these figures illustrate that the maximum sensitivity (max ΔI) done at V_{DD} = 1 V for L_g = 25 nm, V_{DD} = 1.5 V for L_g = 45 nm, V_{DD} = 3.25 V for L_g = 65 nm, V_{DD} = 3.5 V for L_g = 85 nm, and finally V_{DD} = 3.5 V for L_g = 105 nm.

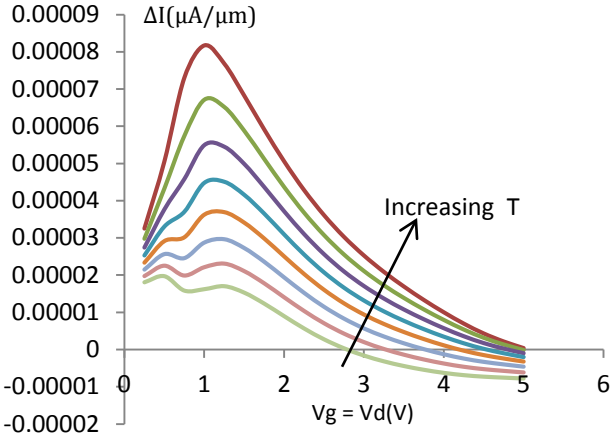

Fig. 8. ΔI_d-V_{DD} characteristics of SiNWT at Lg = 25 nm

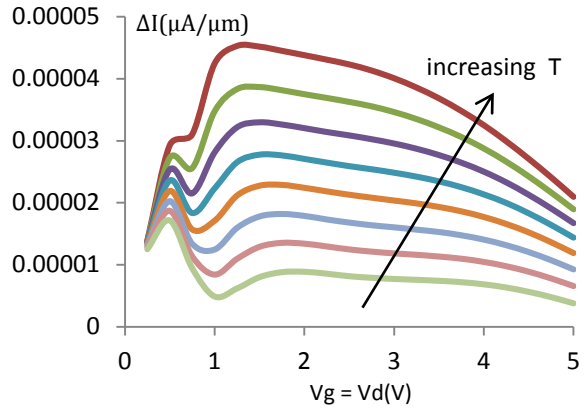

Fig. 9. ΔI_d-V_{DD} characteristics of SiNWT at Lg = 45 nm

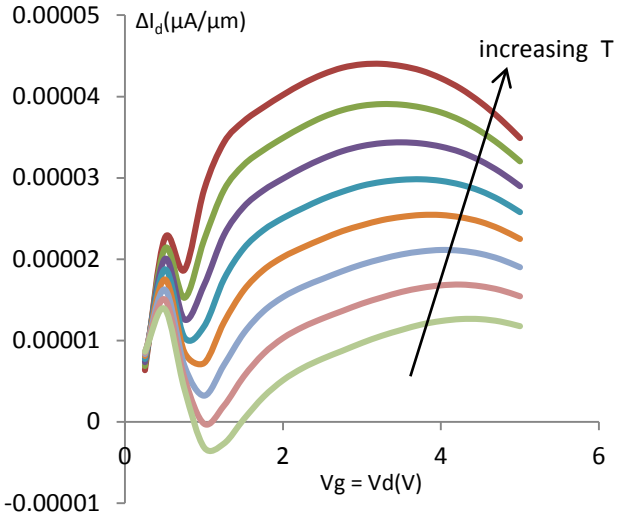

Fig. 10. ΔI_d-V_{DD} characteristics of SiNWT at Lg = 65 nm

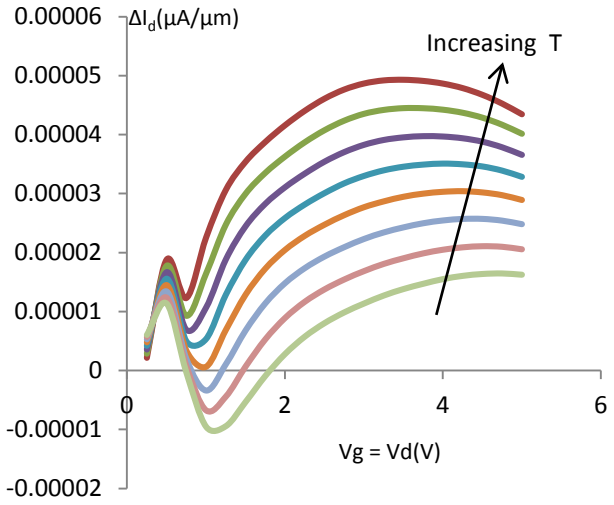

Fig. 11. ΔI_d-V_{DD} characteristics of SiNWT at Lg = 85 nm

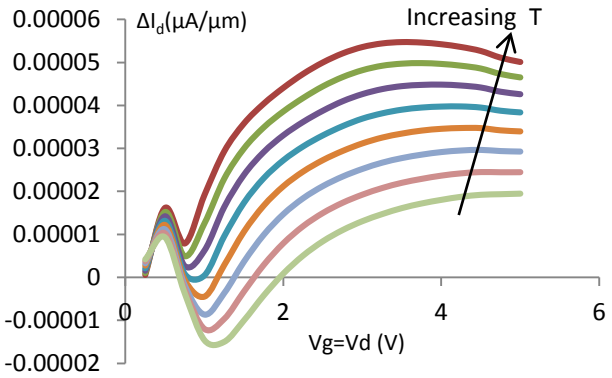

Fig. 12. ΔI_d-V_{DD} characteristics of SiNWT at Lg = 105 nm

Figure 13 shows the optimized operating voltage V_{DD} based on best temperature sensitivity with channel length, this optimized operating voltage V_{DD} related with the peaks of temperature sensitivity in Figures 8 to 12. So the temperature sensitivity will increase remarkably until 65 nm length of the channel, then increased slightly in-between 65 nm and 85 nm length of the channel and finally it will be stable without increasing with increase channel length beyond 85 nm.

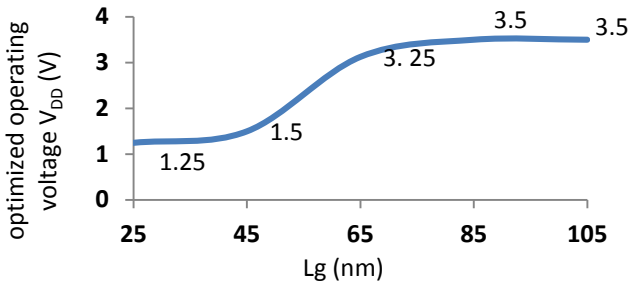

Fig. 13. Optimized operating voltage V_{DD} with channel length based on best temperature sensitivity

V. CONCLUSION

The effects of changing L_g on SiNWT temperature characteristics were investigated. The obtained results show that with diode mode transistor connection, the best increments –sensitivity- in current (ΔI_d) with temperature occur between 25 nm to 85 nm channel length range, and beyond will be stable without any effect by increasing L_g. In the future, more simulations will be carried out to consider the other parameters (such as channel diameter and oxide thickness) and characterize the SiNWT based on temperature sensitivity and stability.

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