Low-Power RFID System Using Analog Circuit Techniques Based on Passive Sensor

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***Abstract*—In this paper, this research introduces low-power radio frequency identification (RFID) using analog circuit techniques for passive sensors. As part of Internet of Things (IoT) transformation, RFID is widely used. In the application where power supply is limited, power consumption is always a remarkable criterion as analog circuits and RF are the common power demanding parts in the system. The proposed design for the optimized rectifier circuit, low-power analog to digital converter (ADC)/resistance to digital converter (RDC) circuit and the high efficiency regulator circuit are focused. In the design of energy harvesting rectifier circuit, the use of zero-threshold negative channel metal oxide semiconductor (NMOS)s in 18-stage rectifier circuit is improved. The high efficiency regulator circuit is added to work directly with rectifier circuit. When the energy accumulation in the charge bank that is supplied by rectifier circuit is enough, only then the regulator circuit start to produce constant voltage. To reduce the power usage of the regulator circuit, the regulator circuit avoids the use of amplifiers. In addition, a low-power ADC/RDC circuit is introduced to achieve lower power consumption by conversion scheme and novel sampling. This will minimize the total capacitance that is used by capacitance sensor (CS) array of ADC/RDC circuit by 50%. The RFID system circuit blocks on passive sensor are designed and optimized using analog circuit techniques. The demands for low-power consumption of RFID passive sensor is well examined. The validity of the proposed design is showed by both hardware measurement and simulation results.**

***Index Terms*—RFID system; Analog circuit techniques; passive sensor; IoT; low-power rectifier circuit; high efficiency regulator circuit; ADC/RDC circuit.**

I. INTRODUCTION

RFID is the wireless use of electromagnetic fields to transfer data in the purposes of tracking and automatically identifying tags attached to the objects. RFID tag and reader are the main components in RFID system. Tags have unique identification numbers in each of them and will attached to the objects meanwhile reader in contrast will executes the tag interrogation process to clarify an object by releasing wireless RF signals to interpret the identification (ID) of the equipped tags.

Due to its relatively small in sizes, low price and power consumption in general, RFID widely used in the era of IoT nowadays. RFID tags can be either active or passive. The latter doesn't have internal power supply meanwhile the former supplies its own energy. In passive tag, since not having its own power supply and limited in the first place, low power consumption is constant requirement. For active tag, low power consumption will increase longevity and also decrease in size of battery.

II. RELATED WORK IN LOW-POWER ANALOG CIRCUIT DESIGN

One disadvantage of the active RFID systems is the accurate synchronization requirement between the reader and tags. Tags are put to sleep mode most of the times in this study, in which all circuitry of tags are turned off. One tag is only activated by the reader command in the small fraction of one reading cycle resulting tag is basically inactive for most portion of the time.

Similar studies on power consumption were conducted in [1]-[4]. These studies have used different approaches and equipment. In this paper, we optimize the complexity of RFID system by improving its analog circuit designs.

As mentioned above, RFID system becomes more and more demanding in terms of long operating cycle, size, cost and power especially. Analog circuits such as rectifier circuit, analog to digital converter (ADC)/resistance to digital converter (RDC) and regulator circuits are normally take in most of the power. To address the challenge of the analog circuit high usage of power, different method of circuit designs had been proposed in [5], [6] and [7].

Figure 1 shows the design of low-power RFID system circuit which includes control logic, memory, modulator, demodulator and voltage multiplier (rectifier). Although the design is quite good in reducing the cost of the tag by having no external components needed with the exception of the antenna and also the tag information can be read effortlessly by the integration of memory in the design, the utilization of this RFID tag is limited because there is no sensor integrated in the tag [5]. This problem will make it limited and cannot be used in application of information collection.

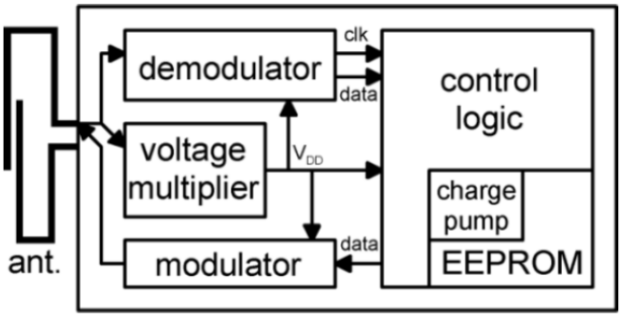

Figure 1: RFID tag proposed in [5]

In [8], voltage regulator of rated 300nA current is proposed. The circuits are capable of using sensor in low-power design in RFID system due to highly improved circuits, these circuits are complex in structures. On top of that, it will make the circuits difficult to stabilize because of the nature of passive RFID sensors.

For the related work for ADC/RDC circuit, Figure 2 shows the proposed tag RFID design taken form [7]. The recovered clock form input wireless signal is acted as counter's reference in order to convert the analog code to the digital code. This process is based on RDC method of converting from analog code to digital code. It has the advantage of more flexibility of the tag if compared to method in [5]. However, RDC cannot be directly be measured the input from the sensors as RDC only capable of measuring the voltage level. To convert input from the sensor to the voltage level, biasing circuit is needed. Unfortunately, integration of biasing circuit in passive RFID tag is complicated due to the limited resolution of RDC that using recovered clock as reference. As was reported in [9], only 5-bits resolution is obtained from the circuit.

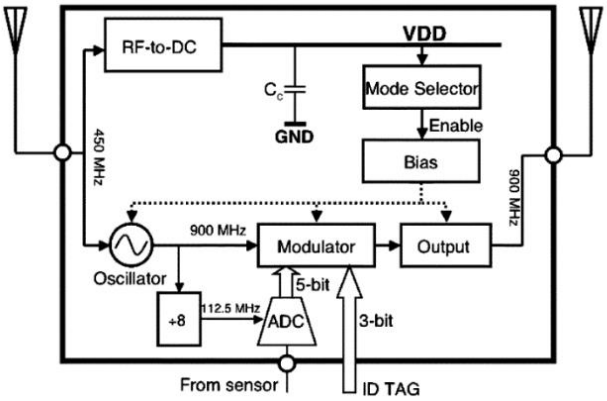

Figure 2: RFID tag proposed in [7]

This creates motivation for research in designing and optimizing low power for the above circuits.

III. Design of Low-Power Analog Circuit for RFID Tag

A. Rectifier Design

RFID circuit can be improved in term of low-power capability by designing the rectifier. RFID can be categorized as passive and active. The difference of passive and active is passive did not need external power supply to be functioned but active need a power supply to be functioned. As passive RFID don't have its own power source, it receives energy from the electromagnetic (EM) field.

Coupling technique indicates that passive RFID can be grouped as two categories which are far-field RFID and near-field RFID. According to Faraday's law, most near-field RFID count on the magnetic field through inductive coupling to the coil in the tag. Small current is induced from the magnetic field around it that is produced by flow of the current through the coil's reader. Limitation for near-filed passive RFID application is due to its operation range that is normally less than 1m only. In compassion to near-field passive RFID, far-field passive RFID usually function in long-range, In the range of 5m to 20m. This is due to it is usually operate in ultra-high frequency (UHF) band in which lies on in between 850 megahertz (MHz) to 960 MHz. Operating at ultra-high frequency gives a far-field passive RFID tag a benefit of smaller antenna. Impedance mismatching between the circuit and the antenna had resulted some of the incident energy of the RFID's tag antenna is reflected back. Backscattering technique is called when the value reflected energy incident can differ according to mismatch on the antenna. Consequently, the cost of assembly and fabrication can be lowered. In addition of using nRF24L01 RF transceiver that already small size and low cost, far-field passive RFID is more acceptable for the proposed RFID system.

To regulate the power input, based on the coupling principle of far field passive RFID, the peak voltage on the antenna of the tag, $v_{\text{s,peak}}$ be represented by [9]:

$$\upsilon_{s.peak} = 2\sqrt{2\boldsymbol{P}_a \boldsymbol{R}_{ANT} \cdot p} \quad (1)$$

Firstly, it shows that $\upsilon_{s.peak}$ is controlled by the available power in which connected to the power sent out by the reader, the distance and the size of the antenna. R_{ANT} is the resistance of the antenna. p is the polarization mismatch. P_a indicates the power obtained by the antenna of RFID tag. Polarization mismatch often is the reason of the limitation of the antenna resistance. The value of the antenna's resistance is normally 50Ω or 75Ω. $\upsilon_{s.peak}$ is very small in value so it cannot be used to give power supply to the other circuits. Type of voltage of $\upsilon_{s.peak}$ as AC voltage also added to the reason of it cannot be used as power supply. In order to give enough power to give power supply to the other circuits, the voltage rectifier is required in passive RFID tag to convert AC voltage to DC voltage.

B. Regulator Design

The proposed regulator circuit is shown in Figure 3. The regulator in the RFID is responsible for the power supply for circuit. The rectifier as the current source acts as an input, I_{in} charging the capacitance tank, C_{tank}. At the top of C_{tank}, V_{DC} acts as the power supply of the regulator circuit. There is little charge stored in the capacitance tank, C_{tank} and V_{DC} is low at the beginning. At the same time, V_B, the voltage across the capacitor C_2, is low and the transistors M_2 and M_3 are off and thus resulting the output of INV_3 is logic "1". This condition will closes switch S_1 in order to charge capacitor C_1 via M_3. V_{DC} will increase slowly when the rectifier start to charge the capacitor tank, C_{tank}. To disconnect the regulator load circuit the source terminal, M_4, switch S_2 is opened. Capacitor C_2 will start to charge and Transistor M_1 and M_2 will to turn on when the value of V_{DC} is increase to the voltage value of two times of V_t, in which where V_t is the threshold voltage.

The proposed regulator design does not need complex circuits such as operation amplifier, loop compensation, voltage reference and unit-gain filter that are used by past designs in [10] and [11]. Consequently, the proposed regulator circuit is very simple and systematic structure. In addition, after the regulator output is enabled, the proposed

circuit has almost zero current dissipation. Even though there are leakage in current before the regulator output is enabled, the amount is irrelevant due to inverters are made up of transistors with very low ratios.

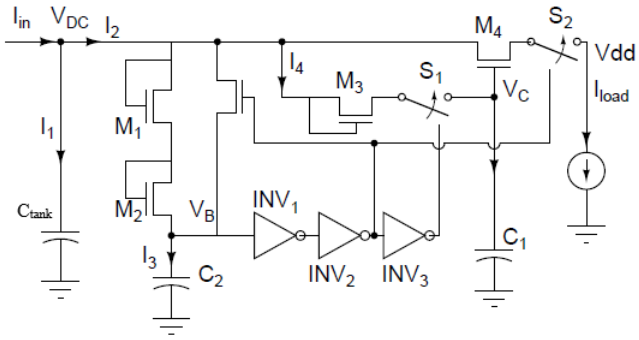

Figure 3: Low-power regulator design

C. Analog to Digital Converter (ADC)/Resistance to Digital Converter (RDC) Design

The single-ended Successive Approximation Register (SAR) Analog to Digital Converter (ADC) is quite important for sensor measurement especially in wireless sensor due to differential signals is difficult for sensor to generate. However, the conventional single-ended SAR ADC require all of the capacitor array to sample the voltage. So, strong energy is needed to power the capacitor array thus will consume high power in general.

Figure 4 shows the block diagram of the traditional SAR ADC. It has SAR logic, comparator, and capacitor array. The figure also indicates that C_P is the parasitic capacitance of the top plate of the capacitor array and V_{CM} is the ground signal level.

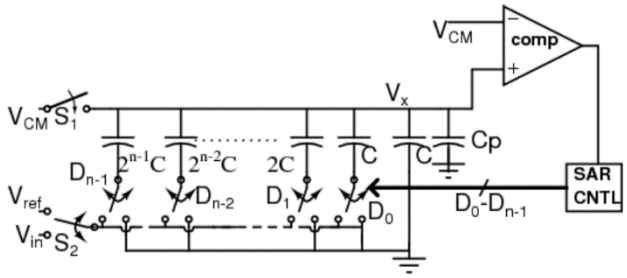

Figure 4: Block diagram of the traditional SAR ADC circuit

Switch $S_1$is closed meanwhile switch $S_2$is connected to V_{in}in which acts as ADC input voltage. As mentioned before, all of the capacitor arrays are used to sample the input voltage.

Initially in the conversion phase, the switches from D_{n-1} to D_0 are connected to the ground terminals. The Switch S_1 is open meanwhile switch S_2 is connected to the reference voltage, V_{ref}. The switching process from D_{n-1} to V_{ref} indicates the beginning of the conversion cycle. After that, the voltage at the top the top of capacitor plate, V_X will becomes to V_{CM} + 0.5·V_{ref}-V_{in}. The switch D_{n-1} stays connected to V_{ref} if and only if all the n-1 conversion cycle is done and the comparator output is 0. At the end of the conversion phase, the total capacitance, C_{eq} connected to V_{ref} is:

$$C_{eq} = D_{out} \cdot C \tag{2}$$

where: C_{eq} = Total capacitance
D_{out} = Digital output code of ADC

In the meantime, take into account that by disregard the difference less than V_{LSB} of the ADC, V_{CM} is the same value as V_X. So, we can conclude:

$$(V_{CM} - V_{in}) \cdot C_{total} + V_{CM} \cdot C_P = (V_X - V_{ref}) \cdot C_{eq} + V_X \cdot (C_{total} - C_{eq} + C_P) \tag{3}$$

Where C_{total} is the total capacitance of the capacitor array and substitute its value by $2^n \cdot C$. Similarly, both $C_{eq} = D_{out}$ and $V_X = V_{CM}$ is substituted respectively into equation in (3), we get:

$$D_{out} = 2^n \frac{V_{in}}{V_{ref}} \tag{4}$$

The equation demonstrates that the parasitic capacitance C_P is not a factor in the conversion accuracy of the traditional SAR ADC. Moreover, it also indicates that ADC output is the perfect representation of the analog input.

The proposed method of ADC circuit design is to minimize the effect of parasitic capacitance, C_P. During sampling phase, the intention is to charge C_P to the ADC input level. This is basis of the proposed method. As mentioned beforehand, V_{in} is estimated to the voltage of the top plate of CS capacitors at the end of the conversion cycle phase. Consequently, both charge stored and the voltage in C_P are remained at a constant value as well as its effect is reduced.

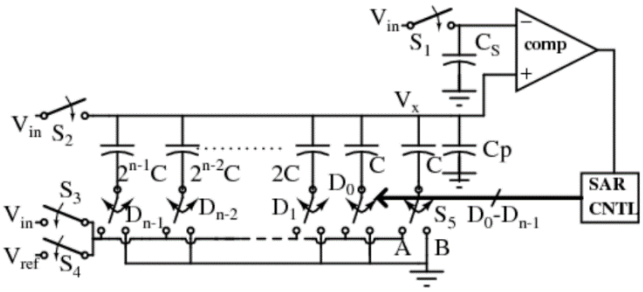

Figure 5: Block diagram of the proposed SAR ADC circuit

In Figure 5, the propose circuit is shown. Comparison between the propose circuit and SAR ADC circuit clearly with added of three switches, S_3, S_4, and S_5 respectively. The switches S_1, S_2, and S_3 are closed meanwhile S_5 acts as connector to ADC input V_{in}(sampled by C_S) to the bottom plate of the capacitor. ADC input V_{in} at the same time is also charged by C_P. It is important to mention that the rest of the scaling capacitors C, C, 2C, $2^{n-2}C$, and $2^{n-1}C$ are uncharged due to their terminals are connected to the V_{in}. The switches S_1, S_2, and S_3 are open; switch S_4 is closed during the conversion phase. During the same phase, last switch S_5 is moved to node B in which directly connected to the ground. From that point on, all the normal charge scaling process are accomplished to produce ADC digital outputs.

Same to previous remarks, we use V_{ref} as indication to the capacitance tied to C_{eq} at the end of conversion cycle phase. Therefore, we get:

$$V_{in} \cdot C_P = (V_X - V_{ref}) \cdot C_{eq} + V_X \cdot (C_{total} - C_{eq} + C_P) \quad (5)$$

Substituting $V_X = V_{in}$, $C_{total} = 2^n C$, and $C_{eq} = D_{out} \cdot C$ respectively into the above equation, we obtain:

$$D_{out} = 2^n \frac{V_{in}}{V_{ref}} \quad (6)$$

Based on a constant C_P, the similarity of the equation of (4) and (6) clearly show that C_P is not a factor in proposed circuit's ADC conversion results. Across the capacitor, the capacitor's value differs with the voltage. It also proven that the proposed circuit method can minimize the effect of parasitic capacitance, C_P.

IV. Experiment Results

The 0.13µm CMOS technology is implemented in the proposed regulator and RDC circuit. Table 1 shows the capacitors and transistors sizes. The optimized rectifier is shown in Figure 6 is for powering the analog circuits. The layout of the design is shown in Figure 7. The transistors with zero threshold devices are proposed in the design. The importance of the simulated regulator and rectifier outputs is shown in Figure 8.

Table 1
List of devices parameters in the proposed rectifier

Number of stages (N)	18
Transistor sizes	25µm for W and 420nm for L
Capacitance of $C_L$and C_C	500fF

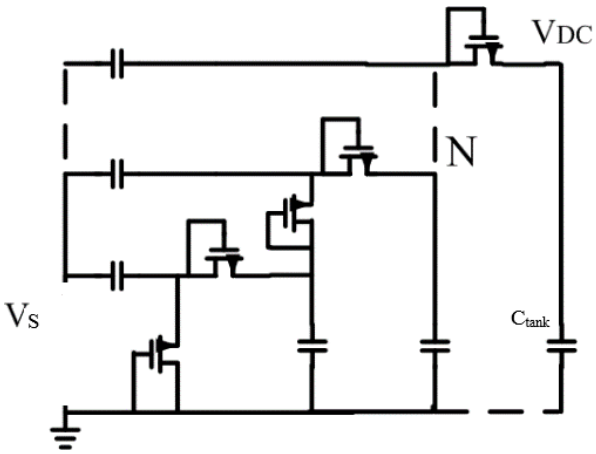

Figure 6: Optimized rectifier

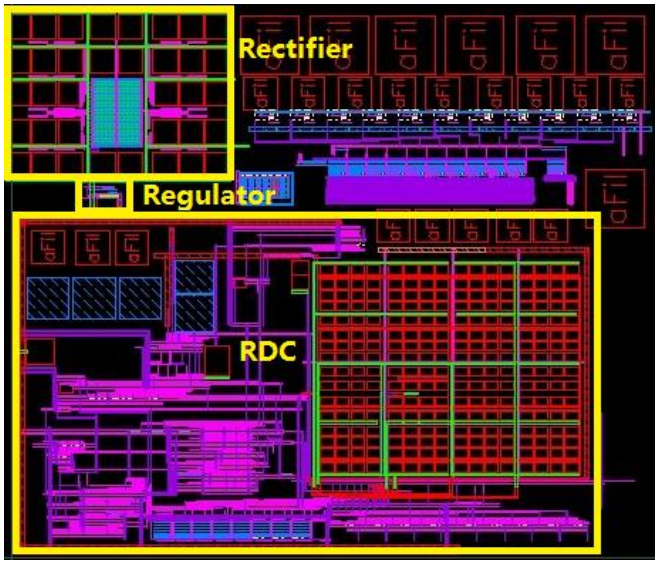

Figure 7: The layout of proposed analog circuit

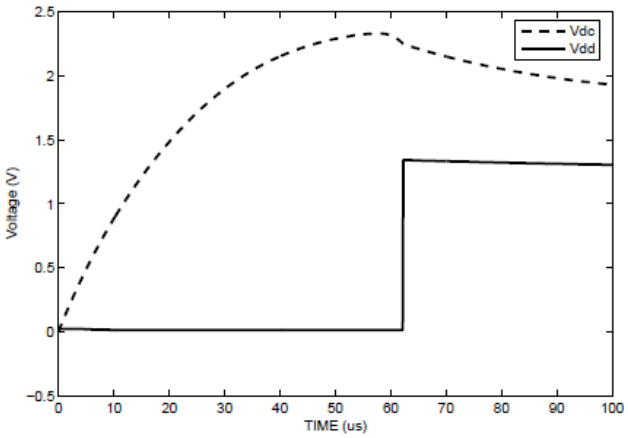

Figure 8: Simulation of the regulator and rectifier output

The rectifier operates with 900MHz RF signals and have of 18 stages altogether. When the input RF signal value is 200mV, subsequently the rectifier circuit is around 10% efficiency in the capacitor-tank charging period in which is related and same value to a Shottky diode in [12].

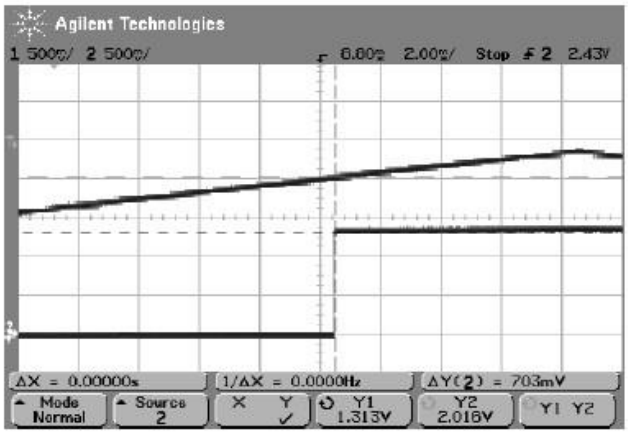

Figure 9: Temporary measurement of V_{dd} vs. V_{DC}.

The regulator circuit's measurement is shown in Figure 9 – 11. In Figure 9 shown that the regulator begins to supply a constant 1.31 V of voltage (V_{dd}) the capacitor tank is charged

with 2.02 V of V_{DC}. The overall constant value is the load current with 20 µA. The graph also suggested that as long as V_{dd}<V_{DC}, the output voltage is generated in constant. Figure 10 shown that V_{dd} will reduce to 63 mV when V_{DC} is dropped to 532 mV.

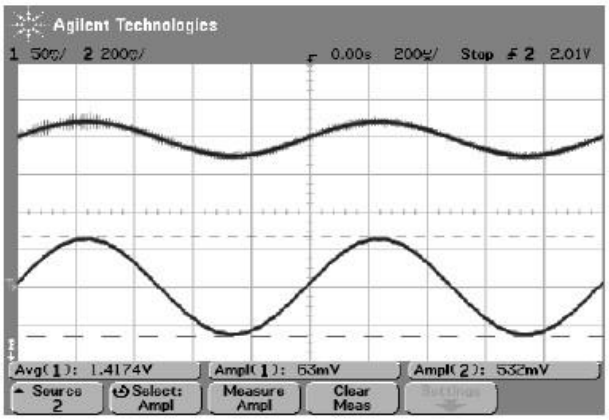

Figure 10: Regulator measurement of V_{dd} vs. V_{DC}

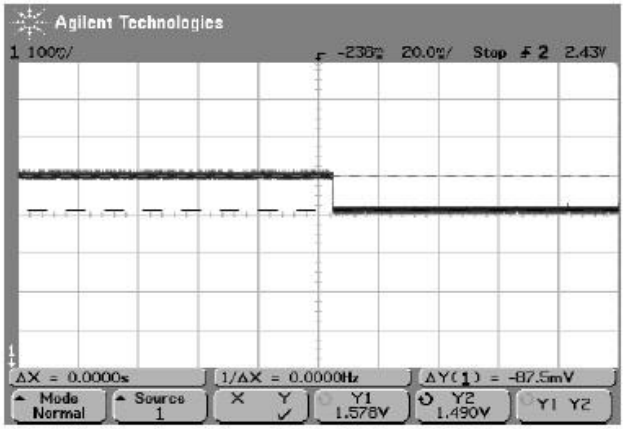

Figure 11: Regulator measurement of V_{dd} vs. l_{load}

Figure 11 indicates that the reduce of V_{dd} is approximately 87.5 mV when the load current increases from 10µA to 100 µA. In Table 2, the parameters of the proposed regulator are summarized.

Table 2
The parameters in the proposed regulator

Input Range	1.1-2.4V
Input regulation (V_{dd}/V_{DC})	11.7%
Efficiency of current	100%
Load regulation (l_{load}/V_{DC})	971Ω
DC current	0
Loop compensation	None
Voltage reference	None

To make simulation for ADC circuit, both circuit voltage reference, V_{ref} and power supply are at 1.2V. The sampling rate is 20MS/s due to the ADC clock frequency is at 200 Mhz. If each of ADC output happens to be eight times during the simulation period of 102.4 µs, the slope of the signal will at 0.0117 V/µs for the ADC to be considered as ideal. The ADC gain errors and output slopes are summarized in Table 3.

Table 3
The gain errors and output slopes comparison between traditional SAR ADC and proposed design

		Traditional SAR ADC	Proposed Design
Gain Error	Derivation from ideal slope	0	0
	V_{LSB}	0	0
Input range (V)		0-1.1	0.1.1
Total load capacitance (pF)		1.83	0.76
ADC output slope		1	1

V. Conclusion and Future Work

In conclusion, the proposed low-power analog design techniques for rectifier circuit, regulator circuit and ADC/RDC circuit are presented for RFID passive sensor. These circuit techniques are not only suitable for the targeted RFID passive sensor system but also can be used in the design of other wireless devices. Furthermore, these circuits are important blocks in wireless sensor circuits. For the design of rectifier circuit, by using zero-threshold NMOSs, an 18 stage rectifier circuit is used. To further up optimizes the rectifier circuit, an efficient regulator circuit is designed. Constant voltage is provided by the regulator only and only if there is sufficient energy collected in the charge tank that is fed by the rectifier circuit. Besides, the regulator circuit also did not use the traditional close-loop method to optimize the power consumption. The low-power ADC/RDC circuit is designed to improve the system even more. It achieved its low-power criteria by conversion scheme and novel sampling thus minimizes the total capacitance used by the CS arrays by 50%. The implemented circuits are verified and observed through multiple simulations and experiments.
Hardware measurement indicates the validity of the proposed techniques. Further research is can be achieved based on the research finding of the study. Hardware optimization is always an option to tackle the next challenges since the new invention is produced regardless.

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