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Enhancement of cascaded multi-level VSC STATCOM performance using ANN in the presence of faults

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ABSTRACT

A system can be disturbed in terms of stability when connected to a number of loads at the distribution ends or when subjected to faults. To reverse such systems to a stable state, FACTS devices such as static synchronous compensator (STATCOM) are used. In this paper, a cascaded multi-level voltage source converter (VSC) STATCOM was designed and implemented with a novel space vector pulse width modulation (SVPWM) scheme. Artificial neural network (ANN) controller was used instead of instead of Proportional-Integral (PI) controller in the proposed scheme to improve the response time (RT) and performance of STATCOM in terms of power factor (PF) and voltage amplitude during periods of voltage sag. During the implementation, two fault sources (single-line-to-ground (SLG) and line-to-line (LL) faults) were used to create voltage sag. STATCOM was subjected to performance evaluation in the presence of these disturbances via MATLAB simulation in IEEE 3-bus system. The outcome of the simulation studies showed the ANN controller to perform better than PI as it was able to rapidly recover voltage value (<1 cycle) with unity PF.

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1. INTRODUCTION

As a non linear system, the power system consists of different types of machines that represent the loads [1-3]. The voltage stability of a power system is affected whenever the system is dominated by faults and when such instability is prolonged, there could be damages to the machines connected to the system. Therefore, the system needs to be restored to its initial state within a short time. With the rapid increase in power electronics deployment, there is a need for power networks improvement using FACTS controllers. STATCOM is among the FACTS devices used in distribution networks for power factor and voltage regulation [4]. A STATCOM is to be cost-effective and capable of reacting rapidly to load changes as it has VSC as one of its major components. Owing to the possibility of multi-level VSC, it has been widely used as an alternative to transformers [5-7]. The 3 common topologies approved for multi-level VSC-based STATCOM are cascaded topology, flying capacitor topology, anddiode clamped topology and among these topologies, more attention has been given to cascaded H-bridge inverter because it is easy to control, has modularity, and requires less number of component [4, 8].

A STATCOM has its control algorithm as the most vital component as it is involved in dynamic reactive power control. The best compensation effect can be obtained by proper control of the STATCOM [9-11]. Conventionally, a STATCOM is controlled by a PI controller; several works exist on the control of STSTCOM using PI controllers. In [12, 13], problems of power quality such as voltage sag and THD were addressed using SPWM and PI controller-based STATCOM model. In another work, an AC and DC side mathematical model of a three-phase AC-DC VSC was derived and dq-axis current and DC voltage control were carried out with a PI controller [14]. A PI controller design for a STATCOM was given by [15, 16] for improvement of PF and voltage fluctuation. In these studies, the parameters of PI controller were tuned using the mathematical model, meaning that the structure of PI is fixed. Thus, the best possible performance from a STATCOM might not be obtained from designed controllers for different operating points [17, 18]. This raises a need for the development of new controllers with more improved performance. In the recent years, ANN techniques have been significantly useful in power electronics for the maintenance of the stability of converter systems over a wide range of operation. ANN-based controllers also provide fast dynamic response and their control requires no mathematical model of the system.

Several studies have proposed the application of ANN-based control of STATCOM in power system distribution [17-20]. Most of the literatures have used sinusoidal PWM (SPWM) technique to control VSC switches. SPWM is seen as a matured technique that yields low PF compared to the SVPWM technique. Although these studies were related to the voltage regulation during fault or increasing loads, no simulation studies was presented to demonstrate the performance and RT of cascaded 3-level VSC STATCOM in consideration of PF amplitude and voltage magnitude during periods of voltage sag.

This study aims at the design and simulation of ANN-based cascaded three-level VSC STATCOM by employing the SVPWM technique based on modulation index control strategy for mitigating the effects of sag problem in distribution networks. This combination was aimed at achieving rapid PF and voltage regulation.

2. STATIC SYNCHRONOUS COMPENSATOR (STATCOM)

2.1. Configuration and fundamental concept

As a shunt-connected compensator device, STATCOM is connected in parallel (through interfacing inductor Lf) at the bus 3 or point of common coupling (PCC). At the fundamental frequency, it produces 3-phase balanced voltage sets with controllable phase angle and magnitude [13]. Figure 1 depicts the proposed STATCOM system, consisting of the interfacing inductor represented as L filter, cascaded 3-level VSC (IGBT devices) with Vdc on each unit, and control strategy (SVPWM technique and control circuit). The main part of the STATCOM device is the VSC that transforms the dc input into a 3-phase output voltage. The reactive power created due to the voltage difference across the Lfis exchanged between the STATCOM and the voltage at bus 3.

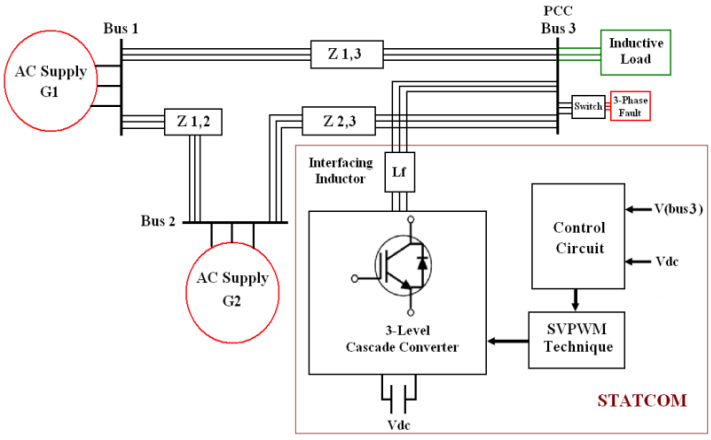


Figure 1. STATCOM configuration connected to IEEE 3-bus system

The STATCOM proposed in this study was implemented on a 6.6 kV distribution network with the aim of achieving voltage regulation with steady PF when there is voltage fluctuation (increase or decrease in

voltage) at the bus 3. This was realized via a continuous variation of the STSTCOM-generated reactive power in both capacitive and inductive operation modes. The exchange of power between STATCOM and the system is governed by (1) and (2). In (1), the value of P is normally positive as it only accounts for the losses by making a minimal steady-state shift (as α =1). This shift allows active exchange of power to the STATCOM to sustain losses-related voltage decreases across the capacitors[21].

$$p = \frac{V_1 * V_2}{X_{Lf}} \alpha \quad (1)$$

$$Q = \frac{V_1}{X_{Lf}} (V_1 - V_2) \quad (2)$$

Where, V1: Voltage of bus 3, V2: VSC output voltage, XLf: interfacing reactance, and α: angle between V1 and V2.

2.2 Cascaded multilevel VSC

Multilevel VSC is advantageous as it allows the use of low-rated switches to generate high voltage [22], thereby eliminating the need for step-up transformers and consequently reducing the weight, inverter cost, and size [23]. Theoretically, the number of levels for multi-level VSC is infinite, but in practice, it is subject to the complexity of the circuit. To be considered multi-level, the minimum number of levels for multilevel VSC must be 3, i.e. +V, 0, and -V.

Several studies have proposed different multilevel STATCOM topologies but the commonly used are diode clamped, H-bridge cascaded, and capacitor clamped inverters and each of these topologies is associated with certain advantages and challenges. For instance, cascaded multilevel VSC is controlled by the number of dc inputs that is later generated at the output to form a staircase-like waveform. Increases in the levels of utilized dc levels increases the output power as more steps will be required to synthesize the output waveforms. If Nm denotes the number of H-bridge units, the level of the phase-to-ground output voltage will be described by 2Nm +1, whereas 4Nm +1 will be the level of the phase-to-phase output voltage[23]. Figure 2 presents 3- phase cascaded 3-level cascaded VSC STATCOM which consists of one H-bridge units in each phase (No. of H-bridge= (No. of level -1)/2) for yielding 5 level phase-to-phase output voltage. The L-filter is used to provide current harmonic attenuation solution in a simple way and hence, considered a first-order filter. To design it, (3) was used.

$$L_f = \frac{1}{8} \times \frac{V_{dc}}{f_{sw} \times \Delta I_{Lmax}} \quad (3)$$

Where f_{sw}= the switching frequency, ΔI_{Lmax}= the maximum rated load current I_{Lmax} peak ripple which is 5 to 20% of the rated current supply of the grid network.

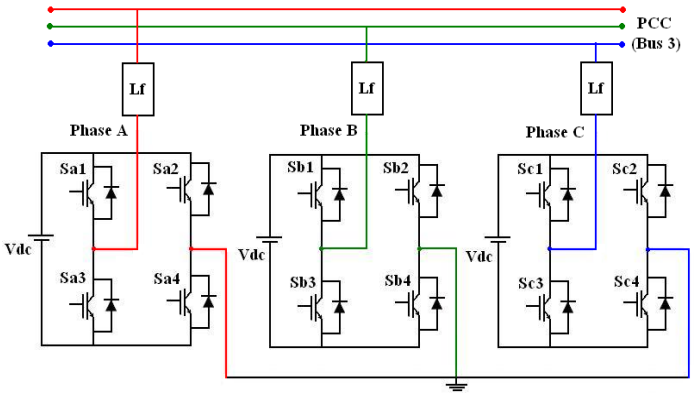


Figure 2. Cascaded H-bridge three-level VSC

2.3 SVPWM technique signal

Many approaches have been proposed for driving a VSC topology using SVPWM. The traditional SVPWM implementation generally involves switching time calculation, voltage space vector estimation, sector identification, and optimal switching time estimation for each sector. Regarding the identification of

sectors, it can be achieved done via the calculation of the sector angle via coordinate transformation by deploying Clarke's transformation. A lookup table is needed to determine the switching sequence for the inverter legs. In this paper, the adopted approach is to device a simple way of SVPWM implementation and the employed technique is wholly reliant on the instantaneous amplitude of the reference phase voltage of all the phases. These reference voltages are expressed in space vectors[24]. By comparing these space vectors with PWM signal (triangular carrier), the appropriate pulses of SVPWM will be generated for each inverter leg in each phase. The SVPWM technique is represented in the block diagram shown in Figure 3.

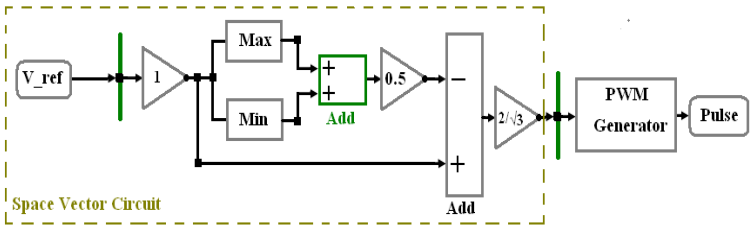


Figure 3. SVPWM technique circuit diagram

The addition of a common mode voltage V_{offset} to V_{ref} generates the maximum obtainable peak amplitude of the phase voltage in linear modulation that reflected the output of space vector circuit. (4) is used to derive the magnitude of V_{offset}[25]:

$$V_{offset} = -(V_{max} + V_{min})/2 \quad (4)$$

Where, V_{max} and V_{min} are the maximum and minimum magnitude of the 3considered reference phase voltages, respectively. The introduction of V_{offset} causes the centering of active inverter switching vectors in a sampling interval; this makes SPWM technique comparable to SVPWM [26]. In (4), the triangular carrier is first crossed by the reference phase with the least magnitude (called the minimum-phase) to cause the first inverter switching state transition, while the reference phase with the highest magnitude (called the maximum-phase) made the last crossing to elicit the last switching transition [27]. Thus, it is possible that the active vectors switching periods can be determined from the amplitudes of the sampled reference phase voltages (maximum-phase and minimum-phase) [28]. The SVPWM technique is a simple approach that determines the time instants of the 3 reference phases crossing the triangular carriers based only on the amplitudes of the instantaneous reference phases. Sorting these time instants will reveal the V_{offset} introduced to the reference phase voltages that elicited the space vector generation for the overall linear modulation range such that there will be centering of the middle inverter switching vectors during sampling as obtainable in the traditional SPWM scheme[29]. The following steps are involved in SVPWM implementation for VSC scheme using the amplitudes of the instantaneous reference phase:

a) Calculation of the equivalent time of the sampled amplitudes of V_{an}, V_{bn}, and V_{cn} for the current sampling interval, where T_S represents the sampling period.

$$T_{as} = V_{an}\frac{T_s}{V_{dc}} \quad (5)$$

$$T_{bs} = V_{bn}\frac{T_s}{V_{dc}} \quad (6)$$

$$T_{cs} = V_{cn}\frac{T_s}{V_{dc}} \quad (7)$$

b) Find Toffset as follows:

$$T_{offset} = 0.5\,(T_{max}+T_{min}) \quad (8)$$

Where T_{max} and T_{min} are the maximum and minimum of T_{as},T_{bs}, and T_{cs}.

c) Calculating Ta(gate), Tb(gate), and Tc(gate) signals; these signals are matched with high frequency triangular wave in PWM generator to generate the gating signals for VSC.

$$T_{a(gate)} = T_{as} + T_{offset} \quad (9)$$
$$T_{b(gate)} = T_{bs} + T_{offset} \quad (10)$$
$$T_{c(gate)} = T_{cs} + T_{offset} \quad (11)$$

From (5) to (11) showed the successful centering of the SVPWM middle inverter switching vectors by adding an offset time signal to the inverter gating signals derived from the amplitude of the sampled reference phase voltages. With the use of the pace vector circuit, the obtained switching pattern is depicted in Figure 4; the SVPWM circuit is applicable in any multilevel VSC setting and in the over-modulation region. Unlike the traditional SVPWM schemes, the generation of the gating signal required no sector angle; the scheme also does not require the look-up tables for inverter switching vectors selection, thereby minimizing the required computation time to estimate the switching times for the inverter legs. This supports the real-time implementation capability of the algorithm.

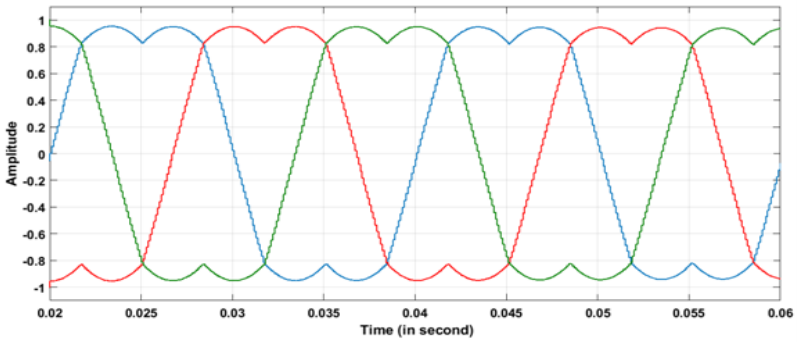


Figure 4. Switching pattern of SVPWM (output of space vector circuit)

2.4. Control circuit strategy

STATCOM control is mainly involved in generation of synchronous output voltage as it regulates the VSC power switches to elicit reactive power exchange between the system and the device. There are two ways to control the output voltage of STATCOM; indirectly, it can be controlled by keeping the modulation index (MI) constant while the DC capacitor voltage is varied. A direct way of the control is by altering the MI value while fixing the voltage of the DC capacitor [11].

$$MI = \frac{V_s^*}{V_{sMax}} \quad (12)$$
$$V_{sMax} = \left(\frac{\sqrt{3}}{\sqrt{2}}\right)\left(\frac{V_{dc}}{\sqrt{3}}\right) \quad (13)$$

Regarding direct control, the MI value is adjusted to vary the output voltage, i.e. varying the switching angles of each H-Bridge unit of the cascaded VSC while keeping the voltages of the DC capacitor constant. MI is directly related to the fundamental output voltage amplitude as given in (12) and (13); so, the adjustment of the MI value translates to the direct adjustment of the output voltage.

Figure 5 depicts the schematic illustration of the direct control strategy. The reference voltage and the actual system voltage are normally compared, and a PI-ANN controller is used to processes the difference (error) between the two voltages. With this process, the appropriate MI value required to change the output voltage of STATCOM is generated; this implies a change in the flow pattern of the reactive power and maintenance of the AC system voltage at a nominal level. The capacitor voltage is maintained by providing minimal active power flow by phase shifting the voltage of STATCOM over a small angle (α) with respect to the voltage of the AC system (called the load angle). Another PI-ANN controller calculates this load angle based on the difference between the actual (V_{dc}) and reference (V_{dc_ref}) capacitor voltages. The α and the output of PLL (θ) are fed to the block of the phase shifter to generate the unit magnitude control signal which is synchronous and locked to the voltage of bus-3 (PCC). This control signal is fed to SVPWM block,

together with MI, to generate the firing pulses to trigger the semi-conductor switches [30]. In this study, the synchronization of the STATCOM output voltage with system output voltage was done using PLL.

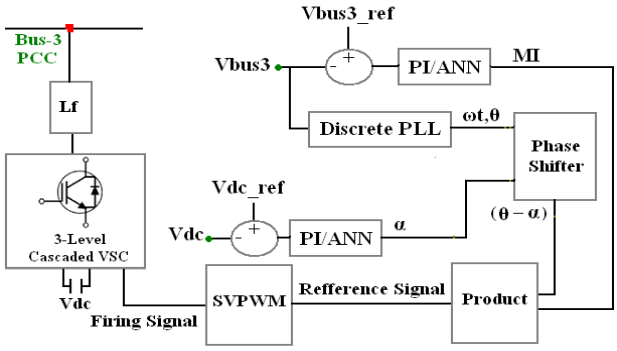


Figure 5. Direct control scheme of 3-level VSC STATCOM

2.4.1. PI controller

A controller is required to control or to operate cascaded 3-level STATCOM during the period of voltage sag. The PCC voltage is sensed and forwarded through a sequence analyzer. Reactive power compensation control loop (control unit of MI) and active power absorption control loop have a separate PI controller (control unit of α). As a feedback controller, the PI controller works by summing the error and integral of those values as revealed in Figure 6 [31].

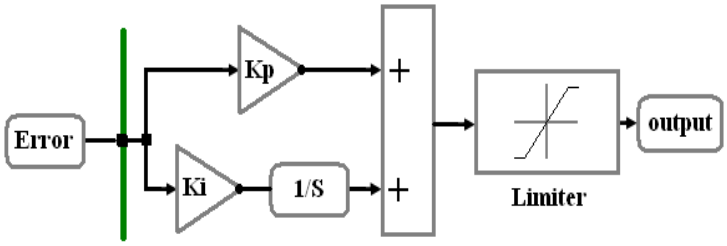


Figure 6. Structure of PI controller

The difference between the reference and actual voltage serve as the input of the PI controller. For the MI control unit, the reference voltage is 1 p.u, where inside this control unit, the proportional gain is 1 whereas the integral gain is 35.In the control unit of α, the proportional and integral gains are 0.025. The output of the PI controller is converted into 3-phase voltage and propagated to the SVPWM pulse generator to generate the pulse that will be forwarded to the cascaded VSC to trigger the IGBT switches.

2.4.2. ANN controller

In this study, a multilayer BP-type ANN controller was used to improve the performance of STATCOM. The ANN was trained using the MATLAB toolbox; Levenberg Marquardt (LM) BP algorithm was utilized as the training algorithm in the ANN controller. Gradient Descent (GD) is a first-order optimization framework for finding the local minimum of any given function. It is a robust method especially when it initiates far from the final minimum; meanwhile, it is prone to poor convergence. LMBP is a second-order optimization framework that lies between GD and Gauss-Newton (GN) frameworks. LM algorithm can find solutions even initiating far from the final solution. LM algorithm is a better option compared to GN and GD methods [32]as it converges rapidly, requires low memory, and can learn [33].

The structure of the ANN controller used in this study has 3 layers as depicted in Figure 7. The layers consist of 1 input layer, 1 hidden layer (comprised of 10 neurons), and 1 output layer. The data for training the ANN are sourced from a conventional PI controller. The ANN controller has the error and the

change in error signals from the MI control unit and α control unit as its input. The ANN controller is expected to minimize this error. The performance metric of the ANN controller is the Mean square error which reflects the error between input values and the target values. 1000 epochs are required for the ANN training in the MI control unit; the best achieved validation performance (0.00000014) is achieved at epoch 6. The total number of epochs in the α control unite is 1000 while the best achieved validation performance (0.00000144) is achieved at epoch 5. The training of the ANN was done offline and was designed for the control of the cascaded VSC STATCOM. Having completed the offline training, the next step is to replace the PI controller with the generated ANN controller.

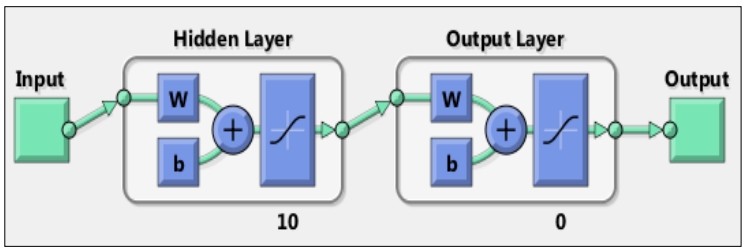


Figure 7. Structure of neural network

3. SYSTEM SPECIFICATIONS

The performance of the STATCOM model was investigated in MATLAB using the parameter shown in Table 1.

Table 1. Power System Parameters

Parameter	Value
3-phase Source (1and2) Parameters	
Rated voltage	6.6 kV (L-L)
Frequency	50 Hz
Impedance	0.89+j5.18 Ω
Impedance of Transmission Line	
Z1,2	0.05+j0.2 Ω
Z1,3	0.02+j0.1 Ω
Z2,3	0.036+j0.12 Ω
Inductive/Capacitive Loads	
Active power	1 MW
Inductive/Capacitive reactive power	1 MVAR
STATCOM device	
Dc Voltage	6 kV
Inductor of Filter	10.7 mH
Switching Frequency	2 kHz

4. SIMULATION RESULTS

For testing the viability of the Cascaded 3-level VSC STATCOM with its two controllers (PI/ANN) in mitigating voltage sag which occurred at bus-3, the following approach was adopted. Each case is classified into three states which are voltage magnitude and PF amplitude during periods of voltage sag. For all the cases, the transition time ranged from 0.8 to 1.3 sec.

4.1. Case A: compensation of voltage sag generated by SLG fault

4.1.1 Voltage magnitude during SLG fault

An SLG fault was applied at bus 3. The first simulation was performed without using STATCOM; it can be observed that the voltage sag of bus 3 was 0.824 pu (14.2% of the reference voltage (0.966 pu)) as displayed in Figure 8. As can be seen, the voltage at bus 3 was not 1 pu within 0 to 0.8 sec and from 1.3 to 2 sec due to the inductive load on the system.

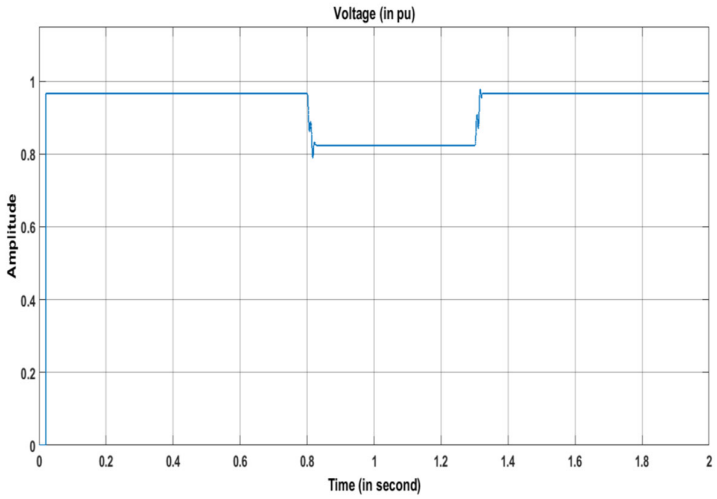
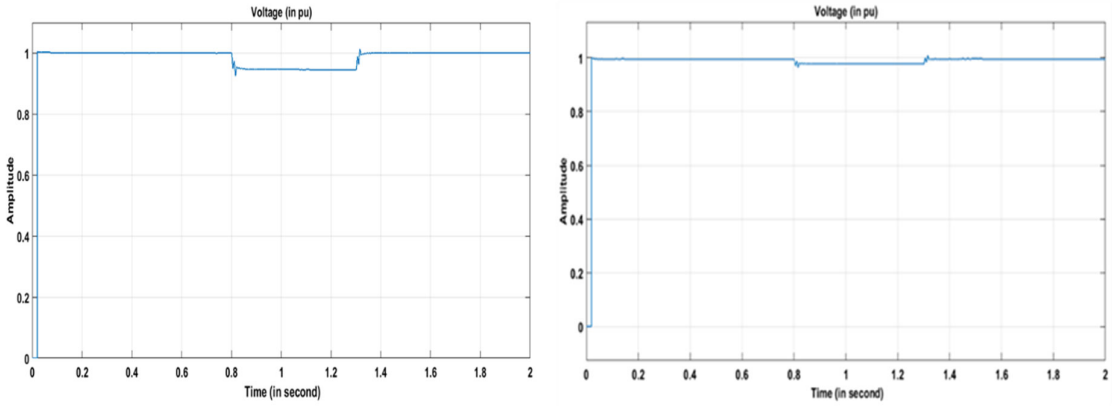


Figure 8. Voltage of bus-3 without STATCOM during SLG fault period

The second simulation was carried out using three-level VSC STATCOM with PI controller connected to the IEEE 3-bus system. During SLG fault, the STATCOM generated the reactive power to the system; then, the voltage sag was mitigated, and the PI took 0.065 sec to maintain voltage at the bus-3 to 0.947 pu (percentage of improvement 12.3 %) as shown in Figure 9(a). Figure 9(b) explained the last simulation that was performed with STATCOM based on ANN controller. In this simulation, ANN needed 0.02 sec to increase the voltage to 0.981 pu (percentage of improvement 15.7%) because the ANN controller reduced the errors to the minimum value.



(a) (b)

Figure 9. Voltage of bus-3 with STATCOM during SLG fault period based on: (a) PI, (b) ANN controllers

4.1.2 Power factor amplitude during SLG fault

Before SLG fault period and without STATCOM, it can see that the PF at bus-3 was 0.71 because of the effect of the inductive load; this increased from 0.71 to unity PF during fault as in Figure 10 due to the load which receives large active power from the supply side. When the 3-level VSC STATCOM-based PI is ON, the PF amplitude recorded 0.997 during SLG fault as described in Figure 11(a). The PI controller required 0.092sec to achieve that value while the STATCOM-based ANN took 0.019sec to maintain the PF at unity as clarified in Figure 11(b).

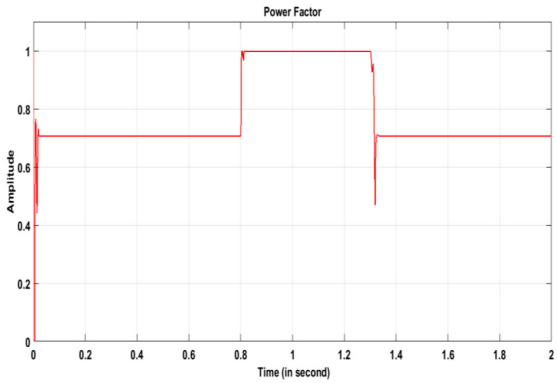
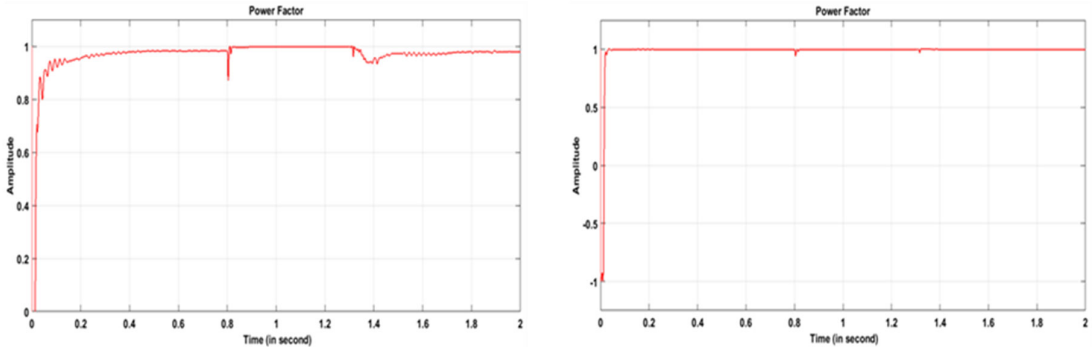


Figure 10. PF of Bus-3 without STATCOM during SLG fault period



(a) (b)

Figure 11. PF of Bus-3 with STATCOM during SLG fault period based on: (a) PI, (b) ANN controllers

4.2. Case B: Compensation of voltage sag generated by LL fault

4.2.1. Voltage magnitude during LL fault

As shown in Figure 12, the connection of LL fault with the Bus-3 provoked a remarkable voltage sag at Bus-3 (phase B), making it to reach 0.78 pu which is 18.6% of the nominal value (0.966 pu).

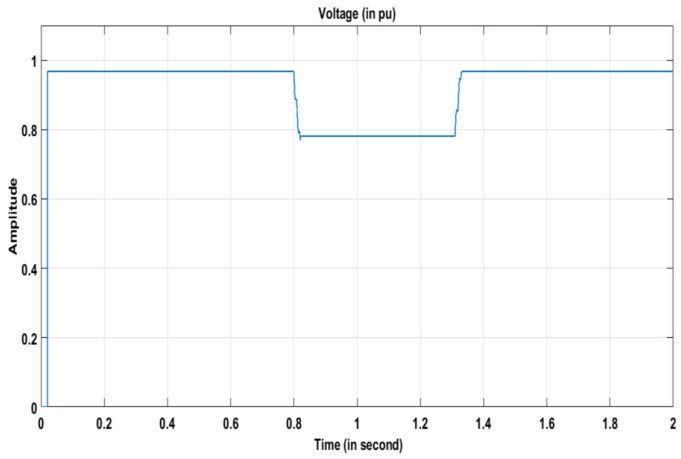
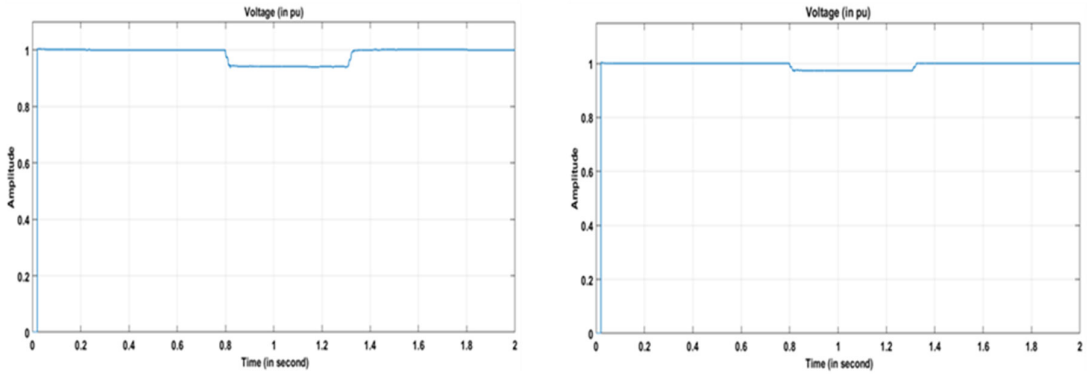


Figure 12. Voltage of Bus-3 without STATCOM during LL fault period

When the PI controller was installed with STATCOM, the PI spent 0.067 sec to make the voltage at the bus-3 around 0.941 pu (improvement 16.1 %) as presented in Figure 13(a). Compared with PI, the ANN controller returned the voltage of bus-3 to a near-normal state (0.973 pu, improvement of 19.3%) within 0.02 sec as shown in Figure 13(b).



(a) (b)

Figure 13. Voltage of bus-3 with STATCOM during LL fault period based on: (a) PI, (b) ANN controllers

4.2.2. Power factor amplitude during LL fault

The PF of bus-3 was boosted from 0.71 to 0.79 by LL fault when the STATCOM was disconnected as depicted in Figure 14.The intervention of the STATCOM controlled by PI and ANN algorithms returned the PF during fault to the acceptable values (0.978 and unity, respectively) with advantages in term of RT for ANN (0.019 sec) compared to PI (0.39 sec) as depicted in Figures 15(a) and 15(b).

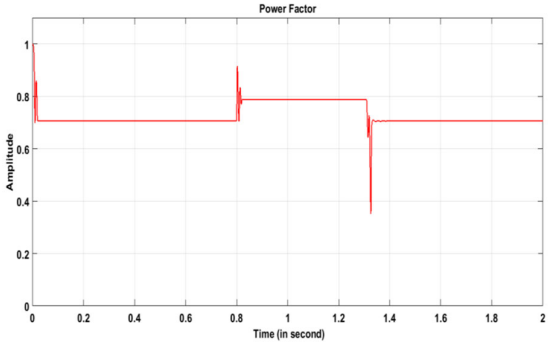
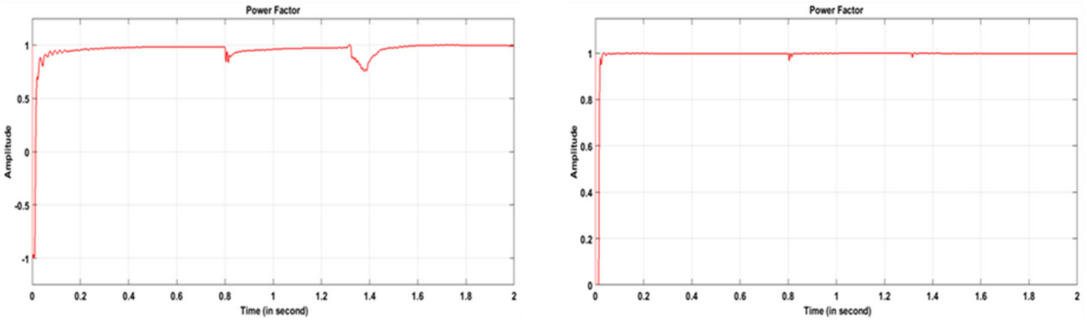


Figure 14. PF of Bus-3 without STATCOMduring LL fault period



(a) (b)

Figure 15. PF of Bus-3 with STATCOM during LL fault period based on: (a) PI, (b) ANN controllers

The comparison of the performance and response time of the proposed model (Cascaded 3-level VSC STATCOM) based on the controllers used (PI and ANN) during voltage sag is depicted in Table 2.

Table 2. Performance and response time of cascaded 3-level VSC STATCOM based on the control mechanism (PI and ANN) during the period of voltage sag sag

Cases	The values during period of voltage sag for			
	SLG Fault		LL Fault	
	Voltage of Bus-3	PF of Bus-3	Voltage of Bus-3	PF of Bus-3
Without STATCOM (pu)	0.824	1	0.78	0.79
With STATCOM based on PI controller (pu)	0.947	0.997	0.941	0.978
Response Time of PI (sec)	0.065	0.092	0.067	0.39
With STATCOM based on ANN controller (pu)	0.981	1	0.973	1
Response Time of ANN (sec)	0.02	0.019	0.02	0.019
Improvement of PI (%)	12.3	- 0.3	16.1	18.8
Improvement of ANN (%)	15.7	0	19.3	21
Response Time of ANN to PI (%)	30.7	20.6	29.8	4.87

5. CONCLUSION

This paper presented the development and performance evaluation of Cascaded three-level VSC STATCOM for improving the power quality of 3-bus distribution systems. A STATCOM based on ANN controller was introduced at bus number-3instead of PI. Furthermore, a novel SVPWM technique was used in this study to control the switching gates of VSC STATCOM. The simulation results as shown in Table 2 revealed that the STATCOM-based intelligent control methodology provided better features and improved power stability during voltage sag in comparison to the conventional PI-based STATCOM.

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