**International Journal of Electrical and Computer Engineering (IJECE)**
Vol. 10, No. 6, December 2020, pp. 5650~5657
ISSN: 2088-8708, DOI: 10.11591/ijece.v10i6.pp5650-5657 

# Temperature characteristics of FinFET based on channel fin width and working voltage

**Yousif Atalla[1], Yasir Hashim[2], Abdul Nasir Abd. Ghafar[3], Waheb A. Jabbar[4]**
[1,3,4]Faculty of Electrical and Electronics Engineering Technology, University Malaysia Pahang (UMP), Malaysia
[2]Computer Engineering Department, Faculty of Engineering, Tishk International University (TIU), Iraq

**Article Info**

***Article history:***

Received Apr 3, 2020
Revised May 6, 2020
Accepted May 20, 2020

***Keywords:***

Channel fin
FinFET
MOSFET
Temperature sensitivity

**ABSTRACT**

This paper shows the temperature sensitivity of FinFET and the possibility of using FinFET as a temperature nano sensor based on Fin width of transistor. The multi-gate field effect transistor (MuGFET) simulation tool is used to examine the temperature effect on FinFET characteristics. Current-voltage characteristics with various temperatures and channel Fin width ($W_F$ = 5,10,20,40 and 80 nm) are at first simulated, the diode mode connection has been used in this study. The best temperature sensitivity of the FinFET is has been considered under the biggest ΔI at the working voltage $V_{DD}$ with range of 0–5 V. According to the results, the temperature sensitivity increased linearly with all the range of channel Fin width (5-80 nm), also, the lower gate Fin width ($W_F$=5nm) with higher sensitivity can achieved with lower working voltage ($V_{DD}$=1.25 V).



***Corresponding Author:***

Yasir Hashim,
Department of Computer Engineering,
Tishk International University (TIU),
Kurdistan-Erbil, Iraq.
Email: yasir.hashim@tiu.edu.iq

## 1. INTRODUCTION

The industry focus on silicon metal-oxide-semiconductor field effect transistors (MOSFETs) for the past 6 decades, this has been mainly due to the simplicity of manufacture, inherent scalability and high levels of possible integration [1, 2]. Until now the industry has kept up with Moore's law [3-5] by making transistors smaller and reducing the distance between them. The problem that arises with reducing size is that the transistor will conduct current even when it turned off and thus consume power. To make the chips with high integration, a new structure of transistors has to be used since old MOSFET structure cannot be reduced further in nano dimension size.

Many new field effect transistor (FET) structures have been extensively explored given that the metal oxide semiconductor FET (MOSFET) technology has continued to approach its downscaling limits. One of the relatively newer FETs is the FinFET as shown in Figure 1 [6], a transistor-structured FET that is a popular research topic in the academic field and semiconductor industry [7-9]. The one new promising MOSFET architecture is the FinFET see Figure 1 that have the gate surrounding the channel which gives a better control and therefore reduces current leaking, one way of creating a FinFET is to use a nanowire as a channel and build a gate around it. [10-12]

The best example of sensors for subsumed electronic applications (i.e. used within equipment) is the semiconductor temperature sensor [13]. Transistor-based temperature sensors are designed on the basis of the temperature characteristics of current–voltage curves of nanowire transistors [14-20]. A bipolar transistor can be used as a temperature sensor by connecting its base and collector and operating them in diode mode. Similarly, a transistor with MOSFET structure can be used as a temperature sensor by connecting the gate with either the source or drain as shown in Figure 2. Electronic devices, such as diodes, transistors, capacitors

and resistors, with nano-dimensions have recently become popular in the electronics industry due to their extremely small electronic circuits.

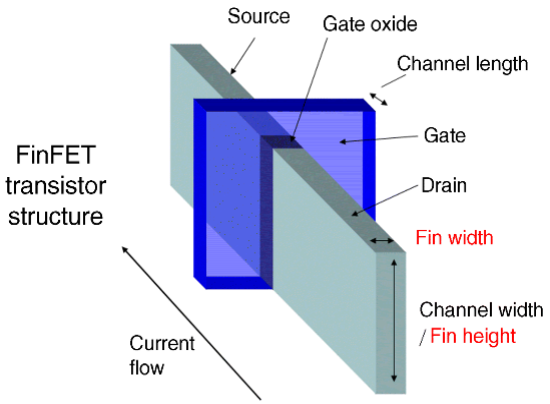


Figure 1. FinFET structure [6]

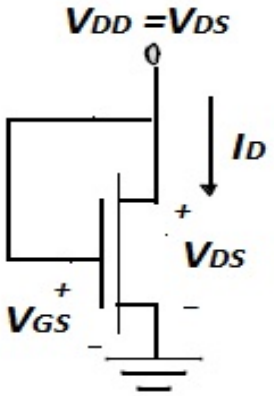


Figure 2. MOSFET as a temperature sensor ($V_g$=$V_d$=$V_{DD}$)

The performance of new devices, which may correspond to a wide array of new applications, will likely depend on the nano-dimensional characteristics of such devices. The chip generation of these relatively new and powerful electronic devices with ultra-small transistors may be even regarded more trustable when new findings from future research are consolidated. However, the new nano-dimensional FET designs and structures are still considered novel technologies and thus necessitate further study and improvement, and they require further innovations despite the limitations in the field of MOSFET science. So, this research explores the effect of width of Fin of FinFET on the temperature sensitivity of transistor and the possibility of using it as a temperature nono-sensor.

## 2. METHOD

Electronic device simulation has become increasingly important in understanding the physics behind the structures of new devices. Thus, simulation tools are adopted in this research for the analysis and evaluation of the temperature sensitivity of FinFET. The simulation tool can be supported the research work for further explore and development of nano-dimensional characterisation [21]. Simulation tools can also help identify device strengths and weaknesses and retrenchment costs and illustrate the extensibility of these devices in the nm range [22, 23].

In this study, MuGFET is used as the simulation tool to explore the characteristics of the FinFET transistor. The output characteristic curves of the transistor under deferent environmental conditions and with deferent parameters are considered. The effect of gate Fin width on the temperature sensitivity has been investigated based on the $I_d$–$V_g$ characteristics. MuGFET [24] simulation tool has been used for the characterization of FinFET with nano-dimensional structure, MUGFET is created and invented at Purdue University.

MuGFET adopts either PADRE or PROPHET for simulation, both of which were developed by Bell Laboratories. The PROPHET is a partial differential equation profiler for one, two, or three dimensions, and PADRE is a device-oriented simulator for 2D or 3D devices with arbitrary geometry [24, 25]. The software can generate useful characteristic FET curves for engineers to help them fully explain the underlying physics of FETs. MuGFET also provides self-consistent solutions to Poisson and drift-diffusion equations [24, 25] and can be used to simulate the motion of transport objects when calculating FinFET characteristics as shown in Figure 1.

This research used a simulation tool, which is called MUGFET. First the suitable parameters and dimensions will be chosen for simulation of FinFET, the data includes dimensions (length channel (Lg), width channel ($W_F$), oxide thickness ($T_{ox}$), doping concentration in channel, source and drain, and finally the temperature (T)), Table 1 illustrate all parameters of FinFET that has been used in the simulation, after simulation complete, the I-V data will have produced depending on parameters entered to the software. Finally, the optimized values were found to optimize the FinFET channel as temperature nano-sensor.

Table 1. Parameters of FinFET used in this study

| Parameter | Values |
|---|---|
| Temperatures T | 250, 275, 300, 325, 350, 375 and 400 K° |
| Working voltage $V_{DD}$ | 0–5 V with 0.25 V steps |
| Channel length Lg | 85 nm |
| Source and Drain lengths | 50 nm |
| Oxide thickness $T_{ox}$ ($SiO_2$) | 2.5nm |
| Gate Fin width $W_F$ | 5,10,20,40 and 80 nm |
| Channel concentration (Si P-type) | $10^{16}$ $cm^{-3}$ |
| Source and Drain concentration (Si N-type) | $10^{19}$ $cm^{-3}$ |

## 3. RESULTS AND DISCUSSIONS

In this research, the $I_d$–$V_g$ characteristics of FinFET at the temperatures of 250, 275, 300, 325, 350, 375 and 400 K° are simulated with the following parameters: channel length= 85 nm, channel concentration (P-type)=$10^{16}$ $cm^{-3}$, source and drain lengths=50 nm, source and drain concentration (N-type)=$10^{19}$ $cm^{-3}$ and oxide thickness=2.5nm. The gate Fin width values are $W_F$=5,10,20,40 and 80 nm.

Figures 3-7 show the change in ΔI when the temperature increased at the $V_{DD}$ range of 0–5 V with 0.25 V steps for the $W_F$ values of 5,10,20,40 and 80 nm. As shown by the figures, the maximum sensitivities (max ΔI) are at the relatively lower temperatures, and the values decreased linearly as temperature increased for all $V_{DD}$. Figures 3 and 4 present the maximum temperature sensitivity values at $V_{DD}$=1.25 V ($W_F$ =5 nm) and $V_{DD}$=1.5 V (W=10nm); followed by Figures 5 and 6 at $V_{DD}$=2 V ($W_F$=20 nm) and $V_{DD}$=3.25 V ($W_F$=40 nm; and finally, Figure 7 at $V_{DD}$=5 V ($W_F$=80 nm).

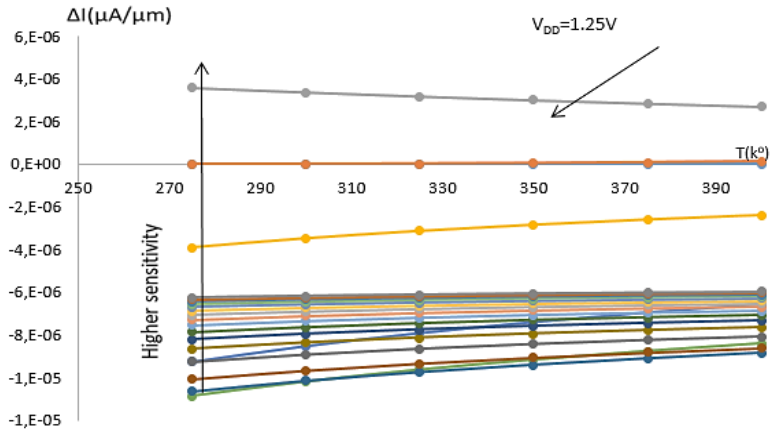


Figure 3. ΔI–Temperature characteristics of FinFET ($W_F$ =5 nm), $V_{DD}$ range of 0–5 V with 0.25 V steps

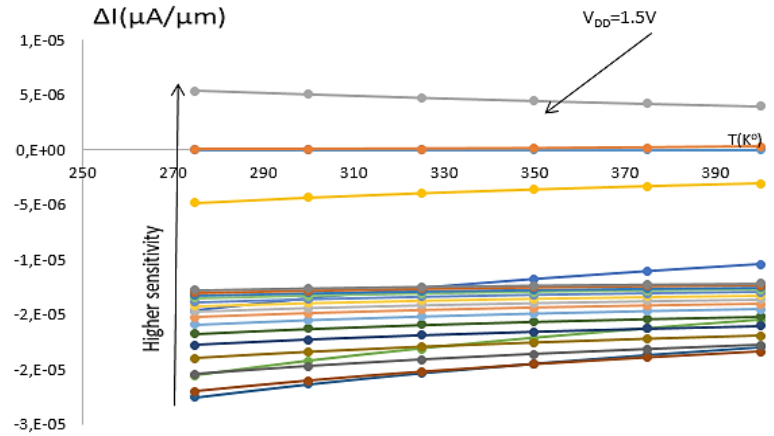


Figure 4. ΔI–Temperature characteristics of FinFET ($W_F$ =10 nm), $V_{DD}$ range of 0–5 V with 0.25 V steps

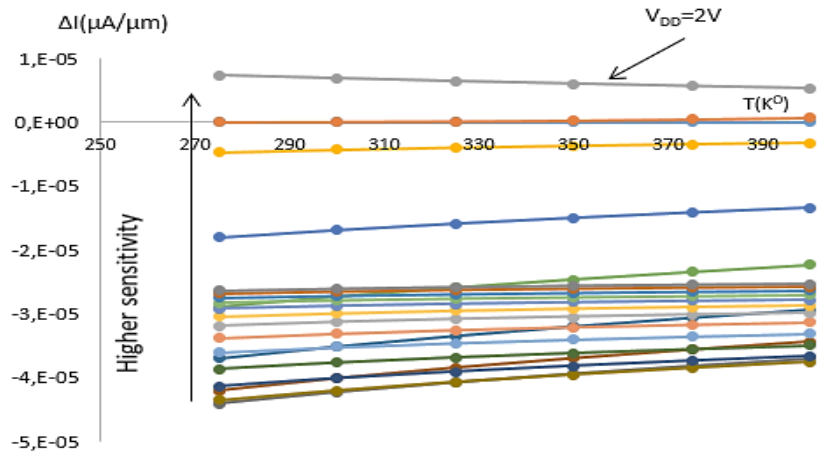


Figure 5. ΔI–Temperature characteristics of FinFET ($W_F$ =20 nm), $V_{DD}$ range of 0–5 V with 0.25 V steps

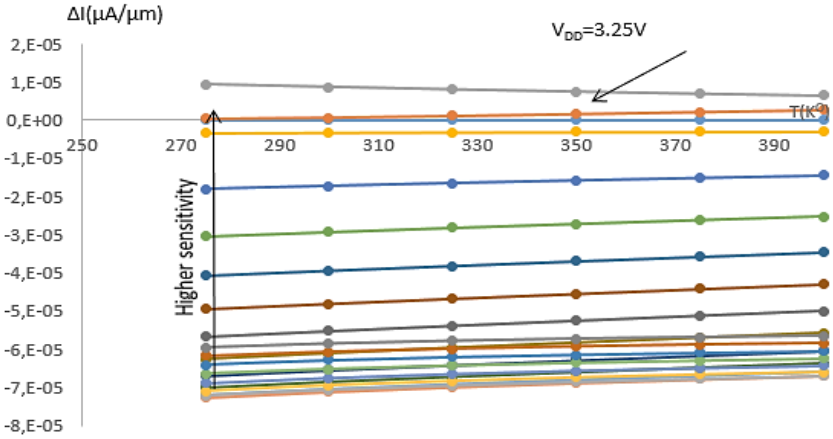


Figure 6. ΔI–Temperature characteristics of FinFET ($W_F$ =40 nm), $V_{DD}$ range of 0–5 V with 0.25 V steps

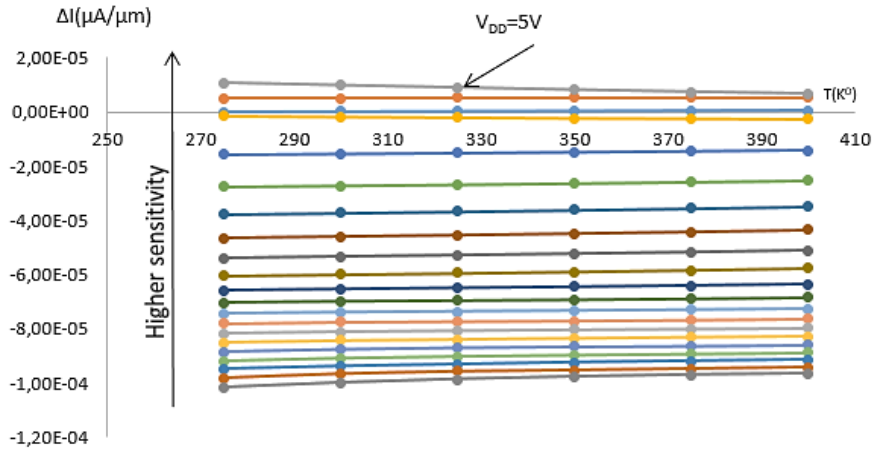


Figure 7. ΔI–Temperature characteristics of FinFET ($W_F$ =80 nm), $V_{DD}$ range of 0–5 V with 0.25 V steps

Figures 8-12 show the changes in ΔI with decreasing $V_{DD}$ at T=250, 275, 300, 325, 350, 375 and 400 K° and W=5,10,20,40 and 80 nm. The following maximum sensitivities (max ΔI) were observed: $V_{DD=}$1.25 V ($W_F$=5 nm), $V_{DD=}$1.5 V ($W_F$=10 nm), $V_{DD=}$2 V ($W_F$=20 nm), $V_{DD=}$3.25 V ($W_F$=40 nm) and $V_{DD=}$5 V ($W_F$=80 nm).

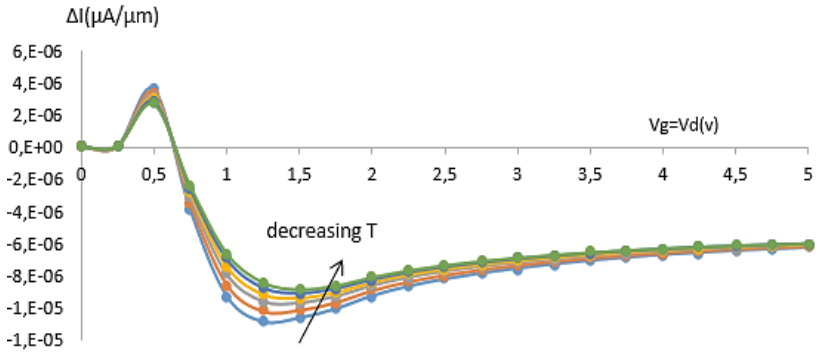


Figure 8. ΔI–$V_{DD}$ characteristics of FinFET ($W_F$=5 nm)

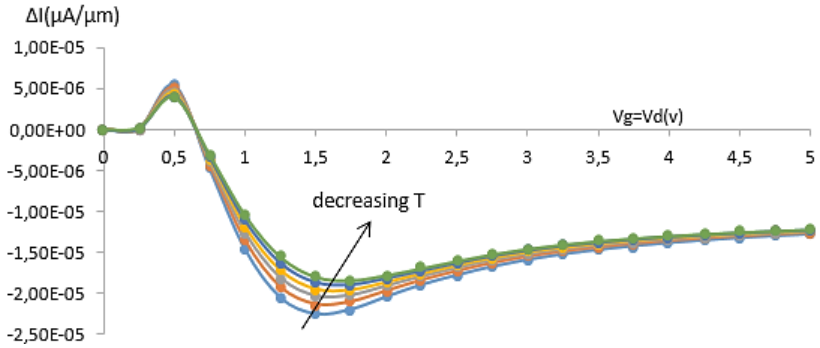


Figure 9. ΔI–$V_{DD}$ characteristics of FinFET ($W_F$=10 nm)

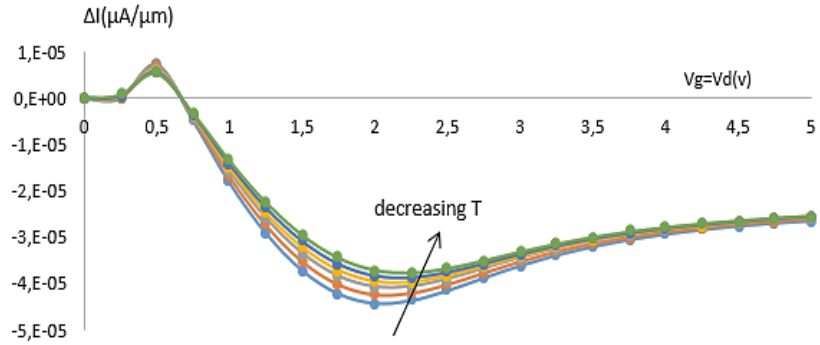


Figure 10. ΔI–$V_{DD}$ characteristics of FinFET ($W_F$=20 nm)

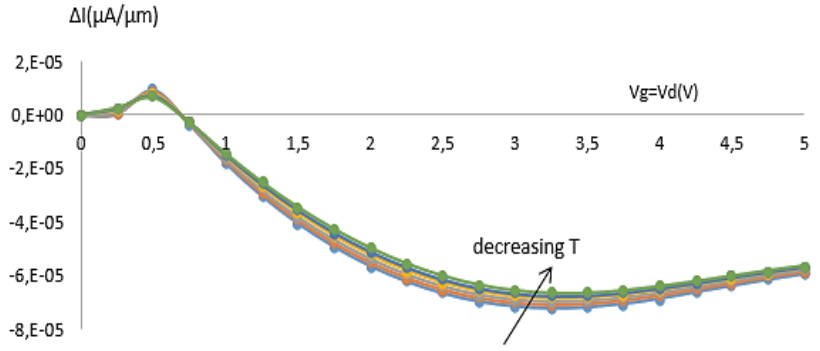


Figure 11. ΔI–$V_{DD}$ characteristics of FinFET ($W_F$=40 nm)

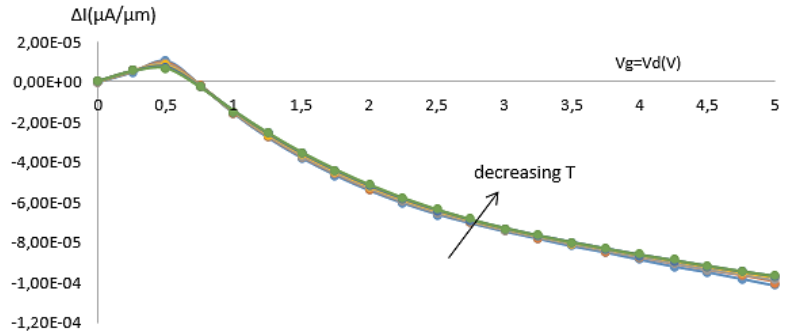


Figure 12. ΔI–$V_{DD}$ characteristics of FinFET ($W_F$=80 nm)

Figure 13 shows the optimum operating voltage ($V_{DD}$) based on the best temperature sensitivity and channel Fin width, where optimal $V_{DD}$ is associated with the temperature sensitivity peaks shown in Figures 8-12. The temperature sensitivity increased linearly with all the range of channel Fin width (5-80 nm). So, the lower gate Fin width ($W_F$=5nm) with higher sensitivity can achieved with lower working voltage ($V_{DD}$=1.25 V).

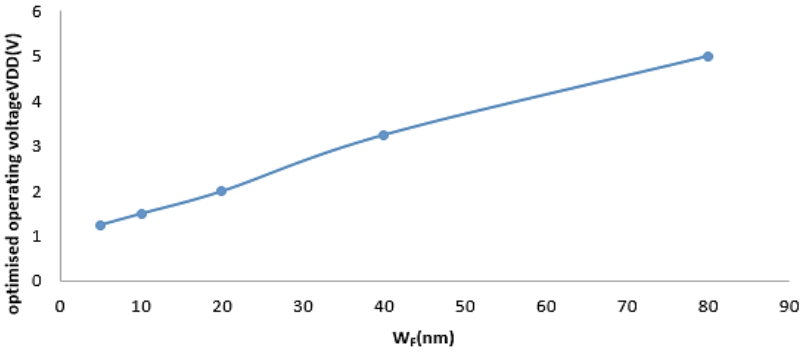


Figure 13. Optimised operating voltage $V_{DD}$ with different channel Fin width based on best temperature sensitivity

## 4. CONCLUSION

The effects of different temperatures (250, 275, 300, 325, 350, 375 and 400 K°) on FinFET characteristics are studied by considering different channel Fin width ($W_F$=5,10,20,40 and 80 nm). For the diode mode transistor connection and increments for the current (ΔI), the working voltage $V_{DD}$ must increase with increasing the gate Fin width to get the best sensitivity, so the lower Fin width has best sensitivity with lower working voltage. The linear relation between temperature sensitivity and working voltage has been result in this study with all range of channel Fin width $W_F$ =5-20nm.

## ACKNOWLEDGEMENTS

This work was supported by the Ministry of Education, Malaysia, under Fundamental Research Grant Scheme FRGS/1/2019/TK04/UMP/02/15 (Grant ID: RDU1901199).

## REFERENCES

[1] G. V. Angelov, D. N. Nikolov, and M. H. Hristov, "Technology and Modeling of Nonclassical Transistor Devices," *Journal of Electrical and Computer Engineering*, vol. 2019, pp. 1-18, 2019.
[2] J. P. Rojas, et al., "Nonplanar Nanoscale Fin Field Effect Transistors on Textile, Paper, Wood, Stone, and Vinyl via Soft Material-Enabled Double-Transfer Printing," *ACS Nano*, vol. 9, no. 5, pp. 5255-5263, 2015.
[3] M. T. Bohr, "Logic Technology Scaling to Continue Moore's Law," *IEEE 2nd Electron Devices Technology and Manufacturing Conference (EDTM)*, pp. 1-3, 2018.
[4] J. M. Shalf and R. Leland, "Computing beyond Moore's Law," *Computer*, vol. 48, no. 12, pp. 14-23, 2015.
[5] L. Eeckhout, "Is Moore's Law Slowing Down? What's Next?," *IEEE Micro*, vol. 37, no. 4, pp. 4-5, 2017.

[6] K. S. Sandha, and S. Singh, "Performance analysis of FinFET based SRAM at nano-scaled technology nodes for low power high speed IC design," *International Journal of Engineering & Technology*, vol. 7, no. 4, pp. 6597-6602, 2018.
[7] B. Yu, et al., "FinFET Scaling to l0nm Gate Length," *International Electron Devices Meeting*, pp. 251-254, 2002.
[8] C. Liu, et al., "Systematical study of 14nm FinFET reliability: From device level stress to product HTOL," *IEEE International Reliability Physics Symposium*, pp. 2F.3.1 - 2F.3.5, 2015.
[9] W. Lu, J. K. Kim, J. F. Klem, S. D. Hawkins and J. A. del Alamo, "An InGaSb p-channel FinFET," *IEEE International Electron Devices Meeting (IEDM)*, pp. 31.6.1 - 31.6.4, 2015.
[10] T. P. Dash, S. Dey, S. Das, E. Mohaptra, J. Jena and C. K. Maiti, "Stress Tuning in NanoScale FinFETs at 7nm," *IEEE Electron Devices Kolkata Conference (EDKCON)*, pp. 166-170, 2018.
[11] X. Xie and J. Ju, "14nm FinFET device electronic study," *China Semiconductor Technology International Conference (CSTIC)*, pp. 1-3, 2016.
[12] L. H. Brendler, A. L. Zimpeck, C. Meinhardt and R. Reis, "Multi-Level Design Influences on Robustness Evaluation of 7nm FinFET Technology," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 2, pp. 553-564, 2020.
[13] G. Meijer, G. Wang, and F. Fruett, "Temperature sensors and voltage references implemented in CMOS technology," *IEEE Sensors J.*, vol. 1, no. 3, pp. 225–234, 2001.
[14] C. N. Liao, C. Chen, and K. N. Tu, "Thermoelectric characterization of Si thin films in silicon-on-insulator wafer," *J. Appl. Phys.*, vol. 86, no. 86, pp. 3204–3208, 1999.
[15] M. Y. Doghish and F. D. Ho, "A comprehensive analytical model for metal-insulator-semiconductor (MIS) devices," *IEEE Trans. Electron Devices*, vol. 39, no. 12, pp. 2771–2780, 1992.
[16] Y. Hashim, and O. Sidek, "Effect of temperature on the characteristics of silicon nanowire transistor," *Journal of nanoscience and nanotechnology*, vol. 12, no. 10, pp. 7849-7852, 2012.
[17] H. T. AlAriqi, W. A. Jabbar, Y. Hashim, H. Bin Manap, "Channel Length-Based Comparative Analysis of Temperature and Electrical Characteristics for SiNWT and GeNWT," *International Journal of Computing and Digital Systems*, vol. 9, no. 1, pp. 89-95, 2020.
[18] G. C. Meijer, G. Wang, and F. Fruett, "Temperature sensors and voltage references implemented in CMOS technology," *IEEE sensors journal*, vol. 1, no. 3, pp. 225-234, 2001.
[19] H. T. AlAriqi, W. A. Jabbar, Y. Hashim, and H. B. Manap, "Temperature Characteristics of Silicon Nanowire Transistor Depending on Oxide Thickness," *Journal of nano- and electronic physics*, vol. 11, no. 3, pp. 1-4, 2019.
[20] Y. Hashim, and O. Sidek, "Temperature effect on IV characteristics of Si nanowire transistor," *IEEE Colloquium on Humanities, Science and Engineering (CHUSER)*, pp. 331-334, 2011.
[21] M. Bescond, K. Nehari, J.L. Autran, N. Cavassilas, D. Munteanu, M. Lannoo, "3D quantum modeling and simulation of multiple-gate nanowire MOSFETs," *IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004., San Francisco, CA*, pp. 617-620, 2004.
[22] H. M. Fahad, C. Hu, and M. M. Hussain, "Simulation Study of a 3-D Device Integrating FinFET and UTBFET," *IEEE Transactions On Electron Devices*, vol. 62, no. 1, pp. 83-87, 2015.
[23] J. Alvarado, J. C. Tinoco, S. Salas, A. G. Martinez-Lopez, B. S. Soto-Cruz, A. Cerdeira and J.-P. Raskin, "SOI FinFET compact model for RF circuits simulation," *IEEE 13th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, pp. 87–89, 2013.
[24] SungGeun Kim, Gerhard Klimeck, Sriraman Damodaran, and Benjamin P. Haley, "MuGFET," 2014. [Online]. Available: https://nanohub.org/resources/NANOFINFET
[25] Y. Hashim, "Optimization of Resistance Load in 4T-Static Random-Access Memory Cell Based on Silicon Nanowire Transistor," *Journal of Nanoscience and Nanotechnology*, vol. 18, no. 2, pp. 1199–1201, 2018.

## BIOGRAPHIES OF AUTHORS

**Yousif Atalla,** the author was born at Iraq, he received the B.Sc. of Engineering in Electronics and Communications Engineering from Engineering Technical College, Iraq. He completed the M.Sc. in Electronics Engineering- Micro and Nano-electronics from Universiti Malaysia Pahang (UMP), Pahang, Malaysia. He is currently working as a Director of the Engineering Affairs Department - Salah Al-Din Governorate Council, Iraq. His research interests include Microelectronics and Nanoelectronic: FinFET transistor.

**Yasir Hashim,** the author was born at Iraq, 1969, he received the B.Sc. and Master of Engineering in Electronics and Communications Engineering from the University of Mosul, Mosul, Iraq, in 1991 and 1995 respectively. He completed the Ph.D. in Electronics Engineering- Micro and Nano-electronics from Universiti Science Malaysia (USM), Penang, Malaysia, in 2013. He is currently a Senior Lecturer in the Faculty of Engineering, Tishk International University, Erbil-Kurdistan, Iraq. His research interests include Microelectronics and Nanoelectronic: Nanowire transistors, FinFET transistor, Multistage Logic Nano-inverters. The author has teaching experience in undergraduate fields of Electrical and Electronics Engineering for 17 years and supervised postgraduate student in Master and Ph.D levels.

**Abdul Nasir Abd. Ghafar,** the author received the B.Sc. in Electrical and Electronics System Engineering, Master in Electronics System and PhD in Systems Engineering from Okayama University of Science, Japan in 2011, 2013 and 2016 respectively. He is currently a Senior Lecturer and Head of Program, Electrical Engineering Technology (Power and Machine), Faculty of Electrical and Electronics Engineering Technology, Universiti Malaysia Pahang (UMP), Malaysia. His research interest includes applied electronics, embedded system, optimization and simulation, robotics, and rehabilitation devices. The author has teaching experience in undergraduate fields of Electrical and Electronics Engineering for 5 years and supervised postgraduate students in both Master and PhD levels.

**Waheb A. Jabbar** received the B.Sc. in Electrical Engineering from the University of Basrah, Iraq, in 2001, the M.Eng. in Communication & Computer and the Ph.D. in Electrical, Electronics, and System Engineering from Universiti Kebangsaan Malaysia (UKM), Bangi, Selangor, Malaysia, in 2011 and 2015 respectively. He is currently a Senior Lecturer in the Faculty of Engineering Technology, Universiti Malaysia Pahang (UMP), Gambang, Pahang, Malaysia. His research interests include Routing Protocols in Ad Hoc Networks, Mobile Communications and Wireless Networking. He also has a keen interest in Nano electronics, Internet of Things applications, and Smart City.