Temperature Impact on The I_{ON}/I_{OFF} Ratio of Gate All Around Nanowire TFET

Firas Natheer Abdul-kadir Agha
Department of Electrical Engineering, College of Engineering
University of Mosu
Mosul, Iraq
firas_nadheer@uomosul.edu.iq

Yasir Hashim
Department of Computer Engineering, Faculty of Engineering,
Tishk International University
Erbil-Kurdistan, Iraq
yasir.hashim@ieee.org

Mohammed Nazmus Shakib
Faculty of Electrical & Electronics Engineering Technology, Universiti Malaysia Pahan
26600 Pekan, Pahang Darul Makmur, Malaysia
nazmus@ump.edu.my

***Abstract*—This research paper presents the effect of working temperature on the I_{ON}, I_{OFF} and I_{ON}/I_{OFF} ratio of gate all around nanowire TFET. The (Silvaco) simulation tool has been used to investigate the temperature characteristics of a transistor. The working temperature range of this study is from -50 to 150 step-up 25 °C. The final results indicate that the negative effects of increasing working temperature of gate all around nanowire TFET due to decreasing of the I_{ON}/I_{OFF} ratio. Hence, the results for I_{ON}/I_{OFF} ratio vs. working temperature characteristics may lead to the use of TFET in electronic circuits with lowest possible working temperature to obtain higher I_{ON}/I_{OFF} ratio.**

Keywords— Nanowire, Transistor, Temperature, TFET, I_{OFF} , I_{ON}.

I. INTRODUCTION

Nowadays, in nanoelectronic technology, a new structures of transistors in nano-scale dimensions has been investigated to overcome the normal MOSFET structure weaknesses in nano-scale [1-3]. One of these structures is the nanowire Tunnel Field Effect Transistors (TFET). TFET are good alternatives to substitute the normal structure of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and it has a potential candidate for electronic devices, because the TFET have low OFF current (I_{OFF}), small sub-threshold swing SS (less than 60 mV/decade), low power consumption and reduced Short Channel Effects (SCE) [4-8]. However, the main drawback of TFET is low ON current (I_{ON}). Hence, a Gate All Around (GAA) structure is exploited to improve the I_{ON} and it can be considered the ultimate solution for the improvement of I_{ON}/I_{OFF} current ratio due to its excellent electrostatic coupling [9-10]. Another advantage of GAA transistor which make it be considered as a promising candidate is the advancements of the applications of complementary metal oxide semiconductor (CMOS) due to its ability to achieve better coupling between channel and gate.

In comparison with a MOSFET, nanowire TFET device controls on the electrostatic of channel better than MOSFET device [11-12]. In MOSFET device the transport mechanism used for carrier diffusion is thermionic injection whereas the tunneling mechanism is used as a reliable technique of the carrier injection in TFET device [13-14]. However, the structure of TFET and MOSFET is similar, but the type of doping in Source and Drain is opposite and the switching mechanism is faster in TFET compared with MOSFET [15]. Moreover, in MOSFET device, the ON current (I_{ON}) increases when the temperature decreases, while in TFET device, the ON current (I_{ON}) increases when the temperature increases, due to the induced temperature which make on the reduction of the band gap [16]. Hence, this research pay attention to analysis and investigation of the effect of working temperature on I_{ON}, I_{OFF} and I_{ON}/I_{OFF} ratio of nanowire TFET with gate all around structure.

Finally, the GAA structure of TFET will increase the density on-chip device with high controllability of gate [12]. So, the GAA TFETs are considered as the one of contenders for the throne of MOSFETs [17-18],

II. METHODOLOGY

A gate all around TFET device, has been designed and simulated by using Silvaco simulation tool by the specified dimension of nanometers scales as shown in Table I. Figure 3 shows a cross-sectional area of the geometric structure and limited dimension of the device, where the radius of the silicon intrinsic channel is (R), the gate length (L_g) and thickness of the gate oxide dielectric material SiO_2 is (T_{ox}).

TABLE I. SIMULATION PARAMETERS OF TFET

Parameter	Value
Channel radius (R)	(35) nm
Oxide thickness (T_{OX})	(4.5) nm
Channel Doping (P)	10^{17} cm^{-3}
Drain Doping (P^+)	10^{19} cm^{-3}
Source Doping (N^+)	10^{19} cm^{-3}
Drain length	80 nm
Source length	80nm
Channel length (L)	(200) nm

Doping concentration of the channel is 10^{17} cm^{-3} and doping concentrations for drain and source is 10^{19} cm^{-3}, respectively. The dimensions of the channel L_g is 200 nm, radius of the channel R is 35nm, SiO_2 thickness Tox is 4.5 nm and dimensions for drain and source lengths (L_S and L_D) is 80 nm, respectively.

In this work, we used various temperature degrees, from -50°C to 150°C step-up by 25°C. The voltage taken at the drain terminal (VDS) is 1 V and voltage applied at the gate terminal (V_{GS}) is varied from 0 V to 1 V in step-up 0.1 V.

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The characteristic of GAA Si TFET has been investigated and verified using Silvaco including I_{ON}, I_{OFF}, and I_{ON}/I_{OFF}.

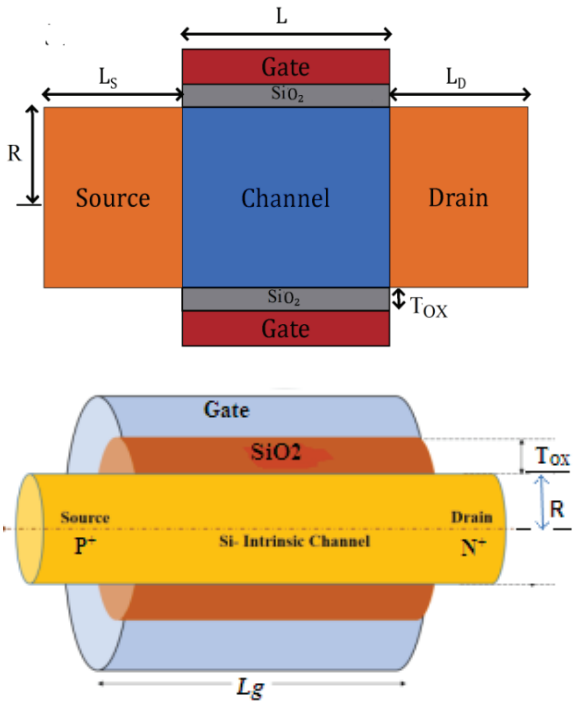

Fig. 1. Structure of simulated GAA Si TFET

III. Results and Descussions

The impact of working temperature on the FET characteristics has been studied and investigated using the dimensions and concentrations demonstrated in Table I. The drain current (I_d) vs. gate voltage (V_g) [transfer characteristics] at working temperatures T= -50, -25, 0, 25, 50, 75, 100, 125, and 150 ºC presented in Figure 2 and Figure 3, where the drain voltage V_d = 1 V. According to the transfer characteristics, the drain current always increases with increasing working temperature for all range of V_g starting OFF state (V_g = 0 V) (Figure 1). Figure 3 explains the increment of drain current at V_g = 1 V. This result refers to the Si channel resistance value going down with increasing working temperature depending on the resistance-temperature characteristics for Si-based devices. Here, it is clear that the higher I_d happens at the higher T.

The transistor working temperature dependent characteristics tend to have a great effect on the major electrical parameters that rule the transistor's features in analog or digital circuits, such as I_{ON}/I_{OFF} ratio, drain-induced barrier lowering (DIBL), and V_T.

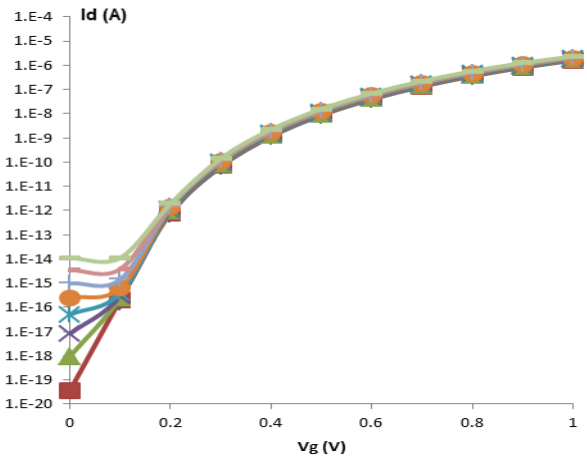

Fig. 2. Transfer characteristics (I_d logarethmic scale) at working temperatures T= -50, -25, 0, 25, 50, 75, 100, 125, and 150 ºC.

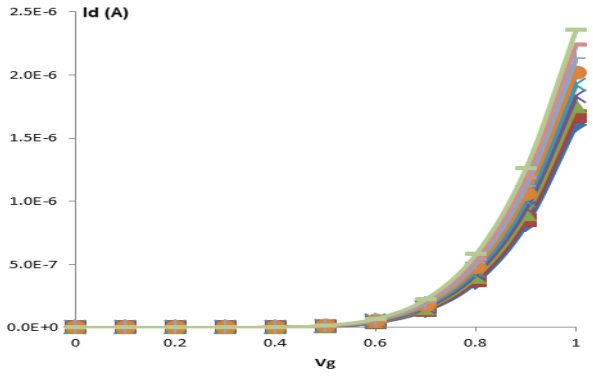

Fig. 3. Transfer characteristics (Id normal scale) at working temperatures T= -50, -25, 0, 25, 50, 75, 100, 125, and 150 ºC.

Figure 4 illustrates the dependence of threshold voltage on working temperature and the V_T decreases linearly with increasing working temperature. Figure 5 shows the drain ON (I_{ON}) and OFF (I_{OFF}) current with temperature characteristics. These results explained that ON drain current increases linearly with increasing temperature, while the drain OFF current increases exponentially with increasing temperature.

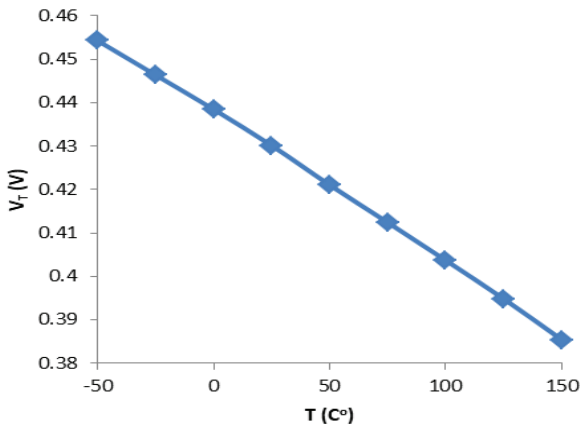

Fig. 4. Threshold voltage vs. working temperature.

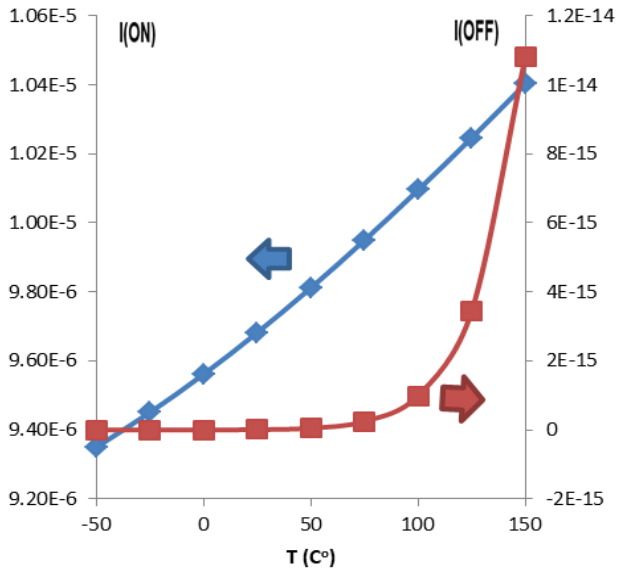

Fig. 5. The drain ON (I_{ON}) and OFF (I_{OFF}) current of GAA Si TFET with temperature characteristics.

Figure 6 illustrates the impact of working temperature on drain ON to OFF current ratio (I_{ON}/I_{OFF}), which is considered as one of the most significant parameters for using transistors in digital electronic circuits. According to Figure 4, the maximum ratio of I_{ON}/I_{OFF} occurs at -25 °C and then exponentially decreased. For numerous transistor applications in electronic circuit such as logic gates and amplifiers, the highest value of I_{ON}/I_{OFF} current ratio is the best for these applications. Thus, the findings of ON to OFF drain current ratio (I_{ON}/I_{OFF}) with temperature characteristics may lead to use of TFET in electronic circuits with lower temperature to obtain a higher I_{ON}/I_{OFF} ratio as possible.

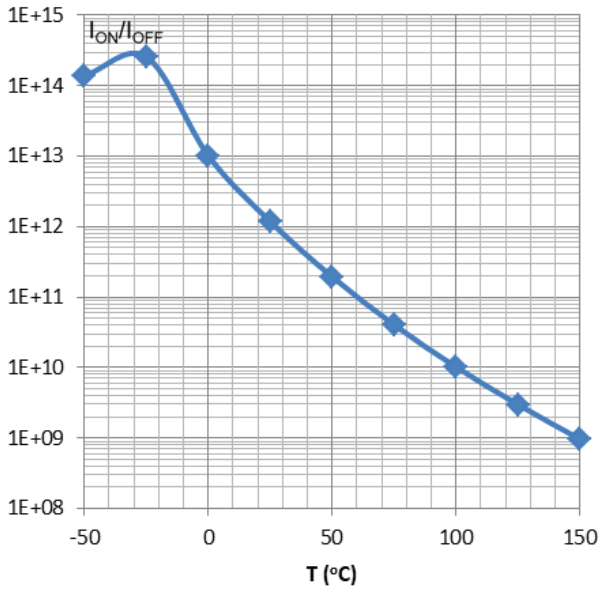

Fig. 6. The impact of working temperature on drain ON to OFF current (I_{ON}/I_{OFF}) of GAA Si TFET.

IV. Conclussions

This research explores the temperature impact on the I_{ON}/I_{OFF} of TFET using Silvaco as a simulation tool. The temperature range was from -50 to 150 step at 25 °C. The results point a serious impact of increasing working temperature on the I_{ON}, I_{OFF} and I_{ON}/I_{OFF} ratio of TFET, while I_{ON} increasing linearly, I_{OFF} increasing exponentially, and I_{ON}/I_{OFF} decreasing exponentially with the increasing working temperature. These changes will affect on its application in electronic circuits with high-temperature environments. This results indicate that using TFET in electronic circuits must be with its lowest possible working temperature to obtain higher I_{ON}/I_{OFF} ratio.

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