Received: 16 March 2020 | Revised: 11 May 2020 | Accepted: 11 June 2020

DOI: 10.1002/est2.193

RESEARCH ARTICLE

ENERGY STORAGE WILEY

Modeling and analysis of hybrid multilevel converter for constant DC and fuel cell sources

Arigela Satya Veerendra[1] | **Mohd Rusllim Mohamed**[1] | **Mohd Herwan Sulaiman**[1] | **Pui Ki Leung**[2]

[1]Sustainable Energy & Power Electronics Research (SuPER) Cluster, Universiti Malaysia Pahang, Kuantan, Pahang, Malaysia

[2]Faculty of Engineering and the Environment, University of Southampton, Highfield, UK

Correspondence
Mohd Rusllim Mohamed, Sustainable Energy & Power Electronics Research (SuPER) Cluster, Universiti Malaysia Pahang, 26600 Kuantan, Pahang, Malaysia.
Email: rusllim@ump.edu.my

Funding information
University Malaysia Pahang

Abstract

This article proposes a symmetrical hybrid multilevel converter topology with a constant DC source and a fuel cell source (FCS) for enhancing the voltage levels and minimization of total harmonic distortions (THD). The proposed topology is employed using a modified phase shifted pulse width modulation (PS-PWM) in order to control the power electronic switches. In this hybrid topology, the first converter operated through low voltage with high frequency and the second converter through high voltage with fundamental frequency for improving the voltage levels. The THD for the hybrid multilevel converter with respect to current and voltage is 1.97% and 15.10%, respectively. The results show that the proposed topology performs better with a constant DC source compared to the fuel cell source. Furthermore, the less component count of the proposed topology is compared with the existing topologies. Comparisons are made to validate the results of the proposed topology with different sources and the existing topologies.

Highlights

- A symmetrical hybrid multilevel converter for different sources is proposed.
- Enhanced voltage levels with less component count are proposed.
- The minimization of THD with constant DC source is proposed.
- A modified PS-PWM controller for effective voltage balancing is discussed.

KEYWORDS

dc-link capacitor, flying capacitor, fuel cell source, hybrid multilevel converter, total harmonic distortion

1 | INTRODUCTION

Multilevel converters have received significant attentions in recent years to achieve high power with enhancing voltage levels.[1-4] Among all classical multilevel topologies, three converters play a key role, namely the cascaded multilevel H-bridge (CHB), the flying capacitor (FC), and the neutral-point clamped (NPC)[5-8] in academic research as well as industrial sectors. Rodriguez et al[6] proposed a three-level NPC converters applicable to high voltage drives over 6 kV. The major drawback of this topology is the restricted voltage blocking for the power electronic switches. Hatti et al[9] proposed a five-level NPC converter in order to overcome the above limitation. However, it endures voltage imbalance of dc-link capacitors.

Following this, for high power applications, Meynard et al[7] proposed a FC multilevel converter that

depends on the balancing of the capacitor voltages.[10-14] Nevertheless, in this converter, the amount of clamping capacitors rises quickly with the voltage level, which improves the complication of the scheme tremendously. Malinowski et al[8] proposed a CHB converter, has been gaining more popularity in greater voltage applications more than 8 kV, is another commercialized multilevel topology. However, these topologies have drawbacks of high cost and component stress. The combination of various multilevel converters leads to novel topologies, known as hybrid multilevel converters, that enhance the voltage levels and reduce the dc sources and number of clamping devices.

One of the primitive multilevel hybrid topologies discussed elsewhere[15,16] is the stacked multicell converter where two multilevel FC converters stacked jointly. Barbosa and Wang et al[17-19] suggested a five-level active NPC (5L-ANPC) hybrid topology. Besides, Chen et al[20] proposed a 3L-ANPC topology. Nevertheless, the main drawbacks of the two topologies are the necessity of two series-connected switches ensures the same voltage stress, which decrease the efficiency of the converters. To overcome the intrinsic disadvantages of above topologies, Tian et al[21] proposed a 4 L (four-level) nested NPC converter and Wang et al[22,23] proposed a 4 L hybrid-clamped topology. However, these various converters are designed by combining the NPC and FC topologies. Nonetheless, the limitation of these combinations is difficult to attain voltage levels not more than five.

Different topologies were proposed with the combination of CHB converters, namely asymmetrical topologies[24-27] and symmetrical topologies.[28-31] Rech et al have conducted various literatures on these hybrid multilevel converters.[25] However, the improper power demands and loss of modularity are the major problems of these converters. Su[28] and Zheng et al[29] have suggested various multilevel hybrid converters to increase the output voltage levels. Nevertheless, these converters have major limitation of excess number of isolated dc-sources. Sandeep et al[32,33] proposed a various multilevel topologies based on switched capacitors. Nevertheless, these topologies have a major limitation of high THD, more dc sources and components.

This article proposes a hybrid multilevel converter topology for different sources such as constant DC and fuel cell sources for enhancing voltage levels. The topology is integrated with modified phase shifted pulse width modulation technique (PS-PWM) in order to analyze the component count and THD for different sources, and comparisons are made accordingly. Furthermore, the voltage balancing of FC and DC link capacitors is also investigated.

2 | PROPOSED TOPOLOGY

Figure 1 shows the proposed configuration of the symmetrical hybrid multilevel converter consisting of two stages or cells, where the first stage reflects dc/dc converter operating through high-frequency with low voltage and the second stage used for fundamental frequency with high voltage. The entire system is examined with constant DC source and fuel cell source (FCS).

The voltage response (V_{dx}) of the first stage is five level with a voltage rating of all switches as $V_{dc}/4$ and the second stage voltage response (V_{ox}) is nine level with a voltage rating of all switches as V_{dc}. This article is a significant review.[19] If the voltage of dc-link capacitor is continuous and reaches to 4 V, then the flying capacitors C_{fx1} and C_{fx2} rated voltages are V. The following working rules should be followed for the generation of multilevel voltage response:

1. It is necessary to operate Switches $S_{x1} - S_{x6}$ and $S'_{x1} - S'_{x6}$, in the complimentary method.
2. Bipolar modulation is used to operate the H-bridge. In other words, S_{x5} and S'_{x6} will be controlled synchronously while S_{x6} and S'_{x5} will be operated synchronously.

By considering the operating regulations, it is possible to write the total output voltage as

$$V_{ox} = V_{dx}.\left(S_{fx5} - S_{fx6}\right) \tag{1}$$

To run S_{x5} and S_{x6} at the basic frequency, it is possible to decide S_{fx5} as follows:

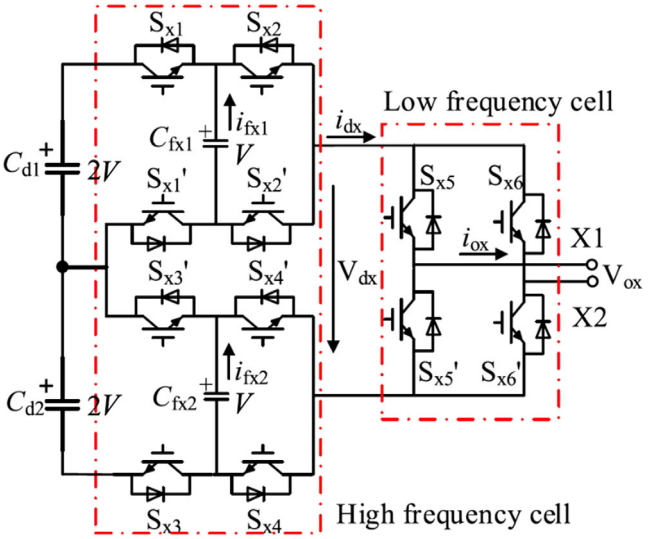

FIGURE 1 Proposed structure of hybrid multilevel converter

$$S_{fx5} = \begin{cases} 0 & u_{ox \le 0} \\ 1 & u_{ox > 0} \end{cases} \quad (2)$$

$$u_{\text{ref}x} = \begin{cases} u_{ox} & S_{fx5=1} \\ -u_{ox} & S_{fx5=0} \end{cases} \quad (3)$$

where

u_{ox} = voltage of the reference stage output.

The reference modulation voltage $u_{\text{ref}x}$ will be represented as follows for the high-frequency cell:

In addition, S_{x1}, S_{x2}, S_{x3}, and S_{x4} switches are independent of each other, allowing the use of phase shifted pulse width modulation (PS-PWM) to regulate the high-frequency cell. The switching states and their respective output voltages are shown as follows in Table 1.

TABLE 1 Switching states with total output voltage

H-bridge cells		DC/DC converter cells				Total output voltage (V_{ox})
S_{x6}	S_{x5}	S_{x4}	S_{x3}	S_{x2}	S_{x1}	
OFF	ON	OFF	OFF	OFF	OFF	0
OFF	ON	ON	OFF	OFF	OFF	+V
OFF	ON	OFF	ON	OFF	OFF	+V
OFF	ON	OFF	OFF	ON	OFF	+V
OFF	ON	OFF	OFF	OFF	ON	+V
OFF	ON	ON	ON	OFF	OFF	+2 V
OFF	ON	OFF	ON	ON	OFF	+2 V
OFF	ON	OFF	OFF	ON	ON	+2 V
OFF	ON	ON	OFF	ON	OFF	+2 V
OFF	ON	OFF	ON	OFF	ON	+2 V
OFF	ON	ON	OFF	OFF	ON	+2 V
OFF	ON	ON	ON	ON	OFF	+3 V
OFF	ON	ON	ON	OFF	ON	+3 V
OFF	ON	ON	OFF	ON	ON	+3 V
OFF	ON	OFF	ON	ON	ON	+3 V
OFF	ON	ON	ON	ON	ON	+4 V
ON	OFF	OFF	OFF	OFF	OFF	0
ON	OFF	ON	OFF	OFF	OFF	−V
ON	OFF	OFF	ON	OFF	OFF	−V
ON	OFF	OFF	OFF	ON	0	−V
ON	OFF	OFF	OFF	OFF	ON	−V
ON	OFF	ON	ON	OFF	OFF	−2 V
ON	OFF	OFF	ON	ON	OFF	−2 V
ON	OFF	OFF	OFF	ON	ON	−2 V
ON	OFF	ON	OFF	ON	ON	−2 V
ON	OFF	OFF	ON	OFF	ON	−2 V
ON	OFF	ON	OFF	OFF	ON	−2 V
ON	OFF	ON	ON	ON	OFF	−3 V
ON	OFF	ON	ON	OFF	ON	−3 V
ON	OFF	ON	OFF	ON	ON	−3 V
ON	OFF	OFF	ON	ON	ON	−3 V
ON	OFF	ON	ON	ON	ON	−4 V

3 | VOLTAGE BALANCING OF CAPACITORS

The effective voltage balancing of the proposed converter is analyzed as follows. Let the instant FC currents (i_{fx1}, i_{fx2}) be represented for the FCs C_{fx1} and C_{fx2} are shown in Equation (4).

$$\begin{cases} i_{fx1} = \left(S_{fx2} - S_{fx1}\right).i_{dx} \\ i_{fx2} = \left(S_{fx4} - S_{fx3}\right).i_{dx} \end{cases} \tag{4}$$

where i_{dx} is the current flowing from the high frequency cell, showed in Equation (5).

$$i_{dx} = i_{ox}.\left(S_{fx5} - S_{fx6}\right) \tag{5}$$

The instant neutral point (NP) currents i_{Nx} can be written for the dc-link capacitors as

$$i_{Nx} = \left(1 - S_{fx1}\right).i_{dx} - \left(1 - S_{fx3}\right).i_{dx} = \left(S_{fx3} - S_{fx1}\right).i_{dx} \tag{6}$$

Let, duty ratios of $S_{fx1} - S_{fx4}$ are $d_{x1} - d_{x4}$, respectively, based on (1), during carrier period of low voltage cell the average output voltage is defined in Equation (7).

$$u_{dx} = (d_{x1} + d_{x2} + d_{x3} + d_{x4}).V \tag{7}$$

When frequency of the carrier is high, it is necessary to note the reference signal as steady. Duty ratios are then displayed in Equation (8).

$$d_{x1} = d_{x2} = d_{x3} = d_{x4} = \frac{u_{\text{ref}x}}{4} \tag{8}$$

The average carrier period FC currents basing on Equation (4) as:

$$\begin{cases} \bar{i_{fx1}} = (d_{x2} - d_{x1}).i_{dx} \\ \bar{i_{fx2}} = (d_{x4} - d_{x3}).i_{dx} \end{cases} \tag{9}$$

The average carrier period NP currents basing on Equation (5) as:

$$\bar{i_{Nx}} = (d_{x3} - d_{x1}).i_{dx} \tag{10}$$

The modified PS-PWM corresponding equations are as follows:

TABLE 2 Specifications of the proposed topology

Parameters	Rating
DC-link capacitor	2820 μF
Flying capacitor	$C_f = 200$ μF
Carrier frequency	$f_c = 5$ kHz
Constant DC voltage	$V_{dc} = 300$ V
FCS voltage	320 V
FCS current	90 A
Total cells	70
Nominal stack efficiency	55%

$$\left.\begin{aligned} \Delta d_{x1} &= -\frac{1}{4}\Delta d_{x21} - \frac{1}{4}\Delta d_{x43} + \frac{1}{2}\Delta d_{x31} \\ \Delta d_{x2} &= \frac{3}{4}\Delta d_{x21} - \frac{1}{4}\Delta d_{x43} + \frac{1}{2}\Delta d_{x31} \\ \Delta d_{x3} &= -\frac{1}{4}\Delta d_{x21} - \frac{1}{4}\Delta d_{x43} - \frac{1}{2}\Delta d_{x31} \\ \Delta d_{x4} &= -\frac{1}{4}\Delta d_{x21} + \frac{3}{4}\Delta d_{x43} - \frac{1}{2}\Delta d_{x31} \end{aligned}\right\} \tag{11}$$

Where $\Delta d_{x1,}\Delta d_{x2}$, $\Delta d_{x3,}$ Δd_{x4} are small change in duty ratio. The proposed topology specifications are displayed in Table 2.

4 | RESULTS AND DISCUSSIONS

Figure 2 shows a symmetrical hybrid multilevel converter modeling and simulation for enhancing the voltage and balancing of the capacitors. The entire system is connected to the 3∅ asynchronous motor to observe the performance. From Figure 3, each phase of this hybrid converter consists of a dc/dc converter and a H-bridge converter. A modified phase-shifted PWM is operated to control the switches of the converters correspondingly.

Figures 4 and 5 show the voltage responses of the three-level dc/dc converter and five level H-bridge converter respectively. It is observed that the voltage levels of the proposed topology with FCS are improved. Furthermore, the effective voltage balancing of the capacitors are obtained is depicted in Figure 6. It is stated that the voltages of the capacitors V_{d1}, V_{d2}, V_{fx1}, and V_{fx2} are 160, 170, 10, and 20 V, respectively.

Figures 7 and 8 display the THD of phase voltage and current of the proposed topology with FCS is 32.04% and 4.86%, respectively. The proposed topology component count with fuel cell source is shown in Table 3.

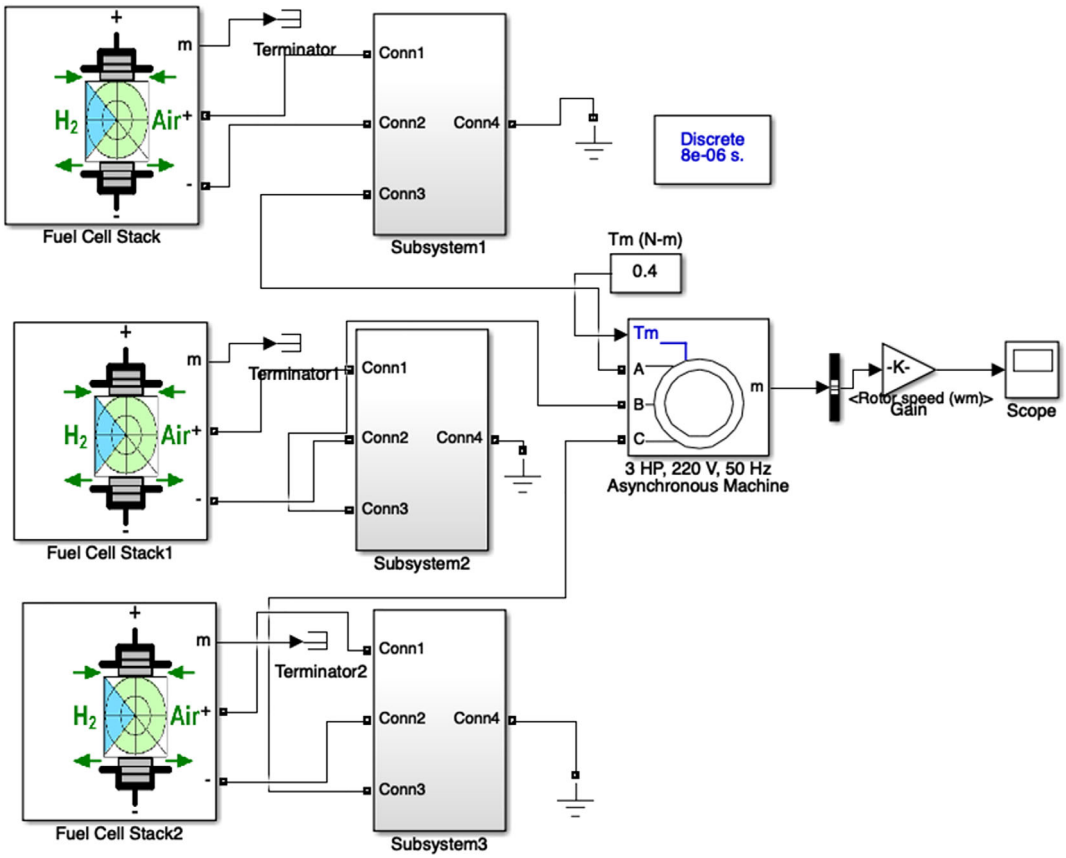

FIGURE 2 Proposed topology with FCS

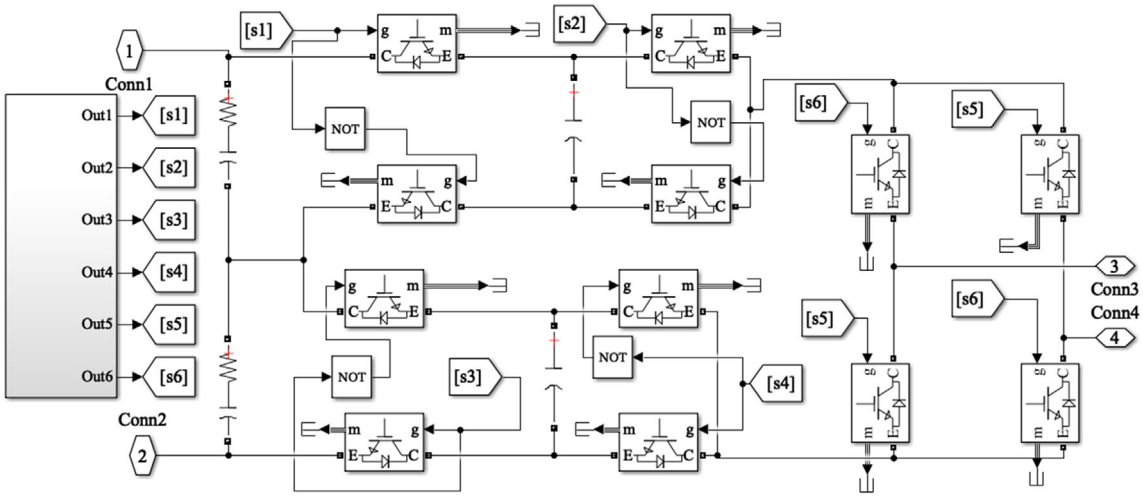

FIGURE 3 Simulation of proposed hybrid converter per phase

Furthermore, the proposed topology is investigated with a constant DC voltage of 300 V and is shown in Figure 9. For a constant DC source, a five-level response of dc/dc converter per phase is depicted in Figure 10 and it is observed that the voltage levels in steps of 60 V has been shaped from 0 to 300 V. Meanwhile, Figures 11 and 12 show the nine-level response of the inverter per phase and 3-∅ has been shaped from −300 to 300 V.

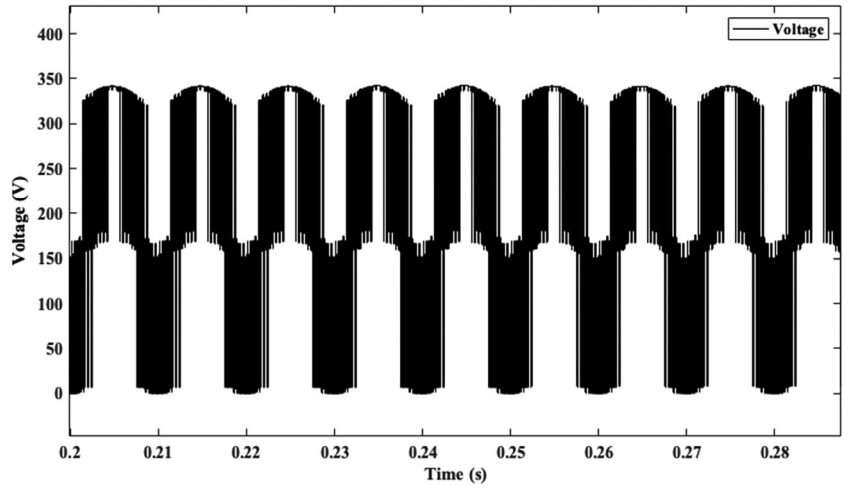

FIGURE 4 DC/DC converter voltage with FCS

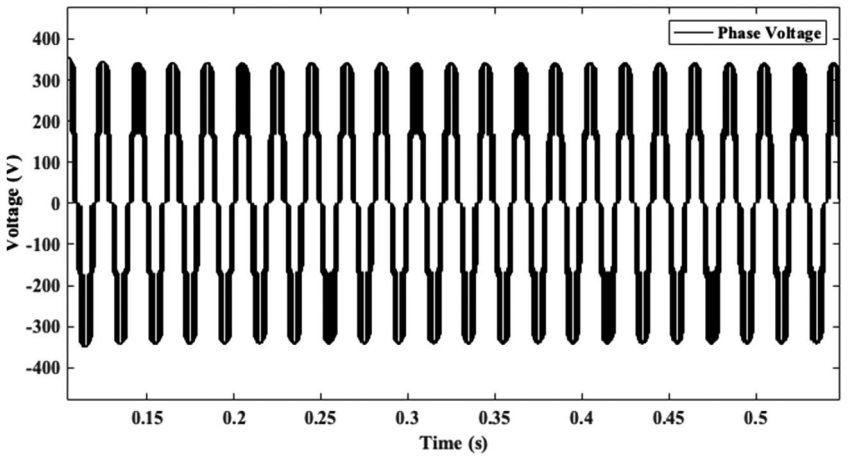

FIGURE 5 H-bridge converter voltage with FCS

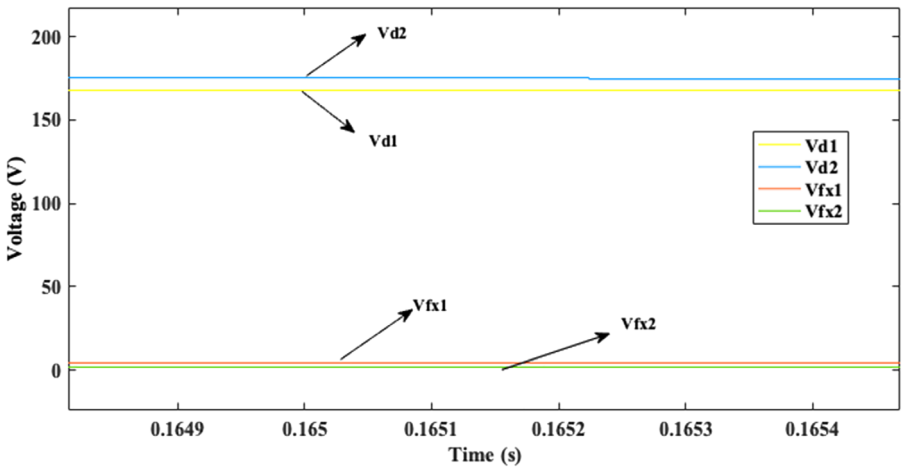

FIGURE 6 Capacitors voltage balancing with FCS

Figure 13 shows the per phase voltage balancing of the flying capacitors and dc-link capacitors. It is observed that the voltages of V_{fx1}, V_{fx2}, V_{d1}, and V_{d2} are 90, 20, 120, and 180 V, respectively. The zoom effect is given in order to depict the well-balanced states of capacitors. Nevertheless, the capacitors voltage balancing can be examined experimentally in the future articles.

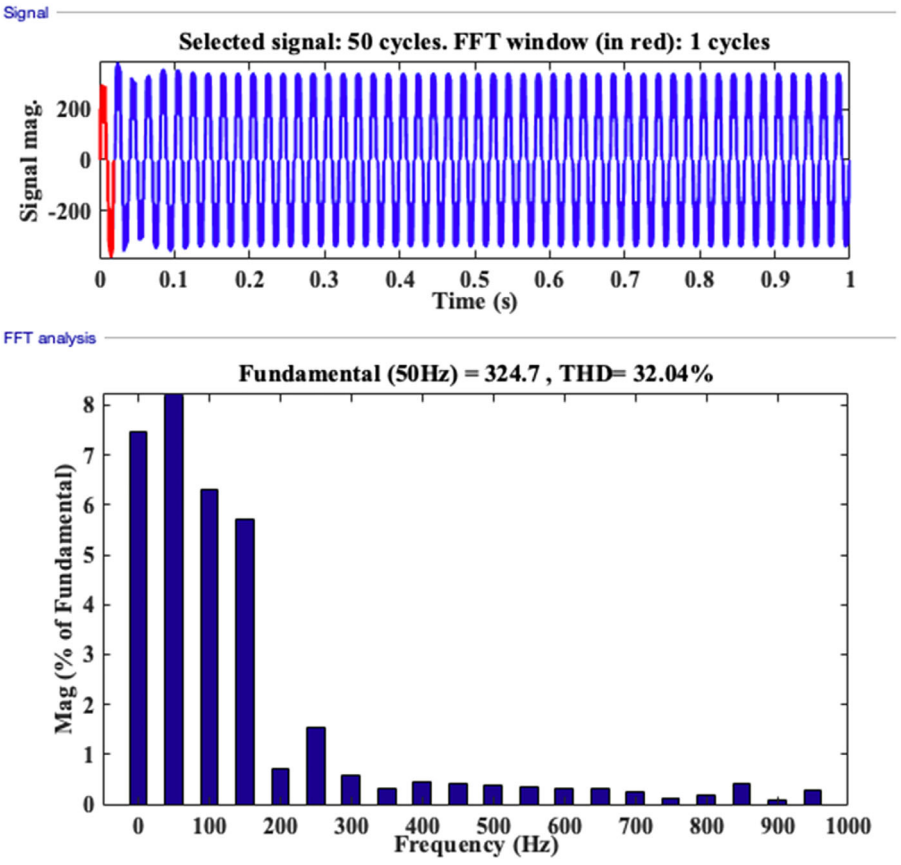

FIGURE 7 THD of phase voltage with FCS

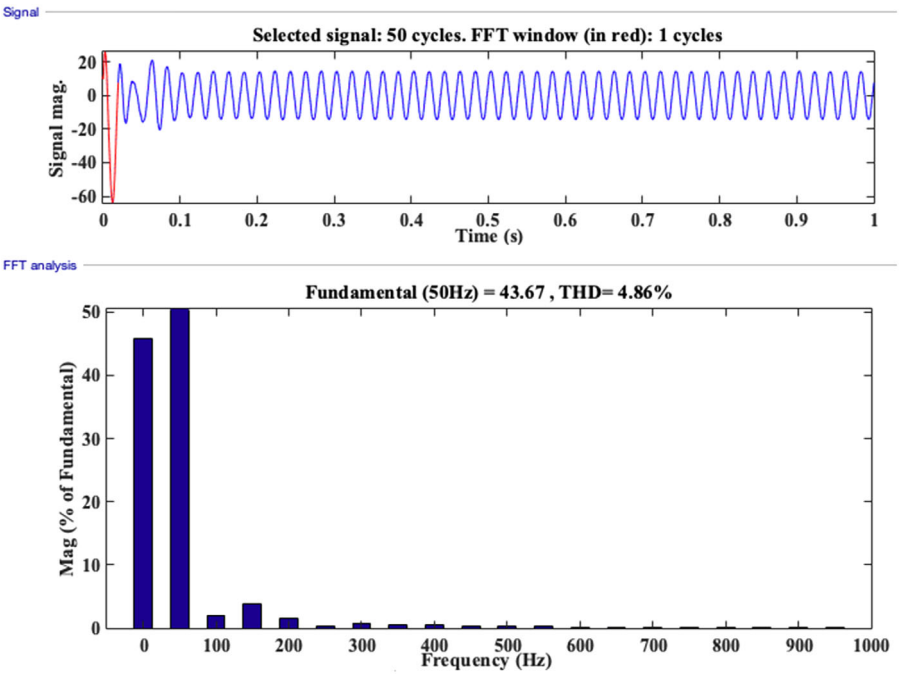

FIGURE 8 THD of phase current with FCS

Figures 14 and 15 show the total harmonic distortion (THD) for a constant DC source with respect to voltage and current is 15.10% and 1.97%, respectively. The component count of the proposed topology is compared with the existing topologies is illustrated in Table 3.

Furthermore, the proposed topology THD with respect to voltage and current is compared to existing

TABLE 3 Component count of the multilevel converter

Topology	DC sources	Flying capacitors	Clamped diode	Active switch	Total components
CHB[34]	4	0	0	16	20
NPC[35]	1	8	8	16	33
Active NPC[17]	1	3	0	12	16
FC[36]	1	7	0	16	23
Proposed topology	1	2	0	12	15

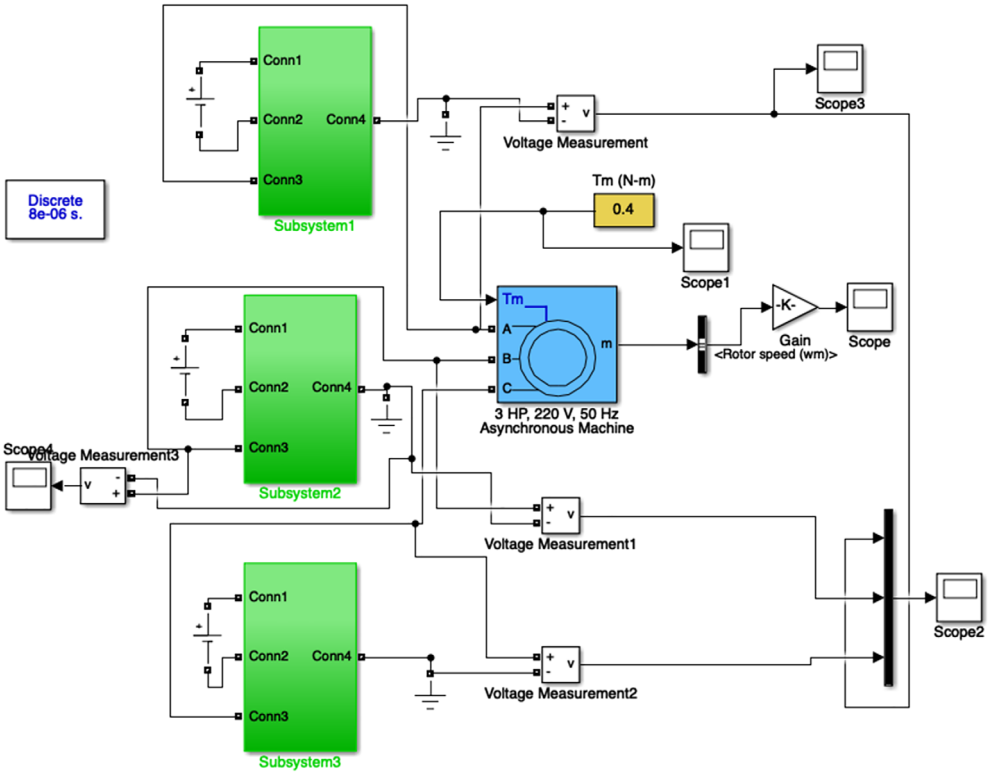

FIGURE 9 Proposed topology with constant DC source

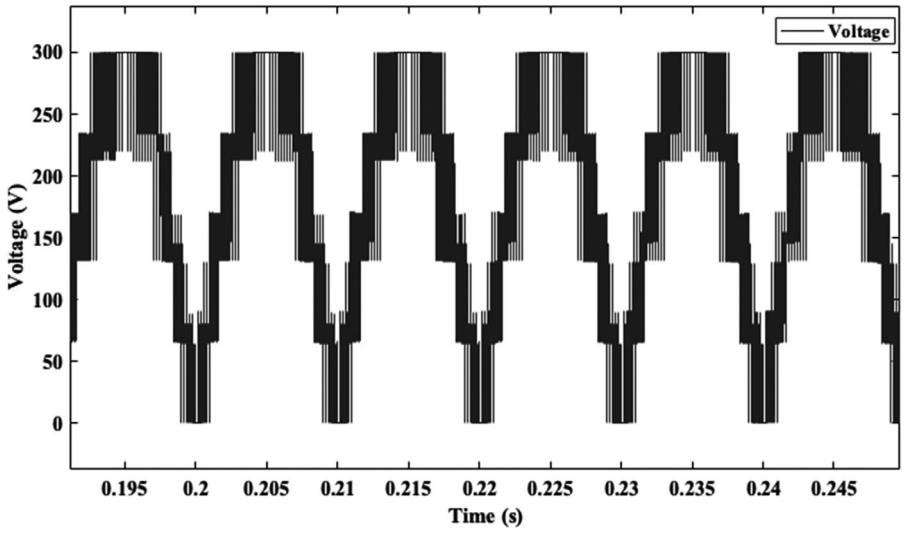

FIGURE 10 DC/DC converter voltage with constant DC source

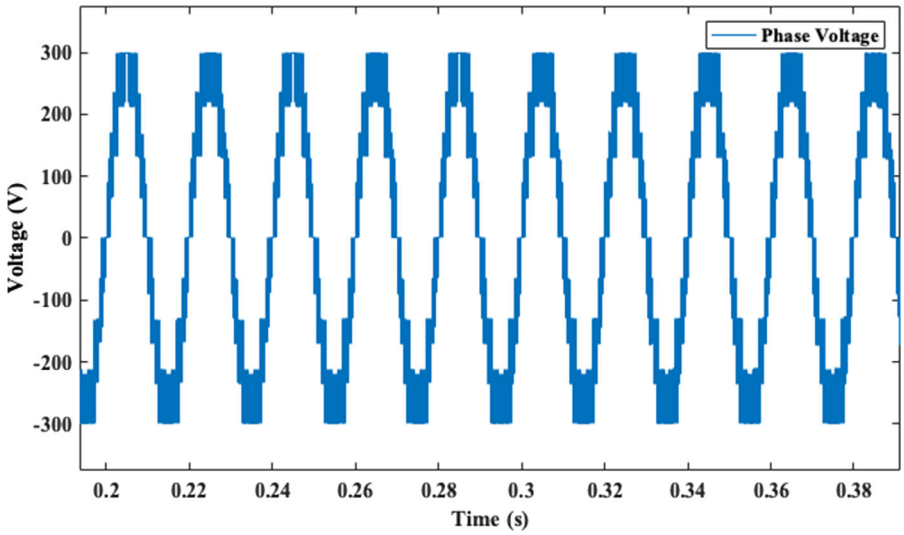

FIGURE 11 Nine level response per phase with constant DC source

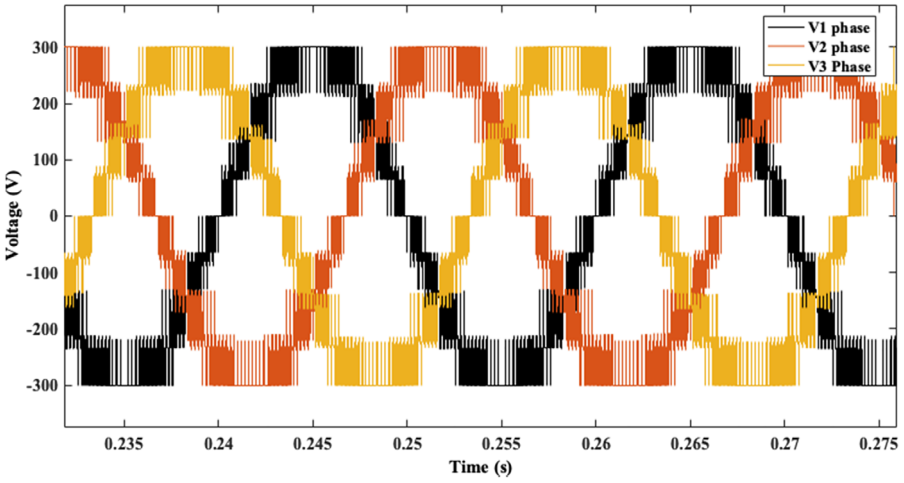

FIGURE 12 3-Ø nine level voltage response with constant DC source

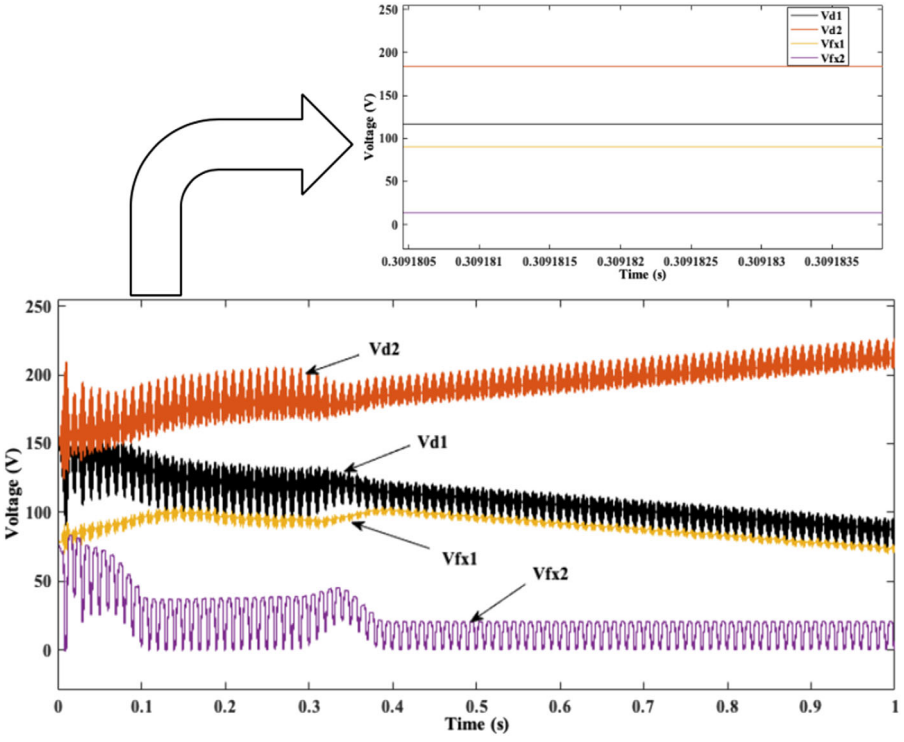

FIGURE 13 Voltage balancing of capacitors with constant DC source

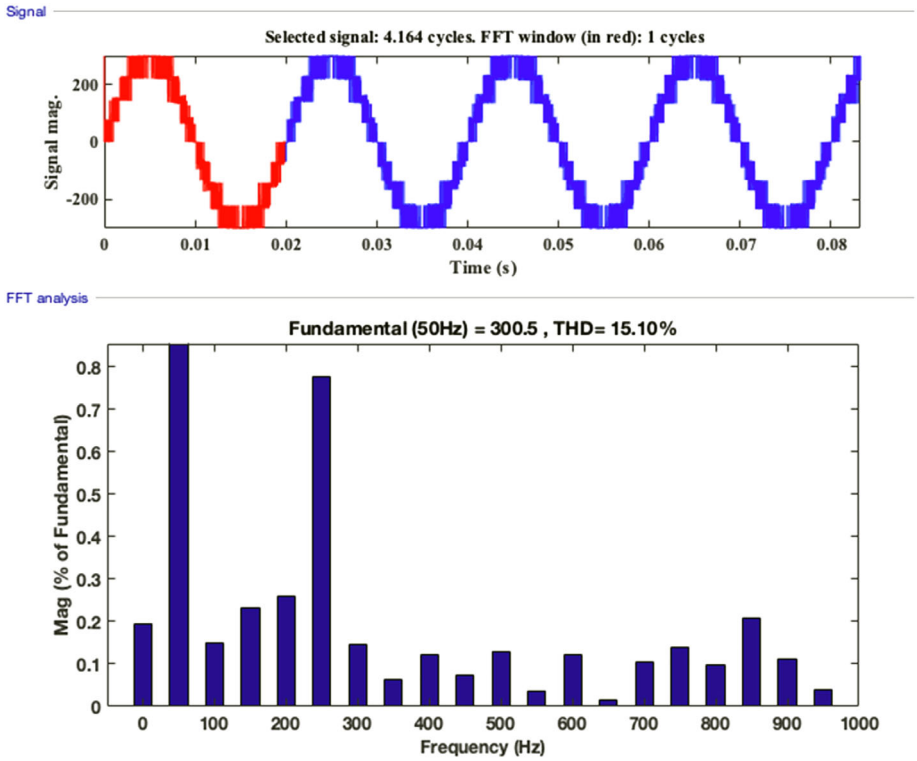

FIGURE 14 THD of phase voltage with constant DC source

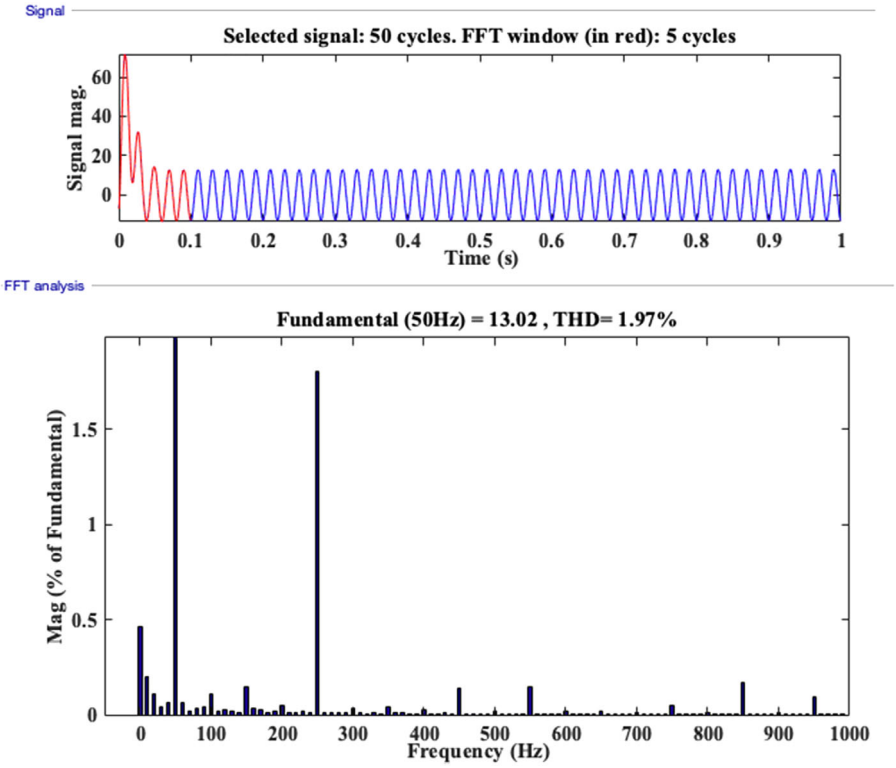

FIGURE 15 THD of phase current with constant DC source

topologies with a constant DC source and it is perceived that the among the multilevel converters with constant DC source the proposed converter has better performance as shown in Table 4.

The THD of the proposed converter with different sources is presented in Table 5, and observed that the proposed topology is appropriate for the constant DC source as compared to the FCS, so as to improve the

TABLE 4 THD of multilevel converters

Topology (with constant DC source)	THD of voltage (%)	THD of current (%)
CHB[34]	17.3	10.14
NPC[35]	36.62	8.92
Active NPC[17]	22.51	10.31
FC[36]	18.56	12.36
Proposed topology	15.10	1.97

TABLE 5 THD of the proposed converter with different sources

Topology	THD of voltage (%)	THD of current (%)
Proposed topology (with FCS)	32.04	4.86
Proposed topology (with constant DC source)	15.10	1.97

voltage and balancing the capacitors even though the component count is similar during both the sources.

5 | CONCLUSION

In this article, a symmetrical hybrid multilevel converter topology has been proposed. The proposed topology enhances the voltage levels of the converter for different sources by adopting a modified PS-PWM. The proposed topology is ideal for generating multilevel voltages with a constant DC source and a fuel cell source. The total harmonic distortion of the proposed converter with respect to voltage and current is 15.10% and 1.97%, respectively, shows better performance compared to the fuel cell source and the existing topologies with constant DC source. The proposed topology has small number of component count as related to existing topologies. Therefore, the proposed topology is more appropriate for a constant DC voltage application.

ACKNOWLEDGMENT

This project is supported by University Malaysia Pahang (UMP) and Mr A. S. Veerendra is working under UMP's Doctoral Research Scheme (DRS).

CONFLICT OF INTEREST

The authors declare no potential conflict of interest.

ORCID

Arigela Satya Veerendra https://orcid.org/0000-0001-5296-1936

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How to cite this article: Veerendra AS, Mohamed MR, Sulaiman MH, Leung PK. Modeling and analysis of hybrid multilevel converter for constant DC and fuel cell sources. *Energy Storage*. 2020;2:e193. https://doi.org/10.1002/est2.193