DESIGN OF OPTIMAL NANOSCALE CHANNEL DIMENSIONS OF FINFET BASED ON CONSTITUENT SEMICONDUCTOR MATERIALS

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ABSTRAK

Aplikasi Nanoelectronic telah mendapat manfaat yang sangat besar daripada kemajuan besar dalam industri teknologi Nano yang baru muncul. Penurunan nilai yang besar dari dimensi transistor telah membolehkan penempatan lebih dari 100 juta transistor pada satu cip sekali gus mengurangkan fungsi peningkatan kos dan prestasi litar bersepadu (IC) yang dipertingkatkan. Walau bagaimanapun, kajian untuk mengurangken saiz transistor konvensional aken menjadi sanjat mencabar kerana kebocoran elektrostatik dan isu fabrikasi lain. Fin Field Effect Transistor (FinFET) menunjukkan potensi besar dalam penskalaan saiz dan pembuatan sebagai calon yang menjanjikan teknologi nano-oksida-semikonduktor (CMOS) pelengkap nanoscale. Struktur FinFET menyediakan kawalan elektrik yang lebih baik ke atas konduksi saluran dengan itu ia telah menarik minat yang luas dari para penyelidik dalam kedua-dua akademik dan industri. Walau bagaimanapun ,ianya secara agresif menurunkan dimensi saluran terutamanya panjang saluran akan menurunkan prestasi keseluruhan akibat kesan saluran pendek yang merugikan (SCEs). Tujuan kajian ini adalah untuk mengkaji dan menganalisis ciri-ciri elektrik pelbagai jenis transistor FinFET (Si GaAs Ge dan InAs) berdasarkan dimensi saluran untuk mengenal pasti had pengukuran fizikal optimum untuk prestasi transistor terbaik. Kajian komparatif berasaskan simulasi TIGA (3) parameter berubah-ubah: lebar panjang dan ketebalan oksida saluran dijalankan. Kesan mengubah dimensi saluran pada prestasi setiap jenis FinFET dinilai berdasarkan EMPAT (4) ciri elektrik iaitu; (i) Nisbah I_{ON} / I_{OFF} (ii) Tegasan Ambang Swing (SS) (V_T) dan Pengurangan Barrier-induced Drain (DIBL). Alat simulasi MuGFET yang terkenal untuk struktur FET pelbagai pintu gerbang nano digunakan untuk menjalankan simulasi percubaan di bawah syarat-syarat yang dipertimbangkan. Dimensi saluran optimum untuk prestasi terbaik dari semua jenis FinFET yang dipertimbangkan telah dicapai pada faktor skala minimum K = 0.125. Selain itu Si-FinFET mengatasi GaAs-FinFET dan kedua-duanya mengekalkan prestasi unggul dari segi nisbah I_{ON} / I_{OFF} dan nilai SS berbanding dengan dua jenis FinFET yang lain. Sebaliknya prestasi Ge-FinFET telah direndahkan dan mencapai nisbah I_{ON} / I_{OFF} paling rendah manakala ciri-ciri terburuk dari segi nilai SS (94 mV / dec) telah berlaku pada InAs-FinFET. Hasil penyelidikan menyumbang ke arah menganalisa had skala dan dimensi saluran penurunan tahap FinFET sebagai pengganti berpotensi untuk transistor planar dan memahaminya lagi prestasi mereka untuk mengurangkan kebocoran semasa dan masalah SCE lain.

ABSTRACT

Nano-electronic applications have benefited enormously from the great advancement in the emerging Nano-technology industry. The tremendous downscaling of the transistors' dimensions has enabled the placement of over 100 million transistors on a single chip thus reduced cost, increased functionality and enhanced performance of integrated circuits (ICs). However, reducing size of the conventional planar transistors would be exceptionally challenging due to leakages electrostatics and other fabrication issues. Fin Field Effect Transistor (FinFET) shows a great potential in scalability and manufacturability as a promising candidate in nanoscale complementary metal-oxide-semiconductor (CMOS) technologies. The structure of FinFET provides superior electrical control over the channel conduction, thus it has attracted widespread interest from researchers in both academia and industry. However, aggressively scaling down of channel dimensions, mainly the channel length, will degrade the overall performance due to detrimental short channel effects (SCEs). The aim of this study is to design optimal Nano-dimensional channel of FinFET based on electrical characteristics and semiconductor material (Si GaAs Ge and InAs) to overcome dimensions shrunk down issues and ensure the best performance of FinFETs. This was achieved by proposing a new scaling factor, *K*, to simultaneously shrinking the physical scaling limits of channel dimensions for various FinFETs without degrading their performance. A simulation-based comprehensive comparative study depending on FOUR (4) variable parameters: length, width and oxide thickness of channel in addition to scaling factor were carried out. The impact of changing channel dimensions on the performance of each type of FinFETs was evaluated base on FOUR (4) electrical characteristics namely; (i) I_{ON}/I_{OFF} ratio (ii) Subthreshold Swing (SS), (iii) Threshold voltage (V_T), and (iv) Drain-induced barrier lowering (DIBL). The well-known MuGFET simulation tool for nano-scale multi-gate FET structure is utilized to conduct experimental simulations under the considered conditions. The obtained simulation results showed that the optimal channel dimensions for best performance of all considered FinFETs types were achieved at a minimal scaling factor K = 0.125 with 5 nm length, 2.5 nm width and 0.625 nm oxide thickness of channel. Furthermore, Si-FinFET achieved the highest I_{ON}/I_{OFF} ratio (up to 2.12×10^8) and outperformed GaAs-FinFET, and both maintained a superior performance in terms of I_{ON}/I_{OFF} ratio and SS value compared to the other two types of FinFETs. In contrast, the Ge-FinFET performance was degraded and reached the lowest I_{ON}/I_{OFF} ratio (2.29×10^5), whereas the worst characteristics in terms of SS value (94 mV/dec) occurred with InAs-FinFET. The obtained results introduced new limits with enhancing FinFETs performance in terms of the investigated characteristics. The outcomes of this research contribute towards new channel nano scaling limits of FinFETs as potential successors to planar transistors in nanoscale devices and nanotechnology applications, and further analysing the electrical characteristics of FinFETs with reducing leakage current and overcoming SCEs.

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LIST OF SYMBOLS

D	Drain
DIBL	Drain induced barrier lowering
I	current
I_d	Drain current
I_{OFF}	OFF Current
I_{ON}	ON current
K	Scaling factor
K_B	Boltzmann's coefficient
L	Length of the channel
Q	Electron charge
R_{OUT}	Output resistance
S	Source
SS	Subthreshold Swing
T	Temperature
T_{OX}	Oxide thickness
V	Voltage
V_d	Drain voltage
V_{DD}	Drain DC voltage source
V_{DS}	Drain to source voltage
V_{GS}	Gate to source voltage
V_T	Threshold voltage
W	Width of the channel

LIST OF ABBREVIATIONS

CPU	Unit processing of the central
DELTA	Depleted lean channel transistor
FDSOI	Full-Depleted Silicon
FDSoI	Depleted Silicon On Insulator
FET	Field Effect Transistor
FinFET	Fin-shaped field effect transistor
GAA	Gate all around
GaAs	Gallium Arsenide
GaN	Gallium Nitride
Ge	Germanium
GIDL	Gate-induced drain leakage
IC	Integrated Circuits
InAs	Indium Arsenide
JFETs	Junction field effect transistor
MOSFET	Metal-Oxide-field-effect transistor
MuGFET	Multi-Gate-Field Effect Transistor
NW	Nanowire
PDSOI	Partially-Depleted Silicon
Rsd	Resistance source drain
SCE	Short channel effect
Si	Silicon
SiC	Silicon Carbide
SiNWT	Silicon nanowire transistor
SOI	Silicon on insulator
VLST-TSA	Technology Systems and Application

CHAPTER 1

INTRODUCTION

1.1 Background of Study

Nowadays, the application of nanoscience and its inherent technology has been extensively used in interdisciplinary research most especially for the past two decades. The concept of nanotechnology involves the use of low dimensional materials with different structural configurations which include the nanowires, Nano-rods, Nano photo laser production , nanotubes or Nano-crystalline films (Harikrishnan, 2018). This has therefore attracted interest in many sciences and engineering fields. It is pertinent to know that materials within the range of one to hundred nanometres exhibit the nanoparticle characteristics of bulk samples from the same material.

It is important to describe the system of units and how small Nano-materials are; which is one-billionth of a meter. Examples of these include a strand of approximately 2.5 nanometres human DNA, and human hair (8-10 × 10^4 nm). The characteristics of these materials include a larger surface area, lower thermal properties, higher electrical resistivity, higher specific heat capacities, excellent magnetic properties and thermal expansivities (Bouville et al., 2014). These properties are responsible for their various applications in medical, biotechnology, bioremediation, solar cell catalysis, separation processes, and in its laser recent application in cancer therapy as illustrated in Figure 1.1.

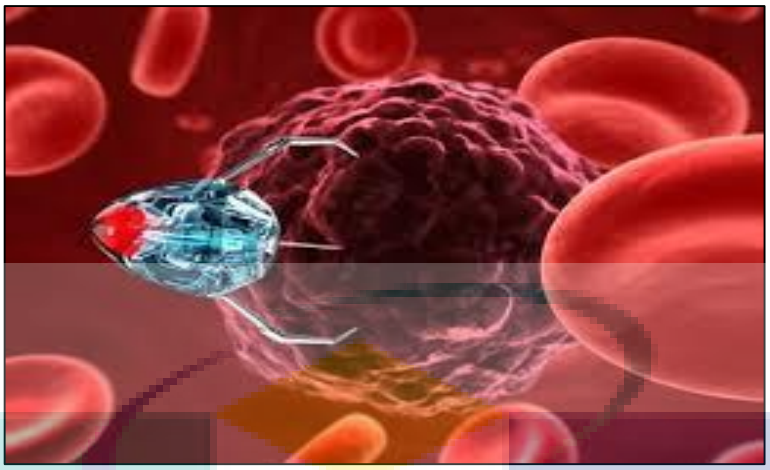

Figure 1.1 Nanomedicine in cancer therapy laser
Source: Wu (2017)

Many researchers and engineers have made lots of efforts on the discovery of different varieties of nanoscale materials such as the field-effect transistor (FET) devices. That application is largely due to the improved properties of these materials which include greater strength, lighter weight, and higher resistance to chemical reactions. In recent years, the uses of FET transistors are widely prevalent in many integrated circuits (ICs). This has therefore provided a great impact on the production of many electronic devices. The application of FET is largely based on the concept of the attraction of charges within a semiconductor channel (Ferrari et al., 2015). The FET comprises of a semiconductor channel coupled with electrodes at either end of the drain and the source. The gate is a control electrode which with a close proximity to the semiconductor channel. The configuration for electric charge effects enables the gate from the FET to effectively control the flow of electrons or holes (i.e. carriers) from source to the drain. The flow of these carriers is achieved by controlling the size and shape of the semiconductor channel (Su, 2011).

There is P-type or N-type of the conductive channel where the current flow occurs which results in two categories of FET known as P-Channel and N-Channel. One is the joining type FET (JFET: Junction gate FET) while the other one is MOSFET (Metal Oxide Semiconductor FET) which is the latest and the most common. MOSFET is manufactured mostly from Si and other materials such as SiC, GaAs, GaN and InGaAs ((Личевская, et al., 2015). The transistors classification can be understood by observing the tree diagram as shown in Figure 1.2.

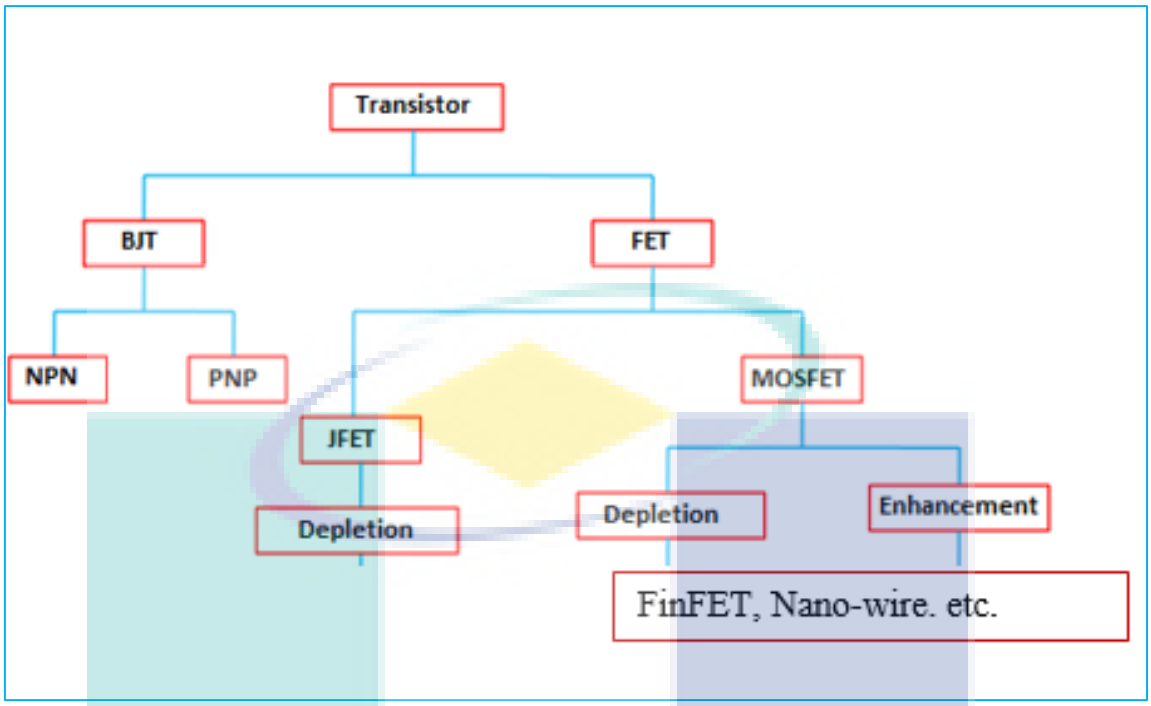

Figure 1.2 The field effect transistor family tree
Source: Schwierz (2010)

New FET structures are being explored on a large scale with one of the structures such as the FinFET, which are described as MOSFET built on a material where the gate is supported by two-to-four channels or configured by to form a dual gate structure. The FinFET technology was derived from the fact that the structure used likes like a group of fins when viewed this form of the gate structure. This described a double-gate non-polar transistor built upon an SOI substrate (Yang 2018). This form provides an improved electrical control on channel delivery and helps to reduce current leakage levels and overcome some other short channel effects (SCEs) (Murray et al., 2013); Alvarado et al., 2013). The FinFET devices have significantly faster switching times and higher current density than the mainstream CMOS technology. This transistor structure has attracted widespread interest from researchers in the fields of industry and academic studies of semiconductors (Ghoneim & Hussain, 2015). Mack, (2015) reported that in every three years there is a makeable similarity in the quadrupling of devices in a chip and improved performances of the transistor as stated in Moore's Law. Figure 1.3 illustrates the structures of MOSFET and its modified version, three dimensions FinFET (3-D FinFET).

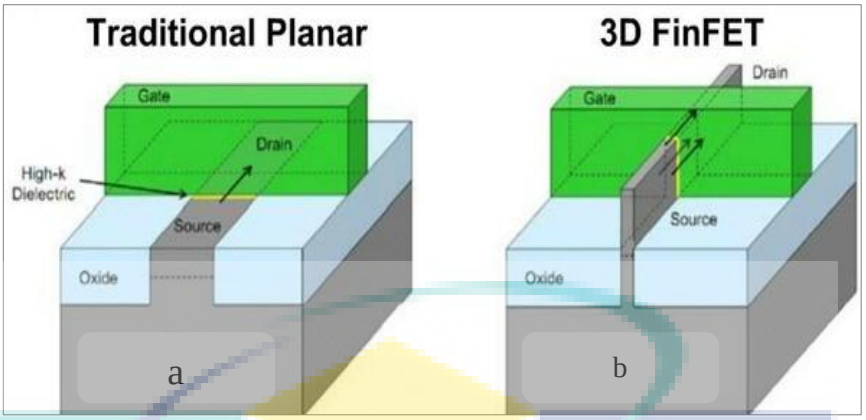

Figure 1.3 (a) 2-D planar transistor MOSFET (b)3-D Tri-Gate transistor FinFET structure
Source: Goettler & Gordon (2011)

Moreover, the Dennard's scaling law states those transistors become faster and consumes less power and are cheaper to manufacture as they become miniature into a smaller form (Flamm, 2018). Scaling down of transistor from large dimensions to smaller dimensions has led to the emergence of ICs production. This could be traced to the need for minimizing the transistors into some basic units into smaller IC chips. As a result of the size minimization, which at present has reached 0.1 microns, in the past 40 years, the MOSFET transistor has transformed to be the basis in the micro-electronic manufacture of many computing devices. The reduction of transistors into a miniature entity with dimensions far below 100 nm has helped in the re-coupling and integration of many transistors to be on a single chip (Tummala, 2012) as shown in Figure 1.4.

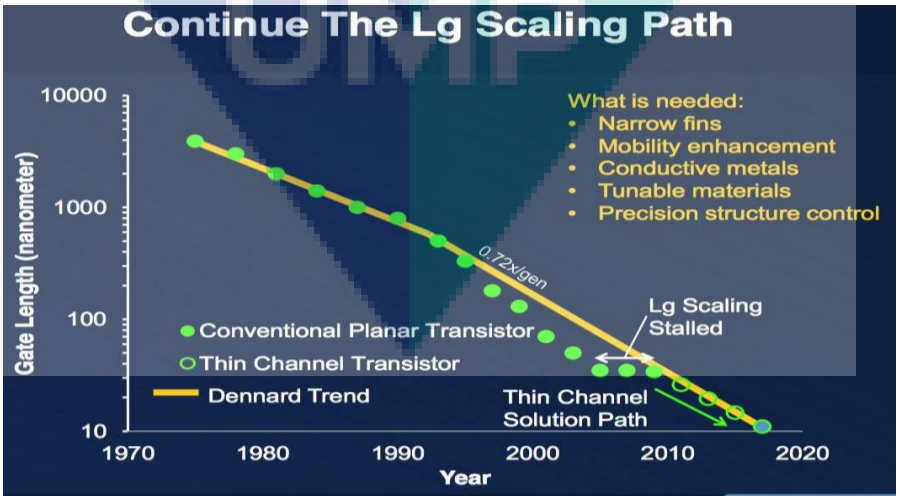

Figure 1.4 Industry Scaling Trend Over the Year
Source: Rana (2017)

These integrations of several circuits have greatly improved the function and reduced cost to many semiconductor industries. The reduction of production cost has therefore aided the speed of transferring data and an overall processing time and computing power (Dennard et al., 2018). This has invariably enabled the simultaneous performance of multiple tasks which is the merit of scaling the transistor However, the researchers are investigating several alternatives to the transistor for ultra-dense circuitry reached to tens of nanometres. This science is called nanotechnology such as the latest FinFET technology demonstrated by Intel company at channel length 10-nm in 2017 (Mistry, 2017).

1.2 Problem Statement

There has been a great improvement in the performance, speed, and density through the scaling-down of transistors from a larger dimension to miniature dimensions (Franklin 2015). As planner MOSFETs continue to shrink in size toward higher circuit density, the adverse consequences arising from (SCEs) become progressively important. Thus, it became difficult to follow Moore's law and scale down further with the planar MOSFET devices. Many techniques had been introduced to keep this trend alive to allow more nodes that are advanced. In addition, power dissipation of nanoscale devices is becoming a major concern with the current market scenarios and it has increased drastically with scaling down transistor as in Figure 1.6 (Rana, 2017)

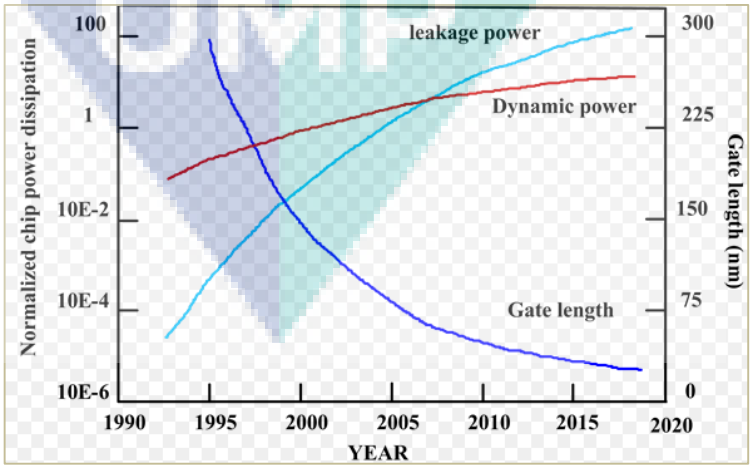

Figure 1.5 Power Dissipation with Technology Scales over years
Source: Bikki & Karuppanan (2017)

Some of the constraints that led to energy dissipations and other problems could be traced to an increase in current gate leakage due to the quantum mechanical tunnel of the tankers through the thin gate. The oxide I_{OFF} increases due to the quantum mechanical tunnel of the tankers from the source to the MOSFET drain. The lower I_{ON}/I_{OFF} ratio is as a result of a reduced density control and dopant atoms location in channel and source/drain region. Another merits is the Subthreshold Swing (SS), which is defined as the change in the voltage of the gate (V_G) required to change the order of the amount of current from state to state (Dennard et al., 2018). The SS is controlled in MOSFET by diffusing the thermal emission carrier across a thermal barrier and has an ideal value of not less than 60 mV/dec at room temperature. Thus, the further reduction of MOSFET is very difficult without a significant increase in I_{OFF} and SS values (Fiori et al., 2014). Driving by the needs to overcome these issues, researchers have generated many plots depicting scaling trends over the years showing the limit of critical dimension. More FETs that are new are explored on a large scale. A substantial attention is being dedicated toward the fabrication MOSFET with of vertical channel such as on an SOI wafer, which is often characterized as a FinFET. The FinFETs have a potential to be fabricated with channel length of less than 25 nm as they can provide high drive current and high immunity to SCEs. The FinFET structure has attracted wide interest from both industry and academia. Such structures provide a good control and help to reduce current leakage levels and overcome some other effects of short channel (Desai et al. 2016).

In order to reduce channel dimensions and improve performance of FinFET design, there is a need for simulate and characterize FinFET behaviour to help in decision-making. Over the last decade, there have been many types of research focusing on the manufacture of FinFETs in various nanoscale devices such as semiconductor materials, insulation materials, and various manufacturing techniques that are developed to predict the performance of FinFET (De'nan et al., 2017). Nevertheless, those researches did not focus on the comprehension of the subject in full form. For example, some studies focused on one channel dimension either length, width or oxide thickness depending on only one metric such as I_{ON}/I_{OFF} or SS, and for one semiconductor material such as Si-FinFET or Ge-FinFET. Hence, the lack of qualitative and quantitative characterization studies on FinFET as a successor to conventional planar

devices is one of the major issue to understanding the electrical characteristics of FinFETs based on their channel dimensions and semiconductor materials.

As aforementioned, there are many challenges in scaling trend of the conventional planar transistors; these include problems of leakages electrostatics and other fabrication issues. This is because downscaling of channel dimensions results in the degradation of the transistors. This culminates into the reduction of I_{ON} /I_{OFF} ratio due to the increase of leakage current thus leads to a large dissipation of energy. It also leads to an increase sub-threshold swing value thus slowing down devices. The FinFET, therefore, presented a great potential in scalability and manufacturability as a promising candidate in nanoscale CMOS technologies. However, the downscaling of FinFET channel dimensions cannot be performed arbitrary or in adhoc manner. Furthermore, the constituent semiconductor materials such as (Si, Ge, GaAs, and InAs) therefore have a tremendous impact on FinFETs performance due to short-channel effects Therefore, it is necessary to investigate the individual impact of each dimension of channel on the performance of different FinFETs based on semiconductor materials, and further analyse the impact of simultaneous downscaling of the three channel dimensions (L, W, and T_{OX}) based on scaling factor.

1.3 Research Objectives

The objectives of this study are stated below:

i. To analyse the electrical characteristics (i.e. I_{ON}/I_{OFF}, SS, $V_{T,}$ and DIBL) of FinFET transistors based on channel's dimensions (Length, width, and oxide thickness) and semiconductor materials (Si, Ge, GaAs, and InAs).
ii. To propose a new scaling factor (K) for scaling down channel dimensions simultaneously without degrading FinFET performance.
iii. To design a FinFET structure with optimal channel dimensions and semiconductor material according to the best performance characteristics.

1.4 Scope of Study

This study is simulation-based which used Multi-Gate-Field Effect Transistor (MuGFET) simulation tool to produce the output characteristics of FinFETs, and it is

limited to the considered parameters and FinFET types. It focuses on investigating the impact of shrinking dimensions of channel (L, W, and T_{ox}) on electrical characteristics of four (4) types of FinFET transistor types (Si, Ge, GaAs and InAs). The performance evaluation of FinFETs in this research is based on four (4) electrical characteristics, which are I_{ON}/I_{OFF} ratio, SS, V_T, and DIBL. Depending on the highest I_{ON}/I_{OFF} and the nearest SS to the ideal value, the best Nano-dimensions of channel and semiconductor FinFET type were selected.

1.5 Thesis Organisation

This thesis is organized into five chapters as follows:

Chapter 1 introduces the framework of this study including research background with emphasis on FinFET transistor followed by problem statement. Also it introduces the research objectives and scope of the research work. The chapter ends with thesis organisation.

Chapter 2 presents a background of the FETs transistors including types, features and applications. It followed by overview of FinFETs and its electrical characteristics. It also provides a review of SCEs, Moor's law, FinFET design and fabrication issues. Finally, chapter ends with highlighting the most related works.

Chapter 3 introduces the adopted methodology in the research, hypothetical and theoretical background. Moreover, this chapter describes procedures, formulas, and simulation design and performance metrics.

Chapter 4 presents the simulation results and discussion. It describes the impact of varying channel dimensions individually and simultaneously on the electrical characteristics of various FinFETs. The changes in I-V electrical characteristics are compared and analysed based on channel dimensions, scaling factor and semiconductor types. Also, the main findings are properly elucidated.

Chapter 5 comprises the conclusions drawn from the work presented in this thesis and it highlights the significance of research, in addition to recommendations and potential trends for future work that can guide for further research.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In this chapter an overview of Nanotechnology and its future implications is presented including, Field-Effect Transistors with their limitations along with Moore's Law and scaling trends of transistors. Then Fin Field Effect Transistors with their advantages and fabrication process is described. This is followed by an overview of the different electrical characteristics and semiconductor materials of transistors. Effects of constituent semiconductor materials on the performance of FinFETs is also highlighted Finally, this chapter as well presents a survey on the most recent studies that investigated the impacts of shrinking channel dimensions on the FinFETs performance. Discussion on research gap and drawbacks of the considered studies with possible solutions are also summarized.

2.2 Overview of Nanotechnology and its Future Implications

The ideas of Nano-science and nanotechnology emanated long ago from the concept promulgated by Richard Feynman at the California Institute of Technology (CalTech). Feynman in his description of the concept put forward a scenario in which researchers can manipulate and control materials at atomic and molecular level. This concept was thereafter christened nanotechnology by Professor Norio Taniguchi in his quest to further explore the ultra-precision machining process. The emergence of a scanning tunnelling microscope in 1981 clearly revealed the application of nanoscience for individual atoms at a molecular level (Hey, 2018).

Nanotechnology is therefore defined as the manipulation of atomic matter on a molecular and super-molecular level (Keyser, 2016) reported the molecular nanotechnology as the atomic or molecular manipulation which results in the fabrication of products on a macro scale. The National Nanotechnology Institute (NNI) further provided a generalized description of nanotech as the manipulation of matter with at least 1-dimension sized from one to hundred nanometres. This definition is a total deviation from the traditional technological point-of-view to a more research-oriented category, which deals primarily with the special properties of matter below a certain size threshold. It is a common practice to therefore to pluralize this miniaturization as form "nanotechnologies" as well as "Nano-scale technologies". This indicated a wide range of research applications with size as the target variable. Many countries have therefore invested more in nanotechnology-related research due to several potential military and industrial applications. (Snodgrass et al., 2013), reported that the United State of America investment through the National Nanotechnology Initiative was put at around $3.7 billion, while the European Union and Japan invested $1.2 billion and $750 million, respectively as presented in Figure 2.1.

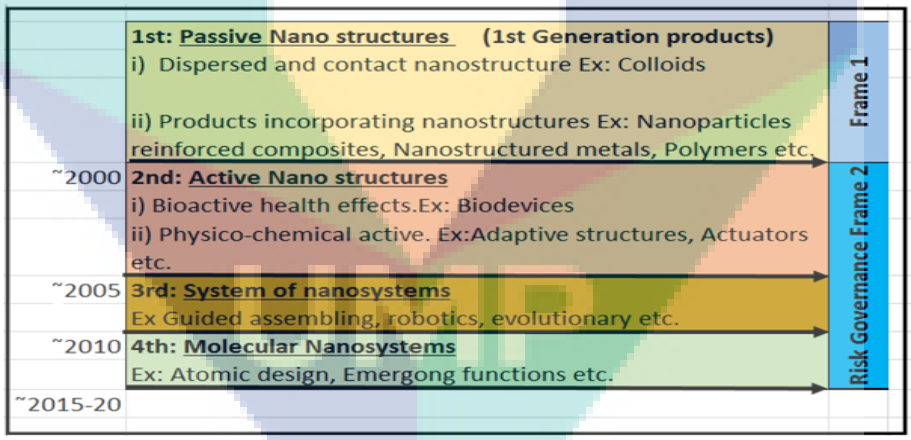

Figure 2.1 Timeline History of Nanotechnology
Source: Snodgrass et al., (2013)

This concept is therefore defined by size and it is applied in different fields of science such as in energy storage applications micro fabrication, molecular engineering. Most of the research applications of nanotechnology range from the extensions of the traditional device to a new approach which are completely based on molecular self-assembly (Wei et al., 2017). The future of nanotechnology has been a major point of discussion by many researchers with the foresight of leading to the development of

entirely new materials and devices which could useful in different application such as in Nano-medicine, Nano electronics, biomaterials, and energy production as shown in Figure 2.2.

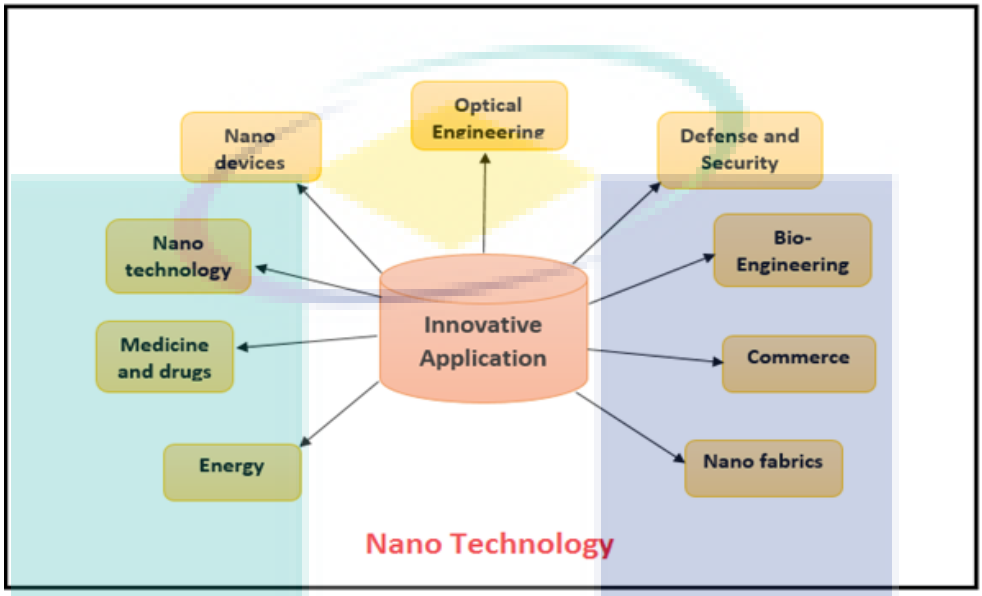

Figure 2.2 Application of Nano-electronics
Source: Dong, et al., (2013)

However, there has been a concern about the hazard and the impact of nanomaterials on the environment with potential speculation about the doomsday scenario of this miniature material which has invariably cast doubt if they are really worth it (Gardea et al., 2014).

2.3 The Field-Effect Transistor

Julius Edgar and Oskar Heil were the first to patent the FET in 1926 and 1934, respectively. However, the JFETs semiconducting devices were thereafter developed about two decades after the patent by the team of William Shockley at Bell Labs in 1947 after the observation on the transistor effects. The first of JFETs was the SIT, invented by Jun-ichi Nishizawa and Y. Watanabe in 1950. The SIT is characterized by a short channel length (Shenai et al., 1989). The MOSFET, which is more advanced than JFET, is ore renowned in the development of digital electronic as invented by Dawon Kahng and Martin Atalla. The current is usually carried mainly by the majority-carriers or minority-carriers in a device in which current flows using the former as reported by

(Uddin et al., 2015). This device is made up of an active channel from where the electrons or holes flow from the source to the drain, which is the two terminal conductors, connected through ohmic contacts to the semiconductor. The ability of the active channels to conduct these carriers is dependent on the applied potential across the gate and source terminals. There is three type of terminals in the FETs these include the source, drains, and the gate. The carriers (electrons and holes) enters the active channels through the source and its designated with 'IS', while the carriers leaves the channel through the drains designated by 'ID'. The gate terminal modulates the channel conductivity and it is designated by 'G'. The application of voltage to the gate (G) controls the ID. The n-type and p-type semiconductor is produced from the FET-channel doping. In the case of FETs mode enhancement, the drain and source are doped to the active channel of the opposite or similar type in relation to the depletion FETs mode. The insulation type between the gate and active channel are also used to categorize the field-effect transistors. Figure 2.3 shows the different type of field-effect as describe.

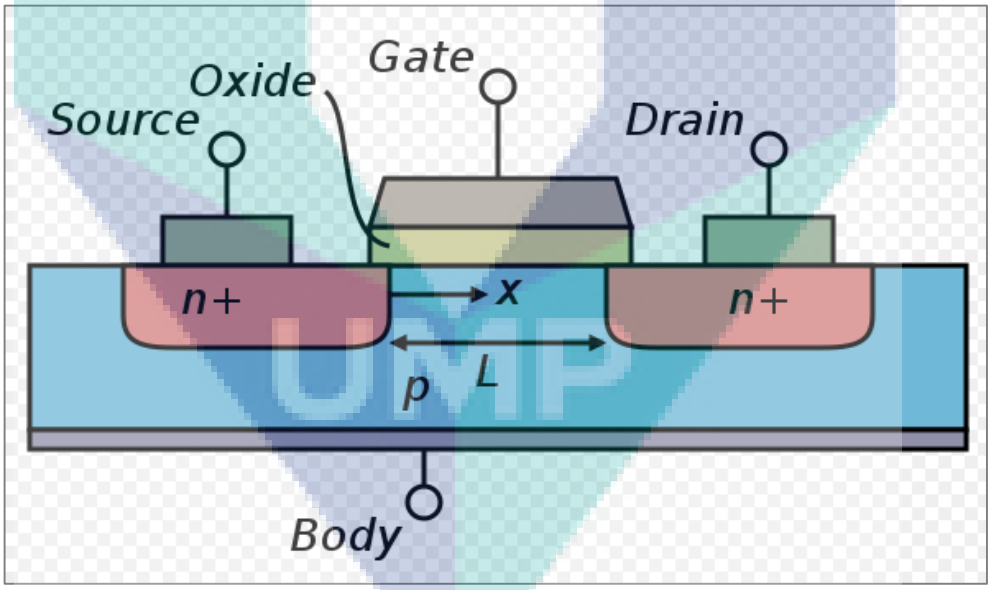

Figure 2.3 Cross-section of an n-type MOSFET
Source: Sakakibara et al., (2008)

2.3.1 Types of the Field-effect Transistor

In the reverse-biased p–n junction is employed for the separation of gate (G) from the main channel. An insulator (usually SiO2) is introduced in the MOSFET

between the main channel and the gate (G). However, in the metal–nitride–oxide–semiconductor (MNOS) transistor the nitride-oxide layer is used as an insulator. Moreover, the dual-gate MOSFET is made of two-played two insulated gates. The depleted FET on the other hand simultaneously amplified the sensor and the memory nodes and therefore acts as photon sensor. A Shetty barrier is used to replace the p-n junction in the JFET to form the metal–semiconductor field-effect (MESFE) transistor. This is usually applied in Gallium arsenide and type III-V semiconductor devices. The nanoparticle organic memory is another type of FETs. Ruzyllo, (2016) reported the use of a graphene nanoribbon FETs which uses a graphene nanoribbon for its active channel. The vertical-slit FETs also is made up of is a square-shaped with a characteristics narrow slit which connects the source and drains at opposite corners. The current is controlled by the gates at this corner through the slit as described by (Ruzyllo, 2016). In addition, the graphene-based FETs are very sensitive transistors that are commonly employed as biosensors and chemical sensors. The higher sensitivity and physical properties of these graphene-based transistors are as a result of its two-dimensional structure which also helps in the reduction of instances of 'false positives' in sensing applications (Cai et al., 2014).

2.3.2 The Metal-Oxide-Semiconductor-Field-Effect-Transistor

The MOSFET is the fundamental of modern very-large-scale-integrated (VLSI) circuits. The appearance of complementary metal-oxide-semiconductor (CMOS) made the rapid growth of the electronics industry. However, since around 1990 to prevent device size scaling several device topological structures were researched to replace the traditional bulk CMOS structure. The reason why electrical engineers do so much research efforts to invent new device structure is that as the technology node keeping scaling the industry begins to face several problems associated with the device scaling (Arora, 2012). For example, before the technology node approaching 180-nm leakage power consumption was not recognized as a big issue. However, for 90-nm or 65-nm technology node, the influence of sub-threshold leakage current became to be momentous because of the large transistor density (Weste & Harris, 2010). Even though the sub-threshold leakage current of one single transistor is really small which only reaches the level of nm? Also since the process technology node reaches 45-nm the gate leakage has been another big issue for controlling power consumption as well as the

subthreshold leakage current To, therefore, keep scaling the size of transistors not only the FinFET was proposed but also another device structure named ultra-thin-body silicon-on-insulator (UTB SOI) MOSFET was presented by Professor Chamming Hu and his colleagues at the same time (Furber, 2017). The structure of UTB SOI MOSFET is shown in Figure 2.4.

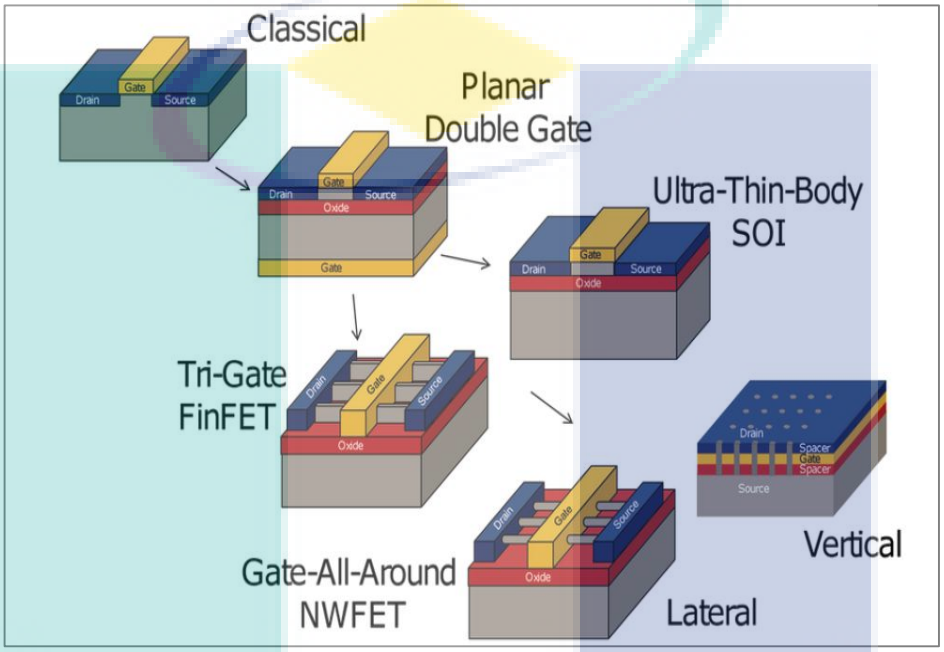

Figure 2.4 The Evolution of the FET Architecture
Source: Furber (2017)

For UTB SOI the near intrinsically- doped body refrains from the dopant number fluctuation effect which helps the size of transistors keeping scaling. In addition, this kind of structure can remove the punch through. However, the BSIM (Berkeley Short-Channel IGFET Model) Group who was led by Professor Chamming Hu and Professor Sayeef Salahuddin focused on the structure of FinFET instead of UTB SOI MOSFET because it has a better prospect than UTB SOI MOSFET. The FinFET Structure as shown in Figure 2.5 improves performances significantly (Sriramkumar et al., 2013).

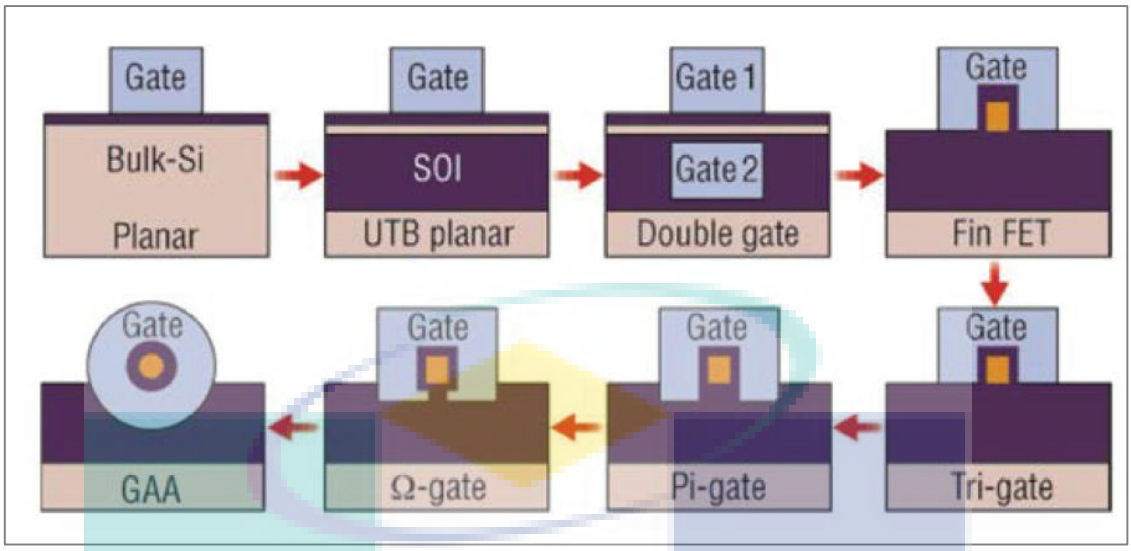

Figure 2.5 Improvements from planar MOSFET to GAA FET
Source: Yang (2018)

2.3.3 The Short Channel Effects

As the sizes of the transistors are miniature, the length of the channel will have the magnitude order that is the same as the width of source and the drain depletion layer. The close proximity between the source and channel reduces gate control and causes undesirable effects called as "Short Channel Effect" (SCE). These effects include the DIBL where drain bias can modulate the drain current (Xie, Xu, & Taur, 2012). Punch-through occurs when the channel doping is very low and short gate results in merging of source-channel and drain-channel junctions. Threshold voltage roll offs defined as the decrease in threshold voltage of MOSFET with a decrease in gate length. Hot carrier degradation, which can be responsible for the reduction in the lifetime of MOSFET. Gate leakage consists of direct and Fowler-Northeim and trap-assisted tunnelling through the gate oxide layer. Gate-induced drain leakage (GIDL) which is band-to-band tunnelling mechanism occurs at the highly doped drain and gate overlap region. Short channel effects mainly result in an increase in OFF state current degradation of ON current and weak gate electrostatics.

Today's planar MOSFETs feature high-k dielectric with metal gate has led substantially reduction gate leakage and mobility improvement by means of source/drain stressor and solicitation of source and drain (Walke & Mohapatra, 2012). In spite of many technological challenges planar MOSFET shows poor subthreshold swing (>80mV/dec) and much higher OFF current (>100nA/μm) when the gate length

is scaled below 30nm. Therefore, further scaling of planar bulk MOSFET is becoming more and more challenging. One way to minimize these short channel effects is to improve gate electrostatics. This can be achieved by increasing the number of gates and reducing body thickness.

2.4 Fin Field Effect Transistor

The FinFET is an advancement based on a device called a fully depleted lean channel transistor DELTA that was described in a scholastic publication in 1989. Both the design of DELTA and FinFET devices shown in Figure 2.6 share the same concept: the channel of the device is very thin compared with the large source and drain junctions (Shen, 2017).

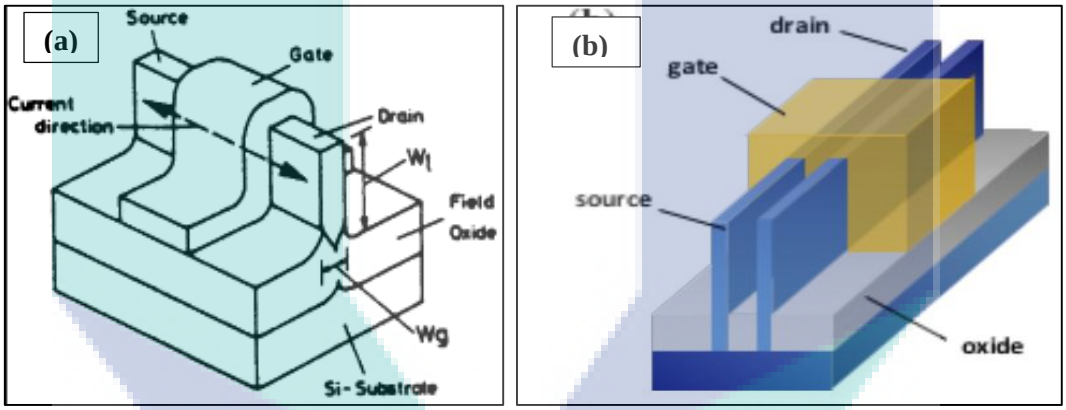

Figure 2.6 Cross-sectional schematics of (a) DELTA transistor (b)FinFET transistor
Source: Peng et al., (2017)

Because the gate dielectric and the gate wrap both sides of the channel, the control of the gate over the channel is remarkably better than that of the planar MOSFET. This is the reason why the leakage current of FinFETs is far smaller than that of planar MOSFETs. The inversion layers formed at both sides of the channel so the device channel width can be approximated as twice of the fin height. The drive current of the FinFET can be easily multiplied by designing several fins in one FinFET device. Although the FinFET has more advantages in device performance than planar MOSFET the momentum for FinFET development in academia did not pick up until early 2000 when the scaling of planar MOSFET was approaching its end. Because of the physical locations of the inversion layers (at the sidewalls of the vertical fin) the convention of

the device metrics of FinFET is slightly different from that of planar MOSFET. For example, the channel width of FinFET is usually referred to the fin height. Given that both sides of the fin are inverted when the device is at the on the state the effective width for carriers traveling from the source to the drain is twice the physical channel width of FinFET. In contrast, this effective width is the same as the physical channel width of planar MOSFET because only one side of the channel near the gate can be inverted. This difference might lead to confusion when evaluating the device performance of planar MOSFET and FinFET. A layer of silicon oxide separates the silicon channel of the DELTA transistor from the silicon substrate, whereas the channel of FinFET transistor is directly connected to the silicon substrate.

The idea about FinFET was paid attention in 1996 since DARPA (the Defense Advantaged Research Projects Agency) asked electronics engineers to propose new Structures below 25 nm technology node. In 1998, Hisamoto and his colleagues invented the first N-type FinFET. In addition, in this year the first P-type FinFET was manufactured. For several years developing Intel Corporation started using FinFET as commercial devices named Ivy Bridge in 2012 which is a kind of tri-gate FinFET (Pradhan & Sahu, 2016). After Ivy Bridge processor Intel developed Has well processor and Skylake processor based on tri-gate FinFET transistors too (Hammarlund et al., 2014). As shown in Figure 2.7, the structure of the planar transistor is on the left and the structure of the tri-gate transistor is on the right. Compared to the planar transistor tri-gate transistor has several benefits. Because the gate of tri-gate transistor surrounds Si from three directions, which improve the control of over channel the leakage current is reduced. Also, tri-gate transistor can operate at low voltage with good performance which reduces active power more than 50% (Peng et al., 2017).

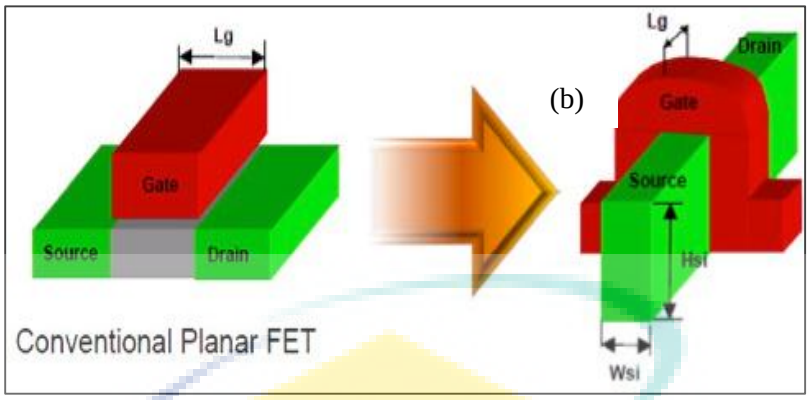

Figure 2.7 (a) 2-D planar transistor (b)3-D Tri-Gate transistor FinFET structure
Source: Bohr & Mistry (2011)

For a smooth transition from planar MOSFET to FinFET, the fabrication of FinFET is similar to that of planar MOSFET. For example, the vertical fins of FinFET are still patterned by using optical photolithography and dry etch. The various functional modules used in FinFET are similar to what is using in planar MOSFET and such modules include gate dielectric high-k metal gate source-drain extension ion implantation epitaxial highly-doped source/drain and self-aligned metal via. The direction of the logic semiconductor industry is to improve the circuit performance by adopting the low-leakage FinFET device while minimizing the risk in design yield and reliability (Mobarakeh et al., 2018). Additionally, because the gate controls both sides of the fin channel the channel control of FinFET is much better than that of planar MOSFET. The use of lightly doped or even un-doped silicon channel is now possible and thus enables higher drive current because of less carrier scattering by the dopants. Intel is the first semiconductor company that commercially sold silicon chips based on FinFET technology in 2012 although Intel called their FinFET a "Tri-gate Transistor". The first generation of 22-nm node FinFET made by Intel as reported by (Van et al., 2018). The next generation of Intel's FinFET technology is the 14-nm FinFET. The fins became taller and thinner than the fins at the 22-nm node. The corner is still somewhat rounded. The aspect ratio of the fin is higher which enables higher drive current and better off-state leakage control The latest 10-nm FinFET technology demonstrated by Intel in 2017 shows an even higher aspect ratio of the fin (Mistry, 2017; Shen, 2017).

FinFET technology is derived from the fact that its structure is made up of a group of fins with characteristics conducting channel packed with a thin silicon "fin".

The structure typically has a vertical fin on a substrate located between the source area and a larger drain. Moreover, the gate is situated at right angles to the vertical fin and transversely from one corner of the fin to the others which enables it to form an interface with the fins or channel. The gate-FinFET provided a remarkable improvement in electrical current control in the conduction channel. This helps to reduce leakages to the current levels, thereby overcoming other short-channel effects (Elayampalayam, 2016; Isukapatla and Soundarya, 2016). Somewhat the expression FinFET is employed in a generic form and this is often used to succinctly describe any structure fin-based multigame transistor describe regardless of a number of gates. A 2D planar transistor forms a conducting path between the drain and source under the gate when it is "ON" However; the 3D FinFET with three fins increases the total drive strength for higher performance as shown in Figure 2.8. A 2D planar transistor, therefore, forms a conducting path between the source and drain down the gate when it is "ON".

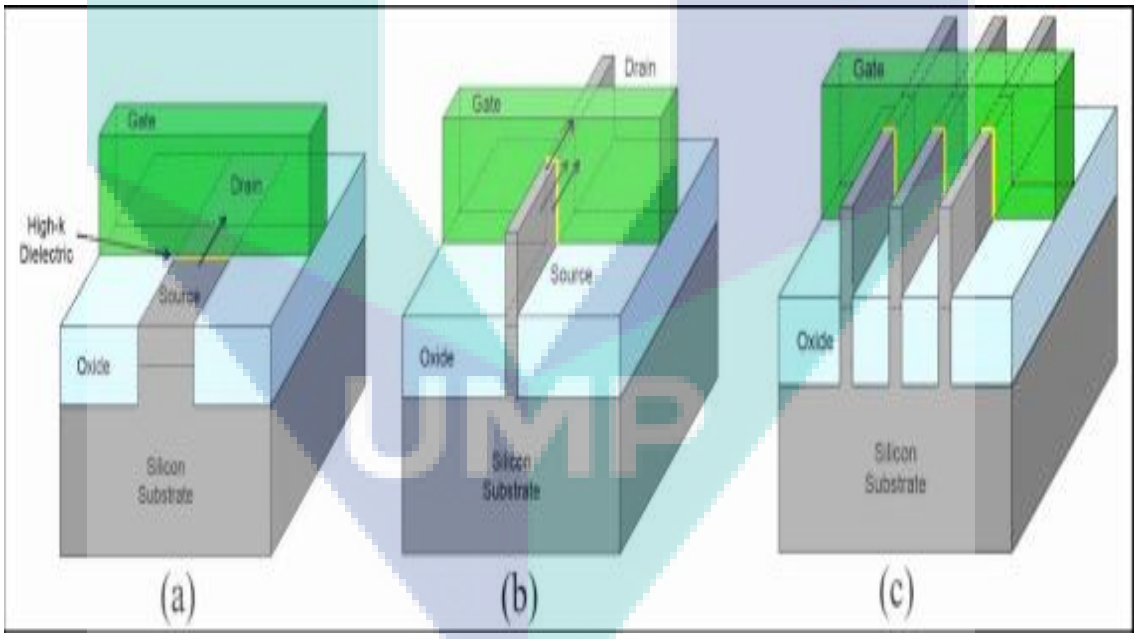

Figure 2.8 (a) Planar transistor (b) A 3D FinFET (tri-gate) (c) 3D FinFET with three fins
Source: Goettler & Gordon (2011)

FinFETs are the present manufacturing platform for all main semiconductor companies it is harder to industry and has more complex challenges (reliability design etc.) vs. the previous planar devices. There existed many advantages in the use of FinFET to the IC industries such as in nanoparticles atomic as Nano medicine in Cancer

Therapy and As an ultra-sensitive sensor in Nano electronics circuits and For applications of electronics and electricity from solar energy and almost all laser applications also in infrared accurate detectors. A reduction in the power consumption is one of such at a very higher integration level with about 150 % improvements. The inherent static leakage current was decreased to an operating speed of about 90 %, which is often in excess of 30% faster than the non-FinFET versions (Elayampalayam, 2016).

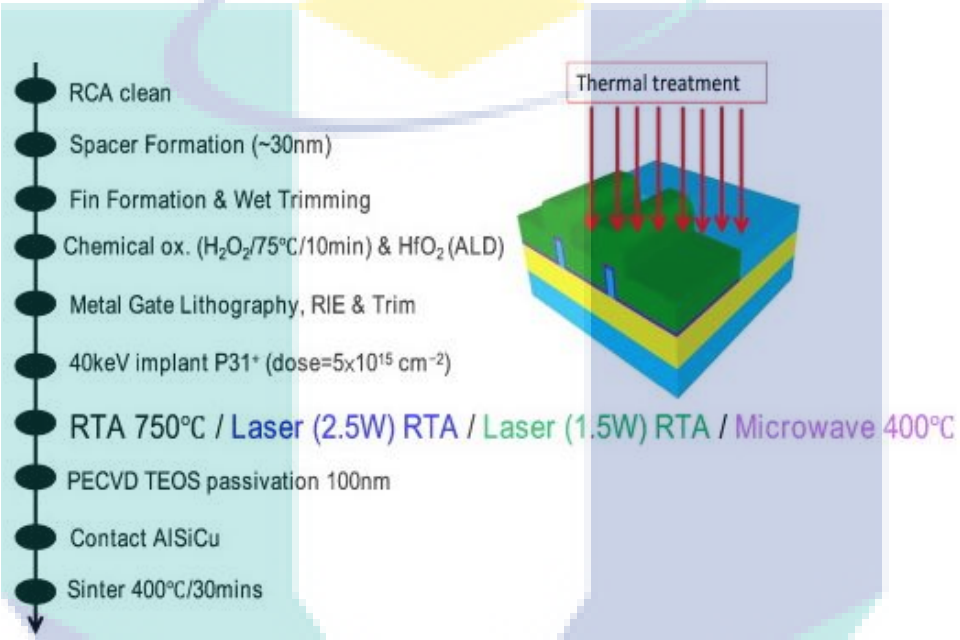

Figure 2.9 Enhanced electrical characteristics of FinFET by laser annealing
Source: Ruan et al., (2017)

2.5 Moore Law and Scaling of Transistors

The Moore's law is an observation that is named after Gordon Moore the co-founder of Fairchild Semiconductor and Intel. This law observed that the number of transistors in a densely packed IC increases every 2 years ((Brock & Moore, 2006). A description of the driving force from the technological and social change on the productivity and economic growth was observed from this law as supported by (Jorgenson et al., 2014). It is an observation and projection of a historical trend and not a physical or natural law. Although this historical trend was made to be steady between 1975 and 21012, the rate was only faster during the first decade. It is, therefore, logical to infer from the historical growth rate into the indefinite future. Take for instance, in 2010 update on the International Technology Roadmap for semiconductors, it was

predicted that the growth would decrease around 2013 and in 2015. Moreover, Gordon Moore forecasted that the rate of progress would reach saturation (Quinn et al., 2018).

In 2015 alone it was reported that the advancement decreases starting from 22 nm feature width around 2012 and continuing at 14 nm and this was expected to reach the 10 nm node in 2018 (Tian, 2017; Sankey et al., 2017). The hyper-scaling was forecasted to continue the trend of Moore's law, thereby offsetting the increased cadence by aggressively scaling beyond the typical transistors doubling (Bohr & Young, 2017). The Moore's 1975 revision was therefore cited as a yardstick for the current reduction arising from technical challenges which are natural parts of the history in Moore's law (Niccolai, 2015).

Table 2.1 The nm technologies advancements in the last years

Technology size (nm)	Year	Technology size (nm)	Year
10000	1971	130	2001
6000	1974	90	2004
3000	1977	65	2006
1500	1982	45	2008
1000	1985	32	2010
800	1989	22	2012
600	1994	14	2014
350	1995	10	2017
250	1997	7	2018
180	1999	5	2020

Source: Asadollahi, (2018)

2.5.1 MOSFET Scaling Down and its Limitations

Significant progress has been achieved by reducing MOSFETs from larger transistor dimensions to smaller transistor dimensions resulting in increased speed and density some constraints have led to the prediction of the end of technological advances in the semiconductor industry. The conventional MOSFET reduction beyond the 50 nm channel length has resulted in innovations to circumvent the barriers due to basic physics that restricts the traditional MOSFET. Limitations on the reduction of low-impedance-resistance circuits (Assad et al., 2000; Wong, 2002) are as follows:

- Increase the leakage of the current gate due to the quantum mechanical tunnel of the tankers through the thin gate oxide.
- I_{OFF} increase due to the quantum mechanical tunnel of the tankers from exchange to the body and from the source to the MOSFET drain.
- Lower I_{ON}/I_{OFF} ratio because of the lower control of the density and location of dopant atoms in the MOSFET channel and source/drain region to provide a high on-off current ratio.
- Lowering of the Subthreshold Swing.

Thus, the further reduction of MOSFET is very difficult without a significant increase in I_{OFF}. For future IC receivers super low energy and energy efficient transistors with SS are needed with acceptable (Gandhi et al., 2011).

2.5.2 The Scaling Down of FinFET

The use of FinFET is increasingly becoming common as featured sizes within integrated circuits are fading out. These are not available separately as devices since there is an increasing need to provide very much higher levels of integration with reduced power consumption within the integrated circuit. FinFET technology is a modified Nano-version of MOSFET as illustrated in Figure 2.10 (a) and (b). Many researchers focused on the invention of new MOSFET structures after overcoming the MOSFET restriction.

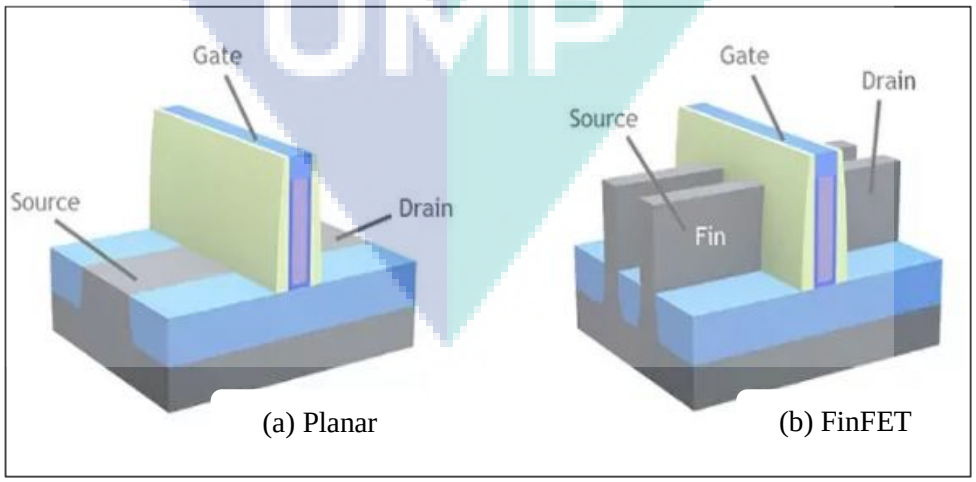

Figure 2.10 (a) planar transistor (b) FinFET transistor
Source: Daniel Fishman (2018)

A transistor's function is to switch ON when current flows from the source to the drain and stops when OFF current ceased at high-speed electrical. The current flows when the transistor ideally does three main things:

- Allow as much current to flow when it is on (active current).
- Allow as little current to flow when it is off (leakage current).
- Switch between on and off states as quickly as possible (performance).

The first point shows much power the CPU uses when it has actively done work while the second point describes how much power it draws when inactive and the third impacts on the clock speed. A 3D Tri-Gate transistor looks a Looks like the planar transistor but with one fundamental difference. Instead of having a planar inversion layer (where electrical current actually flows) Intel's 3D Tri-Gate transistor creates a three-sided silicon fin that the gate wraps around creating an inversion layer with a much larger surface area as shown in Figure 2.11 (Kimura et al., 2018).

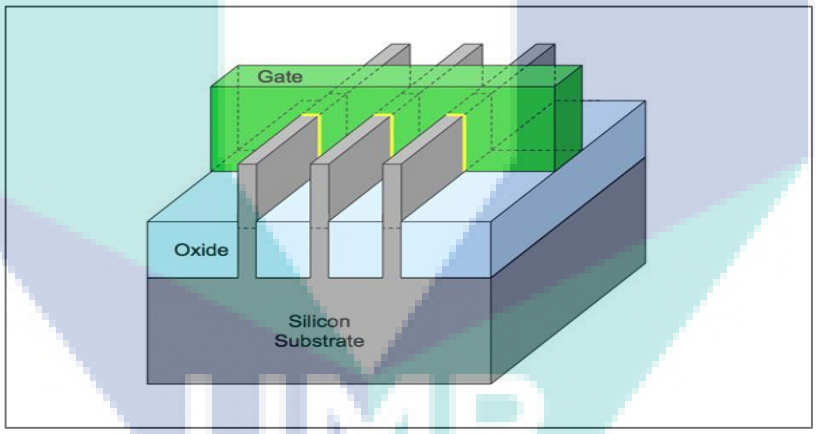

Figure 2.11 The 22 nm Tri-GATe Transistor
Source: Khan et al., (2012)

This results in five different steps as highlighted below:

- The gate exerts more control over the flow of current through the device.
- Voltage has no effect on the current when the transistor is off
- More current can flow when the transistor is ON as a result of a larger inversion layer area.
- The density of Transistor is not negatively affected.
- To increase drive strength and performance can vary the number of fins.

The first and two points in the result in reduce the leakage current and when the Intel's 22 nm 3D-Tri-Gate transistors are off, lesser power is expended than a hypothetical planar 22 nm process. The third point allows for a better transistor performance as well as lower overall power usage. Moreover, the 22 nm 3D-Tri-Gate transistors have the capacity to run at between 75 to 80 % with an operating voltage of 32 nm transistors while switching speed at the same time. This invariably leads to a decrease in active power with the same frequency or the same active power at a higher performance level. The Intel assumes that the decrease in active power can be above 50% compared to its 32 nm process shown in Figure 2.12.

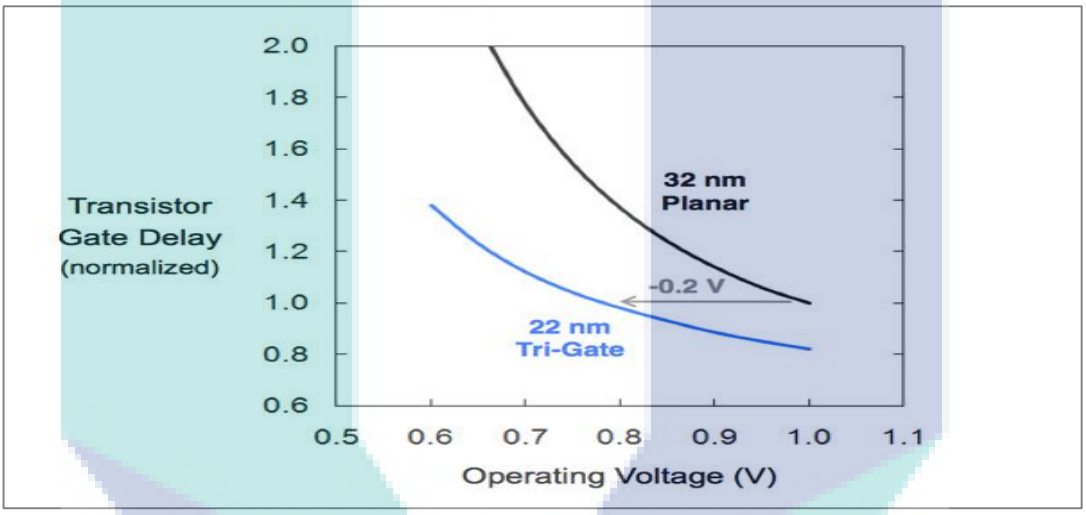

Figure 2.12 Transistor Gate Delay active power can be more than 50% compared to its 32 nm process
Source: Goettler & Gordon (2011)

Moreover, at 1 V, there is an 18 % increase in performance with the 32 nm process. The high-end desktop and mobile parts fall into the latter category with the Ivy Bridge likely to experience gains about 18 % V_s. However, the Sandy Bridge Intel is likely to make use of these gains by reducing the overall power consumption of the chip as well as pushing for higher frequencies (Figure 2.13). The ultra-mobile chips are located at the other end of the curve that is a major boost for news for the 22 nm that is likely noticeable come 2013.

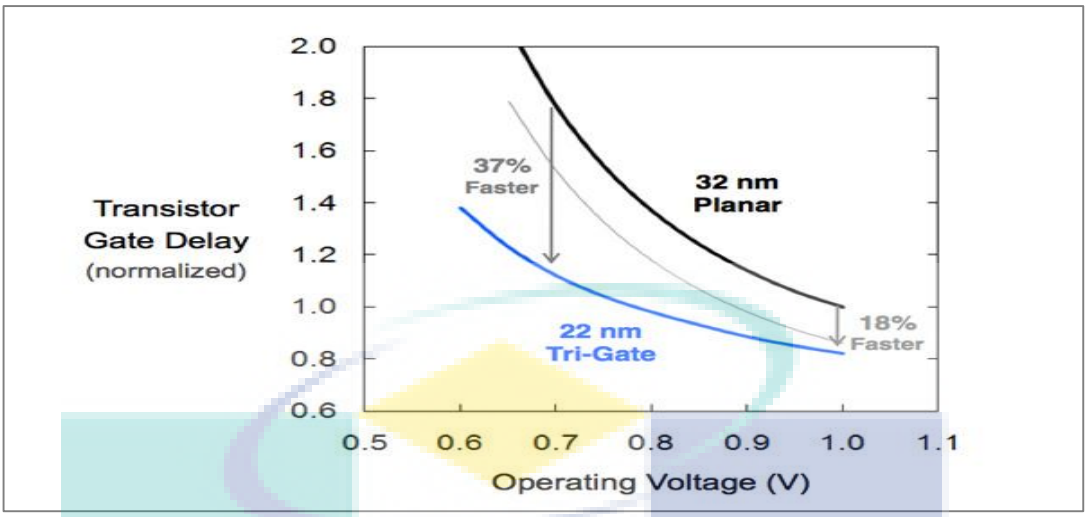

Figure 2.13 Transistor gate delay increase in performance vs operating voltage
Source: Goettler & Gordon (2011)

In an actual sense, there is an improvement in the density from 32 nm to 22 nm that can fit roughly as twice as many transistors. This can fit in the same die-area at 22 nm as could be on Intel's 32 nm (Figure 2.14). Hence, upgrading to 3D Tri-Gate transistors does not affect transistor density in a negative way.

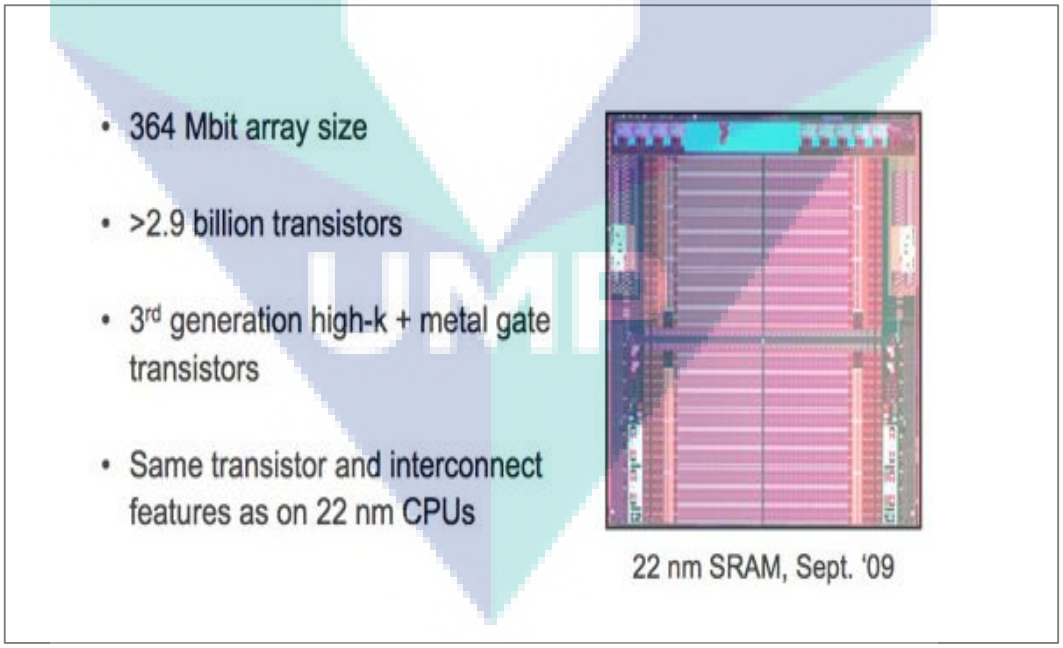

Figure 2.14 Twice fitting of many transistors in the same die area at 22 nm
Source: Khan et al., (2012)

In addition to its effect on the drive strength and performance; it is can also vary the number of fins allowing for a fine tuned, thereby targeting its 22 nm process to

various products. By comparison, to a hypothetical Intel of 22 nm planar process, the impact on manufacturing cost is also minimal. The 3D-Tri-Gate process is therefore expected to cost an extra 2 to 3% as illustrated in Figure 2.14.

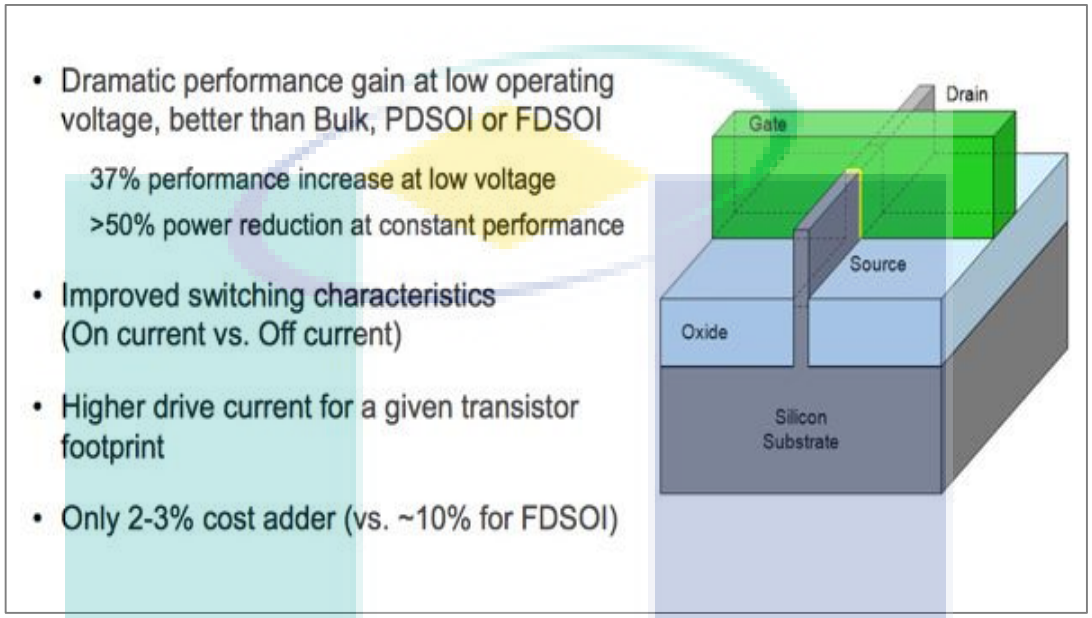

Figure 2.15 Tri-Gate Transistor Benefits
Source: Chun et al., (2011)

The major issue has to do with the atom and the largest gains are obtained at very low voltages enough to give benefit for the ultra-mobile. Their atom is confronted with resistance getting into smartphones. The real future, therefore, lies in the 22 nm process, while there might be a limited breakthrough at 32 nm. The fin width is 8 nm with rounded corners at the top of the fin. The rounded corner might be for reduction of the electric field near the corner for higher reliability or simply a by-product of the fin etch process. The next generation of Intel's FinFET technology is the 14 nm FinFET is shown in Figure 2.16 (b). The fins became taller and thinner than the fins at 22 nm node. The corner is still somewhat rounded. The aspect ratio of the fin is higher which enables higher drive current and better off-state leakage control. The latest 10-nm FinFET technology demonstrated by Intel in 2017 shows an even higher aspect ratio of the fin in Figure. 2.16 (c) (Mistry, 2017). The Intel roadmap is presented in Table 2.2.

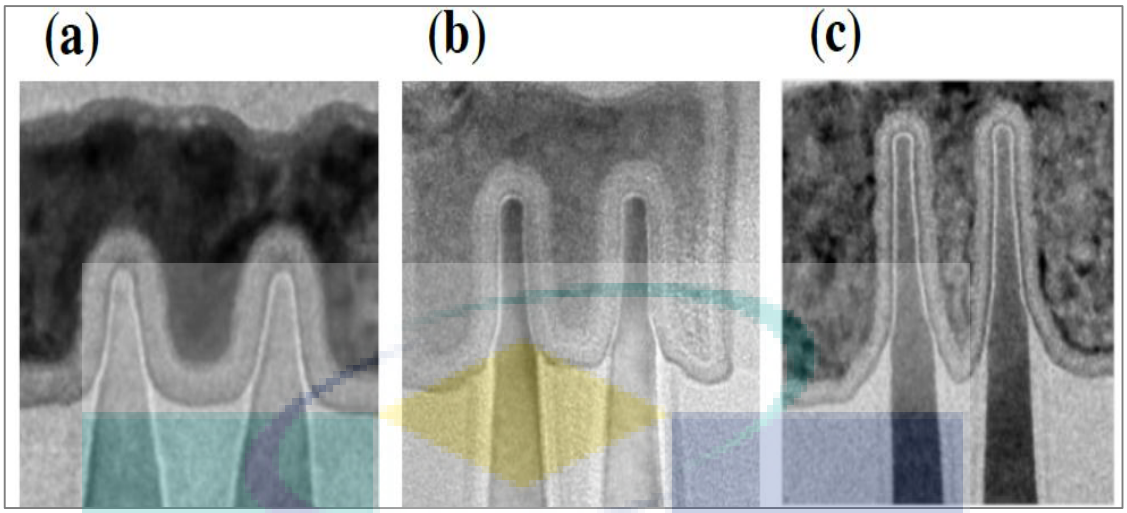

Figure 2.16 (a) First generation FinFET at 22 nm node -2011 (b) Second generation FinFET at 14 nm node- 2013 (c) Third generation FinFET at 10-nm node-2017

Source: Shen (2017)

Table 2.2 Intel Technology Roadmap

Process Name	Lithography	1st Production
P1266	45nm	2007
P1268	32nm	2009
P1270	22nm	2011
P1272	14nm	2013
P1274	10nm	2017

Source: Anand lal chimbi Intel (2011)

Now the mainstream processors are based on FinFET such as Intel core processors Samsung processors and so on (Yang, 2018). Also, Taiwan Semiconductor Manufacturing Company (TSMC) uses FinFET structure for their chips(Yang, 2018). Not only the newest full custom Integrated Circuits are based on FinFET structure but also some FPGAs use FinFET process. However, to keep scaling the size of transistors the structure of devices should be improved. Similar to the FinFET and tri-gate FETs which can extend Moore's law to 20 – 15-nm the new kind of structures are named Lateral Gate-All-Around (LGAA) FET and vertical Gate-All-Around (VGAA) FET which give further gate length scaling down to 10–5 nm. According to ITRS shown Figure 2.17 (Cherupalli et al., 2017).

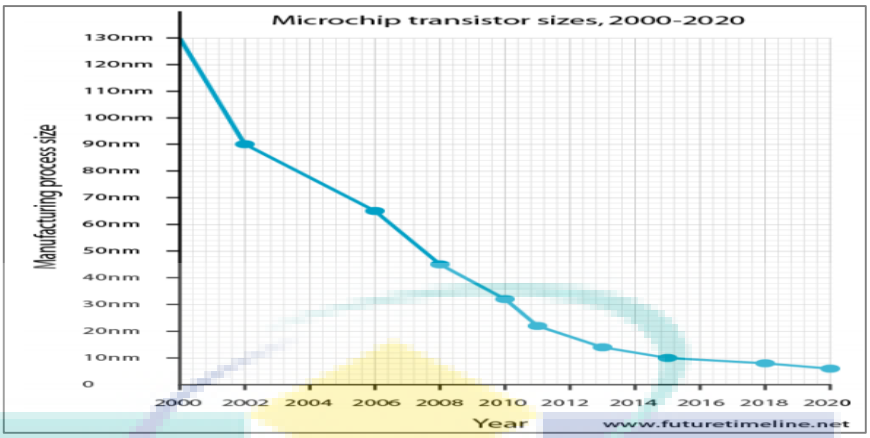

Figure 2.17 Semiconductors manufacture pressers
Source: Richerson & Lee (2018)

2.6 Electrical Properties of Transistor

This study will explore the electrical properties of types of FinFET (Si Ge InAs and GaAs) and the structure of FinFET as shown in Figure 2.9. The properties of I-V and the relevant key criteria will use to determine the strength and weakness of FinFET characteristics. The main parameters are the voltage threshold (V_T) swing under threshold (SS) DIBL and current ratio (I_{ON} / I_{OFF}). The output curve from MuGFET simulation is the variance of the product drain voltage (V_d) with the product drain current (I_d) at constant input gate voltage (V_g). There are main to this curve that includes the linear area and saturation region. A low output resistance characterizes the former, while the latter has higher output resistance. The R_{out} can be calculated using the following using Equation (2.1).

$$R_{out} = \frac{\Delta V_d}{\Delta I_d} \qquad 2.1$$

where (V_d) represent drain voltage and (I_d) drain current

The transfer curve is obtained from the variation of Vg with respect to I_d at constant V_d. The helps in the measurement of the effect of the input voltage on the output currents and this is used in the determination of many key parameters such as Tran's conductance (gm), I_{ON}/I_{OFF} ratio, V_T, SS, and DIBL. The performance of the transistor can, therefore, be measured using these key parameters.

2.6.1 Sub-threshold Swing

This involves a change in the gate voltage that is required to produce a corresponding change in the drain current. This value is expected to be as lower as possible in order to turn the transistor ON or OFF more quickly with a surge in I_{ON} leading to a corresponding reduction in the SS value. Hence, an improved trans-conductance must be taken into consideration mathematically as SS is expressed in millivolt per decade (dec). Similarly, a reduction in the I_{OFF} of SS is the inverse of the slope of I_d (with logarithmic scale) versus V_g. This parameter represents the severity of the ON-to-OFF switching of a transistor which has in theory lower (best) value at SS = 60 mV/dec SS (Colinge et al., 2010; Ionescu, 2010) at room temperature can be calculated using Equation 2.2 .

$$SS = \left(\frac{kBT}{q}\right) \ln 10. \qquad 2.2$$

where KB is the Boltzmann's coefficient, T is the temperature, q is the electronic charge.

2.6.2 ON-to-OFF Current Ratio

The I_{ON} is the drain current, I_d at the ON state where V_g = 1 V and I_{OFF} is the I_d at the OFF state where V_g = 0 V and both I_{OFF} and I_{ON} are calculated directly from the transfer characteristics of FinFET. Where it depends heavily on the mobility (M). where M_{Si} =15000cm^2/v.s, M_{Ge} =3900cm^2/v.s ; M_{GaAs} =8500cm^2/v.s, M_{InAs} = 40000c/v.s.

2.6.3 Threshold Voltage

Represents the threshold threshold of the voltages after which the transistor becomes in the case of ON and the best rate of value in the low electric circuits is from 0.4 to 0.8mV Where the transistor able to have good electrical control with acceptable performance at this range.

2.6.4 Drain-Induced Barrier Lowering

The I_{OFF} has been a major point of concern in logic circuits because it hinders the scaling because of its important passive power consumption. Its impacts on the smaller V_T at higher V_d because of the reduction of the potential barrier at the source–channel region by V_d. Moreover, the DIBL, which causes VT to roll OFF, tends to increase in the OFF state of the transistor leakage current as supported by Chaudhry & Kumar (2004). This is calculated using Equation 2.3 as presented by Lu et al., (2010).

$$\text{DIBL} = \frac{\Delta V_T}{\Delta V_d} \qquad 2.3$$

DIBL (in millivolt per volt) measured by ΔV_T is calculated with the following equation (Lee Kim & Park 2005).

2.7 Semiconductor Materials

The constituent of semiconductor materials has a tremendous impact on FinFET performance due to short-channel effects; therefore, have been studying these effects with four semiconductors.

2.7.1 Silicon Semiconductor

Silicon is a solid crystalline semiconductor metallic material with a characteristics brittleness, hardness, and lustres. It is located above carbon on the periodic table with an atomic number 14. It is usually unreactive with germanium, tin, and lead below it on the periodic table. The unreactive nature of silicon is due to its high affinity for oxygen. It was first prepared and characterized in its pure form in 1823 by Berzelius. It is melting and boiling points of-of 1414 °C and 3265 °C, respectively makes them the second highest unreactive metalloids. This important element exists mostly in dust, sands, planetoids, planets and as various forms of silicon dioxide (silica) or silicates. More than 90% of the earth's crust is made up of silicate minerals. This placed it as the second most abundant element (28%) in the Earth's (Yaroshevich & Mileiko, 2018).

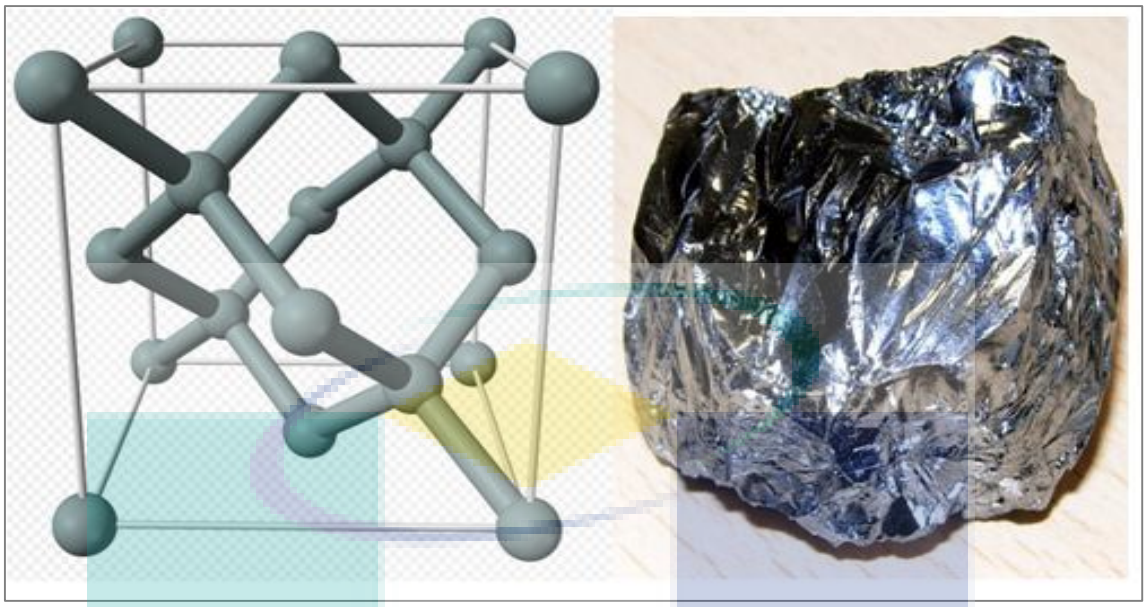

Figure 2.18 Purified crystalline silicon with a diamond cubic crystal structure
Source: Taylor (2012).

Most of the silicon elements stay as an alloy with only one-fifth accounting for 1.3-1.5 million metric tons/year are refined at higher purity to metallurgical grade. From the total world production, only about 15 % are further refined to semiconductor purity grade (Issa, 2016). The diamond structured mono-crystalline silicon is usually costly and only produced when it is potential use is in integrated circuits which require miniature crystal accuracy. This usually has its application in some high-cost and high-efficiency photovoltaic using Czochralski process (Sousa et al., 2015). Moreover, the pure silicon is a conductor electricity using heat through electron holes and electron released from atoms. The electrical conductivity increases with an increase in temperature. However, pure silicon is characterized by too high resistivity (i.e. lower conductivity) which makes them unsuitable in the electronic circuit in its pure form. Moreover, pure silicon is usually doped with a small concentration of other elements that in turn increases the electrical conductivity of the material. The doping with other elements increases the conductivity by controlling the positive or negative charge of the activated carriers. These electrical controls are usually as transistors in solar cells, semiconductor detectors and other semiconductor devices used in the computer industry and other technical applications. In addition, the silicon photonics can be used as continuous wave Raman laser medium to produce coherent light.

2.7.2 Germanium Semiconductor

Germanium is a solid-lustre whitish-grey metalloid belonging to carbon group that shares a resemblance in chemical activities with tin and silicon (Figure 2.19). Germanium is a chemical element with an atomic number 32 that is similar in appearance to elemental silicon. Like silicon germanium naturally reacts and forms complexes with oxygen in nature (Meija et al., 2016).

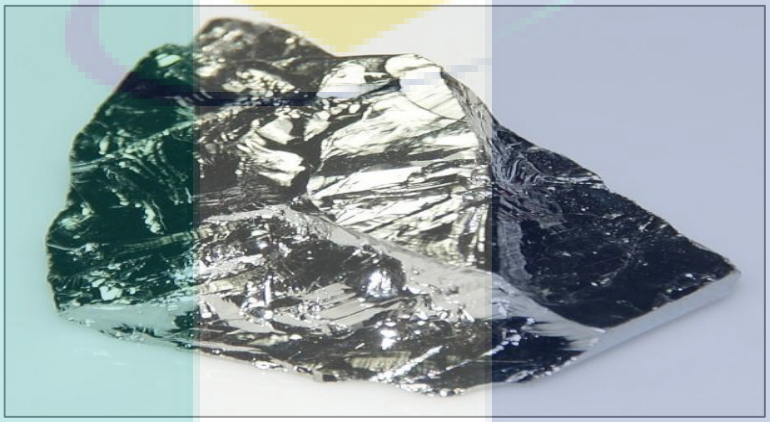

Figure 2.19 Grayish lustrous block with an uneven cleaved surface
Source: Meija et al., (2016)

Germanium at elemental level is usually employed in transistors as a semiconductor and in several other electronic devices. The use of semiconductors in electronic is back traced to germanium. The quantity of germanium used in semiconductor applications is about 20 % of the total amount of high-purity silicon produced for the same purpose. In recent times, germanium is majorly used in fibre-optic systems, infrared optics, solar cell, applications and light-emitting diodes (LEDs). Moreover, they are also used for catalyst polymerization catalysts and is recently found its applications in nanowires production. Germanium forms a huge number of organometallic compounds such as tetraethyl germane, that is useful in organometallic chemistry (Geological, 2008).

2.7.3 Indium Arsenide Semiconductor

The Indium arsenide is a grey-cubic crystalline semiconductor that comprises indium and arsenic with a melting point of 942 °C (Figure 2.20). InAs has found application in the construction of infrared detectors (usually photovoltaic photodiodes)

with a wavelength ranging from 1.0–3.8 nm (Issa, 2016). However, the cryogenically cooled detectors exhibit lower noise while InAs detectors can also be applied in higher-power applications at room temperature. Furthermore, InAs can also be applied to the manufacture of diode lasers. InAs can sometimes be coupled with indium phosphide and alloyed with gallium arsenide to forms indium gallium arsenide. A material with band gap is dependent on Indium to gallium ratio. This method is principally similar to alloying indium nitride with gallium nitride to yield indium gallium nitride as reported by Angelo et al., (2018). In addition, InAs exhibits a high-electron mobility and narrow energy band gap which makes them useful used as terahertz radiation source with a strong photo-Dumber emitter.

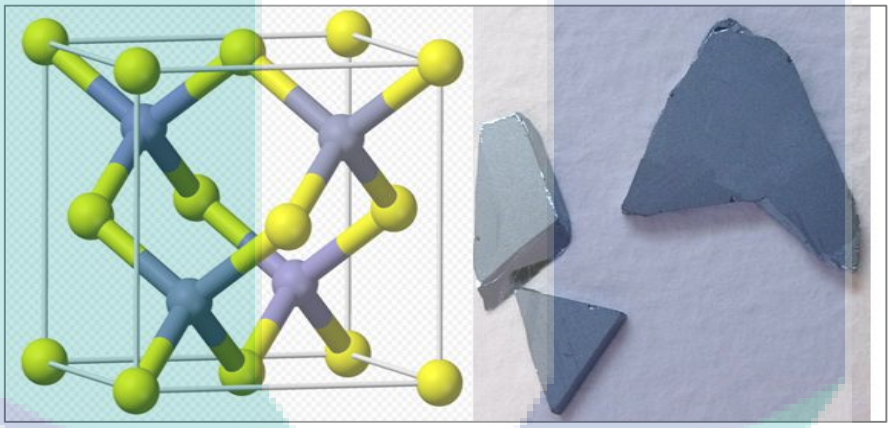

Figure 2.20 Sphalerite-unit-cell-3D-balls with Indium arsenide crystals
Source: Rowell (2012)

However, the quantum dots could also form in a monolayer of indium arsenide on indium phosphide or gallium arsenide. The mismatch of constants lattice from these materials form tension in the surface layer which in turn results in the formation of the inherent quantum dots as reported by Becker & Ossig (2013). It can also be formed in indium-gallium arsenide as indium arsenide dots sitting in the gallium arsenide matrix.

2.7.4 Gallium Arsenide

The GaAs is a compound formed from a combination of elemental gallium and arsenic. It has III-V direct band-gap semiconductor with a zinc blende crystal structure (Figure 2.21). The GaAs has found its application in the manufacture of devices such as microwave frequency integrated circuits, monolithic microwave integrated circuits,

infrared light-emitting diodes, laser diodes, solar cells, and optical windows. It is often used as a substrate material for epitaxial growth of other III-V semiconductors which include indium gallium arsenide, aluminium gallium arsenide, and others (Haider et al., 2017).

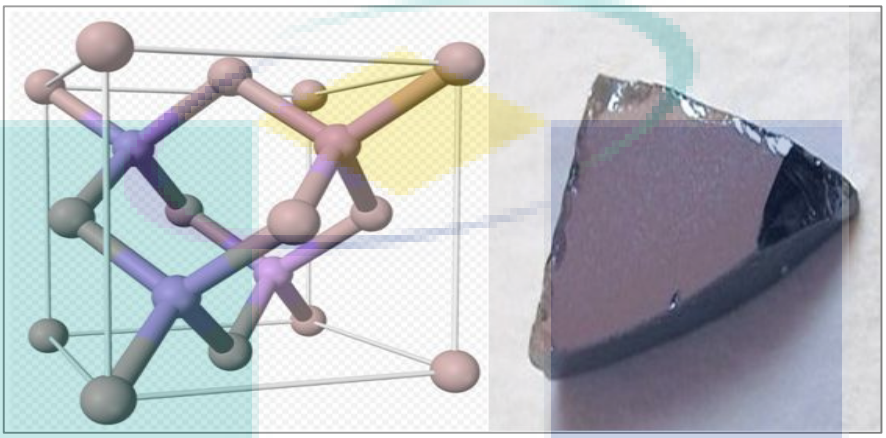

Figure 2.21 GaAs can be used for various transistor types
Source: Rowell (2012)

2.8 The Effect of Semiconductor Materials on the Electrical Properties of Transistors

When the scaling limit of transistors reaches Nano-scale dimensions the use of nonconventional semiconductors such as silicon becomes more and more because the properties of these materials change when they reach the nanoparticles. This is what we will explain in this research with (GaAs-InAs and Ge). Since the debut of complementary metal-oxide-semiconductor (CMOS) in industry production line in late 1970s, Silicon-based CMOS technology has been the driving force for the semiconductor industry. various evolutional techniques have been invented and introduced into devices such as multi-core structure to lower the power consumption high-gate dielectric to limit the leakage and enhance the gate control strain technology to improve the carrier mobility gate the last process for a better reliability silicon on insulator (SOI) substrate for superior immunity to 3D multi-gate structure to boost the gate control. Most importantly the critical length of MOSFET has been evolutionally scaled from micron level to sub-micron node then to deep sub-micron node and to the 14 nm node available in these days to enhance the device performance increase the integration density reduce the production cost and lower the power consumption (M.

Bohr, 2014). However, the performance gain enabled by scaling down becomes more and more limited. With the shrinking pitch size in CPU, the power density on the chip will increase correspondingly. Figure 2.22 shows the CPU power density trend in the last decade and the power density is controlled below 100 W/cm^2 to avoid overheating clearly indicating that the MOSFET scaling trend has switched into the power constraint scaling (Pop, 2010).

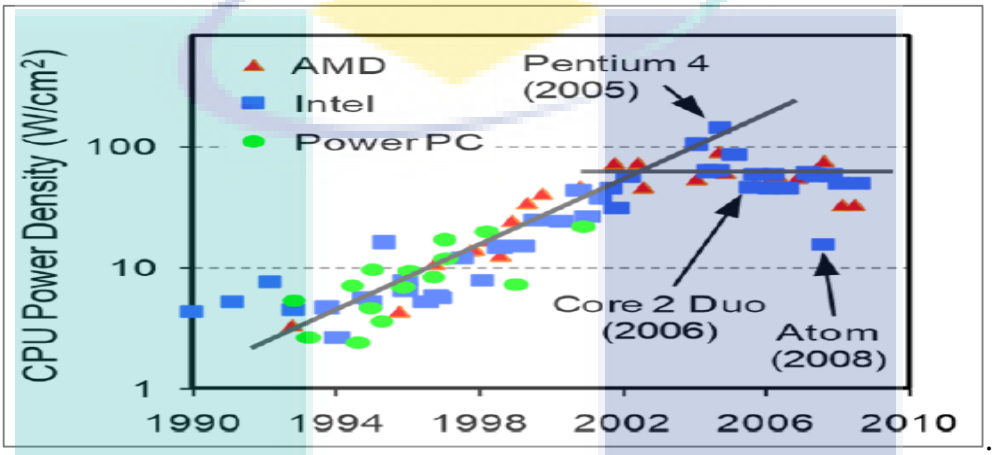

Figure 2.22 CPU power density trend in the last decade
Source: Khan & Pop (2010)

Since the transition of CPU architecture from single core to multi-core, the clock rate of CPU has not changed too much. The number of transistors keeps increasing with device scaling requiring a reduction in the supply voltage. However, lowering supply voltage would reduce drive current thus degrades the speed of circuits. To solve this it is necessary to maintain or increase the drive current with reduced operation voltage (Zhang et al., 2011). The Q_s is total charges and V_{inj} is the injection velocity of the carriers near the source side in MOSFET along the channel direction. This simple analysis indicates that the drive current could be improved with higher V_{inj}. By introducing high mobility channel materials higher injection velocity can be archived even under lower operation voltage (Duriez et al., 2013).

Table 2.3 is a list of basic electrical properties of various semiconductor materials. Ge and III-V compounds have a much larger hole and electron mobility than Si respectively. To full the needs of next-generation low power and high-speed circuits, high mobility channel materials are of great importance (Van Dal et al., 2012).

Table 2.3 Basic electrical properties of Si-Ge and III-V compounds

T=300 K	Si	GaAs	InAs	GaSb	Ge
μ_p (cm^2/V.s)	450	400	500	1000	1900
μ_n (cm^2/V.s)	1500	8500	40000	3000	3900
n_i (cm^{-3})	1×10^{10}	2.1×10^{6}	1×10^{15}	1.5×10^{12}	2×10^{13}
E_g (eV)	1.12	1.42	0.36	0.726	0.66

Source:Van Dal et al., (2012)

2.9 Comparative Summary of Previous Studies

This section highlighted the most recent related studies on Nano-scale dimensions' effects on electrical characteristics of FinFET. In order to reduce channel dimensions and improve performance in FinFET design, there is a need to simulate the characterization of FinFET behaviour and help in decision-making. Over the last decade there have been many types of research focusing on the manufacture of FinFET in various nanometres such as semiconductor materials insulation materials and various manufacturing techniques developed to predict the performance of FinFET (De'nan et al., 2017) But those researches did not focus in its study on the comprehension of the subject in full form as is shown when reading in this section that some the researches discussed in one channel dimension length or width or oxide thickness, for example, depending on one property such as I_{ON}/I_{OFF} or SS or DIBL only and for one semiconductor type such as Si-FinFET or Ge-FinFET .and these some literature previous work about certain related topics.

Mobarakeh et al., (2018) investigated the theoretical logic performance estimation of Silicon Germanium and SiGe nanowire Fin-Field Effect Transistor. Those researchers propose and analyse three different nanowire FinFETs: Silicon Germanium and SiGe nanowire FinFETs. they studied the influence of the parameters doping concentration the channel length and dielectric thickness in order to analyse and determine the short channel effects such as DIBL and also I_{ON}/I_{OFF} ratio for switching application then they found that the logic performance parameters such as I_{ON}/I_{OFF} ratio and drain induced barrier lowering (DIBL) in the silicon structure show a significant advancement compared to two other structures. It is shown that the ON current and therefore the I_{ON}/I_{OFF} ratio in the structures can be improved by increasing the doping

concentration and it also effects on DIBL. They also compared the analogy performance parameters including the Tran's conductance (gm) output conductance (gd) and voltage gain (AV) for all three simulated devices. The obtained his results show that the SiGe FinFET is suitable for the analogy application were reach to length channel 7 nm with Si-FinFET and I_{ON}/I_{OFF} ratio 10^9, DIBL = 28. However, they did not test the channel width and did not show SS value that had a direct effect on transistor velocity.

The physical insights on the scaling of Gaussian channel design junction less FinFET have been studies by Kaundal & Rana, (2018). In the present work junction less FinFET with Gaussian, channel design has been proposed and investigated for its scaling capability in Nano regime. The device performance metrics this means the OFF-state current (I_{OFF}) ON to OFF current ratio (I_{ON}/I_{OFF}) drain-induced barrier lowering (DIBL) and sub-threshold swing (SS) are evaluated as function of gate physical length (LG) gate dielectric thickness (T_{OX}) and fin thickness (T_{SI}). This proposed graded structure is also compared and contrasted with conventional uniformly doped junction less FinFET (UD-JL FinFET) structure. The Gaussian channel junction less FinFET (GC-JL FinFET) structure shows superior performance in terms of I_{ON}/I_{OFF} and SS for LG down to 7 nm. Nevertheless, at the same time, DIBL performance significantly degrades below L G = 14 nm. We observed that SS as low as 85 mV/dec and DIBL up to 100 mV/V can be achieved with GC-JL FinFET at LG down to 10 nm. Further, the gate dielectric scaling limit, which is primarily restricted due to gate tunnelling current, is explored for both GC-JL FinFET and UD-JL FinFET structures. Although he is reached the length of the 10 nm gate the value of SS = 85 mV/dec is still large and the value of DIBL = 100 mV/V.

The impact of Cross-Sectional Shape on 10 nm Gate-Length InGaAs FinFET Performance and variability have been studies by Seoane et al., (2018). FinFETs with a gate length of 10.4 nm are modelled using in-house 3-D finite-element density-gradient quantum-corrected drift-diffusion and Monte Carlo simulations. We investigate the impact of the shape on I-V characteristics and on the variability induced by metal grain granularity (MGG) line-edge roughness (LER) and random dopants (RDs) and compared with their combined effect. The more triangular the cross-section the lower the OFF current the drain induced-barrier-lowering and the Subthreshold Swing. The I_{ON}/I_{OFF} ratio is three times higher for the triangular-shaped FinFET than for the

rectangular-shape one. Independent of the cross section the MGG variations are the preeminent fluctuations affecting the FinFETs with four to two time's larger V_T than that from the LER and the RDs respectively.

However, the variability induced threshold voltage (V_T) shift is minimal for the MGG (around 2 mV) but V_T shift increases 4-fold and 15-fold for the LER and the RDs respectively. The cross-sectional shape has a very small influence in V_T and OFF current of the MGG LER and RD variability both separated and in combination with standard deviation differences of only 4% among the different device shapes. Finally, the statistical sum of the three sources of variability can predict simulated combined variability with only a minor overestimation. However, the results were SS = 61.3 mV/dec, DIBL = 67.3 mV/V, $I_{ON}/I_{OFF} = 4.70\times10^4$. Note that the value of SS is good but the value of I_{ON}/I_{OFF} was low resulting in dissipation of energy. (Das & Baishya, 2018) investigated the application of dual-material gate, dual-stacked gate dielectrics, gate-source overlap, and tri-gate germanium FinFET. The study proposed a novel dual-material-gate, dual-stacked-gate; dielectrics gate-source overlaps Ge-FinFET and compares its characteristics with the conventional FinFET. The proposed device thereafter showed lesser leakage current (I_{OFF}) ($\sim 10^{-17}$ A) that is significant on drain current ($\sim I_{ON}$) ($\sim 10^{-4}$ A) at a very high ratio of I_{ON}/I_{OFF} ($\sim 10^{13}$) with less sub-threshold swing (SS = 71 mV/dec) and length channel of 40 nm.

The effect of different dielectrics oxide thicknesses (T_{OX}) and back-gate voltages (V_{GB}) on transfer characteristics were proposed. The effect of channel concentration on I_{ON}/I_{OFF} threshold voltage (V_{th}), Tran's conductance (gm) and SS was also investigated. The overlap length (L_{OV}) effect on the analogy parameter gate-source capacitance (C_{gs}) was analysed. Moreover, the effect of fin thickness (T_{fin}) on V_{th} and SS were considered. The height of the B_{OX} plays an important role in reducing the I_{OFF}. Emphasis was laid on the digital application using the proposed device as a digital inverter circuit. This was implemented investigates using the mixed-mode simulation. Furthermore, the effect of variation on the geometry parameters of S_{ub}-50 nm FinFET with their direct impact on FinFET performance was investigated as reported by Chugh, (2018). The variability of various parameters like I_{ON}/I_{OFF} Subthreshold Swing and DIBL with variations in gate length to reached 20 nm, at width=5 nm, oxide thickness = 0.9 nm. These results indicated that with shorter gate lengths the parameters showed a significant improvement. It is important to note that there are constraints of current

leakage that increases beyond 10 nm. The transfer characteristics, therefore, showed a significant improvement when the gate length is kept at 20 nm.

However, the leakage current parameter becomes more significant as the value gets close to the gate length of 12 nm. At this point, this threshold cannot be ignored any further. For good results to be obtained, the devices below sub-10 nm are to be designed with optimum values of mesh spacing and doping concentrations where value I_{ON}/I_{OFF} = 3.6×10^{8}, DIBL = 69.96 mV/V, SS = 69.11 mV/dec. These enable a succinct exploration of the gate work function variations, mesh spacing parameters, and further enhance the characteristics of the device at lower gate lengths. The data and results were however modest enough except for dimension of oxide thickness that was a novelty.

In FinFET versus Gate-All-Around Nanowire-FET, the performance of scaling and variability were investigated by (Nagy et al., 2018). A combined 3D-quantum-corrected FEDD and MC simulation of the performance scalability and variability were reached with a length channel ranging from 25 to 10 nm and the best results was 10nm where the I_{ON}/I_{OFF} = 15.3×10^{4}, V_T =26 mV, SS = 68 mV/dec (MGG and LER) is performed for 25/10.7 nm gate length Si FinFETs and 22/10 nm gate length Si GAA NW FETs. In the OFF-region, the FinFET devices have 9 % larger SS values over an order of magnitude larger than OFF currents with those of the equivalent GAA NW FETs. Moreover, in the ON-region the 25/10.7 nm gate length FinFETs deliver 20/58% larger ON-currents than the equivalent 22/10 nm gate length GAA NW. The ON/OFF ratio of the FinFETs (1×10^{4} when LG =10.7 nm) are more than an order of magnitude lower than those of the GAA NWs (13×10^{4} when LG =10 nm). In addition, with increased scaling deteriorated significantly especially with $I_{ON}/_{OFF}$ ratio and this lead to large energy dissipation due to increased I_{OFF} at the expense of I_{ON}.

An improved electrical characteristic of CMOS inverters comprises of GeN and P-FinFETs which were demonstrated using a newly introduced Ge surface treatment (Yeh et al., 2018). The in-situ ALD digital O-3 treatment was adopted on the surface of Ge-Fin sidewall in order to reduce the roughness and etching damages through the GeO desorption mechanism. The combination of this treatment with optimized a microwave annealing (MWA), SS and I_{ON} /I_{OFF} ratio were remarkably improved in both the n-FinFET and p-FinFET and Ge-CMOS inverters with a high voltage gain of 50.3 V/Vat low V_D =0.6 V were realized. A newly introduced combination processes of MWA and in-situ ALD digital-O3 treatment successfully demonstrated the Ge-FinFET CMOS

inverters. The superior SS characteristics of 71 mV/dec. and 88 mV/dec. with high I_{ON}/I_{OFF} = 10, width cannel=20nm and length channel= 200 nm ratio was achieved for Ge n- and p-FinFET, respectively. The Ge-CMOS inverter shows the high voltage gain of 50.3 V/V thanks to the interface states reduction caused by the in-situ ALD digital O3 indicating the potential of Ge for CMOS applications in advanced technology nodes. However, the length of the gate was very long and the width. This was not commensurate with the developments today that lead to the lack of density, cost increase and large size.

Hashim, (2017) investigated the FinFET as a temperature Nanosensor Based on the channel semiconductor type. The temperature sensitivity of FinFET was simulated with Si, Ge, GaAs, and InAs as semiconductor channels. The FinFET transfer properties with V_d = 1 V were studied at different operating temperature values (-25, 0, 25, 50, 75, 100 and 125 °C) for all semiconductor channel types. This shows that FinFET is best used as a Nanosensor with GaAs because it has a larger ΔI (10.9 %) indicating a type II at 25 ^{o}C. The best stability of FinFET with increasing working temperature is therefore Si-FinFET, because it has a minimum ΔI (6%) and is referred to as type II at 25 ° C. However, the leakage current value (I_{OFF}) and value of SS must be taken into consideration especially in modern complex sensor systems that contain millions of sensors.

The electrostatic analysis of Gate-All-Around (GAA) nanowire over FinFET has been studied by Prashant as reported in Rana, (2017). The CMOS technology has been scaled down to 7 nm with FinFET replacing planar MOSFET devices. Due to short channel effects, the FinFET structure was developed to provide better electrostatic control on sub-threshold leakage and saturation current over planar MOSFETs while having the desired current drive. The SS increases from 67.03 to 89.7 mV/dec by sweeping the L-gate from 23 nm to 13 nm. Whereas for nanowire the SS varies from 64.42 mV/dec to 76.13 mV/dec and do not show much variation. For scaling down to 5 nm and at L-gate = 15 nm, the nanowire shows the SS = ~71 mV/dec. The SS of the nanowire (L-gate = 15 nm) is not the same as FinFET at L-gate = 21 nm. However, the value of SS = 64.2 mV/dec is still significant as it does neglect the calculation of the leakage current I_{ON}/I_{OFF} ratio which is very important with calculation it SS value. The summary of the previous investigation is presented in Table 2.4.

Table 2.4 Summary of previous studies main finding

References	I_{ON}/I_{OFF}	SS mV/dec	DIBL mV/V	V_T V	Length nm	Material	Drawbacks
Mobarakeh et al., (2018)	10^9	_	28	_	7	Si & Ge	Only considered channel length and two electric properties for two types of semiconductors.
Kaundal & Rana, (2018)	_	85	10 0	_	10	Si	Tested only one dimensions for Si-FinFET only.
Seoane et al; (2018)	4.7×10^4	_	67	_	10.4	InGaAs	Focused on channel length and two electrical properties, for InGaAs only.
Das & Baishya, (2018)	10^{13}	71	_	0.46	40	Ge	Only considered Ge-FinFET with long channel length 40 nm and ignored DIBL.
Chugh, (2018)	3.6×10^8	69	69	_	20	Si	Shortest channel length was 20 nm, one semiconductor was considered with ignoring V_T.
Nagy et al., (2018)	15.3×10^4	68	_	0.26	10	Si	One dimensions and two properties, with the low I_{ON}/I_{OFF} for Si-FinFET.
Yeh et al., (2018)	10^5	71	_	0.6	200	Ge	Very long channel length, no significant results , one semiconductor was investigated.
Current study	High I_{ON}/I_{OFF} Ratio	Near to ideal SS	Acceptable level	Acceptable level	Considered three channel dimensions (L, W, T_{OX})	Si, Ge, GaAs and InAs)	Achieved new channel limits (THREE (3) dimensions) with good performance in terms of FOUR (4) electrical characteristics for FOUR(4) semiconductor materials.

2.10 Summary

This chapter provided the fundamentals on the FET devices and its development into MOSFET that is the most common FET. The introduction of FinFET provided modern technology in terms of design, fabrication types, and merits. Quick reviews detailing the effect of the short channel (SCE) due to the quick scaling of FET transistor lead to power consumption problems electric were highlighted. The characteristic of the transistor and the operation of CMOS device used for advanced FinFET transistor were also presented. Moore's law and miniaturization of transistor size was the latest FinFET technology demonstrated by Intel with length channel 10 nm in 2017. The performances of electrical characteristics of the transistors were also highlighted. This acts as the quality of transistor key criteria, which determine the strength, and weakness of FinFET. The main parameters used include the voltage threshold (V_T), swing under threshold (SS), I_{ON}/I_{OFF} ratio and drain-induced barrier lowering (DIBL). The effect of the different semiconductor materials (Si, Ge, GaAs, and InAs) on the electrical properties of transistors in relation to previous studies were succinctly addressed in this chapter.

CHAPTER 3

METHODOLOGY

3.1 Introduction

This chapter describes the methodology adopted in this thesis. The theoretical base and the methodology of the research are described in details. First, a general methodology and different phases are described then the details research methodology flow chart is illustrated. Following this is an overview of the simulation environment including the simulation tools and the simulation procedure, is presented. This chapter also describes the simulation design of various simulation scenarios that used in the performance evaluation of FinFETs. Finally, it ends with defining the considered metrics for the performance evaluation in the thesis.

3.2 General Research Methodology

After reviewing the relevant literature and highlighting limitations in the field of nanotechnology applications, the problem statement of this research was identified, and four main phases adopted for the general descriptive research methodology. These phases include different stages and research activities in conjunction with the detailed simulation environment. The involved research phases were as follows:

- **Phase I** – Considering FinFET transistor as the main focus of this study since it is the successor of FET-based nanoscale devices. Then, selecting MuGFET as the simulation tools to conduct the study due to its superiority and reliability in evaluating the performance of multi-gate FET transistors and in particular FinFETs and Nanowire transistors.

- **Phase II** – Simulation and characterization of FinFETs based on various channel dimensions (L, W, and T_{OX}) and identifying the best performance per each dimension for different semiconductor materials of FinFETs.
- **Phase III** – According to the obtained results of Phase III, a new scaling factor, K, has been proposed to scaling down all dimensions of the channel simultaneously to achieve new physical limits of channel dimensions.
- **Phase IV** – Design FinFETs with optimal nanoscale channel dimensions for the best transistor performance. Finally, evaluation and comparative analysis of different FinFETs performances based on electrical characteristics for identifying the best constituent semiconductor materials.

3.3 Simulation Tools

The use of simulations is an important tool that helps in the proper understanding of devices behaviour and evaluating their performance. The use of simulation tools accelerates the development of FinFET and helps in providing support to experimental works carried by industry (Bescond et al., 2004; Yueh 2015). The merit of using simulation tools is that it reduces costs identify strengths and weaknesses of various models and approaches. It also benefits in the demonstration of the viability of materials up to the range of nanometre. Computer-assisted designs for nanometre-scale semiconductor devices require an appropriate measure of mechanical quantum models that capture the atomic accuracy of the simulation field. Most researchers in the field of Nano devices used to simulate the proposed new structure and investigate their characteristics using the available simulation tools. Among simulation tools that are used to simulate the characteristics of FinFET is Multi-Gate-Field Effect Transistor (MuGFET). A simulation tool solves the Schrodinger equation with open orbital conditions. The burden of calculation depends directly on the complexity of this basis. The size of the Hamiltonian matrices depends on the orbits to describe the atom (Hashim, 2017).

The procedure of simulation setup and design of simulation scenarios are explained in detail in the following sections. Figure 3.1 illustrates the flowchart of the conducted simulations for analysing the electrical characteristics of the considered FinFETs based on various channel dimensions.

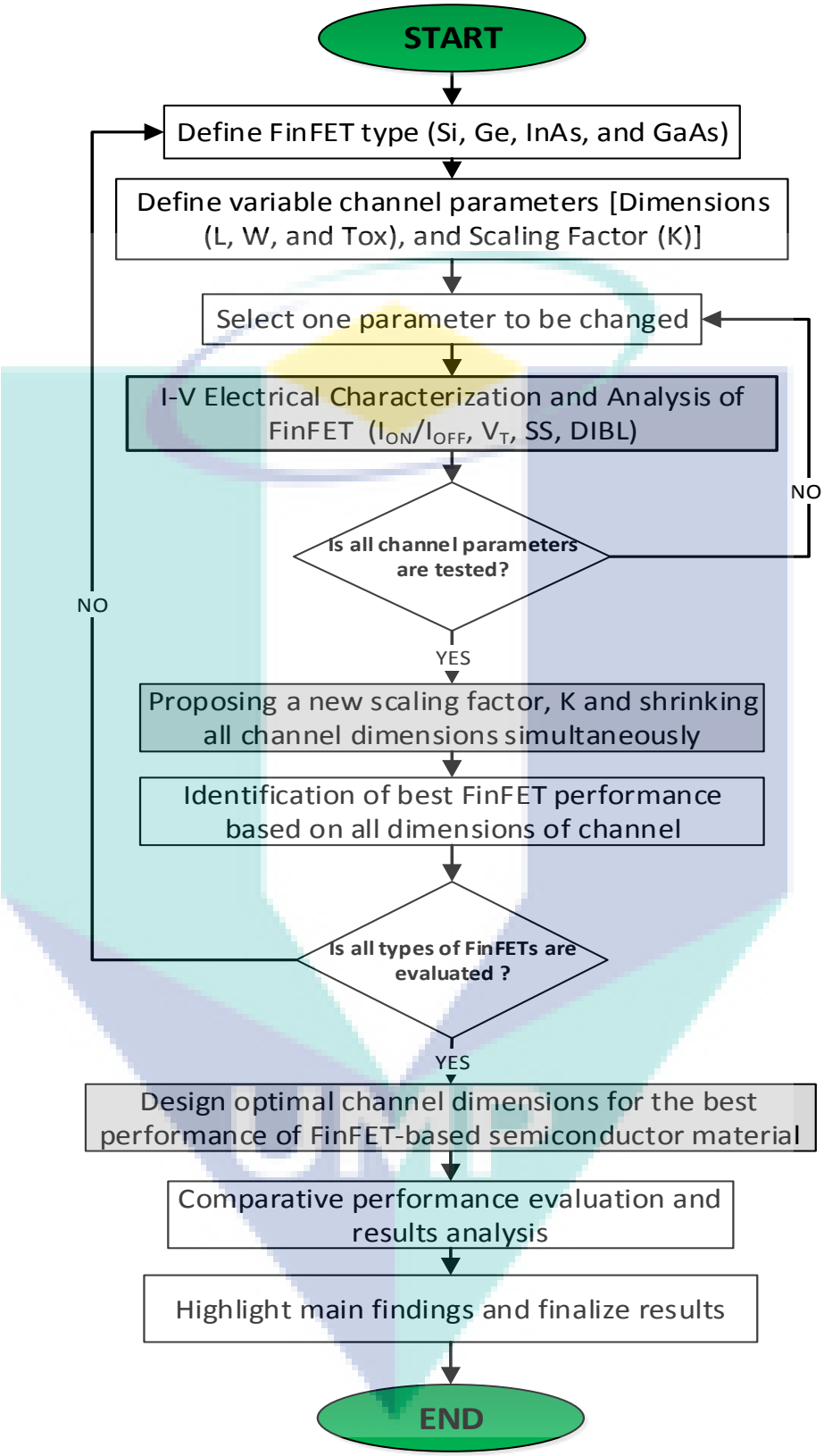

Figure 3.1 Flow chart of research methodology

The MuGFET utilizes either PADRE or PROPHET simulators that are both advanced by Bell Laboratories. PADRE is a device-oriented simulator for 2D and 3D devices with arbitrary geometry PROPHET is a partial differential equation (PDE) solver for equations with one two or three dimensions (Lloyd et al. 1995). It supplies plots that are more useful for engineers but requires a deep understanding of physics. MuGFET, therefore, provides a self-consistent solutions to the Poisson and drift-diffusion equation (Hashim, 2017).

The MuGFET has a provision for selecting either FinFET or NANOWIRE for simulation. Moreover, quantum transport is being simulated by the MuGFET at the Nano-level which approximates to the atomistic dimension. However, the demerit of quantum transport which makes the drift-diffusion type simulation as a better tool. The PROPHET and PADRE are the two drift-diffusion based simulators in this case. It is important to note that either of the simulators can be used for FinFET. Only PADRE can be employed for NANOWIRE. There six different sections with each section having different parameters that can be varied according to the requirement. Form the requirement the gate length channel, width oxide thickness, and doping concentration can be varied. Many options existed after simulating the graphs such as IV characteristics, train-conductance, drain induced barrier lowering and threshold voltage as shown in Figure 3.2 (Hajare et al., 2015).

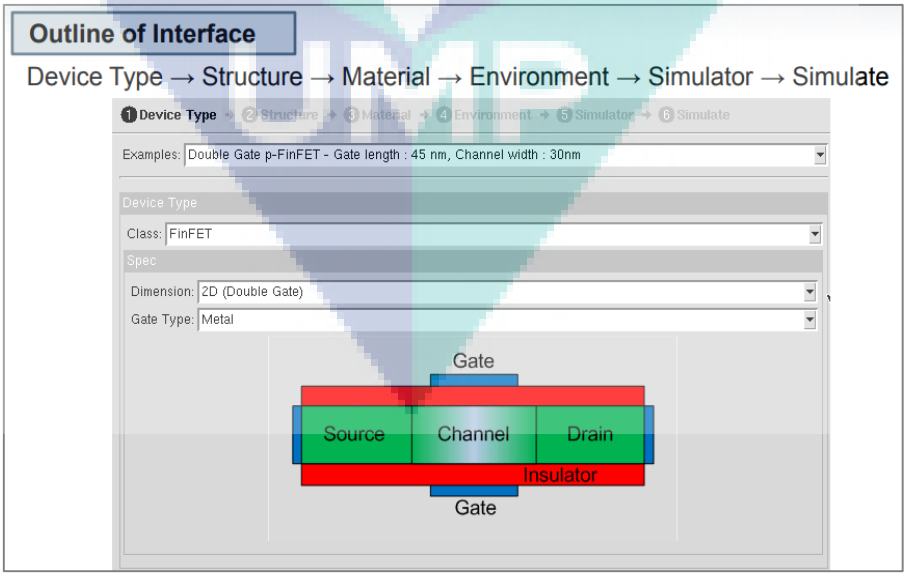

Figure 3.2 The "MuGFET " simulation tool homepage

3.4 Simulation Design

The process rule used to evaluate the electrical properties of FinFETs would be explained in detail in this section. This is done through four simulation scenarios to investigate the effect of the dimensions of the channel (length, width, oxide thickness and scaling factor) on electrical characteristics. The highest channel dimension was selected as 40 nm on the basis that the problem of leakage current and SCEs occur at channel length lower than 40 nm, similar to MOSFET. Then, this length was shrinking to achieve new Nano scale channel limits at 5 nm, while maintaining acceptable performance level. For the same reasons, initial channel width and oxide thickness were selected according to the previous studies, then scaling down to accomplish the aims of study by the design of optimal nanoscale channel dimensions for FinFETs. The scaling factor of channel dimensions, K was selected based on the obtained results from individual dimension scenarios for the aim of scaling down all channel dimensions as once. Table 3.1 listed the detailed simulation parameters for all scenarios.

Table 3.1 Simulation Parameters

Parameters	**Value**
Channel length (L)	(5, 10, 20, 40) nm
Channel width (W)	(5, 10, 15, 20) nm
Channel oxide thickness (T_{OX})	(1.5, 2.5, 5, 7) nm
Scaling factor (K)	(1.0, 0.5, 0.25, 0.125)
Channel concentration P-type	10^{16} cm^{-3}
Channel concentration N-type	10^{19} cm^{-3}
Gate voltage	0.5 - 5 V
Temperature	300 K

3.4.1 Selection of Semiconductor Material

The semiconductor parameters were selected initially selected as shown in Figure 3.3. Silicon (Si) was selected initially as a semiconductor and ending with the InAs.

Figure 3.3 Parameter selection
Source: http://www.ioffe.ru/SvA/NSM/Semicond/

The selection of silicon as a parameter in the simulator is illustrated in Figure 3.4. This is because these materials are very cheap and are available in nature as mentioned in the second chapter. At the same time, they are standardly used in the manufacture of integrated circuits.

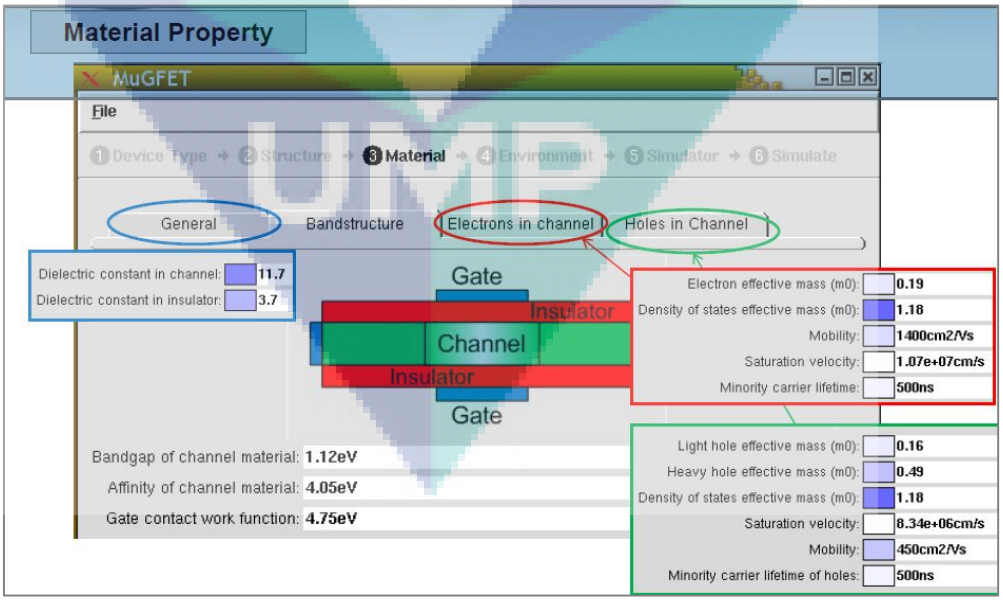

Figure 3.4 Selection of silicon parameters as a semiconductor in simulation

From environment option, select temperature 300k and the channel voltage will be selected from 0.5 to 5 V with a choice of 21 points. The number of points will be 21 points between the length and the voltage gate as shown in Figure 3.5.

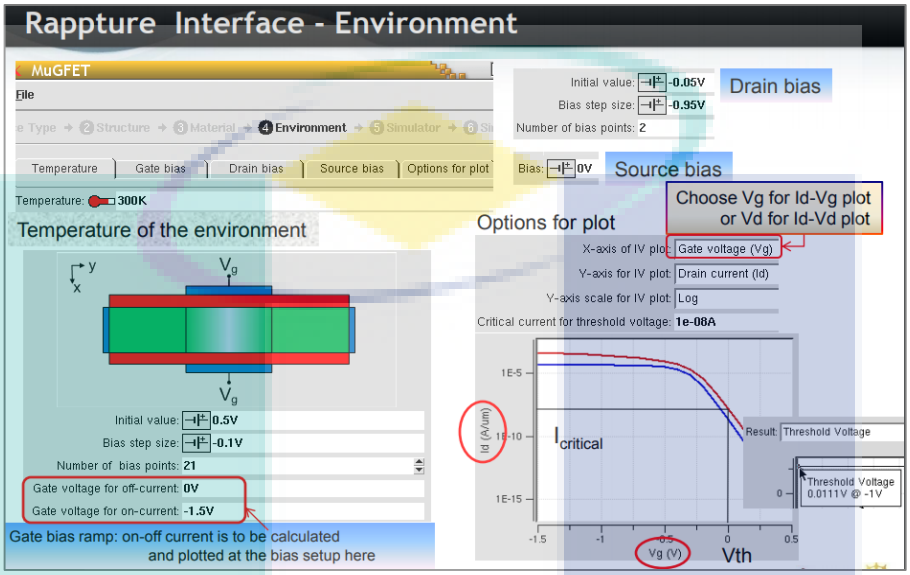

Figure 3.5 Voltage gate and temperature options

3.5 Selection of Channel Dimensions

This section explains how to select the dimensions of the channel and the effect of each dimension (length, width, the thickness of oxide) on the electrical properties. It also elucidated how to calculate the effect of the dimensions of the combined channel on the characteristics through the scaling factor K.

3.5.1 Channel Length Scenario

The first scenario was the channel length variables (i.e. 5, 10, 20 and 40) nm. The width of the channel and the oxide thickness was constant (i.e. W =5 nm, T_{OX} = 2.5 nm. After the simulation, the electrical properties were extracted for each length and then the properties were drawn with the length variable at certain points. The I_{ON}/ I_{OFF} ratio was calculated at V_{DD} =5 V and 0.5 V, the SS calculation at V_{DD} = 0.25 V and V_T at V_{DD} = 0.5 V and DIBL at V_{DD} = 0.75 V as shown in Figure 3.6.

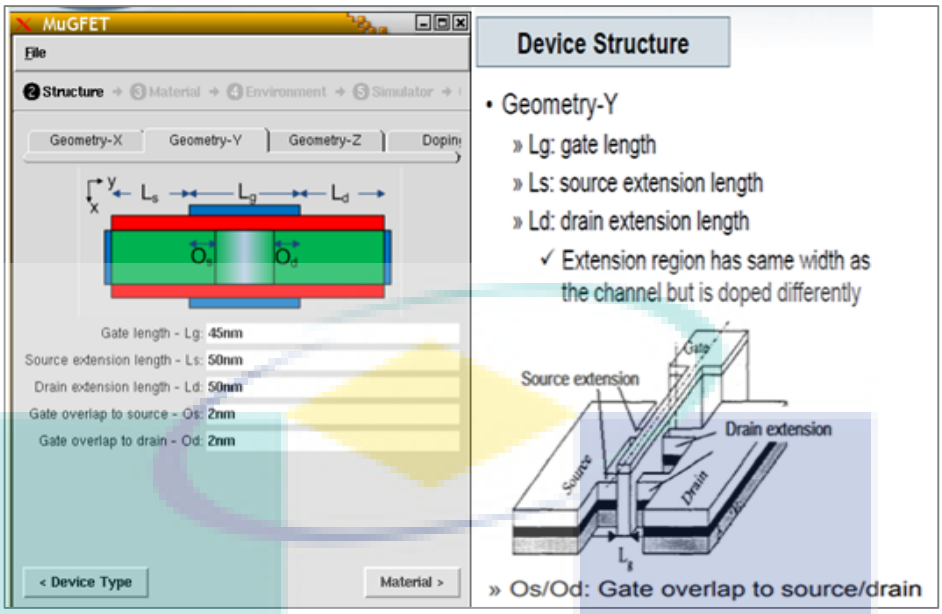

Figure 3.6 The channel length selection
Source: Choi et al., (2002)

3.5.2 Channel Width Scenario

The second scenario width of channel changes through 5, 10, 15, to 20 nm. While the length and oxide thickness will be constant L =40 nm T_{OX} =2.5 nm. The electrical properties are drawn in relation to the width change shown in Figure 3.7.

3.5.3 Oxide Thickness Scenario

The third scenario the oxide thickness changes as 1.5, 2.5, and 5, 7 nm with the stability of the value of the length and width. Then the data of properties will draw with the change in the oxide thickness shown in Figure 3.7.

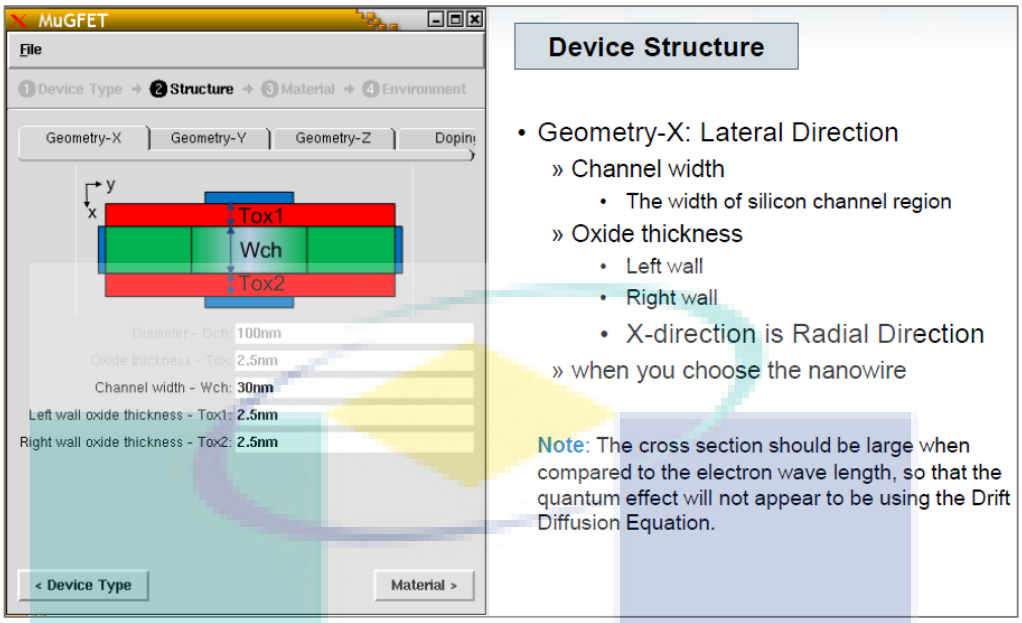

Figure 3.7 Selection of channel width and oxide thickness

3.5.4 Scaling Factor Scenario

The fourth scenario (i.e. length, width and oxide thickness) changes by scaling factor (K) and the data multiplied by 0.5. For example, if the initial length is 40 nm, the width 20 nm, the thickness 5 nm, and the second step will become length 20 nm, width 10 nm, thickness 2.5 nm and according to Table 3.2. The electrical properties will then be extracted and the extent of the scaling ratio was determined. This process is repeated by choosing other semiconductors (i.e. Ge, GaAs, and InAs etc.).

Table 3.2 The parameter used with condition scaling factor K. of Si-FinFET

K	L (nm)	W (nm)	T_{ox} (nm)
1.00	40	20	6
0.5	20	10	3
0.25	10	5	1.5
0.125	5	2.5	0.625

3.5.5 The I-V Characteristics

The electrical properties were extracted from the 'simulate' option and then the desired properties such as I_{ON}/I_{OFF}, SS, $V_{T,}$ and DIBL were thereafter drawn and the values extrapolated as illustrated in Figures 3.8, 3.9, and 3.10.

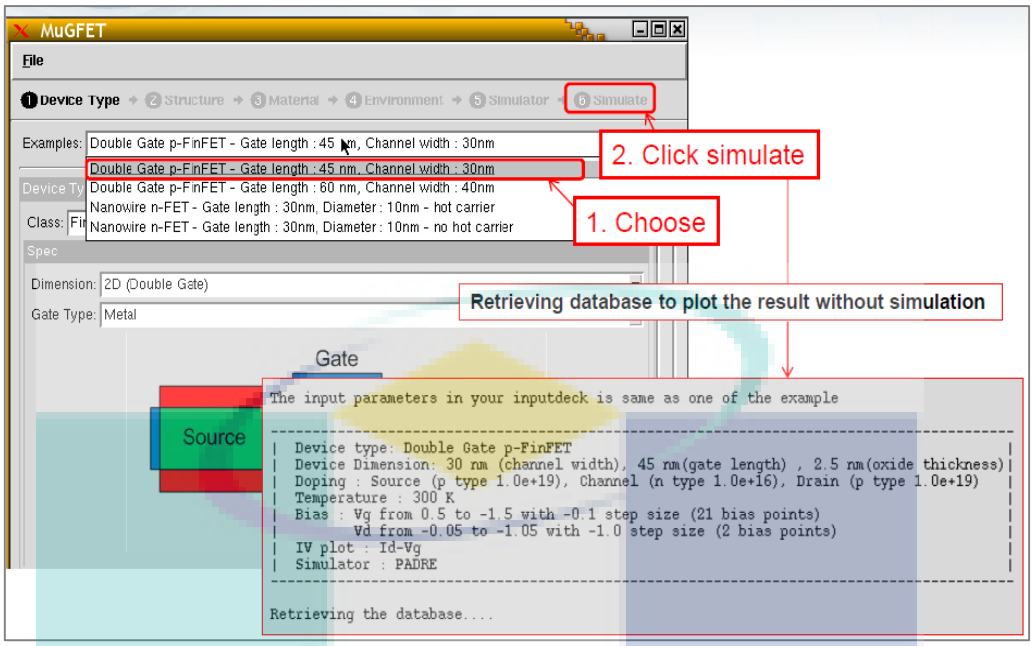

Figure 3.8 Selection of electrical characteristics from the 'simulate' option

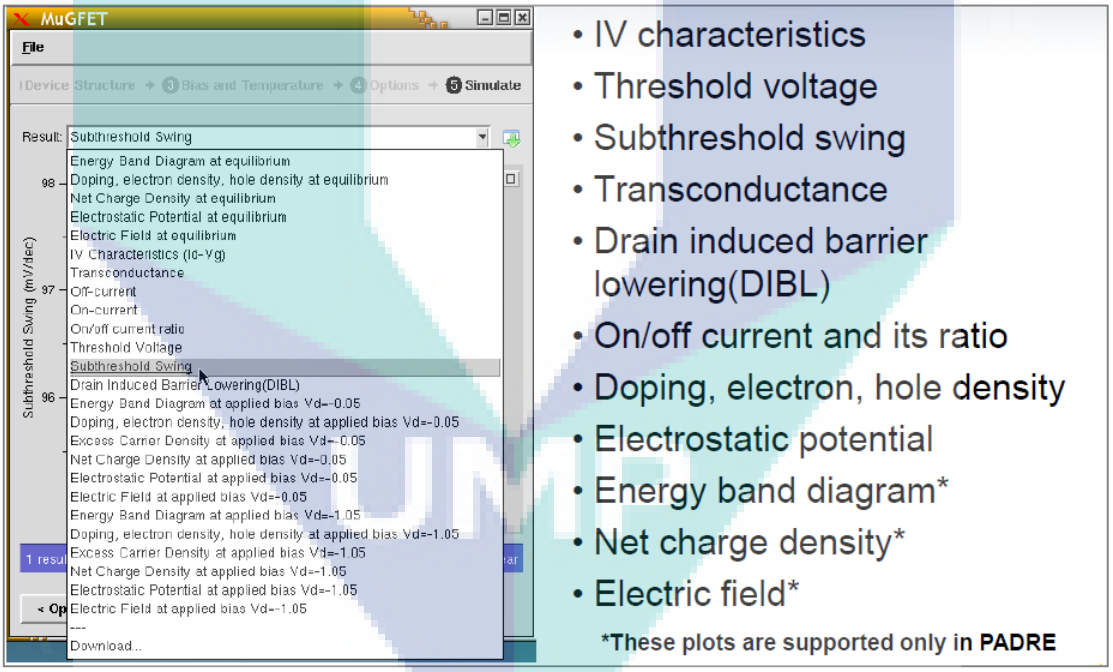

Figure 3.9 Selection of the electrical characteristic type

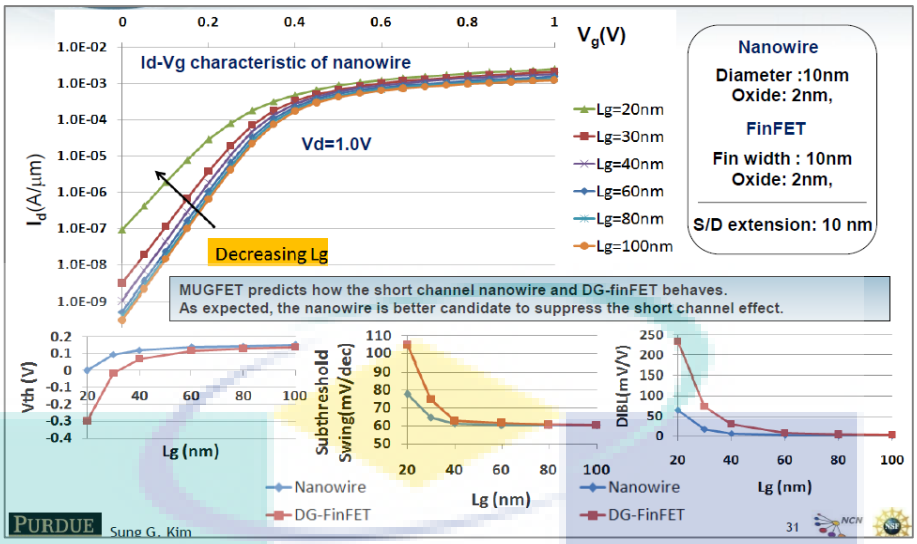

Figure 3.10 Description of how to extract and draw electrical properties with changing length (20 to 100) nm in FinFET and Nanowire.

3.6 Summary

The section focused on the systematic description of the simulation software employed in estimating the characteristics of FinFET and how to choose semiconductors by from different parameters. It also discussed how to change the dimensions in different scenarios, and finally highlighted how to extract electrical properties and estimate with the drawings.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Introduction

This chapter introduces simulation results and electrical characteristics of Si, Ge, GaAs and InAs FinFET transistors based on various channel's dimensions. The output characteristic curves of the transistor under different conditions and with different parameters were considered. The effects of variable channel dimensions such as channel length, width and oxide thickness in addition to scaling factor of the (Si, Ge, GaAs and InAs)-FinFET transistors, were determined based on the I–V characteristics that are derived from the conducted simulations. In this study, the I_d–V_g characteristics of (Si, Ge, GaAs and InAs)-FinFET at 300 K were simulated and evaluated with the simulation parameters. The SS-ideal represent the minimum sub-threshold swing that can be found with a yield 59.5 mV/dec at room temperature. Furthermore, four simulation experiments were designed to evaluate the performance of Si, Ge, InAs and InAs-FinFET in terms of the considered metrics. In the first scenario, channel length was changed, whereas other dimensions (W and T_{OX}) were kept constant. In the second scenario, the impact of changing channel width was investigated while both the length and thickness of the channel were kept constant. In the third scenario, oxide thickness was changed and length and width were fixed. Finally, the impacts of changing scaling factor were studied by changing the three dimensions at once, based on a changeable scaling factor K.

4.2 The Si-FinFET Scenarios

The MuGFET was utilized to investigate the electrical characteristics of the Si-FinFET transistor by varying dimensions of the channel. The electrical characteristics

were based on the I–V relation under varying conditions and were based on different parameters that were evaluated. The effects of variable channel dimensions such as channel length, width and oxide thickness, in addition to the scaling factor of the Si-FinFET transistor, were determined. Most importantly, the I_d–V_g characteristics of Si-FinFET at room temperature were simulated and analysed. The setting of simulation parameters in this study is listed in Table 4.1.

Table 4.1 List of Simulation Parameters

Parameters	Value
Channel length (L)	(5, 10, 20 and 40) nm
Channel width (W)	(5, 10, 15 and 20) nm
Oxide thickness (T_{OX})	(1.5, 2.5, 5 and 7) nm
Scaling factor (K)	(1.00, 0.5, 0.25and 0.125)
Channel concentration P-type	10^{16} cm^{-3}
Channel concentration N-type	10^{19} cm^{-3}

Four simulation scenarios were designed from different simulation parameters to evaluate the electrical characteristics of Si-FinFET based in relation to the channel's dimensions. The first scenario focused on the impact of varying channel length only, while keeping other dimensions (W and T_{OX}) constant. The second scenario investigated electrical characteristics based on various channel width, while both length and oxide thickness of channel were unchanged. In the third scenario, only oxide thickness was changed and other dimensions were kept constant. The last scenario was designed for simultaneous consideration of all dimensions, L, W, and T_{OX} by changing the scaling factor, K to decrease all dimensions and evaluate transistor performance for each value of K.

4.2.1 Effect of Varying Channel Length

The scaling down of channel length (L) and its effect on the electrical characteristics of InAs-FinFET was investigated. The simulation of transfer characteristics (i.e. drain current I_d –gate voltage Vg) was evaluated with different channel lengths. The optimal channel dimensions were selected based on the deliberated metrics of the performance characteristics. In this scenario, L was set to 5, 10, 20, and 40 nm, whereas W and T_{OX} were kept at default dimensions of MuGFET, which were 5

and 2.5 nm, respectively. Figure 4.1 shows the varying I_{ON}/I_{OFF} ratio with different channel length. It was observed that the I_{ON}/I_{OFF} ratio increases to 10^8 with increasing L from 5 to 40 nm at V_{DD} = 5 V. In contrast, at V_{DD} = 0.5 V, the highest value of I_{ON}/I_{OFF} ratio was more than 10^7 at L =40 nm. It was obvious that, for L range from 5 to 20 nm, the highest I_{ON}/I_{OFF} ratio occurred for V_{DD} = 0.5 V, while for 20 to 40 nm, L range the highest I_{ON}/I_{OFF} ratio occurred for V_{DD} =5 V which indicated that leakage current I_{OFF} smaller at L = 40 nm.

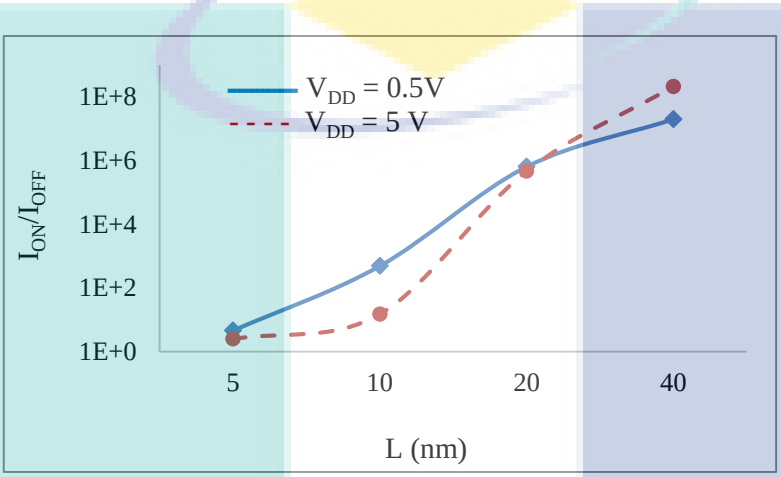

Figure 4.1 ION/IOFF ratio with a channel length of Si-FinFET

Figure 4.2 described the relation between the channel lengths with SS of the Si-FinFET. This figure illustrated that the value of SS starts with 86.6 mV/dec at L = 5 nm and becomes The furthest value from the ideal SS where SS = 169.9 mV/dec where transistor is slower, and at L = 40 nm this value decreases to 60.6 mV/dec and becomes the nearest value to the ideal SS (59.5 mV/dec) where the transistor is faster.

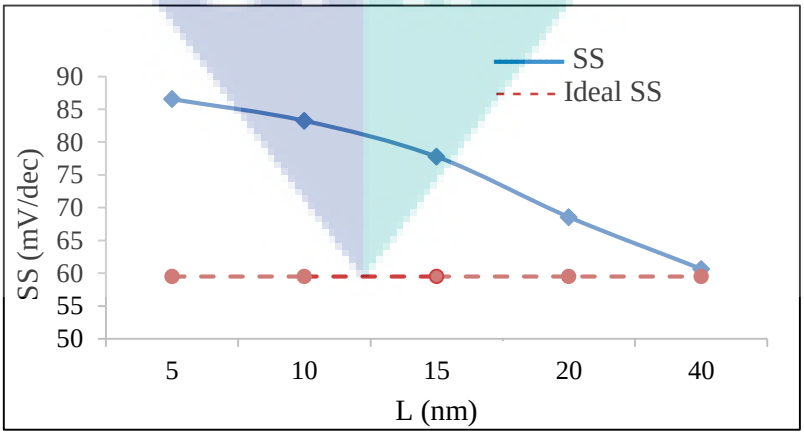

Figure 4.2 SS with a channel length of Si-FinFET

Figure 4.3 depicted the variation of both V_T and DIBL with different channel length. The value of V_T is proportionally increased with channel length from 0.24 at L = 5 nm at the lowest and reaches to 0.63 V at the longest channel. On the other hand, DIBL decreases as channel length increased from 392 mV/V at L = 5 nm until it reached only 7.8 mV/V at L = 40 nm. This rapid in reducing value DIBL allows the exchange of high-integration charge electrical. According to the obtained characteristics in this scenario, the best performance in terms of both the I_{ON}/I_{OFF} ratio and SS value can be achieved in the case with 40 nm channel length. So the best channel length was at L = 40 nm.

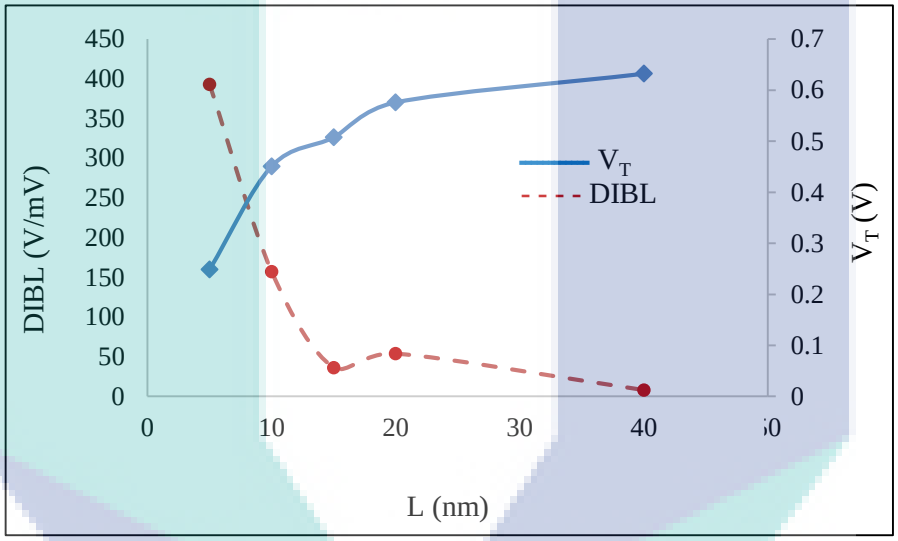

Figure 4.3 V_T and DIBL with a channel length of Si-FinFET

4.2.2 Effect of Varying Channel Width

The scaling down of channel width (W) and its effect on the characteristics of Si-FinFET were investigated in this scenario. The value of W was changed (5, 10, 15 and 20 nm) while L and T_{OX} were set to 40 nm and 2.5 nm, respectively. The I_{ON}/I_{OFF} ratio for both voltages (V_{DD} = 5 V and V_{DD} = 0.5 V) in terms of the varying width of the channel are illustrated in Figure 4.4. Unlike the channel length scenario, the ratio is inversely proportional with channel width. Ratios for both voltages drop down to approximately 10^3 when W increases to 20 nm. In contrast, the highest I_{ON}/I_{OFF} ratio (more than 10^8) was achieved for V_{DD} = 5 V where the leakage current I_{OFF} has the lowest value with the smallest channel width at W = 5 nm.

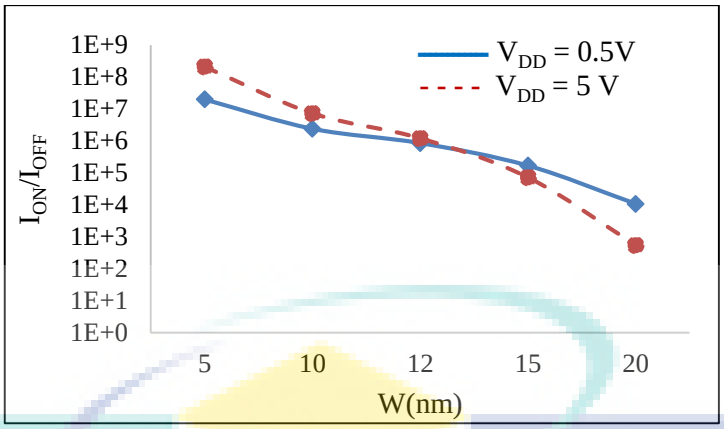

Figure 4.4 I_{ON}/I_{OFF} with a channel width of Si-FinFET

Figure 4.5 depicted the variation of SS value with variable channel width. It illustrated that the SS started with 60.65 mV/dec at W = 5 nm which represents the closest value from the ideal SS (95.5 mV/dec). The best value case the transistor was speed and increases with an increasing the channel width until it reaches the highest value (75.69 mV/dec) at W = 20 nm where slow transistor happens.

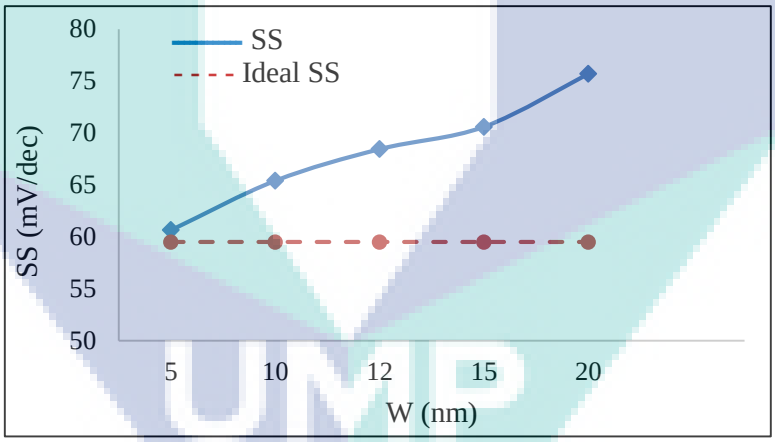

Figure 4.5 SS with a channel width of Si-FinFET

Figure 4.6 shows the relation between the channel width with threshold voltage (V_T) and drain-induced barrier lowering (DIBL) of the FinFET the observe value V_T decreased with increasing the channel width where V_T = 0.63 V at the higher value at W =5 nm and V_T = 0.47 V at the lower value at W = 20 nm. Finally, the DIBL increased as channel width increased until it reached 69.3 mV/V at the width of channel = 20 nm. This led to a slow exchange of charges. Hence, the best channel width was Si-FinFET at W =5 nm when minimal width.

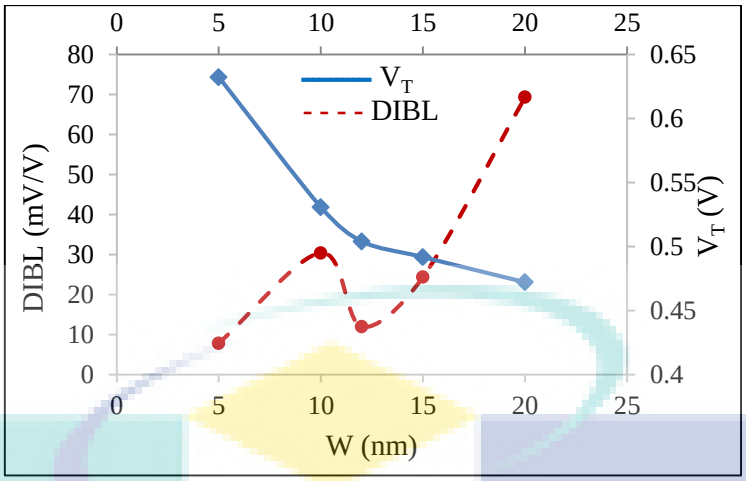

Figure 4.6 V_T, DIBL with a channel width of Si-FinFET

4.2.3 Effect of Varying Channel Oxide Thickness

The characteristics of silicon FinFET was investigated with scaling down of channel oxide thickness and its effect on the electrical characteristics. Figure 4.7 shows the I_{ON}/I_{OFF} ratio with the channel oxide thickness of 1.5, 2.5, 5 and 7 nm and at L = 40 nm and W =5 nm when increasing T_{OX} from 1.5 to 7 nm. The maximum value for I_{ON}/I_{OFF} ratio was more than 107 at V_{DD} =5 V at T_{OX} = 1.5 nm and after that decreased to about 102 at T_{OX} = 7 nm and for V_{DD} = 0.5 V, the I_{ON}/I_{OFF} ratio has the highest value (i.e. more than 106 at W = 1.5 nm and then decreased to 103 at T_{OX} = 7 nm. So with minimal T_{OX}, the leakage current at T_{OX} = 1.5 nm.

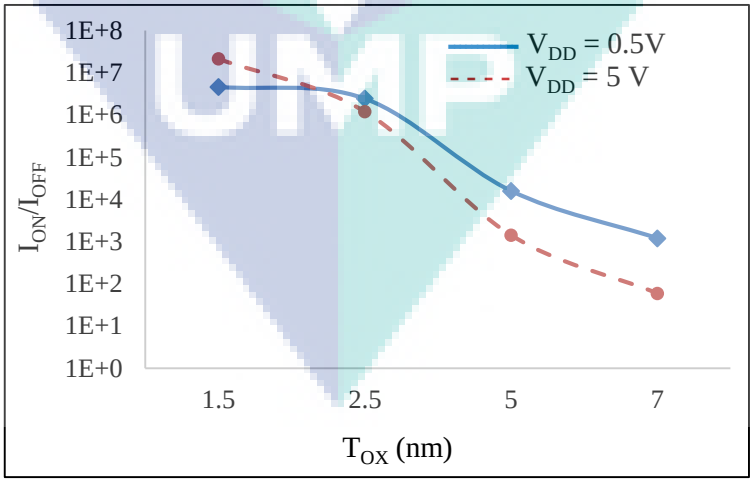

Figure 4.7 I_{ON}/I_{OFF} with an oxide thickness of Si-FinFET

Figure 4.8 presented the channel with characteristics of sub-threshold swing (SS) of the FinFET. In this result, the channel oxide thickness was (1.5, 2.5, 5 and 7) nm, the length (L = 40 nm) and width (W = 12 nm). This figure illustrates that the SS started with 62.85 mV/dec at T_{OX} = 1.5 nm which is the closest value to the ideal SS (59.5 mV/dec). The value represents the best SS with oxide thickness. Moreover, SS increased with increasing the channel oxide thickness until it reached to the highest value (106 mV/dec) at T_{OX} = 7 nm and this value represents the worst value of SS transistor to become slow.

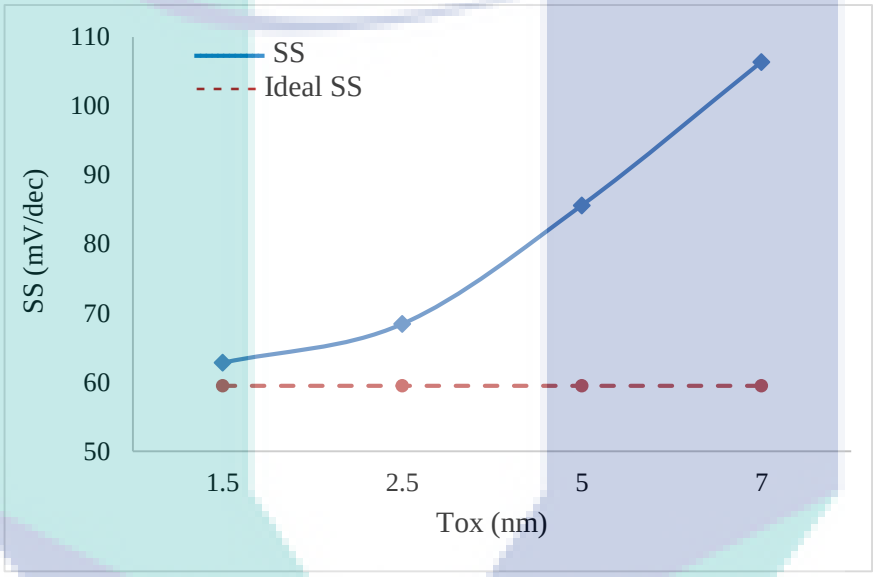

Figure 4.8 SS with an oxide thickness of Si-FinFET

Figure 4.9 presents the relation between channel oxide thickness with a threshold voltage (V_T) and drain-induced barrier lowering (DIBL) of the Si-FinFET. The V_T value increased with increasing channel oxide thickness where V_T = 0.49 V at T_{OX} = 1.5 nm. In addition, V_T = 0.53 V at channel oxide thickness of 7 nm with the DIBL finally increased from 5.49 mV/V to 99.3 mV/V. However, the oxide thickness increased from 1.5 to 7 nm, respectively. Hence, the best channel oxide thickness is the Si-FinFET at T_{OX} = 1.5 nm with minimal oxide thickness.

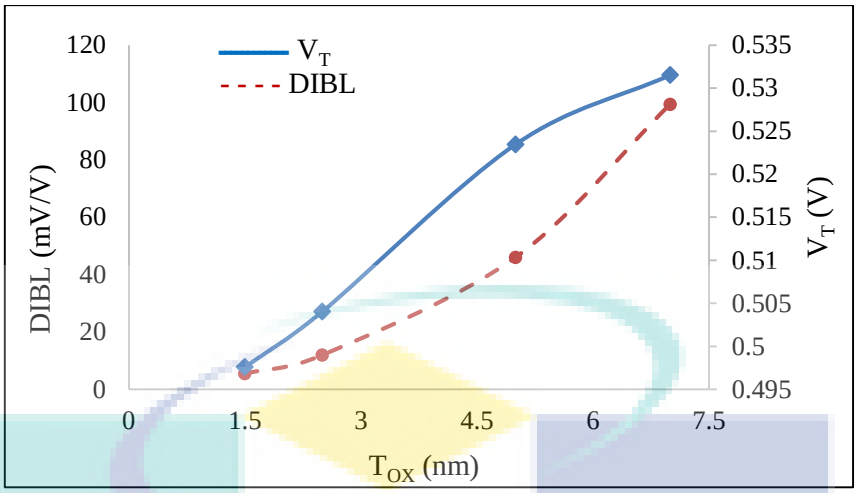

Figure 4.9 V_T and DIBL with channel oxide thickness of Si-FinFET

4.2.4 Effect of Varying Scaling Factor of Channel Dimensions

According to the aforementioned scenarios, the best performance in terms of the considered electrical characteristics was achieved at channel length L = 40 nm, channel width, W = 5 nm, and channel oxide thickness, T_{OX} =1.5 nm. Thus, Si-FinFET could not achieve a proper performance with a shrinking channel length where it attains better performance at the longest channel case. In order to scale down all channel dimensions at once, a scaling factor K was applied to all dimensions including, length, width, and thickness. Thereafter the electrical characteristics were investigated based on the scaling factor. The reference value of 'K' is defined as "1" with its highest channel dimensions. Then, all dimensions scaled down to new physical limits for the channel of Si-FinFET. All corresponding dimensions to the defend scaling factors are presented in Table 4.2.

Table 4.2 The parameter used with condition scaling factor K. of Si-FinFET

K	**(L nm)**	**W (nm)**	**T_{OX} (nm)**
1.00	40	20	6
0.5	20	10	3
0.25	10	5	1.5
0.125	5	2.5	0.625

Figure 4.10 shows the relation between the I_{ON}/I_{OFF} ratio with the scaling factor K from 0.125 to 1.00 Obviously, we can notice the improvement in I_{ON} /I_{OFF} characteristics by downscaling all channel dimensions together. The best value of I_{ON}

/I_{OFF} ratio was higher than 10^7 which is achieved at scaling factor of K = 0.125 for both V_{DD} = 5 V and for V_{DD} = 0.5 V. The worst I_{ON} /I_{OFF} ratios (less than10^4) occurred at the reference value of scaling factor for V_{DD} = 5 V and less than 10^3 V for a V_{DD} = 0.5 V. This indicated that the best value of I_{ON} /I_{OFF} ratio at the lowest scaling factor K where minimal leakage current I_{OFF}.

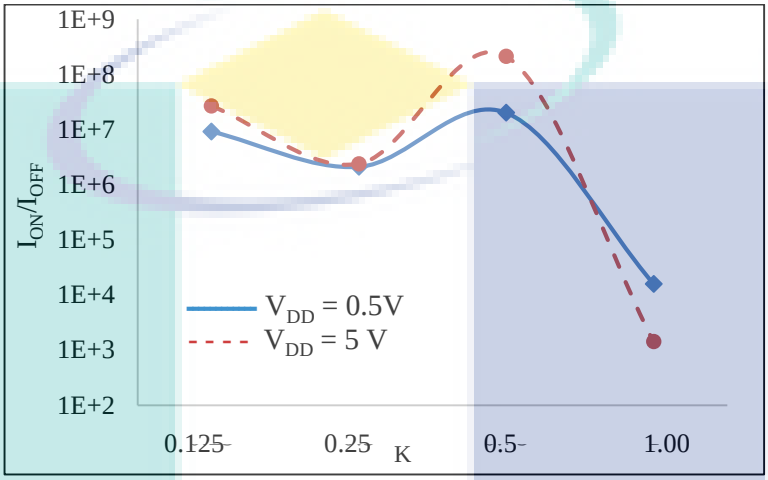

Figure 4.10 I_{ON}/I_{OFF} with scaling factor of Si-FinFET

Figure 4.11 presented the relationship between the scaling factors K with sub-threshold swing (SS) for Si-FinFET. The Figure 4.11 illustrated the furthest value of SS from the ideal SS (59.5 mV/dec) at K = 1.00 where SS = (85.6 mV/dec) while at K = 0.125 the nearest value to the ideal SS (62.2 mV/dec. Therefore, with increased K-value the SS increased significantly and lead to decrease speed in the transistor.

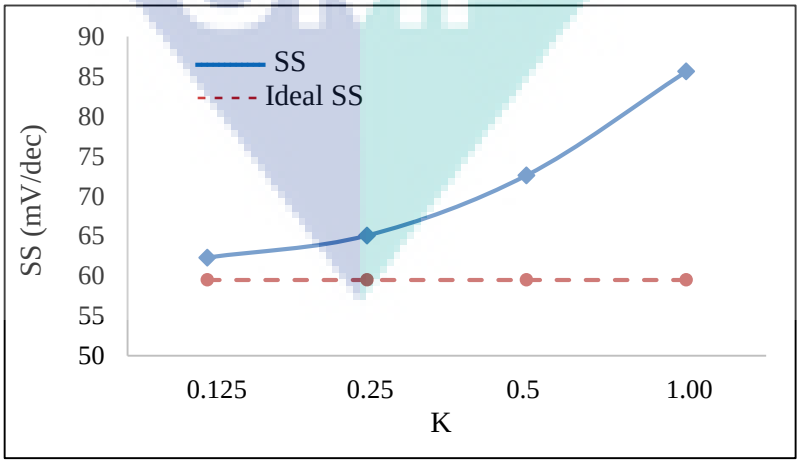

Figure 4.11 SS with scaling factor (K) of Si-FinFET

Figure 4.12 presents the relation between scaling factor K with a threshold voltage (V_T) and drain-induced barrier lowering (DIBL) of the Si-FinFET. Where V_T = 0.74 V (the higher value) happen at K=0.5 and V_T = 0.49 V at the lowest value at K = 1. Finally, the DIBL value ranges from 45 to 50 mV/V until it reached 49.99 mV/V at K = 0.125. This indicated that the charge exchange is almost stable at the different dimensions of the silicon channel. Also, the best channel scaling factor for Si-FinFET at K = 0.125 when minimal scaling factor. Table 4.3 summarizes the main findings of Si-FinFET as described above.

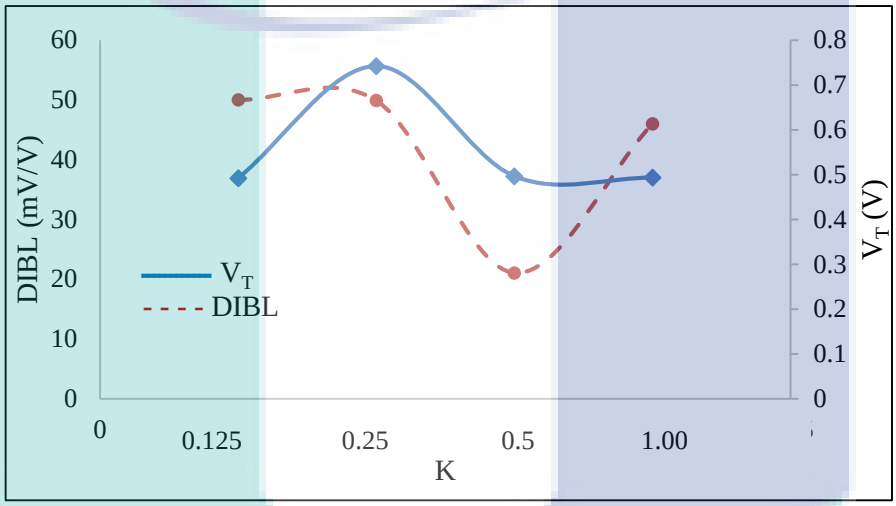

Figure 4.12 V_T and DIBL with scaling factor of Si-FinFET

Table 4.3 Summary of Si-FinFET main findings

Scenario	Characteristics	Value
Scenario 1	I_{ON}/I_{OFF}	2.12×10^8
	SS(mV/dec)	60
L	Best L(nm)	40
Scenario 2	I_{ON}/I_{OFF}	2.12×10^8
	SS(mV/dec)	60
W	Best W(nm)	5
Scenario 3	I_{ON}/I_{OFF}	2.15×10^7
	SS(mV/dec)	62
T_{OX}	Best T_{OX} (nm)	1.5
Scenario 4	I_{ON}/I_{OFF}	2.15×10^7
	SS(mV/dec)	62.2
K	Best K	0.125

4.3 The GaAs-FinFET Scenarios

This section investigated the effect of channel dimensions on the I–V characteristics of GaAs-FinFET. A simulation tool (MuGFET) was used to investigate the effect of channel dimensions on its electrical characteristics. The I_d–V_g characteristics of GaAs- FinFET at the temperature of 300 K were simulated with the parameters as listed in Table 4.4.

Table 4.4 Simulation Parameters

Parameters	Value
Channel length (L)	(10, 15, 20 and 40) nm
Channel width (W)	(5, 10, 12, 15 and 20) nm
Oxide thickness (T_{OX})	(1.5, 2.5, 5 and 7) nm
Scaling factor (K)	(0.25, 0.5, 0.75 and 1.00)
Channel concentration P-type	10^{16} cm^{-3}
Channel concentration N-type	10^{19} cm^{-3}

4.3.1 Effect of Varying Channel Length

The effect of scaling down the channel length on the characteristics of GaAs-FinFET was investigated in this simulation scenario. The simulation of transfer characteristics (drain current Id – gate voltage Vg) was scaled down with different channel lengths (L), the channel width (W), and oxide thicknesses (T_{OX}). Four limitation parameters were considered to find the optimal channel dimensions: (i) I_{ON}/I_{OFF} ratio (where I_{OFF} is the Id value at OFF state with Vg = 0 V and ION is the Id value at ON state with Vg = 1 V), (ii) Sub-threshold swing (SS), (iii) Threshold voltage (V_T) and (iv) Drain-induced barrier lowering (DIBL). In this case, the value of L was changed to 10, 15, 20, and 40 nm, while the channel width and T_{OX} were fixed at W = 5 nm and T_{OX} = 2.5 nm, respectively.

Figure 4.13 shows the relation between the I_{ON}/I_{OFF} ratio with the different GaAs-FinFET channel length. The I_{ON}/I_{OFF} ratio increases up to more than 10^8 for increasing L from 10 to 40 nm for V_{DD} = 5 V, and for V_{DD} = 0.5 V, the maximum value of I_{ON}/I_{OFF} ratio is more than108 at L = 35 nm. It is noticed that for L range from 10 to

25 nm the highest I_{ON}/I_{OFF} happen for V_{DD} = 0.5 V, while for 25 to 40 nm L range, the highest I_{ON}/I_{OFF} ratio occurs for V_{DD} = 5 V.

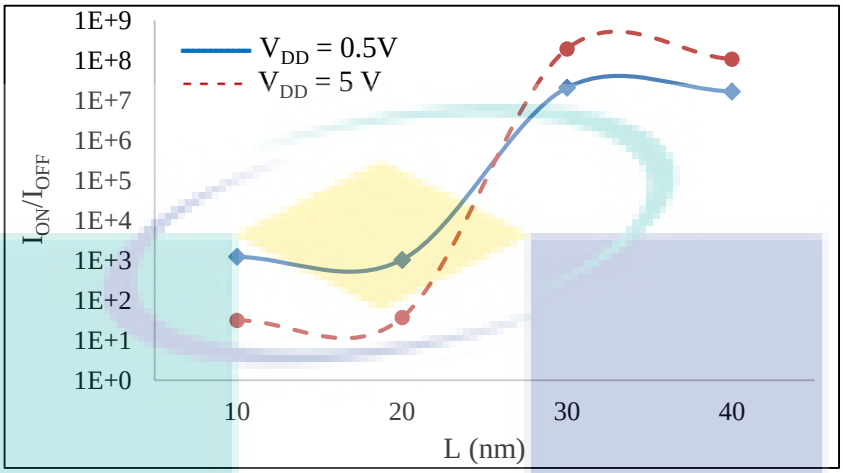

Figure 4.13 I_{ON}/I_{OFF} with a channel length of GaAs-FinFET

Figure 4.14 shows the relation between channel lengths with SS value. The SS started with 163 mV/dec at L = 10 nm which is the furthest value from the ideal SS (59.5 mV/dec) and then decreases with increasing the channel length, at L = 30 to 40 nm the closest value to the ideal SS (59.65 mV/dec) was achieved.

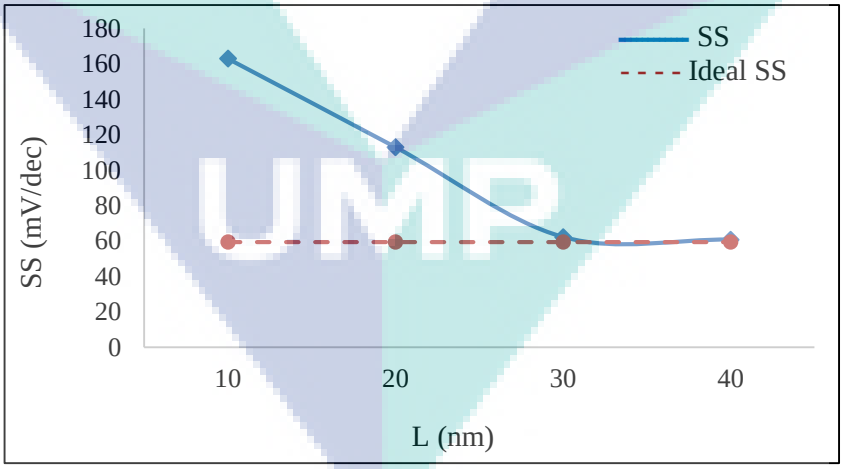

Figure 4.14 SS with a channel length of GaAs-FinFET

The characteristics of V_T and DIBL of the GaAs-FinFET with respect to channel length are illustrated in Figure 4.15. The value of V_T is increased with increasing the channel length from 0.43 V at 10 nm to 0.50 V at 40 nm. In contrast, the DIBL is

decreased as channel length increased until it reached 5.52 mV/V at 40 nm length of channels. Where the best electrical conductivity occurs.

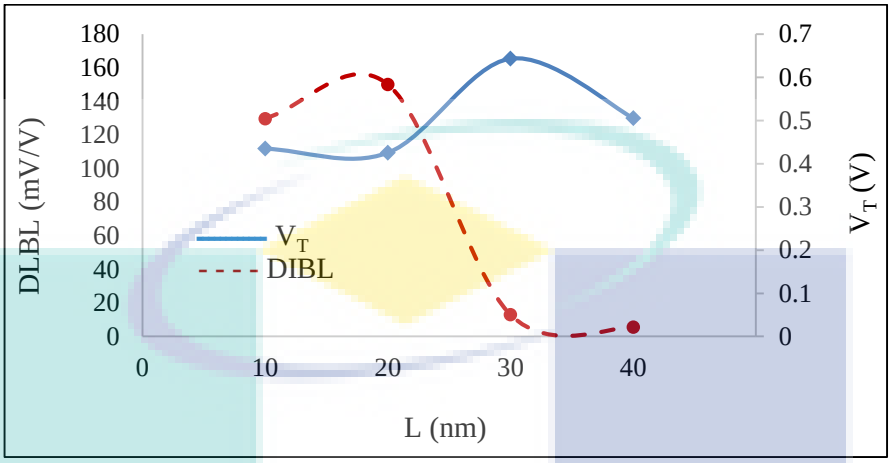

Figure 4.15 V_T and DIBL with a channel length of GaAs-FinFET

4.3.2 Effect of Varying Channel Width

In this case, the impact of scaling down the channel width, W, on the GaAs-FinFET characteristics was investigated. The value of W was changed to 5, 10, 15 and 20 nm while keeping L at 40 nm and T_{OX} at 2.5 nm. Figure 4.16 represents I_{ON}/I_{OFF} ratio with the channel width. At W = 20 nm, the value of I_{ON}/I_{OFF} ratio decreases from 10^8 to 10^2 for V_{DD} = 5 V, and from 107 to 104 for V_{DD} = 0.5 V. It is noticed that for W range from 5 to 12 nm the highest I_{ON}/I_{OFF} ratio happen for V_{DD} = 5 V, while for 12 to 20 nm W range highest I_{ON}/I_{OFF} ratio occur for VDD = 0.5 V. where the minimal leakage current ratio.

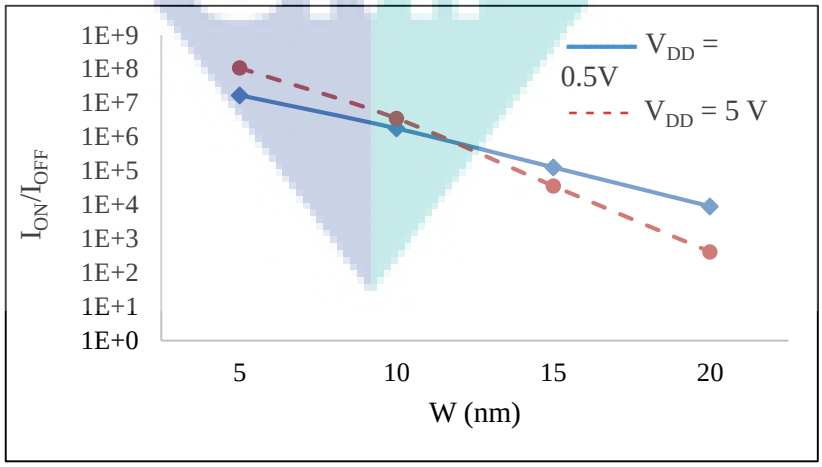

Figure 4.16 I_{ON}/I_{OFF} with a channel width of GaAs-FinFET

Figure 4.17 illustrates sub-threshold swing (SS) characteristics in terms of channel width. This figure revealed that the SS started with 60.8 mV/dec at W = 5 nm which is the nearest value to the ideal SS (59.5 mV/dec), where the transistor is faster and increases with increasing the channel width until it reaches the highest value 74.9 mV/dec at 20 nm.

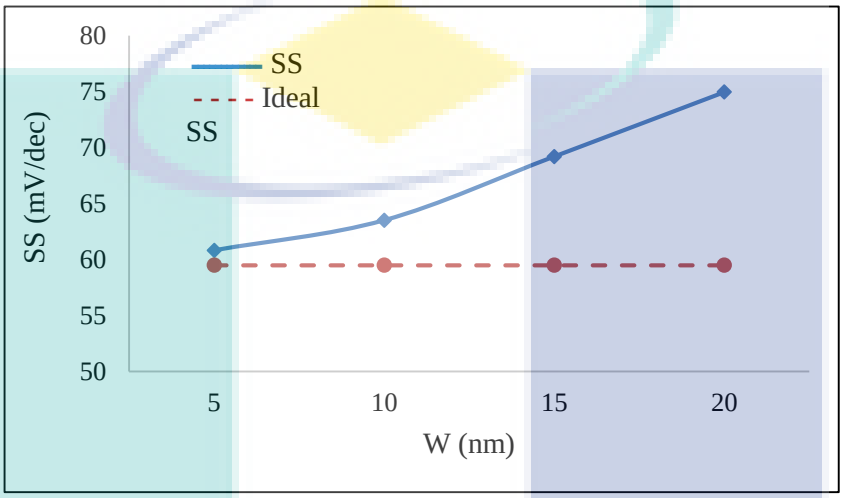

Figure 4.17 SS with a channel width of GaAs-FinFET

The relation between channel width with V_T and DIBL are shown in Figure 4.18. The V_T decreases with increasing the channel width. In contrast, the DIBL value increases as channel width increased from 50.5 mV/V at W = 5 nm to 81.4 mV/V at a channel width of 20 nm. Where the least electrical conductivity occurs.

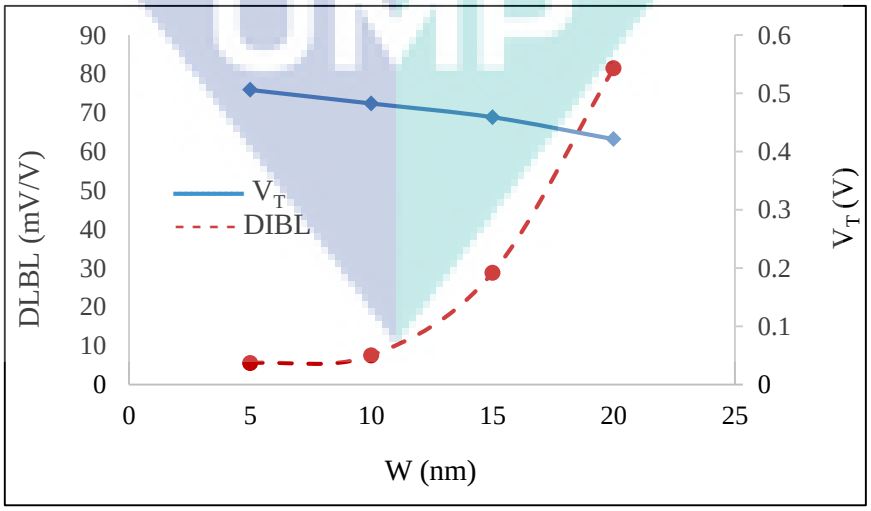

Figure 4.18 V_T and DIBL with a channel width of GaAs-FinFET

4.3.3 Effect of Varying Channel Oxide Thickness

The scaling down of channel oxide thickness and its impact on the characteristics of GaAs-FinFET were explored in this section. T_{OX} was changed from 1.5 to 7 nm while L was fixed at 40 nm and W at 5 nm as shown in Figure 4.19.

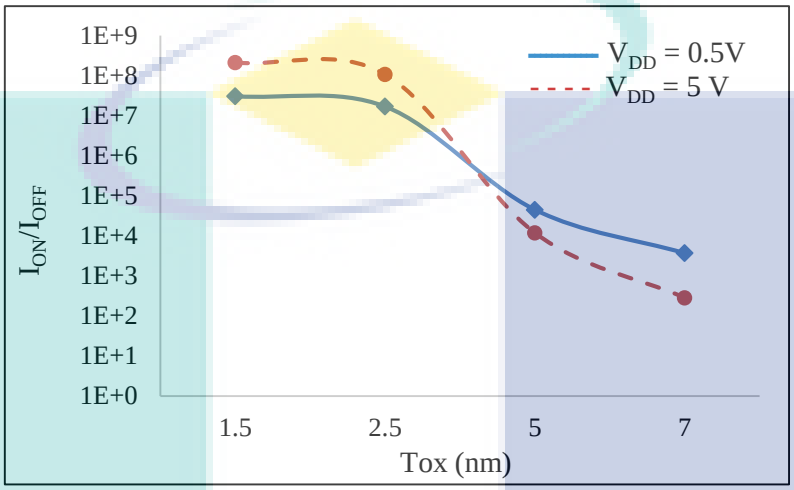

Figure 4.19 I_{ON}/I_{OFF} with an oxide thickness of GaAs-FinFET

The ratio reduced more than 10^7 at T_{OX} = 1.5 nm to 10^4 at 7 nm. The relation between T_{OX} and SS was shown in Figure 4.20. The SS starts with 60.2 mV/dec at T_{OX} = 1.5 nm which is the closest value to the ideal SS, where transistor the faster and increases to more than 160 mV/dec with increasing the T_{OX} to 7 nm.

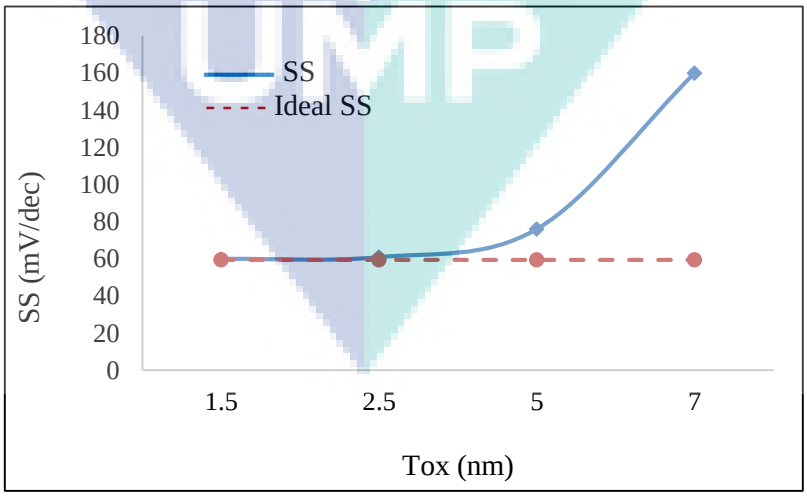

Figure 4.20 SS with an oxide thickness of GaAs-FinFET

Similarly, the effect of varying channel oxide thickness on V_T and DIBL characteristics is presented in Figure 4.21. It was obvious that the value of V_T almost stables regardless of the channel oxide thickness. On the other hand, the DIBL increases from 0.54 mV/V to 70.9 mV/V at the oxide thickness of channel varied from 1.5 to 7 nm.

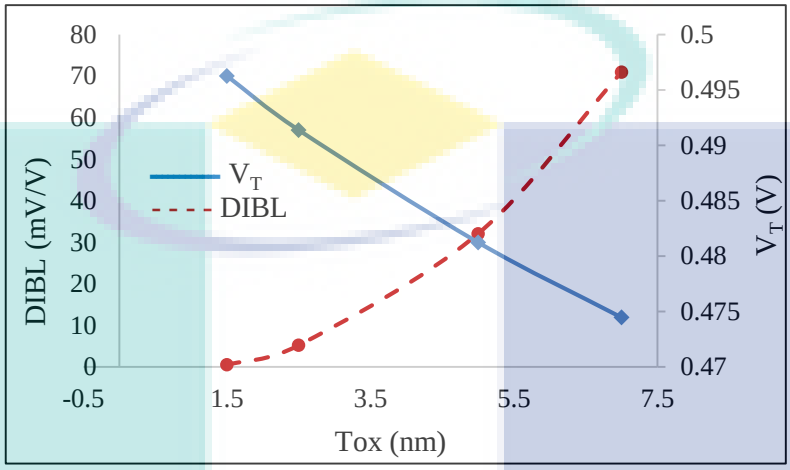

Figure 4.21 V_T and DIBL with channel oxide thickness of GaAs-FinFET

4.3.4 Effect of Varying Scaling Factor of Channel Dimensions

The scaling down of channel dimensions and its effect on the characteristics of GaAs-FinFET was simulated for the same voltage range in all simulations. The length, width, and thickness will be scale-down by a factor (K), while K = 0.125 represent the minimal dimension's value and K = 1 represents the original dimensions as summarized in Table 4.5.

Table 4.5 The parameter used with condition scaling factor K. of GaAs-FinFET

K	L (nm)	W (nm)	Tox (nm)
0.125	8	3	1
0.25	10	5	1.5
0.5	20	10	3
1.00	40	20	6

Figure 4.22 shows the relation between the I_{ON}/I_{OFF} ratio with the scaling factor K from 0.125 to 1. The maximum value of I_{ON}/I_{OFF} ratio is higher than 10^6 occurs at scaling factor K = 0.125 for both V_{DD} =5 V and for V_{DD} = 5 V. After that the I_{ON}/I_{OFF} ratio was decreased significantly to 10^1 at K = 1.00 for V_{DD} = 5 V compared to more than 10^3 for V_{DD} = 5 V. Figure 4.23 shows the furthest SS value (189 mV/dec) from the

ideal SS that obtained at K = 1.00 in contrast, the nearest value to the ideal SS (65.7 mV/dec) was obtained at K = 0.125. Therefore, with increasing K, the SS value is increased significantly.

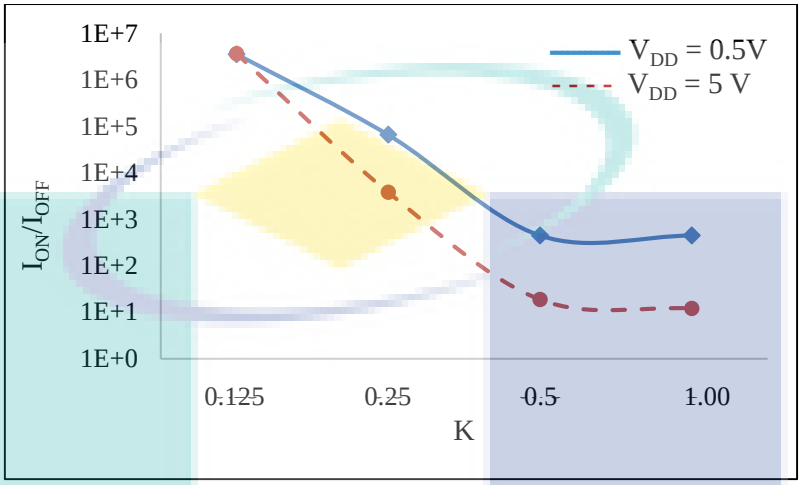

Figure 4.22 I_{ON}/I_{OFF} with scaling factor of GaAs-FinFET

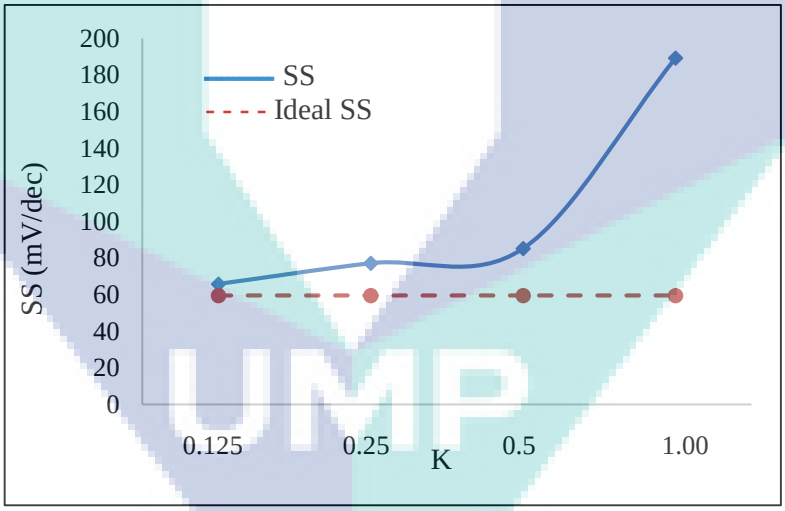

Figure 4.23 SS with scaling factor of GaAs-FinFET

The impact of changing scaling factor (K) on V_T and DIBL is illustrated in Figure 4.24. Where the highest value of VT = 0.62 V is obtained at K = 0.125, compared to the lowest value, VT = 0.36 V at K =1.00 Conversely, the DIBL value ranges from 48 mV/V at K = 0.125 to 298 at K = 1.00

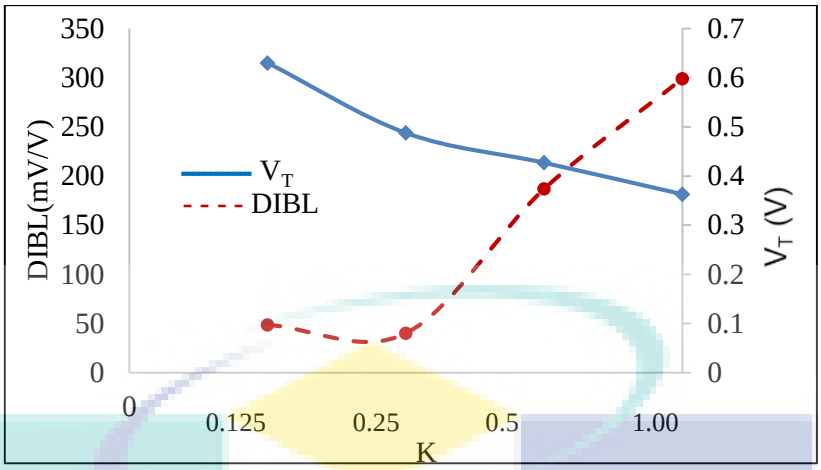

Figure 4.24 V_T and DIBL with scaling factor of GaAs-FinFET

The effects of channel dimensions (i.e. length, width, and oxide thickness) on the selected characteristics of GaAs-FinFET were investigated and analysed using MuGFET simulation tool. Highest I_{ON}/I_{OFF} ratio and nearest SS to the ideal value were considered to select the optimal dimensions of GaAs-FinFET. According to simulation results, the higher L (= 32 to 40 nm), the lower W (= 5 nm), and the lower T_{OX} (= 1.5 nm) are the optimal dimensions for GaAs-FinFET. For scaling factor (K), the optimal value was at K= 0.125. This value of K represents the lowest dimensions of the transistor as shown in Table 4.6.

Table 4.6 Summary of GaAs-FinFET main findings

Semiconductor	**GaAs**
I_{ON}/I_{OFF}	1.08×10^{8}
SS(mV/dec)	59.65
Best L(nm)	30-40
I_{ON}/I_{OFF}	1.08×10^{8}
SS(mV/dec)	60
Best W(nm)	5
I_{ON}/I_{OFF}	2.11×10^{8}
SS(mV/dec)	59.7
Best T_{OX} (nm)	1.5-2.5
I_{ON}/I_{OFF}	3.65×10^{6}
SS (mV/dec)	65.7
Best K	0.125

4.4 The Ge-FinFET Scenarios

The MuGFET was utilized to investigate the characteristics of the Ge-FinFET transistor by varying dimensions of the channel. The electrical characteristics based on the I–V relation under various conditions and based on different parameters were studied and evaluated. The effects of variable channel dimensions such as the channel length, width and oxide thickness in addition to the scaling factor of the Ge-FinFET transistor, were determined. In particular, the I_d–V_g characteristics of Ge-FinFET at the temperature of 300 K are simulated and analysed. The setting of simulation parameters in this study is listed in Table 4.7.

Table 4.7 The simulation parameters

Parameters	Value
Channel length (L)	(10, 15, 20 and 40) nm
Channel width (W)	(5, 10, 12, and 20) nm
Oxide thickness (T_{OX})	(1.5, 2.5, 5 and 7) nm
Scaling factor (K)	(0.125, 0.25, 0.5 and 1.00)
Channel concentration P-type	10^{16} cm^{-3}
Channel concentration N-type	10^{19} cm^{-3}

In order to evaluate the electrical characteristics of Ge-FinFET based on channel's dimensions, four simulation scenarios were designed for different simulation parameters. The first scenario focused on the impact of varying channel length only, while keeping other dimensions (W and T_{OX}) constant. The second scenario investigated electrical characteristics based on various channel width while both length and oxide thickness of channel were unchanged. In the third scenario, only oxide thickness was changed and other dimensions were kept constant. The last scenario was designed for simultaneous consideration of all dimensions, L, W, and T_{OX} by changing the scaling factor, K to decrease all dimensions and evaluate transistor performance for each value of K.

4.4.1 Effect of Varying Channel Length

This scenario investigated the effect of channel length scale down on the characteristics of Ge FinFET. The channel length, L was changed between 10 and 40

nm, whereas W and T_{OX} were kept constant at default values of MuGFET that are 5 nm and 2.5 nm respectively. The simulation of transfer characteristics (drain current I_d – gate voltage Vg) have been conducted with different channel lengths (L). Figure 4.25 shows the varying I_{ON}/I_{OFF} ratio with a different channel length of Ge-FinFET. We can notice that the I_{ON} /I_{OFF} ratio is proportionally increased with channel length at both voltages, V_{DD} = 5 V and 0.5 V. The maximum value of I_{ON}/I_{OFF} ratio was more than 10^4 at L = 40 nm.

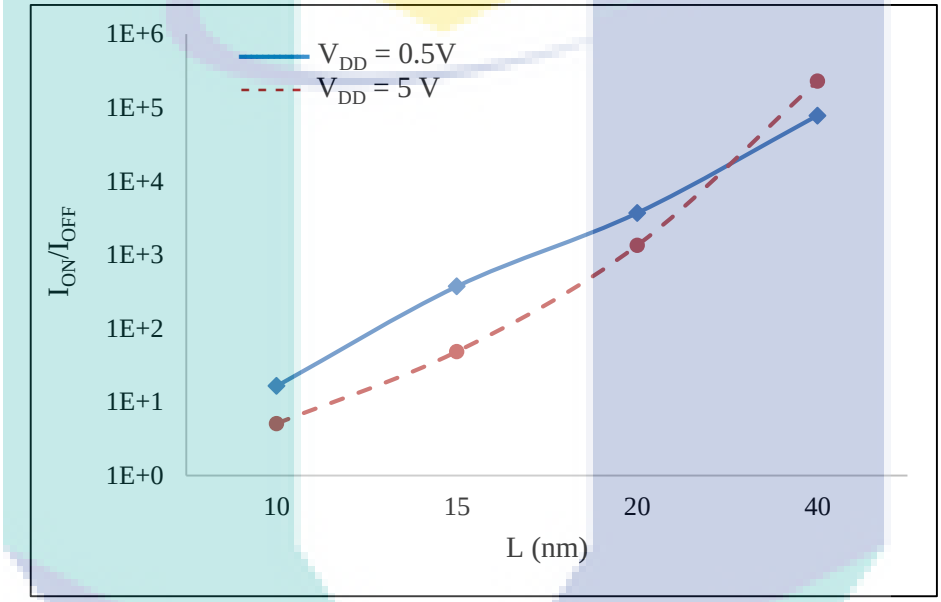

Figure 4.25 I_{ON}/I_{OFF} with a channel length of Ge-FinFET

For L range from 10 to 30 nm the highest I_{ON}/I_{OFF} ratio happens for V_{DD} = 5 V, while for 30 to 40 nm, L range the highest I_{ON}/I_{OFF} ratio occurs for V_{DD} = 5 V. The relation between SS characteristic and channel lengths is illustrated in Figure 4.26. It shows that the SS is improved as the channel length increased and reached 65 mV/dec the nearest value to the ideal SS at L = 40 nm.

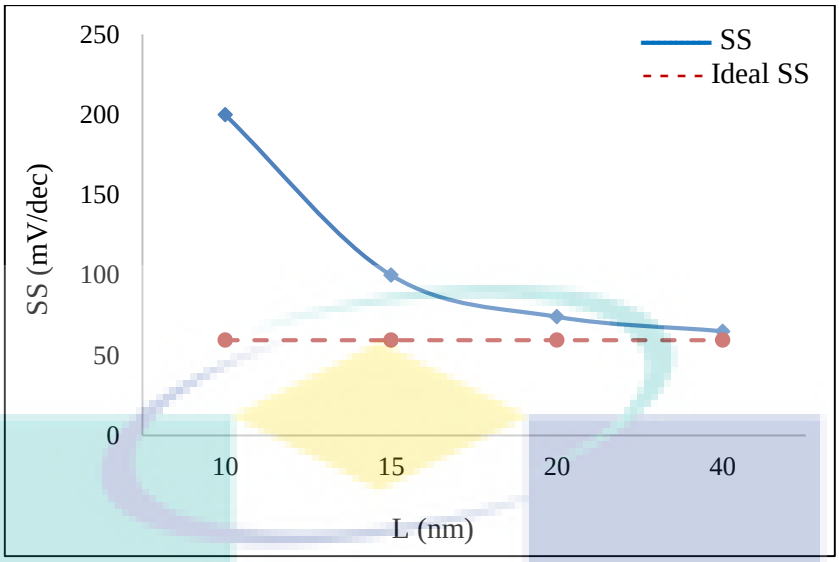

Figure 4.26 SS with a channel length of Ge-FinFET

Regarding the threshold voltage (V_T), Figure 4.27 depicts the gain in V_T characteristics with increasing the channel length, where V_T = 0.43 V at the maximum L of 40 nm and V_T = 0.20 V at the minimum L of 10 nm. Conversely, drain-induced barrier lowering (DIBL) of the Ge-FinFET reduces with increasing channel length and reaches to 4.8 mV/V at L = 40 nm as shown in Figure 4.27.

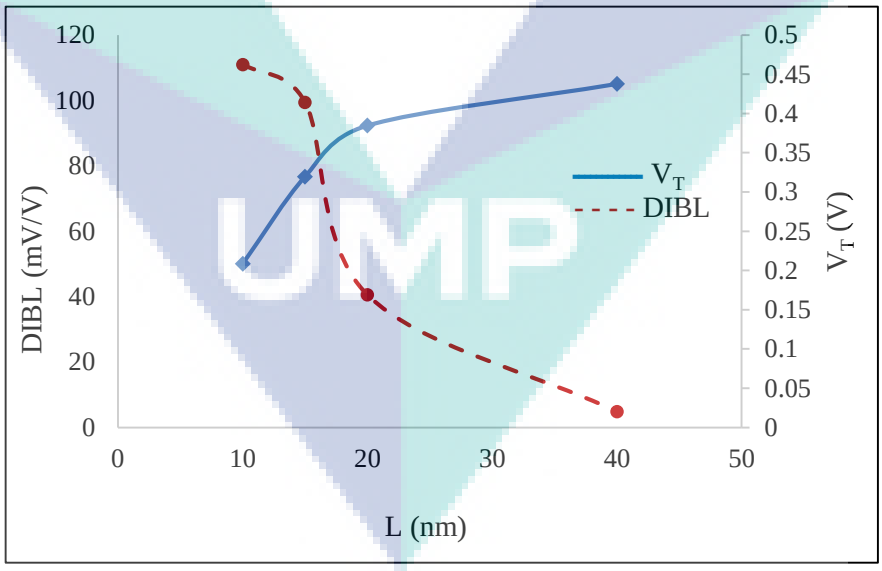

Figure 4.27 V_T and DIBL with a channel length of Ge-FinFET

According to the obtained characteristics in this scenario, the best performance in terms of all performance metrics can be achieved in the case with 40 nm channel length. Therefore, it is obvious that with considering channel length only, we cannot go

far in downscaling channel dimensions due to the degradation of transistor performance, especially in short length channel.

4.4.2 Effect of Varying Channel Width

The impact of scaling down channel width, W and on the considered performance metrics of Ge-FinFET was evaluated in this scenario. The value of W was decreased from 20 nm to 5 nm while L and T_{OX} were fixed to 40 nm and = 2.5 nm respectively. Unlike the previous scenario, the downscaling of channel width improved the performance of the transistor in terms of all characteristics as shown in Figure 4.28.

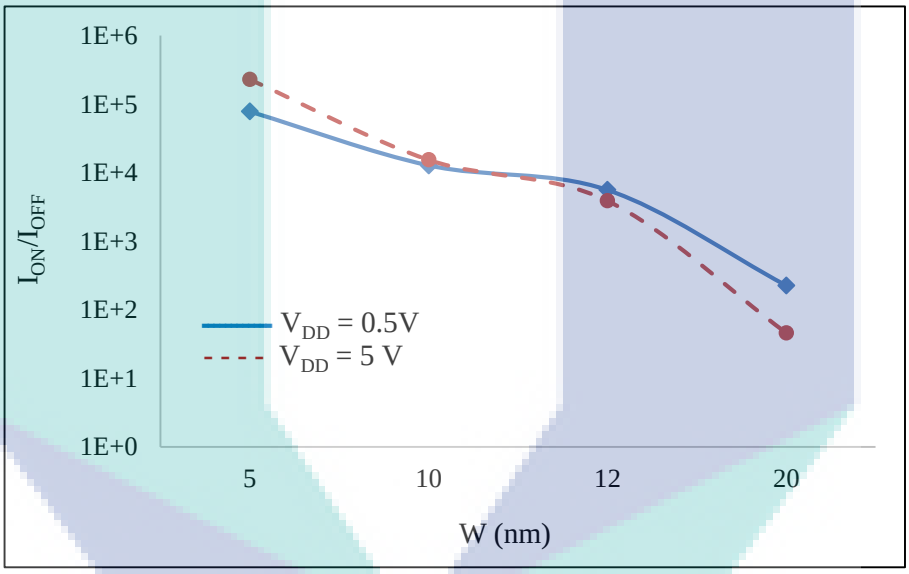

Figure 4.28 I_{ON}/I_{OFF} with a channel width of Ge-FinFET

The best performance was achieved with the smallest channel width, W = 5nm where I_{ON}/I_{OFF} ratio is more than 105and SS = 62 mV/dec according to the results in Figure 4.29.

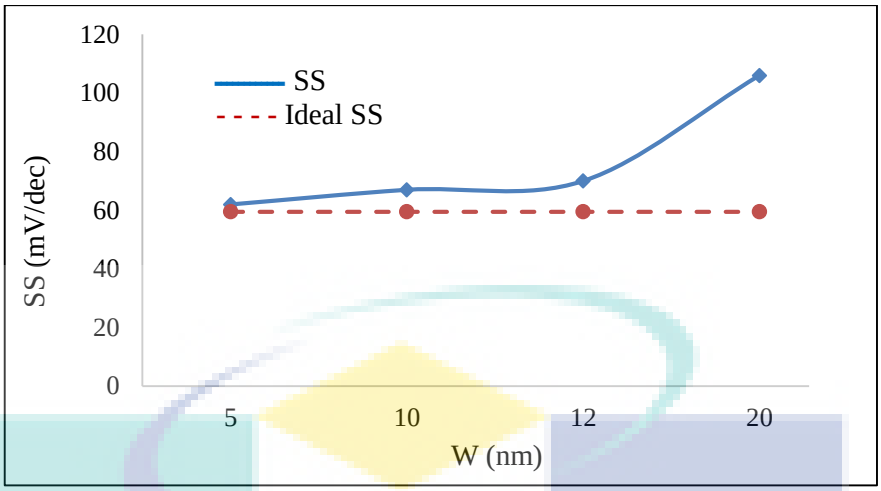

Figure 4.29 SS with a channel width of Ge-FinFET

The improvement in Ge-FinFET with shrinking channel width is also obvious in terms of the threshold voltage and DIBL as depicted in Figure 4.30. The V_T is inversely proportional to channel width, where V_T = 0.435 V at the minimum channel width of 5nm and V_T = 0.24 V at the maximum channel width of 20 nm. Meanwhile, the DIBL is proportional to channel width and it attains the minimum and best value of 4.9 mV/V when W = 20 nm and this lead to the exchange of high-integration electrical charge.

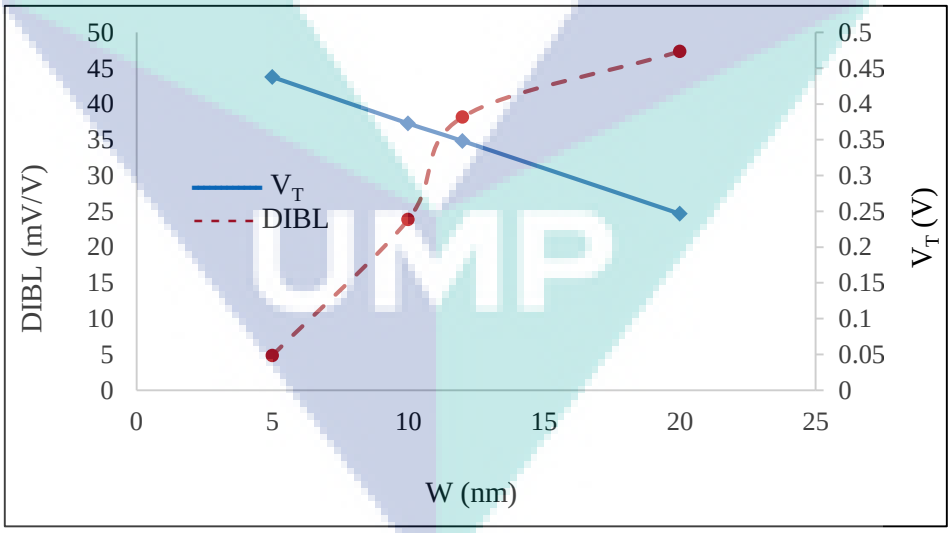

Figure 4.30 V_T and DIBL with a channel width of Ge-FinFET

4.4.3 Effect of Varying Channel Oxide Thickness

The behaviour of Ge-FinFET in terms of most electrical characteristics with scaling down channel oxide thickness is consistent with the previous scenario of

channel width variation. As the oxide thickness of channel decreased, characteristics were enhanced, even though the improvement is less comparing with the width-based scenario. For the simulation scenario carried out in channel oxide thickness, T_{OX} has been changed (1.5, 2.5, 5 and 7 nm), while both channel length and width were kept constant at 40 and 10 nm respectively. Figure 4.31, describes the variation of I_{ON}/I_{OFF} ratio with the channel oxide thickness. The best I_{ON}/I_{OFF} ratio was greater than 104 and was obtained with V_{DD} = 5 V at minimum T_{OX} = 1.5 nm and then decreased to 10^2 at T_{OX} = 7 nm. Almost similar results were obtained for 0.5 V that represents the nearest voltage to OFF state voltage (0 V).

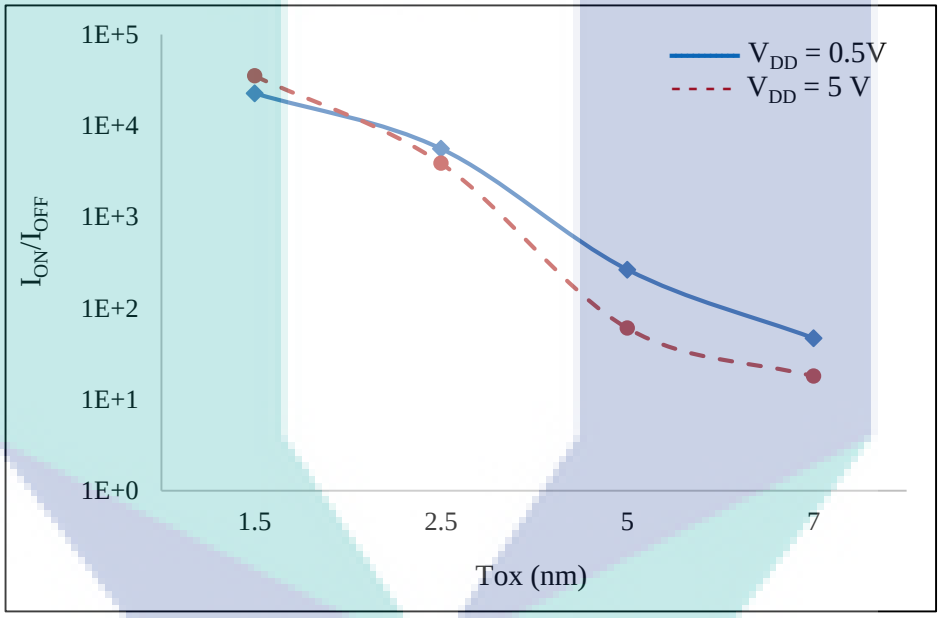

Figure 4.31 I_{ON}/I_{OFF} with an oxide thickness of Ge-FinFET

From the results shown in Figure 4.32, it was so obvious that for a channel oxide thickness, T_{OX} = 7 nm the Ge-FinFET shows better SS characteristics with the best SS value of 67 mV/dec compared to other T_{OX} values with a faster transistor. Conversely, the farthest value from ideal SS (59.5 mV/dec) occurred at T_{OX} = 7 nm where SS is 229 mV/dec with a slower transistor.

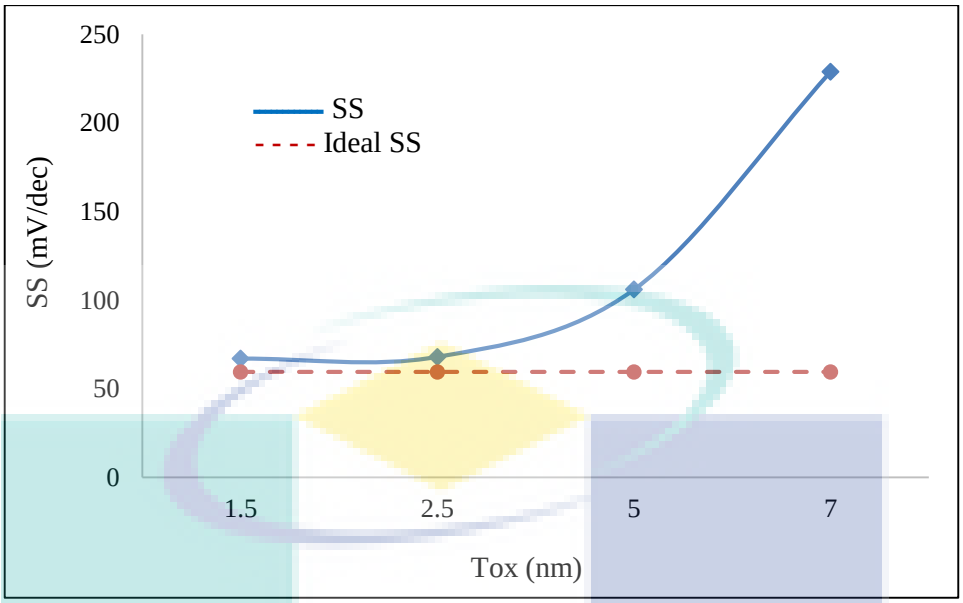

Figure 4.32 SS with an oxide thickness of Ge-FinFET

Furthermore, Figure 4.33 shows the gained improvement in terms of both V_T and DIBL characteristics of Ge-FinFET due to decreasing channel oxide thickness. While the voltage threshold increased linearly with decreasing T_{OX}, the DIBL was not consistent and its value fluctuating with different oxide thickness. The best and highest threshold voltage was V_T = 0.35 V at the smallest channel oxide thickness of 1.5 nm. Similarly, DIBL achieved the smallest value of 19 mV/V at the minimal T_{OX}. Where the best electrical conductivity occurs.

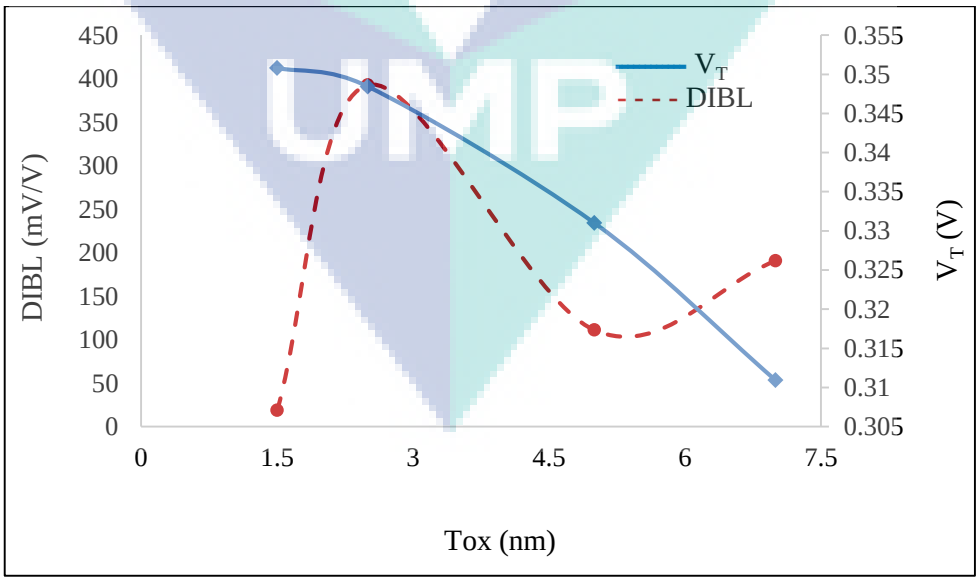

Figure 4.33 V_T -DIBL with channel oxide thickness of Ge-FinFET

4.4.4 Effect of Varying Scaling Factor of Channel Dimensions

According to the aforementioned scenarios, the best performance in terms of the considered electrical characteristics was achieved at channel length L = 40 nm, channel width, W = 5 nm, and channel oxide thickness, T_{OX} =1.5 nm. Thus, Ge-FinFET has not achieved a proper performance with a shrinking channel length where it attains better performance at the longest channel case. In order to scale down all channel dimensions at once, we have applied a scaling factor, K on all dimensions including, length, width, and thickness. Following we study the electrical characteristics based on the scaling factor, the reference value of K is defined as "1" with its highest channel dimensions. Then, all dimensions are scaling down to reach new physical limits for the channel of Ge-FinFET. All corresponding dimensions to the defend scaling factors are shown in Table 4.8.

Table 4.8 Channel dimensions based on scaling factor K

K	L (nm)	W (nm)	T_{OX} (nm)
1.00	40	20	6
0.5	20	10	3
0.25	10	5	1.5
0.125	5	2.5	0.625

Figure 4.34 shows the relation between the I_{ON}/I_{OFF} ratio with the scaling factor K from 0.125 to 1.00 Obviously, there is an improvement in I_{ON} /I_{OFF} characteristics with downscaling all channel dimensions together. The best value of I_{ON} /I_{OFF} ratio is higher than 10^4 which is achieved at scaling factor of K = 0.125 for both V_{DD} = 0.5 V and for V_{DD} = 0.5 V. The worst I_{ON}/I_{OFF} ratios, less than10^2 occurred at the reference value of scaling factor for both V_{DD} voltages.

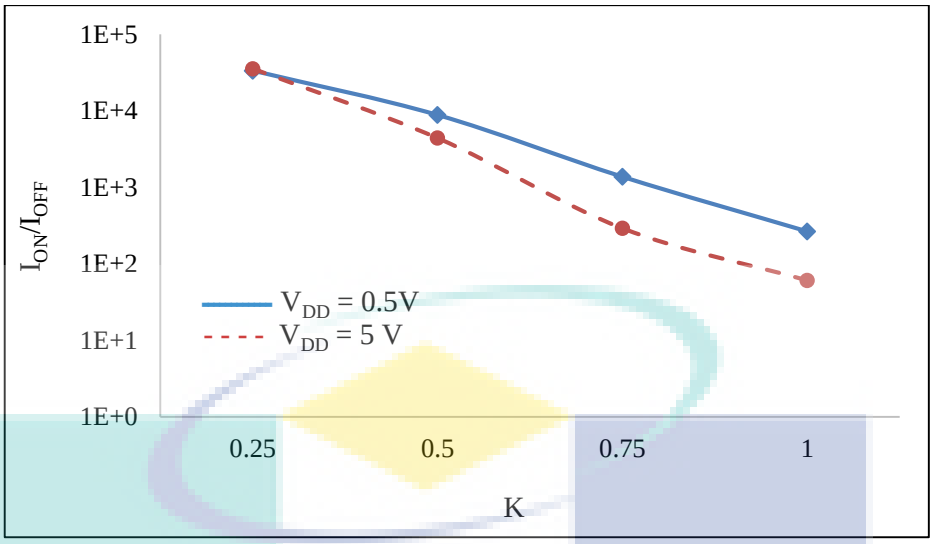

Figure 4.34 I_{ON}/I_{OFF} with scaling factor of Ge-FinFET

Figure 4.35 shows the worst SS characteristic value (100 mV/dec) that is obtained at K = 1.00 in contrast, the nearest value to the ideal SS is 68.9 mV/dec was acquired at K = 0.125. It can be noticed that, with increasing K, the SS value is increased significantly.

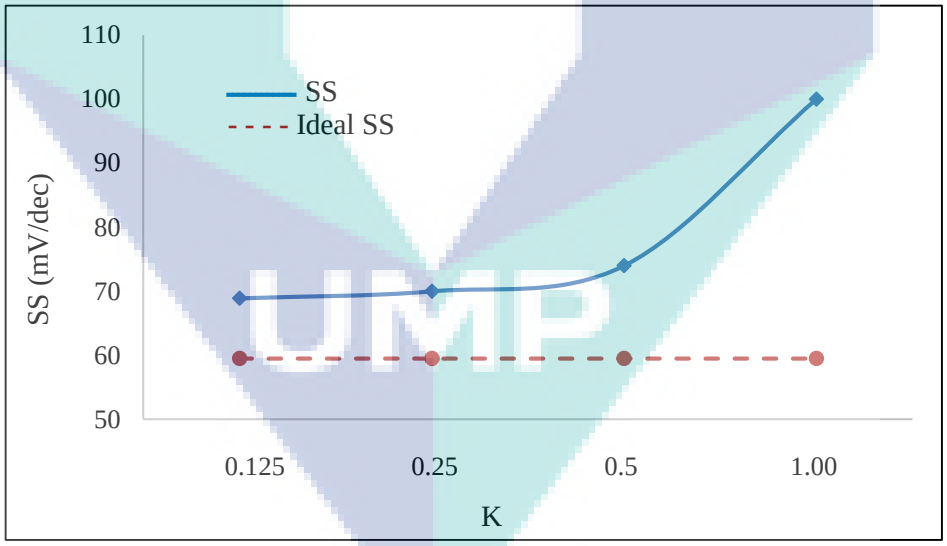

Figure 4.35 SS with scaling factor of Ge-FinFET

Likewise, the impact of changing Scaling Factor (K) on V_T and DIBL is illustrated in Fig 4.36. Where the highest value of V_T = 0.64 V is obtained at K = 0.125, compared to the lowest value, V_T = 0.33 V at the at K = 1.00 On the other hand, the DIBL value ranges from 356 mV/V to 111 mV/V between the minimum and the

maximum value of K respectively, with inconsistent behaviour in between. The summary of findings for the Ge-FinFET are presented in Table 4.9.

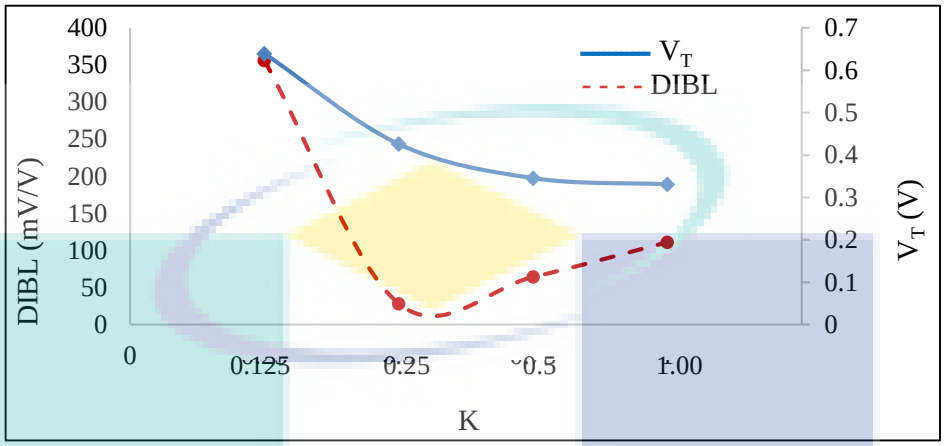

Figure 4.36 V_T and DIBL with scaling factor of Ge-FinFET

Table 4.9 Summary of Ge-FinFET main findings

Scenario	Characteristics	Value
Scenario 1	I_{ON}/I_{OFF}	2.29×10^5
	SS(mV/dec)	65
L	Best L(nm)	40
Scenario 2	I_{ON}/I_{OFF}	2.29×10^5
	SS(mV/dec)	62
W	Best W(nm)	5
Scenario 3	I_{ON}/I_{OFF}	3.53×10^4
	SS(mV/dec)	67
T_{OX}	Best T_{OX} (nm)	1.5
Scenario 4	I_{ON}/I_{OFF}	3.56×10^4
	SS(mV/dec)	68.9
K	Best K	0.125

4.5 The InAs-FinFET Scenarios

This simulation tool was utilized to investigate the characteristics of the InAs-FinFET transistor based on various channel's dimensions. The output characteristic curves of the transistor under different conditions and with different parameters are

considered. The effects of variable channel dimensions, namely; channel length, width and oxide thickness in addition to scaling factor of the InAs-FinFET transistor, are determined based on the I–V characteristics that derived from the simulation. In this paper, the I_d–V_g characteristics of InAs-FinFET at the temperature of 300 K are simulated and evaluated with the simulation parameters that listed in Table 4.10.

Table 4.10 Simulation parameters

Parameters	**Value**
Channel length (L)	(10, 15, 25, 35 and 45) nm
Channel width (W)	(5, 10, 12, 15 and 20) nm
Oxide thickness (T_{OX})	(1.5, 2.5, 5 and 7) nm
Scaling factor (K)	(0.125, 0.25, 0.5 and 1.00)
Channel concentration P-type	10^{16} cm^{-3}
Channel concentration N-type	10^{19} cm^{-3}

Four simulation experiments were designed to evaluate the performance of InAs-FinFET in terms of the considered metrics. In the first scenario, channel length was changed, whereas other dimensions (W and T_{OX}) were kept constant. In the second scenario, the impact of changing channel width was investigated while both the length and thickness of the channel were kept constant. In the third scenario, oxide thickness was changed and length and width were fixed. Finally, the impact of changing scaling factor was studied by changing the three dimensions all at once based on a changeable scaling factor. This section investigates the effect of channel dimensions on the I–V characteristics of InAs-FinFET. A simulation tool (MuGFET) was used to investigate the effect of channel dimensions on its electrical characteristics.

4.5.1 Effect of Varying Channel Length

The scaling down of channel length L and its effect on the characteristics of InAs FinFET have been studied. The simulation of transfer characteristics (drain current I_d –gate voltage V_g) have been down with different channel lengths (L) channel width (W) and oxide thicknesses (T_{OX}). The limitation parameters were used to find the optimal channel dimensions were I_{ON}/I_{OFF} ratio (where I_{OFF} is an I_d at OFF state at V_g =

0 V and I_{ON} is an I_d at ON state at V_g = 1 V) and sub-threshold swing (SS) and the threshold voltage (V_T) and drain-induced barrier lowering (DIBL).

Figure 4.37 illustrates the relation between I_{ON}/I_{OFF} ratio with the channel length of 10 15 25 35 and 45 nm and at W = 5nm and T_{OX} = 2.5 nm the I_{ON} /I_{OFF} ratio increased to 10^6 for increasing L from 10 to 40 nm for V_{DD} = 5 V. For V_{DD}= 5 V increased value for I_{ON}/I_{OFF} ratio were more than10^4 at L =40 nm. It is noticed that for L range from 10 to 30nm the highest I_{ON}/I_{OFF} ratio happen for V_{DD}= 5 V while for 30 to 45 nm, L range the highest I_{ON}/I_{OFF} ratio happen for V_{DD}= 5 V where the lowest leakage current I_{OFF}.

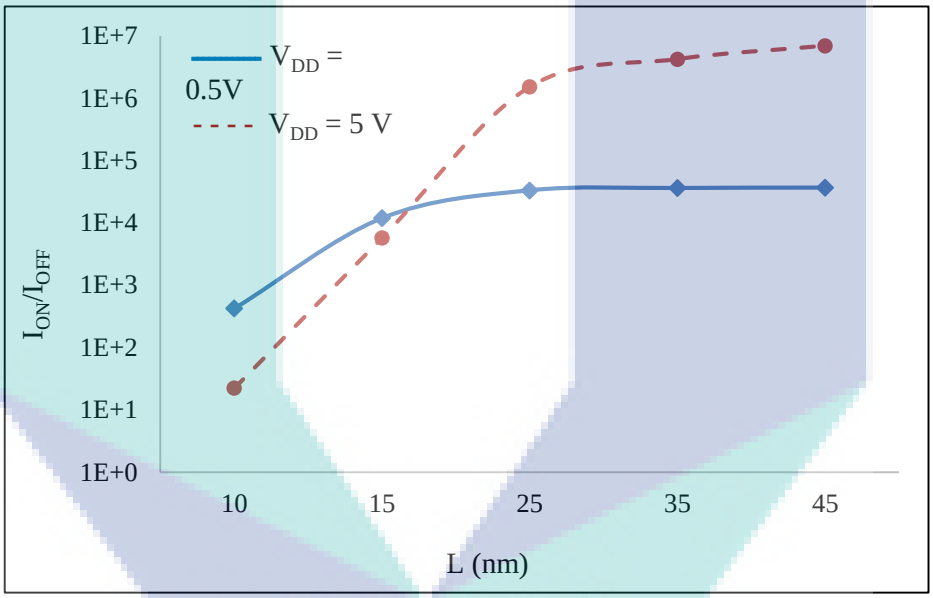

Figure 4.37 I_{ON}/I_{OFF} with a channel length of InAs-FinFET

Figure 4.38 presents the relation between channel length with (SS) of the IaAs-FinFET in this results the channel length was 10, 15, 25, 35 and 45 nm the W = 5 nm and T_{OX} = 2.5 nm. This figure illustrated that the value SS started with 124 mV/dec at L = 10 nm and at L = 15 nm this value to becomes the nearest value to the ideal SS (101 mV/dec) were happen. The furthest value from the ideal SS (59.5 mV/dec) where the higher channel length at L = 45nm SS = 169.9 mV/dec where the transistor is slower.

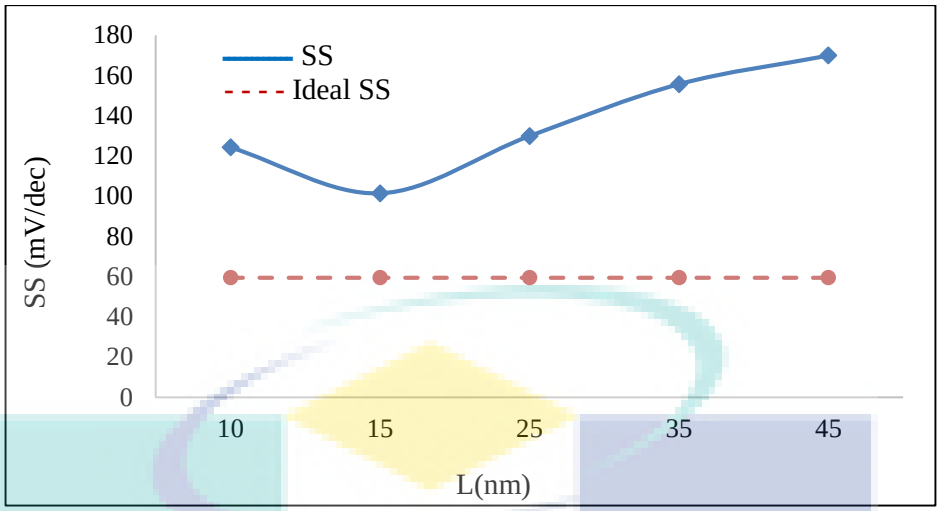

Figure 4.38 SS with a channel length of InAs-FinFET

Figure 4.39 depicts the variation of both V_T and DIBL with different channel length value of V_T is proportional increases with channel length and reaches to 1.2 V at the longest channel. On the other hand, DIBL increases as channel length increased from 360 mV/V at L = 10 until it reached 517 mV/V at L = 45 nm leading to poor electrical conductivity due to the high DIBL value.

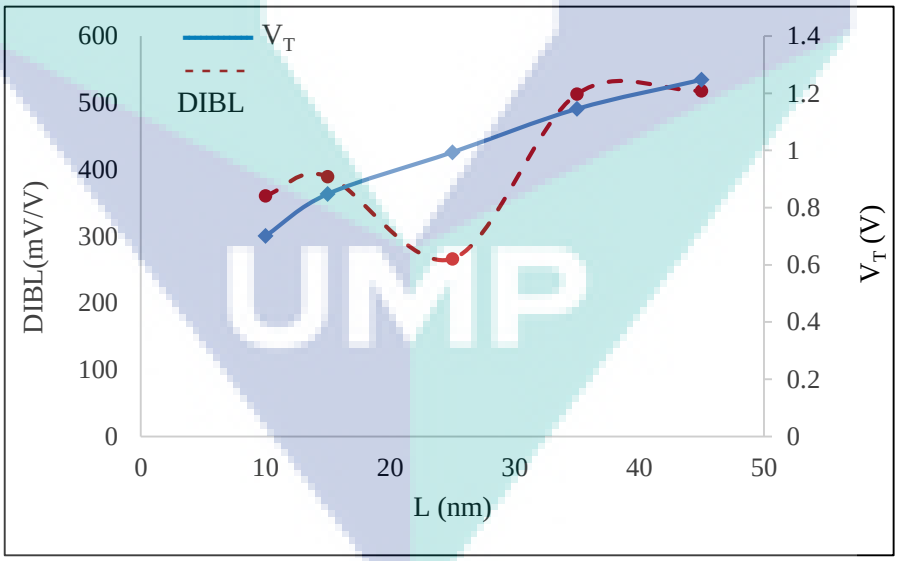

Figure 4.39 V_T and DIBL with a channel length of InAs-FinFET

According to the obtained characteristics in this scenario, the best performance in terms of both the I_{ON}/I_{OFF} ratio and SS value can be achieved in the case with 25 nm channel length. However, in the case with L = 45 nm, although I_{ON}/I_{OFF} ratio is the best, the SS value is too far from idle SS.

4.5.2 Effect of Varying Channel Width

The scaling down of channel width W and its effect on the characteristics of InAs-FinFET have been studied in this scenario. The value of W was changed (5, 10, 15 and 20 nm) while L and T_{OX} were set to 40 nm and = 2.5 nm respectively. Figures 4.40, 4.41 and 4.42 show the electrical characteristics, I_{ON}/I_{OFF} ratio, SS, V_T, and DIBL correspondingly. The I_{ON}/I_{OFF} ratio for both voltages (V_{DD} = 5 V and V_{DD} = 5 V) in terms of the varying width of the channel are illustrated in Figure 4.40.

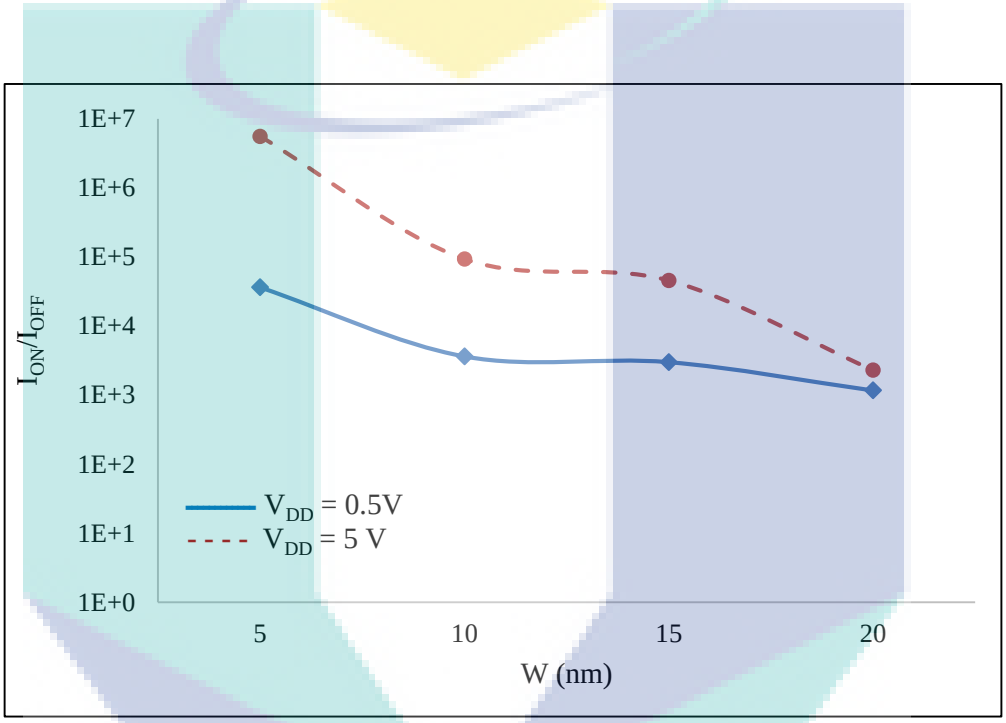

Figure 4.40 I_{ON}/I_{OFF} with a channel width of InAs-FinFET

Unlike the channel length scenario, the ratio is inversely proportional with channel width. Ratios for both voltages drop down to approximately 10^3 when W increases to 20 nm. In contrast, the highest I_{ON}/I_{OFF} ratio (more than 10^6) was achieved for V_{DD} = 5 V with the smallest channel width. Fig. 4.41 depicts the variation of SS value with variable channel width. The closest SS to ideal value was achieved at W = 5 nm which is 124 mV/dec, then it was increased to156 mV/dec at W = 20 nm.

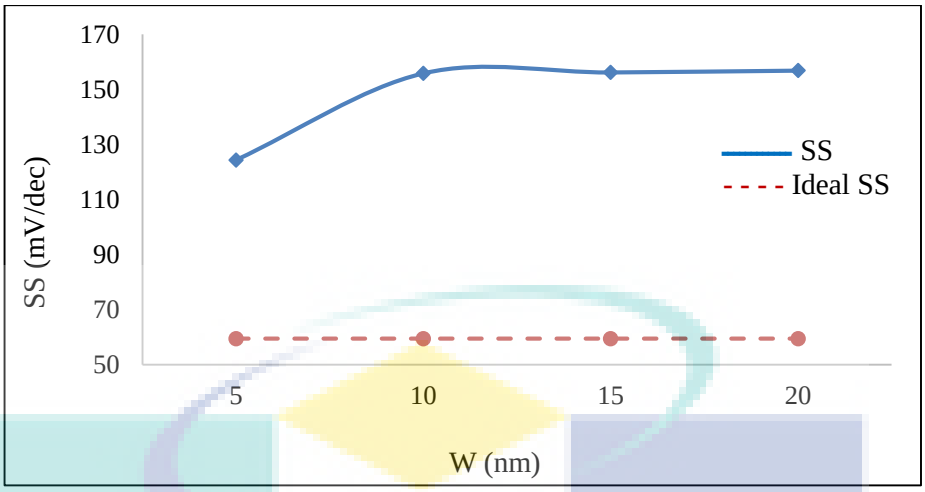

Figure 4.41 SS with a channel width of InAs-FinFET

Furthermore, the impacts of varying channel width on V_T and DIBL are illustrated in Figure 4.42. The voltage threshold is almost constant regardless channel width except in the first case with W = 5 nm, where V_T scores the highest value of 1.2 V. Finally, the DIBL decreased as channel width increased. InAs-FinFET achieved worst DIBL = 517 at W = 5 nm then DIBL characteristics improved and achieved the best value at W = 10 nm.

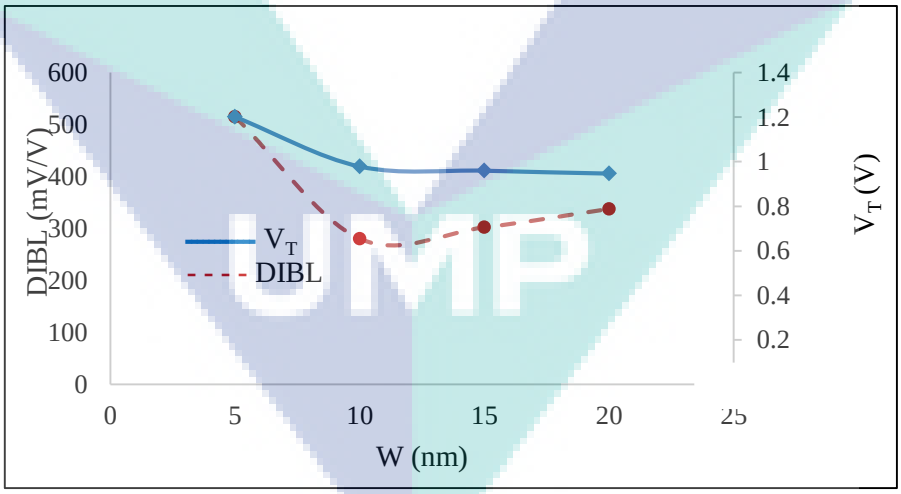

Figure 4.42 V_T and DIBL with a channel width of InAs-FinFET

4.5.3 Effect of Varying Channel Oxide Thickness

Figures 4.43, 4.44, and 4.45 show the channel oxide thickness variation in relation to the electrical characteristics of InAs-FinFET. For the simulation scenario carried out in Figure 4.43 channel oxide thickness, T_{OX} has been varied (1.5, 2.5, 5 and

7 nm), the channel length, L is kept constant at 40 nm, while as the channel width, W is kept fixed at 5 nm. Fig. 4.43 illustrates the relation between the I_{ON}/I_{OFF} ratio with the channel oxide thickness which is consistent with previous channel width scenario. The maximum I_{ON}/I_{OFF} ratio (more than 10^6) with V_{DD} = 5 V was obtained at minimum T_{OX} = 1.5 nm and then decreased to 10^3 at T_{OX} = 7 nm.

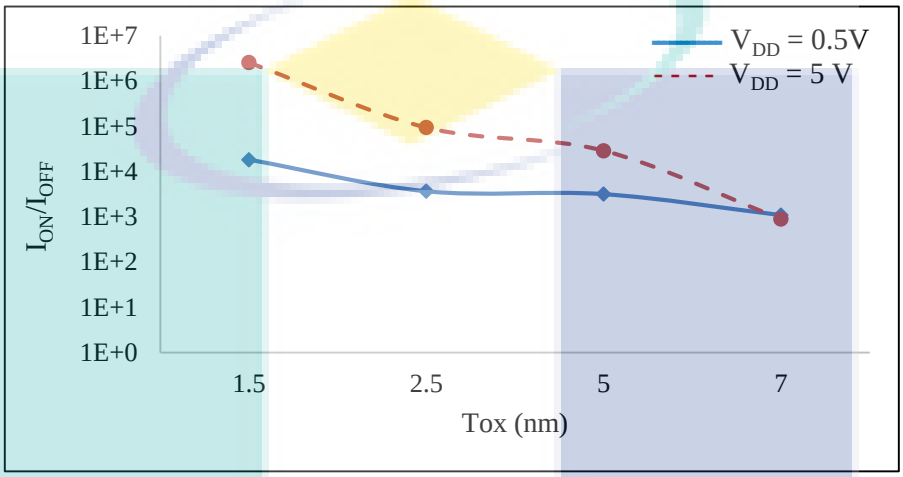

Figure 4.43 I_{ON}/I_{OFF} with an oxide thickness of InAs-FinFET

From the results shown in Figure 4.44, it is obvious that for a channel oxide thickness, T_{OX} = 7 nm the InAs-FinFET has shown better SS characteristics with the best SS value of 140 mV/dec compared to other T_{OX} values. Conversely, the farthest value from ideal SS occurred at T_{OX} = 5 nm where SS is 216 mV/dec.

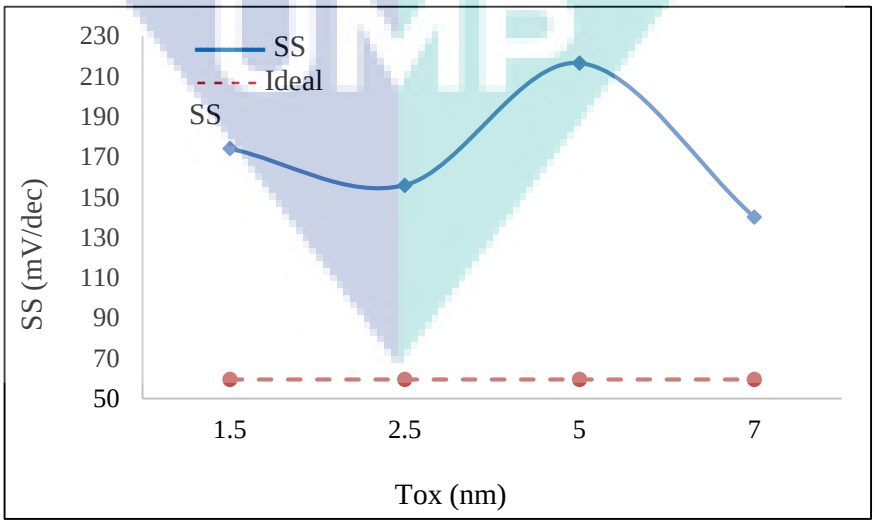

Figure 4.44 SS with an oxide thickness of InAs-FinFET

On the other hands, in Figure 4 45 displays channel oxide thickness versus both V_T and DIBL characteristics of InAs-FinFET. Both characteristics behave inconsistent manner with decreasing channel thickness, they decrease as T_{OX} decreased. The best V_T = 15.8 V at the highest T_{OX} value, whereas the best value of DIBL is 165 mV/V at oxide thickness of channel = 1.5 nm.

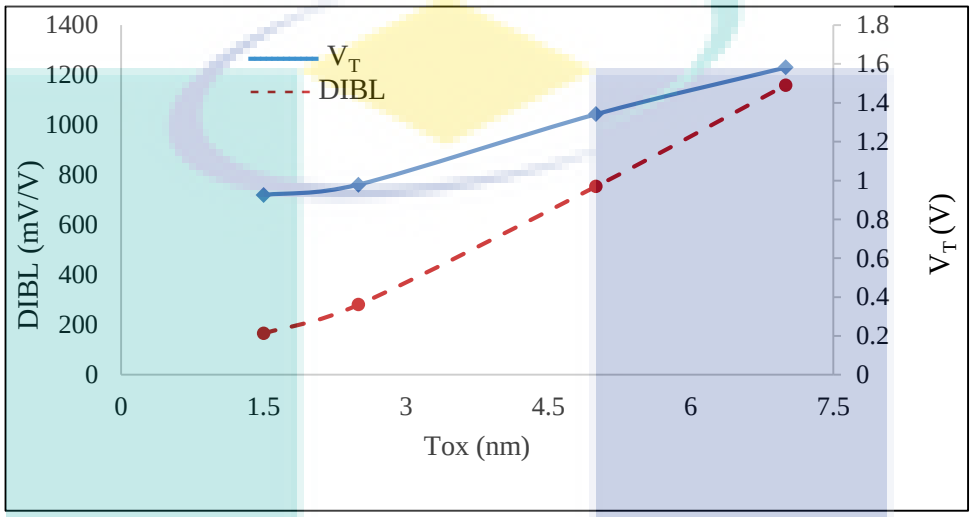

Figure 4.45 V_T and DIBL with channel oxide thickness of InAs-FinFET

4.5.4 Effect of Varying Scaling Factor of Channel Dimensions

The scaling down of all channel dimensions at once can be achieved by applying scaling factor, K. All channel dimensions, length, width, and thickness will be scaling-down together by a factor (K). In order to study the electrical characteristics based on the scaling factor, the reference value of K is defined as "1" with its channel dimensions. All corresponding dimensions to the defend scaling factors are shown in Table 4.11.

Table 4.11 Channel dimensions based on scaling factor K

K	L (nm)	W (nm)	T_{ox} (nm)
1.00	40	20	6
0.5	20	10	3
0.25	10	5	1.5
0.125	5	2.5	0.75

Figure 4.46 shows the relation between the I_{ON}/I_{OFF} ratio with the scaling factor K from 0.125 to 1.00 The maximum value of I_{ON}/I_{OFF} ratio is higher than 10^4 which was attained at scaling factor K = 0.125 for both V_{DD} = 5 V and for V_{DD} = 5 V. The worst I_{ON}/I_{OFF} ratios, less than 10^2 occurred at the reference value of K = 1.00 for both V_{DD} values.

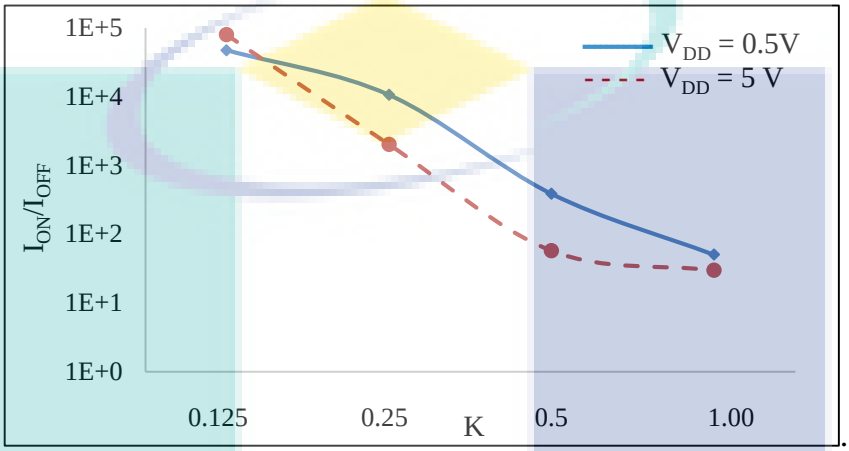

Figure 4.46 I_{ON}/I_{OFF} with scaling factor of InAs-FinFET

Figure 4.47 shows the worst SS value (194 mV/dec) that obtained at K = 1.00 in contrast, the nearest value to the ideal SS (94 mV/dec) is obtained at K = 0.125. It can be noticed that, with increasing K, the SS value is increased significantly.

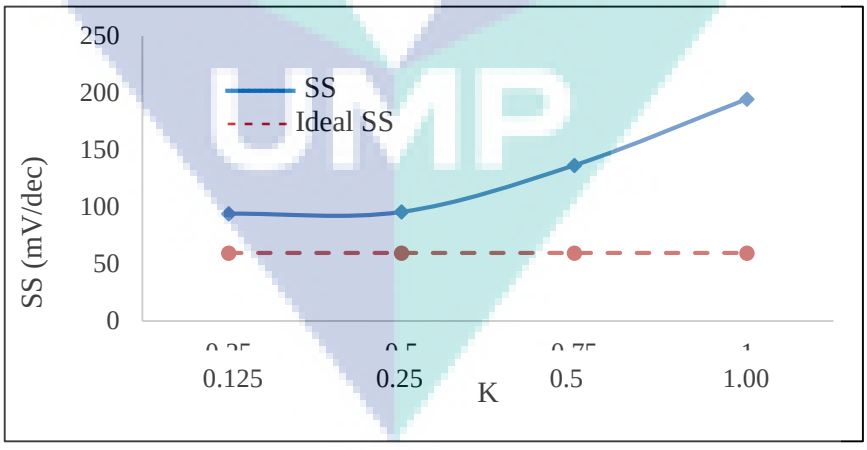

Figure 4.47 SS with scaling factor of InAs-FinFET

The impact of changing Scaling Factor (K) on V_T and DIBL is illustrated in Figure 4.48. Where the highest value of V_T = 1.28 V is obtained at K = 1.00 compared to the lowest value, V_T = 0.7 V at K = 0.125 conversely, the DIBL value ranges from

376 mV/V at K = 0.125 to 934 mV/V at K = 1.00 and the best value is attained at K = 0.125 which is 195 mV/V. Table 4.12 presents the summary of main findings for InAs-FinFET.

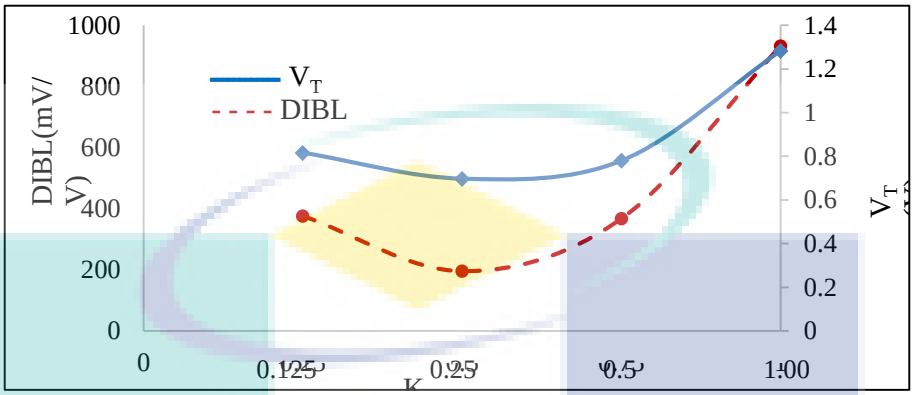

Figure 4.48 V_T and DIBL with scaling factor of InAs-FinFET

Table 4.12 Channel summary of main findings for InAs-FinFET

Scenario	Characteristics	Value
Scenario 1	ION/IOFF	6.97×106
	SS(mV/dec)	101
L	Best L(nm)	25
Scenario 2	ION/IOFF	5.58×107
	SS(mV/dec)	124
W	Best W(nm)	5
Scenario 3	ION/IOFF	2.54×106
	SS(mV/dec)	155
TOX	Best TOX (nm)	1.5-2.5
Scenario 4	ION/IOFF	7.94×104
	SS(mV/dec)	94
K	Best K	0.125

4.6 Comparison of FinFETs Constituent Semiconductor Materials

This section presents an overall comparison between different FinFETs based on the type of semiconductor materials and according to the obtained results from the fourth scenario of each type as mentioned earlier. Based on the scaling factor, K, the electrical characteristics (I_{ON}/I_{OFF}, SS, $V_{T,}$ and DIBL) of FinFET transistors (Si, Ge,

GaAs, and InAs) are compared. Due to their importance as key metrics of transistor performance, I_{ON}/I_{OFF} and SS were given the privilege in our evaluation to identify the best performance based on semiconductor materials. As shown in Figure 4.49 and Figure 4.50, Si-FinFET achieved the highest I_{ON}/I_{OFF} ratio in all cases compared to other materials regardless of scaling factor value. Although, Si-FinFET obtained the highest I_{ON}/I_{OFF} at K = 0.5; however, its SS value at K = 0.5 is far from ideal value. With the increment of K-value, the SS increased significantly and lead to decrease speed in the transistor. Therefore, the best performance of Si-FinFET by considering both metrics, I_{ON}/I_{OFF} was achieved at K = 0.125, just similar to other types. The Si-FinFET maintained more than 10^8 I_{ON}/I_{OFF} ratio and 62.2 mV/dec SS value comparing to the nearest competitor which is GaAs-FinFET that attained more than 10^6 I_{ON}/I_{OFF} ratio and 65.7 mV/dec at the same scaling factor of 0.125. It is obvious that GaAs-FinFET did not perform well in terms of the considered metrics at other scaling factor values. It is obviously that there is an improvement in I_{ON} /I_{OFF} characteristics with downscaling all channel dimensions together. The results for both Ge-FinFET and InAs are consistent where the best value of I_{ON} /I_{OFF} ratio is higher than 10^4 which is achieved at scaling factor of K = 0.125 and its worst I_{ON}/I_{OFF} ratios is less than10^2 occurred at the reference value of scaling factor for both V_{DD} voltages. In terms of SS value, both InAs- and GaAs-FinFETs recoded the worst results in all scenarios regardless of channel dimensions due to their highest permittivity values comparing to other semiconductors. They achieved 195 and 189 mV/dec respectively at K = 1. Overall, the subthreshold swing is proportionally increasing with K nevertheless the semiconductor material.

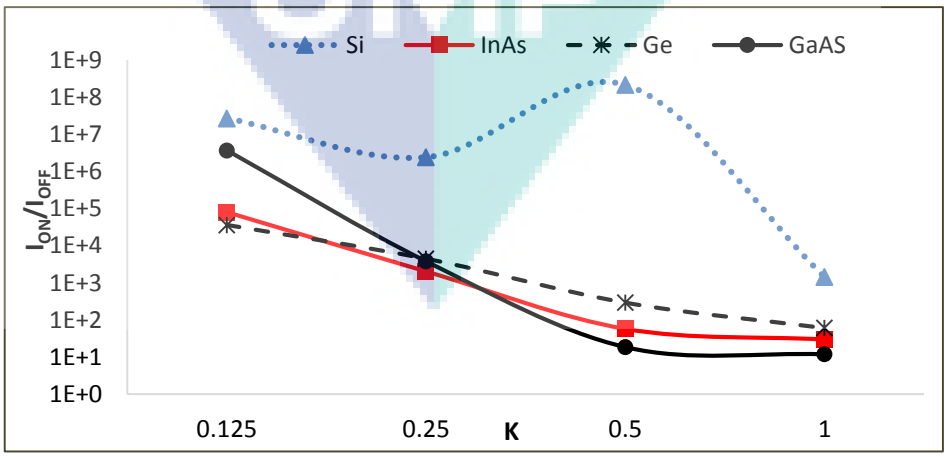

Figure 4.49 I_{ON}/I_{OFF} vs. K for different semiconductors of FinFET

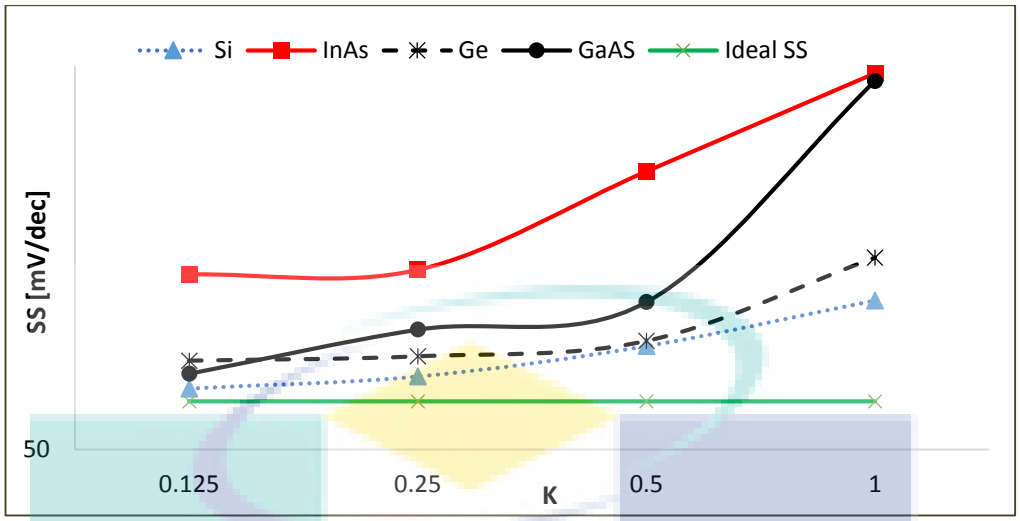

Figure 4.50 SS vs. K for different semiconductors of FinFET

The impact of changing scaling factor (K) on threshold voltage (V_T) and drain-induced barrier lowering (DIBL) is illustrated in Figure 4.51 and Figure 4.52 respectively. Oxide thickness is a key player in changing the value of threshold voltage, V_T while other dimensions have marginally effects on this metric. Therefore, we can notice that the variation of V_T with changing scaling factor is limited except for InAs-FinFET which attained the highest V_T in all cases. It achieved the highest value of V_T = 1.28 V at K = 1, compared to the lowest value, V_T = 0.7 V at K = 0.25. It was followed by Si-FinFET which outperformed others in all cases except at K = 0.125 where V_T = 0.49 V was the lowest among all semiconductors. Similarly, InAs-FinFET achieved the highest DIBL results in all cases comparing with other semiconductor materials. For Si-FinFET, the DIBL value ranges from 45 to 50 mV/V until it reached 49.99 mV/V at K = 0.125. This indicated that the charge exchange is almost stable at the different dimensions of the silicon channel. For GaAs-FinFET, the DIBL value decreases from 298 mV/V at K = 1 to 48 mv/v at K = 0.125 where it becomes similar to Si-FinFET at these channel dimensions. As we can notice, the obtained results in terms of V_T and DIBL cannot provide a good indication to compare the considered semiconductor material because they are based on multiple parameters related to nature of these Fin-FETs rather than channel dimensions. Therefore, our conclusion for these simulation results was drawn up mainly based on the first two electrical metrics, I_{ON}/I_{OFF} and SS value.

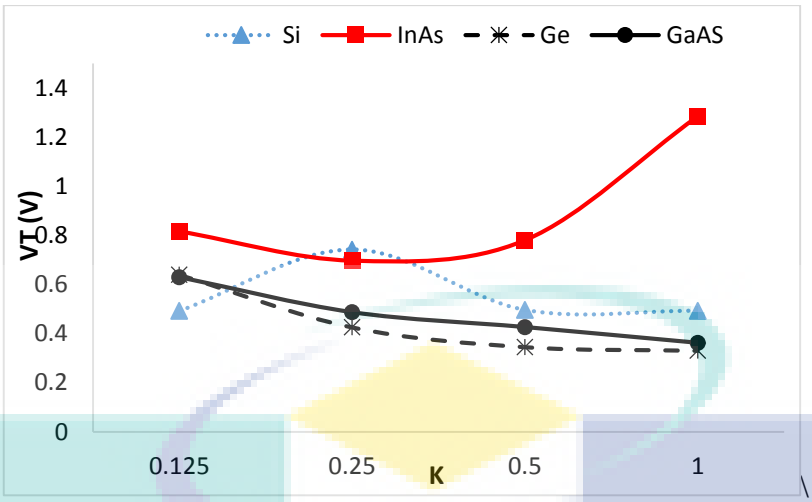

Figure 4.51 VT vs. K at different semiconductors of FinFET

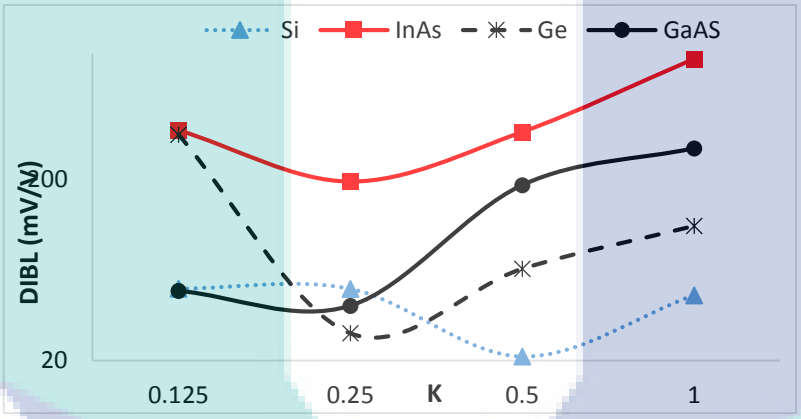

Figure 4.52 DIBL vs. K for different semiconductors of FinFET

Overall, the I_{ON}/I_{OFF} ratio and SS values of all FinFETs improved with simultaneous scaling down of their channel dimensions. Accordingly, based on the considered semiconductor materials of FinFETs, Si-FinFET can be considered as the best choice for applications that required very low leakage current and high speed. The GaAs-FinFET comes next with acceptable I_{ON}/I_{OFF} and SS value. For applications that not required a high-speed processing, InAs-FinFET will be a good choice since it has smaller leakage current comparing to Ge-FinFET with higher SS value. The main results of this comparison along with the main finding of all simulation scenarios are summarized in and Table 4.13.

Table 4.13 Overall comparison of semiconductors channel type FinFET

Semiconductor	**Si**	**GaAs**	**Ge**	**InAs**
I_{ON}/I_{OFF}	2.12×10^{8}	1.08×10^{8}	2.29×10^{5}	6.97×10^{6}
SS(mV/dec)	60	59.65	65	101
Best L(nm)	40	30-40	40	25
I_{ON}/I_{OFF}	2.12×10^{8}	1.08×10^{8}	2.29×10^{5}	5.58×10^{7}
SS(mV/dec)	60	60	62	124
Best W(nm)	5	5	5	5
I_{ON}/I_{OFF}	2.15×10^{7}	2.11×1^{8}	3.53×10^{4}	2.54×10^{6}
SS(mV/dec)	62	59.7	67	155
Best T_{OX} (nm)	1.5	1.5-2.5	1.5	1.5-2.5
I_{ON}/I_{OFF}	2.15×10^{7}	3.65×10^{6}	3.56×10^{4}	7.94×10^{4}
SS(mV/dec)	62.2	65.7	68.9	94
Best K	0.125	0.125	0.125	0.125
Potential applications	In nanoparticles atomic as Nano medicine in Cancer Therapy laser	As an ultra-sensitive sensor in Nano electronics circuits	For applications of electronics and electricity from solar energy	In infrared accurate detectors

* The values with bold colour represents the novelty of research

4.7 Summary

In this chapter, the obtained simulation results were introduced and classified based on simulation scenarios. The impact of changing channel dementias (L, W, T_{OX}) individually on the electrical characteristics (I_{ON}/I_{OFF} ratio SS, V_T, and DIBL) for different types of FinFETs (Ge-FinFET, InAs-FinFET, and GaAs-FinFET) were analysed and compared. The effects of varying all dimensions of channel together based on a predefined scaling factor, K also evaluated. An overall comparison of the simulation results for the considered scenarios also presented.

CHAPTER 5

CONCLUSION

5.1 Introduction

This chapter concludes the presentation of the work by resuming the achieved results, and directions for further studies are indicated. This thesis investigated and analysed the effects of channel dimensions (L, W, and T_{ox}) on the electric characteristics of (Si, Ge, GaAs, and InAs)-FinFET using MuGFET simulation tool. The results of the investigation study in the first three simulation scenarios showed that the best characteristics were obtained when L was increased and W and T_{ox} were decreased. Accordingly, in the last scenario, a new nanoscale dimensions' limits of the channel for different FinFETs semiconductor materials were achieved by scaling-down the three dimensions of the channel simultaneously.

5.2 Conclusion

The objectives of this study were achieved successfully. In the first part, the impact of changing each channel dimension on the electrical characteristics of each semiconductor material was well investigated and evaluated. Depending on the highest value I_{ON}/I_{OFF} ratio and the nearest SS to the ideal SS, the best dimensions were selected. It proved that the performance of FinFETs improved with increasing channel length, decreasing both width and oxide thickness. This was due to the short channel effects on the I_{ON}/I_{OFF} and subthreshold swing. Si-Fin-FET outperformed other semiconductors in the considered single-dimension-based scenarios.

In order to achieve new downscaling limits, a scaling factor, K was proposed to shrinking down all channel dimensions at the same time. Three steps were considered to decreased channel length along with width and oxide thickness to 25% of their default

values. The obtained results introduced new limits with good performance in terms of the investigated characteristics. The default values at K = 1 were set to L = 40 nm, W = 20 nm, and T_{ox} = 6 nm. These dimensions were downscaled to L = 5 nm, W = 2.5 nm, and T_{ox} = 0.625 nm when the proposed K was set to 0.125.

Based on the new scaling factor, the new Nano-dimensional channel was designed for four types of semiconductor material-based FinFETs (Si, Ge, GaAs, and InAs). The performance of different FinFETs was evaluated and compared. The highest I_{ON}/I_{OFF} ratio (more than 10^8) and the nearest SS to the ideal value (62.2 mV/dec) were obtained with Si-FinFET with the new limits of channel dimensions. The GaAs-FinFET came second with I_{ON}/I_{OFF} (more than 10^6) and SS (65.7 mV/dec). InAs-FinFET had the worst performance in terms of SS (94 mV/dec), whereas Ge-FinFET attained the lowest I_{ON} /I_{OFF} compared to other types.

5.3 Significance of the Study

The significance of the study in this thesis and its research contributions can be summarized as follows:

- A new simulation-based model for electrical characterization of FinFETs transistors for highest I_{ON} /I_{OFF} ratio and closest sub-threshold swing to the ideal value.
- A new scaling factor, K to shrinking channel dimensions to new nano-scale limits with maintaining an acceptable performance of FinFETs with various constituent semiconductor materials, thus reducing short channel effects.
- The obtained simulation results and outcome of this study will play a role in investigating the field of nano-electronics devices and can accelerate the development of FinFETs applications in nanotechnology through introducing new nanoscale limits for different semiconductor FinFETs.

5.4 Recommendations for Future Work

This thesis focuses only on the effects of scaling down channel dimensions of the FinFET transistor on its electrical characteristics. Four semiconductors materials-based FinFETs were considered. However, there is still much work to be addressed in

the aspect of FinFETs as an inheritor to nanoscale and planner devices. The following suggested recommendations show how this work can be expanded in various research directions.

- Performing a comparative study between FinFET and SiNWT as suggested successors to MOSFET at the achieved Nano-dimension limits;
- Investigating temperature characteristics of various semiconductor material–based FinFETs with different insulating materials;
- Application of the suggested model with the optimal channel dimensions on FinFET inverters;
- Conducting experimental researches to investigate the ability to achieve such Nano-scale of channel dimensions in real transistors and compare the performance criteria of different FinFETs in both simulation and experimental studies.

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