INTERCONNECTION AND DAMPING ASSIGNMENT PASSIVITY BASED CONTROLLER FOR MULTILEVEL INVERTER

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requirements for the award of the degree of
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DECLARATION

I declare that this thesis entitled "*Interconnection and Damping Assignment Passivity-Based Controller for Multilevel Inverter*" is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in the candidature of any other degree.

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To my lovely mother, who gave me endless love, trust, constant encouragement over the years, and for her prayers.

To my husband, kids, my mother in law and siblings, for their patience, support, love, and for enduring the ups and downs during the completion of this thesis.

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ABSTRACT

This thesis proposes an Interconnection and Damping Assignment Passivity-Based Controller (IDA-PBC) to control a 5-level Cascaded H-Bridge Multilevel Inverter (CHMI). The proposed IDA-PBC uses the Port-Controlled Hamiltonian (PCH) theory to modify the CHMI system energy by adding damping, thereby modifying dissipation structures related to dynamics and stability. The objective is to maintain output voltage regulation, resulting in fast response and low Total Harmonic Distortion (THD) values. Although the proposed IDA-PBC control algorithm showed outstanding performance during transient and nonlinear load condition, further improvements are required during no-load condition. To address this, improvements in the form of modification to the proposed IDA-PBC algorithm was made by adding a single loop Proportional-Integral (PI) controller at the voltage side, which was aimed at regulating the voltage before it was fed back into the IDA-PBC. To verify the viability of the proposed IDA-PBC-PI controller for the CHMI, a simulation study was conducted using MATLAB/Simulink at a 20 kHz switching frequency and 1 μs sample time. The controller was tested at five load conditions, namely, steady state, no-load to full-load, load uncertainty, structural uncertainty and nonlinear load condition. The performance of the proposed controller showed regulated output voltage while maintaining THD values below 5% in all load conditions and a maximum of 220 μs response time during load uncertainty. The simulation results revealed the superiority of the proposed controller compared to the conventional double loop PI controller and the conventional IDA-PBC in terms of transient response, THD value, as well as regulation of the output voltage. The feasibility of the proposed IDA-PBC-PI controller was validated by developing its proof-of-concept hardware prototype. The simulation and experimental results obtained based on a 3 kHz switching frequency and 38 μs sample time were found to be consistent, which confirmed the capability of the proposed controller in controlling the 5-level CHMI output voltage.

ABSTRAK

Tesis ini mengusulkan Penetapan Terhadap Sambungan dan Redaman bagi Pengawal yang Berasaskan Konsep Pasif (IDA-PBC) untuk mengawal 5-aras Penyongsang Jejambat-H Pelbagai Aras (CHMI). IDA-PBC yang diusulkan menggunakan teori Tempat-Kawalan Hamiltonian (PCH) untuk mengubah suai tenaga CHMI dengan menambah redaman dan mengubah suai struktur pelesapan yang berkaitan dengan dinamik dan kestabilan. Objektif kawalan adalah untuk mengekalkan aturan voltan keluaran, serta menghasilkan masa tindak balas yang cepat dan Jumlah Gangguan Harmonik (THD) yang rendah. Walaupun algoritma kawalan IDA-PBC yang diusulkan menunjukkan prestasi cemerlang semasa kondisi peralihan dan beban yang tidak linear, penambahbaikan diperlukan semasa kondisi ketiadaan beban. Oleh itu, pengubahsuaian kepada algoritma IDA-PBC yang diusulkan telah dilaksanakan dengan menambah kawalan Berkadar-Kamiran (PI) pada bahagian voltan, untuk mengawal selia voltan sebelum ia disuap-balik ke dalam IDA-PBC. Bagi mengesahkan kebolehupayaan kawalan ini, kajian simulasi dijalankan menggunakan MATLAB/Simulink pada frekuensi pensuisan 20 kHz dan 1 μs sampel masa. Pengawal ini diuji di lima keadaan beban iaitu pada keadaan tetap, tiada beban kepada beban penuh, beban yang tidak menentu, ketidakpastian struktur dan beban yang tidak linear. Prestasi pengawal yang diusulkan menunjukkan voltan keluaran adalah teratur, disamping mengekalkan nilai THD bawah 5% dan masa tindak balas maksimum sehingga 220 μs. Keputusan simulasi mendedahkan keunggulan pengawal yang dicadangkan berbanding pengawal PI dua gegelung konvensional dan pengawal IDA-PBC konvensional dari segi masa tindakbalas, nilai THD serta aturan voltan keluaran. Semua pelaksanaan pengawal IDA-PBC-PI yang dicadangkan telah disahkan dengan membangunkan perkakasan prototaip berdasarkan konsep-pembuktian. Keputusan simulasi dan eksperimen yang diperolehi berdasarkan frekuensi pensuisan 3 kHz dan 38 μs sampel masa adalah didapati konsisten, yang mengesahkan keupayaan pengawal yang dicadangkan dalam mengawal voltan keluaran bagi 5-aras CHMI.

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LIST OF ABBREVIATIONS

A	-	Ampere
A_c	-	Amplitude of the carrier signal
A_m	-	Amplitude of the modulating signal
A/D	-	Analog/Digital
CHMI	-	Cascaded H-bridge Multilevel Inverter
CPU	-	Central Processing Unit
DC	-	Direct Current
DSP	-	Digital Signal Processor
EMI	-	Electromagnetic Interference
EV	-	Electric Vehicle
FFT	-	Fast Fourier Transform
FPGA	-	Field-Programmable Gate Array
I/O	-	Input/Output
IGBT	-	Insulated-Gate Bipolar Transistor
kHz	-	kilo Hertz
m	-	Number of staircase level
m_a	-	Amplitude modulation ratio
MLI	-	Multilevel Inverter
N	-	Harmonic order
PS-PWM	-	Phase-shift Pulse Width Modulation
PV	-	Photovoltaic
PWM	-	Pulse Width Modulation
r1, r2	-	Random number in a range of 0 to 1
n	-	Number of single phase full bridge inverters
THD	-	Total Harmonic Distortion
V	-	Volt
Var	-	Volt amperes reactive
VDC1	-	DC supply module 1
VDC2	-	DC supply module 2

Vc	-	Capacitor output voltage of CHMI
W	-	Watt
μs	-	micro seconds
θ	-	Angle

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