Received: 19 March 2020 | Revised: 29 December 2020 | Accepted: 21 January 2021

DOI: 10.1002/2050-7038.12820

RESEARCH ARTICLE

WILEY

A novel fault-detection methodology of proposed reduced switch MLI fed induction motor drive using discrete wavelet transforms

Arigela Satya Veerendra[1] | **Mohd Rusllim Mohamed**[1] | **Chavali Punya Sekhar**[2]

[1]College of Engineering, Universiti Malaysia Pahang, Kuantan, Malaysia

[2]Department of Electrical & Electronics Engineering, Acharya Nagarjuna University, Guntur, Andhra Pradesh, India

Correspondence
A. S. Veerendra and M. R. Mohamed, College of Engineering, Universiti Malaysia Pahang, Kuantan, Pahang 26300, Malaysia.
Email: veerendraump@gmail.com (A. S. V.) and rusllim@ump.edu.my (M. R. M.)

Funding information
Universiti Malaysia Pahang, Grant/Award Number: PES18003; National Key Research and Development Program of China, Grant/Award Number: 2017YFB0701700

Summary

Induction motors are typically promoted in industrial applications by adopting energy-efficient power-electronic drive technology. Multilevel inverters (MLI) have been widely recognized in recent days for high-power, medium-voltage-efficient drives. There has been vital interest in forming novel multilevel inverters with reduced switching elements. The newly proposed reduced-switch five-level inverter topology extends with fewer switches, low dv/dt stress, high efficiency, and so on, over the formal multilevel inverter topologies. The multilevel inverter's reputation is greatly affected due to several faults on switching elements and complex switching sequences. In this paper, a novel fault identification process is evaluated in both healthy and faulty conditions using discrete-wavelet transform analysis. The discrete wavelet transform utilizes the multi-resolution analysis with a feature extraction methodology acquired for fault identification over the classical methods. A novel fault identification scheme is implemented on reduced-switch five-level MLI topology using the Matlab/Simulink platform to increase the drive system's reliability. The effectiveness of simulation outcomes is illustrated with proper comparisons. The proposed topology's hardware model is implemented using a dSPACE DS1103 real-time digital controller and the results of the experiment are presented.

KEYWORDS

discrete wavelet transform, feature extraction methodology, feature decomposition rate, multilevel inverter, multi-resolution analysis, induction motor drive

1 | INTRODUCTION

Many industries require medium-voltage high power rated drives for process control by using advanced power-electronic conditioning systems in recent days. The multilevel inverter drive (MIMD) system becomes an optimum

List of Symbols and Abbreviations: AC, alternating current; CHB, cascaded H-bridge; DC, direct current; DFR, decomposition feature rate; DFT, discrete Fourier transform; DOC, diode-open circuit; DSC, diode-short circuit; DWT, discrete wavelet transform; FEM, feature extraction methodology; FFT, fast Fourier transform; GOC, gate-open circuit; GSC, gate-short circuit; IGBT, insulated gate bipolar transistor; IM, induction motor; IOC, IGBT-open circuit; ISC, IGBT-short circuit; LS-PWM, level-shifted modulation; MIMD, multilevel inverter drive; MLI, multilevel inverter; MRA, multi resolution analysis; OC, open circuit; PS-PWM, phase-shifted modulation; RSMLI, reduced switch multilevel inverter; SC, short circuit; VSI, voltage-source Inverters; Vdc, DC link voltage; N, ON state; F, OFF state; m_{in}, modulation index; A_r, sinusoidal reference; A_c, triangular carrier; V_o, output staircase voltage; V_{car1}, V_{car2}, dual carrier signal; D_{fr}, decomposition feature rate; n, number of levels; STD, standard deviation.

solution for adjustable speed drives (ASD) in many applications.[1,2] Multilevel inverter (MLI) itself influences the several advantages over the standard square-wave inverter, such as RMS quality voltage and current wave-shapes, low dv/dt stress, low electromagnetic interference compatibility, greater working efficiency, low harmonic profile, and so on. Additionally, a MLI furnishes high-power status and enables to control the speed of the induction motor drive.[3,4] The traditional MLI topologies are neutral-clamped type,[5] flying-capacitor type,[6] and cascaded H-bridge (CHB) type,[7,8] and play a significant role in many applications. Among these, the CHB type is the most recognized topology in ASDs, but it is restricted to low voltage levels. Many researchers contribute outstanding efforts to extend the novel MLI topologies with traditional topologies' anatomy by utilizing low switching elements.

Most industries rely on induction motors for process control and/or manufacturing by interfacing the inverter or multilevel inverters with the help of a front-end controlled rectifier. The safe and reliable operation of multilevel inverters in high-power industrial applications is essential to monitore the power electronic switches and components in MLI structure. Increment of number of switches is proportionate to the increase of probable faults and fault diagnosis. Therefore, it is crucial to overcome the drive's continuous operation under abnormal conditions. Several faults on switching elements are classified as short-circuit (SC) fault and open-circuit (OC) fault, which are mostly occurred on switches, diodes, gate-drive circuits, and so on.[9] The OC fault can prevail for many reasons like deterioration of inner wire, gate-signal fault, and so on. The SC fault can prevail on overcurrent, over-voltage, improper gate-signal fault issues, and so on.

Generally, SC fault is more troublesome to handle because of high-rated current flow, severely affecting the entire system and adjacent components. For the MIMD system's continuous performance under faults, formal protection circuits are used for sustaining the stable performance of drives like fuses, relays, breakers, and other protective circuits.[10] These are unfavorable because it de-energizes the MIMD from the main supply, which affects the unit's production and experiences economic loss. To defend the continuous functioning of the MIMD system, unique knowledge is needed on the behavior of various faults; fault identification and fault diagnosis are mandatory. For fault diagnosis, prior information is a pre-requisite for identifying the type of fault by using voltage and/or current sensing elements, limiting the entire drive system's failure. Although intended MLI topologies have been created successfully, too many applications with advanced technology, failure of switching elements, and fault diagnosis are an up-to-date area of many researchers.

Several researchers review fault diagnosis, which is focused initially on classical voltage-source inverters (VSI) topologies are explored in Reference 11. Some researchers highlight that the fault analysis is carried based on the output voltage and/or currents to establish the fault diagnosis system. Lezana et al proposes the study of the fault on a multilevel inverter, which consists of a more significant number of switching elements. The increasing importance of faults in MLI, several fault analysis and identification techniques are studied and implemented.[12] Priya et al studied the effect of SC fault on switching elements is very severe over the OC faults under no protective elements; several faults are analyzed with advanced algorithms proposed for analyzing and mitigating the faults to increase the reliability of drive system.[13]

The identification of IGBT switch-faults on MLI's are still a trendy concept, and several researchers are trying very hard to identify faults accurately. Based on the above facts, the inverter output voltage and currents are the key factors determining the fault switch of MLI topology by using the advanced methodology. Several traditional fault identification techniques are modified-slope algorithm developed to measure the slope of current-vector approach in complex αβ-plan,[14] using current reference sequences in Reference 15, frequency domain analysis using signal-processing techniques such as fast-Fourier transform (FFT) analysis,[16] discrete Fourier transform (DFT) analysis.[17] The discrete wavelet transform (DWT) strategy[18] is used to extract the effect of faults, fault type, fault occurrence in which phase and/or switch, gate-pulse, and so on, on outcomes of MLI at various frequency bands. The wavelet transforms evaluate a wave-shape simultaneously in both frequency and time-domains and very convenient to analyze the intermittent, non-periodic, transient, and non-stationary signals. A numerous wavelet technique is implemented and/or developed for signal interrogation and manipulation. In this paper, healthy and faulty conditions are carried on proposed symmetrical five-level inverter fed induction motor drive using discrete wavelet transform-multiresolution analysis (DWT-MRA) based feature extraction methodology (FEM) analysis. Individual and dual fault constraints are considered to validate the proposed MIMD system using Matlab/Simulink tool; results are conferred with comparisons.

The major objectives of the paper is as follows:

1. To analyze the proposed topology under healthy conditions using discrete wavelet transforms.
2. To analyze the proposed topology under different open circuit fault conditions using discrete wavelet transforms.
3. To analyze the proposed topology under other short circuit fault conditions using discrete wavelet transforms.

2 | HEALTHY CONDITION OF NEWLY PROPOSED SYMMETRIC MLI TOPOLOGY

The newly proposed five-level symmetrical MLI topology requires equal DC sources ($V_{dc1} = V_{dc2}$). The staircase output voltage is acquired based on the series action of DC-link voltages as ($V_{dc} = V_{dc1} + V_{dc2}$). The newly proposed topology requires six IGBT switches, two equal DC sources, a single load, and a switching pattern. A front-end diode-bridge rectifier is used to convert the single-phase AC supply to definite DC voltage by interfacing a DC-link capacitor. The DC-link capacitor acts as an interface between the front-end rectifier and the proposed MLI topology. The input DC voltage is transformed to AC staircase voltage by conducting the respective switches appropriately; the five-level voltages are V_{dc}, $2V_{dc}$, $0V_{dc}$, $-V_{dc}$, and $-2V_{dc}$ (Figure 1 and Table 1).

The high-switching frequency-based modulation schemes are extensively recognized for generating a feasible switching pattern named multi-carrier pulse-width modulation schemes.[19] This multi-carrier PWM scheme commands the pulse-width of the output voltage to regulate the dv/dt stress, harmonic shifting, loss minimization, and so on. The scheme requires a single sinusoidal reference signal and several triangular carrier signals for the generation of switching patterns, considered as sinusoidal switching pattern technique (SPWM) commanded by modulation index (m_{in}). The modulation index is differentiated based on amplitudes of sinusoidal reference (A_r) and triangular carrier (A_c) signals; it varies from 0 to 1, as shown in Equation (1).

$$m_{in} = \frac{A_r}{A_c} \; (m_{in} \leq 1) \tag{1}$$

The magnitude of output staircase voltage (V_o) waveform is dependent on input DC-link voltage (V_{dc}) and the modulation index (m_{in}) as shown in Equation (2),

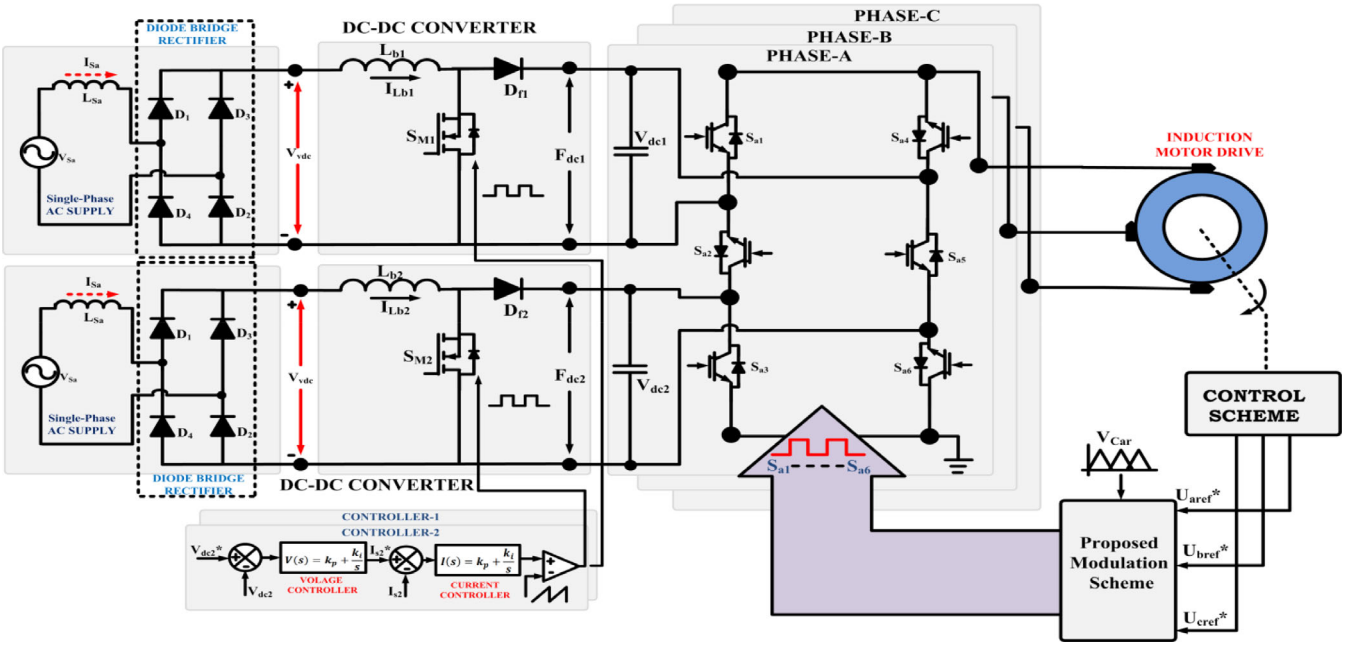


FIGURE 1 Schematic diagram of proposed three-phase five-level symmetric MLI fed induction motor drive system

TABLE 1 Switching sequences of proposed five-level symmetric MLI topology

Outcome voltages	S_1	S_2	S_3	S_4	S_5	S_6
V_{dc}	N	F	F	F	N	N
$2\,V_{dc}$	N	F	N	F	N	F
$-V_{dc}$	F	N	N	N	F	F
$-2\,V_{dc}$	F	N	F	N	F	N
$0\,V_{dc}$	F	F	F	N	N	N

Abbreviations: F, OFF state; N, ON state.

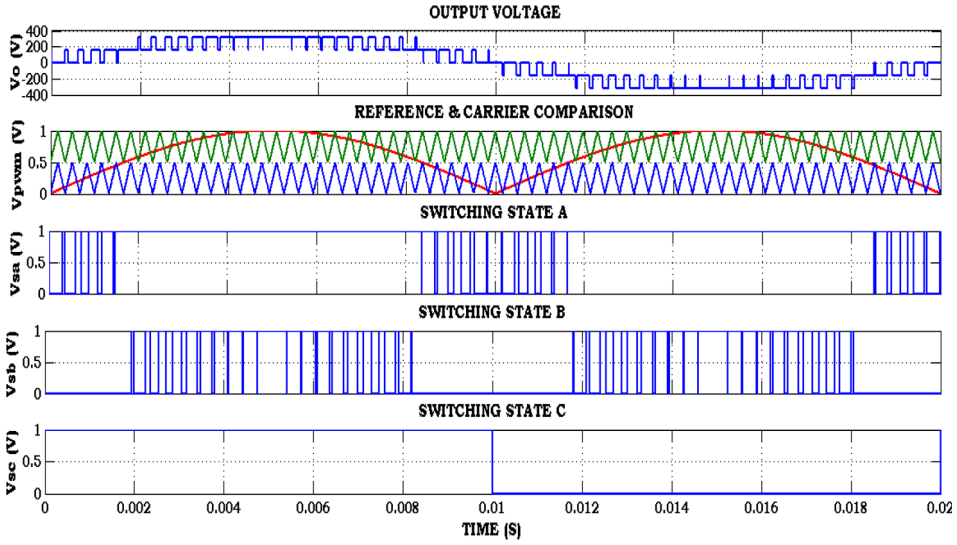


FIGURE 2 Simplified switching pattern

$$V_o = m_{\text{in}} * V_{\text{dc}} \tag{2}$$

Among the classical SPWM techniques, phase-shifted modulation (PS-PWM) technique,[20] level-shifted modulation (LS-PWM) technique,[21] and space vector modulation (SVPWM) technique[22] are reviewed by so many works of literature to control the staircase output waveform of MLI topology. This paper employs the new simplified multi-carrier based sinusoidal PWM technique consisted of one reference signal U_{aref}*, U_{bref}* U_{cref}* is compared with a dual carrier signal (V_{car1}, V_{car2}). All the carriers have high switching frequency with a little difference in peak magnitude and are disposed of vertically. The carrier signals are compared with dual carrier signals to create the switching states A and B. These switching states A and B are controlled by an additional pulse generated switching state C. This simplified switching technique has been used for controlling the switches in the proposed MLI topology for getting constant five-level output voltage under normal or post-fault conditions. The generation of optimal pulses to the proper switches is defined by mathematical notation which is depicted in Equation (3). The switching pattern of the proposed five-level symmetric MLI is shown in Figure 2.

$$\begin{aligned} S_{a1} &= \bar{A}C + \bar{C} \\ S_{a2} &= C \\ S_{a3} &= \bar{B}C + \bar{A}\bar{C} + B\bar{C} \\ S_{b1} &= AC \\ S_{b2} &= \bar{C}A \\ S_{b3} &= BC \end{aligned} \tag{3}$$

3 | SEVERAL OPEN-CIRCUIT AND SHORT-CIRCUITED FAULTS

The most active common faults are open-circuit (OC) and short-circuit (SC) faults of power switches, short-circuit of DC-link capacitor, and so on, applicable in MLI fed induction motor drive system. These faulty conditions create a malfunction of the over-all drive system due to excessive electrical and thermal stress experiencing on many applications. Most systematic faults in MIMD system is categorized as gate-open circuit (GOC) fault, gate-short circuit (GSC) fault, diode-open circuit (DOC) fault, diode-short circuit (DSC) fault, IGBT-open circuit (IOC) fault and IGBT-short circuit (ISC) faults, as clearly shown in Figure 3.

Figure 3A represents the GOC-fault in phase-A of switch S_{a5} in the proposed MIMD system by opening the gate-pulse signal of the respective switch S_{a5}. During this faulty instant, it is un-feasible to transfer energy to I.M. drive for continuous

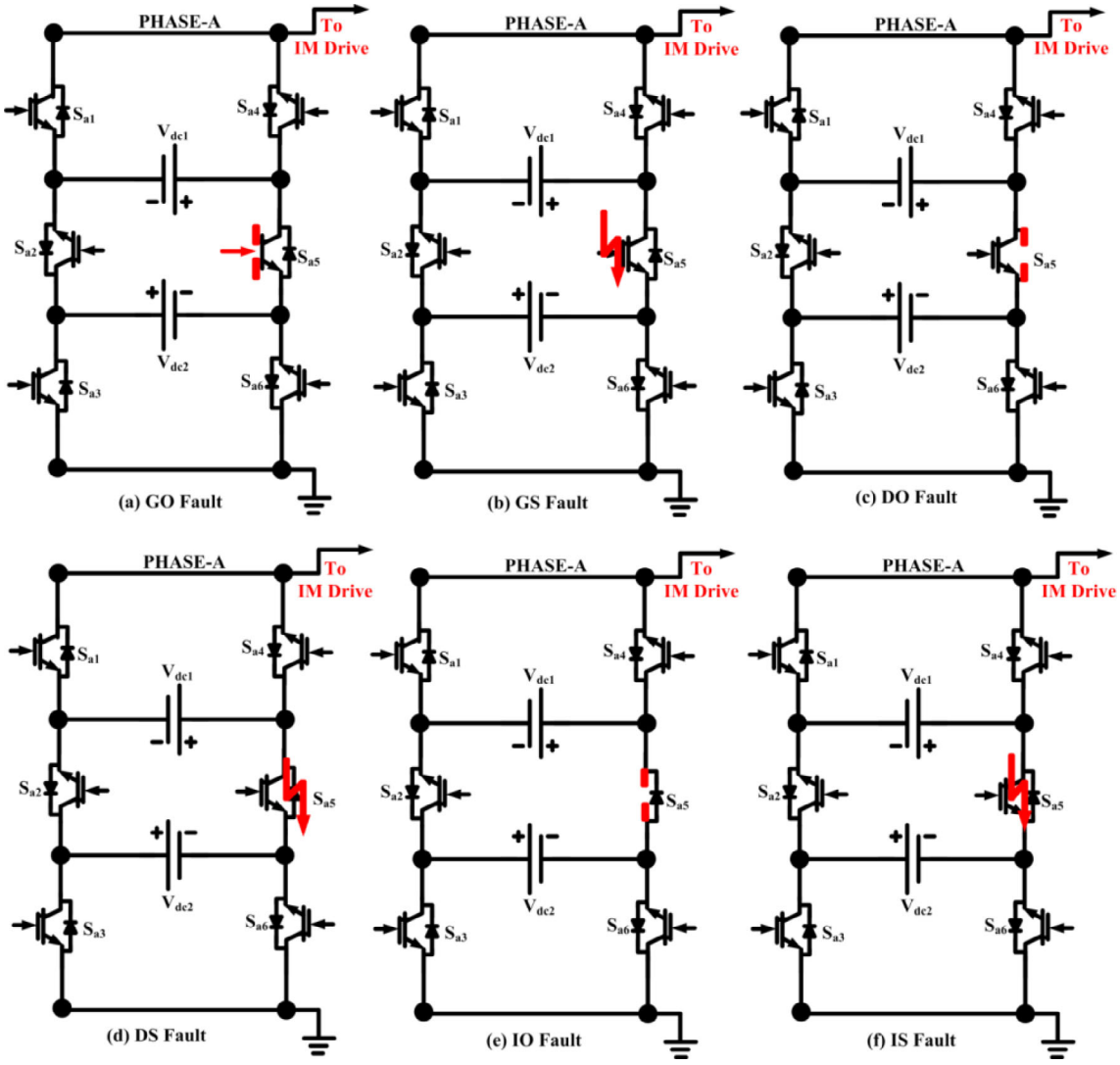


FIGURE 3 Several open and short-circuited fault conditions

operation. This is because the current flow path is affected and unbalanced in the negative region. The output phase-A voltage is involved in the positive region. It implies the drive's speed and electromagnetic torque, which degrades IM's performance in a gate-open fault situation. Figure 3B represents the GSC-fault in phase-A of switch S_{a5} in the proposed MIMD system by creating the short circuit on the gate-pulse signal of the respective switch S_{a5}. It is feasible to flow high amounts of unbalanced current to IM drive and affected positive region during this faulty instant. The output phase-A voltage is affected in the negative region; it implies the drive's speed and electromagnetic torque, which degrades the IM drive in a gate-short fault situation. Similarly, several fault conditions are applied to the proposed MIMD system to develop a feasible fault diagnosis system to increase the drive system's reliability. In this paper, a discrete-wavelet transform (DWT) analysis is carried on the proposed MIMD system to analyze faulty situations and faulty cells. The DWT furnishes the efficient path to decompose the time-series from time-domain to scale-domain, localizing the change over time-state with definite scale factors. The faults mentioned above are analyzed by using DWT with the help of FEM analysis.

4 | FAULT ANALYSIS USING DISCRETE WAVELET TRANSFORMS

The wavelet transform (WT) was first introduced in 1980 by enchantment in image/signal processing system and merely power-engineering applications. It is just like a linear transformation process like Fourier or fast Fourier transforms, with a slight difference that it recognizes the time-localization scheme of distinct frequency components of the

respective signal. The short-time Fourier transform attains partly the same things but is used as fixed-width windowing analyzed functions. WTs have diagnosed functions as wavelets. It will adjust the time-width of respective frequency in an efficient path as higher/lower frequency with narrow/wide characterization.[18,23] This multi-resolution character is predominantly used for analyzing the fault transient's high-frequency signals that are super-imposing on power frequency signals.[24] So, WTs are most suitable for analyzing the signals with small-lived high-frequency disturbances super-imposed on low-frequency continuous signals under its zoom inability. The function, $x(t)$, is analyzed by continuous wavelet transform (CWT) as,

$$\mathrm{WT}(a,b) = \frac{1}{\sqrt{a}} \int_{-\infty}^{\infty} x(t) \psi \left(\frac{t-b}{a} \right) dt \tag{4}$$

where (a, b) are scaling and translation constants, ψ is assumed as simplicity of real wavelet-function. In CWT, the mother wavelet function is translated and dilated continuously over a continuous real function, so it furnishes significant redundant information. The mother-wavelet function can be discretely translated and dilated by substitute as $a = a_o^m$ and $b = nb_o a_o^m$; whereas a_o, b_o is the exact constants with $a_o > 1$, $b_o > 0$, and m, n as N is the range of positive integers. The new mother wavelet in discrete function is defined as

$$m,n(t) = a_o^{-\frac{m}{2}} \left(\frac{t - nb_o a_o^m}{a_o^m} \right) \tag{5}$$

and the relative DWT is defined as follows:

$$\mathrm{DWT}x(m,n) = \int_{-\infty}^{\infty} x(t)^*_{m,n}(t) dt \tag{6}$$

The DWT analysis is a very well-known technique for evaluating the signals in the event of transient response related to several faults in power-electronic converters, power transmission/distribution systems, and so on. It decomposes a respective signal into several scales with divergent time-frequency resolutions. The DWT-MRA technique plays a vital role in the DWT series,[25] which decomposes an original signal usually non-stationary form into low-frequency signal called "Approximations," and the high-frequency signal called "Details," with divergent scales/levels of resolution that utilizes the mother wavelet as a prototype function. The analyzed signal is a convolution signal that acquires an approximated signal with a low-pass filter at every level. The convolution of a signal attains the exact signal by the high-pass filter, and a dyadic decimation process accompanies both the signals. The procedure evaluates the discrete signal $x[n]$ of length "N" passing through a digital high-pass filter with an impulsive response $h[n]$. The high-pass and low-pass filters are treated as wavelet and scaling filters, respectively. The outcome of the low-pass filter is approximated coefficients of the discrete signal at the first-level of MRA and the outcome from the high-pass filter are the detailed coefficients of the signal at the first level of MRA of DWT series.[26,27] The outcome of respective high and/or low pass filters comprised of N-wavelet coefficient functions. This initiates the first level of decomposition of discrete signal and can be represented mathematically as,

$$a^1[n] = \sum_{k=0}^{N-1} g[k] x[n-k] \tag{7}$$

$$d^1[n] = \sum_{k=0}^{N-1} h[k] x[n-k] \tag{8}$$

The approximated coefficients a^1 at the first level of MRA are used to input another set of wavelet filter (analogous with the first pair) sampled by dual functionality. The second level of resolution filters produces the set of new approximations and detail coefficients of length N/2. This establishes the second level of decomposition of discrete signal and represented mathematically as,

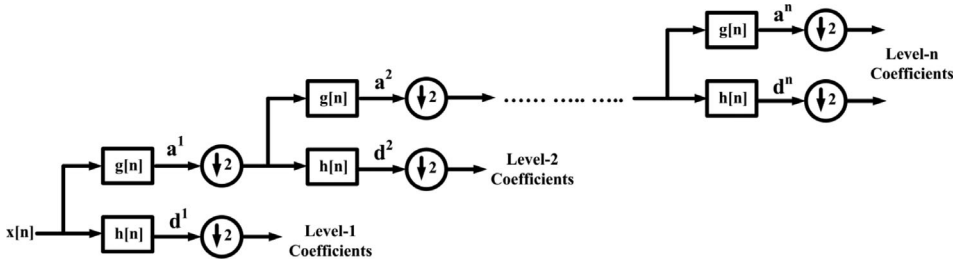


FIGURE 4 Decomposition process of discrete signal of DWT

$$a^2[n] = \sum_{k=0}^{\frac{N}{2}-1} g[k]a^1[2n-k] \tag{9}$$

$$d^2[n] = \sum_{k=0}^{\frac{N}{2}-1} h[k]a^1[2n-k] \tag{10}$$

Likewise, this decomposition process is repeatedly at level-3, level-4, level-5, and so on to level-n, to enhance the frequency-resolution of a discrete signal. In this way, the wavelet decomposition level-9 was utilized for the extraction of efficient wavelet features. In this work, the wavelet families utilize the Haar wavelet because a single wavelet function with the non-child wavelet and other wavelet functions has child wavelets. A high transformation value is produced if the wavelet function satisfies the signal's shape well within a distinct location and scale. On the other half, if the wavelet signals and functions in-correlate, then a low transformation value is produced. The decomposition process of the discrete signal is shown in Figure 4.

In general, the MIMD system's fault is determined by the slope of the line current measured by current sensors. It resembles the differentiation of the actual line current with a healthy line current can be distinguished in Equation (11) as follows:

$$I_{\text{slope}} = \frac{(I_{\text{act}} - I_h)}{dt} \times \frac{1}{2\pi f \times |I_{\text{act}}|} \tag{11}$$

The above-mentioned Equation (11) specifies the presence of a fault in the proposed MIMD system, but this is unsuitable for dynamic, varying situations. A novel, simple wavelet decomposition feature technique is effectively used for fault occurrence based on decomposition feature rate (DFR). This rate is determined by FEM of line currents under healthy and faulty conditions of the MIMD system, it can be distinguished in Equation (12) as follows:

$$D_{fr} = \frac{\text{std}(d2) + \text{std}(d3) + \text{std}(d4)...\text{std}\,(dn-2)}{\text{std}(dn-1) \times n} \times 100 \tag{12}$$

where D_{fr} is decomposition feature rate, n is the number of levels, and STD is the standard deviation at different levels and measured from feature extraction of line currents values under healthy and faulty conditions.

5 | SIMULATION RESULTS AND ANALYSIS

Generally, the proposed MIMD system is powered by a single-phase AC source with a front-end AC-DC/DC-DC converter for getting constant DC-link voltages to the multilevel inverter with enhanced power-quality features at AC utility side. The proposed multilevel inverter topology is controlled by an optimal switching pattern generated by a new simplified multi-carrier based sinusoidal PWM technique with the pre-requisite of single reference and dual-carrier signals. The IM drive's speed is controlled by changing the switching pattern's modulation index; the rated speed of the IM drive under healthy condition is 1360 rpm to attain the load torque 10 N-m. Several faults in the MIMD system created

TABLE 2 Operating specifications

Parameters	Values
AC source	Vsa-230 V, F-50 Hz
Inductors	Lb1 = Lb2 = 1.2 mH
DC-link capacitor	Cdc-690 μF, Vdc1-Vdc2-200 V
Switching frequency	Fs-3050 Hz
Induction motor	Vo-400V, Pm-10HP, Tm-10 N-m

by using a command signal, a command signal set as "0" for open-circuit fault and "1" for short-circuit fault conditions. Several faults are applied to the proposed MIMD system, which is evaluated using DWT-MRA analysis using an effective Matlab/Simulink tool. This DWT-MRA furnishes the signal analysis at different frequency ranges based on the level of decomposition and extracts the faulty switches and faulty phases by measuring mean, median, standard deviation, and so on, values by using feature decomposition rate. The following section presents the MIMD system's outcome in healthy conditions, and several faulty conditions are discussed with proper specifications. The operating specifications of the MIMD system are illustrated in Table 2.

5.1 | Case A: Performance evaluation of three-phase five-level reduced switch symmetric MLI topology fed induction motor drive under healthy condition

The attractive performance of the proposed reduced-switch symmetric MLI topology fed induction motor drive is evaluated under healthy conditions by using Matlab/Simulink tool, and results are presented. In that (a) three phase line currents, (b) stator current, (c) rotor speed, (d) electromagnetic torque, respectively, as shown in Figure 5. The sinusoidal line currents (I_{Labc}) are maintained constant with a value of 43.1 A displaced by 120° phase displacement. The characterization of reduced-switch MLI topology fed induction motor drive is attained from stator current (I_{sa}) maintained sinusoidal and constant with a value of 58 A at starting and 43.1 A at the steady-state condition. The induction motor (N_{r}) reaches the steady-state constant value as 1360 rpm with a time of 0.1 second. The electromagnetic torque (T_{e}) of the induction motor is nearly 45 N-m starting and slowly reduces to a predefined value 10 N-m settles the rated mechanical torque when speed attains the steady-state region.

5.2 | Case B: Performance evaluation of three-phase five-level reduced switch symmetric MLI topology fed induction motor drive under GOC fault condition

The attractive performance of the proposed reduced-switch symmetric MLI topology fed induction motor drive is evaluated under GOC fault condition, as shown in Figure 6. The GOC fault is initiated at a time instant of 0.5 second by furnishing the gate-pulse opening by adding the step response to the switching pattern of switch S_{a5} in the proposed MIMD system. Due to this open-fault on gate-pulse generation, the switch S_{a5} is treated as a gate-pulse failure and affected by MLI and the induction motor drive's specific characteristics. In pre-fault, the line-currents (I_{Labc}) are maintained constant with a value of 43.1 A and displaced by 120° phase displacement. During a fault, the faulty phase's line current is eventually decreased and unbalanced with a value of 12 A in the negative half-cycle, and other phases are slightly decreased to 8 A. Due to this, the induction motor may losses the mechanical characteristics and attains noisy operation. In pre-fault condition, current wave-shape is maintained with a value of 43 A; during fault current, wave-shape is decreased to 12 A in negative regions. The rotor speed (N_{r}) is held constant as 1360 rpm in pre-fault condition, steadily fluctuated, and slightly reduced to 1050 rpm under fault condition. The electromagnetic torque (T_{e}) of the induction motor is nearly 10 N-m in pre-fault conditions to achieve the rated mechanical load. During a fault, torque is fluctuated and decreased to 3.5 N-m and retrieved to rated torque within a time of 0.2 second, which affects the stability index of the entire induction motor drive system.

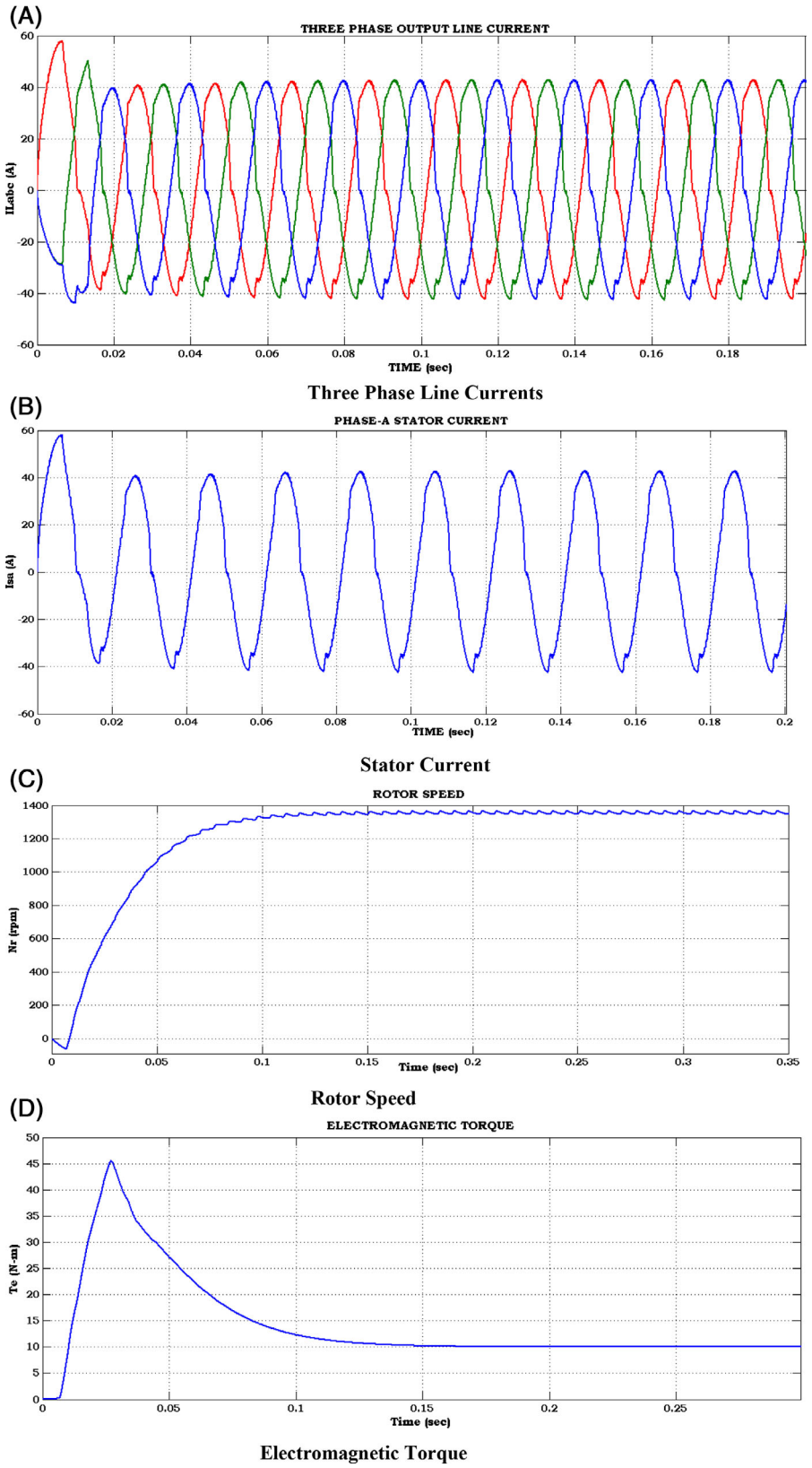
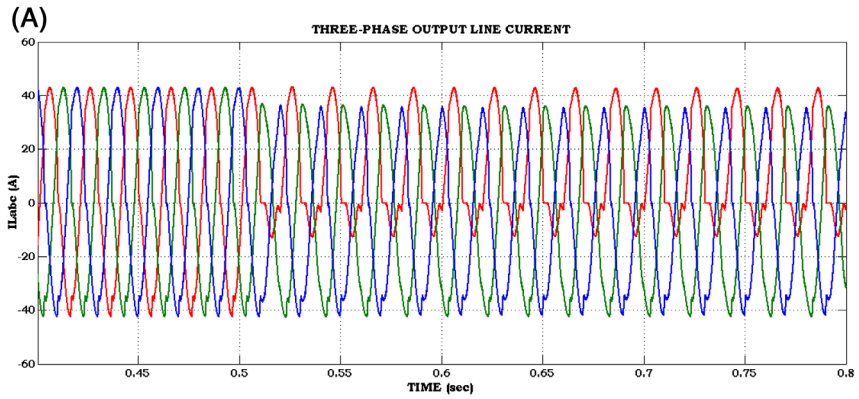
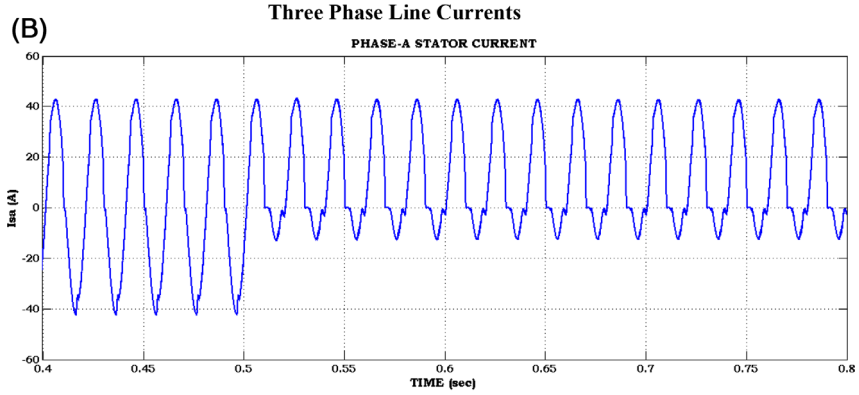


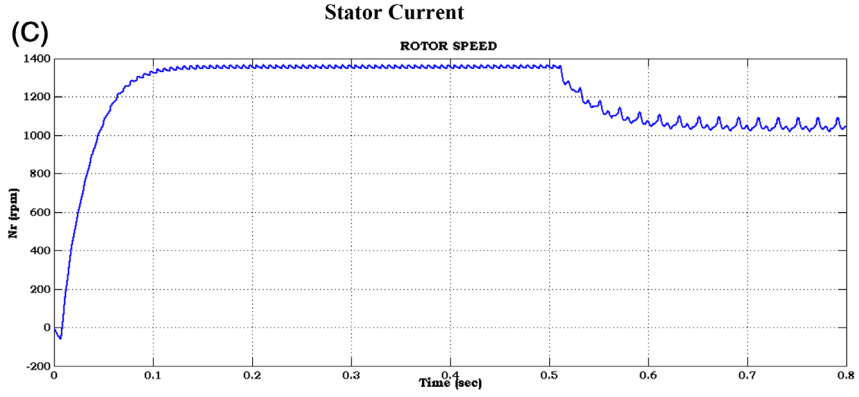
FIGURE 5 Simulation outcomes of three-phase five-level reduced switch symmetric MLI topology fed induction motor drive under healthy condition. A, Three phase line currents. B, Stator current. C, Rotor speed. D, Electromagnetic torque



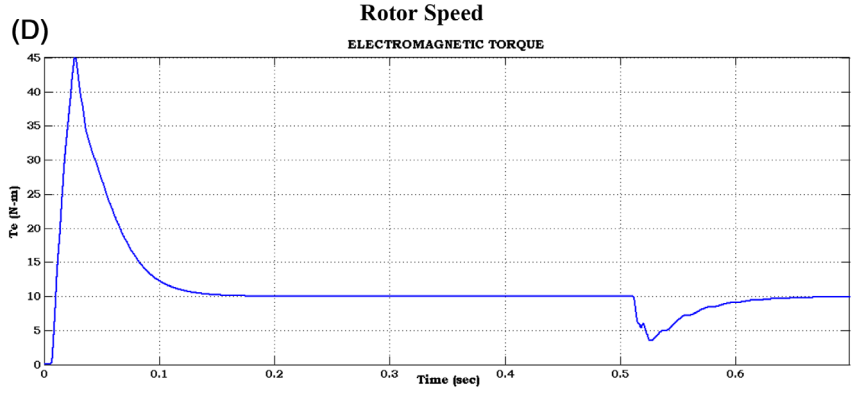
Three Phase Line Currents



Stator Current



Rotor Speed



Electromagnetic Torque

FIGURE 6 Simulation outcomes of three-phase five-level reduced switch symmetric MLI topology fed induction motor drive under GOC faulty condition. A, Three phase line currents. B, Stator current. C, Rotor speed. D, Electromagnetic torque

5.3 | Case C: Performance evaluation of three-phase five-level reduced switch symmetric MLI topology fed induction motor drive under GSC fault condition

The attractive performance of the proposed reduced-switch symmetric MLI topology fed induction motor drive is evaluated under GSC fault condition, as shown in Figure 7. The GSC fault is initiated at a time instant of 0.5 second by furnishing the misfiring of gate-pulse by adding the step response to the switching pattern of switch S_{a5} at different phase angles over the desired switching angles. Due to this short-circuited fault on gate-pulse generation, the switch S_{a5} is treated as a mal-function of gate-pulse and affected by MLI and induction motor drive characteristics. In pre-fault, the line-currents (I_{Labc}) are maintained constant with a value of 43.1 A and displaced by 120° phase displacement. During a fault, the faulty phase's line current is eventually decreased & unbalanced with a value of 27.5 A in positive half-cycle, and other phases are maintained constant. Due to this, the induction motor may losses the mechanical characteristics and attains noisy operation. In pre-fault condition, stator current (I_{sa}) wave-shape is maintained with a value of 43 A, during GSC fault current wave-shape is decreased to 27.1 A in the positive region. The rotor speed (N_{r}) is maintained constant value as 1360 rpm in pre-fault condition, steadily fluctuated, and slightly reduced to 1230 rpm under fault condition. The electromagnetic torque (T_{e}) of the induction motor is nearly 10 N-m in pre-fault conditions to achieve the rated mechanical load. During a fault, torque is fluctuated and decreased to 6 N-m and retrieved to rated torque within a time of 0.15 second, which affects the stability index of the entire induction motor drive system.

5.4 | Case D: Performance evaluation of three-phase five-level reduced switch symmetric MLI topology fed induction motor drive under DOC fault condition

The attractive performance of the proposed reduced-switch symmetric MLI topology fed induction motor drive is evaluated under DOC fault condition, as shown in Figure 8. The DOC fault is initiated at a time instant of 0.5 second by furnishing the open-circuit fault condition with additional diode-circuitry by adding the step response to the switching pattern of switch S_{a5}. Due to this open-circuit fault on the respective switch's diode, S_{a5} is treated as malfunctioning of the diode and slightly affected by MLI and the induction motor drive's characteristics. In pre-fault, the line-currents (I_{Labc}) are maintained constant with a value of 43.1 A and displaced by 120° phase displacement. During a fault, the faulty phase's line current is slightly decreased and unbalanced with a value of 41 A as attain more spikes in positive half-cycle, and other phases are also affected and decreased somewhat. In pre-fault condition, stator current (I_{sa}) wave-shape is maintained with a value of 43 A, during GOC fault current wave-shape is decreased to 41 A in the positive region. The rotor speed (N_{r}) is maintained constant value as 1360 rpm in pre-fault condition, steadily fluctuated, and slightly reduced to 1220 rpm under DOC fault condition. The electromagnetic torque (T_{e}) of the induction motor is nearly 10 N-m in pre-fault conditions to achieve the rated mechanical load. During DOC fault, torque is fluctuated and decreased to −8.89 N-m and retrieved to rated torque within a time of 0.1 second, which affects the stability index of the entire induction motor drive system.

5.5 | Case E: Performance evaluation of three-phase five-level reduced switch symmetric MLI topology fed induction motor drive under DSC fault condition

The attractive performance of the proposed reduced-switch symmetric MLI topology fed induction motor drive is evaluated under DSC fault condition, as shown in Figure 9. The DSC fault is initiated at a time of 0.5 second by furnishing the short-circuit fault condition with additional diode-circuitry by adding the step response to the switching pattern of switch S_{a5}. Due to this short-circuit fault on the respective switch's diode, S_{a5} is treated as a misfiring of the diode and slightly affected by MLI and the induction motor drive's characteristics. In pre-fault, the line-currents (I_{Labc}) are maintained constant with a value of 43.1 A and displaced by 120° phase displacement. During DSC fault, the faulty phase's line current is slightly decreased and unbalanced with a value of 27 A in positive half-cycle, and other phases are also affected and slightly decreased. In pre-fault condition, stator current (I_{sa}) wave-shape is maintained with a value of 43 A, during DSC fault current wave-shape is decreased to 27 A in the positive region. The rotor speed (N_{r}) is maintained constant value as 1360 rpm in pre-fault condition, steadily fluctuated, and slightly reduced to 1230 rpm under DSC-fault condition. The electromagnetic torque (T_{e}) of the induction motor is nearly 10 N-m in pre-fault conditions to achieve the rated mechanical load. During DSC-fault, torque is fluctuated and decreased to 5.9 N-m and

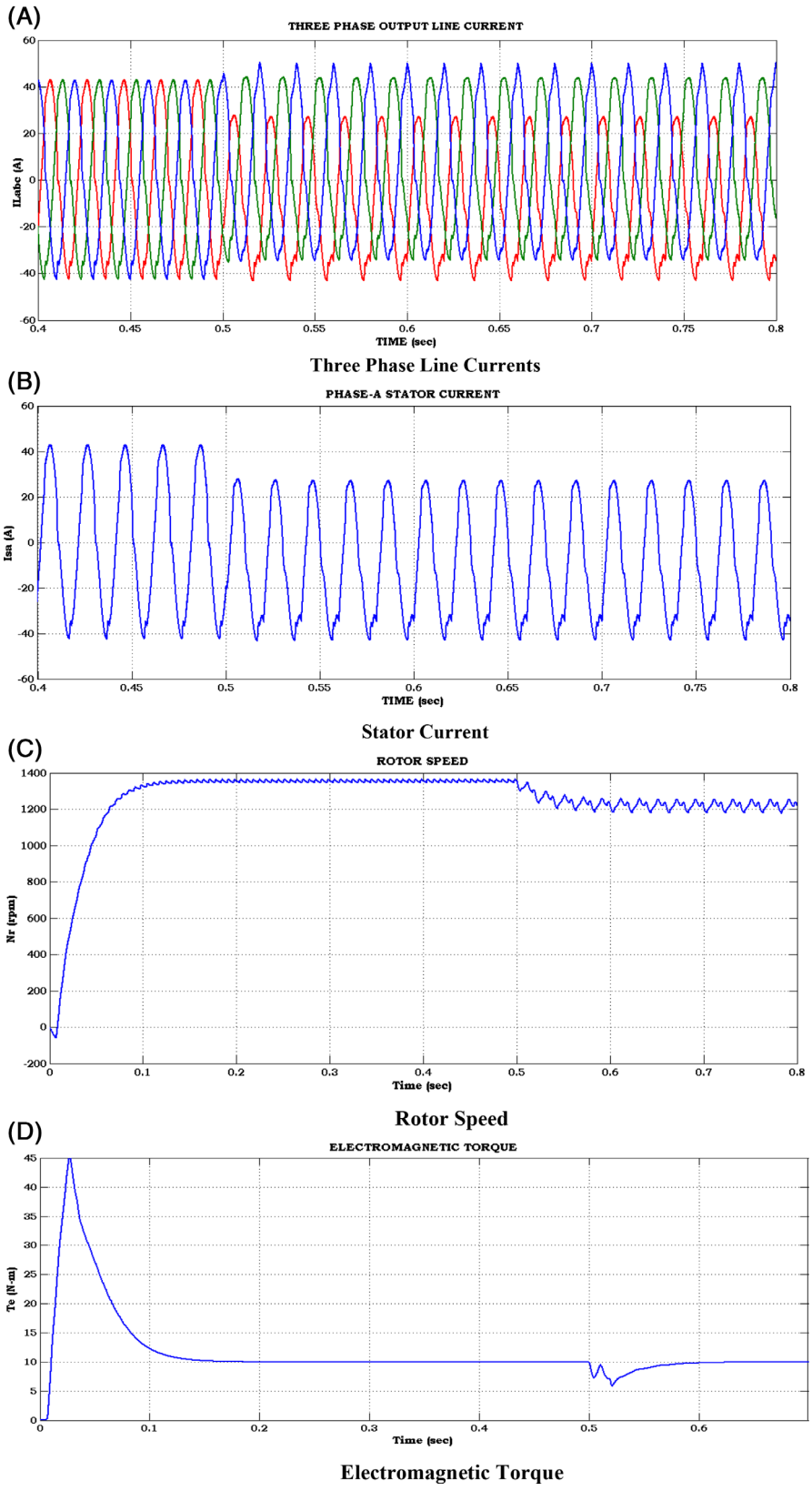


FIGURE 7 Simulation outcomes of three-phase five-level reduced switch symmetric MLI topology fed induction motor drive under GSC faulty condition. A, Three phase line currents. B, Stator current. C, Rotor speed. D, Electromagnetic torque

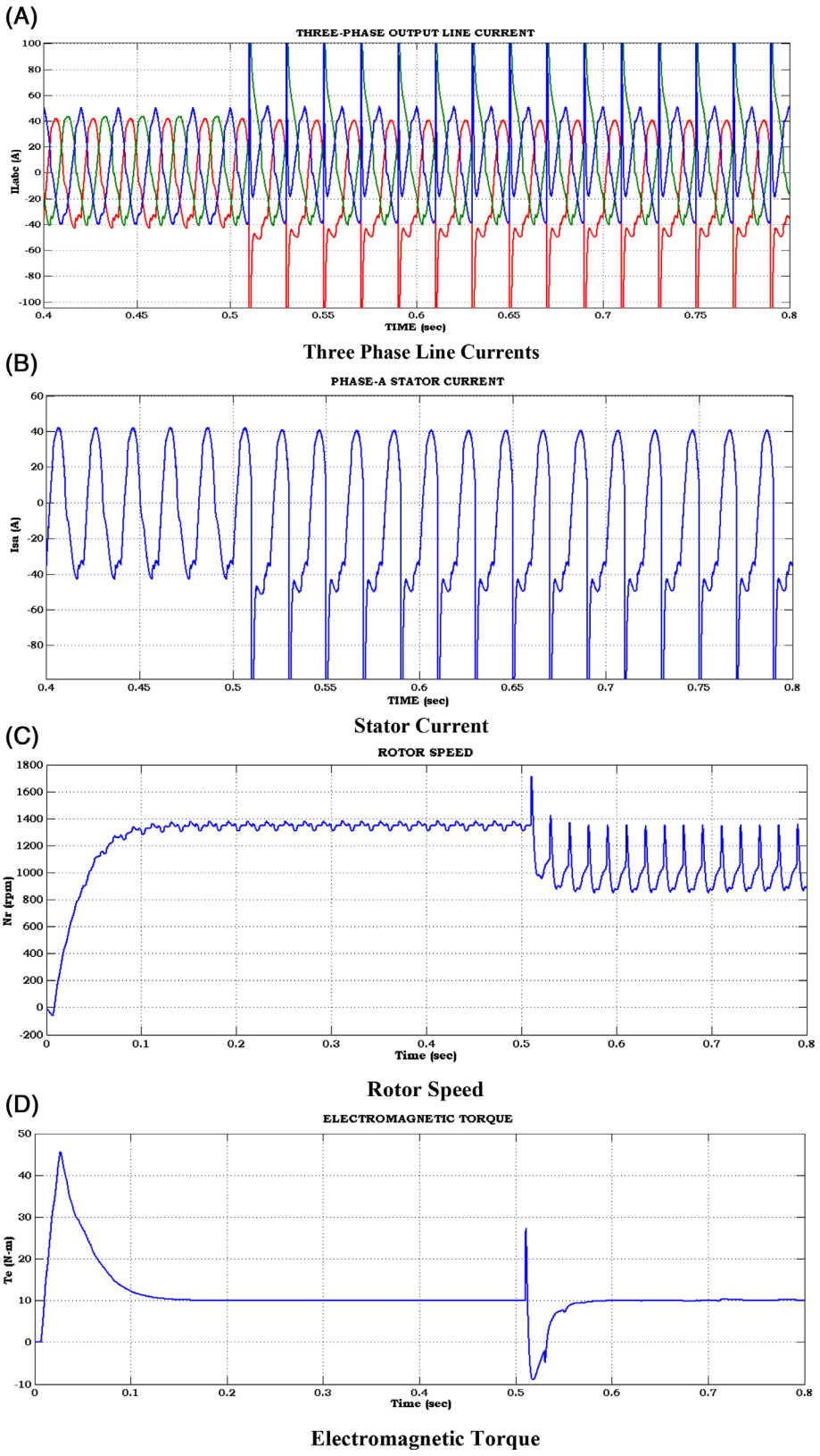
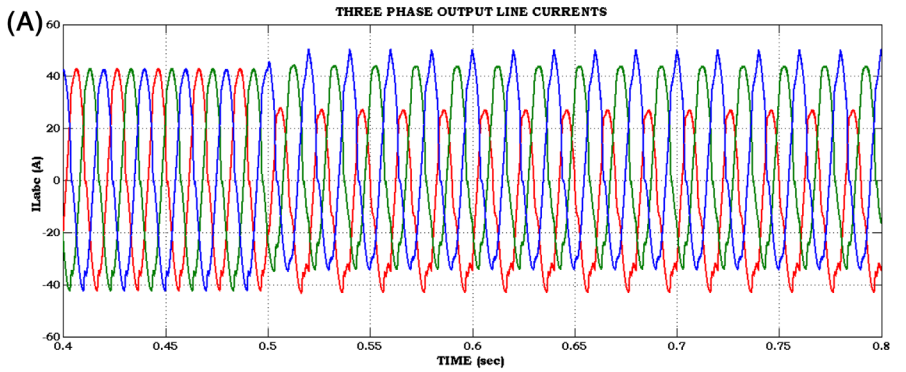
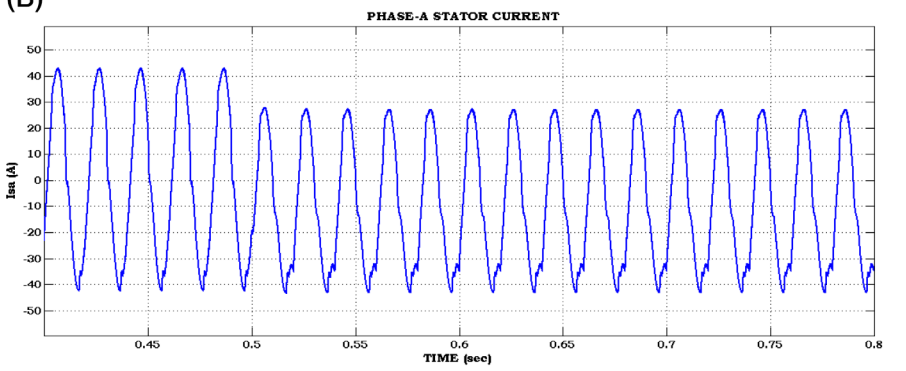


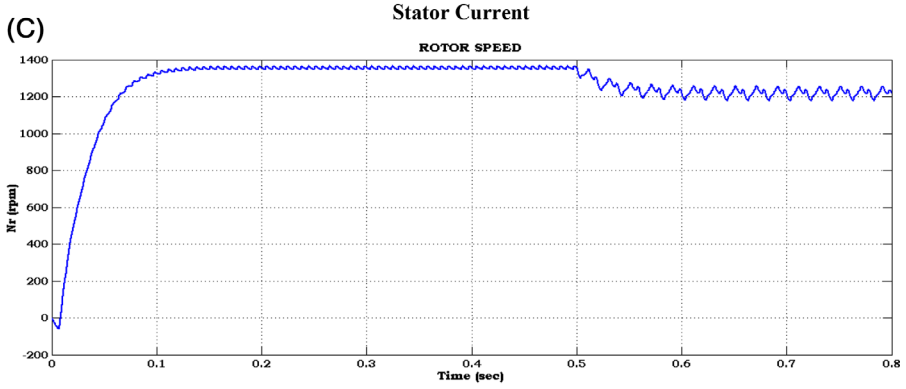
FIGURE 8 Simulation outcomes of three-phase five-level reduced switch symmetric MLI topology fed induction motor drive under DOC faulty condition. A, Three phase line currents. B, Stator current. C, Rotor speed. D, Electromagnetic torque



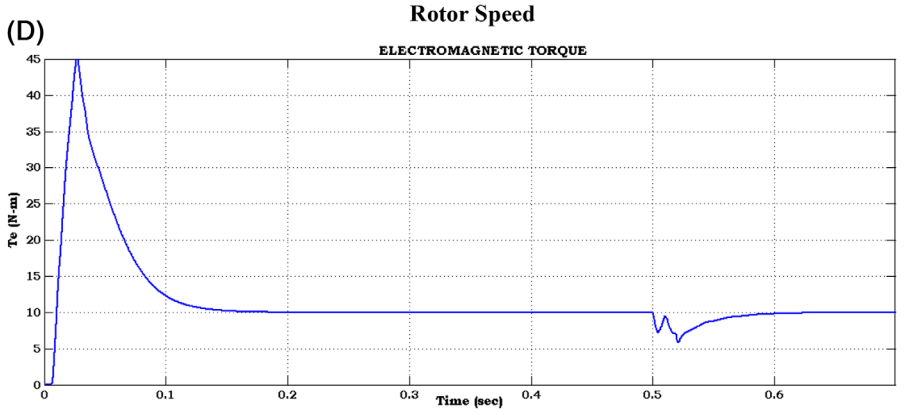
Three Phase Line Currents



Stator Current



Rotor Speed



Electromagnetic Torque

FIGURE 9 Simulation outcomes of three-phase five-level reduced switch symmetric MLI topology fed induction motor drive under DSC faulty condition. A, Three phase line currents. B, Stator current. C, Rotor speed. D, Electromagnetic torque

retrieved to rated torque within a time of 0.12 second, which affects the stability index of the entire induction motor drive system.

5.6 | Case F: Performance evaluation of three-phase five-level reduced switch symmetric MLI topology fed induction motor drive under IOC fault condition

The attractive performance of the proposed reduced-switch symmetric MLI topology fed induction motor drive is evaluated under IOC fault conditions, as shown in Figure 10. The IOC fault is initiated at a time of 0.5 second by creating the open-circuit pulse with an additional step response to a switching pattern of switch S_{a5} in the proposed MIMD system. Due to this open-fault on the IGBT switch, the switch S_{a5} is treated as an IGBT switch is mis-operated and affected by MLI and the induction motor drive's specific characteristics. In pre-fault, the line-currents (I_{Labc}) are maintained constant with a value of 43.1 A and displaced by 120° phase displacement. During IOC fault, the faulty phase's line current is eventually decreased and unbalanced with a value of 12 A in the negative half-cycle, and other phases are slightly decreased to 8 A. Due to this, the induction motor may losses the mechanical characteristics and attains noisy operation. In pre-fault condition, the current wave-shape is maintained with a value of 43 A; during IOC fault current wave-shape is decreased to 12 A in negative regions. The rotor speed (N_{r}) is maintained constant value as 1360 rpm in pre-fault condition, steadily fluctuated, and slightly reduced to 1050 rpm under the IOC-fault condition. The electromagnetic torque (T_{e}) of the induction motor is nearly 10 N-m in pre-fault conditions to achieve the rated mechanical load. During IOC-fault, torque is fluctuated and decreased to 3.5 N-m and retrieved to rated torque within a time of 0.2 second, which affects the stability index of the entire induction motor drive system.

5.7 | Case G: Performance evaluation of three-phase five-level reduced switch symmetric MLI topology fed induction motor drive under ISC fault condition

The attractive performance of the proposed reduced-switch symmetric MLI topology fed induction motor drive is evaluated under the ISC fault condition, as shown in Figure 11. The ISC fault is initiated at a time of 0.5 second by furnishing the IGBT switch's misfiring by adding the step response to the switching pattern of IGBT switch S_{a5}. Due to this short-circuited fault on gate-pulse generation, the switch S_{a5} is treated as a malfunction of the IGBT switch affected by MLI and induction motor drive characteristics. In pre-fault, the line-currents (I_{Labc}) are maintained constant with a value of 43.1 A and displaced by 120° phase displacement. During ISC fault, the faulty phase's line current is eventually decreased and unbalanced with a value of 27.5 A in positive half-cycle, and other phases are maintained constant. Due to this, the induction motor may losses the mechanical characteristics and attains noisy operation. In pre-fault condition, stator current (I_{sa}) wave-shape is maintained with a value of 43 A, during ISC fault current wave-shape is decreased to 27.1 A in the positive region.

The rotor speed (N_{r}) is maintained constant value as 1360 rpm in pre-fault condition steadily fluctuated and slightly reduced to 1230 rpm under the ISC-fault condition. The electromagnetic torque (T_{e}) of the induction motor is nearly 10 N-m in pre-fault conditions to achieve the rated mechanical load. During ISC-fault, torque is fluctuated and decreased to 6 N-m and retrieved to rated torque within a time of 0.15 second, which affects the stability index of the entire induction motor drive system. The DWT-MRA energy content of both short-circuits and open-circuit fault conditions is observed; there is modest variation in healthy condition energy content. As expected, a healthy condition's energy content is more significant compared with both open and short-circuited fault conditions. It exists there is little difference between the various fault components. Based on this analysis, several signatures are carried out, such as mean, median, maximum, standard deviation, mode, and so on. Using feature extraction methodology under healthy, open-circuit, and short-circuit faulty conditions. Several signatures are measured concerning the level of decomposition (level-9) under healthy condition, OC faulty condition; SC faulty condition and are illustrated in Figures 12, 13 and 14, respectively.

The discrete wavelet transform is generally used to extract time-frequency features in the particular signal under healthy and faulty conditions by utilizing multi-resolution analysis. The superior method developed for most practical relevance by decomposing the original loaded signal under non-stationary form into the low-frequency signal, as approximations and are transformed into the high-frequency signal as details with different levels resolutions. The DAQ-9227 current acquisition card will measure the values up to predefined levels directly from the

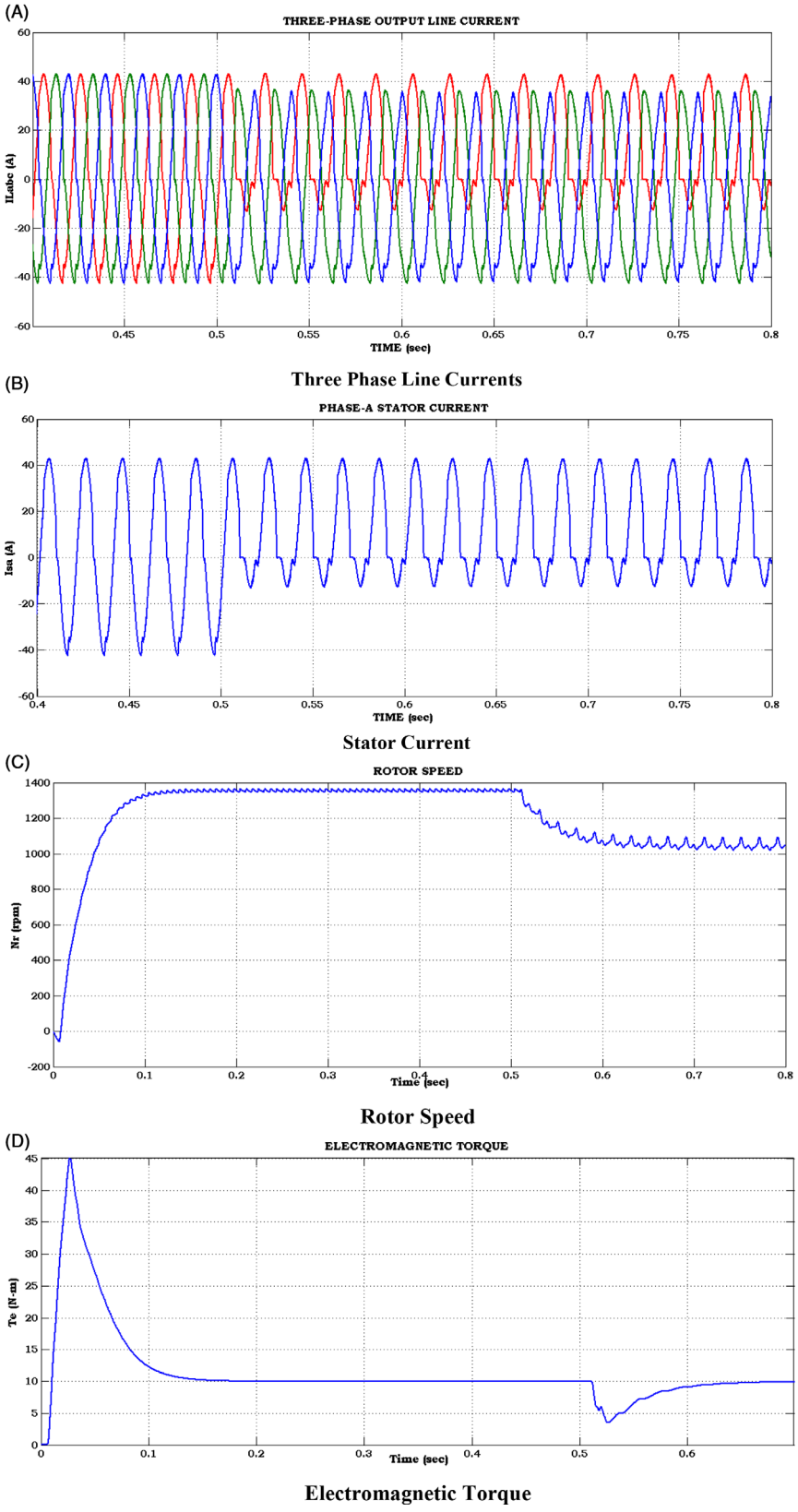
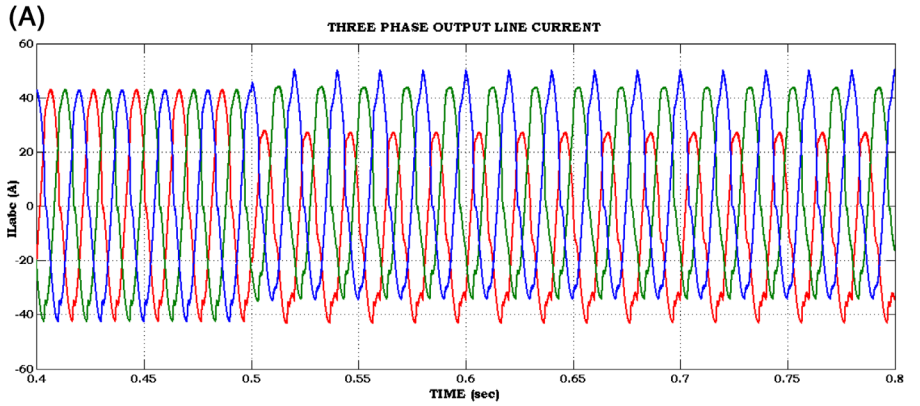
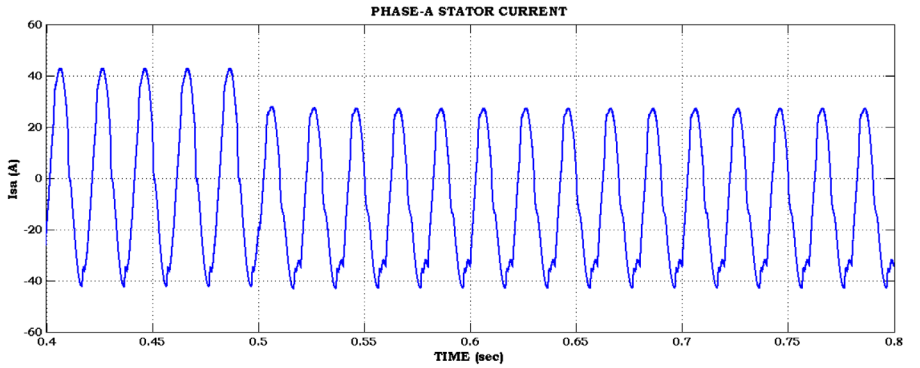


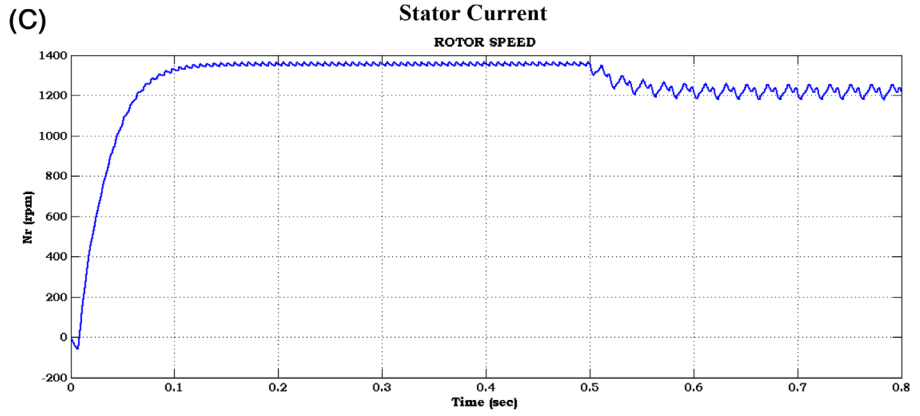
FIGURE 10 Simulation outcomes of three-phase five-level reduced switch symmetric MLI topology fed induction motor drive under IOC faulty condition. A, Three phase line currents. B, Stator current. C, Rotor speed. D, Electromagnetic torque



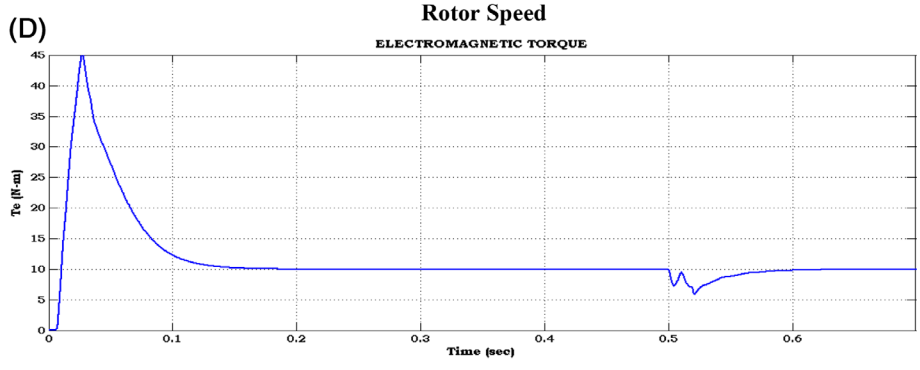
Three Phase Line Currents



Stator Current



Rotor Speed



Electromagnetic Torque

FIGURE 11 Simulation outcomes of three-phase five-level reduced switch symmetric MLI Topology fed induction motor drive under ISC faulty condition. A, Three phase line currents. B, Stator current. C, Rotor speed. D, Electromagnetic torque

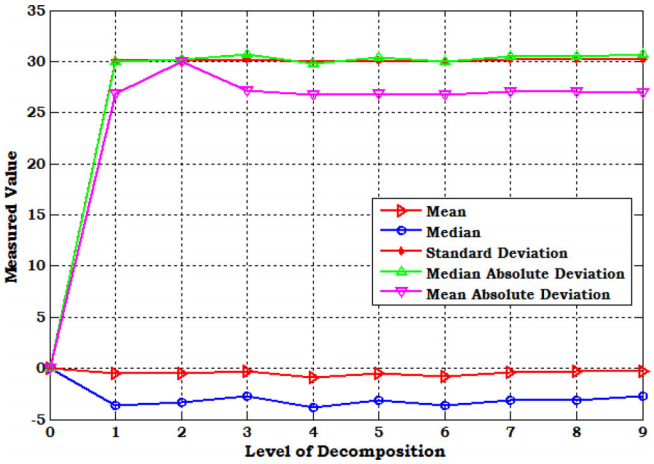


FIGURE 12 Several signatures of line current of MIMD system under healthy condition

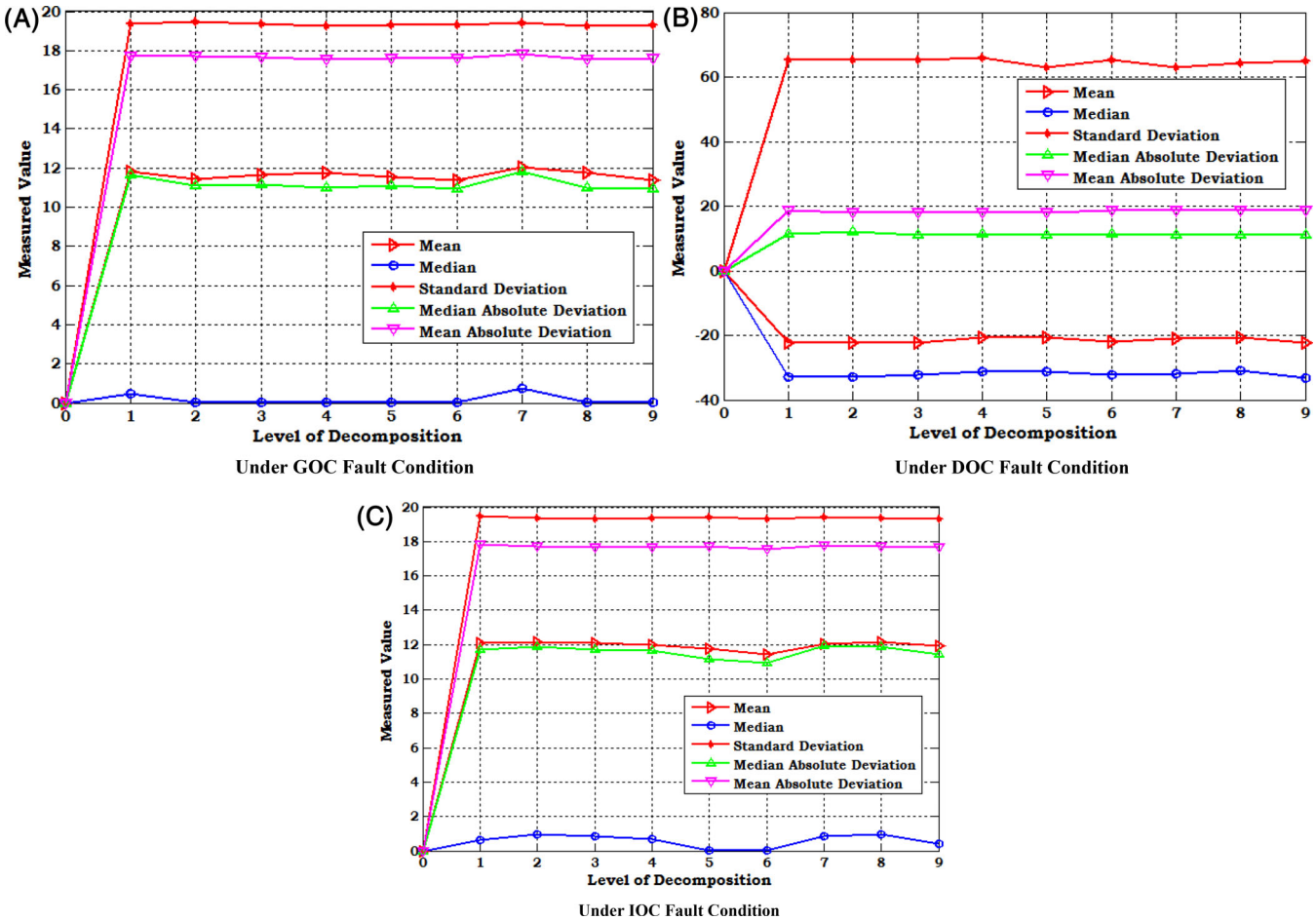


FIGURE 13 Several signatures of line current of MIMD system under OC fault condition. A, Under GOC fault condition. B, Under DOC fault condition. C, Under IOC fault condition

hardware-interaction system. The data is sent back to an excel sheet in a computer-interface and import into a mat-file program. This mat-file program will generate several signatures of respective wave-shape under definite decomposition levels. Several line current signatures of the MIMD system under the healthy condition with definite decomposition levels is represented graphically in Figure 12. The measured mean value is slightly negative as −0.93 is attained at level-d4.

The median is also slightly negative as −3.82 at level-d4. The highest value of standard deviation is attained at level-d3 with a value of 30.18. The highest value of median absolute deviation is attained at level-d3/level-d9 with a value of 30.73; the highest value of mean absolute deviation is attained at level-d2 with a value of 29.96, and the rest of things are monotonically near-constant values. Several line current signatures of the MIMD system under open-circuit fault condition with definite decomposition levels is represented graphically in Figure 13. Figure 13A shows the several signatures under the GOC fault condition; the measured highest mean, median, standard deviations are 12.06, 0.75, 19.43 attained at level-d7. The highest value of the median absolute deviation is 11.82 is attained at level-d7, and the mean absolute is 17.81 reached level-d7; all other things are monotonic near-constant values. Figure 13B shows the several signatures under DOC fault condition, the measured highest mean is in negative slope with a value of −22.41 is attained at level-d8, the median is also slightly negative as −33.13 at level-d8 due to certain spikes inline current, the highest value of standard deviation is attained at level-d4 with a value of 65.92. The highest value of the median absolute deviation is 11.99 is attained at level-d2, and the mean absolute is 18.82 attained at level-d9; all other things are monotonic near-constant values. Figure 13C shows several signatures under the IOC fault condition. The measured highest mean, the median, is attained at level-d2/d7 with 12.16 and 0.96. The highest value of standard deviation is attained at level-d1 with a value of 19.46. The highest value of the median absolute deviation is 11.91, attained at level-d7, and the mean absolute is 17.81 attained at level-d1; all other things are monotonic near-constant values.

Several lines of current MIMD system signatures under short-circuit fault condition with definite decomposition levels are represented graphically in Figure 14. Figure 14A shows the several signatures under the GSC fault condition, the measured highest mean is on a negative slope with a value of −10.96 is attained at level-d6, the median is also slightly negative as −13.81 at level-d6 due to short-circuit fault, the highest value of standard deviation is attained at level-d9 with a value of 24.65. The highest value of the median absolute deviation is 22.08, attained at level-d2, and the mean absolute is 22.13 reached level-d2; all other things are monotonic near-constant values. Figure 14B shows the

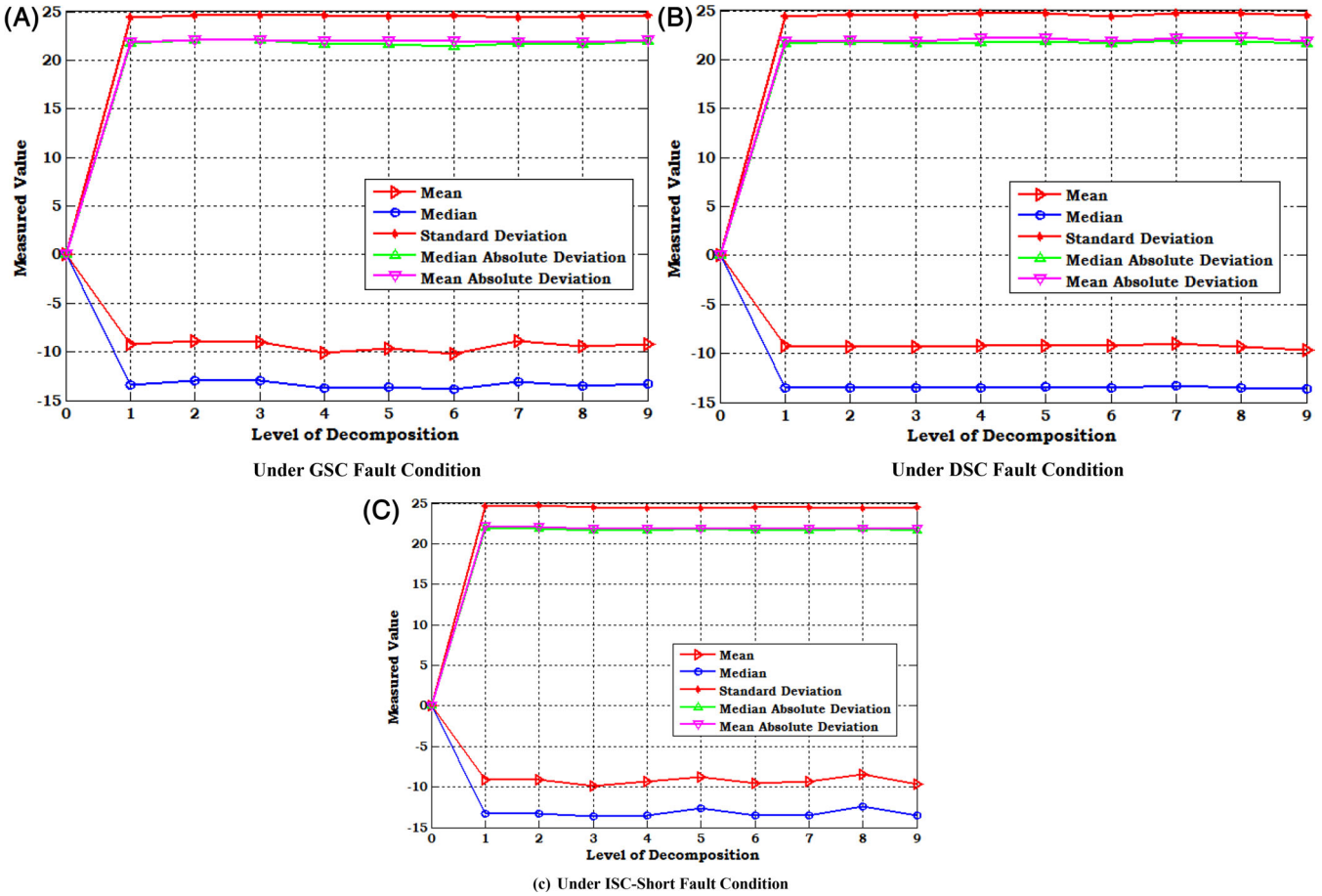


FIGURE 14 Several signatures of line current of MIMD system under S.C. fault condition. A, Under GSC fault condition. B, Under DSC fault condition. C, Under ISC-short fault condition

D_{fr} (%)	Healthy	GOC	DOC	IOC	GSC	DSC	ISC
Line current	63%	66.9%	66.67%	66.76%	66.78%	66.67%	66.8%

TABLE 3 Measured DFR values under healthy and faulty conditions

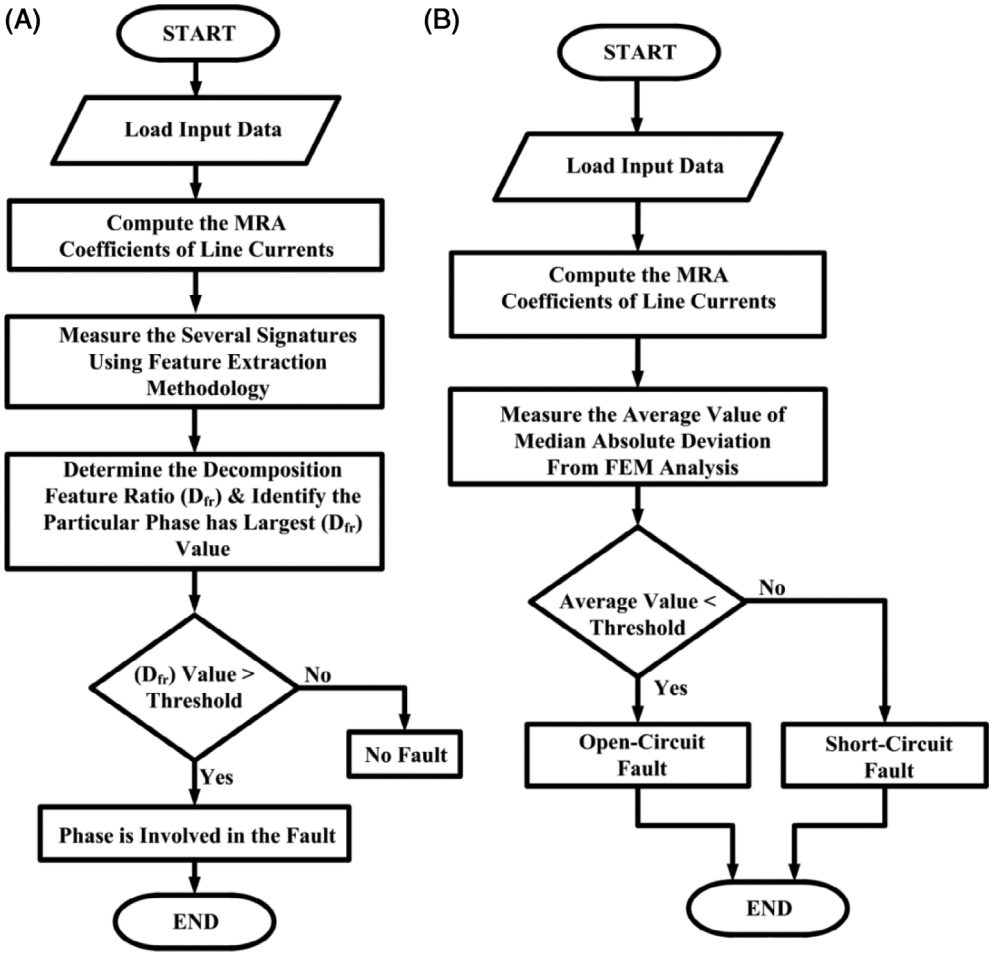


FIGURE 15 Flow chart of fault identification, A, fault occurrence, B, fault type

several signatures under the DSC fault condition; the measured highest mean is in negative slope with a value of −9.68 is attained at level-d9, the median is also slightly negative as −13.63 at level-d9, the highest value of standard deviation is attained at level-d5 with a value of 24.72. The highest value of the median absolute deviation is 21.99, attained at level-d7, and the mean absolute is 23.25 attained at level-d8; all other things are monotonic near-constant values. Figure 14C shows several signatures under ISC fault condition, the measured highest mean is on a negative slope with a value of −9.85 is attained at level-d3, the median is also slightly negative as −13.64 at level-d3, the highest value of standard deviation is attained at level-d2 with a value of 24.69. The highest value of the median absolute deviation is 21.93 is attained at level-d1, and the mean absolute is 22.15 attained at level-d1; all other things are monotonic near-constant values.

The above-measured signatures are valuable for identifying the fault type, but a fault in the MIMD system is determined by decomposition feature rate by differentiating line currents' standard deviation under healthy and faulty conditions refer Equation (12). The DFR values under healthy and faulty conditions are illustrated in Table 3. The values are extensively used to identify the fault with the flow chart's help, as shown in Figure 15. Since the provision to authorize adjustable window-length, DWT is significantly needed for analyzing the faults by using MRA-FEM analysis. Unlike FFT analysis, DWT-FEM can analyze the signal in both times and frequency features and are distinguished in several signatures of data like mean, median, mode, standard deviations, and so on. The DWT is most useful for identifying the fault occurrence in the MIMD system and realizing the non-stationary sequences consisting of high/low-frequency

components. Fault identification can be acquired from various signatures of first decomposition level-d1 of calculated line current signals using Haar wavelet. This level of high-frequency levels is associated with the faults. It can be identified by observing the decomposition feature rate (D_{fr}) of DWT-FEM coefficients under both healthy and faulty conditions. If the D_{fr} value of the line current is greater than the particular threshold value, then the fault occurs in the respective phase. Otherwise, there is no-fault in the respective phase of the MIMD system, as shown in the flowchart in Figure 15A, but the D_{fr} does not classify the type of fault. To illustrate how fault can be classified using DWT-FEM signatures under healthy and different faulty conditions, they are created and obtained the median absolute deviation (M_{ad}) value. The averaging of this (M_{ad}) of every phase and the threshold value classifies the fault type. If the M_{ad} value of line current is less than the certain threshold value, then the fault is classified as an open-circuit fault. Otherwise, there is a short circuit fault in the respective phase of the MIMD system, as shown in Figure 15B. The above-proposed fault identification and recognizing the fault type is very attractive over classical techniques.

6 | HARDWARE RESULTS AND ANALYSIS

For the validation of the proposed RSMLI topology, an experimental setup is established using the dSPACE DS1103 real-time digital controller interfaced with MATLAB/ Simulink models in the host PC shown in Figure 16. In the prototype model, Six Si4850BDY TrenchFET Gen IV power MOSFET are used for implementing the proposed RSMLI

FIGURE 16 Hardware prototype model

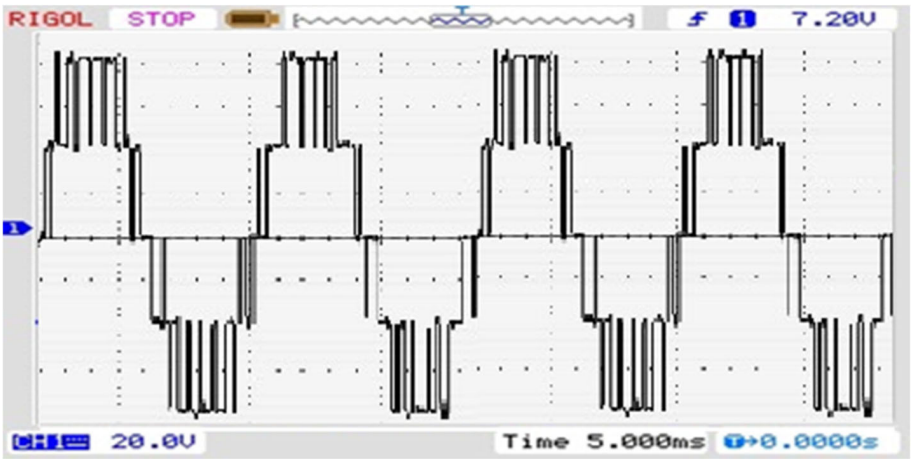


FIGURE 17 Five-level output voltage of proposed symmetrical RSMLI topology under healthy condition

topology fed I.M. drive. This drain-to-source voltage is 80 V, and the gate-to-source voltage is ±20 V with a dissipated power of 4.5 W at 25°C. The low-voltage, high-performance CMOS 8-bit microcomputer with 4 K bytes of flash-programmable memory is used to design the dSPACE DS1103 real-time digital controller power saving option. The dSPACE was used to generate PWM signals and faults.

The hardware prototype results of the proposed five-level symmetrical RSMLI topology output voltages under healthy and faulty conditions are depicted in Figures 17 and 18. For ease of understanding, the results are explained in a single phase. The staircase five-level output voltages are obtained by switching the respective switches in the proposed RSMLI topology controlled by a simplified fundamental frequency-based voltage pulse method. To investigate the faulty condition in the proposed RSMLI, an open-switch fault is introduced to switch S_{a5} by misfiring its gate driver. The established fault on S_{a5} results in missing on the voltage. To be more specific, when the fault was created in S_{a5}, the highest voltage level is missed as shown in Figure 18. Output current of proposed RSMLI under healthy condition is depicted in Figure 19A. A short-circuit fault is introduced for the switch S_{a5} by misfiring of its gate pulse. Due to this short-circuit fault on the gate-pulse generation, the switch S_{a5} is treated as a malfunction of the gate-pulse and the line current is decreased as shown in Figure 19B. The rotor speed and electromagnetic torque of the induction motor under healthy conditions and faulty conditions are shown in Figures 20A and 21A, respectively. When the fault is initiated, the rotor speed and electromagnetic torque fluctuate, as displayed in Figures 20B and 21B, respectively.

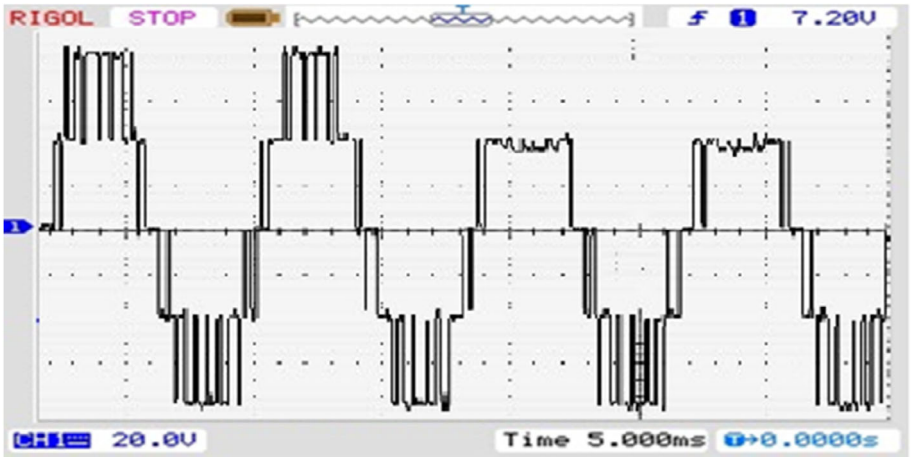


FIGURE 18 Five-level output voltage of proposed symmetrical RSMLI topology under the faulty condition

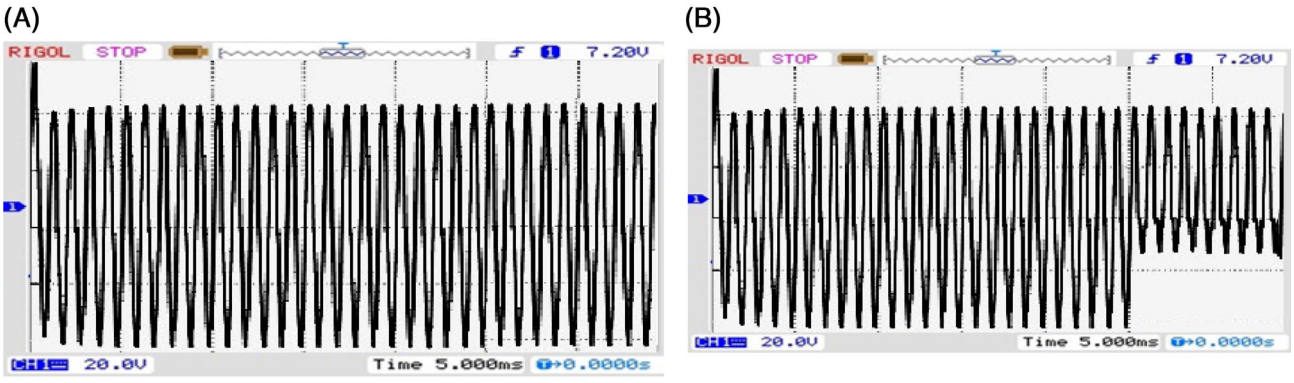


FIGURE 19 Five-level output current of proposed symmetrical RSMLI topology under the healthy and faulty condition. A, Healthy condition. B, Faulty condition

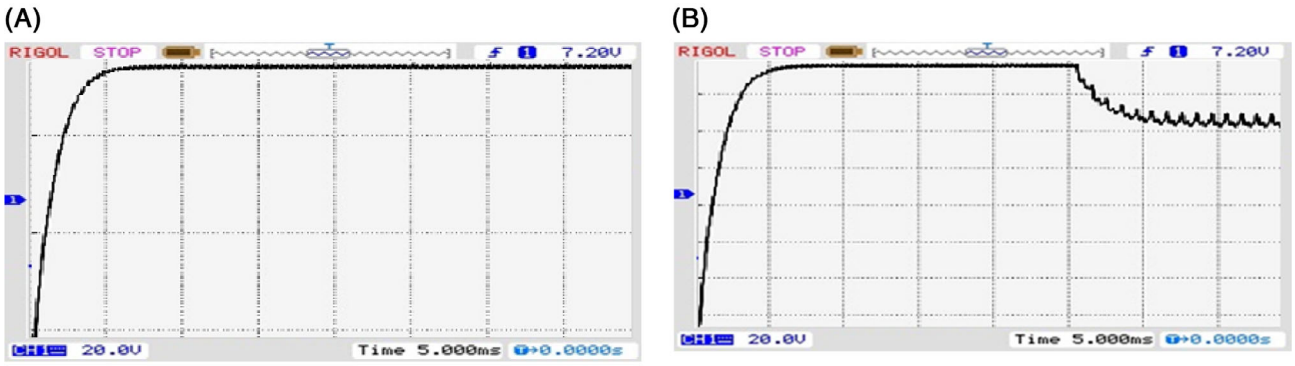


FIGURE 20 Rotor speed of induction motor under. A, Healthy condition. B, Faulty condition

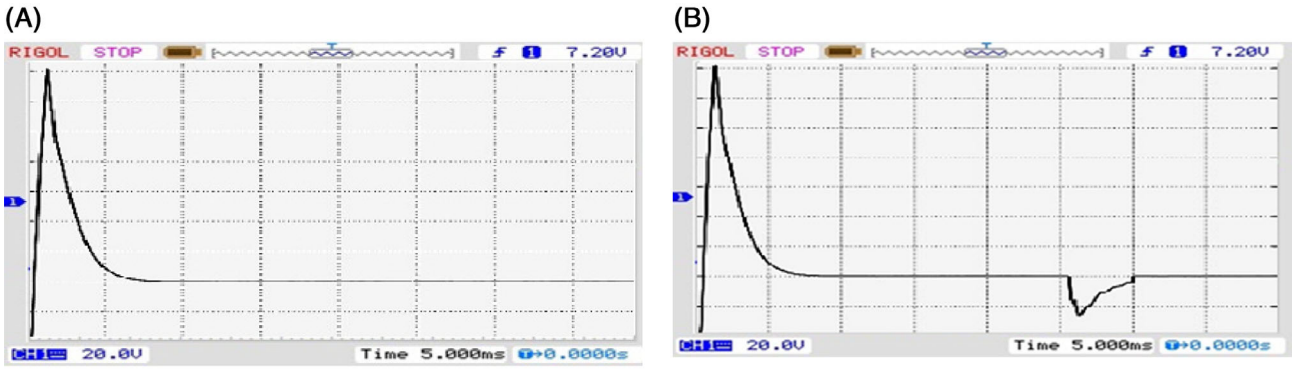


FIGURE 21 Electromagnetic torque of induction motor under the healthy and faulty condition. A, Healthy condition. B, Faulty condition

7 | CONCLUSION

The proposed novel symmetric five-level MLI topology requires fewer switching elements and low minimized carrier signal generation, which is more feasible in adjustable speed drive applications. Faults commonly occur in MIMD systems. An efficient fault detection method has been implemented to diagnose faults, which minimizes the production loss, drives failure, and increases the drive system's reliability. The proposed DWT-MRA technique provides accurate results for analyzing the MIMD system under several fault conditions over the classical fault identification methods. The proposed DWT-MRA decomposes the signal in both time and frequency features as various decomposition levels for analyzing the current trajectory's fault. This technique furnishes a good description of faults under several signatures using FEM analysis, which classifies the fault type. These extracted signatures are utilized to calculate the DFR value to detect fault appearance in the MIMD system under both healthy and faulty conditions. The detailed simulation analysis of the proposed MIMD system is verified under healthy and faulty conditions. Using proposed DWT-FEM with the help of a computer simulation tool and results is illustrated with proper comparisons. The hardware model is also implemented for the proposed-topology, and results are also displayed. The workflow of fault detection and fault identification is represented in the flowchart by analyzing the faults in definite signatures. In further recommendations, a fault-tolerant scheme is to be proposed by adopting novel fault compensation schemes with proposed DWT-FEM analysis.

ACKNOWLEDGMENTS

This project is supported by Universiti Malaysia Pahang (UMP) (Grant No: PGRS200321) and Mr. A. S. Veerendra is working under UMP's Doctoral Research Scheme (DRS) and was partially supported by the National Key Research and Development Program of China (Grant No. 2017YFB0701700).

CONFLICT OF INTEREST

No potential conflict of interest was reported by the authors.

PEER REVIEW

The peer review history for this article is available at https://publons.com/publon/10.1002/2050-7038.12820.

DATA AVAILABILITY STATEMENT

Data sharing not applicable to this article as no datasets were generated or analysed during the current study.

ORCID

Arigela Satya Veerendra https://orcid.org/0000-0001-5296-1936
Mohd Rusllim Mohamed https://orcid.org/0000-0002-9194-0553

REFERENCES

1. Ge BM, Peng FZ, de Almeida AT, Abu-Rub H. An effective control technique for medium-voltage high-power induction motor fed by cascaded neutral-point-clamped inverter. *IEEE Trans Ind Electron*. 2010;57(8):2659-2668. https://doi.org/10.1109/tie.2009.2026761.
2. Mahato B, Raushan R, Jana KC. Modulation and control of multilevel inverter for an open-end winding induction motor with constant voltage levels and harmonics. *IET Power Electron*. 2017;10(1):71-79. https://doi.org/10.1049/iet-pel.2016.0105.
3. Sankala A, Korhonen J, Ström JP, et al. Modular double-cascade converter for high-power medium-voltage drives. *IET Power Electron*. 2015;8(9):1661-1669. https://doi.org/10.1049/iet-pel.2014.0341.
4. Kouro S, Malinowski M, Gopakumar K, et al. Recent advances and industrial applications of multilevel converters. *IEEE Trans Ind Electron*. 2010;57(8):2553-2580. https://doi.org/10.1109/tie.2010.2049719.
5. Rodriguez J, Bernet S, Steimer PK, Lizama IE. A survey on neutral-point-clamped inverters. *IEEE Trans Ind Electron*. 2010;57(7):2219-2230. https://doi.org/10.1109/tie.2009.2032430.
6. Abdullah R, Abd Rahim N, Raihan SRS, Ahmad A. Five-level diode-clamped inverter with three-level boost converter. *IEEE Trans Ind Electron*. 2014;61(10):5155-5163. https://doi.org/10.1109/tie.2013.2297315.
7. Villanueva E, Correa P, Rodriguez J, Pacas M. Control of a single-phase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems. *IEEE Trans Ind Electron*. 2009;56(11):4399-4406. https://doi.org/10.1109/tie.2009.2029579.
8. Veerendra AS, Mohamed MR, Sulaiman MH, Sudhakar K, Peddakapu K. Modelling and simulation of dual sourced front-end converter for hybrid electric vehicles. *Int J Ambient Energy*. 2020. https://doi.org/10.1080/01430750.2020.1712245.
9. Rodriguez J, Pontt J, Musalem R, Hammond P. Operation of a medium-voltage drive under faulty conditions (IPEMC 2004: the 4th International Power Electronics and Motion Control Conference, Vols 1–3, Conference Proceedings). 2004:799-803.
10. D'Aversa A, Hughes B, Patel S. Challenges and solutions of protecting variable speed drive motors. In 66th Annual Conference on Protective Relay Engineers, College Station, TX, Apr 08-11 2013, in Annual Conference for Protective Relay Engineers; 2013:250-256.
11. Ali AIM, Sayed MA, Mohame EEM, Azmy AM. "advanced single-phase nine-level converter for the integration of multiterminal DC supplies," (in English). *IEEE J Emerg Select Top Power Electron*. 2019;7(3):1949-1958. https://doi.org/10.1109/jestpe.2018.2868734.
12. Lezana P, Pou J, Meynard TA, Rodriguez J, Ceballos S, Richardeau F. Survey on fault operation on multilevel inverters. *IEEE Trans Ind Electron*. 2010;57(7):2207-2218. https://doi.org/10.1109/tie.2009.2032194.
13. Priya YK, Kumar MV. Analysis of various switch faults of the Three Level Neutral Point Clamped Inverter Feeding Induction Motor Drive. Proceedings of the 2016 IEEE 2nd International Conference on Advances in Electrical & Electronics, Information, Communication & Bio Informatics (IEEE Aeeicb-2016). 2016:580-586.
14. Trabelsi M, Boussak M, Gossa M. Multiple IGBTs open circuit faults diagnosis in voltage source inverter fed induction motor using modified slope method. In The XIX International Conference on Electrical Machines-ICEM 2010: IEEE; 2010:1-6.
15. Estima JO, Marques Cardoso AJ. A new algorithm for real-time multiple open-circuit fault diagnosis in voltage-fed PWM motor drives by the reference current errors. *IEEE Trans Ind Electron*. 2013;60(8):3496-3505. https://doi.org/10.1109/tie.2012.2188877.
16. de Jesus Romero-Troncoso R. Multirate signal processing to improve FFT-based analysis for detecting faults in induction motors. *IEEE Tran Ind Inform*. 2017;13(3):1291-1300. https://doi.org/10.1109/tii.2016.2603968.
17. Moussa MA, Boucherma M, Khezzar A. A detection method for induction motor Bar fault using Sidelobes leakage phenomenon of the sliding discrete Fourier transform. *IEEE Trans Power Electron*. 2017;32(7):5560-5572. https://doi.org/10.1109/tpel.2016.2605821.
18. Bouzida A, Touhami O, Ibtiouen R, Belouchrani A, Fadel M, Rezzoug A. Fault diagnosis in industrial induction machines through discrete wavelet transform. *IEEE Trans Ind Electron*. 2011;58(9):4385-4395. https://doi.org/10.1109/tie.2010.2095391.
19. McGrath BP, Holmes DG. Multicarrier PWM strategies for multilevel inverters. *IEEE Trans Ind Electron*. 2002;49(4):858-867. https://doi.org/10.1109/tie.2002.801073.
20. Naderi R, Rahmati A. Phase-shifted carrier PWM technique for general cascaded inverters. *IEEE Trans Power Electron*. 2008;23(3):1257-1269. https://doi.org/10.1109/tpel.2008.921186.
21. Sreenivasarao D, Agarwal P, Das B. Performance evaluation of carrier rotation strategy in level-shifted pulse-width modulation technique. *IET Power Electron*. 2014;7(3):667-680. https://doi.org/10.1049/iet-pel.2013.0109.

22. Ahmed I, Borghate VB. Simplified space vector modulation technique for seven-level cascaded H-bridge inverter. *IET Power Electron*. 2014;7(3):604-613. https://doi.org/10.1049/iet-pel.2013.0135.
23. Aktas M, Turkmenoglu V. Wavelet-based switching faults detection in direct torque control induction motor drives. *IET Sci Measure Technol*. 2010;4(6):303-310. https://doi.org/10.1049/iet-smt.2009.0121.
24. Bialasiewicz JT, Gonzalez D, Balcells J, Gago J. Wavelet-based approach to evaluation of signal integrity. *IEEE Trans Ind Electron*. 2013; 60(10):4590-4598. https://doi.org/10.1109/tie.2012.2217713.
25. Keswani RA, Suryawanshi HM, Ballal MS. Multi-resolution analysis for converter switch faults identification. *IET Power Electron*. 2015; 8(5):783-792. https://doi.org/10.1049/iet-pel.2014.0450.
26. Ananthan SN, Padmanabhan R, Meyur R, Mallikarjuna B, Reddy MJB, Mohanta DK. Real-time fault analysis of transmission lines using wavelet multi-resolution analysis based frequency-domain approach. *IET Sci Measure Technol*. 2016;10(7):693-703. https://doi.org/10.1049/iet-smt.2016.0038.
27. Jung S-M, Park J-S, Kim H-W, Cho K-Y, Youn M-J. An MRAS-based diagnosis of open-circuit fault in PWM voltage-source inverters for PM synchronous motor drive systems. *IEEE Trans Power Electron*. 2013;28(5):2514-2526. https://doi.org/10.1109/tpel.2012.2212916.

How to cite this article: Veerendra AS, Mohamed MR, Punya Sekhar C. A novel fault-detection methodology of proposed reduced switch MLI fed induction motor drive using discrete wavelet transforms. *Int Trans Electr Energ Syst*. 2021;e12820. https://doi.org/10.1002/2050-7038.12820