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JUDUL: **SINGLE PHASE MOTOR SPEED CONTROL USING
SPWM INVERTER**

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SINGLE PHASE MOTOR SPEED CONTROL
USING SPWM INVERTER

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This thesis is submitted as partial fulfillment of the requirements for the award of the
Bachelor of Electrical Engineering (Hons.) (Power System)

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NOVEMBER 2008

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Date : 17 NOVEMBER 2008

*Dedicated to my beloved mother, brothers, grandmother, and
Sisters-in-laws*

Che Esah Bt Musa

Thanks for the love and supports

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ABSTRACT

An inverter circuit by using Sinusoidal Pulse Width Modulation (SPWM) switching schemes is developed to control the speed of single-phase AC motor and being verified experimentally. Inverters are circuit that convert a DC source to an AC source. DC is one type of energy found in batteries and AC is a type of energy that is produced by the power company and found in electrical homes/offices appliances. The application of this AC motor controller is to provide single-phase ac induction motor less than $\frac{1}{2}$ hp (372.85 W). Semiconductor device, Metal Oxide Field Effect Transistor (MOSFET) is used as switch in the full bridge (H-bridge) inverter configuration with unipolar voltage switching. A variable frequency output waveform is produced by the inverter to run a motor at variable speeds that are directly proportional to this frequency. Besides the MOSFETs as the inverter, driver for the MOSFET also very important in this circuit development because it is use to interface between control circuits (low voltage part) and inverter (high voltage part). Another important part in this inverter design is PICmicro microcontroller chip that is used to provide the switching schemes to the MOSFETs. This microchip acts as a controller circuit that produces the carrier signal and modulating signal for the inverter. The objective of this project is to build an ac motor speeds controller for holiday usage appliances, to simulate and analyze the single-phase SPWM operation of the inverter switching characteristics. The Programmable Interface Computer PIC used is PIC 18F4550 and the MOSFET driver used is IR2110. At the end of this project, the SPWM output is developed from the controller circuit and applied to the driver circuit and the inverter, and hence can be used to control the speed of the AC motor.

ABSTRAK

Litar penyongsang dengan menggunakan teknik pemodulatan lebar denyut sinus (SPWM), aturan pensuisan dibina untuk mengawal kelajuan AC fasa tunggal motor dan dibuktikan secara ujikaji. Litar pengongsang adalah litar yang menukarkan sumber arus terus (DC) kepada sumber arus ulang-alik (AC). DC adalah salah satu tenaga yang boleh dijumpai di dalam bateri (dihasilkan oleh bateri) dan AC pula adalah sumber tenaga yang dihasilkan oleh syarikat pembekalan kuasa dan digunakan oleh alatan elektrik rumah ataupun pejabat. Aplikasi pengawal AC motor ini adalah untuk menyediakan ac motor teraruh fasa tunggal kurang daripada $\frac{1}{2}$ hp (372.85 W). Alat separa pengalir, Metal Oxide Field Effect Transistor (MOSFET) digunakan sebagai suis di dalam topologi litar penyongsang tetimbang penuh (full-bridge/ H-bridge) dengan pensuisan unipolar. Gelombang keluaran dengan frekuensi yang berlainan dihasilkan oleh penyongsang untuk menggerakkan motor dengan kelajuan yang berkadar terus dengan frekuensi tersebut. Selain daripada MOSFET yang bertindak sebagai, pemacu MOSFET juga sangat penting dalam pembangunan litar ini kerana ia digunakan sebagai perantaraan antara litar pengawal (voltan rendah) dan penyongsang (voltan tinggi). Suatu lagi bahagian penting di dalam rekaan penyongsang ini adalah mikroPIC, mikropengawal yang digunakan untuk menghasilkan aturan pensuisan kepada MOSFET. Cip mikro ini bertindak sebagai litar pengawal yang menghasilkan isyarat pembawa dan isyarat pemodulat kepada penyongsang. Objektif projek ini adalah untuk merekabentuk litar, mensimulasi dan menganalisa sifat pensuisan penyongsang bagi operasi SPWM fasa tunggal. Programmable Interface Computer (PIC) mikropengawal yang digunakan adalah PIC 18F4450 dan pemacu MOSFET pula adalah IR2110. Pada akhir projek ini, keluaran SPWM telah berjaya dikeluarkan dari PIC mikropengawal dan diaplikasikan kepada litar pengawal dan penyongsang yang boleh digunakan untuk mengawal kelajuan motor AC.

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

This chapter will mainly discuss about type of inverters and the basic operation and also the advantages of the SPWM inverter compares to other type of inverter. The objectives, scopes and thesis outline also presented in this chapter.

1.2 OVERVIEW OF THE PROJECT

Inverters are circuits that convert DC to AC. It transfers power from DC source to AC load. The mainly purpose of designing the inverter is to create an AC voltage when only a DC voltage source is available. There are many types of inverters, such as half wave inverter and full wave inverter and they are also can be designed to be single-phase full-bridge (H-bridge) inverter, two-phase inverter and

three-phase inverter. The switching schemes that can be produce from full wave inverter are square wave (SW), quasi-square wave (QWS)/modified sine wave and pulse width modulation technique.

The proposed of this project is how to develop a sinusoidal pulse width modulation inverter to control the speed of single phase motor. Square wave inverter has a high harmonic output, which can lead the equipment component to overheat, so no longer relevant for modern use. The modified square wave inverter is designed to have better characteristics than square wave inverter, but it is still cannot give a perfect electrical as pure sine wave. Pulse width modulation (PWM) provides a way to decrease the total harmonic distortion (THD) of load current.

In PWM, the amplitude of the output voltage can be controlled width the modulating waveforms. Reduced filter requirements to decrease harmonics and the control of the output voltage amplitude are two distinct advantages of PWM. The SPWM inverter is the generation of PWM outputs with sine wave as the modulating signal and triangular wave as carrier signal. The on and off occurrence are determined by comparing sinusoidal (modulating) wave with triangular (carrier) wave. The sine waves determine the frequency of the output waveform while the carrier signal determine the switching frequency of the MOSFET.

SPWM technique with filter can produce true sine wave output; hence make it compatible with all AC equipments including the sensitive equipments.

1.3 OBJECTIVES OF THE PROJECT

The objectives of this project are :

- i. Develop SPWM Inverter for single phase ac motor application that generates 240Vrms, 50Hz and ½ hp.
- ii. Develop an open loop system by using PIC microcontroller to produce SPWM pulse to control speed of motor.
- iii. Design circuit, simulate and analyze the switching characteristics of sinusoidal pulse width modulated inverter.

1.4 SCOPES OF THE PROJECT

The scopes of the projects are;

- i. To design SPWM inverter to control the speed of single phase motor.
- ii. PIC microcontroller is used to control the switching process.
- iii. ORCAD Pspice program is used to design and simulate the SPWM inverter circuit.

1.5 THESIS OUTLINE

Chapter 1 explains the operation of an inverter and advantages of SPWM method. The overview of project objectives and project scopes also discuss in this chapter.

Chapter 2 focuses on the literature review that related to this project. The inverter design, driver circuit, theory and also the calculation which is involved in the design and the PIC microcontroller are explain more detail

Chapter 3 discusses about methodology of this project. This chapter also discuss about overall circuit design and the system work. The software used and the source codes of how to generate SPWM from PIC is explained.

Chapter 4 explains and discusses all the results obtained and the analysis of the overall project. The comparisons of Pspice simulation's results and hardware results are explain more detail.

Chapter 5 discusses the conclusion of the SPWM method that is implemented into the project. This chapter also gives the recommendation about the future development of the inverter projects by making some additional featured to the circuit and the software coding.

CHAPTER 2

THEORY AND LITERATURE REVIEW

2.1 AC Motor and Loads

An inverter is an electronic device which inverts DC energy (the type of energy found in batteries) into AC energy. Household appliances such as refrigerators, TVs , lighting, stereos, computer etc., all run off of AC electricity [?]. An AC motor is an electric motor that is driven by an alternating current. The motor is connected to the mains through an AC switch. The AC voltage varies across the motor in phase control mode by means of a microcontroller, which sets the triggering time. The application example of AC motor load is vacuum cleaner, washing machines power tools and food processors.

Besides that, small single-phase AC motors are usually used to power mechanical clocks, audio turntables, and tape drives; formerly they were also much used in accurate timing instruments such as strip-chart recorders or telescope drive mechanisms [a].

2.2 Inverters

There are many type of inverters have been developed. But the most common inverters and are square wave inverter, modified square wave inverter and pure sine wave inverter.

Mobility and versatility have become a must for the fast-paced society today. People can no longer afford to be tied down to a fixed power source location when using their equipments. Overcoming the obstacle of fixed power has led to the invention of DC/AC power inverters. While the position of power inverter in the market is relatively well established, there are several features that can be improved upon.

A comparison analysis of the different power inverter has been compiled. Aside from the differences in power wattage, cost per wattage, efficiency and harmonic contend, power inverters can be categorized into three groups: square wave, modified sine wave, and pure sine wave.

2.2.1 Square Wave Inverter

Power inverters of first designed are inverters using a square wave as the output form. This led to many different problems involving the functionality of devices that were being powered because they were designed to work with a sine wave instead of a square wave. These old-fashioned inverters are the cheapest to make, but the hardest to use. They just flip the voltage from plus to minus creating a square waveform. They are not very efficient

because the square wave has a lot of power in higher harmonics that cannot be used by many appliances.

2.2.2 Modified Square Wave Inverter

The modified sine wave is designed to minimize the power in the harmonics while still being cheap to make. There were some changes made to the hardware to eliminate the harsh corners from the square wave to transform it to a “modified sine wave”. Modified square wave can have detrimental effects on electrical loads. First of all, abnormal heat will be produced, causing a reduction in product reliability, efficiency, and useful life. Another disadvantage of a “modified sine wave” is that its choppy waveform can confuse the operation of some digital timing devices. This can cause a device to perform undesirable or abnormal functions. Also, nearly 5 % of household electronics will not even work with a modified sine wave.

Appliances that are known to have problems with the modified sine wave are some digital clocks, some battery chargers, light dimmers, some battery operated gadgets that recharge in an AC receptacle, some chargers for hand tools (Makita is known to have this problem). In the case of hand tools, the problem chargers usually have a warning label stating that dangerous voltages are present at the battery terminals when charging.

2.2.3 Pure Sine Wave Inverter

A pure sine wave inverter produces power that is exactly like the power which is produced by the utility company without the spikes and brownout of course. This type of inverter produces pure sine waves at the cost of some efficiency loss and at a much higher price compares to modified sine wave inverter. In fact, most pure sine wave inverters are typically priced at least 75% higher than their modified sine wave counterparts [2].

Modulation techniques are used in inverter to regulate output voltage/current. The type of pulse width modulation technique used decides the switching losses in the inverter, harmonic contents in output waveform, and overall performance of the inverter. Sine wave pulse width modulation (SPWM) is most widely used scheme due to its simplicity and better output profile.

Pulse width modulation (PWM) is a powerful technique for controlling analog circuits with a microprocessor's digital outputs. PWM is employed in a wide variety of applications, ranging from measurement and communications to power control and conversion [2].

Control of the switches for sinusoidal PWM requires (1) a reference signal, sometimes called a modulating or control signal, which is a sinusoid in this case; and (2) a carrier signal, which is a triangular wave that controls the switching frequency [1].

In Sinusoidal Pulse Width Modulation, SPWM, multiple pulses are generated, each having different width time. The width of each pulse is varied in proportion to the

instantaneous integrated value of the required fundamental component at the time of its event. In other words, the pulse width becomes a sinusoidal function of the angular position. The repetition frequency of the output voltage will be a frequency higher than the fundamental. In applying SPWM, the lower order harmonics of the modulated voltage wave are highly reduced in contrast to the use of uniform pulse width modulation [5].

2.2.3.1 SPWM Inverter – Bipolar Switching

The graph below shows the harmonic distortion that occurs by using bipolar PWM switching. Bipolar PWM output contains either +V or -V always. Because the transition switching involving peak to peak value, hence switching harmonic content in this scheme is more. In addition, the switching harmonic content is the highest when the PWM is trying to generate zero volt output after the averaging filter. It is difficult to synthesise good 'zero crossings' in a bipolar scheme unless heavy filtering (with consequent degradation in response time) is used.

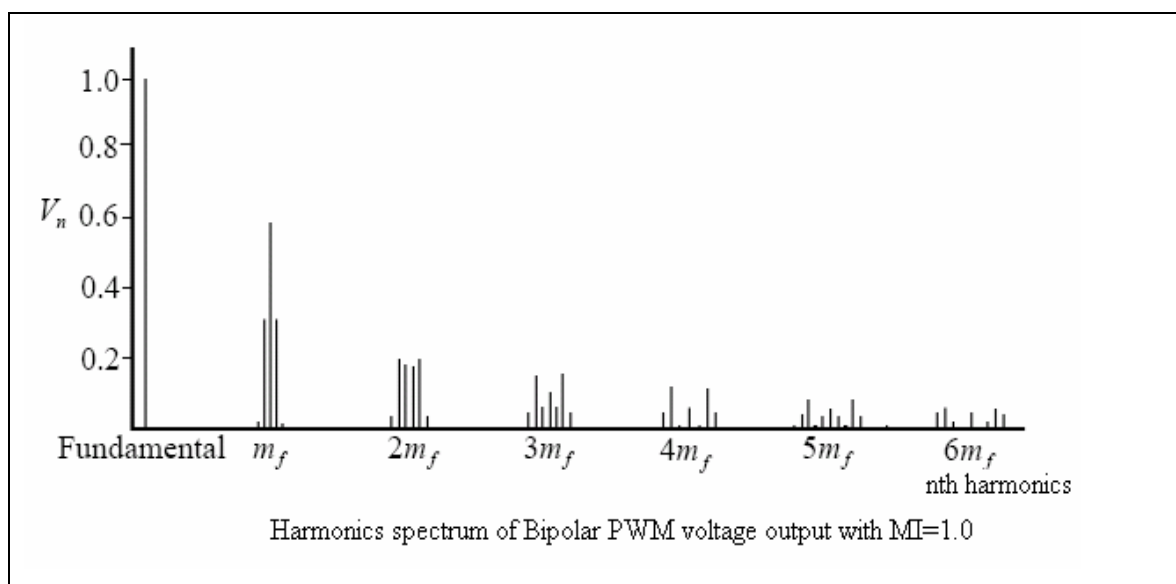


Figure 2.1 : Harmonics Spectrum of Bipolar SPWM

2.2.3.2 SPWM Inverter – Unipolar Switching

The graph below shows the harmonic distortion that occurs with using unipolar PWM switching. Unipolar PWM uses +V and zero to make positive outputs and -V and 0 to make negative outputs. Switching Harmonic Content in this case will be small and will be zero at zero crossings

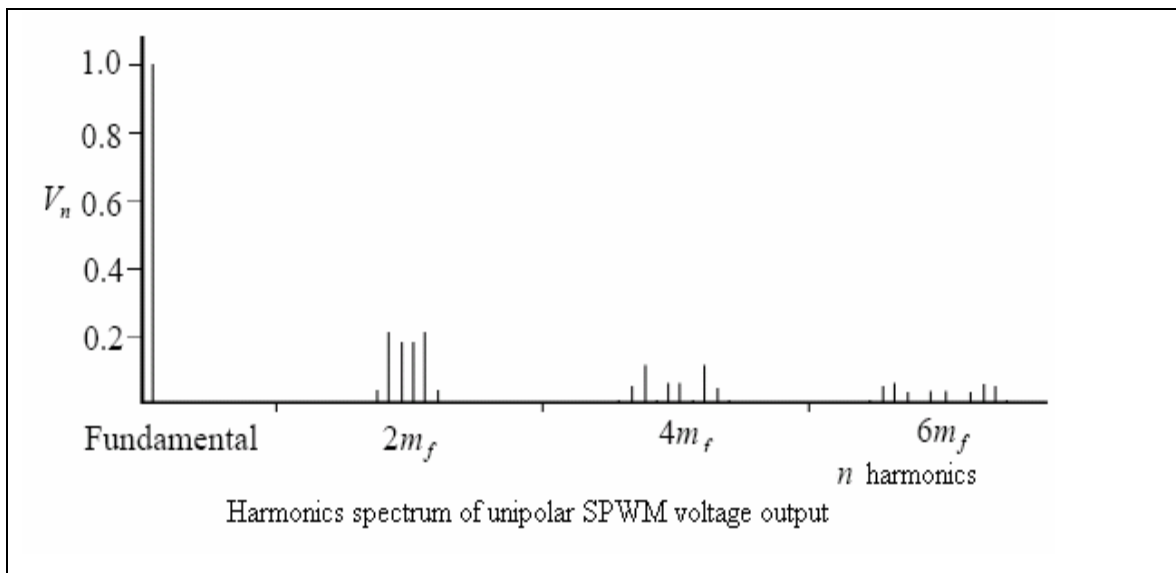


Figure 2.2 : Harmonics Spectrum of Unipolar SPWM

By comparing to the both harmonics spectrum of the switchings, it is best to apply the unipolar switching where the lower the THD current the better the output waveform.

2.3 PIC Microcontroller

A microcontroller is a single chip computer. *Micro* suggests that the device is small, and *controller* suggests that the device can be used in control applications. Another term used for microcontroller is *embedded controller*, since most of the microcontrollers are built into (or embedded in) the devices they control [6].

Microcontroller is general purpose microprocessor which has additional parts that allow them to control external devices. Basically, a microcontroller executes a user program which is loaded in its program memory. [6]

The reason for using microcontroller is general purpose microprocessor which has additional parts that allow them to control external devices. Basically, a microcontroller executes a user program which is loaded in its program memory.

Instead of using the microcontroller, PIC type of microcontroller architecture is distinctively minimalist. PIC microcontroller is the name for the microchip microcontroller (MCU) family, consisting of a microprocessor, I/O ports, timer (s) and other internal, integrated hardware. [6] It is characterized by the following features:

- (i) Separate code and data spaces.
- (ii) A small number of fixed length instructions.
- (iii) Most instructions are single cycle execution (4 clock cycles), with single delay cycles upon branches and skips.
- (iv) A single accumulator (W), the use of which (as source operand) is implied

- (v) All RAM locations function as registers as both source and/or destination of math and other functions.
- (vi) A hardware stack for storing return addresses.
- (vii) A fairly small amount of addressable data space (typically 256 bytes), extended through banking.
- (viii) Data space mapped CPU, port, and peripheral registers.
- (ix) The program counter is also mapped into the data space and writable (this is used to synthesize indirect jumps).

PIC is a family of Harvard architecture microcontrollers made by Microchip Technology, derived from the PIC1640 originally developed by General Instrument's Microelectronics Division. The name PIC initially referred to "**Programmable Interface Controller**", but shortly thereafter was renamed "**Programmable Intelligent Computer**" [7].

The PICs architecture has no (or very meager) hardware support for saving processor state when servicing interrupts. The 18 series improved this situation by implementing shadow registers which save several important registers during an interrupt. The PICs architecture may be criticized on a few important points:

- (i) The few instructions, limited addressing modes, code obfuscations due to the "skip" instruction and accumulator register passing makes it difficult to program in assembly language, and resulting code difficult to comprehend. This drawback has been alleviated by the increasing availability of high level language compilers.

- (ii) Data stored in program memory is space inefficient and/or time consuming to access, as it is not directly addressable.

2.3.1 PIC18F4550

Figure below shows the pin configuration of PIC18F4550. there were 40 pins with variable input /output configuration.

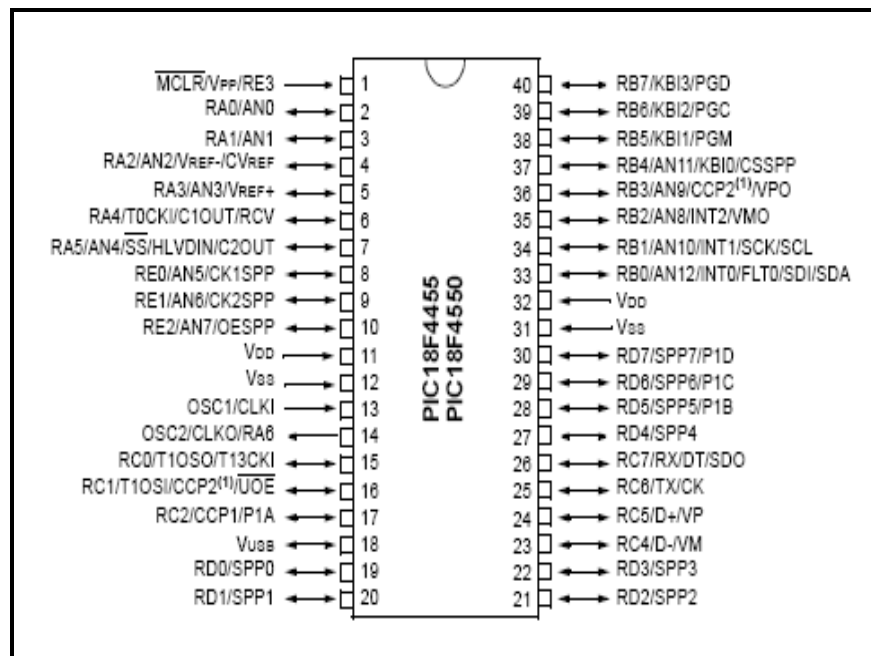


Figure 2.3 : PIC 18F4550 Pins Configuration

2.3.2 PIC18F4550 Peripherals

Table 2.1 shows some of its important parameters and features.

Table 2.1 : PIC 18F4550 features

Parameter Name	Value
Program Memory Type	Flash
Program Memory Size (Kbytes)	32
RAM	2,048
Data EEPROM (bytes)	256
I/O	35
Features	
Full Speed USB 2.0 (12Mbit/s) interface	
☐ 1K byte Dual Port RAM + 1K byte GP RAM ☐ Full Speed Transceiver ☐ 16 Endpoints (IN/OUT) ☐ Streaming Port ☐ Internal Pull Up resistors (D+/D-) ☐ 48 MHz performance (12 MIPS) ☐ Pin-to-pin compatible with PIC16C7X5	

2.4 Half_Bridge Inverter Topology

The half-bridge converter of Figure 2.4 can be used as an inverter. The number of switches is reduced to two by dividing the dc source voltage into two parts with the capacitors. Each capacitor will be the same value and will have voltage $V_{dc}/2$ across it. When s_1 is closed, the load voltage is $-V_{dc}/2$. when s_2 is closed, the load voltage is $+V_{dc}/2$. Thus, a square wave output or a bipolar pulse width modulated output can be produced [1].

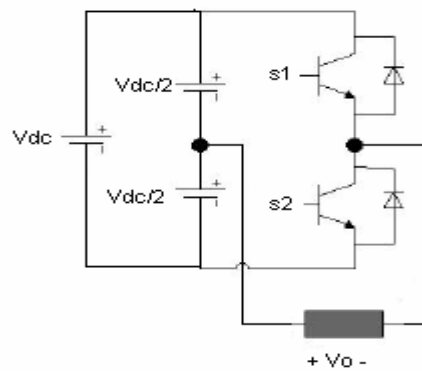


Figure 2.4 : Half-Bridge Inverter Circuit

2.5 Full Bridge Inverter Topology

Full bridge inverter is given the best topology to design a single-phase power inverter. By using power transistor such as IGBT or MOSFET it can give better output voltage than half bridge inverter. Figure 2.3 shows how the connection of full-bridge is made by using power transistor and PIC as a digital controller circuit.

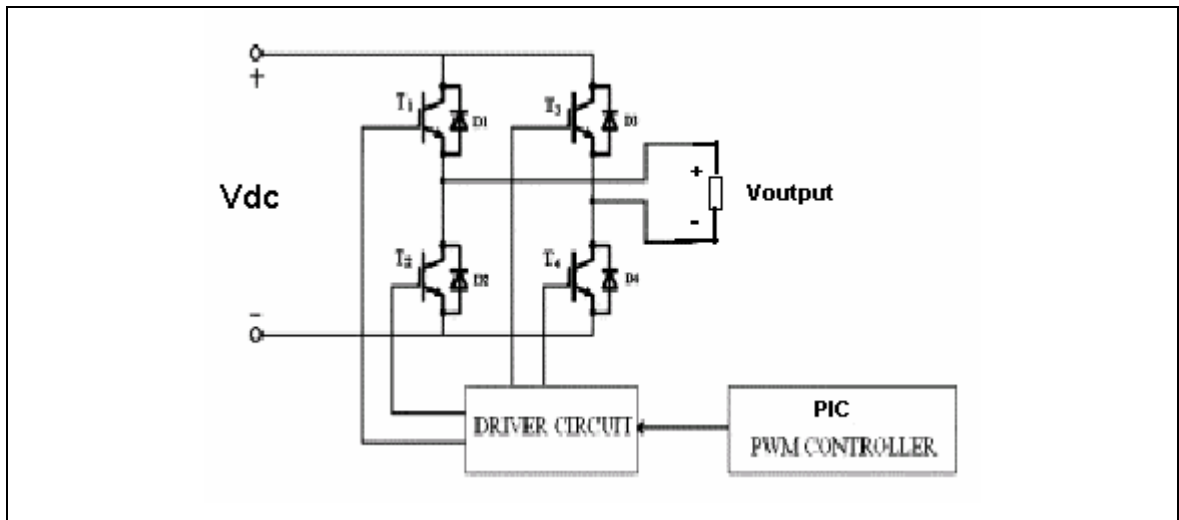


Figure 2.5 : Full Bridge Inverter Circuit

The circuit shows the full-bridge inverter with switches implemented as bipolar junction transistors with feedback diodes. Power semiconductor modules usually include feedback diodes with the switches [1].

CHAPTER 3

METHODOLOGY

3.1 Overview

This chapter explains how the software and hardware of this project is developed using the right procedures. Basically the hardware tools developed in this project not have many different from the previous project except for the part of PIC microcontroller circuit where the addition of analog controller has been made and the type of PIC itself has been changed to a better one with more advantages on it. Before going further through this report, let's look up the general idea of this project through the block diagram below.

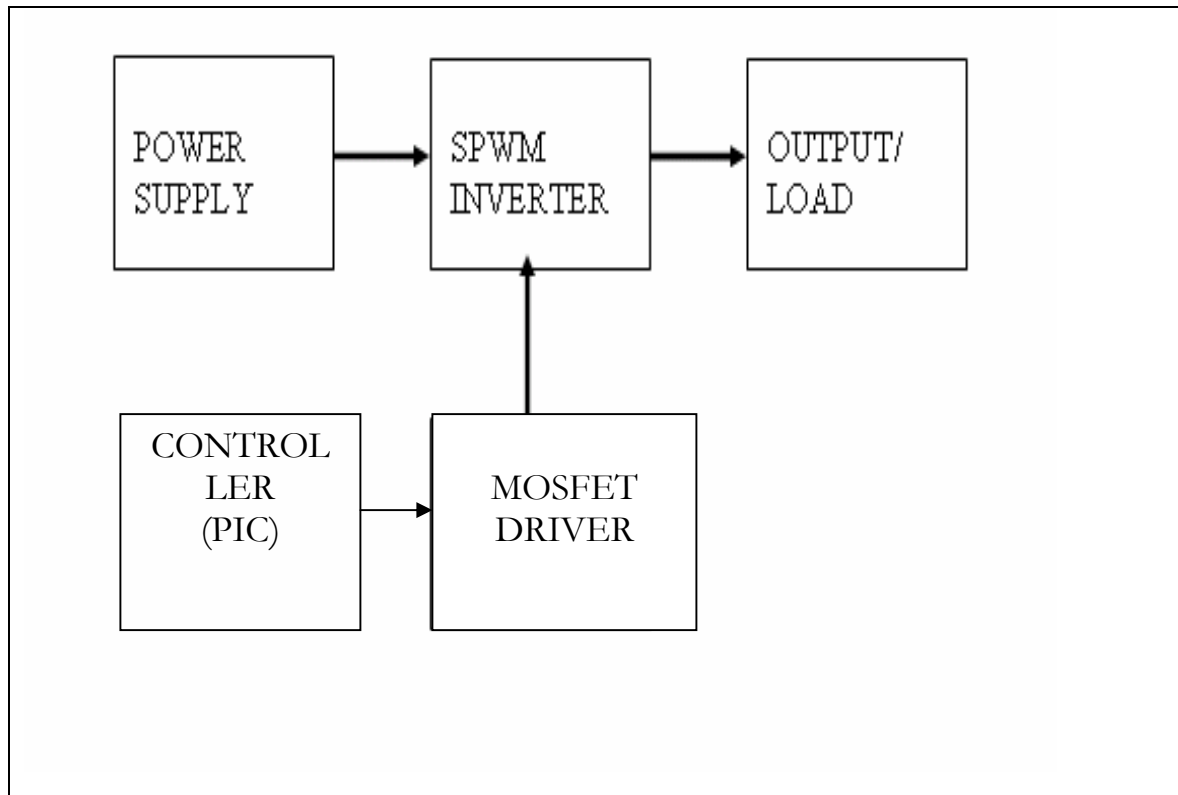


Figure 3.1: Basic Block diagram of the Project

Figure 3.1 shows the basic block diagram of the whole project. The design will accomplish through the use of high frequency switching and implementation of a microprocessor to digitally pulse our transistors. The PIC will give pulses that needed to drive the drivers hence control the switching scheme of the full-bridge inverter. The output of the load in the diagram is the speed of the motor.

3.2 Overall System Design

Design Specifications

Input Voltage	:	$<300 V_{DC}$
Output Voltage	:	Single-phase $240V_{AC}$ RMS
Output Frequency	:	40Hz , 50Hz and 60Hz
Output Power Range	:	>500 Watts
Switching Frequency	:	Variable frequency, Variable dutycycle
PIC Controls	:	PIC 18F4550

The design specification above has many different compare to the previous design specification, although the hardware use is the same configuration. The frequency and duty cycle are variables in order to get the variable output frequency from the inverter.

3.3 SPWM Inverter

Spwm inverter is a better approach in designing an AC output compare to the square wave inverter and modified square wave inverter.

3.3.1 Theoretical operation of SPWM inverter

In SPWM inverter, the output voltage signal can be obtained by comparing a control signal, $cont\ v$, against a sinusoidal reference signal, $ref\ v$, at the desired frequency as shown in Fig 3.3. At the first half of the output period, output voltage takes a positive value ($+dc\ V$), whenever the reference signal is greater than the control signal. At the same way, at the second half of the output period, the output voltage takes a negative value ($-dc\ V$) whenever the reference signal is less than the control signal [5].

The control frequency $cont\ f$ determines the number of pulses per half of cycle for the output voltage signal. Also, the output frequency O_f is determined by the reference frequency $ref\ f$. The modulation index Ma is defined as the ratio between the sinusoidal magnitude and the control signal magnitude [5].

To obtain a vary train of pulses, each pulse has to vary proportional to the necessary fundamental component precisely at the time when this pulse occurs. The frequency of the output waveform needs to be higher than the frequency of the fundamental component. By varying the width of each pulse, the inverter is able to produce different levels of output voltage for the corresponding pulse event [5].

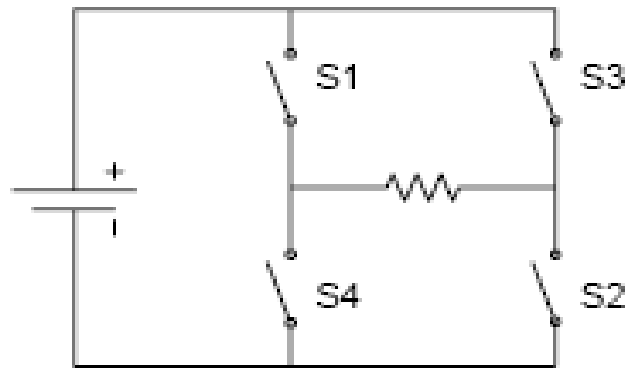


Figure 3.2 : Full Bridge Inverter

By referring to the Figure 3.2 above, we can apply unipolar switching scheme by control the switch as follows :

S1 is on when $v_{sine} > v_{tri}$

S2 is on when $-v_{sine} < v_{tri}$

S3 is on when $-v_{sine} > v_{tri}$

S4 is on when $v_{sine} < v_{tri}$

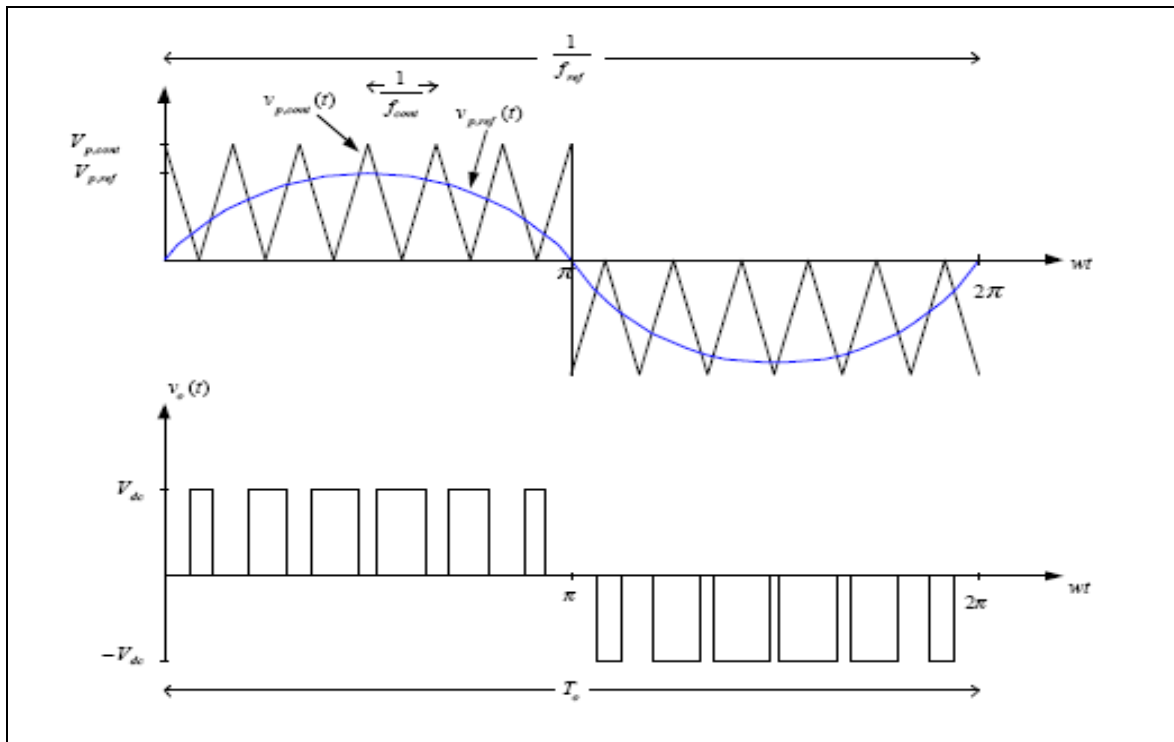


Figure 3.3 : Input and Output of unipolar SPWM Inverter.

3.3.2 PWM input/output

Pulse width modulation (PWM) analog signal can be used to pass analog data from a digital device. By varying wide pulses to indicate the actual voltage value, it is repeating signal that is on for a set period of time that is proportional to the voltage output. The higher the ratio of the pulse width to the periode (duty cycle), the more power deliver to the motor.

The inverter synthesizes an AC sine wave from the DC by the switching intervals. The small signal waveform from the PWM shapes the high voltage sinusoidal

output waveforms that run the motor. The variable width pulses from the PWM also control the duration and frequency that the switches turn on and off. Frequency of carrier signal, also determine the resulting number of square notches in the output of the inverter. The amplitude of the synthesized sine wave is determined by the width of the resulting square wave. The relatives' widths of these square waves represent the applied voltage.

3.3.3 Strategy to Develop SPWM Switching Schemes

There are many ways to produce variable pulse width modulation besides using typical way, which is by comparing the reference signal with the modulation signal. Figures below will show you how to produce SPWM output. This method is a more straight forward way which still have many advantages.

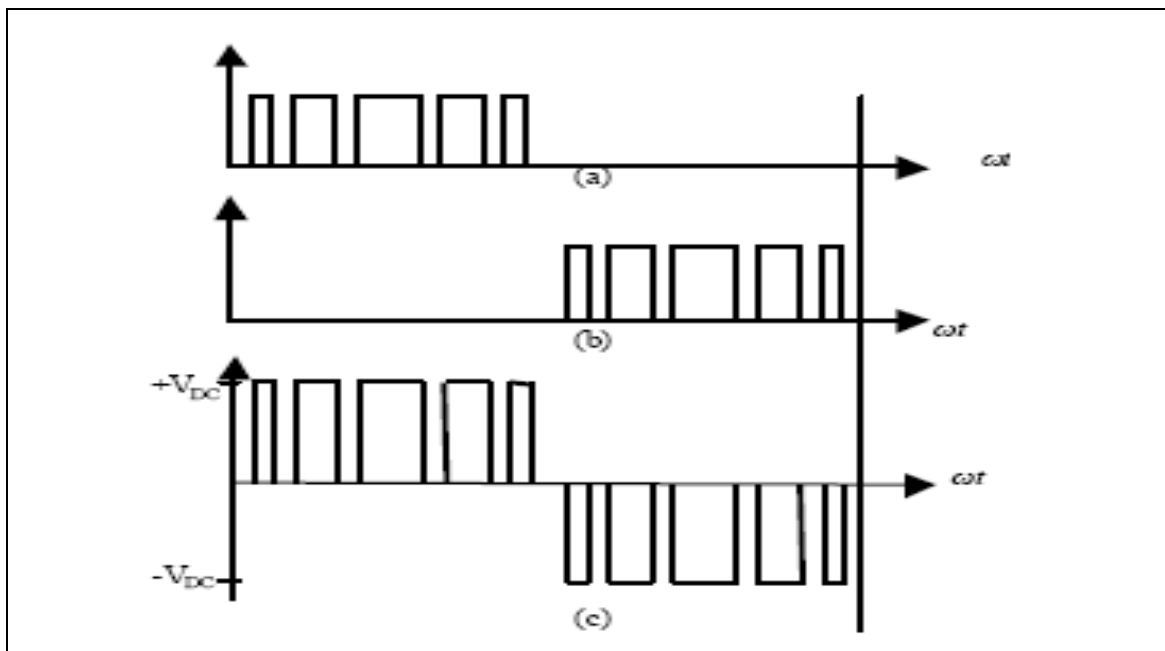


Figure 3.4: The switching signals; (a) Channel 1, (b) channel 2 and (c) the expected unipolar SPWM

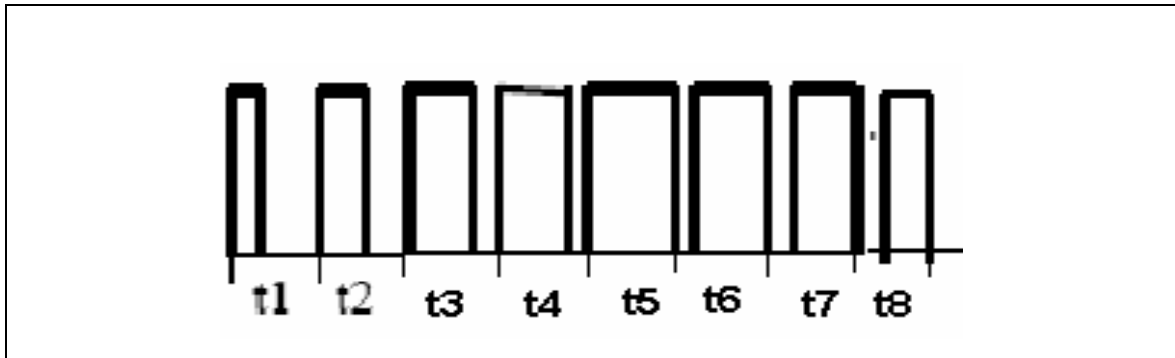


Figure 3.5: Graphical view of the switching pulses

The switching signals as shown in Fig. (a) and (b) are the desired SPWM signal for channel 1 and channel 2 respectively. Each channel is used to control a pair of inverter switches. The resultant output from a bridge inverter is shown in Fig. 1c. Designing switching pulses with high changes flexibility is the challenge in order to get the best approximation of the sinusoidal signal.

Each channel contributes half cycle of the inverter output waveform as illustrated in Fig. 3.4. This method eliminates the use of electronics component to generate the switching signals.

3.3.4 Design Method

The number of pulses, the switching time and the duty cycle generation are summarized in Table 1. The period for each cycle is fixed at certain calculated value and the duty cycle are then associated with the corresponding duty cycle. The switching

pulse characteristics as shown in Fig. 3.5 illustrates graphically the design strategy used to generate the single channel SPWM switching pulses.

Time t_1 represent the time for the predetermined duty cycle as tabulated in Table 1 is loaded. This next cycle is followed by t_2 and this cycle continuous until the last cycle, t_9 . Then the dead time for the channel 1 switching pulse is loaded. The dead time is set as 1 ms which is acceptable for various types of power transistor. Typically, the switching devices consume only a few nanoseconds to operate as a switch. This delay time is necessary to avoid the damage on the inverter circuit during the switching pair transition. This cycle produce half cycle of the inverter output waveform with eight switching pulses. The channel 2 then produces another cycle sequentially. This cycle again produce eight pulses. The total time and for the full cycle is then calculated as follow:

No. of switching pulses = 19 pulses $\times$ 1ms = 19.00ms

Total time + dead time = 20 pulses $\times$ 1ms = 20.00ms

Output Frequency = 50.0 Hz.

This approach shall produce the desired frequency, duty cycle and the number of pulses. Table 2 summarized all the calculated parameters. However, this is only the initial calculation on how to determine the duty cycle. The details on how the programs of the program works will be present on the next sub.

Table 3.1 : Early calculation of duty cycle

TIME	Duty Cycle %		Period of both pin	Output frequency
	Pin 1	Pin 2		
t1	68	40	1.25m	$1.25\text{ms} \times 16 = 20\text{ms.}$ $f = 1/20\text{m} = 50\text{ Hz}$
t2	80	20		
t3	92	12		
t4	72	28		
t5	40	68		
t6	20	80		
t7	12	92		
t8	28	72		

3.4 Hardware Design

The hardware design is divided into 4 parts. The power supply design, PIC microcontroller design, MOSFET driver design and Inverter design. Before the hardware has been developed, the simulation part of every circuit also has been made so that the circuit design will be in the right connection

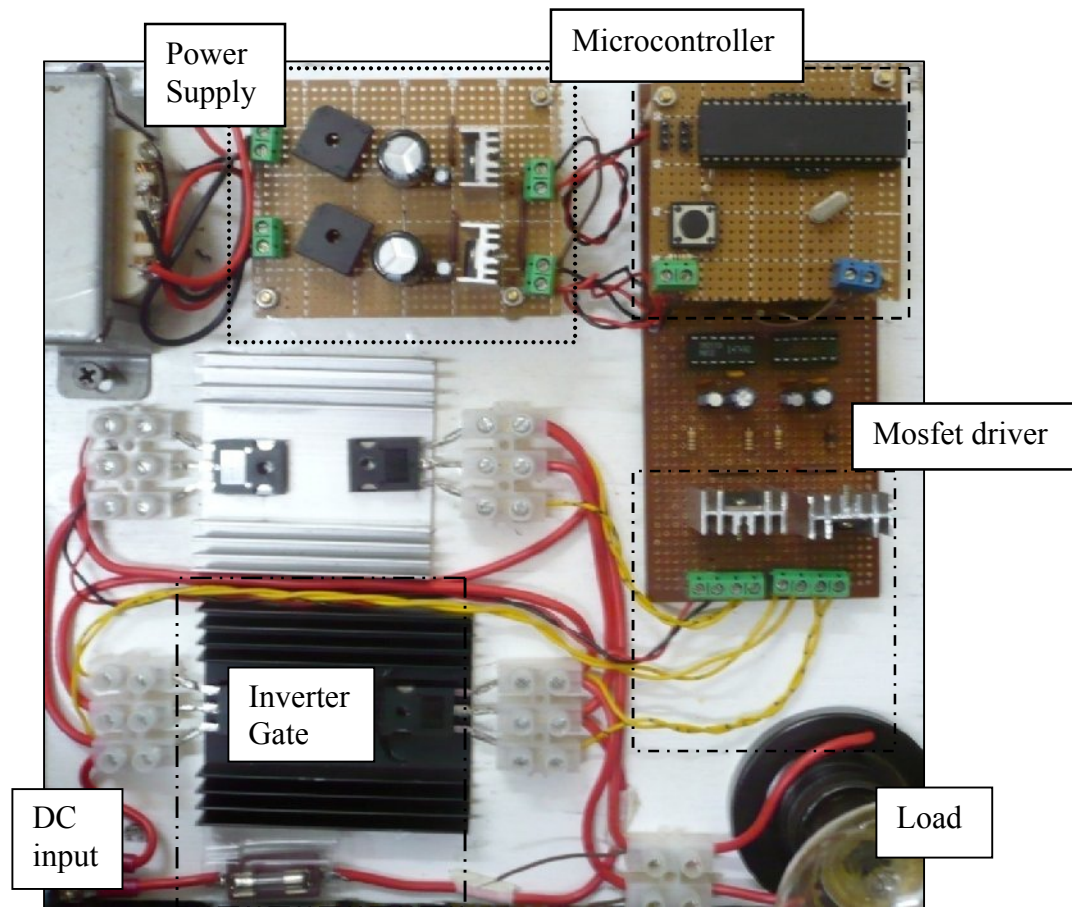


Figure 3.6: The full picture of hardware

3.4.1 Power Supply Design

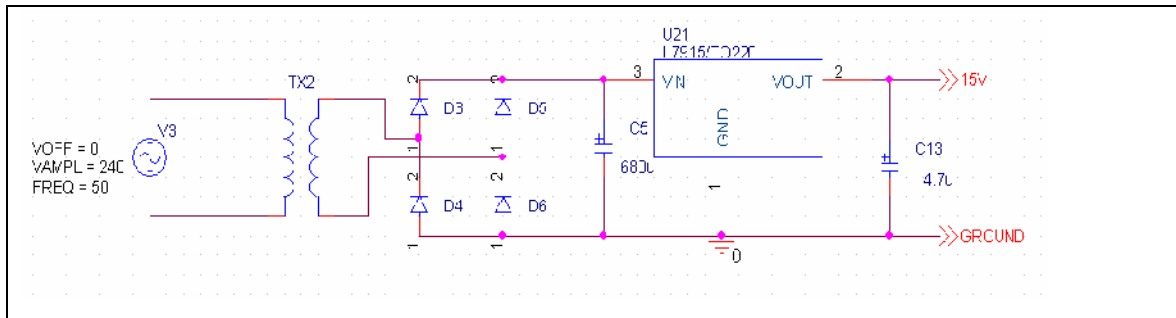


Figure 3.7: Power supply circuit

The power supply is developed by using full bridge rectifier and regulator to convert AC power supply to DC. This power supply is used as a replacement of battery that been used as a supply in UPS. This supply produces two voltages at the output, one is 5V and the other is 15V. The voltage is step down by power transformer from 240Vrms socket supply to 20Vrms and 12Vrms. The step down AC voltage been rectified by bridge rectifier and then voltage regulator LM7805 and LM7815 been used to regulate and stabilize the voltage at the output of the power supply. The 5V voltage is used to supply control circuit that contain PIC microcontroller and the 15V voltage is used to supply MOSFET driver circuit.

3.4.2 PIC Microcontroller Circuit Design

The microcontroller that used in designing the switching controller is 18F4550 and the crystal used is 20MHz. This PIC is chosen because it can generate high switching pulses and easy to get in the market. The high frequency crystal is used so it can support high switching pulses that can be used in further improvement of the inverter. The output pin used in this design is pin 33 and pin 34 and the input is in pin 2. The more detail about the software development is explained in the software parts.

3.4.3 Driver Design

In this part, there are two drivers being used. Each driver takes one PWM signal as input and produces two PWM outputs, one being complementary to the other. These two signals are used to drive one half bridge of the inverter: one to the upper switch, the other to the lower switch. The driver also adds a fixed dead time between the two PWM signals.

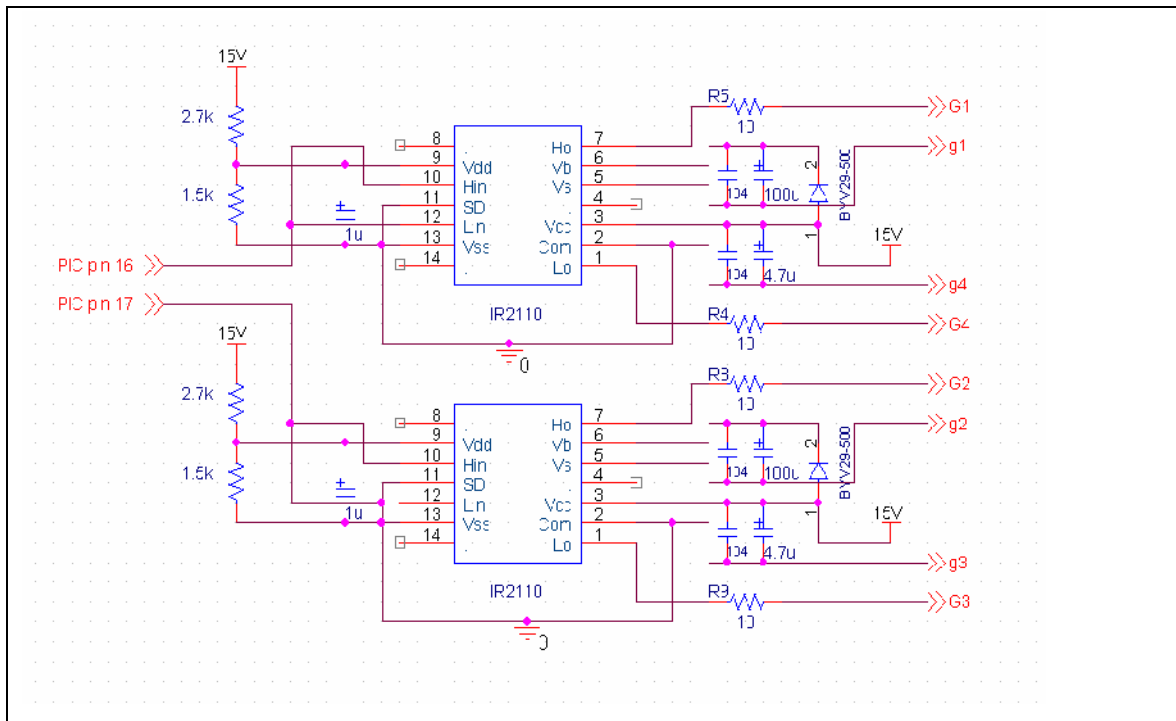


Figure 3.8: IR2110 MOSFET driver circuit

The IR2110 MOSFET gate driver chips play two vital roles in creating drive pulses suitable for operation of a full-bridge inverter circuit. First of all, the IR2110's amplify the 5-volt logic signals output by the microcontroller to obtain a 15 volt signal necessary to fully turn on the gate of the full-bridge circuit. A gate drive pulse of less than 10 volts could result in excessive heating which occurs when the MOSFET is driven are operating in the linear mode of operation, which by the physical MOSFET construction, happens to be the most resistive regions of operation.

The other role played by the IR2110 chips is to provide electrical isolation between the upper control pulses and the upper gate of the full-bridge inverter circuit. Electrical isolation is extremely important in biasing the upper full-bridge gate with the appropriate drive signal voltages. Without proper electrical isolation, the upper gate would be considered “floating”. In other words, the upper full-bridge MOSFETs would have a gate-to-source voltage ranging from 0 VDC to 340 VDC because they are not directly referenced to ground potential.

The IR2110 gate driver chips provide electrical isolation by inserting a capacitor and diode, also known as a “bootstrap supply”, are shown in Figure 3.9 below. When V_s is pulled down to ground (either through the low side FET or the load, depending on the circuit configuration), the bootstrap capacitor (C_{bs}) charges through the bootstrap diode (D_{bs}) from the 15 Vcc supply. This provides a supply to V_{bs} .

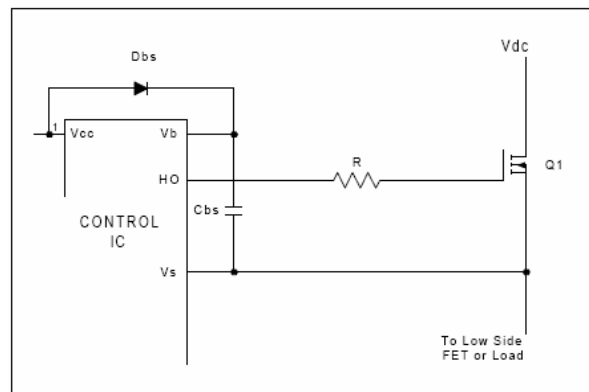


Figure 3.9: Bootstrap diode/capacitor circuit used with IR 2110 control IC's

3.4.3.1 Calculating Bootstrap Capacitor Value

The following equation gives the minimum charge which needs to be supplied by the capacitor:

$$Q_{bs} = 2Q_g + \frac{I_{qbs(max)}}{f} + Q + \frac{I_{cbs(leak)}}{f} \quad (3.2)$$

Q_g = Gate charge of high side FET (refer to IRFP450 datasheet)

f = frequency of operation

$I_{cbs(leak)}$ = Bootstrap capacitor leakage current (neglected if using ceramic capacitor)

Q_{ls} = level shift charge required per cycle = 5nC (500V/600V IC's) or 20nC (1200V IC's)

$$\begin{aligned} Q_{bs} &= 2(75n) + \frac{230u}{50} + 5n + \frac{0}{50} \\ &= 4.755uC \end{aligned}$$

The bootstrap capacitor must be able to supply the charge given by equation 3.2 and retain its full voltage. Otherwise, there will be a significant amount of ripple on the V_{bs} voltage which could cause the Ho output to stop functioning. Therefore, the charge in the C_{bs} capacitor must be a minimum of twice the value given by equation 3.2. The minimum capacitor value can be calculated from the equation 3.3 below:

$$C \geq \frac{2[Q_{bs}]}{V_{ce} - V_f - V_{LS} - V_{min}} \quad (3.3)$$

Where:

V_f = Forward voltage drop across the bootstrap diode (refer to BYV29-500 datasheet)

V_{LS} = Voltage drop across the low side FET (V_{SD} in IRFP450 datasheet)

V_{Min} = Minimum voltage between V_B and V_S (minimum V_{BSUV} in IR2110 datasheet)

$$C \geq \frac{2[4.755\mu]}{15 - 1 - 1.4 - 7}$$

$$\geq 1.698\mu F$$

The C_{bs} Capacitor value obtained from the above equation above is the absolute minimum required, however due to the nature of the bootstrap circuit operation, a low value capacitor can lead to overcharging, which could in turn damage the IC. Therefore to minimize the risk of overcharging and further reduce ripple on the V_{bs} voltage the C_{bs} value obtained from the above equation should be multiplied by a factor of 15 (rule of thumb).

$$\begin{aligned} C_{new} &\geq 1.698\mu F \times 15 \\ &\geq 25.47\mu F \\ &\geq 47\mu F \text{ (nearest available value)} \end{aligned}$$

3.4.3.2 Selecting Bootstrap Diode

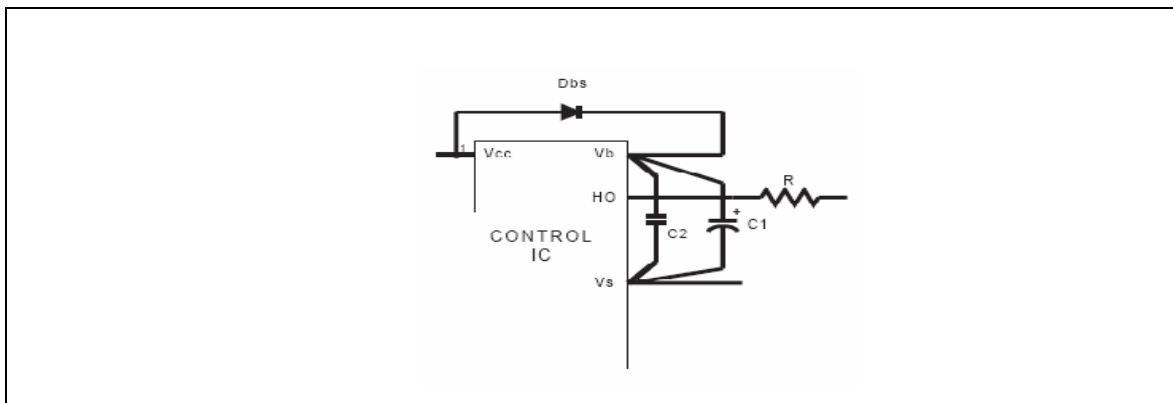
The bootstrap diode (D_{bs}) needs to be able to block the full power rail voltage, which is seen when the high side device is switched on. It must be a fast recovery device to minimize the amount of charge fed back from the bootstrap capacitor into the V_{cc} supply, and similarly the high temperature reverse leakage current would be important if the capacitor has to store charge for long periods of time. There BYV29 – 500 is chosen because of the following characteristics listed on the table below:

Table 3.2 : Diode Characteristics

Max / min wanted Characteristics	BYV29 – 500
V_{RRM} = Power rail voltage ≥ 400 V	$V_{RRM} = 500$ V
Maximum $t_{rr} = 100$ ns ≤ 100 ns	$t_{rr} \leq 60$ ns
$I_F = Q_{bs} \times f$ $= 4.755\mu C \times 50$ Hz $= 0.238$ mA	$I_F = 9$ A

3.4.3.3 IR2110 Circuit Layout Considerations

For the layout of IR2110 circuit, the bootstrap capacitor is placed closed to the pins of the IC (as shown in Figure 3.10). At least one low ESR capacitor should be used to provide good local decoupling. If an aluminium electrolytic capacitor is used for the bootstrap capacitor, a separate ceramic capacitor need to be placed close to the IC. If the bootstrap capacitor is a ceramic or tantalum type, the capacitor alone should be sufficient as the local decoupling.

**Figure 3.10:** Recommended layout of the Bootstrap Component

3.4.4 Inverter Design

There are 3 main type of inverter in the market today. The most simple and cheapest type is square wave inverter, the improved version of square wave inverter is a modified square wave inverter, the best and most expensive type is true sine wave inverter. Through the development, the design inverter of this project is true sine inverter by using full-bridge inverter configuration (H-Bridge).

The full-bridge inverter used for this project is very simple to construct because it only consists 4 switches, as shown in Figure 3.11. The function of the full-bridge inverter is to convert 340 VDC from supply into 240Vrms with variable frequency. The gate chosen for the full-bridge inverter circuit are IRFP450's. The IRFP450 MOSFET are chosen because they have appropriate voltage and current ratings ($V_{DS\ max} = 500V$, $I_{D\ max} = 14A$). This is suitable for high switching frequency.

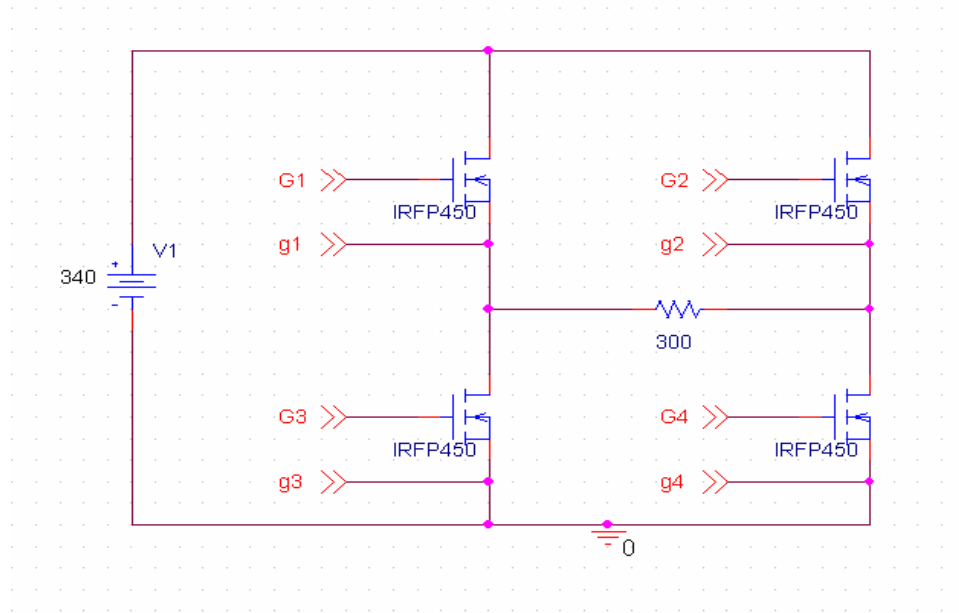


Figure 3.11: Full-bridge inverter

The two PWM pulses produced by the microcontroller circuit are fed into the full-bridge inverter. One signal is sent in parallel to MOSFET gate G1 and G4. The other signal is sent in parallel to MOSFET gate G2 and G3. The signal programmed in the microcontroller will allow for MOSFET gate G1 and G4 to be ON while MOSFET gate G2 and G3 are OFF, and vice versa.

There is no load applied in this design, but the output could be check by using oscilloscope. The actual value of power that can be sustained by the designed inverter can sustain up to 500W.

3.4.4.1 Low-Pass Filter

In addition, for a better frequency and voltage output a low- pass filter is also developed. It can be used to eliminate any frequency that higher than cutoff frequency.

Low-pass filter can result a great reduction of the inverter output harmonics and hence provide clean power for the load. The filter is inserted after the output of full-bridge inverter in order to eliminate any frequency higher than cutoff frequency. The cutoff frequency can be calculated by using following formula:

$$C \text{ chosen} = 100\mu$$

$$f = 50 \text{ Hz}$$

$$f_{cutoff} = \frac{1}{2\pi\sqrt{LC}}$$

$$\begin{aligned} L &= \left(\frac{1}{2\pi \times f_{cutoff} \times \sqrt{C}} \right)^2 \\ &= \left(\frac{1}{2\pi \times 50 \times \sqrt{100\mu}} \right)^2 \\ &= 101.3 \text{ mH} \end{aligned}$$

Although the frequency is changed between 40 Hz, 50 Hz and 60 Hz, the value of the calculated inductor is still could be accepted.

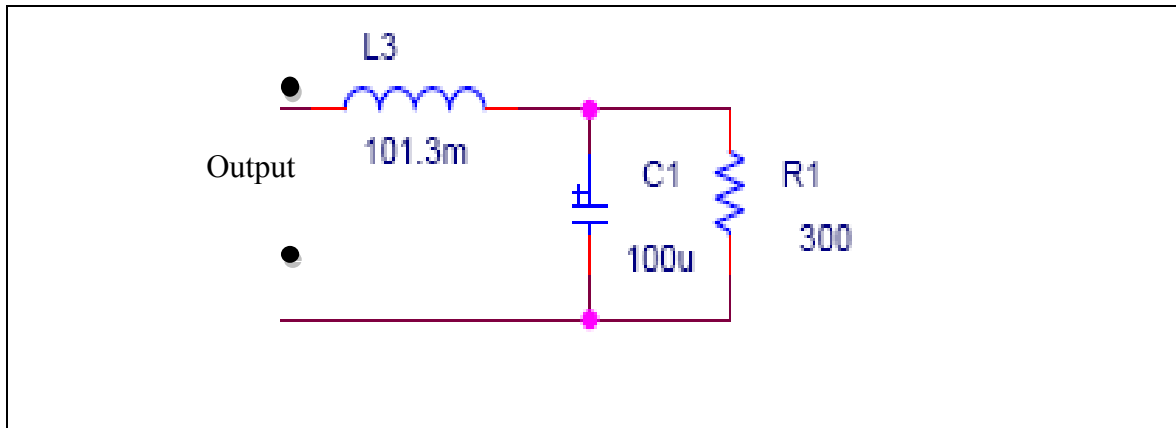


Figure 3.12: L-C low-pass filter schematic

The Figure 3.12 shown is the configuration of L-C filter. The capacitor is placed parallel with load and the inductor is placed series with capacitor and load.

3.5 Software Development

It is important to know that the software development playing the significant role in this project. let seen some important features and methods used to program the PIC.

3.5.1 PIC18F4550 Microcontroller Structure

A PIC microcontroller is used as a brain in this circuit. Microcontroller that is chosen is PIC18F4550. This is because, PIC18f4550 offers the advantages of all PIC18 microcontrollers where they are namely, high computational performance at an economical price with the addition of high endurance, Enhanced Flash program memory. In addition to this feature, the PIC18F4550 family introduces design enhancements that make these microcontrollers a logical choice for many high-performances, power sensitive applications. It has large amounts of RAM memory for buffering and Enhanced Flash program memory make it ideal for embedded control and monitoring applications that require periodic connection with a (legacy free) personal computer via USB for data upload/download and/or firmware updates.

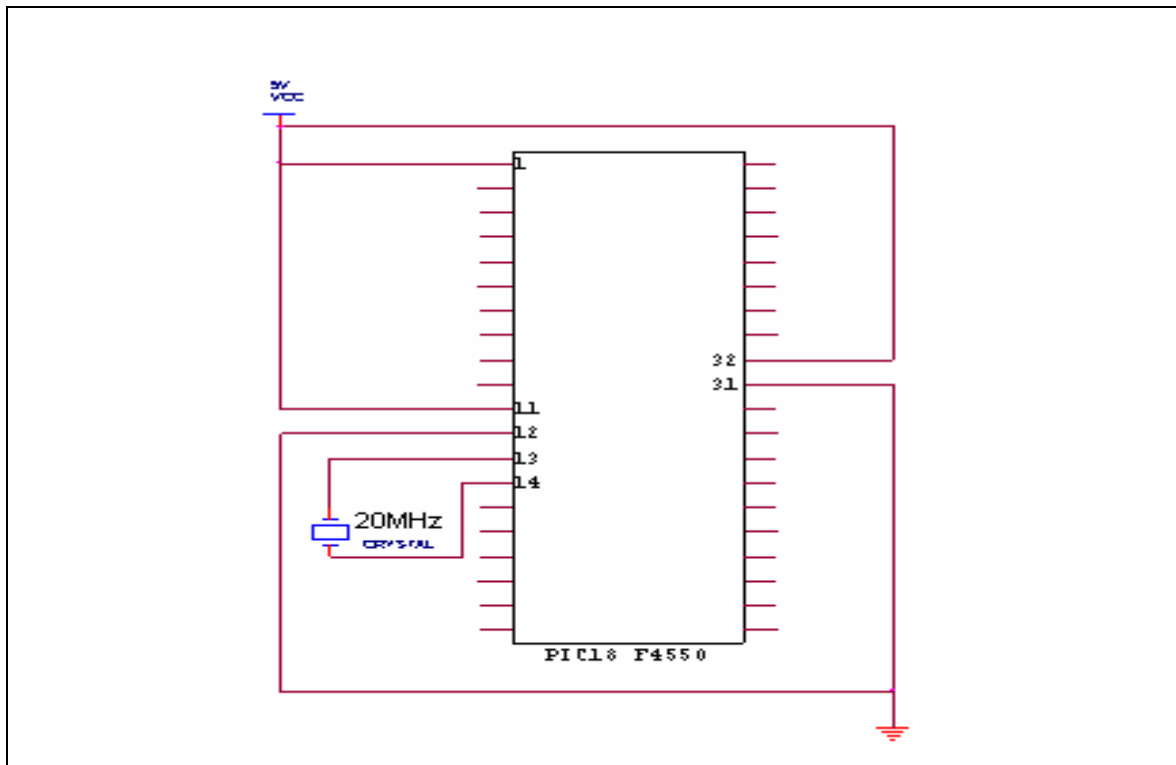


Figure 3.13: Basic schematic diagram of 18F4550

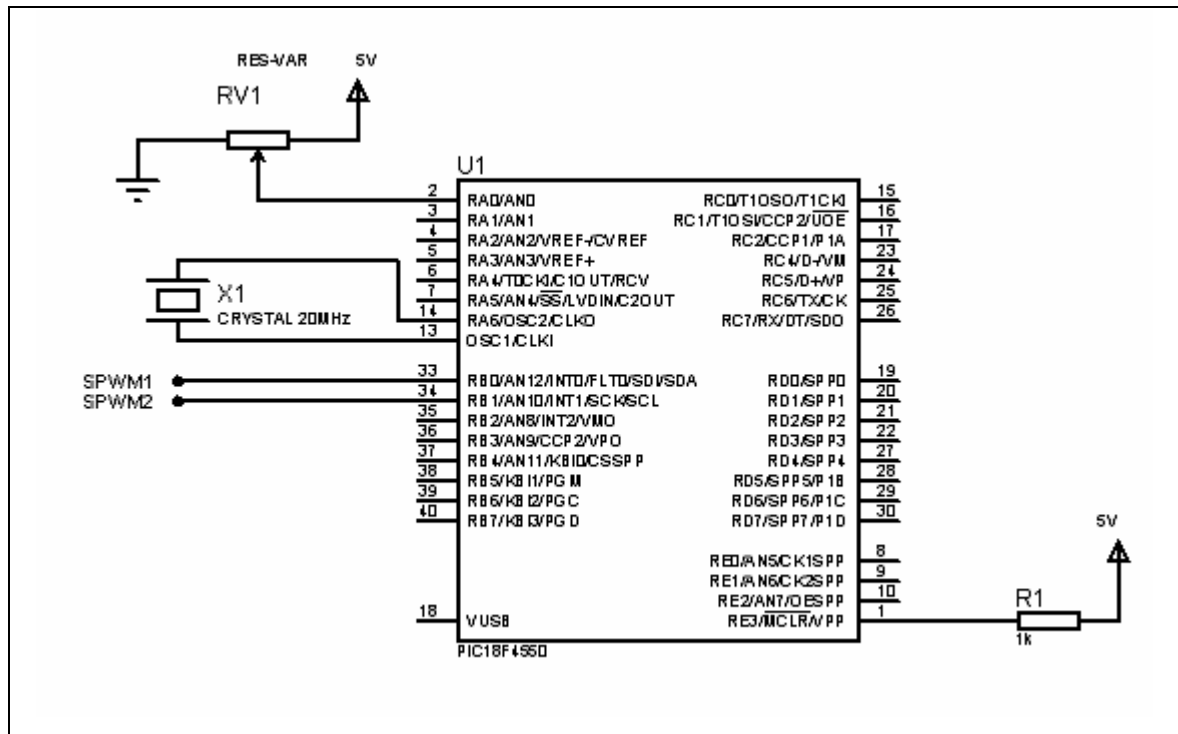


Figure 3.14: Additional circuit of 18F4550

Figure A shows the basic schematic diagram of any pic should be designed (connection of ground (Vss) and +5V (Vdd) while figure B shows the input and output connection of the pic. A 2k ohm variable resistor / potentiometer control the input (ADC) and the output is SPWM1 and SPWM2.

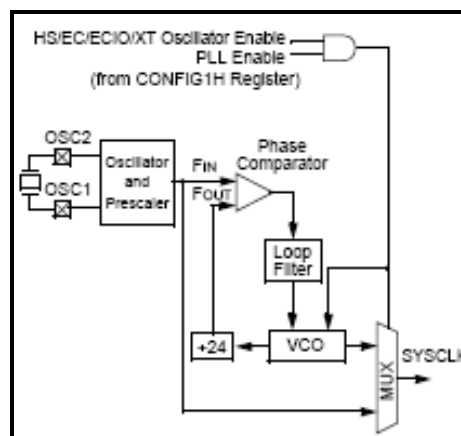


Figure 3.15: PLL block diagram (HS mode)

In this project, crystal value of 20 MHz is used. The crystal frequency for 8 MHz and 20 MHz are on HS type. Figure C explain the internal circuit built in the PIC Microcontroller about PLL for HS mode. The HSPLL, ECPLL and ECPIO modes make use of the HS mode oscillator for frequencies up to 48 MHz. The prescaler divides the oscillator input by up to 12 to produce the 4 MHz drive for the PLL. The XTPLL mode can only use an input frequency of 4 MHz which is drives the PLL by default.

3.5.2 PIC18F4550 Microcontroller Interface

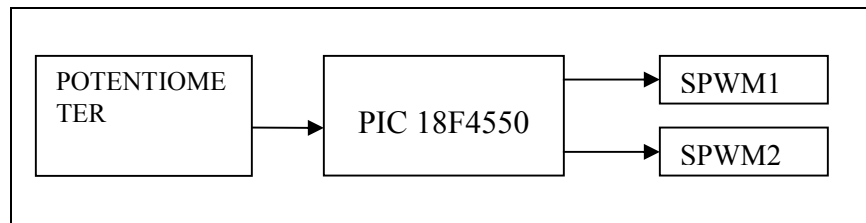


Figure 3.16 : Block diagram of PIC controller

Figure 3.12 shows how PIC 18f4550 is used as the controller circuit in the SPWM development that will be fed into the full bridge inverter. Potentiometer in this circuit is used as the analog input. By vary the potentiometer, at certain point the program will execute at the specific data register and then the output pulses are varied by this way. By controlling the potentiometer, the program will execute in three different phases (40Hz, 50Hz and 60Hz). The detail of the program will be discussed on Chapter 4.

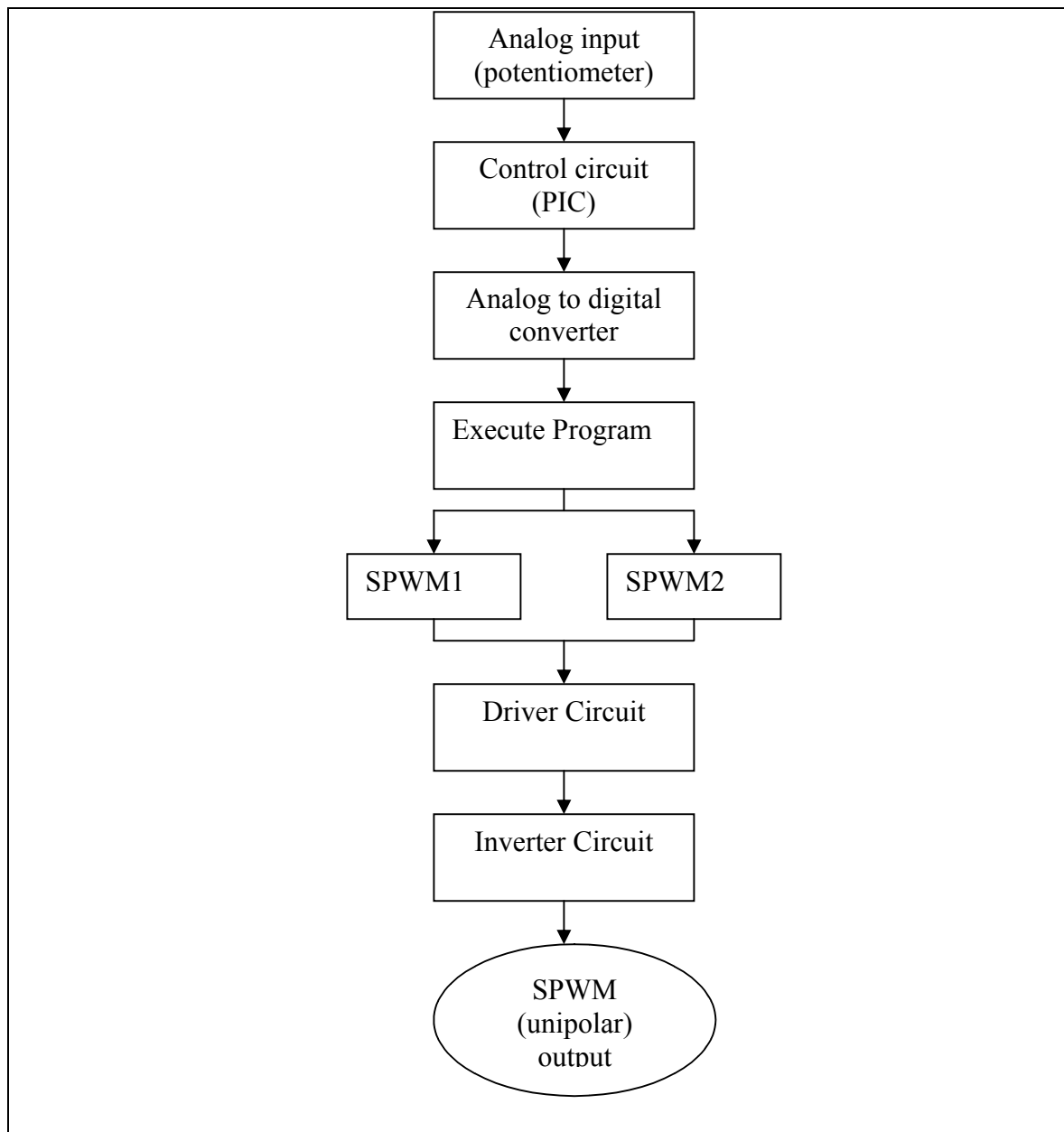
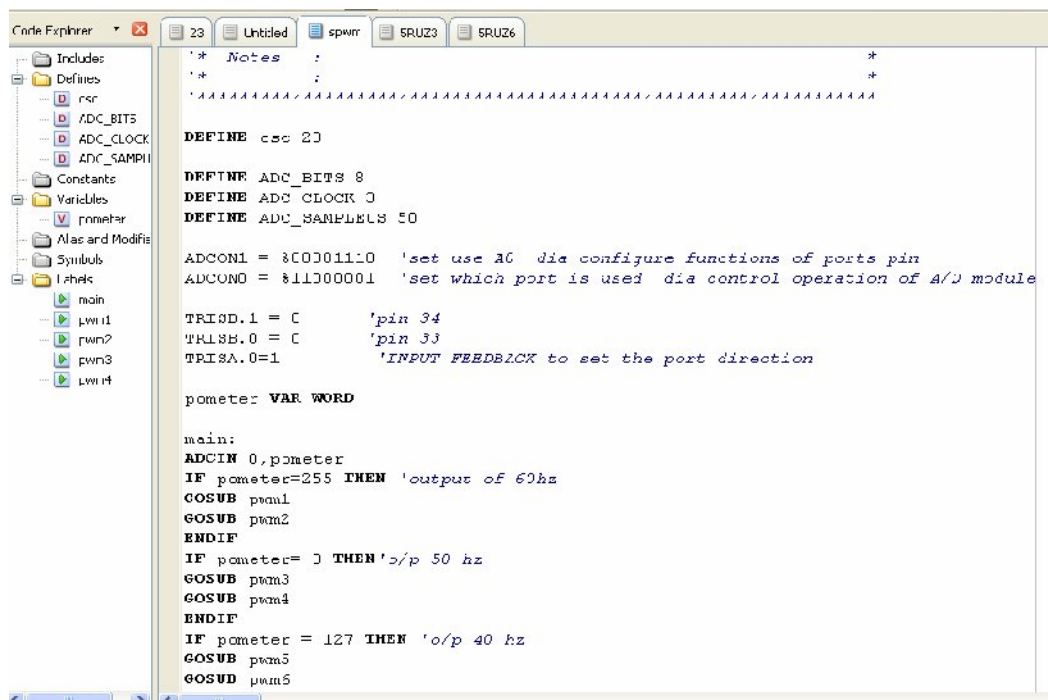


Figure 3.17 : Flow chart of software and hardware interface

3.5.3 PIC18F4550 Microcontroller Programming

In order to interface the hardware with the electronic equipment, the following tools are usually required in a PIC microcontroller based project development. These software run on a PC to develop applications for Microchip microcontrollers. The program is written in a text editor named Microcode Studio and the compiler is known as PicBasic Pro Compilers. To complete them, a PIC programmer device software is used. Below are the steps on how to develop the project using this software:

3.5.4.1 Writing program in microcode studio.



```

Code Explorer
├── Includes
├── Defines
│   ├── rscr
│   ├── ADC_BITS
│   ├── ADC_CLOCK
│   └── ADC_SAMPLE
├── Constants
├── Variables
│   └── pometer
├── Alias and Modifiers
├── Symbols
├── I/O
├── main
├── pwm1
├── pwm2
├── pwm3
└── pwm4

23  Untitled  spwr  SRUZ3  SRUZ6

'* Notes :
'* :
'*****

DEFINE csc 20

DEFINE ADC_BITS 8
DEFINE ADC_CLOCK 0
DEFINE ADC_SAMPLES 50

ADCON1 = %0001110 'set use AC dia configure functions of ports pin
ADCON0 = %11000001 'set which port is used dia control operation of A/D module

TRISD.1 = 0 'pin 34
TRISB.0 = 0 'pin 33
TRISA.0 = 1 'INPUT FEEDBACK to set the port direction

pometer VAR WORD

main:
ADCON 0, pometer
IF pometer=255 THEN 'output of 60hz
GOSUB pwm1
GOSUB pwm2
ENDIF
IF pometer= 0 THEN 'o/p 50 hz
GOSUB pwm3
GOSUB pwm4
ENDIF
IF pometer = 127 THEN 'o/p 40 hz
GOSUB pwm5
GOSUB pwm5

```

Figure 3.18: Earlier program of ADC controller in PIC

ADCIN channel, var (ADCIN 0,pometer) is used to read the on-chip analog to digital converter channel and store the result in the variable (Var) . While the ADC registers can be accessed directly, ADCIN makes the process a little easier. Before ADCIN can be used, the appropriate TRIS register must be set to make the desired pins inputs. ADCON1 is set to assign the desired pins to analog inputs and in some cases to set the result format and clock source.

3.5.3.2 Compile the program

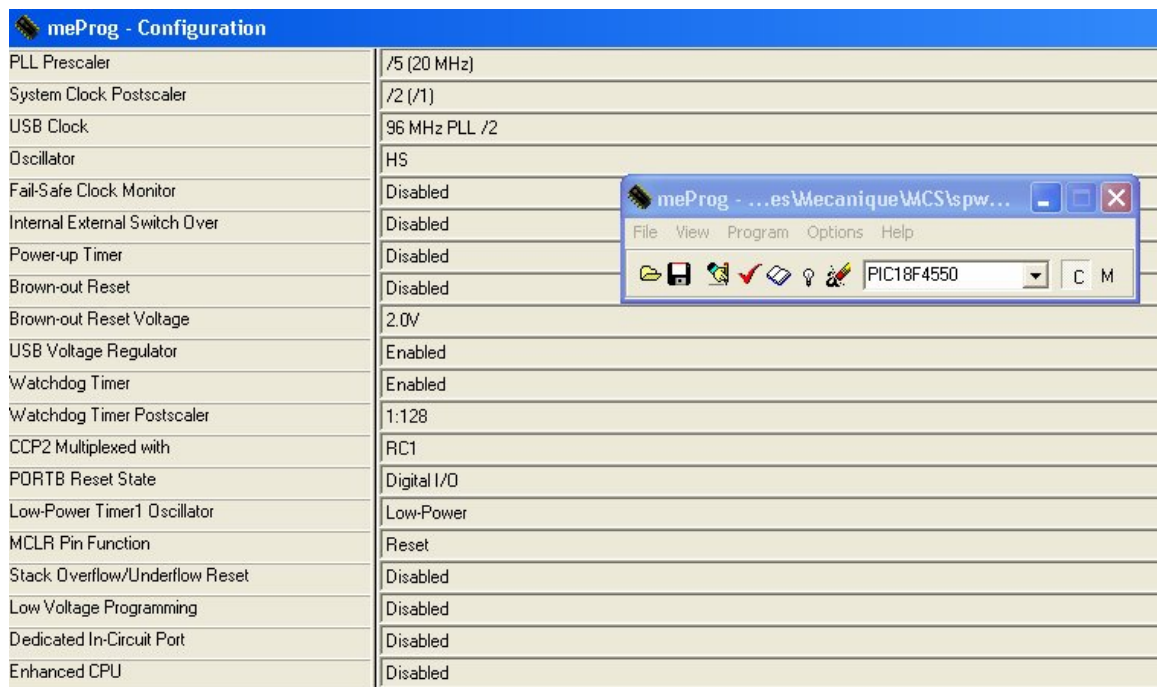


Figure 3.19 : Compiler Configuration

PicBasic Pro is used to compile the written program. If the program is compiled successfully, the above configuration will appear. The configurations need to be set in an appropriate setting before proceed to the next step.

3.5.3.3 Verify program

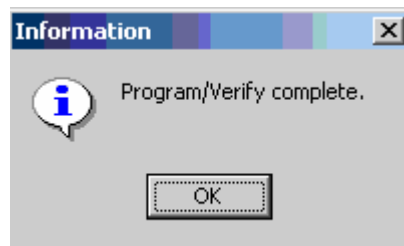


Figure 3.20: Verifying the program

Figure 3.13 shows the complete of verifying the program. This step is the last step where the program is burned to the PIC. Now the PIC is ready to be used with the hardware circuit.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Introduction

This chapter shows the result and analysis of the Inverter. The comparison between hardware result and simulation by using Orcad Pspice 9.1 will be analyzed. The measurement of hardware output is using oscilloscope. The analysis is divided into 4 parts:

- i. Orcad Pspice Simulation
- ii. Power supply output voltages
- iii. Microcontroller output pulses
- iv. Analysis of driver and inverter output

4.2 Simulation of SPWM inverter by using PSpice

By using the Pspice, the early topology of the circuit of the project could be design. The inverter circuit is designed using the topology of single-phase full-bridge (H-bridge) inverter, and the switching technique that has been applied is the SPWM technique with filter. However in PSpice, the real topology of a real PIC microcontroller could not be applied. Moreover, the PIC microcontroller is based on the software programming not the hardware topology.

From the simulation result the output is a unipolar sine wave. So, for the moment the result is satisfied the objective of the project, where from this output, we can determine on how to control the output(the speed of the motor) by verifying the pulses that given to the inverter.

Below are the block diagram of SPWM inverter by using PSPICE and its' simulation result. The op-amps are used to replace the PIC microcontroller in this circuit, where in the hardware design, there should be the PIC.

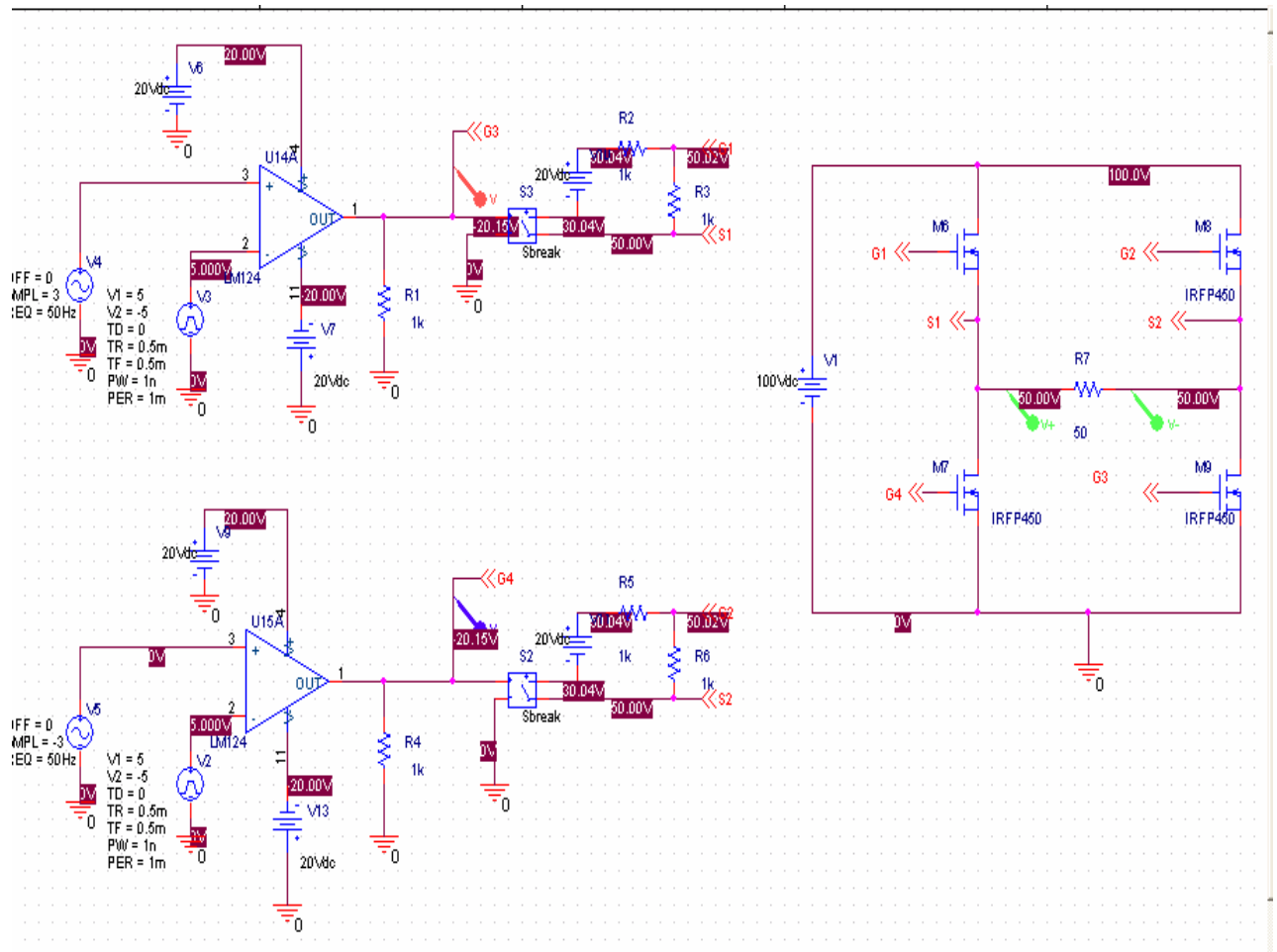


Figure 4.1 : SPWM Inverter using Pspice Simulation

The purpose of the op-amps is to produce pulses to fed into the driver circuit so that the voltage of the pulses will be in suitable form for the full bridge inverter to function. V pulses that supplied to the both op-amps part s set to be 5 V because it is the same voltage that PIC could receive.

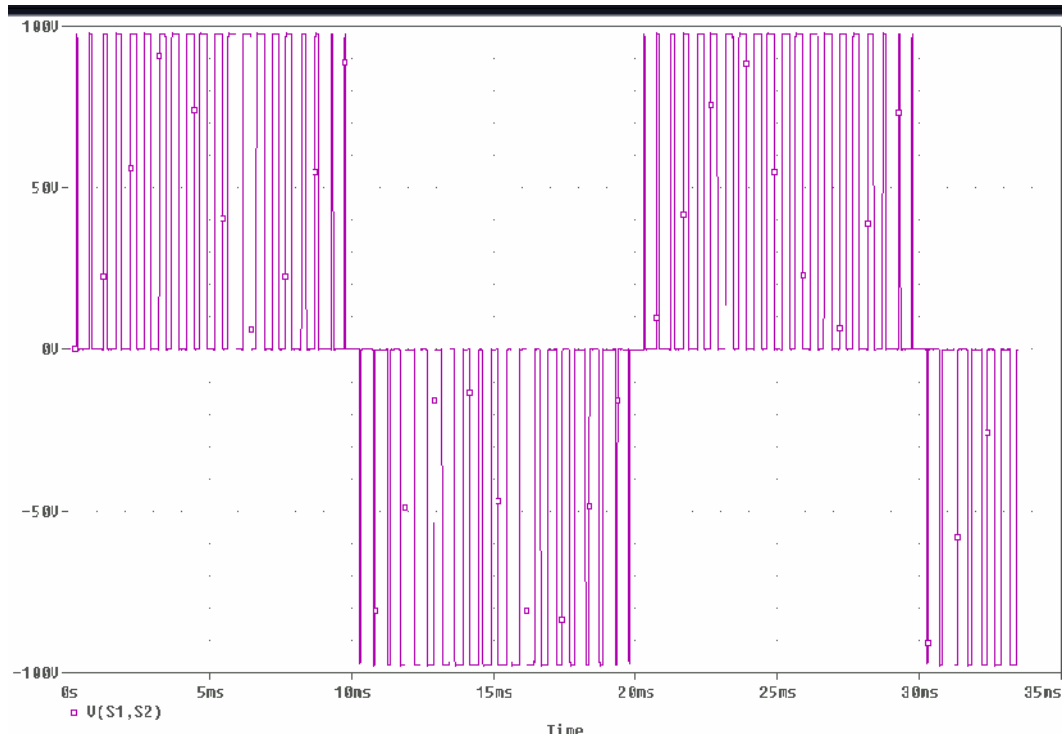


Figure 4.2: PSpice simulation result

The simulation result shows that the output is a unipolar Spwm output which is satisfied the objective of this project. the output frequency also comes out with 50 Hz, which is the desired frequency. To change the frequency duration, the value of TR and TF have to be adjusted.

4.3 Power supply output voltages

The analysis of supply voltage is important to ensure the voltage is not exceeding the required value. Electronic component such as PIC just need 5V to operate. If the component is supplied with high voltage, the component will be hot

and in some cases it can blow. The other factor need to be considered is voltage ripple. The ripple will bring effect to generated pulses and it will make the output of the inverter not smooth.

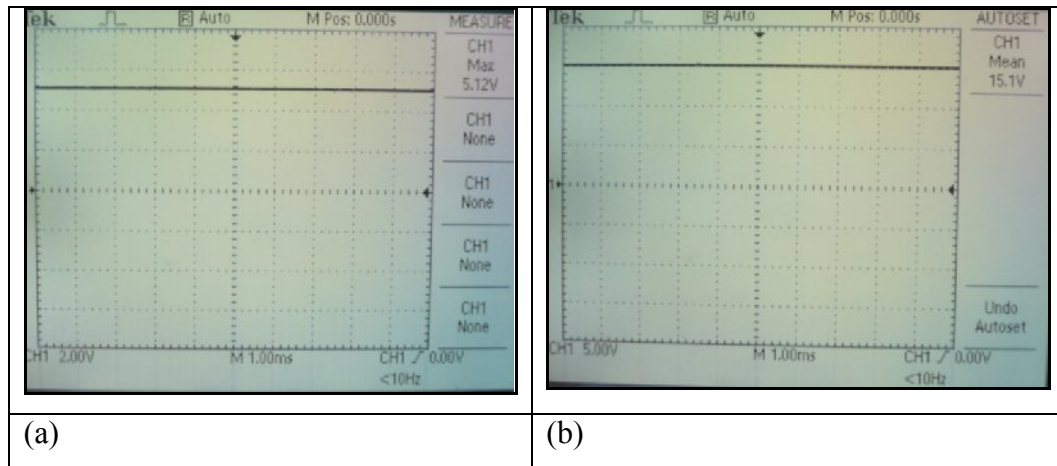


Figure 4.3: Power supply output voltage (a) output1 (b) output2

The Figure 4.1(a) and 4.1(b) is the output of power supply. From the figure we can see that the output is very smooth and the voltage is near to the desired value. The voltage magnitude of the power supply output is show at Table 4.1.

Table 4.1: Supply output versus design constrain

	Design constrain	Supply output
Output 1	5V	5.12V
Output 2	15V	15.1V

4.4 Microcontroller output result and analysis

This part will discuss detail on how the program works and how the pulses are achieved.

4.4.1 Software design

Command HIGH, LOW and PAUSE are used to produce the output of PWM inverter. Other command such the PWM and HPWM cannot be used, although they were much easier to get pulses, but because of the minimum requirement of their delay is below some values that can not be used to give an output frequency like the desired one. They are limited to some certain values that couldn't make the desired output frequency. Potentiometer is used as the variable input for this circuit topology. When the potentiometer is tuning at the certain values, via programming the PIC will execute at certain coding then the output is varied. For this design they are only 3 output of frequencies (40, 50 and 60 Hz). From chapter three, there has been a discussion on the strategy how to produce output frequencies can be made without involving the traditional method (comparing sine wave and triangular wave). The determination of duty cycle for every pulse is still the same, but due to the limitation of the instruction of the PIC Basic Pro, recalculation has been made. Table below shows the values of instruction PAUSE which are use together with LOW and HIGH.

Table 4.2 : Delay time

Time/Pause	Frequency (Hz)					
	40		50		60	
	HIGH	LOW	HIGH	LOW	HIGH	LOW
t1	30	170	50	200	250	50
t2	50	150	70	180	100	200
t3	70	130	90	160	170	130
t4	130	70	140	110	180	120
t5	150	50	170	80	200	100
t6	160	40	190	60	250	50
t7	180	20	210	40	270	30
t8	70	130	110	140	50	150
t9	50	150	70	180	100	200
t10	30	170	50	200	130	170
Total	2000=20Hz		2500=25Hz		3000=30Hz	

4.4.2 Coding Statement

For better understanding about the software development, let's see the coding statement that are used involving the PIC Basic Pro software. Below are listed some important statement that are used in this coding.

TABLE 4.3: Coding Statement

Statement	Function
PAUSE	Pause the program for period milliseconds. Period is 16-bits, so delays can be up to 65,535 milliseconds (a little over a minute).
HIGH	Make the specified Pin high (5V). Pin is automatically made an output
LOW	Make the specified Pin low(0V). Pin is automatically made an output.
ADC	Read the on-chip analog to digital converter channel. (potentiometer)
IF...THEN	Performs one or more comparisons. Each Comp term can relate a variable to a constant or other variable and includes one of the comparison operators. Then evaluates the comparison terms for true or false.

```

DEFINE osc 20

DEFINE ADC_BITS 8
DEFINE ADC_CLOCK 3
DEFINE ADC_SAMPLEUS 50

ADCON1 = %00001110  'set use A0 dia configure functions of ports pin
ADCON0 = %11000001  'set which port is used dia control operation of A/D module

TRISB.1 = 0          'pin 34
TRISB.0 = 0          'pin 33
TRISA.0=1            'INPUT FEEDBACK to set the port direction

pometer VAR WORD

main:
ADCIN 0,pometer
IF pometer=255 THEN 'output of 60hz
GOSUB pwm1
GOSUB pwm2
ENDIF
IF pometer= 0 THEN 'o/p 50 hz
GOSUB pwm3
GOSUB pwm4
ENDIF
IF pometer = 127 THEN 'o/p 40 hz
GOSUB pwm5
GOSUB pwm6
GOTO main

```

Figure 4.4: Software Programming Codes

Figure 4.4 shows the coding that is written in the microcode studio. The whole program is listed on the appendix part.

4.4.3 Result Analysis

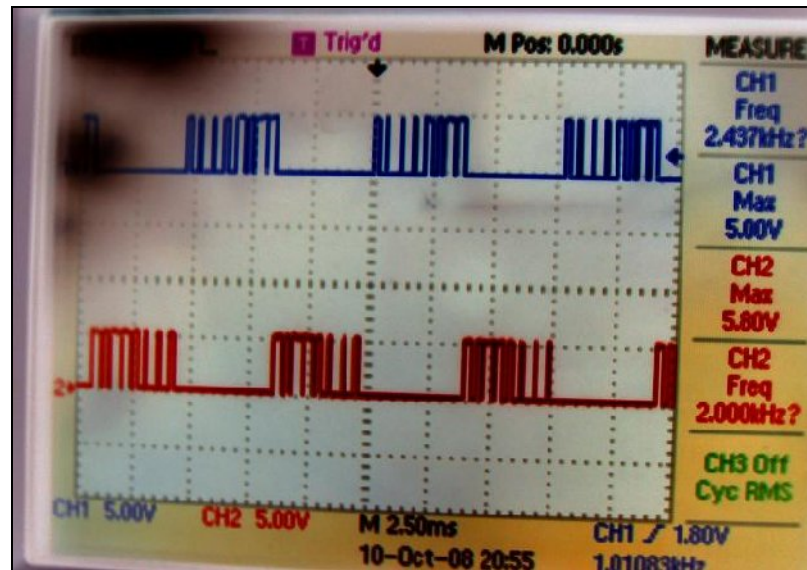


Figure 4.5 : 2kHz output.

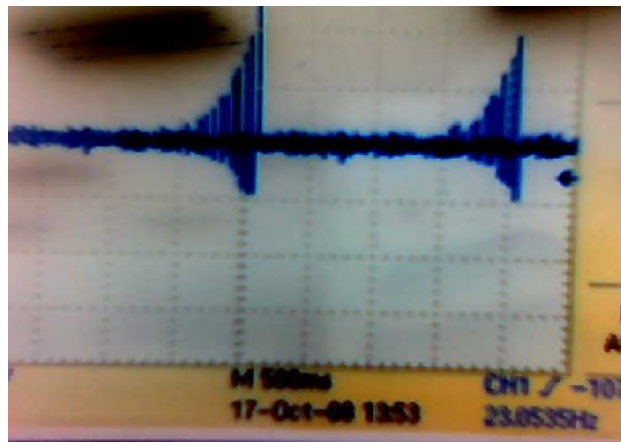
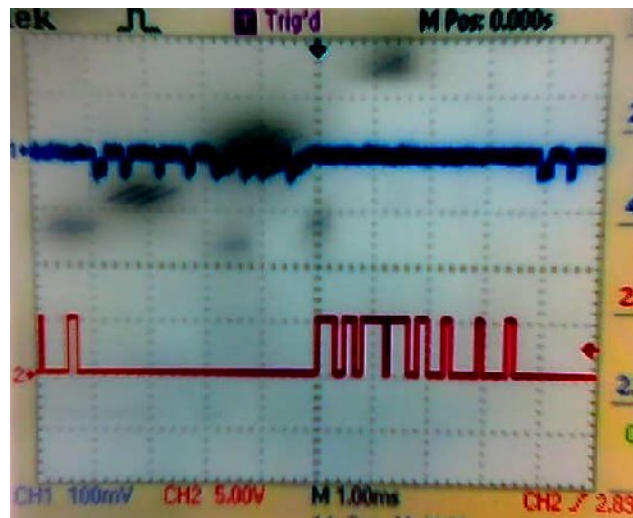
Figure 4.5 shows the output of PIC 18F4550. The output frequency is quite high. But the idea is when this both pulses apply to inverter, they will give the output of SPWM pulses. The upper pulses will give the positive value and the lower one will give the negative magnitude. The output voltages are same with the input voltage. This frequency is suitable for power MOSFET switching frequency.

They are long delay before the cycle of the pulses starting back to the next cycle. This delay satisfied the theoretical condition to give pulses to the inverter.

Later with some modification of the codes to get the frequency output (40/50/60Hz) like the desired one, the output pulses are really small and the peak to peak value of the output voltage also small. This is due to the programming statement itself that could not support the value like the desired one. Refer to the table below to compare the theoretical value and the output result from PIC.

Table 4.4: Frequency output

Desired output (Hz)	Output result(Hz)
20	23
25	28
30	36

**Figure 4.6 :** 23 Hz Output Frequency**Figure 4.7 :** 28 Hz output frequency

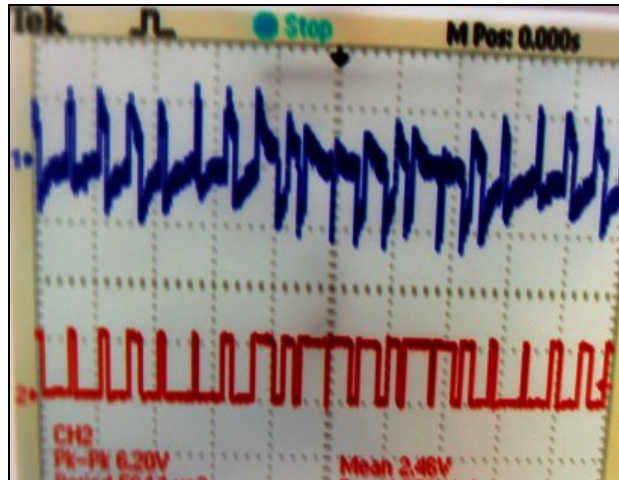


Figure 4.8 : 35 Hz output frequency

The results show that there is different from the theoretical one, but they still could be consider and is still in the range. It can be seen that when the frequency getting smaller the output pulse wave is not in rectangular form anymore. This is due to the PIC or the software programming itself . They have some limited function.

4.5 Inverter output analysis.

For the inverter, the desired result could not be performed in this project. But the analysis of the simulation part of total harmonic distortion (THD) is performed in this subtopic .

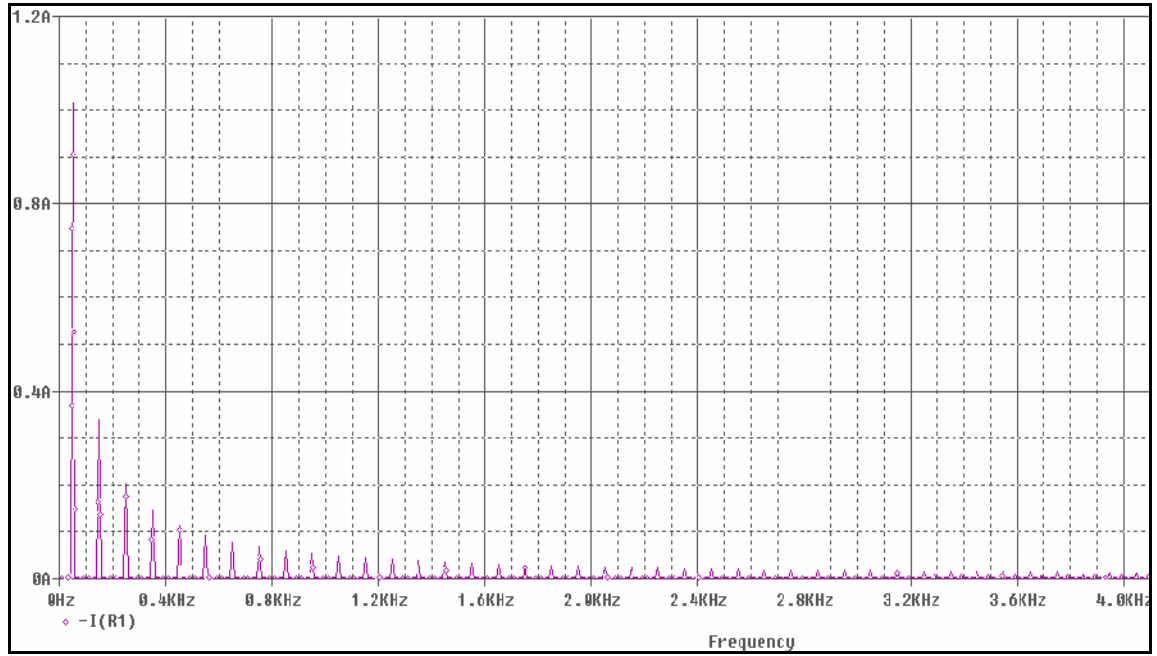


Figure 4.9: THD of Modified Square Wave Inverter

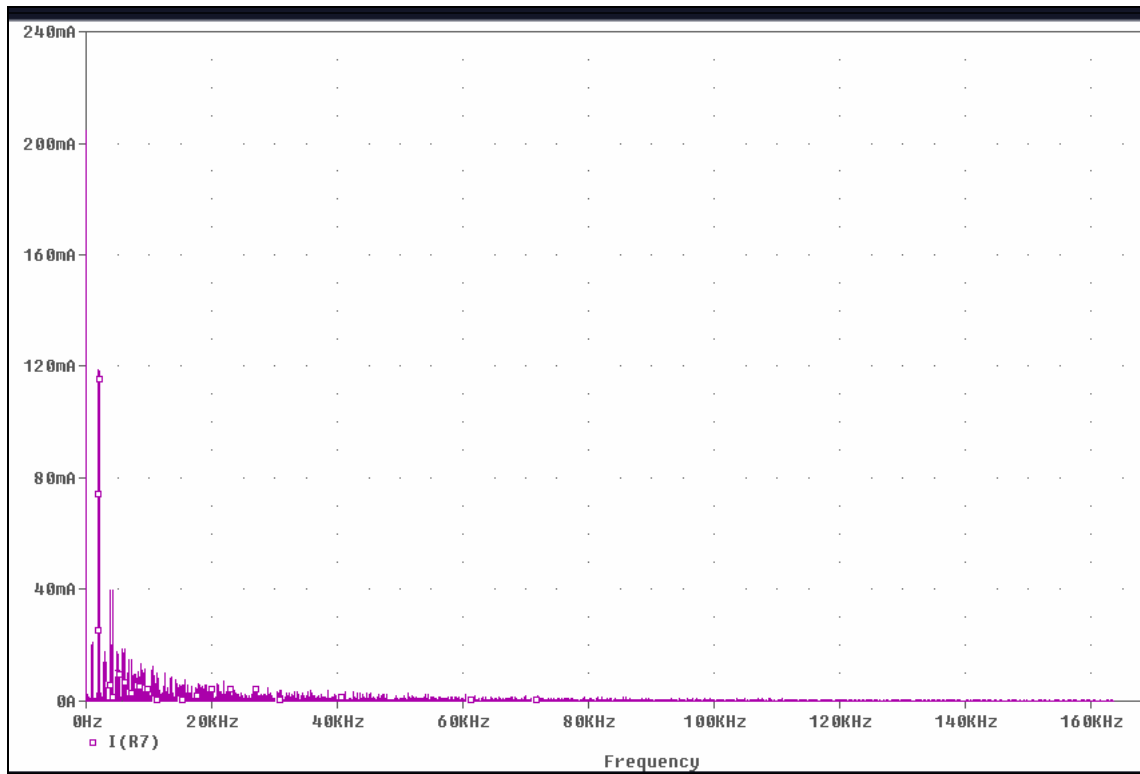


Figure 4.10: THD of SWPM Inverter

By comparing the both figures, the harmonic distortion for modified square wave inverter is high compare to the SPWM inverter with the same loads. The SPWM inverter only has current distortion up to 0.12 A compare to modified square wave inverter that has highest THD 1A. the reducing in THD is really important for AC motor so that it will not breakdown in short time.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

The SPWM inverter is an inverter that converts DC voltage to an AC voltage. In this project, the SPWM output from the PIC microcontroller is succeed to develop. However, the overall objectives are not achieved, where the switching pulses from the controller circuit could not receive by the full bridge inverter circuit. The inverter could not give the desired output result.

5.2 Recommendation

Due to the objectives that could not be accomplished until to the final stage, future development on how to improve the full bridge of hardware circuit should be redesign. The sensitivity of the electronic devices and the PIC microcontroller itself could be the main problems that have to be aware of.

Change the inverter opened loop system to closed loop system. Sensors can be added to the circuit. The load requirements are determined by feedback from sensors to the PWM waveform generation. Try to change the programming language by using C, where the processing of the data could give much better result.

Another improvement can be made to this project is to have additional circuits that will charge batteries when another external AC source is fed to the inverter. This is known as an inverter/charger. A device known as an AC transfer switch is the additional part in this new design. Basically, the inverter will charge the batteries from a generator or other AC source, then passes the AC power through the inverter to the load while the batteries are being charged. When the AC power source is turn off or removed from the inverter, the inverter/charger will automatically returns to functioning as an inverter, outputting it's own AC power.

5.3 Costing and Commercialization

This part explains briefly about the whole costing of the project and the commercialization that could be made and considered.

5.3.1 Costing

This part explains about the costing of this project. The total project cost for all components is estimated to be RM 230.40. The highest cost is reflected in the price in the price of power electronic device such as MOSFET (IRFP 450), MOSFET driver

(IR2110) and high rating fast recovery diode (BYV29-500). Even though the price of these components is expensive, it is still a necessary item and the less expensive substitutes are nonexistent. The component chosen based on the performance of the component, means that the chosen component rating is above designed value. The table of component cost is on Table 5.1.

Table 5.1: The cost of component

Device	Manufacture	Qty	Unit	Unit Cost (RM)	Extended Cost (RM)
IRFP 450	International Rectifier	4		6.50	26.00
IR2110	International Rectifier	2		18.00	36.00
BYV29-500	Philips	2		20.00	40.00
Capacitor ceramic		4	0.1uF	0.20	0.80
Capacitor 50V		2	1uF	0.20	0.40
Capacitor 50V		4	4.7uF	0.40	1.60
Capacitor 50V		2	680uF	2.00	4.00
Capacitor 50V		2	100uF	0.40	0.80
Resistor		2	1.5k Ω	0.10	0.20
Resistor		2	2.7k Ω	0.10	0.20
Resistor		4	10 Ω	0.10	0.40
LM7815	Bay Linear	1		1.50	1.50
LM7805	Bay Linear	1		1.50	1.50
KBPC 610		2		3.00	6.00
Transformer		1	240V - 20V	20.00	20.00
Crystal		1	20MHz	5.00	5.00
18F4550	Microchip	1		40.00	40.00

Touch switch		1		1.50	1.50
Strip board		2		2.00	4.00
Heat sink (small)		4		1.50	6.00
Heat sink (big)		2		8.00	16.00
Plug		1		2.00	2.00
Connector 0384		13		1.50	19.50
Fuse		1	10A	0.30	0.30
3 core cable		1	1m	2.80	2.80
jumper wire		2	1m	0.30	0.60
black red cable		2	1m	0.40	0.80
IC Base		2	14 pin	0.50	1.00
IC Base		1	40 pin	1.00	1.00
IC Base		1	16 pin	0.50	0.50
Potentiometer		1		0.60	0.60
				TOTAL	RM 240.00

5.3.1 Commercialization

The total project cost is RM 230.40. Even though the price is quite expensive and it does not have DC-DC converter component, the price is still considered reasonable because the power rating for the inverter designed is high (up to 1000W). Usually the price of inverter sold in the market based on power rating and it is about RM 1 per watt. The estimated price of DC-DC converter is about RM 300 and if it been added, the full inverter system price is about RM 550. The price of the full system is considered low because it just about half of market price. The cost can be reduced if the inverter is mass-produced.

The size of the inverter designed in this project is large but the size can be reduced by using Printed Circuit Board (PCB) instead of using strip board. It will be an advantage when the designed circuit is small but have same capability with original circuit.

A cost analysis of the different types of inverter shows that sine wave power inverter, though has the best power quality performance, has a big spike in cost per unit power. The standard sine wave in the market has an average efficiency of 85-90%. Power dissipated due to efficiency flaws will be dissipated as heat and the 10-15% power lost in the will shorten operational lifespan of inverters. The quality of the output power could also be improved. It is imperative that the output signal be as clean as possible. Distortion in the output signal leads to a less efficient output and in the case of a square wave , which has a lot of unwanted harmonics, it will damage some sensitive equipment. In designing any type of power supply, it is important to examine the intended market and place the product in a particular niche market.

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APPENDIX A : PIC18F4550 DATASHEET



MICROCHIP PIC18F2455/2550/4455/4550

28/40/44-Pin High-Performance, Enhanced Flash USB Microcontrollers with nanoWatt Technology

Universal Serial Bus Features:

- USB V2.0 Compliant SIE
- Low-speed (1.5 Mb/s) and full-speed (12 Mb/s)
- Supports control, Interrupt, Isochronous and bulk transfers
- Supports up to 32 endpoints (16 bidirectional)
- 1-Kbyte dual access RAM for USB
- On-board USB transceiver with on-chip voltage regulator
- Interface for off-chip USB transceiver
- Streaming Parallel Port (SPP) for USB streaming transfers (40/44-pin devices only)

Power Managed Modes:

- Run: CPU on, peripherals on
- Idle: CPU off, peripherals on
- Sleep: CPU off, peripherals off
- Idle mode currents down to 5.8 μ A typical
- Sleep current down to 0.1 μ A typical
- Timer1 oscillator: 1.1 μ A typical, 32 kHz, 2V
- Watchdog Timer: 2.1 μ A typical
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Five Crystal modes, including High-Precision PLL for USB
- Two External RC modes, up to 4 MHz
- Two External Clock modes, up to 40 MHz
- Internal oscillator block:
 - 8 user selectable frequencies, from 31 kHz to 8 MHz
 - User tunable to compensate for frequency drift
- Secondary oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor
 - Allows for safe shutdown if any clock stops

Peripheral Highlights:

- High current sink/source: 25 mA/25 mA
- Three external interrupts
- Four Timer modules (Timer0 to Timer3)
- Up to 2 Capture/Compare/PWM (CCP) modules:
 - Capture is 16-bit, max. resolution 6.25 ns (Tcy/16)
 - Compare is 16-bit, max. resolution 100 ns (Tcy)
 - PWM output: PWM resolution is 1 to 10-bit
- Enhanced Capture/Compare/PWM (ECCP) module:
 - Multiple output modes
 - Selectable polarity
 - Programmable dead-time
 - Auto-Shutdown and Auto-Restart
- Addressable USART module:
 - LIN bus support
- Master Synchronous Serial Port (MSSP) module supporting 3-wire SPI™ (all 4 modes) and I²C™ Master and Slave modes
- 10-bit, up to 13-channels Analog-to-Digital Converter module (A/D) with programmable acquisition time
- Dual analog comparators with input multiplexing

Special Microcontroller Features:

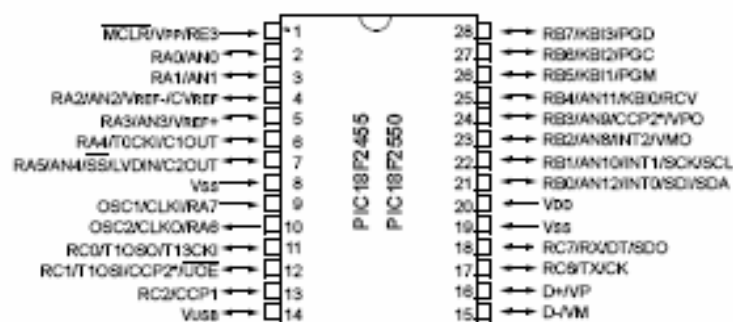
- C compiler optimized architecture with optional extended instruction set
- 100,000 erase/write cycle Enhanced Flash program memory typical
- 1,000,000 erase/write cycle data EEPROM memory typical
- Flash/data EEPROM retention: > 40 years
- Self-programmable under software control
- Priority levels for interrupts
- 8 x 8 Single Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
 - Programmable period from 41 ms to 131s
- Programmable Code Protection
- Single-supply 5V In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via two pins
- Wide operating voltage range (2.0V to 5.5V)

Device	Program Memory		Data Memory		I/O	10-bit A/D (ch)	CCP/ ECCP (PWM)	SPP	MSSP		EUSART	Comparators	Timers 8/16-bit
	FLASH (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)					SPI	Master I ² C			
PIC18F2455	24K	12288	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F2550	32K	16384	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F4455	24K	12288	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3
PIC18F4550	32K	16384	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3

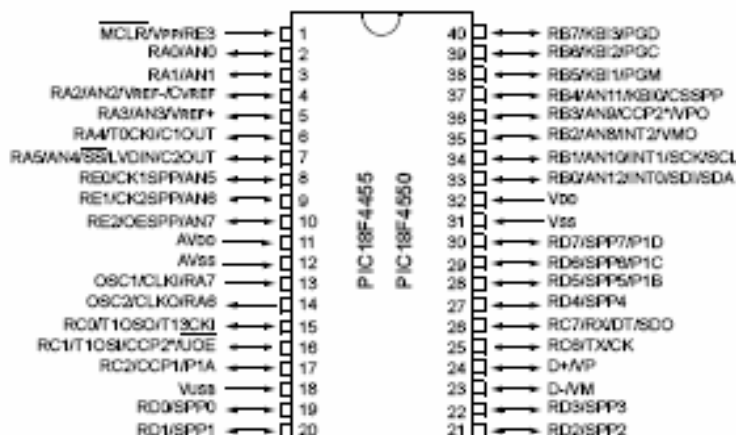
PIC18F2455/2550/4455/4550

Pin Diagrams

28-Pin SDIP, SOIC



40-Pin PDIP

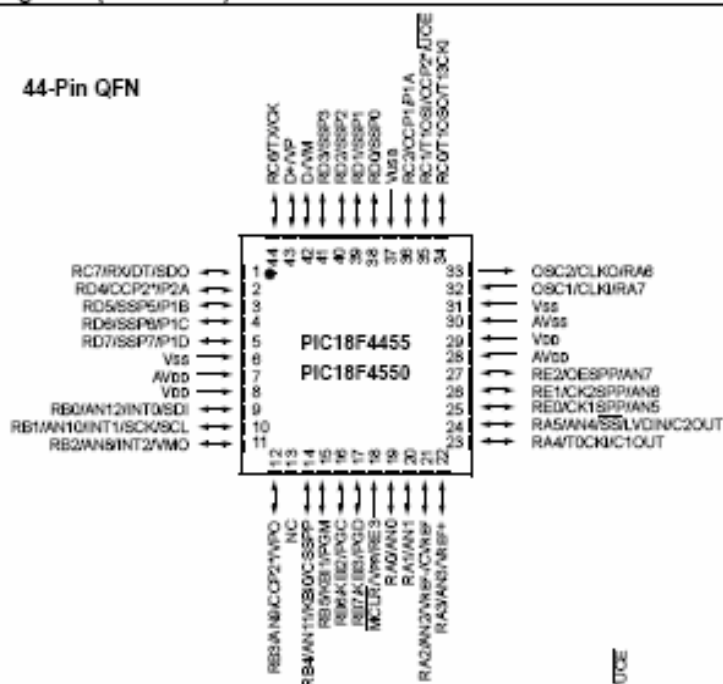


Note: Pinouts are subject to change.

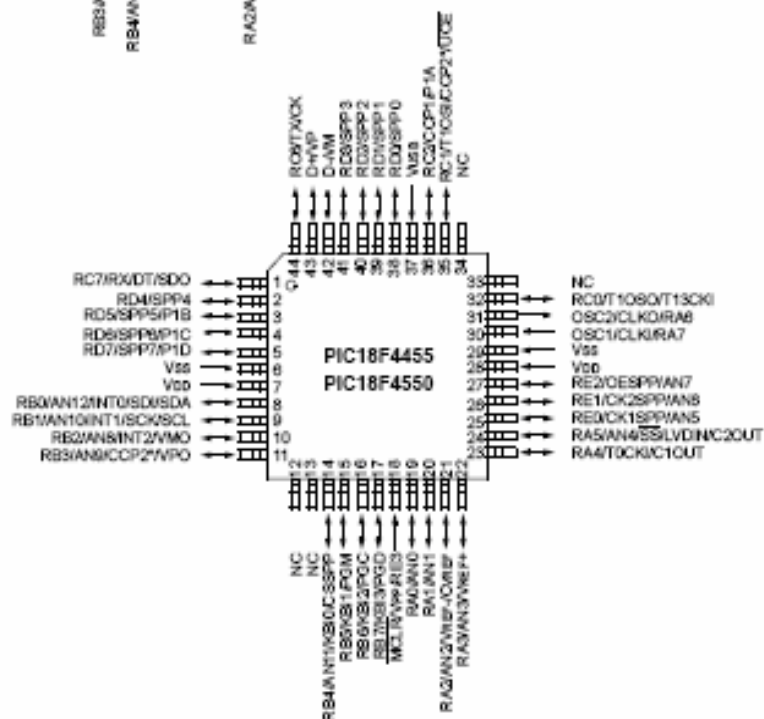
* Assignment of this feature is dependent on device configuration.

Pin Diagrams (Continued)

44-Pin QFN



44-Pin TQFP



Note: Pinouts are subject to change.

* Assignment of this feature is dependent on device configuration.

PIC18F2455/2550/4455/4550

1.0 DEVICE OVERVIEW

This document contains device specific information for the following devices:

- PIC18F2455
- PIC18F2550
- PIC18F4455
- PIC18F4550
- PIC18LF2455
- PIC18LF2550
- PIC18LF4455
- PIC18LF4550

This family of devices offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of high endurance, Enhanced Flash program memory. In addition to these features, the PIC18F2455/2550/4455/4550 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power sensitive applications.

1.1 New Core Features

1.1.1 nanoWatt TECHNOLOGY

All of the devices in the PIC18F2455/2550/4455/4550 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the internal oscillator block, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- **Low Consumption In Key Modules:** The power requirements for both Timer1 and the Watchdog Timer are minimized. See Section 28.0 "Electrical Characteristics" for values.

1.1.2 UNIVERSAL SERIAL BUS (USB)

Devices in the PIC18F2455/2550/4455/4550 family incorporate a fully featured Universal Serial Bus communications module that is compliant with the USB Specification Revision 2.0. The module supports both low-speed and full speed communication for all supported data transfer types. It also incorporates its own on-chip transceiver and 3.3V regulator and supports the use of external transceivers and voltage regulators.

1.1.3 MULTIPLE OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F2455/2550/4455/4550 family offer twelve different oscillator options, allowing users a wide range of choices in developing application hardware. These include:

- Four Crystal modes using crystals or ceramic resonators.
 - Four External Clock modes, offering the option of using two pins (oscillator input and a divide-by-4 clock output) or one pin (oscillator input, with the second pin reassigned as general I/O).
 - An Internal oscillator block which provides an 8 MHz clock ($\pm 2\%$ accuracy) and an INTRC source (approximately 31 kHz, stable over temperature and V_{DD}), as well as a range of 6 user selectable clock frequencies, between 125 kHz to 4 MHz, for a total of 8 clock frequencies. This option frees an oscillator pin for use as an additional general purpose I/O.
 - A Phase Lock Loop (PLL) frequency multiplier, available to both the high-speed crystal and external oscillator modes, which allows a wide range of clock speeds from 4 MHz to 48 MHz.
 - Asynchronous dual clock operation, allowing the USB module to run from a high-frequency oscillator while the rest of the microcontroller is clocked from an internal low-power oscillator.
- Besides its availability as a clock source, the internal oscillator block provides a stable reference source that gives the family additional features for robust operation:
- **Fail-Safe Clock Monitor:** This option constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator block, allowing for continued low-speed operation or a safe application shutdown.
 - **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

PIC18F2455/2550/4455/4550

TABLE 1-1: DEVICE FEATURES

Features	PIC18F2455	PIC18F2550	PIC18F4455	PIC18F4550
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	24576	32768	24576	32768
Program Memory (Instructions)	12288	16384	12288	16384
Data Memory (Bytes)	2048	2048	2048	2048
Data EEPROM Memory (Bytes)	256	256	256	256
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/Compare/PWM Modules	0	0	1	1
Serial Communications	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART
Universal Serial Bus (USB) Module	1	1	1	1
Streaming Parallel Port (SPP)	No	No	Yes	Yes
10-bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Comparators	2	2	2	2
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWR, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWR, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWR, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWR, OST), MCLR (optional), WDT
Programmable Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 63 with Extended Instruction Set enabled	75 Instructions; 63 with Extended Instruction Set enabled	75 Instructions; 63 with Extended Instruction Set enabled	75 Instructions; 63 with Extended Instruction Set enabled
Packages	28-pin PDIP 28-pin SOIC	28-pin PDIP 28-pin SOIC	40-pin PDIP 44-pin QFN 44-pin TQFP	40-pin PDIP 44-pin QFN 44-pin TQFP

APPENDIX B: IRFP 450 DATASHEET-MOSFET



IRFP450

N - CHANNEL 500V - 0.33 Ω - 14A - TO-247
PowerMESH™ MOSFET

TYPE	V _{DS}	R _{DS(on)}	I _D
IRFP450	500 V	< 0.4 Ω	14 A

- TYPICAL R_{DS(on)} = 0.33 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED

DESCRIPTION

This power MOSFET is designed using the company's consolidated strip layout-based MESH OVERLAY™ process. This technology matches and improves the performances compared with standard parts from various sources.

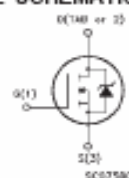
APPLICATIONS

- HIGH CURRENT SWITCHING
- UNINTERRUPTIBLE POWER SUPPLY (UPS)
- DC/DC CONVERTERS FOR TELECOM, INDUSTRIAL, AND LIGHTING EQUIPMENT.



TO-247

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	500	V
V _{DG} R	Drain- gate Voltage (R _{GS} = 20 k Ω)	500	V
V _{GS}	Gate-source Voltage	± 20	V
I _D	Drain Current (continuous) at T _c = 25 °C	14	A
I _D	Drain Current (continuous) at T _c = 100 °C	8.7	A
I _{DM} (*)	Drain Current (pulsed)	56	A
P _{tot}	Total Dissipation at T _c = 25 °C	190	W
	Derating Factor	1.5	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	3.5	V/ns
T _{stg}	Storage Temperature	-65 to 150	°C
T _j	Max. Operating Junction Temperature	150	°C

(*) Pulse width limited by safe operating area

(1) I_{DS} $\leq$ 14 A, di/dt $\leq$ 130 A/ μ s, V_{DS} $\leq$ V_{DSmax}, T_j $\leq$ T_{Jmax}

IRFP450

THERMAL DATA

$R_{th(j-case)}$	Thermal Resistance Junction-case	Max	0.66	°C/W
$R_{th(j-amb)}$	Thermal Resistance Junction-ambient	Max	30	°C/W
$R_{th(c-sink)}$	Thermal Resistance Case-sink	Typ	0.1	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max. Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_J max)	14	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DS} = 50\text{ V}$)	800	mJ

ELECTRICAL CHARACTERISTICS ($T_{case} = 25\text{ °C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)SS}$	Drain-source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ $V_{GS} = 0$	500			V
I_{OSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125\text{ °C}$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$ $I_D = 8.4\text{ A}$		0.33	0.4	Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10\text{ V}$	14			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 8.4\text{ A}$	9.3	13		S
C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$		2600		pF
C_{oss}	Output Capacitance			330		pF
C_{rss}	Reverse Transfer Capacitance			40		pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	$V_{DD} = 250\text{ V}$ $I_D = 7\text{ A}$		24		ns
t_r	Rise Time	$R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 1)		14		ns
Q_g	Total Gate Charge	$V_{DD} = 400\text{ V}$ $I_D = 14\text{ A}$ $V_{GS} = 10\text{ V}$		75		nC
Q_{gs}	Gate-Source Charge			13.5		nC
Q_{gd}	Gate-Drain Charge			27		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Off-voltage Rise Time	$V_{DD} = 400\text{ V}$ $I_D = 14\text{ A}$		15		ns
t_f	Fall Time	$R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 3)		25		ns
t_c	Cross-over Time			35		ns

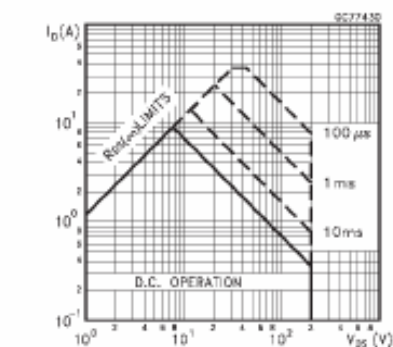
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				14	A
$I_{SDM}^{(*)}$	Source-drain Current (pulsed)				56	A
$V_{SD}^{(*)}$	Forward On Voltage	$I_{SD} = 14\text{ A}$ $V_{GS} = 0$			1.4	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 14\text{ A}$ $dI/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ $T_J = 150^\circ\text{C}$ (see test circuit, figure 3)		680		ns
Q_{rr}	Reverse Recovery Charge			9		μC
I_{RRM}	Reverse Recovery Current			26		A

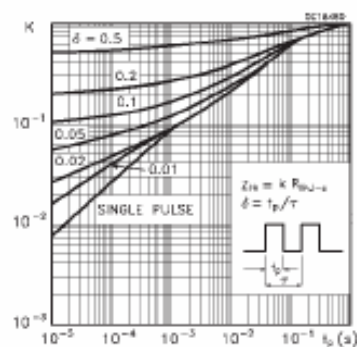
(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(*) Pulse width limited by safe operating area

Safe Operating Area



Thermal Impedance



APPENDIX C : IR2110 DRIVER DATASHEET

International
IR Rectifier

Data Sheet No. PD60147 rev.U

IR2110(-1-2)(S)PbF/IR2113(-1-2)(S)PbF

HIGH AND LOW SIDE DRIVER

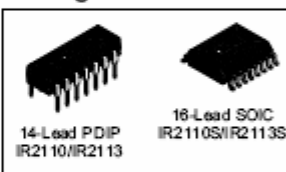
Features

- Floating channel designed for bootstrap operation
- Fully operational to +500V or +600V
- Tolerant to negative transient voltage
- dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
- Separate logic supply range from 3.3V to 20V
- Logic and power ground $\pm 5V$ offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Product Summary

V_{OFFSET} (IR2110)	500V max.
(IR2113)	600V max.
$I_{\text{O+/-}}$	2A / 2A
V_{OUT}	10 - 20V
$t_{\text{on/off}}$ (typ.)	120 & 94 ns
Delay Matching (IR2110)	10 ns max.
(IR2113)	20ns max.

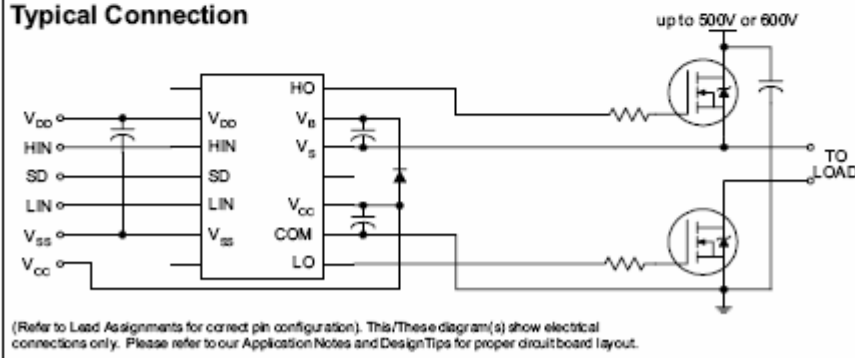
Packages



Description

The IR2110/IR2113 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 or 600 volts.

Typical Connection



www.irf.com

IR2110(-1-2)(S)PbF/IR2113(-1-2)(S)PbF

International
IGR Rectifier

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply voltage (IR2110)	-0.3	525	V
	(IR2113)	-0.3	625	
V_S	High side floating supply offset voltage	$V_B - 25$	$V_B + 0.3$	
V_{HO}	High side floating output voltage	$V_S - 0.3$	$V_B + 0.3$	
V_{CC}	Low side fixed supply voltage	-0.3	25	
V_{LO}	Low side output voltage	-0.3	$V_{CC} + 0.3$	
V_{DD}	Logic supply voltage	-0.3	$V_{SS} + 25$	
V_{SS}	Logic supply offset voltage	$V_{CC} - 25$	$V_{CC} + 0.3$	
V_{IN}	Logic input voltage (HIN, LIN & SD)	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V/ns
dV/dt	Allowable offset supply voltage transient (figure 2)	—	50	
P_D	Package power dissipation @ $T_A \leq +25^\circ\text{C}$ (14 lead DIP)	—	1.6	W
	(16 lead SOIC)	—	1.25	
$R_{\theta JA}$	Thermal resistance, junction to ambient (14 lead DIP)	—	75	$^\circ\text{C/W}$
	(16 lead SOIC)	—	100	
T_J	Junction temperature	—	150	$^\circ\text{C}$
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in figures 36 and 37.

Symbol	Definition	Min.	Max.	Units
V_B	High side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
V_S	High side floating supply offset voltage (IR2110)	Note 1	500	
	(IR2113)	Note 1	600	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side fixed supply voltage	10	20	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{DD}	Logic supply voltage	$V_{SS} + 3$	$V_{SS} + 20$	
V_{SS}	Logic supply offset voltage	-5 (Note 2)	5	
V_{IN}	Logic input voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	$^\circ\text{C}$
T_A	Ambient temperature	-40	125	

Note 1: Logic operational for V_S of -4 to +500V. Logic state held for V_S of -4V to - V_{SS} . (Please refer to the Design Tip DT97-3 for more details).

Note 2: When $V_{DD} < 5V$, the minimum V_{SS} offset is limited to - V_{DD} .

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	7	—	120	150	ns	$V_S = 0V$
t_{off}	Turn-off propagation delay	8	—	94	125		$V_S = 500V/600V$
t_{sd}	Shutdown propagation delay	9	—	110	140		$V_S = 500V/600V$
t_r	Turn-on rise time	10	—	25	35		
t_f	Turn-off fall time	11	—	17	25		
MT	Delay matching, HS & LS turn-on/off	(IR2110) (IR2113)	—	—	—	10 20	

Static Electrical Characteristics

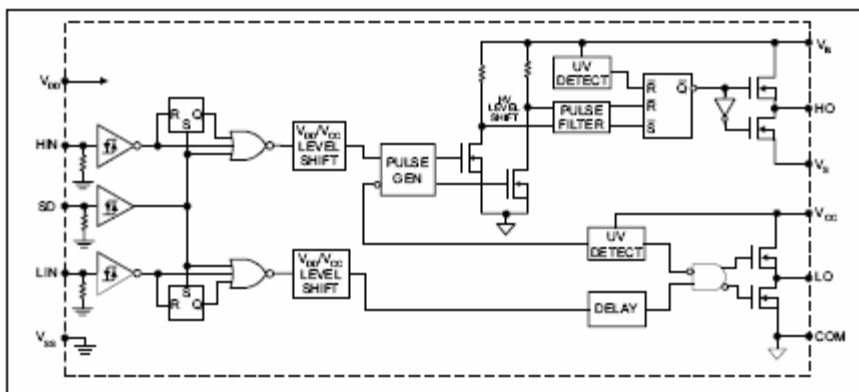
V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IH} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	12	9.5	—	—	V	
V_{IL}	Logic "0" input voltage	13	—	—	6.0		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	14	—	—	1.2		$I_O = 0A$
V_{OL}	Low level output voltage, V_O	15	—	—	0.1		$I_O = 0A$
I_{LK}	Offset supply leakage current	16	—	—	50		$V_B = V_S = 500V/600V$
I_{QBS}	Quiescent V_{BS} supply current	17	—	125	230		$V_{IN} = 0V$ or V_{DD}
I_{QCC}	Quiescent V_{CC} supply current	18	—	180	340	μA	$V_{IN} = 0V$ or V_{DD}
I_{QDD}	Quiescent V_{DD} supply current	19	—	15	30		$V_{IN} = 0V$ or V_{DD}
I_{IN+}	Logic "1" input bias current	20	—	20	40		$V_{IN} = V_{DD}$
I_{IN-}	Logic "0" input bias current	21	—	—	1.0		$V_{IN} = 0V$
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	22	7.5	8.6	9.7	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	23	7.0	8.2	9.4		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	24	7.4	8.5	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	25	7.0	8.2	9.4		
I_{O+}	Output high short circuit pulsed current	26	2.0	2.5	—	A	$V_O = 0V$, $V_{IN} = V_{DD}$ $PW \leq 10 \mu s$
I_{O-}	Output low short circuit pulsed current	27	2.0	2.5	—		$V_O = 15V$, $V_{IN} = 0V$ $PW \leq 10 \mu s$

IR2110(-1-2)(S)PbF/IR2113(-1-2)(S)PbF

International
IR Rectifier

Functional Block Diagram



Lead Definitions

Symbol	Description
VDD	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
VSS	Logic ground
Vb	High side floating supply
HO	High side gate drive output
Vs	High side floating supply return
VCC	Low side supply
LO	Low side gate drive output
COM	Low side return

APPENDIX D : DIODE BYV29

Philips Semiconductors

Product specification

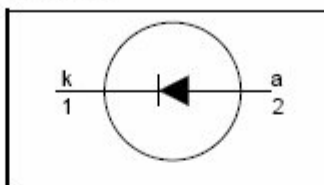
Rectifier diodes
ultrafast

BYV29 series

FEATURES

- Low forward volt drop
- Fast switching
- Soft recovery characteristic
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

$$V_R = 300 \text{ V} / 400 \text{ V} / 500 \text{ V}$$

$$V_F \leq 1.03 \text{ V}$$

$$I_{F(AV)} = 9 \text{ A}$$

$$t_r \leq 60 \text{ ns}$$

GENERAL DESCRIPTION

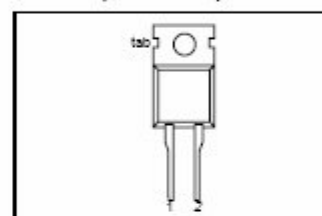
Ultra-fast, epitaxial rectifier diodes intended for use as output rectifiers in high frequency switched mode power supplies.

The BYV29 series is supplied in the conventional leaded SOD59 (TO220AC) package.

PINNING

PIN	DESCRIPTION
1	cathode
2	anode
tab	cathode

SOD59 (TO220AC)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
		BYV29		-300	-400	-500	
V_{RRM}	Peak repetitive reverse voltage		-	300	400	500	V
V_{RRM}	Crest working reverse voltage		-	300	400	500	V
V_R	Continuous reverse voltage		-	300	400	500	V
$I_{F(AV)}$	Average forward current ¹	square wave; $\delta = 0.5$; $T_{mb} \leq 123^\circ\text{C}$	-	9			A
I_{FRM}	Repetitive peak forward current	$t = 25 \mu\text{s}$; $\delta = 0.5$; $T_{mb} \leq 123^\circ\text{C}$	-	18			A
I_{FSM}	Non-repetitive peak forward current	$t = 10 \text{ ms}$	-	100			A
		$t = 8.3 \text{ ms}$ sinusoidal; with reappplied $V_{RRM(max)}$	-	110			A
T_{stg}	Storage temperature		-40	150			$^\circ\text{C}$
T_J	Operating junction temperature		-	150			$^\circ\text{C}$

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th(j-mb)}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th(j-a)}$	Thermal resistance junction to ambient	in free air.	-	60	-	K/W

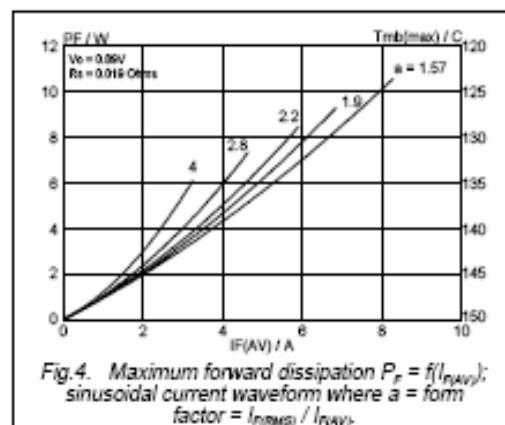
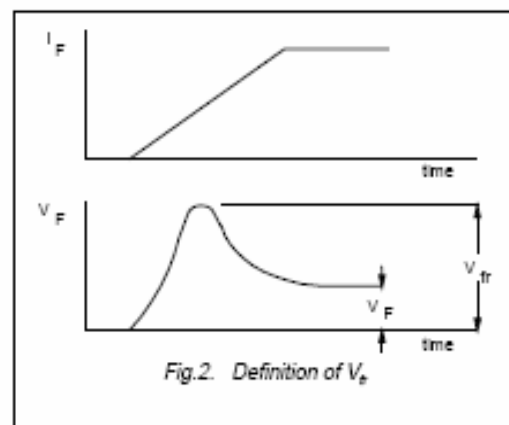
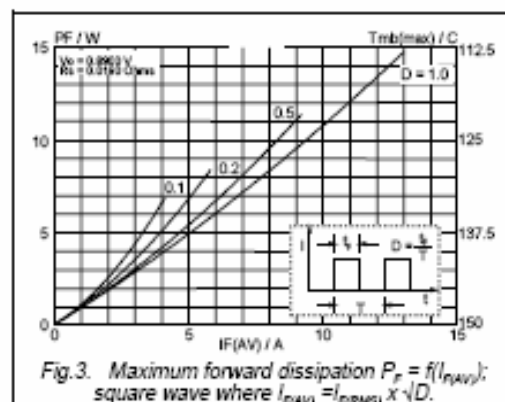
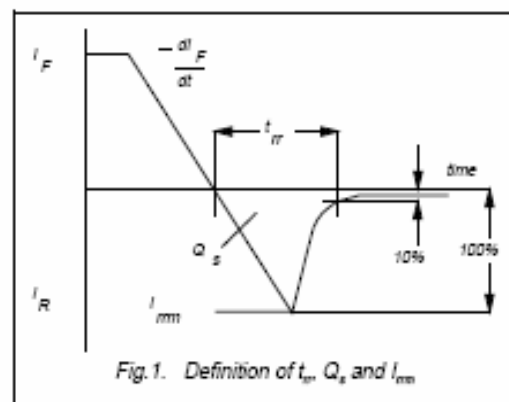
Rectifier diodes
ultrafast

BYV29 series

ELECTRICAL CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_F	Forward voltage	$I_F = 8\text{ A}$; $T_j = 150^\circ\text{C}$	-	0.90	1.03	V
		$I_F = 8\text{ A}$	-	1.05	1.25	V
		$I_F = 20\text{ A}$	-	1.20	1.40	V
I_R	Reverse current	$V_R = V_{RRM}$	-	2.0	50	μA
		$V_R = V_{RRM}$; $T_j = 100^\circ\text{C}$	-	0.1	0.35	mA
Q_s	Reverse recovery charge	$I_F = 2\text{ A}$ to $V_R \geq 30\text{ V}$; $dI_F/dt = 20\text{ A}/\mu\text{s}$	-	40	60	nC
t_{rr}	Reverse recovery time	$I_F = 1\text{ A}$ to $V_R \geq 30\text{ V}$; $dI_F/dt = 100\text{ A}/\mu\text{s}$	-	50	60	ns
I_{rm}	Peak reverse recovery current	$I_F = 10\text{ A}$ to $V_R \geq 30\text{ V}$; $dI_F/dt = 50\text{ A}/\mu\text{s}$; $T_j = 100^\circ\text{C}$	-	4.0	5.5	A
V_F	Forward recovery voltage	$I_F = 10\text{ A}$; $dI_F/dt = 10\text{ A}/\mu\text{s}$	-	2.5	-	V



APPENDIX E: 18F4550 PROGRAMMING CODES

```

* Name      : UNTITLED.BAS
* Author    : [select VIEW...EDITOR OPTIONS]
* Notice    : Copyright (c) 2008 [select VIEW...EDITOR OPTIONS]
*           : All Rights Reserved
* Date      : 10/12/2008
* Version   : 1.0
* Notes     :
*           :
*****

DEFINE osc 20

DEFINE ADC BITS 8
DEFINE ADC CLOCK 3
DEFINE ADC_SAMPLEUS 50

ADCON1 = %00001110 'set use A0 dia configure functions of ports pin
ADCON0 = %11000001 'set which port is used dia control operation of A/D
module

TRISB.1 = 0        'pin 34
TRISB.0 = 0        'pin 33
TRISA.0=1          'INPUT FEEDBACK to set the port direction

pometer VAR WORD

main:
ADCIN 0,pometer
IF pometer=255 THEN 'output of 60hz
GOSUB pwm1
GOSUB pwm2
ENDIF
IF pometer= 0 THEN 'o/p 50 hz
GOSUB pwm3
GOSUB pwm4
ENDIF
IF pometer = 127 THEN 'o/p 40 hz
GOSUB pwm5
GOSUB pwm6
ENDIF
GOTO main

'output for 50hz
pwm1:
'T1
HIGH PORTB.0
PAUSEUS 50
LOW PORTB.0
PAUSEUS 200
'T2
HIGH PORTB.0
PAUSEUS 70

```

```

LOW PORTB.0
PAUSEUS 180
'T3
HIGH PORTB.0
PAUSEUS 90
LOW PORTB.0
PAUSEUS 160
'T4
HIGH PORTB.0
PAUSEUS 140
LOW PORTB.0
PAUSEUS 110
'T5
HIGH PORTB.0
PAUSEUS 170
LOW PORTB.0
PAUSEUS 80
'T6
HIGH PORTB.0
PAUSEUS 190
LOW PORTB.0
PAUSEUS 60 '
'T7
HIGH PORTB.0
PAUSEUS 210 '
LOW PORTB.0
PAUSEUS 40 '
'T8
HIGH PORTB.0
PAUSEUS 110 '
LOW PORTB.0
PAUSEUS 140 '
't9
HIGH PORTB.0
PAUSEUS 70 '
LOW PORTB.0
PAUSEUS 180 '
't10
HIGH PORTB.0
PAUSEUS 50 '
LOW PORTB.0
PAUSEUS 200 '
RETURN
pwm2:
'T1
HIGH PORTB.0
PAUSEUS 50
LOW PORTB.0
PAUSEUS 200
'T2
HIGH PORTB.0
PAUSEUS 70
LOW PORTB.0

HIGH PORTB.0
PAUSEUS 90
LOW PORTB.0
PAUSEUS 160
'T4
HIGH PORTB.0
PAUSEUS 140
LOW PORTB.0
PAUSEUS 110
'T5
HIGH PORTB.0
PAUSEUS 170
LOW PORTB.0
PAUSEUS 80
'T6
HIGH PORTB.0
PAUSEUS 190 '
LOW PORTB.0
PAUSEUS 60 '
'T7
HIGH PORTB.0
PAUSEUS 210 '
LOW PORTB.0
PAUSEUS 40 '
'T8
HIGH PORTB.0
PAUSEUS 110 '
LOW PORTB.0
PAUSEUS 140 '
't9
HIGH PORTB.0
PAUSEUS 70 '
LOW PORTB.0
PAUSEUS 180 '
't10
HIGH PORTB.0
PAUSEUS 50 '
LOW PORTB.0
PAUSEUS 200 '
RETURN

pwm3 : 'o/p Of 40Hz

'T1
HIGH PORTB.0
PAUSEUS 30
LOW PORTB.0
PAUSEUS 170
'T2
HIGH PORTB.0
PAUSEUS 50
LOW PORTB.0

```

```

PAUSEUS 150
'T3
HIGH PORTB.0
PAUSEUS 70
LOW PORTB.0
PAUSEUS 130
'T4
HIGH PORTB.0
PAUSEUS 130
LOW PORTB.0
PAUSEUS 70
'T5
HIGH PORTB.0
PAUSEUS 150
LOW PORTB.0
PAUSEUS 50
'T6
HIGH PORTB.0
PAUSEUS 160
LOW PORTB.0
PAUSEUS 40 '
'T7
HIGH PORTB.0
PAUSEUS 180 '
LOW PORTB.0
PAUSEUS 20 '
'T8
HIGH PORTB.0
PAUSEUS 70 '
LOW PORTB.0
PAUSEUS 130 '
't9
HIGH PORTB.0
PAUSEUS 50 '
LOW PORTB.0
PAUSEUS 150 '

't10
HIGH PORTB.0
PAUSEUS 30 '
LOW PORTB.0
PAUSEUS 170 '
RETURN

```

pwm4:

```

'T1
HIGH PORTB.0
PAUSEUS 30
LOW PORTB.0
PAUSEUS 170
'T2
HIGH PORTB.0
PAUSEUS 50

```

```

LOW PORTB.0
PAUSEUS 150
'T3
HIGH PORTB.C
PAUSEUS 70
LOW PORTB.0
PAUSEUS 130
'T4
HIGH PORTB.C
PAUSEUS 130
LOW PORTB.0
PAUSEUS 70
'T5
HIGH PORTB.C
PAUSEUS 150
LOW PORTB.0
PAUSEUS 50
'T6
HIGH PORTB.C
PAUSEUS 160 '
LOW PORTB.0
PAUSEUS 40 '
'T7
HIGH PORTB.C
PAUSEUS 180 '
LOW PORTB.0
PAUSEUS 20 '
'T8
HIGH PORTB.C
PAUSEUS 70 '
LOW PORTB.0
PAUSEUS 130 '
't9
HIGH PORTB.C
PAUSEUS 50 '
LOW PORTB.0
PAUSEUS 150 '

't10
HIGH PORTB.C
PAUSEUS 30 '
LOW PORTB.0
PAUSEUS 170 '
RETURN

```

pwm5: '60Hz

```

'T1
HIGH PORTB.C
PAUSEUS 250
LOW PORTB.0
PAUSEUS 50
'T2
HIGH PORTB.C

```

```

PAUSEUS 100
LOW PORTB.0
PAUSEUS 200
'T3
HIGH PORTB.0
PAUSEUS 170
LOW PORTB.0
PAUSEUS 130
'T4
HIGH PORTB.0
PAUSEUS 180
LOW PORTB.0
PAUSEUS 120
'T5
HIGH PORTB.0
PAUSEUS 200
LOW PORTB.0
PAUSEUS 100
'T6
HIGH PORTB.0
PAUSEUS 250
LOW PORTB.0
PAUSEUS 50
'T7
HIGH PORTB.0
PAUSEUS 270 '
LOW PORTB.0
PAUSEUS 30 '
'T8
HIGH PORTB.0
PAUSEUS 50 '
LOW PORTB.0
PAUSEUS 150 '
't9
HIGH PORTB.0
PAUSEUS 100 '
LOW PORTB.0
PAUSEUS 200 '

't10
HIGH PORTB.0
PAUSEUS 130 '
LOW PORTB.0
PAUSEUS 170 '
RETURN

```

pwm6:

```

'T1
HIGH PORTB.0
PAUSEUS 250
LOW PORTB.0
PAUSEUS 50

```

```

HIGH PORTB.0
PAUSEUS 100
LOW PORTB.0
PAUSEUS 200
'T3
HIGH PORTB.0
PAUSEUS 170
LOW PORTB.0
PAUSEUS 130
'T4
HIGH PORTB.0
PAUSEUS 180
LOW PORTB.0
PAUSEUS 120
'T5
HIGH PORTB.0
PAUSEUS 200
LOW PORTB.0
PAUSEUS 100
'T6
HIGH PORTB.0
PAUSEUS 250
LOW PORTB.0
PAUSEUS 50 '
'T7
HIGH PORTB.0
PAUSEUS 270 '
LOW PORTB.0
PAUSEUS 30 '
'T8
HIGH PORTB.0
PAUSEUS 50 '
LOW PORTB.0
PAUSEUS 150 '
't9
HIGH PORTB.0
PAUSEUS 100 '
LOW PORTB.0
PAUSEUS 200 '

't10
HIGH PORTB.0
PAUSEUS 130 '
LOW PORTB.0
PAUSEUS 170 '
RETURN

```