

**A STUDY ON THE IMPACT OF PROCESSING
PARAMETERS ON LOW-VOLTAGE POWER
MOSFET**

NUR AQILAH BINTI OTHMAN

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Abstract

Power MOSFET is the most commonly used power device due to its low gate drive power and fast switching speed compared to the existing power bipolar transistor. It features a vertical structure with source and drain on opposite sides of the wafer to support higher current and voltage. The performance of power MOSFET is restricted by the internal resistance. A careful optimisation of the gate width (W_G) is required to minimise the internal resistance. Moreover, the doping concentration of N-epitaxial drift region and its thickness are chosen to obtain the desired breakdown voltage. In the device designed to support low voltage (<50 V), the doping concentration of the P-base region is comparable with the doping concentration of the N-drift region to support part of the applied voltage. The maximum doping concentration of the P-base region must be chosen to attain a threshold voltage for low voltage power MOSFET in the range of 1 – 2 V. In this study, the vital parameters in manufacturing the power VD-MOSFET, such as P-base and N-drift doping concentrations, thickness of N-drift region, and gate width are investigated. The impact of those parameters on the threshold voltage, breakdown voltage and internal on-resistance is recorded and analysed. The VD-MOSFET model used in this study is capable to withstand the breakdown voltage less than 30V. The model is simulated using 2D device and process simulation software from SILVACO; ATLAS and ATHENA. In the simulation, one parameter is varied, while the rest are kept constant. It is shown that, P-base doping concentration is significant in determining the threshold voltage. The threshold voltage is proportional to the P-base doping concentration. On the other hand, the breakdown voltage is inversely proportional to the N-drift doping concentration. Thicker N-drift region may support higher breakdown voltage, but will increase the internal on-resistance.

Abstrak

'Power MOSFET' ialah peranti kuasa yang biasa digunakan kerana ia mempunyai kuasa 'gate' pemanduan rendah dan kelajuan pensuisan yang tinggi berbanding transistor bipolar kuasa. Ia mempunyai struktur menegak dengan 'source' dan 'drain' bertentangan dengan wafer untuk menyokong arus dan voltan yang tinggi. Prestasi 'power MOSFET' ini dihadkan oleh rintangan dalaman. Kelebaran 'gate' (W_G) perlu dioptimumkan secara berhati-hati untuk mengurangkan rintangan dalaman. Selain itu, kepekatan 'doping' pada kawasan 'N-epitaxial drift' dan ketebalannya perlu ditentukan untuk memperolehi voltan kegagalan yang diinginkan. Bagi peranti yang direka untuk menyokong voltan rendah (<50 V), kepekatan 'doping' pada kawasan 'P-base' akan dibandingkan dengan kepekatan 'doping' pada kawasan 'N-drift' bagi menyokong sebahagian daripada voltan yang digunakan. Kepekatan 'doping' maksimum pada kawasan 'P-base' adalah perlu bagi mencapai voltan 'threshold' bagi 'power MOSFET' voltan rendah di antara 1 – 2 V. Di dalam penyelidikan ini, parameter-parameter penting dalam penghasilan 'power VD-MOSFET' seperti kepekatan 'doping' pada kawasan 'P-base' dan 'N-drift', ketebalan kawasan 'N-drift', dan kelebaran 'gate' dikaji. Impak parameter-parameter tersebut ke atas voltan 'threshold', voltan kegagalan dan rintangan dalaman dianalisa dan direkodkan. Model 'VD-MOSFET' yang digunakan di dalam kajian ini mampu menahan voltan kegagalan yang kurang daripada 30 V. Model ini telah disimulasi menggunakan perisian simulasi 2D untuk peranti dan proses daripada SILVACO iaitu ATLAS dan ATHENA. Di dalam simulasi, nilai satu parameter diubah-ubah manakala yang lain dikekalkan. Keputusan menunjukkan bahawa kepekatan 'doping' pada 'P-base' adalah signifikan dalam menentukan voltan 'threshold'. Voltan 'threshold' berkadar terus dengan kepekatan 'doping' pada 'P-base'. Voltan kegagalan pula berkadar songsang dengan kepekatan 'doping' pada 'N-drift'. Kawasan 'N-drift'

yang lebih tebal boleh menyokong voltan kegagalan yang lebih tinggi, tetapi akan meninggikan rintangan dalaman.

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List of Symbols and Abbreviations

a	Width of current flow	$[\mu\text{m}]$
α	Constant	–
BV	Breakdown voltage	$[\text{V}]$
C_{OX}	Specific capacitance of the oxide	$[\text{F}/\text{cm}^2]$
ϵ_s	Dielectric constant of the semiconductor	$[\text{F}/\text{cm}]$
ϵ_{OX}	Dielectric constant of the oxide	$[\text{F}/\text{cm}]$
k	Boltzmann's constant	$[\text{J}/\text{K}]$
K_A	Constant	–
L_{CH}	Channel length	$[\mu\text{m}]$
L_{N^+}	N^+ source width	$[\mu\text{m}]$
n_i	Intrinsic carrier concentration	$[\text{cm}^{-3}]$
N_{D}	N-drift region doping concentration	$[\text{cm}^{-3}]$
N_{DJ}	JFET region doping concentration	$[\text{cm}^{-3}]$
N_{N^+}	N^+ source doping concentration	$[\text{cm}^{-3}]$
N_{P}	P-base doping concentration	$[\text{cm}^{-3}]$
N_{S}	N^+ substrate doping concentration	$[\text{cm}^{-3}]$
N_{r}	Constant	$[\text{cm}^{-3}]$
ρ_{JFET}	Resistivity of JFET region	$[\Omega]$
ρ_{D}	Resistivity of N-drift region	$[\Omega]$
q	Charge of an electron	$[\text{C}]$
t	Thickness of N-drift region	$[\mu\text{m}]$
t_{OX}	Thickness of gate oxide	$[\mu\text{m}]$
t_{SUB}	Thickness of N^+ substrate	$[\mu\text{m}]$
T	Absolute temperature	$[\text{K}]$
μ_{n}	Mobility of electron in silicon	$[\text{cm}^2/\text{Vs}]$
μ_{ni}	Mobility of electron in inversion layer	$[\text{cm}^2/\text{Vs}]$
μ_{nA}	Mobility of electron in accumulation layer	$[\text{cm}^2/\text{Vs}]$
μ_{nb}	Bulk mobility of electron	$[\text{cm}^2/\text{Vs}]$
μ_{min}	Constant	$[\text{cm}^2/\text{Vs}]$

μ_{\max}	Constant	[cm ² /Vs]
V_{bi}	Built-in potential	[V]
V_G	Gate bias voltage	[V]
V_{TH}	Threshold voltage	[V]
W_C	Contact window width	[μm]
W_{Cell}	Cell width / cell pitch	[μm]
W_G	Gate width	[μm]
W_S	N ⁺ source ion implant window width	[μm]
W_{PW}	Polysilicon window width	[μm]
W_0	Zero-bias depletion width	[μm]
x_{JP}	Junction depth of the P-base region	[μm]

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Appendix I:

- 1) Calculation of specific channel resistance.
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CHAPTER 1 : Introduction

1.1 Overview

The power metal oxide semiconductor field effect transistor (MOSFET) has become the standard choice for the main switching devices in a broad range of power conversion applications. With the wide spread use of power MOSFET in the consumer, industrial, medical, and transportation sectors, power MOSFET may contribute an impact on the economy because it determines the cost and efficiency of the systems [Baliga, 2010].

In the 1970s, the power MOSFET product was first introduced by International Rectifier Corporation [Baliga, 2008]. Power MOSFET cannot be fabricated by merely scaling up low-power MOSFET to the desired voltage and current [Chin-yu et al., 1997]. The high-voltage blocking capability requires a large depletion area across the drift-body junction. Thus, power MOSFET structure contains a low-doped epitaxial layer which can support the blocking voltage. The structure is usually fabricated by the double-diffused technique and has a vertical structure, giving rise to the name of vertical-double-diffused power MOSFET (VD-MOSFET).

Power MOSFET initially acclaimed as a replacement for all bipolar power devices due to its high input impedance and fast switching speed for low voltage (<200 V) and high switching speed (>100 kHz) applications, however it failed to seriously contribute in the high voltage field. This is due to the on-state resistance of silicon power MOSFET that increases very rapidly with the increment in the breakdown voltage [Baliga, 2010]. The resulting high conduction loss degrades the efficiency of the overall system.

Therefore in manufacturing the power VD-MOSFET structure, each processing parameter should be handled and optimised wisely. There are lots of important factors to be considered such as doping concentration of P-base region and N-drift region, thickness of drift region, width of gate, and so on. All of these parameters affect the performance and efficiency of the device.

1.2 Background of Study

This study was aimed to investigate the factors influencing the main features of power VD-MOSFET devices, i.e. threshold voltage (V_{TH}), breakdown voltage (BV) and specific on-resistance (R_{ON}). From the literature study, it was found that four processing parameters significantly affecting threshold voltage, breakdown voltage and specific on-resistance. The parameters were P-base doping concentration, N-drift region doping concentration, thickness of drift region and gate width. The target was to determine which parameter possessed the highest influence on the threshold voltage, significantly affecting the breakdown voltage as well as the internal on-resistance. This is important to make sure that the structure has a desired threshold and breakdown voltage, besides low internal on-resistance value to gain maximum performance and efficient.

1.3 Objectives of Study

The objectives of this study are as follows:

- 1) To study the impact of processing parameters (P-base doping concentration, N-drift doping concentration, N-drift region thickness and gate width) on the threshold voltage, breakdown voltage and specific on-resistance of the proposed structure.

- 2) To investigate which parameter has the most significant impact on the threshold voltage, breakdown voltage and specific on-resistance.
- 3) To determine the specific on-resistance of the power VD-MOSFET structure and compare to the ideal on-resistance of the proposed structure.

1.4 Scope and Limitation

This study only involves simulation and theoretical calculations. The experiment on the actual power VD-MOSFET structure is not conducted due to minimal time and no funding. The study was conducted analytically. Since the simulated model is a low voltage power VD-MOSFET (<30 V), the difference in value of the effect of each studied parameter on the breakdown voltage, threshold voltage and specific on-resistance is not so obvious.

1.5 Organisation of the Research Report

This report is organised as follows:

CHAPTER 1 : Introduction

A brief introduction on the power MOSFET, the application and fabrication process of power MOSFET is presented.

CHAPTER 2 : Literature review

In this chapter, the theories relevant to this study are presented. They were reviewed from various books, journals and articles, which are listed in the references section. The theories include the structure and operation of power MOSFET, basic characteristics of

the structure, and so on. Since the determination of specific on-resistance involves many calculations, all the equations involve are presented and discussed in this chapter.

CHAPTER 3 : Methodology

The methodology of the study is discussed in this chapter. The procedures and steps to conduct the simulation are explained. The structure and dimensions of simulated model used in this study are elaborated.

CHAPTER 4 : Results and discussion

The results obtained from the simulation and calculation are presented and discussed in this chapter. Tables and graphs are included to ensure the results can be clearly observed and understood. Subsequent to the tables and graphs are the discussions of the results obtained.

CHAPTER 5 : Conclusions and recommendations

This study is concluded in this chapter where the methodology used and the results obtained are summarised. Moreover, further works that can be conducted are also recommended.

CHAPTER 2 : Literature Review

2.1 Introduction

In the mid-1970s, the VD-MOSFET structure, which was developed using a process known as double-diffusion process, was the first power MOSFET structure commercially introduced by the power semiconductor industry. The channel in the structure was formed by controlling the depth of two junctions. The channel length can be reduced by controlling the diffusion depths of the P-base and N+ source regions instead of opting for the expensive lithography tools [Baliga, 2008].

Power MOSFETs are commonly used in the power electronic circuits that operated at low voltages (<200V). The fast switching speed and sturdiness of the VD-MOSFET structure were significant advantages compared to the performance of the existing power bipolar transistor.

ATHENA and ATLAS are TCAD simulation softwares developed by SILVACO. The structure of the device is implemented in ATHENA by following the production steps in actual manufacturing process of the device. The electrical behaviour of the structure is simulated using ATLAS to study the performances of the device.

In this chapter, brief descriptions of the VD-MOSFET's structure, the device operation, basic characteristics of the device and the device specific on-resistances are presented. Furthermore, the simulation software used in this study is explained.

2.2 Power MOSFETs' Structure and Operation

2.2.1 VD-MOSFET Structure

A cross-section of the basic cell structure for the silicon power vertical-diffused VD-MOSFET is illustrated in Figure 2.1 [Baliga, 2010]. The structure of this device is fabricated starting with an N-type epitaxial layer grown on a heavily doped N^+ substrate. The n-type channel is formed by the difference in lateral extension of the P-base and N^+ source regions produced by their diffusion cycles. Both regions are self-aligned to the left hand-side and right hand-side of the gate region during ion-implantation to introduce the respective dopants. A refractory gate electrode, such as polysilicon, is required to allow diffusion of the dopants under the gate electrode at elevated temperatures.

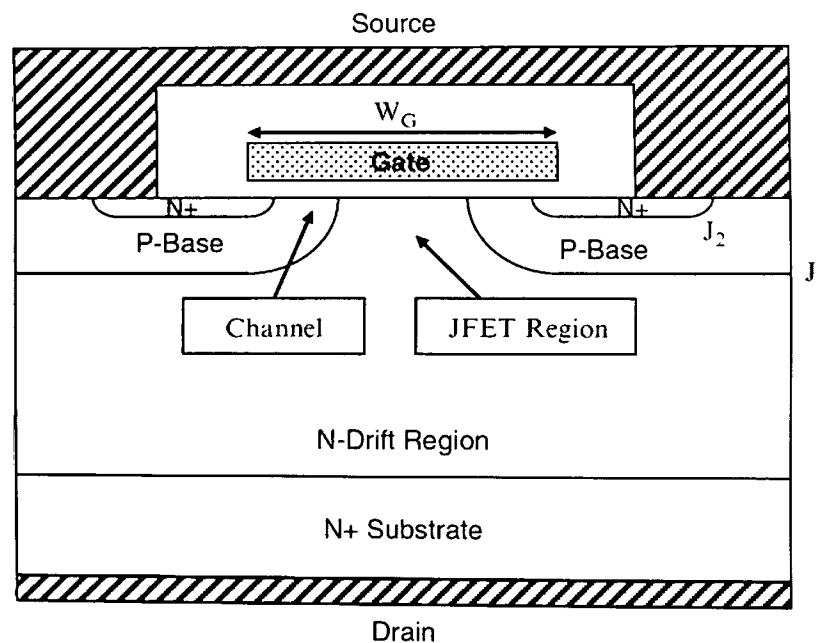


Figure 2.1 : The VD-MOSFET structure [Baliga, 2010].

VD-MOSFET is a vertical architecture structure, which is capable to handle high voltages and currents. In a vertical structure, the two high current-carrying electrodes can be located on the opposite sides of the wafer. It enables the use of thick

source and drain electrodes, which leads to avoiding the transport of the current through thin metal fingers.

The device supports positive voltage applied to the drain across the P-base to N-drift region junction. The doping and thickness of the N-drift region determine the voltage blocking capability. Although low voltage silicon power MOSFET possesses small on-resistances, the drift region resistance increases rapidly with increasing blocking voltage limiting the performance of silicon power VD-MOSFET to less 200 V [Baliga, 2010].

2.2.2 VD-MOSFET Operation

Without the application of a gate bias, a high voltage can be supported in the VD-MOSFET structure when a positive bias is applied to the drain. In this case, junction J_1 (Figure 2.1) formed between the P-base region and N-drift region becomes reversed biased. The voltage is supported mainly within the thick lightly doped N-drift region. Drain current flow in the D-MOSFET structure is induced by the application of a positive bias to the gate electrode. This produces an inversion layer at the surface of the P-base region under the gate electrode. This inversion layer channel provides a path for transporting electrons from the source to the drain when a positive drain voltage is applied.

After transport from the source region through the channel, the electrons enter the N-drift region at the upper surface of the device structure. They are then transported through a relatively narrow JFET region located between the adjacent P-base regions within the VD-MOSFET structure. The constriction of the current flow through the JFET region substantially increases the internal resistance of the VD-MOSFET structure. A careful optimization of the gate width is required, in order to minimise the

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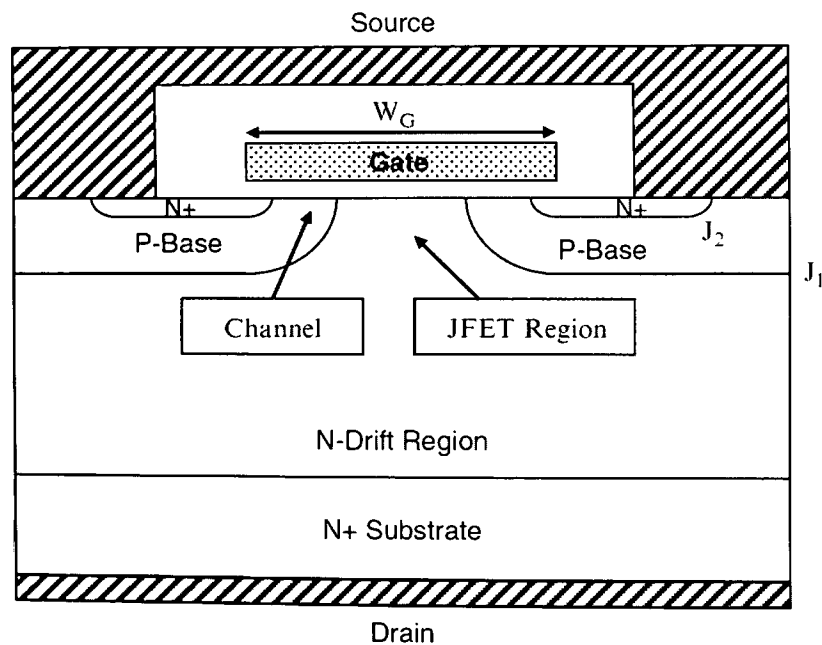


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internal resistance for this structure [Baliga, 2008]. In addition, it is customary to enhance the doping concentration in the JFET region to reduce the resistance to current flow through this portion of the device structure.

After being transported through the JFET region, the electrons enter the N-drift region below junction J_1 . The current spreads from the relatively narrow JFET region to the entire width of the cell cross-section. This non-uniform current distribution within the drift region enhances its resistance making the internal resistance of the VD-MOSFET structure larger than the ideal specific on-resistance of the drift region.

2.2.3 Other Structures of Power MOSFET

The large internal resistance for the VD-MOSFET structure has provided motivation for the development of the trench-gate power MOSFET structure in the 1990s. This structure was developed due to availability of the technology for etching trenches that has evolved for dynamic random access memory (DRAM) applications. The trench-gate or U-MOSFET structure offered opportunity to reduce the internal resistance of the power MOSFET closer to the ideal value by elimination of a JFET region within the VD-MOSFET structure [Baliga, 2010]. The optimization of this structure also enables increasing the operating frequency for power MOSFET to the 1-MHz range.

Figure 2.2 shows the trench extends from the upper surface of the structure through the N^+ source and P-base region into the N-drift region [Baliga, 2008]. The gate electrode is placed within the trench after the formation of the gate oxide by thermal oxidation of the bottom and sidewalls.

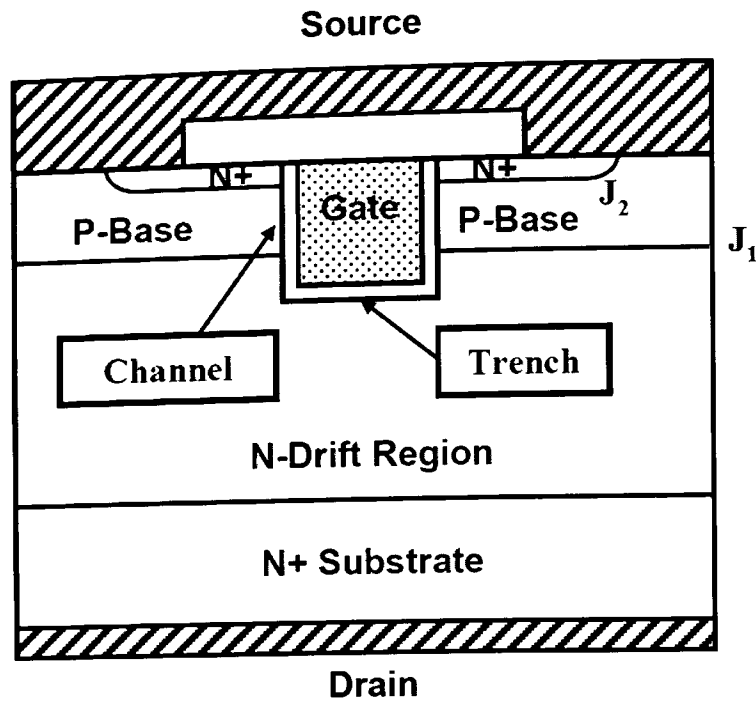


Figure 2.2 : U-MOSFET structure [Baliga, 2008].

Besides U-MOSFET, there are more structures of power MOSFET that have been developed such as shielded-channel power MOSFET (SC-MOSFET), charge-coupling power MOSFET (CC-MOSFET), super-junction power MOSFET (SJ-MOSFET) and so forth [Baliga, 2010]. Each of the newly developed structure contains improvements to become the ideal power MOSFET. However this will not be discussed further in this study.

2.3 Basic Device Characteristics

2.3.1 Transfer Characteristics

Current flow between the source and drain electrodes can occur through the power MOSFET structure when the gate bias exceeds the threshold voltage. For a constant drain bias voltage in excess of the pinch-off voltage for the channel, the saturated drain current, $I_{D,sat}$ is related to the gate voltage by Equation 2.1