

## 6 PULSE GTO THYRISTOR CONVERTER SIMULATION

MOHAMAD FADZLI BIN ABDUL RAHMAN

UNIVERSITI MALAYSIA PAHANG

# UNIVERSITI MALAYSIA PAHANG

## BORANG PENGESAHAN STATUS TESIS♦

JUDUL: **6 PULSE GTO THYRISTOR CONVERTER SIMULATION**

SESI PENGAJIAN: 2008/2009

Saya MOHAMAD FADZLI BIN ABDUL RAHMAN (850223-09-5053)  
(HURUF BESAR)

mengaku membenarkan tesis (Sarjana Muda/~~Sarjana~~ /~~Doktor Falsafah~~)\* ini disimpan di Perpustakaan dengan syarat-syarat kegunaan seperti berikut:

1. Tesis adalah hakmilik Universiti Malaysia Pahang (UMP).
2. Perpustakaan dibenarkan membuat salinan untuk tujuan pengajian sahaja.
3. Perpustakaan dibenarkan membuat salinan tesis ini sebagai bahan pertukaran antara institusi pengajian tinggi.
4. \*\*Sila tandakan ( ✓ )

**SULIT**

(Mengandungi maklumat yang berdarjah keselamatan atau kepentingan Malaysia seperti yang termaktub di dalam AKTA RAHSIA RASMI 1972)

**TERHAD**

(Mengandungi maklumat TERHAD yang telah ditentukan oleh organisasi/badan di mana penyelidikan dijalankan)

**TIDAK TERHAD**

Disahkan oleh:

\_\_\_\_\_  
(TANDATANGAN PENULIS)

\_\_\_\_\_  
(TANDATANGAN PENYELIA)

Alamat Tetap:

**BATU 6 ¼, JALAN PADANG  
MELANGIT, 02400 KANGAR  
PERLIS.**

**MUHAMAD ZAHIM BIN SUJOD**  
( Nama Penyelia )

Tarikh: **04 MEI 2009**

Tarikh: : **04 MEI 2009**

- CATATAN:
- \* Potong yang tidak berkenaan.
  - \*\* Jika tesis ini SULIT atau TERHAD, sila lampirkan surat daripada pihak berkuasa/organisasi berkenaan dengan menyatakan sekali tempoh tesis ini perlu dikelaskan sebagai atau TERHAD.
  - ♦ Tesis dimaksudkan sebagai tesis bagi Ijazah doktor Falsafah dan Sarjana secara Penyelidikan, atau disertasi bagi pengajian secara kerja kursus dan penyelidikan, atau Laporan Projek Sarjana Muda (PSM).

“I hereby acknowledge that the scope and quality of this thesis is qualified for the award of the Bachelor Degree of Electrical Engineering (Power Systems)”

Signature : \_\_\_\_\_

Name : MUHAMAD ZAHIM SUJOD

Date : 04 MAY 2009

## 6 PULSE GTO THYRISTOR CONVERTER SIMULATION

MOHAMAD FADZLI BIN ABDUL RAHMAN

This thesis is submitted as partial fulfillment of the requirements for the award of the  
Bachelor of Electrical Engineering (Power Systems)

Faculty of Electrical & Electronics Engineering  
Universiti Malaysia Pahang

MAY, 2009

“All the trademark and copyrights use herein are property of their respective owner. References of information from other sources are quoted accordingly; otherwise the information presented in this report is solely work of the author.”

Signature : \_\_\_\_\_

Author : MOHAMAD FADZLI BIN ABDUL RAHMAN

Date : 04 MAY 2009

To my beloved mother, father, and brothers

## **ACKNOWLEDGEMENT**

In the name of Allah, The Most Loving and The Most Compassionate

I would like to take this opportunity to extend my deepest gratitude to the following persons who helped me a lot in this project, which enabled me to complete my research project in time as a partial of the requirement for the Bachelor of Electrical Engineering (Power Systems).

First and foremost, a special thank to my supervisor En. Muhamad Zahim Sujod, who helped me a lot to complete this project with all the support, continuous patience, and supervision given throughout the project.

I would like to give my appreciation to my parents and family for supporting me, financially and mentally from the early stage of my studies. Their support is indeed very much appreciated from the bottom of my heart.

Last but not least, thank you to my colleagues with their encouragement and help for me to finish this project.

## **ABSTRACT**

Nowadays, the development of a large capacity Gate Turn Off (GTO) thyristor has made it possible to manufacture self-commutated converter employing GTO thyristor for power applications. This project focused on the design of GTO thyristor model by using PSPICE, the analysis of switching waveform of GTO thyristor and the implementation of GTO thyristor as a control element in 6 pulse converter circuit. This project also includes the explanations of the settings of operation condition and gate circuit parameters including firing angle and time delay of turn-on and turn-off pulses. Simulation results of dc output voltage are compared with mathematical calculation results, and it is shown that almost similar characteristics curves are obtained.



## ABSTRAK

Dewasa ini penghasilan *Gate Turn Off (GTO) thyristor* dengan kapasitas yang besar memungkinkan pengilang untuk menghasilkan *converter* yang mampu mengekal atau mengubah arah arus sendirinya dengan menggunakan *GTO thyristor* untuk aplikasi sistem kuasa. Projek ini memfokuskan pada membina model *GTO thyristor* menggunakan perisian *PSPICE* dan menjalankan analisis ke atas gelombang penyambung atau pemutus litar *GTO thyristor*. Model ini juga kemudiannya akan diimplankan kedalam litar *6 pulse converter* sebagai elemen pengawal. Projek ini juga menerangkan tentang penetapan kondisi operasi dan nilai-nilai pada litar pintu termasuklah sudut pancaran dan masa tangguhan pada kondisi buka dan kondisi tutup *GTO thyristor*. Keputusan voltan keluar arus terus dari simulasi kemudiannya akan dibandingkan dengan keputusan dari pengiraan matematik yang akhirnya akan menunjukkan bahawa keputusan yang hampir sama didapati.

## TABLE OF CONTENTS

CHAPTER	TITLE	PAGE
	TITLE PAGE	i
	DECLARATION	ii
	DEDICATION	iii
	ACKNOWLEDGEMENT	iv
	ABSTRACT	v
	ABSTRAK	vi
	TABLE OF CONTENTS	vii
	LIST OF TABLES	ix
	LIST OF FIGURES	x
	LIST OF ABBREVIATIONS	xi
	LIST OF SYMBOLS	xii
<b>1</b>	<b>INTRODUCTION</b>	1
	1.1 Background	1
	1.2 Project objective	2
	1.3 Project scope	2
	1.4 Thesis outline	3
<b>2</b>	<b>LITERATURE REVIEW</b>	4
	2.1 Gate Turn-off Thyristors (GTO's or Latching Transistors)	4

2.2	Basic structure	4
2.3	Switching performance	7
2.3.1	Gate turn-on	8
2.3.2	Gate turn-off	9
2.4	GTO characteristics	12
2.5	GTO gate drive circuits	13
2.5.1	Various-off gating circuits	14
2.5.2	Gate drive for high power GTO's	17
2.6	Snubber circuits	18
2.7	Overcurrent protection of GTO's	19
2.8	Paralleling of GTO's	21
<b>3</b>	<b>METHODOLOGY</b>	<b>24</b>
3.1	Introduction	24
3.2	GTO thyristor model	26
3.3	6 pulse converter circuit	28
<b>4</b>	<b>RESULTS AND ANALYSIS</b>	<b>30</b>
4.1	Introduction	30
4.2	The simulation results	30
4.2.1	The GTO thyristor model	30
4.2.2	6 pulse converter circuit	35
4.3	The mathematical calculation and comparison	39
4.4	Summary	42
<b>5</b>	<b>CONCLUSION AND RECOMMENDATIONS</b>	<b>43</b>
5.1	Conclusion	43
5.2	Future recommendations	43
5.3	Costing and commercialization	44
	<b>REFERENCES</b>	<b>45</b>

**LIST OF TABLES**

<b>TABLE NO.</b>	<b>TITLE</b>	<b>PAGE</b>
3.1	Operation circuit parameters of GTO thyristor model	27
3.2	Total cost on the development of the security system	28
4.1	Storage time, fall time, tail time and turn-off time for a different anode current	34
4.2	Result	40

## LIST OF FIGURES

FIGURE NO.	TITLE	PAGE
2.1	Circuit symbols	5
2.2	Two-transistor analogy of GTO	6
2.3	Basic GTO structure showing anode to N-base short-circuitry spots	7
2.4	Basic gate-drive circuit for a GTO	8
2.5	Delay, rise and turn-on times during gated turn-on	9
2.6	Basic GTO switching circuit with a clamped inductive load	10
2.7	Voltage and current waveforms during turn-off of a GTO	11
2.8	Various off-gating circuits	16, 17
2.9	Gate drive for high power GTO's	18
2.10	Connection is direct paralleling of GTO's	22
2.11	Switching waveforms of parallel devices	23
3.1	Flow chart of the project	25
3.2	Two transistor model	26
3.3	GTO thyristor model and it's operation circuit	27
3.4	6 pulse converter circuit	29
4.1	GTO thyristor model circuit	31
4.2	Turn-on and turn-off characteristics of GTO thyristor with different $I_d$	32,33,34
4.3	6 pulse converter circuit	35
4.4	Result of 6 pulse converter circuit with different firing angle	36,37,38
4.5	DC output voltage vs firing angle	41

## LIST OF ABBREVIATIONS

GTO	-	Gate Turn Off
SCR	-	Silicon Controlled Rectifier
AC	-	Alternating Current
DC	-	Direct Current
HVDC	-	High Voltage Direct Current
PSPICE	-	Personal Simulation Program with Integrated Circuit Emphasis
MOSFET	-	Metal-Oxide-Semiconductor Field-Effect Transistor

**LIST OF SYMBOLS**

$\mu$	-	Micro
K	-	Kilo
Hz	-	Hertz
$\Omega$	-	Ohm
m	-	Milli
V	-	Volts
R	-	Resistor
W	-	Watt
L	-	Inductor
H	-	Henry
$^{\circ}$	-	Degree
$\alpha$	-	Firing angle

## CHAPTER 1

### INTRODUCTION

#### 1.1 Background

As far as we all know, early distribution was by direct current (dc). Then the transformer was developed so that alternating current (ac) became the universal choice for generation, transmission, distribution and operation. However during the last 40 years, many high voltage direct current (hvdc) systems have been built with the systems that are fully integrated into the adjoining ac systems and in some instance are fully embedded in ac systems.

Using hvdc system, the power flow can be controlled rapidly and accurately as to both the power level and the direction. The hvdc converter consists of many types of circuits, for example a 12 pulse converter connected to the ac system through the converter transformer. Harmonic filters are provided on the ac and dc sides of the converter as required to limit interference to acceptable levels.

Conventional thyristor (known as SCR) has being used in various applications such as in power converter of hvdc transmission system and as a dc speed controller for dc motor application.

Conventional thyristor can only be turned on with two conditions, that is when the device is in forward blocking state or when positive gate current is applied at the gate. This thyristor cannot be turned off by applying negative gate current. It



can only be turned off if anode current goes negative (reverse). This happens when negative portion of the sine wave occurs (natural commutation). Another method of turning off is known as “forced commutation” where anode current is “diverted” to another circuitry.

The disadvantage of conventional thyristor can be overcome by using GTO thyristor. GTO thyristor behave like conventional thyristor, but can be turned off using gate signal. It needs very large reverse gate current (normally  $1/5$  of anode current) to turn-off. Since a GTO thyristor converter is self-commutated, it can be used to supply power to a weak ac system, and even to a “load-only” system. At the same time, it is able to control reactive power from lead to lag to keep an ac bus voltage constant.

## **1.2 Project objective**

The objective of this project is to design GTO thyristor model by using PSPICE, the analysis of switching waveform of GTO thyristor and the implementation of GTO thyristor as a control element in 6 pulse converter circuit.

## **1.3 Project scope**

The scope of this project is to make a simulation of 6 pulse GTO thyristor converter simulation, then make an analysis of switching waveform of GTO thyristor and the implementation of GTO thyristor as a control element in 6 pulse converter circuit. This also includes the explanations of the settings of operation condition, gate circuit parameters, firing angle and time delay of turn-on and turn-off pulses. Simulation results of dc output voltage are compared with mathematical calculation results.

## **1.4 Thesis outline**

Chapter 1 outlines the background of high voltage direct current (hvdc) systems followed by conventional thyristor and GTO thyristor. This chapter also explains about the project objective and the scope of this project.

Chapter 2 outlines the literature review of this project. This chapter explains the fundamental of the GTO thyristor such as basic structure, switch performance, characteristics and turn-on and turn-off time.

Chapter 3 outlines the methodologies used in this project to perform the simulation. It briefs about the designation of GTO thyristor model, the operation circuit for the model and the implementation of the GTO thyristor model with its operation circuit in the 6 pulse converter circuit.

Chapter 4 outlines the result obtained from simulation and mathematical calculation. Both of the results are compared to each other to determine either the simulation result is the same with the calculation result or not. Then the analysis of the result is performed.

Chapter 5 concludes this project together with a future recommendation. There are also a brief discussion covering about the cost of the project and the probability of project commercialization.

## CHAPTER 2

### LITERATURE REVIEW

#### 2.1 Gate Turn-off Thyristors (GTOs or Latching Transistors)

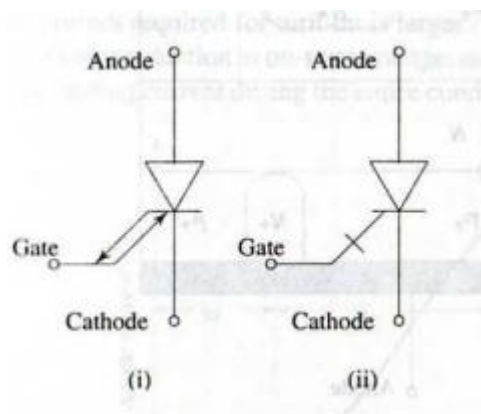
A previous chapter describes the thyristor and their use in power electronic applications. Also, we have seen that thyristors can block high voltage (several thousand volts) in the off-state and conduct large currents (several thousand amperes) in the on-state with only a small on-state voltage drop (a few volts). The most useful of all is their capability of being switched on when desired by means of a control signal applied at the gate of the thyristors. However, as we know that once an SCR is turned on by the gate signal, the gate loses control and it can be brought back to the blocking state only by reducing the forward current to a level below that of the holding current. This is the serious deficiency in thyristors that prevent their use in switch mode applications. This section describes the structure and operation of thyristors that have a gate turn-off capability, the so-called gate turn-off thyristors or GTOs

#### 2.2 Basic Structure

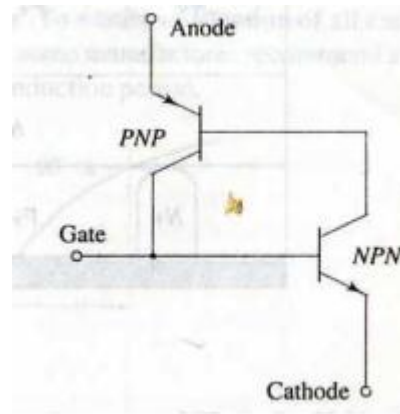
The gate turn-off thyristor (GTO) incorporates many of the advantages of the conventional thyristor and the high-voltage switching transistor. It is a *PNPN* device that can be triggered into conduction by a small positive gate-current

pulse, but also has the capability of being turned-off by a negative gate-current pulse. However, the turn-off current gain is low (typically 4 or 5). For example, a 4000 V, 3000 A device may need -750 A gate current to turn it off. This facility allows the construction of inverter circuits without the bulky and expensive forced commutating components associated with conventional thyristor circuitry. The GTO also has a faster switching speed than the regular thyristor, and it can withstand higher voltage and current than the power transistor or MOSFET.

The GTO is a three-terminal device with anode, cathode and gate terminals. The various circuit symbols are shown in Figure 2.1. The two-way arrow convention (Figure 2.1(i)) on the gate lead distinguishes the GTO from the conventional thyristor. Figure 2.2 shows the two-transistor analog of the GTO. Like the conventional thyristor, the GTO switches regeneratively into the on-state when a positive gating signal is applied to the base of the *N-P-N* transistor. In a regular thyristor, the current gains of the *N-P-N* and *P-N-P* transistors are large in order to maximize gate sensitivity at turn-on and to minimize on-state voltage drop. But this pronounced regenerative. Latching effect means that the thyristor cannot be turned-off at the gate. Internal regeneration is reduced in the GTO by a



**Figure 2.1** Circuit symbols



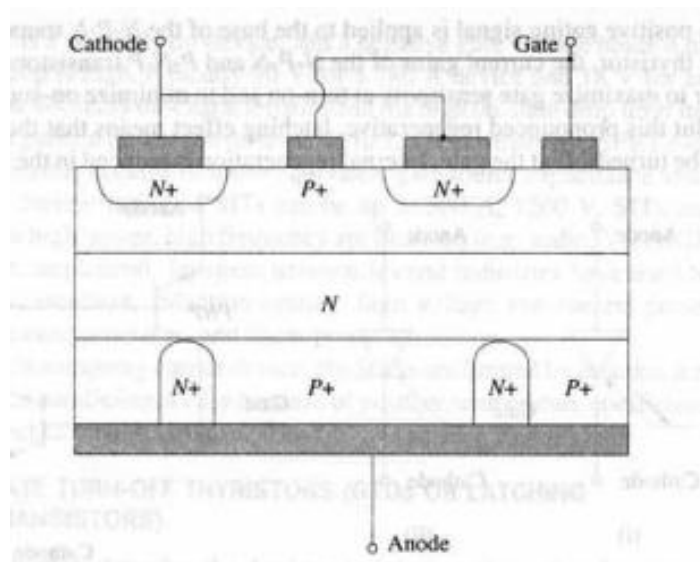
**Figure 2.2** Two-transistor analogy of GTO

reduction in the current gain of the  $P-N-P$  transistor, and turn-off is achieved by drawing sufficient current from the gate. The turn-off action may be explained as follows. When a negative bias is applied at the gate, excess carriers are drawn from the base region of the  $N-P-N$  transistor, and the collector current of the  $P-N-P$  transistor is diverted into the external gate circuit. Thus, the base drive of the  $N-P-N$  transistor is removed and this, in turn, removes the base drive of the  $P-N-P$  transistor, and stops conduction.

The reduction in gain of the  $P-N-P$  transistor can be achieved by the diffusion of gold or other heavy metal to reduce carrier lifetime, or by the introduction of anode to N-base short-circuiting spots, as in Figure 2.3, or by a combination of these two techniques. Device characteristics are influenced by the particular technique used. Thus, the gold-doped GTO retains its reverse-blocking capability but has a high on-state voltage drop. The shorted anode emitter construction has a lower on-state voltage, but the ability to block reverse voltage is sacrificed. Large GTO does also have an interdigitated gate-cathode structure in which the cathode emitter consists of many parallel connected N-type fingers diffused into the P-type gate region, as in Figure 2.3. This configuration ensures a simultaneous turn-on or turn-off of the whole active area of the chip.

GTO's are available with symmetric or asymmetric voltage blocking capabilities. A symmetric blocking device cannot have anode shorting and, therefore, is somewhat slower. The use of asymmetrical GTO's requires the

connection of a diode in series with each GTO to gain the reverse blocking capability, whereas symmetrical GTO's have the ability to block a reverse voltage. In symmetrical GTO's, N-base is doped with a heavy metal to reduce the turn-off time. The asymmetrical GTO's offer more stable temperature characteristics and lower on-state voltage compared to symmetrical GTOs.

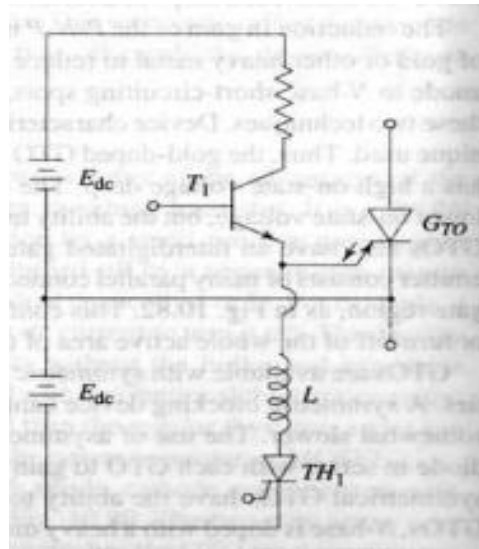


**Figure 2.3** Basic GTO structure showing anode to N-base short-circuiting spots

### 2.3 Switching Performance

The simplified gate drive circuit of Figure 2.4 shows separate dc supplies for turn-on and turn-off. The GTO is gated into conduction by means of transistor  $T_1$  in the turn-on circuit. The switching device in the turn-off circuit should have a high peak current capability. An auxiliary thyristor or MOSFET is appropriate for this duty. Figure 2.4 shows an auxiliary SCR,  $TH_1$ , which is gated to initiate the turn-off process. Turn-off performance may be enhanced by the presence of some series inductance,  $L$ , as shown. The voltage supply for the turn-off circuit is in the region of 10 to 20 V and the gate current at turn-off, applied for few microseconds, is typically about one-fifth of the anode current prior to turn-off. Consequently, the

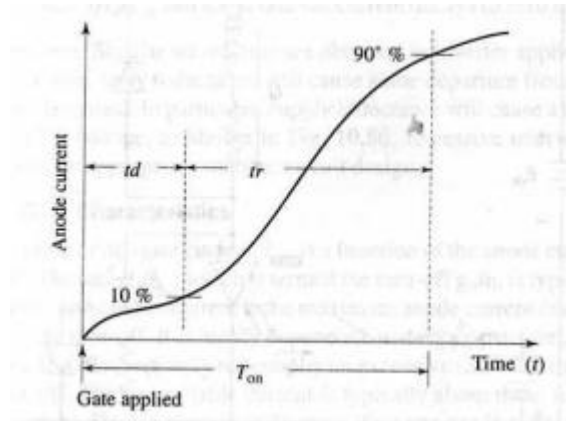
energy required to turn off the GTO is much less than that needed to turn-off a conventional thyristor.



**Figure 2.4** Basic gate-drive circuit for a GTO

### 2.3.1 Gate turn-on

The gate turn-on mechanism of the GTO is similar to that of a conventional thyristor. A steep-fronted pulse of gate current turns-on the device, and gate drive can be removed without the loss of conduction when the anode current exceeds the latching current level. However the anode current of the GTO does not respond immediately to the applied gate signal. The turn-on response of the anode current is characterized by a turn-on time,  $T_{on}$ , which consists of a delay time,  $t_d$  and a rise time,  $t_s$ , as shown in Figure 2.5. Turn-on time is reduced by increasing forward gate current as in a conventional thyristor, but because the regenerative effect is reduced in the GTO, the gate drive current required for turn-on is larger. To ensure conduction of all cathode fingers and a reduction in on-state voltage, some manufactures recommend a continuous gating current during the entire conduction period.



**Figure 2.5** Delay, rise and turn-on times during gated turn-on

For high frequency applications, a short turn-on time, especially a short rise time is required to reduce the switching power loss. The power loss dissipated during the delay-time is negligible because of the low anode current.

The GTO is expected to have a faster turn-on time than the conventional thyristor because of its narrower emitter width. The delay time decreases with increasing gate current, while the rise time does not vary so far as the gate current is much smaller than the anode current in the on-state. However, for larger gate drive, the rise time also decreases. The turn-on time also depends upon the rising rate of the gate current; the faster the rising rate, the shorter the turn-on time.

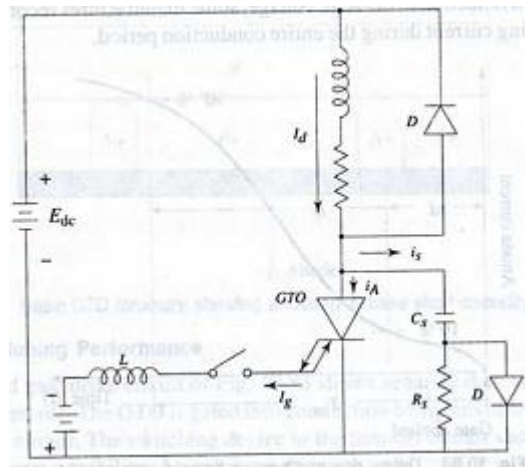
### 2.3.2 Gate turn-off

In the conducting state, the central region of the GTO crystal is filled with a conducting electron-hole plasma. To achieve turn-off, excess holes in the P-base must be removed by the application of a negative bias to the gate. During the storage phase of the turn-off process, negative gate current extracts excess holes in the P-base through the gate terminal. As a result, the anode current path is pinched into a narrow filament under each cathode finger (Figure 2.3). In this non-regenerative three-layer section of the crystal, current cannot sustain itself and

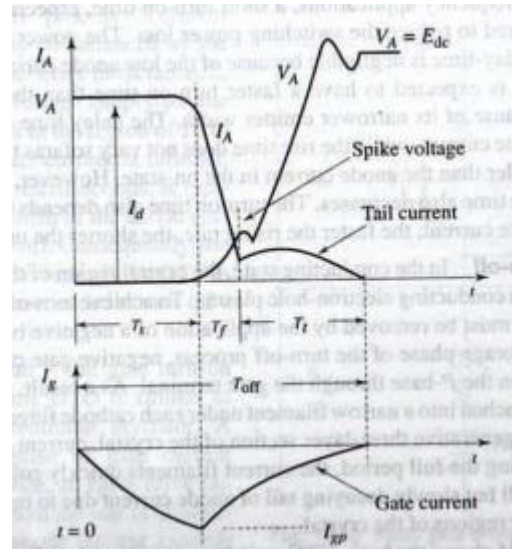


during the full period, the current filaments quickly collapse. Finally, there is a small but slowly decaying tail of anode current due to residual charges in the remoter regions of the crystal.

Figure 2.6 shows the basic GTO switching circuit with a clamped inductive load. Figure 2.7 shows the associated voltage and current waveforms at turn-off for the simplified circuit of Figure 2.6. As shown, the dc supply feeds an inductive load through a series connected GTO. A freewheeling diode is connected across the load to allow circulation of load current during the off-period of the GTO. The snubber capacitor reduces the rate of rise of forward voltage at turn-off, thereby improving the current interrupt capability of the GTO and also limiting the turn-off losses in the device.



**Figure 2.6** Basic GTO switching circuit with a clamped inductive load



**Figure 2.7** Voltage and current waveforms during turn-off of a GTO

Assume the GTO is conducting a steady load current,  $I_d$  when the gate turn-off is initiated at time zero by the application of a reverse bias between gate and cathode. A reverse gate current,  $I_g$ , builds up at a rate determined by the inductance of the gate circuit, but the anode current remains constant throughout the storage time  $T_s$ . Anode current,  $I_A$ , then decreases rapidly to the residual, or tail, current during the fall time,  $T_f$  and the load current is diverted into the snubber capacitance,  $C_s$ . As a result, forward voltage,  $V_A$ , builds up across the device at a rate  $dV_A/dt$  equal to  $I_d/C_s$ , and the anode tail current decays to zero to complete the turn-off process. Similar waveforms are obtained in inverter applications, but in practical circuits, stray inductance will cause some departure from the idealized waveforms described. In particular, supply inductance will cause a transient overshoot in GTO voltage, as shown in Figure 2.7. Excessive overvoltage can be avoided with an appropriate snubber circuit design.

## 2.4 GTO Characteristics

The peak value of off-gate current,  $I_{gp}$ , is a function of the anode current,  $I_d$ , prior to turn-off. The ratio  $I_d/I_{gp}$ , which is termed the turn-off gain, is typically between 3 and 5. The controllable current is the maximum anode current that can be interrupted by gate turn-off. It is highly dependent on device structure and gate drive conditions. It is also seriously reduced by an excessive rate of rise of anode voltage at turn-off. The controllable current is typically about three-times the RMS on-state current. Device damage will occur if an attempt is made to turn-off an anode current that is greater than the maximum controllable current. Consequently, auxiliary snubber circuits are imperative to slow the build-up of reapplied anode voltage but snubberless GTOs are also being developed.

In order to realize the gate-turn off capability of the GTO, basic design trade-offs are necessary and therefore, some device characteristics are inferior to those of a conventional thyristor of comparable ratings. Because of low internal regeneration, there is an increase in latching and holding current levels, and there is also an increase in the on-state voltage drop and the associated power loss. In a GTO with a shorted anode emitter, the reverse voltage rating is appreciably less than the forward-blocking voltage but many inverter circuits do not require the capability withstand reverse voltage. However, the GTO retains many of the advantages of the thyristor and has a faster switching speed. Its surge current capability is comparable to that of a conventional thyristor, so that device protection is possible with a fast semiconductor fuse. Because of the interdigitated gate-cathode structure of the GTO, the  $di/dt$  limitation at turn-on is less stringent than that in a conventional thyristor. In general, the GTO has the high blocking voltage and large current capability that are characteristic of thyristor devices. Consequently, the GTO can be used in equipment operating directly from three-phase ac supplies at 440V and above. A wide range of GTO devices is now

available, and a single device can be obtained with a present power capability of 4500V and 3500A.

The GTO inverter has a number of advantages over the conventional thyristor inverter. In particular, the GTO circuit has about 60 percent of the size and weight of the thyristor unit and has a higher efficiency because the increase in gate-drive power and on-state powerloss is more than compensated by the elimination of forced commutation losses. Several manufacturers have adopted GTO devices as switching elements in a range of packaged adjustable-frequency inverter drives, and the use of GTOs in inverters is growing rapidly.

The  $I$ — $V$  characteristics of a GTO in the forward direction are identical to that of a conventional thyristor. However in the reverse direction, the GTO has virtually no blocking capability because of the anode short structure. The latching current for large power GTOs is several amperes (here, 2A) as compared to 100—500 mA for conventional thyristors of the same rating.

## **2.5 GTO Gate Drive Circuit**

The gate drive requirements of the GTO can be divided into three classes.

- (1) During turn-on
- (2) On-state
- (3) During turn-off

The GTO gating circuits have a great influence on performance and operation of GTO equipment. Since the turn-on process of the GTO is similar to that of the SCR, the on-gating requirements are similar to those of an SCR.

During the on-state, load current greater than the latching current must flow

to maintain it in the conducting state. It is recommended that a low on-state gate current must be given during the forward on-state, to prevent any cathode island from dropping out of conduction since unlike the SCR, the GTO has a multi-cathode structure to facilitate the turn-off process.

After triggering, the load current must flow for a certain minimum duration ( $T_{\min}$ ) before the GTO is turned-off. This is to ensure that the junction temperature rise, which has occurred due to the turn-on power dissipation has come down before the turn-off power dissipation occurs. Moreover, the RC snubber should be so designed that the capacitor is fully discharged within  $T_{\min}$  otherwise there is a possibility of the forward off-state voltage increasing with a high  $dv/dt$  to an excessive value.

### 2.5.1 Various off-gating circuits

The off-gating circuits are the most important for reliable operation of GTO equipment. Various types of off-gating circuits are shown in Figure 2.8. Here, we discuss the classification of these typical circuits in brief.

*Type 1:* Power source voltage,  $E_{dc}$ , is chosen less than the gate-cathode breakdown voltage  $V_{(BR)R}$  in Type I(a). The gate current supplied from a power source becomes nearly zero after the tail current diminishes.

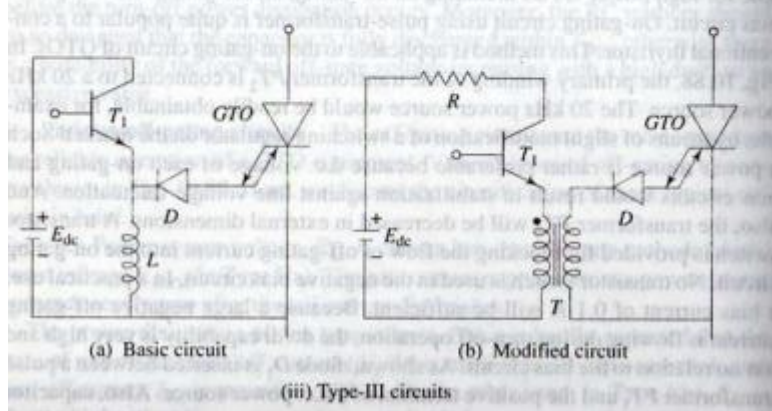
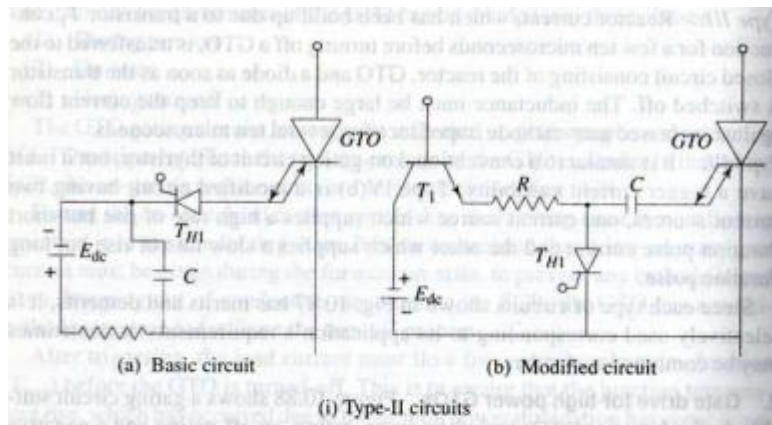
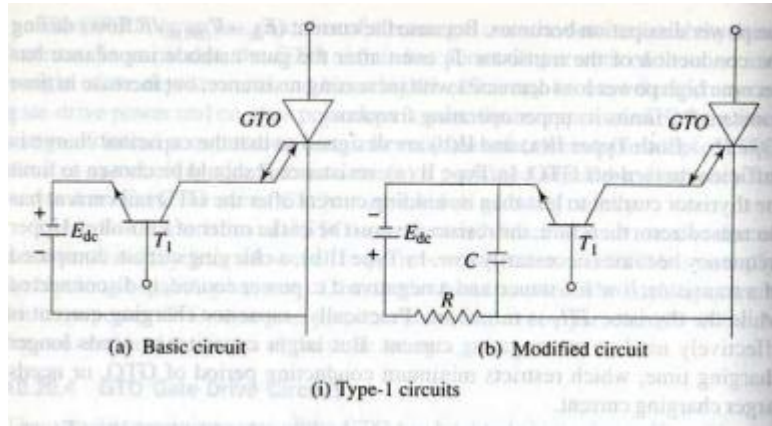
The power dissipation of this type is least. But it is hardly expected that the state of rise of gate turn-off current ( $di_g/dt$ ) is more than 10 A/ $\mu$ s and peak gate turn-off current  $I_{GP}$  is more than 100 A. On the other hand, in Type I(b),  $E_{dc}$  is chosen higher than  $V_{(BR)R}$  so as to improve ( $di_g/dt$ ), hence current limiting resistor  $R$  is inserted. The  $di_g/dt$  increases in proportion to  $E_{dc}$ . But the higher the  $E_{dc}$  is, larger the power dissipation becomes. Because the current  $(E_{dc} - V_{(BR)R})/R$  flows during the conduction of the transistor  $T_1$  even after the gate cathode impedance has become high power loss decreases with increasing resistance, but increase in time constant  $RC$  limits its upper operating frequency.

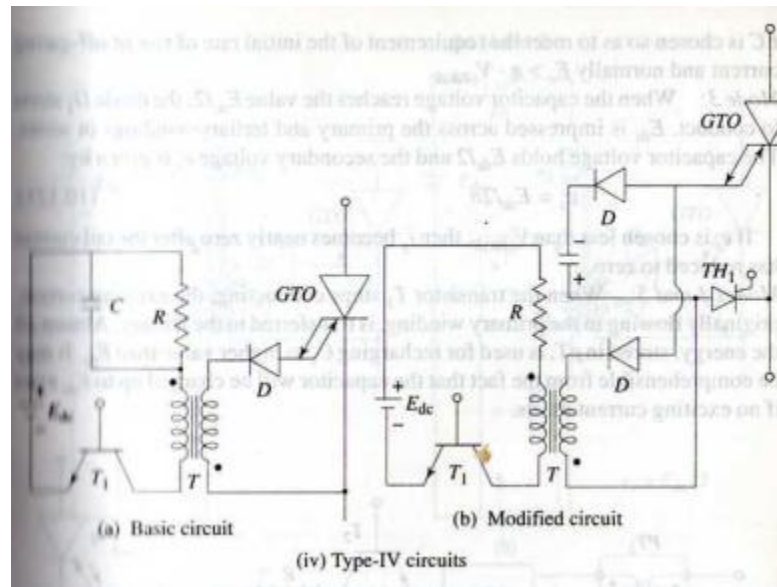
*Type II:* Both Types II(a) and II(b) are designed so that the capacitor charge is sufficient to turn-off GTO. In Type II (a), resistance  $R$  should be chosen to limit the thyristor current to less than its holding current after the GTO tail current has decreased zero, therefore, the resistance must be of the order of kilo-ohm. Upper frequency becomes necessarily low. In Type II(b), a charging circuit, composed of a transistor, low resistance and a negative dc power source, is disconnected while the thyristor  $TH_1$  is turned-on. Practically, capacitor charging current is effectively used as an on-gating current. But larger capacitance needs longer charging time, which restricts minimum conducting period of GTO, or needs larger charging current.

*Type III:* Reactor current, which has been build up due to a transistor  $T_1$  conduction for a few ten microseconds before turning off a GTO. is transferred to the closed circuit consisting of the reactor, GTO and a diode as soon as the transistor is switched off. The inductance must be large enough to keep the current flow against increased gate-cathode impedance for several ten microseconds.

*Type IV:* It is similar to a conventional on-gating circuit of thyristor, but it must have a bigger current capability. Type IV(b) is a modified circuit having two current sources, one current source which supplies a high rate of rise but short duration pulse current and the other which supplies a slow rate of rise but long duration pulse.

Since each type of circuits shown in Figure 2.8 has merits and demerits, it is selectively used corresponding to its application's requirements or sometimes maybe combined each other.





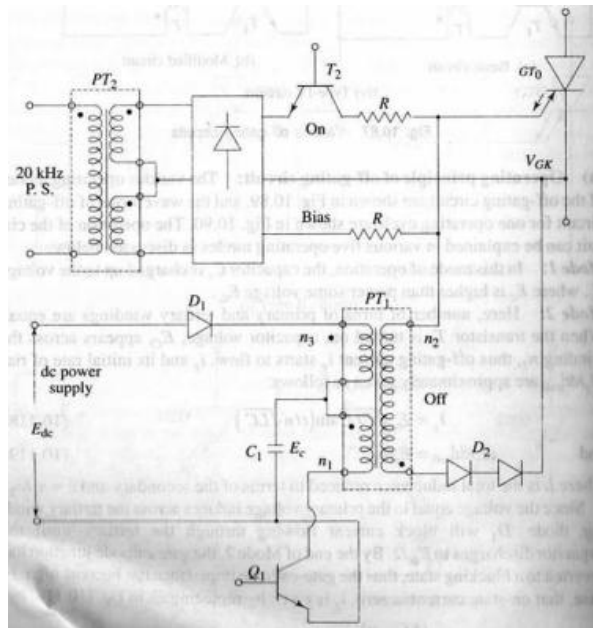
**Figure 2.8** Various off-gating circuits

### 2.5.2 Gate drive for high power GTO's

Figure 2.9 shows a gating circuit suitable for high power GTO's including an on-gating, an off-gating and a negative bias circuit. On gating circuit using pulse-transformer is quite popular to a conventional thyristor. This method is applicable to the on-gating circuit of GTOs. In Figure 2.9, the primary winding of the transformer  $PT_2$  is connected to a 20 kHz power source. The 20 kHz power source would be readily obtainable, for example, by means of slight modification of a switching regulator on the market. Such a power source is rather preferable because dc voltage of each on-gating and bias circuit would result in stabilization against line voltage fluctuation. And also, the transformer  $PT_2$  will be decreased in external dimensions. A transistor switch is provided for blocking the flow of off-gating current into the on-gating circuit. No transistor switch is used in the negative bias circuit. In a practical use, a bias current of 0.1A will be sufficient. Because a large negative off-gating current is flowing during turn-off operation, the  $dv/dt$  capability is very high and has no relation to the bias circuit. As shown, diode  $D_1$  is inserted between a pulse transformer  $PT_1$  and the positive terminal of a dc power



source. Also, capacitor  $C_1$  is connected across the connecting point of  $PT_1$  primary and tertiary windings and the negative terminal of the power source.



**Figure 2.9** Gate drive for high power GTO's

## 2.6 Snubber Circuits

The GTO turn-off characteristics will depend on the snubber circuit. The function of the snubber circuit is three fold:

- 1) With inductive load, when the GTO is switched off, the current which was flowing through the GTO is diverted into the snubber circuit which would otherwise have caused a loss (power dissipation) in it.
- 2) The snubber capacitor suppresses the rate of rise of forward voltage ( $dv/dt$ ) immediately following a turn-off, thereby preventing the possibility of maltriggering of GTO.
- 3) It helps increasing the peak gate controllable current capability.

The requirements of a snubber circuit are as follows:

- i. The snubber circuit must be wired as short as possible to reduce wiring inductions.

- ii. Fast recovery diode is necessary to decrease the  $dv/dt$  and GTO and turn-off power dissipation.
- iii. The smallest internal inductance of the capacitor will also be desirable

The power dissipation ( $W_s$ ) of the snubber circuit is approximately expressed as follows:

$$W_s = (1/2)C_s \cdot V_c^2 \cdot f \quad (2.1)$$

where  $C_s$  is snubber capacitor,  $V_c$ , the capacitor voltage,  $f$  the operating frequency.

The snubber capacitor of GTO should be larger, say 2  $\mu$ F, than that of a conventional thyristor, say 0.5  $\mu$ F. Therefore, GTO snubber circuit power dissipation will be larger by about four times than thyristor one. But a commutation circuit power dissipation of conventional thyristor equipment will be larger by about 50 times than off-gating circuit one of GTO. For instance, at operating frequency of 1000 Hz, the calculated results are follows:

	<b>GTO</b>	<b>SCR</b>
Snubber + switching	680 W	190 W
Commutating (turn-off)	40 W	2140
On-state	600 W	580 W
Total	1320 W	2910

Therefore, the total efficiency of a GTO inverter will increase more than the conventional thyristor.

## **2.7 Overcurrent Protection of GTO's**

In common with other semiconductor devices, GTOs are most susceptible to damage by excessive voltage and current than most other non-solid-state electrical components. Many of the protection requirements of conventional thyristors are also applicable to GTO devices; however, the gate turn-off capability offers not only a different method for overcurrent protection but also

opens a new avenue for possible failure.

Many electric power converters or other apparatus employing power semiconductors require the equipment to be so designed as to deliver a certain amount of overcurrent to the load for a certain time and to protect the load against higher currents for longer durations. Such an operation must be regarded as normal for the switching devices and must be within their repetitive rating. However, if such an overcurrent control system is not provided or fails to operate properly, or if there is an internal failure in the converter equipment, fault conditions will prevail and the devices must be protected as much as possible. For conventional thyristors, the surge current should be limited to less than the rated capability of the device by suitable surge limiting impedances, eventual natural or forced commutation of the surge, fuses, or fast circuit breakers.

Because GTO devices also have a significant surge capability, they may also be protected in the same way; however, any attempt to extinguish a high surge current by gate turn-off control is almost certain to result in destruction of the device. The limit of safety is the noncurrent peak turn-off capability,  $I_{ATO(max)}$ . The usual failure mechanism of the GTO under on overcurrent condition is reverse bias second breakdown, just as in a power transistor. For most practical circuits, the reapplied  $dv/dt$  will increase in direct proportion to the anode current because the snubber capacitor is usually a fixed value. Thus, the peak power dissipated by the GTO will increase very rapidly with the anode current.

From the above discussion, the following design techniques are recommended:

- 1) Some means should be provided to monitor the anode current in a GTO device and to suppress the generation of any gate pulses if a level exceeding  $I_{ATO}$  (non-respective) is detected. The conventional surge limit will then be in effect.
- 2) If a current level between the repetitive and non-repetitive turn-off rating is sensed, turn-off action should be initiated at once, on a one-shot basis. The current sensing device is already available in many power conversion circuits, to perform other functions. In any event, the current sensor should

have a suitably fast response, so corrective action can be taken to gate the GTO off at less than  $I_{ATO}$  (non-repetitive) in the event of a fault or to suppress gating if the anode current is greater than  $I_{ATO}$  (non-respective).

## 2.8 Paralleling of GTO's

Paralleling with no anode current balancers, i.e. direct paralleling, is useful in simplifying large capacitor power converters. Direct paralleling also makes it easier to replace a large current GTO with paralleled small current GTOs. For the equipment handling a large current, over several hundred amperes, a flat type type GTO is used, although it is more expensive than the stud type. By replacing the flat type GTO with the direct paralleled stud type GTO, costs of large capacity power can be reduced. In this section, stationally and transient operations for direct paralleling of GTO's has been discussed. Also, the current balancing ability of GTO's caused by the commutation of the gate current between parallel devices is described.

Current unbalance in the stationally and the transient state is generally attributed to the mismatch of the on-state voltage and the switching time. However, in case of GTO paralleling, exchange of the gate current between parallel devices also has much influence on current unbalance. In order to investigate this influence, the following two methods of gate connection are used:

- 1) The external impedances are connected in series with each gate terminal, so that the gate current can be equally divided among the devices (gate-coupling).
- 2) The gate terminals are directly connected with each other, so that the gate current can be divided by the gate impedance of the device itself (gate-coupling).

Current unbalance is compared for the two methods of gate-connections in Figure 2.10 to investigate of gate interaction. External impedance is determined as shown in Figure 2.10, so that a whole gate current can flow in the same way for the

both methods.

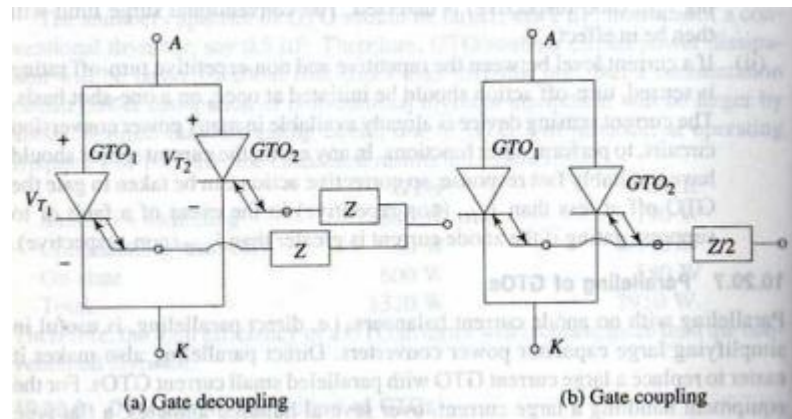
Typical switching waveform of both devices is shown in Figure 2.11. The current unbalance  $\Delta I_p$  and  $\Delta I_T$  during turn-on and steady on-state are given by

$$\Delta I_p = I_{p1} - I_{p2} \quad (2.2)$$

$$\Delta I_T = I_{T1} - I_{T2} \quad (2.3)$$

where  $I_p$  is the peak anode current during turn-on,  $I_T$  is the conducting current during the on-state.

Subscripts 1, 2 represent the number of the parallel branches, assuming the conducting current of branch 1 is larger than that of branch 2.



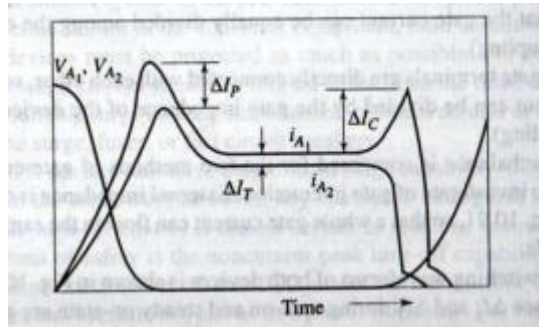
**Figure 2.10** Connections in direct paralleling of GTO's

Current unbalance during turn-off is evaluated by the incremental current,  $\Delta I_c$  in the transient state, and it is given by

$$\Delta I_c = I_{c1} - I_{T1} \quad (2.4)$$

where  $I_{c1}$  is the peak anode current during turn-off. The whole value of current unbalance during turn-off is the difference between the peak current  $I_{c1}$  and the average on-state current. It is the sum of  $\Delta I_c$  and  $\Delta I_T/2$ . The anode and gate currents can be measured using a current transformer. The impedance inserted in the circuit

is  $0.2 \text{ m}\Omega$ , which is sufficiently small enough not to produce a disturbance in the parallel operation.



**Figure 2.11** Switching waveforms of parallel devices

## CHAPTER 3

### METHODOLOGY

#### 3.1 Introduction

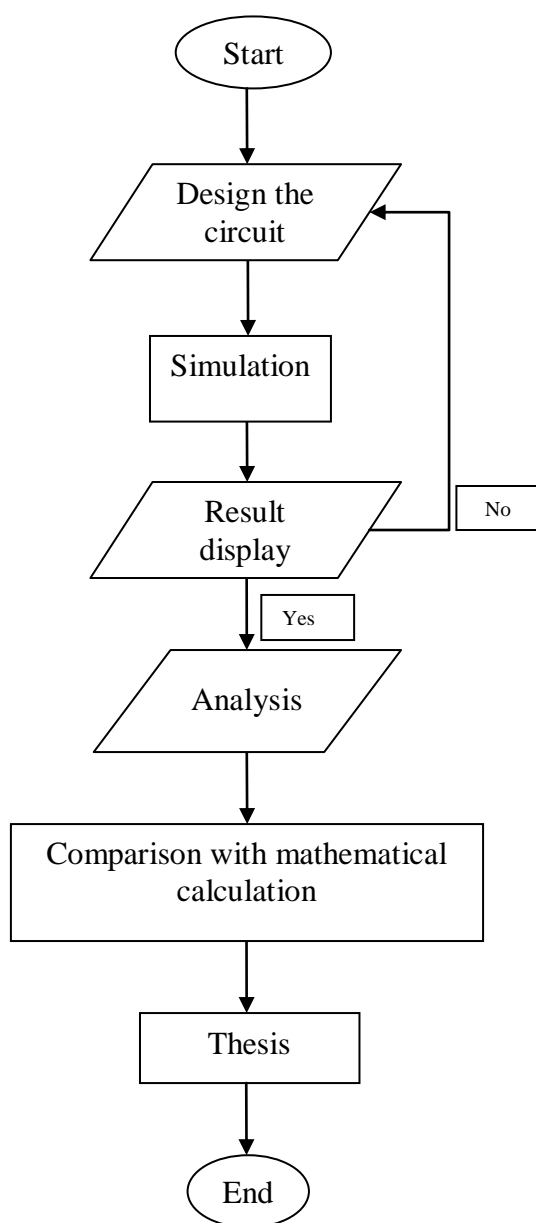
The methodology of this project consists of three major parts which are circuit design, simulation and analysis of the circuit designed and comparison of the results obtained with mathematical calculation result. Designing the circuit is the most important part for this project since the simulation and analysis parts are depending on the circuit designed in this initial part of the project.

After the circuit has been designed, the simulation of the circuit will be done by using ORCAD PSPICE simulator software. This simulation is based on the 6 pulse GTO thyristor converter, the analysis of switching waveform of GTO thyristor and the implementation of GTO thyristor as a control element in 6 pulse converter circuit. The important things in this simulation are the settings of operation condition, gate circuit parameters, firing angle and time delay of turn-on and turn-off pulses. If the result is not displayed as it is expected, the progress of the project will be held back to the circuit designing part and if the displayed results show the anticipated result of that circuit, then the progress will move on to the last part.

The last part of this project is the comparison between the simulation results of dc output voltage with the mathematical calculation results. This comparison result will show us the connection between the simulation and mathematical calculation.

In a simple word, we create a model of GTO thyristor with its operation circuit using ORCAD PSPICE simulator and make an analysis of their switching characteristics at different anode currents. Then, we implement this GTO thyristor model in the 6 pulse converter circuit. Finally, we compare the simulation results of dc output voltage with mathematical calculation results.

Below is the flow chart of the project process;

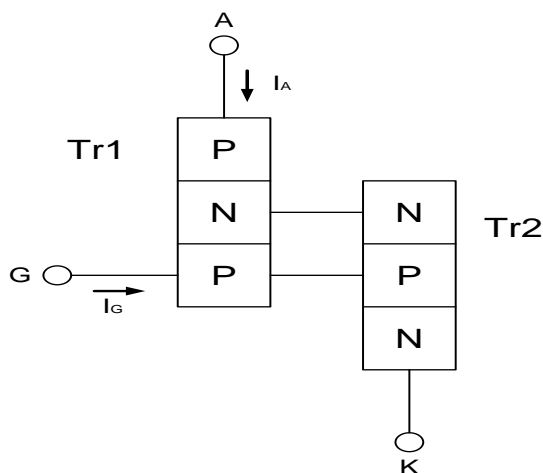


**Figure 3.1** Flow Chart of the Project



### 3.2 GTO Thyristor Model

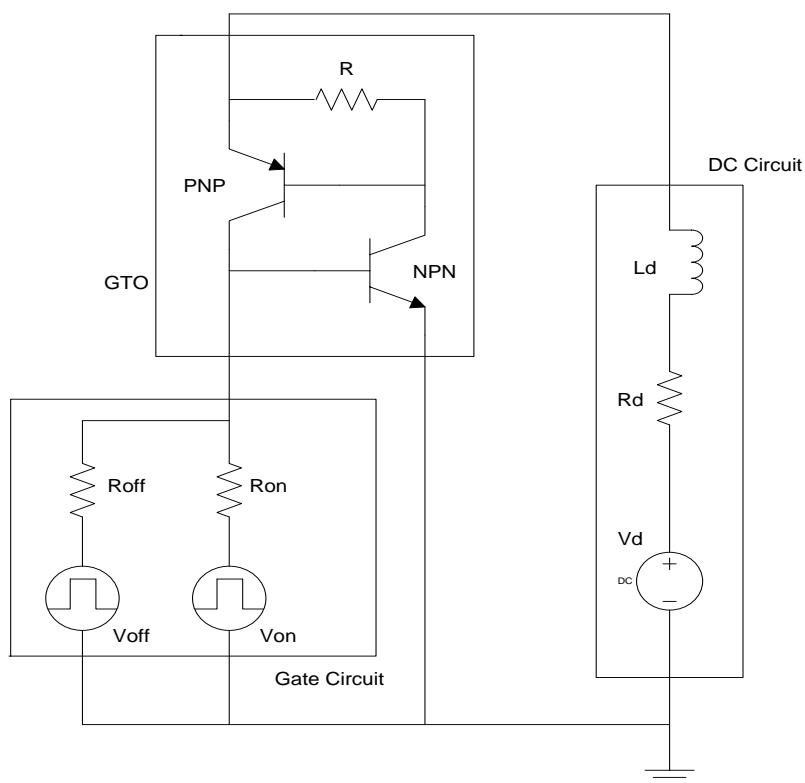
Since GTO thyristor model is not included in the library of ORCAD PSPICE simulator, we use two transistor models to create GTO thyristor model for the simulation. The monolithic pnpn structure of GTO thyristor can be conceptualized as comprising an npn transistor and a pnp transistor, interconnected as shown in Figure 3.2.



**Figure 3.2** Two Transistor Model

Figure 3.2 shows the collector on npn transistor provides base-drive to the pnp, while the collector of the pnp, along with any externally supplied gate current, supplies gate current to the npn. In this positive feedback arrangement, regeneration occurs once the loop gain exceeds one, when each transistor drives another transistor into saturation.

The GTO thyristor model is then connected to the gate circuit with its operation circuit parameters which are shown in Figure 3.3 and Table 1.



**Figure 3.3** GTO thyristor model and its operation circuit

Operation Circuit	Ld	1 $\mu$ H
	Rd	20 $\Omega$ , 10 $\Omega$ , 5 $\Omega$
	Vd	100V
GTO	PNP	SMBT3906
	NPN	SMBTA06
	R	1 $\Omega$
Gate Circuit	Von	10V
	Voff	-60V
	Ron	40 $\Omega$
	Roff	22 $\Omega$ , 10 $\Omega$ , 5 $\Omega$

**Table 3.1** Operation circuit parameters of GTO thyristor model

We are using the Texas Instruments of SMBTA06 for the NPN transistors and SMBT3906 for the PNP transistors in this simulation. Turn-on and turn-off of GTO thyristor model are controlled by connecting the gate terminal to the gate circuit. GTO thyristor will turned on when positive gate pulse current is applied. Small gate pulse current is enough to turn it on.

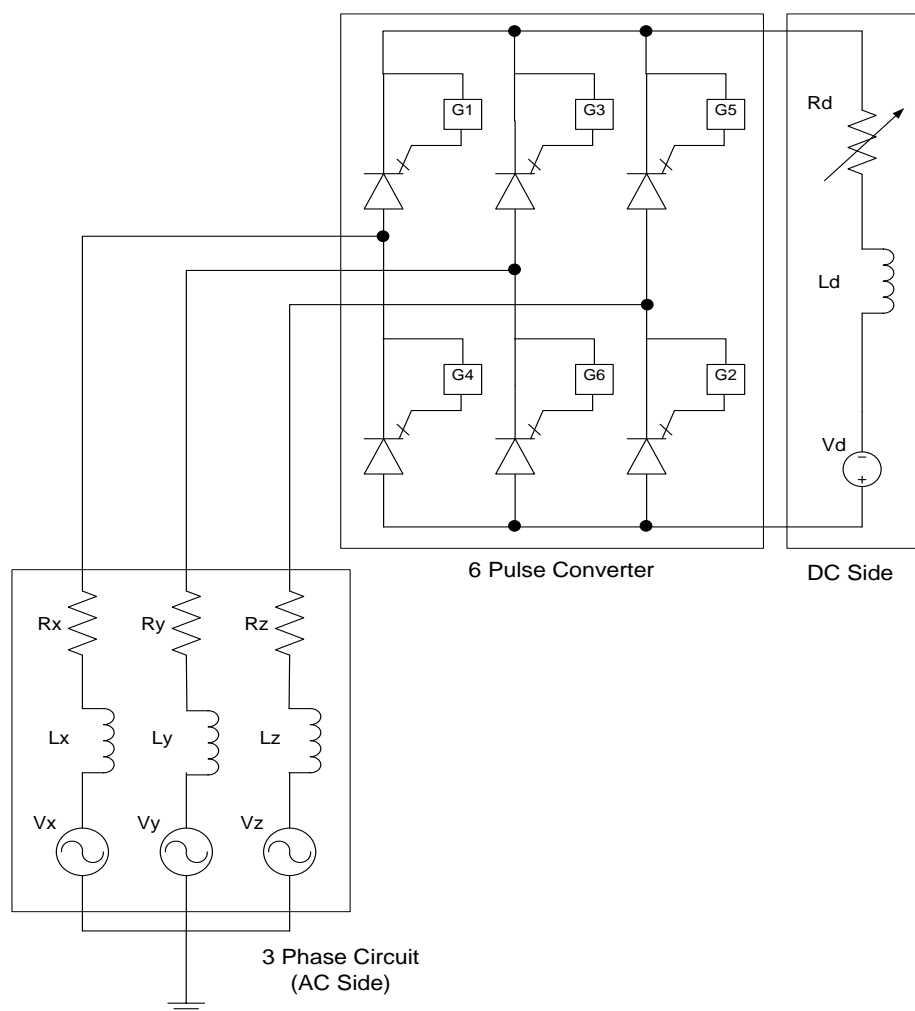
Here, we set the gate pulse current 5% of the anode current. Beside, GTO thyristor will turned off when negative gate pulse current is applied. Then, we set the gate pulse current 60% of the anode current. Normally the gate current required to turn it off is as much as 20% of the anode current. In this project, we want to consider the turn-off time, where at 60% of anode current, the turn-off time is smaller than at 20% of anode current.

### 3.3 6 Pulse Converter Circuit

Figure 3.4 is considered in which a 3 phase, 6 pulse converter supplies power to a load. Each three single phase power supply,  $V_x$ ,  $V_y$  and  $V_z$  fed 50V and 50 Hz of ac voltage and frequency. The other parameters in the ac side are shown in Table 2.

3 Phase Circuit (AC Side)	$R_x, R_y, R_z$	0.1m $\Omega$
	$L_x, L_y, L_z$	0.1mH
	$V_x, V_y, V_z$	50V, 50Hz
6 Pulse Converter	G1 ~ G6	Gate Circuit
DC Side	$R_d$	Variable
	$L_d$	1mH
	$V_d$	1 $\mu$ V ~ 200V

**Table 3.2** Parameters of 6 pulse converter circuit



**Figure 3.4** 6 pulse converter circuit

The 6 pulse converter circuit consists of 6 GTO thyristors, and each GTO thyristors are triggered by the gate circuit G1~G6. The gate circuit parameters for this simulation are the same as in Table 1, explained before. At the dc side, the load is composed of a dc voltage  $V_d$  and a variable resistor  $R_d$  in series with a smoothing inductor  $L_d$ . The parameters of these components are shown in Table 2.

The value of variable resistor is varying to fix a value of dc output current at one level. 6 pulse converter can be functioned as a rectifier and an inverter depend on the firing angle,  $\alpha$ . It is function as a rectifier when the firing angle is in the range of  $0^\circ \sim 90^\circ$ . When the firing angle is advance from  $90^\circ$ , the converter will function as an inverter. Therefore, dc voltage,  $V_d$  is required during the inverter operation. So, the dc voltage value is varying in the range of  $1\mu V \sim 200V$  for this simulation.

## CHAPTER 4

### RESULTS AND ANALYSIS

#### 4.1 Introduction

This chapter will briefly discuss on the results and discussions of the simulation. The discussion in this chapter focused on the comparison between the result of the simulation and mathematical calculation.

#### 4.2 The simulation result

The simulation result in this project is divided into two parts, which are the GTO thyristor model and the 6 pulse converter circuit.

##### 4.2.1 The GTO thyristor model

The simulation result of the GTO thyristor model focused on the turn-on and turn-off time of the GTO thyristor model. In this simulation, the turn off time that will be put into consideration is at 60% of anode current and the turn-off time is smaller than at 20% of anode current while the value of anode-cathode voltage used

is 100V. This voltage is supplied to the GTO thyristor model. Figure 4.1 below show the simulated circuit of GTO thyristor model.

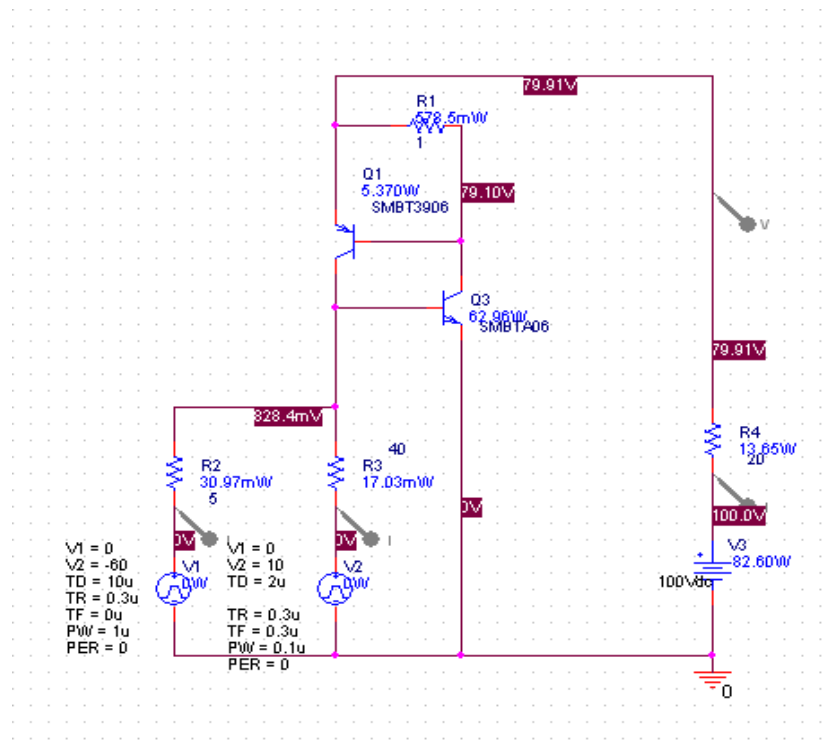


Figure 4.1

The results obtained are shown in the figure below. From the results obtained, we measured the storage time, fall time, tail time and turn-off time. These measured values are stated in Table 4.1.

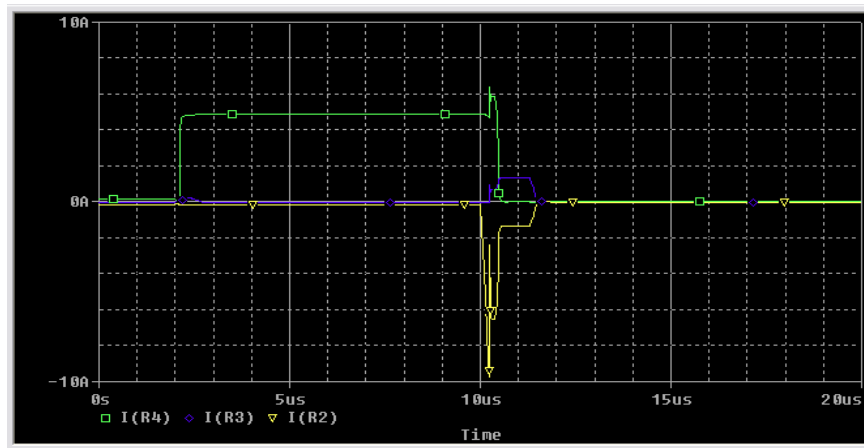


Figure 4.2.1 Turn-on and turn-off characteristics of GTO thyristor ( $I_d=5A$ )

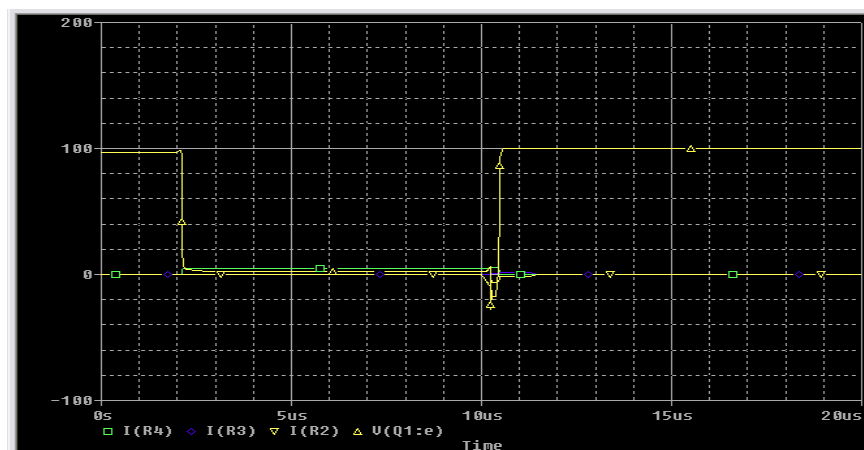


Figure 4.2.2 Turn-on and turn-off characteristics of GTO thyristor ( $I_d=5A$ ,  $V=100V$ )

Storage time,  $T_s = 11.287 - 10.000 = 1.287$

Fall time,  $T_f = 11.478 - 11.287 = 0.191$

Tail time,  $T_t = 11.480 - 11.478 = 0.002$

Turn-off time =  $11.480 - 10.000 = 1.480$

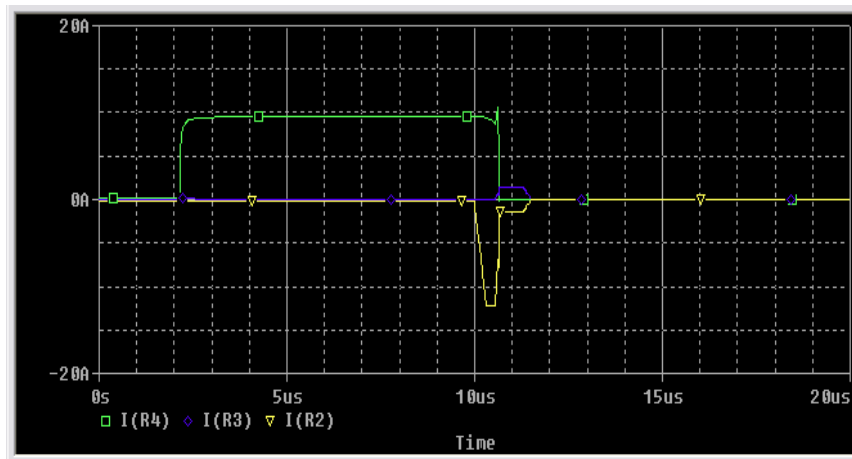


Figure 4.2.3 Turn-on and turn-off characteristics of GTO thyristor ( $I_d=10\text{A}$ )

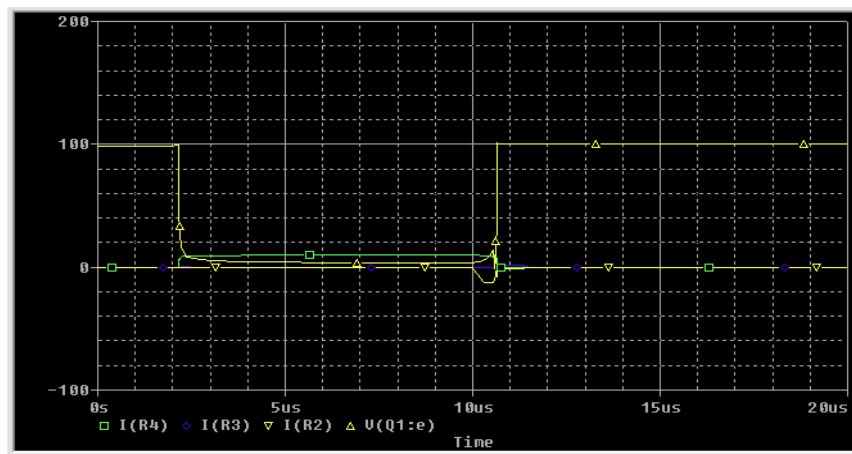


Figure 4.2.4 Turn-on and turn-off characteristics of GTO thyristor ( $I_d=10\text{A}$ ,  $V=100\text{V}$ )

Storage time,  $T_s = 10.557 - 10.000 = 0.557$

Fall time,  $T_f = 10.645 - 10.557 = 0.088$

Tail time,  $T_t = 10.647 - 10.645 = 0.002$

Turn-off time =  $10.647 - 10.000 = 0.647$



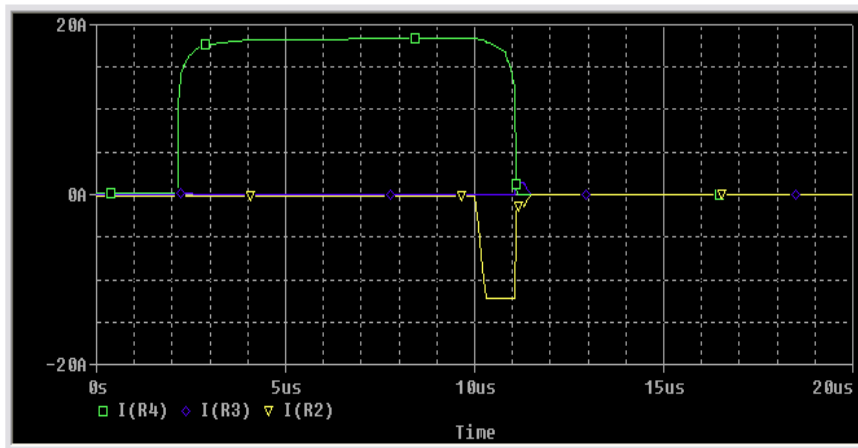


Figure 4.2.5 Turn-on and turn-off characteristics of GTO thyristor ( $I_d=20A$ )

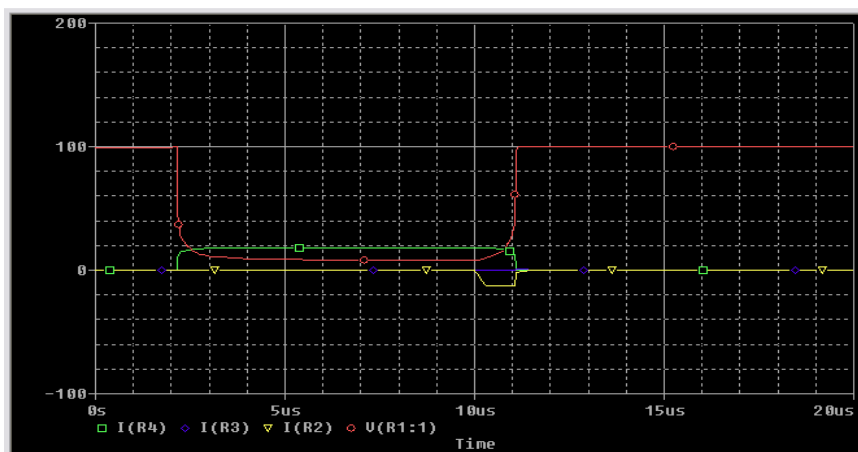


Figure 4.2.6 Turn-on and turn-off characteristics of GTO thyristor ( $I_d=20A$ ,  $V=100V$ )

Storage time,  $T_s = 10.296 - 10.000 = 0.296$

Fall time,  $T_f = 11.024 - 10.296 = 0.728$

Tail time,  $T_t = 11.044 - 11.024 = 0.002$

Turn-off time =  $11.044 - 10.000 = 1.044$

Anode Current [A]	5	10	20
Storage Time, $T_s$ [ $\mu s$ ]	1.287	0.557	0.296
Fall Time, $T_f$ [ $\mu s$ ]	0.191	0.088	0.728
Tail Time, $T_t$ [ $\mu s$ ]	0.002	0.002	0.002
Turn-off Time [ $\mu s$ ]	1.480	0.647	1.044

Table 4.1

Based on these results, the GTO thyristor can be turned on and turned off with a small turn-off time in the range current of 5A~20A. With these parameters, this GTO thyristor model will be implemented in the 6 pulse converter circuit.

#### 4.2.2 6 pulse converter circuit

The 6 pulse converter circuit consists of 3 phase 6 pulse converter that supplies power to a load. Every single phase power supply fed 50V of ac voltage with the frequency of 50Hz. All 6 of GTO thyristors are each triggered by the gate circuit G1~G6 while the parameters used for GTO thyristor are the same. Figure 4.4 below show the 6 pulse converter circuit designed in PSPICE for a simulation.

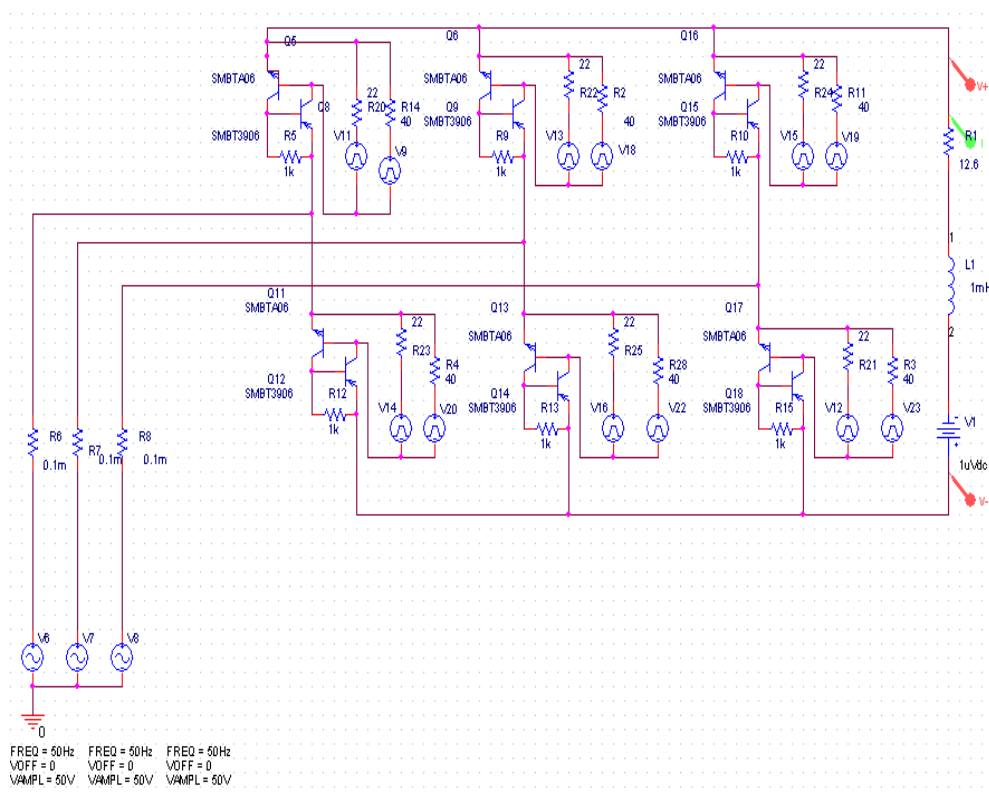


Figure 4.3 6 pulse converter circuit

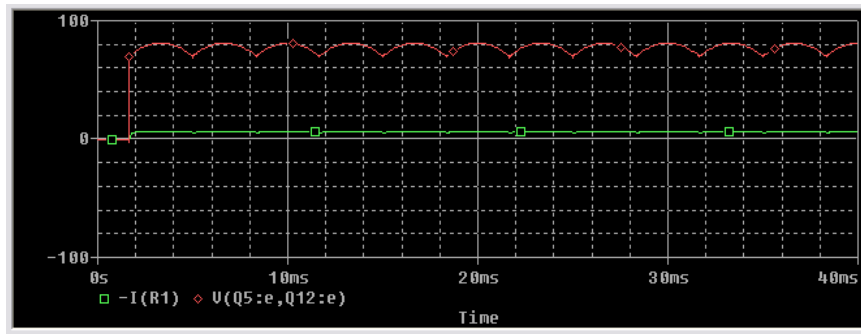


Figure 4.4.1 Alpha,  $\alpha = 0^\circ$ ,  $V_{dc} = 77V$ ,  $R1 = 15\Omega$ ,  $V1 = 1\mu V$

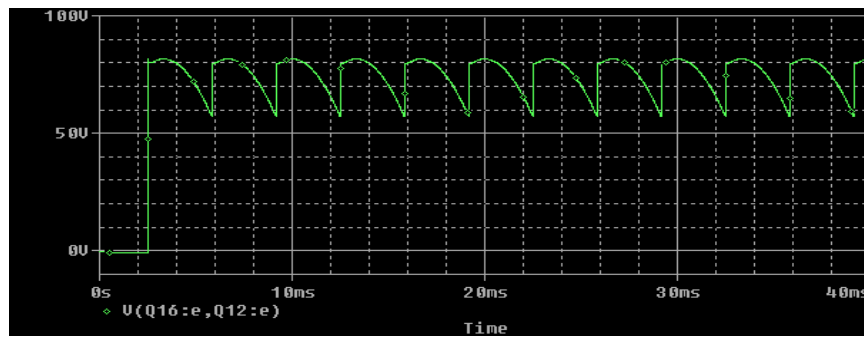


Figure 4.4.2 Alpha,  $\alpha = 15^\circ$ ,  $V_{dc} = 69V$ ,  $R1 = 15\Omega$ ,  $V1 = 1\mu V$

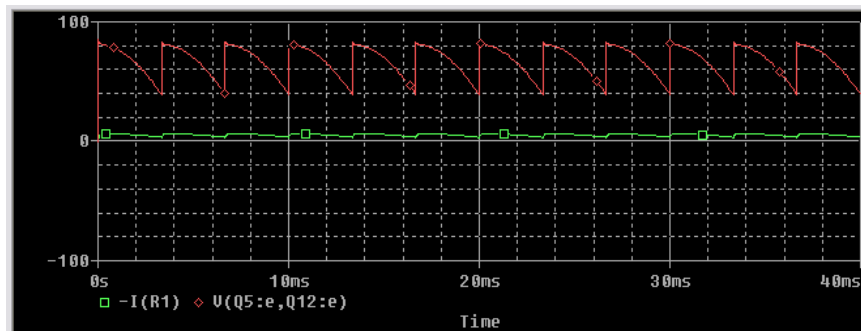


Figure 4.4.3 Alpha,  $\alpha = 30^\circ$ ,  $V_{dc} = 60V$ ,  $R1 = 12.6\Omega$ ,  $V1 = 1\mu V$

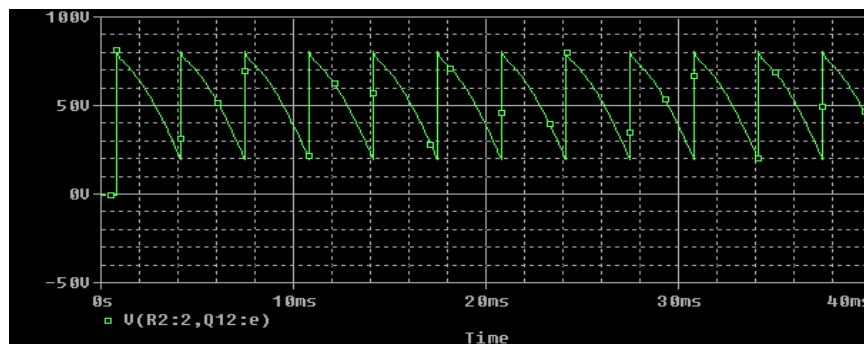


Figure 4.4.4 Alpha,  $\alpha = 45^\circ$ ,  $V_{dc} = 50V$ ,  $R1 = 9.8\Omega$ ,  $V1 = 1\mu V$

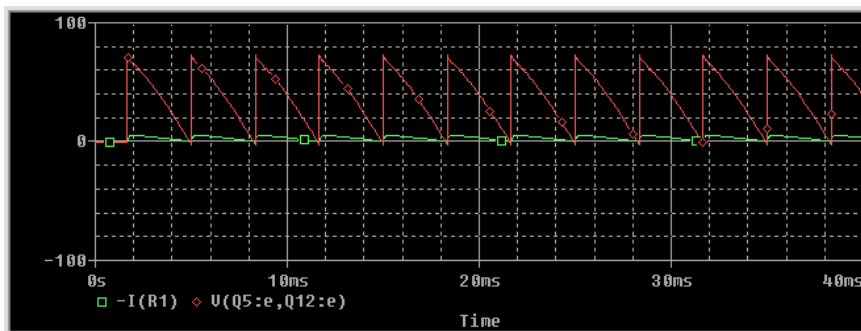


Figure 4.4.5 Alpha,  $\alpha = 60^\circ$ ,  $V_{dc} = 35V$ ,  $R_1 = 6\Omega$ ,  $V_1 = 1\mu V$

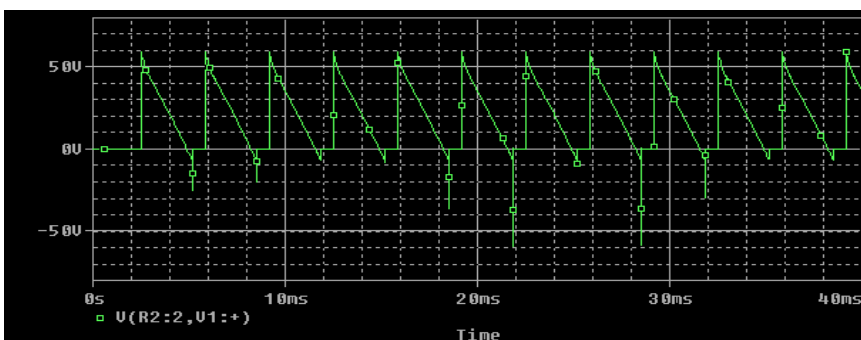


Figure 4.4.6 Alpha,  $\alpha = 75^\circ$ ,  $V_{dc} = 25V$ ,  $R_1 = 3.8\Omega$ ,  $V_1 = 1\mu V$

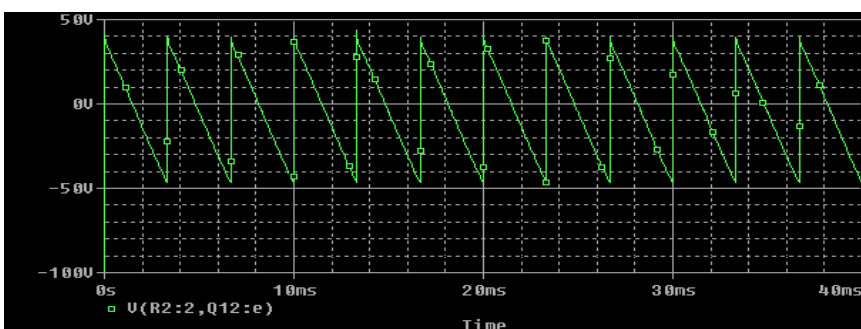


Figure 4.4.7 Alpha,  $\alpha = 90^\circ$ ,  $V_{dc} = -2V$ ,  $R_1 = 19\Omega$ ,  $V_1 = 100V$

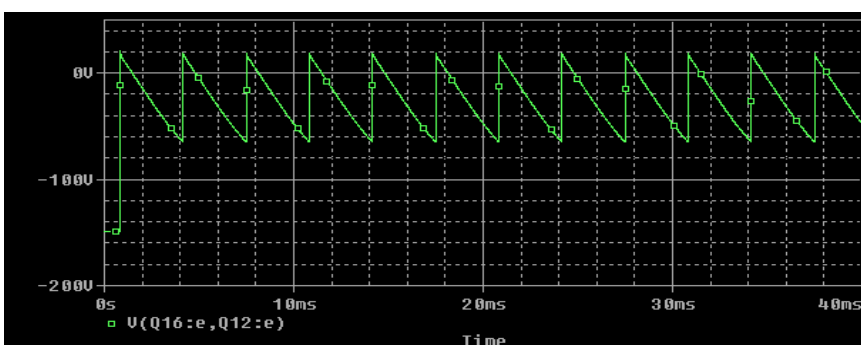


Figure 4.4.8 Alpha,  $\alpha = 105^\circ$ ,  $V_{dc} = -22V$ ,  $R_1 = 25\Omega$ ,  $V_1 = 150V$

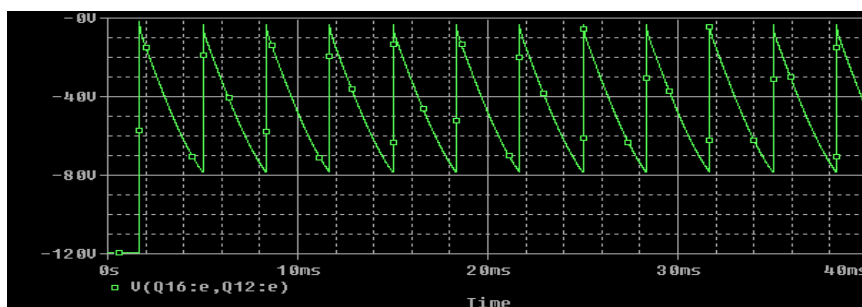


Figure 4.4.9 Alpha,  $\alpha = 120^\circ$ ,  $V_{dc} = -45V$ ,  $R1 = 15\Omega$ ,  $V1 = 120V$

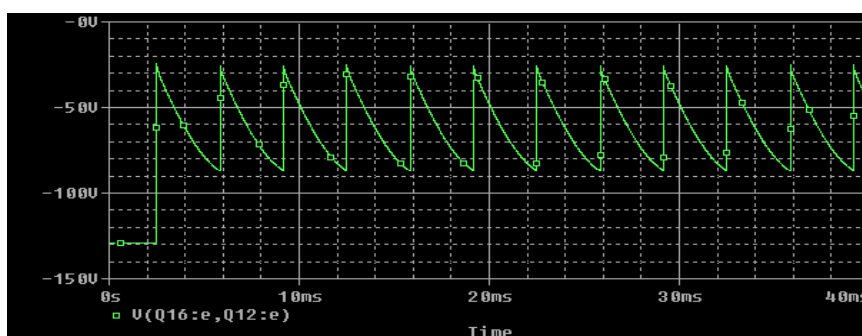


Figure 4.4.10 Alpha,  $\alpha = 135^\circ$ ,  $V_{dc} = -58V$ ,  $R1 = 17\Omega$ ,  $V1 = 130V$

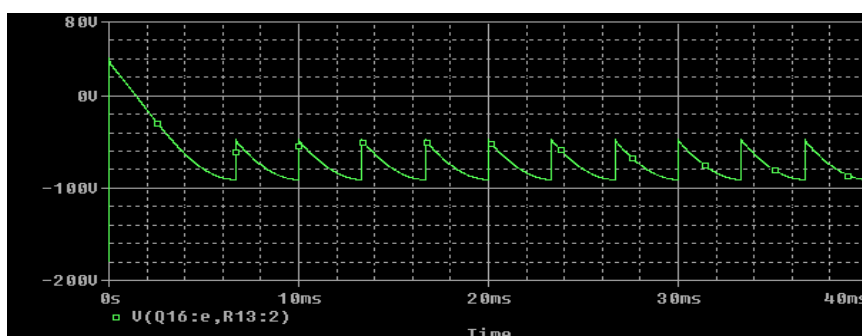


Figure 4.4.11 Alpha,  $\alpha = 150^\circ$ ,  $V_{dc} = -73V$ ,  $R1 = 21.5\Omega$ ,  $V1 = 180V$

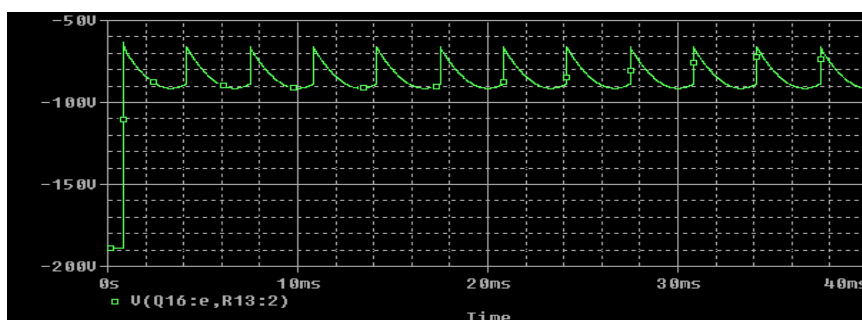


Figure 4.4.12 Alpha,  $\alpha = 165^\circ$ ,  $V_{dc} = -80$  ( $\sim 77$ )  $V$ ,  $R1 = 19\Omega$ ,  $V1 = 190V$

The simulation results show the dc output voltages with different firing angles where the dc output current is fixed to 5A. Based from these results, the 6 pulse converter circuit can be controlled to function as a rectifier or as an inverter. This whole control thing is depend on the value of the firing angle,  $\alpha$  which has been set up earlier in the GTO thyristor. When the firing angle is set in the range of  $0^\circ \sim 90^\circ$ , the 6 pulse converter circuit will function as a rectifier while when the firing angle is over than  $90^\circ$ ; the 6 pulse converter circuit will function as an inverter. The required firing angle can be implemented into the circuit by the settings of time delays. The equation used to set the time delays is,

$$TD = \frac{\alpha + 30^\circ}{360^\circ} \times \frac{1}{f} \quad (4.1)$$

Where  $f$  = frequency

### 4.3 The mathematical calculation and comparison

The results of the simulation obtained earlier will be compared with the mathematical calculation results to measure the similarity of both outputs. After taking in the consideration of commutation overlap, the range of firing angle to be use are within  $0^\circ \sim 165^\circ$ . The dc output voltages of the circuit are obtained from the equation,

$$E_{dc} = \frac{3\sqrt{3}}{2\pi} E_m \left[ \cos \alpha + \cos (\alpha + u) \right] \quad (4.2)$$

where,  $E_m$  = maximum ac voltage

$\alpha$  = firing angle

$u$  = commutation overlap

while  $\alpha + u$  is given as,

$$\alpha + u = \phi - \frac{\pi}{2} + \cos^{-1} \left( \cos \left( \alpha + \frac{\pi}{2} - \phi \right) - \frac{2I_d \sqrt{R^2 + \omega L^2}}{\sqrt{3}E_m} \right) \quad (4.3)$$

where,  $I_d$  = dc output current

$$\phi = \tan^{-1} \frac{\omega L}{R}$$

The parameters in Table 3.2 will be used along with equation 4.2 and equation 4.3 to determine the result of mathematical calculation. The results are shown in Table 4.2 below.

Firing Angle, $\alpha$ (°)	Simulation Result (DC output voltage)	Calculation Result (DC output voltage)
0	77	81
15	69	79
30	60	72
45	50	67
60	35	41
75	25	23
90	-2	-1
105	-22	-21
120	-45	-43
135	-58	-57
150	-73	-72
165	-80	-80

Table 4.2

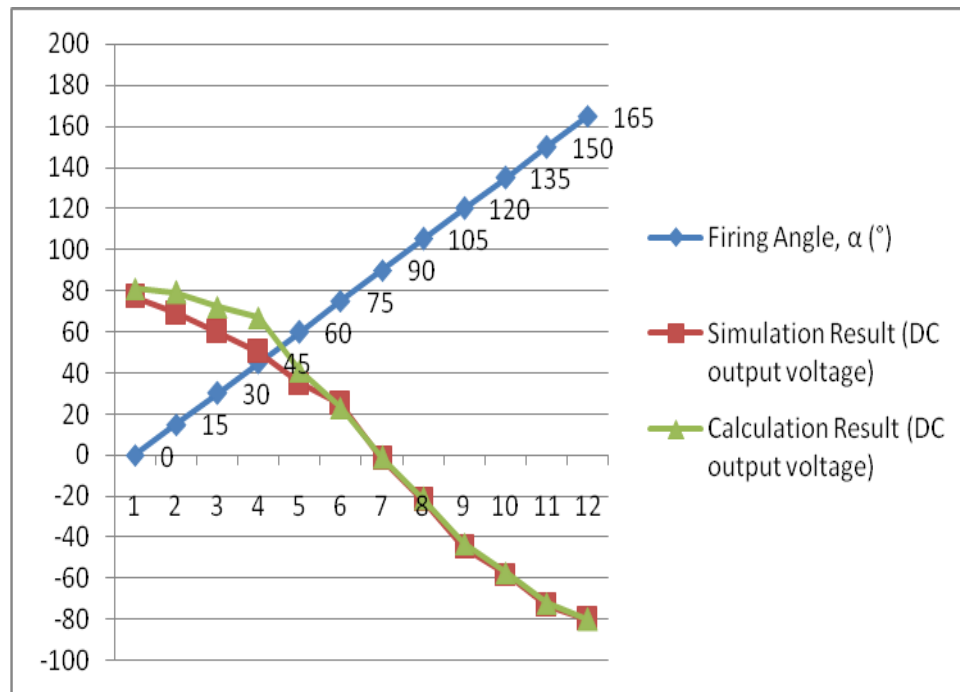


Figure 4.5 DC Output Voltage vs Firing Angle

Figure 4.6 illustrates the comparison between simulation results and calculation results by plotting a chart. Based from the chart, the curve of the simulation results are almost the same as the curve of the calculation results. The values of dc output voltages within the range of  $60^{\circ}$ ~ $165^{\circ}$  are almost the same and almost in the same line while in the range  $0^{\circ}$ ~ $45^{\circ}$  there are a little difference. The values of the simulation results are smaller than the values from calculation but it is not too much of a difference. This difference in the values of dc output voltages may happen due to some reason such as voltage drop during the turn-on and turn-off of operation of the GTO thyristors, power losses due to commutation overlap and measurement error in maintaining the same level of dc output current during the simulation. The 6 pulse converter circuit can function as a rectifier or as an inverter since the power transfer can be controlled by varying the firing angle and power transmission direction can be feed either to the dc side or to the ac side.



#### **4.4 Summary**

The result of each elements stated from the previous chapter has been discussed in this chapter. The analysis is done on the results obtained by comparing the results from both simulation and calculation.

## CHAPTER 5

### CONCLUSION AND RECOMMENDATIONS

#### 5.1 Conclusions

The GTO thyristor model can be created using PSPICE simulator along with its gate and operation circuit. The switching characteristics of the model can also be obtained from the simulation. The GTO thyristor can be turned on and turned off in the range current of 5A~20A with a small turn-off time. With the same parameter, this GTO thyristor model is being implemented in the 6 pulse converter circuit with controlled gate circuits. The comparison between the results obtained in both simulation and calculation is analyzed and show that the characteristics curve of dc output voltage vs firing angle show almost the similar characteristics except in the range  $0^{\circ}$ ~ $45^{\circ}$  of firing angle. The simulation results within this range are a bit smaller compared to the mathematical calculation results. It is also confirmed that power transfer can be controlled either as a rectifier or as an inverter.

#### 5.2 Future recommendations

For the future plan of this project, it is recommended to other candidate to implement the snubber circuit into the GTO thyristor circuit. The snubber inductor will act as a turn-on snubber while turn-off snubber is included as part of the switching circuit.

### **5.3 Costing and Commercialization**

Since this project did not based on hardware implementation, there is no cost usage to complete this project. This project can be a pioneer in the semiconductor industry which increased the use of power semiconductor in power applications. The characteristics of GTO thyristor has made it possible to manufacture self-commutated converter since the switching can be controlled freely.

## REFERENCES

- [1] Don Peter, "ORCAD PSpice, Capture, and Probe Tutorial", Seattle Pacific University, 2000.
- [2] Muhamad Zahim Sujod, "6 Pulse GTO Thyristor Converter Simulation", The 5<sup>th</sup> Student Conference on Research and Development, 2007.
- [3] Dorin O.Neacsu. "Power-switching Converters: Medium and High Power", CRC Press, Taylor & Francis Group, 2006.
- [4] Irving M.Gottlieb, "Power Supplies, Switching Regulators, Inverters, and/ Converters".
- [5] Theodore Wildi, "Electrical Machines, drives, and power systems", Prentice Hall, 2002.
- [6] Jai P. Agrawal, "Power electronic systems theory and design", 2001.
- [7] Don Peter, "PSpice tutorial", Dept. of Engineering Seattle Pacific University, 2000.
- [8] M.D. Singh, K.B. Khanchandani, "Power Electronics", 1998.