ANALYSIS OF POWER LOSSES AND LIFETIME FOR THE INVERTER IN ELECTRIC VEHICLES USING VARIABLE VOLTAGE CONTROL AND VARIABLE SWITCHING FREQUENCY MODIFIED PWM

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Thesis submitted in fulfillment of the requirements

for the award of the degree of

Master of Science

College of Engineering

UNIVERSITI MALAYSIA PAHANG

NOVEMBER 2020

ACKNOWLEDGEMENTS

First and foremost, all thanks and glory are due to "ALLAH" the Almighty, who gave me the power, the health and patience to accomplish this research.

It is my great fortune to have Ir. Dr. Ing. Muhamad Zahim Bin Sujod as the supervisor during my Master. I would like to express my warmest appreciation, gratitude and sincere thanks to him for his guidance, encouragement, support, kind help and sound advice throughout the period of this research. Dr. Zahim's technical expertise, and energy have been invaluable during my study and I am truly honored to have worked with a world class researcher such as him.

I would like to acknowledge the administrative and teaching staff of University Malaysia Pahang (UMP) for providing the facilities to conduct this research. Also, I am very grateful to the Ministry of Higher Education Malaysia (MOHE) for their financial support of this research through the Fundamental Research Grant Scheme (RDU1803165).

Lastly, I would like to express my deepest gratitude and greatest appreciation to my parents, brothers, and sisters for their enormous love, inspiration, and prayers. They always respect what I want to do and give me their full support and encouragement over the years. I just want to say that I love you all very much and that dedicated this thesis to all of you.

ABSTRAK

Dengan meningkatnya permintaan untuk pengurangan emisi dan penjimatan bahan bakar, pembuat kenderaan memberi tumpuan kepada pembangunan kereta elektrik (EV). Prestasi EV dinilai dari segi jarak pemanduan dan jangka hayat komponennya. Penukar kuasa adalah antara komponen pemacu EV yang paling terkesan dan kurang kebolehpercayaan. Oleh itu, meningkatkan jangka hayat penukar kuasa adalah perkara yang penting untuk penggunaan EV yang baik. Jangka hayat penukar kuasa dapat ditingkatkan dengan mengurangkan kitaran haba peranti kuasa, yang merupakan penyebab utama kerosakan. Oleh kerana suhu dan kehilangan kuasa penukar kuasa adalah berkadar terus, kitaran haba boleh dikurangkan dengan meminimumkan kehilangan kuasa. Sebagai tambahan kepada peningkatan jangka hayat, meminimumkan kehilangan kuasa penukar kuasa dapat meningkatkan julat EV kerana penggunaan kuasa dikurangkan dalam keadaan tertentu. Sehubungan itu, tesis ini bertujuan untuk mengkaji kesan teknik pengurangan kehilangan kuasa yang dikenali sebagai kawalan voltan arus-terus (VVC) bolehubah pada jangka hayat penyongsang. Di samping itu, tesis ini mengusulkan strategi baru iaitu modulasi lebar pulsa (PWM) yang dikenali sebagai frekuensi pensuisan bolehubah PWM (VSF-MPWM) untuk tiga fasa dua level penyongsang sumber voltan. VSF-MPWM bertujuan untuk mengurangkan kehilangan kuasa penyongsang tanpa mengurangkan kualiti arus keluaran. Untuk mengkaji kesan VVC pada jangka hayat penyongsang, kaedah anggaran jangka hayat dikemukakan. Kaedah ini menggunakan kitaran pemanduan Artemis Urban dan US06 untuk mendapatkan pemuatan haba, dan seterusnya penggunaan jangka hayat peranti kuasa penyongsang. Kemudian, VSF-MPWM digunakan bagi meminimumkan kehilangan kuasa dengan menyepit mana-mana kaki tiga fasa pada puncak arus fasa untuk mengurangkan jumlah peralihan melalui frekuensi pensuisan bolehubah. Walau bagaimanapun, untuk mencapai kualiti arus yang boleh diterima, VSF-MPWM digunakan bagi mengawal kedua-dua tempoh pengapit dan frekuensi pensuisan bolehubah mengikut had kualiti arus konvensional PWM. Kesan VVC pada jangka hayat penyongsang dan prestasi VSF-MPWM terhadap kehilangan kuasa penyongsang dan kualiti arus dilakukan menggunakan perisian MATLAB Simulink. Analisis jangka hayat menunjukkan bahawa VVC mempunyai kemampuan untuk meningkatkan jangka hayat penyongsang dengan faktor 5.06 bagi Artemis Urban dan 3.43 bagi US06 berbanding dengan kawalan voltan arus-terus konvensional (CVC). Hasil simulasi menunjukkan bahawa VSF-MPWM dapat mengurangkan sehingga 35.4% kehilangan pensuisan dan 23.8% kehilangan kuasa dibandingkan dengan konvensional PWM. Sementara itu, VSF-MPWM dapat mengekalkan kualiti arus keluaran yang sama dengan konvensional PWM.

ABSTRACT

With the increasing demand for reduced emissions and improved fuel economy, the automakers are focusing on the development of electric vehicles (EVs). The performance requirements for EVs includes high driving range and long life of its components. The power converters are among the most stressed and less reliable EV drivetrain components. Hence, improving the lifetime of the power converters is essential for the success of EV adoption. The lifetime of the power converters can be improved by reducing thermal stress of the power devices, which represents the main cause of failure. Since the temperature and power losses of the power device are proportional, thermal stress can be reduced by minimizing the power losses. In addition to the lifetime improvement, minimizing the power losses of the power converters can extend the EV range since the power demand under a given loading conditions is reduced. In this regard, this thesis aims to study the impact of an existing power loss reduction technique known as variable dc-bus voltage control (VVC) on the inverter lifetime. In addition, it proposes a new pulse width modulation (PWM) strategy called variable switching frequency modified PWM (VSF-MPWM) for three-phase two-level voltage source inverter. The VSF-MPWM aims to minimize the inverter power losses, but without sacrificing the output current quality. In order to study the impact of the VVC on the inverter lifetime, a lifetime estimation method is first presented. This method uses the Artemis urban and US06 driving cycles in order to obtain the thermal loading, and consequently the lifetime consumption of the inverter power devices. Then, the VSF-MPWM is proposed, which minimizes the switching loss by clamping any of the three-phase legs at the phase current peak and by reducing the number of commutations through variable switching frequency. However, in order to achieve an acceptable current quality, the proposed VSF-MPWM controls both the clamping period and the switching frequency according to the current quality constraints of the conventional PWM strategy. The impact of the VVC on the inverter lifetime and the performance of the proposed VSF-MPWM on the inverter power losses and current quality are investigated through MATLAB Simulink. The lifetime analysis reveals that the VVC has the ability to improve the lifetime of the inverter by a factor of 5.06 and 3.43 under Artemis urban and US06 driving cycles, respectively, compared to the conventional constant dc-bus voltage control (CVC). On the other hand, the simulation result shows that the proposed VSF-MPWM can save up to 35.4 % and 23.8 % of switching and power losses, respectively, compared to the conventional PWM. Meanwhile, the VSF-MPWM can obtain the same output current quality as that of the conventional PWM.

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α	Grade angle
M	Mass
v	Velocity
F_t	Tractive effort
F_R	Resisting forces
F_r	Rolling resistance
C_r	Rolling resistance coefficient
g	Gravitational acceleration
F_{ad}	Aerodynamic drag
ρ	Air density
C_d	Aerodynamic drag coefficient
A_f	Vehicle frontal area
F_g	Grade resistance
T	Motor torque
ω_m	Mechanical speed
i_g	Gear ratio of the gearbox
i_o	Differential gear ratio
r_d	Radius of the wheel
η_t	Transmission efficiency
d, q	Axis in the rotating reference frame.
V_{ds}, V_{qs}	Stator voltages in the d-q reference frame
i_{ds}, i_{qs}	Stator currents in the d-q reference frame
L_{ds}, L_{qs}	Winding inductances in the d-q reference frame
R_s	Stator resistance
P	Number of pole pairs
ψ_{pm}	Rotor flux produced by the permanent magnets
ω_m^*	Reference mechanical speed
T^*	Reference motor torque
i_{ds}^*, i_{qs}^*	Reference stator currents in the d-q reference frame
V_{ds}^*, V_{qs}^*	Reference stator voltages in the d-q reference frame
θ_m	Rotor position

V_{as}^*, V_{bs}^*, V_{cs}^*	Reference stator voltages in the *abc* reference frame
S_a, S_b, S_c	gating signals of the inverter
Δi_{ds}^*	Extra negative *d*-axis current for flux weakening
ω_{base}	Base speed
$V_{s\text{-}limit}$	Stator voltage limit
V_s^*	Reference stator voltage
$i_{s\text{-}limit}$	Stator current limit
n	Negative dc-bus
V_{dc}	Dc-bus voltage
S_1	Upper inverter switch of phase-*a*
S_4	Lower inverter switch of phase-*a*
V_{an}	Voltage from phase-*a* to the negative dc-bus
V_o	Output voltage vector of the inverter
V_1	Active voltage vector V_1 (100)
V_2	Active voltage vector V_2 (110)
V_0	Zero voltage vector V_0 (000)
V_7	Zero voltage vector V_7 (111)
V_{ref}	Reference voltage vector
θ	Position of the reference voltage vector
T_s	Sub-cycle duration
T_1	Dwell time of active voltage vector V_1
T_2	Dwell time of active voltage vector V_2
T_3	Dwell time of the two zero voltage vector V_0 and V_7
T_{sw}	Switching cycle duration
m_{tri}	Triangular carrier
f_{sw}	Switching frequency
m_{cmv}	Common mode voltage signal
m_{as}^*, m_{bs}^*, m_{cs}^*	Modulating signals of the inverter
I_1	RMS value of the fundamental current
I_n	RMS value of the *nth* harmonic current component
I_r	Current ripple
L_s	Equivalent stator winding inductance
V_Z	Applied voltage vector

N_f	Number of cycles to failure
T_{jm}	Mean junction temperature
ΔT_j	Thermal cycle amplitude
K_b	Boltzmann constant
E_a	Activation energy
a_1, a_2	Experimentally determined factors for lifetime estimation
n_i	Number of cycles at a certain stress level (T_{jm} and ΔT_j)
N_{fi}	Number of cycles to failure at a certain stress level (T_{jm} and ΔT_j)
LC	Accumulated damage
T_j	Power device junction temperature profile
$Z_{j\text{-}c}$	Junction to case thermal impedance
$Z_{c\text{-}h}$	Case to heat sink thermal impedance
$Z_{h\text{-}a}$	Heat sink to ambient thermal impedance
T_h	Temperature of the heat sink
T_a	Temperature of the ambient
R	Resistance
C	Capacitance
P_{loss}	Total losses of a power device
S_{up}	Upper inverter switch
$P_{C,T}(S_{up})$	Conduction loss of an IGBT in an upper inverter switch
$P_{C,D}(S_{up})$	Conduction loss of an FWD in an upper inverter switch
V_{ce}	IGBT on-state voltage drop
V_F	FWD on-state voltage drop
$T_{j,T}$	IGBT junction temperature
$T_{j,D}$	FWD junction temperature
i_{xs}	Stator phase current
$d_{xs}(S_{up})$	Duty ratio of an upper inverter switch
$P_{sw,T}(S_{up})$	Switching loss of an IGBT in an upper inverter switch
$P_{sw,D}(S_{up})$	Switching loss of an FWD in an upper inverter switch
E_{on}	IGBT turn on energy loss
E_{off}	IGBT turn off energy loss
E_{rr}	FWD reverse recovery energy loss
$V_{dc\text{-}ref}$	Reference dc-bus voltage in the manufacturer datasheet

p	Positive dc-bus
f_{nom}	Nominal switching frequency
I_{rp}	Peak current ripple over a fundamental cycle for the CSVPWM
I_{rms}	RMS current ripple over a fundamental cycle for the CSVPWM
V_B	Battery voltage
V_R	Rated dc-bus voltage
P_o	Motor output power
V_{dc}^*	Reference dc-bus voltage
D	gating signal of the dc-dc converter
V_{xs}	Stator phase voltage
t	Time
O	Origin point (0,0)
q_y, d_y	Corner points of Current ripple trajectory
$T_{s,nom}$	Nominal sub-cycle duration
$I^2_{(\text{sequence})}$	RMS current ripple over a sub-cycle for a switching sequence
$I^2_{(\text{CSVPWM})}$	RMS current ripple over a sub-cycle for the CSVPWM
$I^2_{(\text{DPWM})}$	RMS current ripple over a sub-cycle for the DPWM
i_{as}^*, i_{bs}^*, i_{cs}^*	Reference stator currents in the *abc* reference frame
K_f	Switching frequency coefficient

LIST OF ABBREVIATIONS

ICE	Internal combustion engine
EV	Electric vehicle
dc	Direct current
ac	Alternating current
PWM	Pulse width modulation
VVC	Variable dc-bus voltage control
CVC	Constant dc-bus voltage control
CSVPWM	Conventional space vector pulse width modulation
DPWM	Discontinuous pulse width modulation
VSF	Variable switching frequency
VSF-MPWM	Variable switching frequency modified pulse width modulation
PMSM	Permanent magnet synchronous motor
EMF	Back-electromotive force
MTPA	Maximum torque per ampere
FW	Flux weakening
MMF	Magnetomotive force
VSI	Voltage source inverter
CBPWM	Carrier based pulse width modulation
CCBPWM	Conventional carrier based pulse width modulation
CTHD	Current total harmonic distortion
RMS	Root mean square
Si	Silicon
DBC	Direct bonded copper
Cu	Copper
Al	Aluminium
CTE	Coefficient of thermal expansion
IGBT	Insulated gate bipolar transistor
FWD	Freewheeling diode
DPWM1	DPWM with clamping duration at the voltage reference peak
DPWM0	DPWM with clamping duration shifted by -30° with respect to DPWM1

DPWM2	DPWM with clamping duration shifted by +30° with respect to DPWM1
HP-PWM	High performance- pulse width modulation
ADPWM	Advanced discontinuous pulse width modulation
EMI	conducted electromagnetic interference
USV-RPWM	Universal space vector-random pulse width modulation
CSF	Constant switching frequency
VSF1	VSF using peak current ripple requirement
VSF2	VSF using RMS current ripple requirement
VSFSVPWM	Variable switching frequency space vector pulse width modulation
SPMSM	Surface permanent magnet synchronous motor
LUT	Lookup table
WBG	Wide bandgap
SiC	Silicon Carbide
GaN	Gallium Nitride

CHAPTER 1

INTRODUCTION

1.1 Background

In the last 100 years, the development of vehicles powered by internal combustion engine (ICE) have made a great contribution to the society by providing many of the needs for transportation in everyday life. However, the large number of ICE vehicles in use around the world has caused serious problems for the environment and humans. The soaring fuel prices due to the rapid resources depletion, Air pollution, and global warming due to the greenhouse gases emissions are problems of paramount concern (Ehsani, Gao, Longo, & Ebrahimi, 2018). In recent decades, the vehicle manufacturers and researchers have focused their attention on the development of vehicles to overcome these issues. The electric vehicle (EV) is believed to be the ultimate category to replace the ICE vehicle in the near future. EVs run on electricity only in which one or more traction motors propel the wheels using a rechargeable battery packs as the power source. Therefore, they produce zero emissions at the point of use. Moreover, they can reduce running costs dramatically because of the high efficiency of electric drivetrain components compared with the ICE (Mi & Masrur, 2017).

The EV is similar to the ICE vehicle except in the drivetrain. A drivetrain configuration in EV applications is shown in Figure 1.1. In this configuration, two-stage power converters (dc-dc converter and dc-ac converter) are used between the battery and the traction motor. The dc-ac converter (inverter) is necessary to control the speed and torque of the traction motor (Choudhury, 2015). On the other hand, the dc-dc converter is an optional converter and it is used to regulate the voltage of the dc-bus. Although, the additional dc-dc converter in this configuration adds some disadvantages like extra power losses and more complexity, it creates several advantages over the conventional configuration where the battery directly supplies the inverter. For instance, it has the advantage of improving the motor output without increasing the battery size and cost (Estima & Cardoso, 2012). In addition, it allows the use of batteries with lower voltages,

which can improve their lifetime since the spread in cell aging becomes less influential with lower number of series connections (Stippich et al., 2017). This configuration also permits manufacturers to design a multi-modular battery system with more than one battery technology (e.g. high-power and high-energy batteries) in parallelized configuration, which leads to significant reduction in their cost and size. The resulting cheaper and lighter battery system can effectively compensate for the additional size and cost of the dc-dc converter (Rothgang et al., 2015). This configuration has been successfully verified for EVs as a part of multi-modular architecture in the publicly funded projects *Europahybrid* and *e performance* (Stippich et al., 2017), and thus its implemented in this thesis.

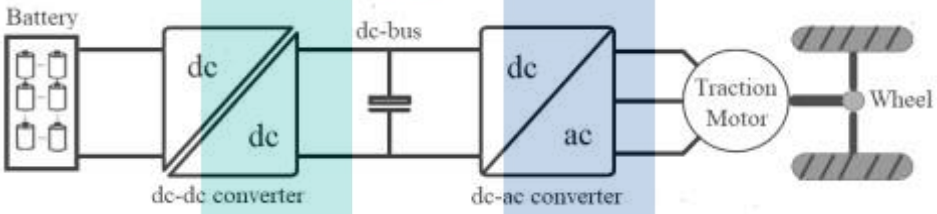

Figure 1.1 Drivetrain configuration for electric vehicle.

The electric drivetrain consists of several components as shown in Figure 1.1. Each of these components has some requirements that must be satisfied. Regarding the inverter, the performance requirements includes low cost, minimum size, minimum power losses, and long life (Kimura et al., 2014). According to (Kent, 2012), the power converters are among the most stressed and less reliable drivetrain components. In addition, they contribute the greatest cost of EV after batteries when compared to the conventional ICE vehicle. Therefore, the fulfilment of these requirements when designing the inverter is critical for the success of EV adoption.

The low reliability of the inverter can be significantly attributed to the power devices. In automotive applications, the torque and speed operating point of the traction motor depends on several factors such as the driving behavior and road conditions. The large variation in the torque and speed creates a large fluctuation in the inverter loading, and consequently on the temperature within the power devices. In addition, the temperature of the surrounding environment varies significantly over seasons. The resulting temperature fluctuation put large thermal stress on the internal connections of the power device, which can lead to fatigue and eventually failure (Wang, Cai, Du, &

Zhou, 2017). Hence, in order to meet the lifetime requirements, an adequate thermal management system that is able to keep the temperature within the power devices at specific limit is indispensable. Unfortunately, this often comes at the expense of increased size and cost of the system (Lemmens, Driesen, & Vanassche, 2013). Another possibility is to focus on the heat source instead of the heat sink. The temperature and power losses of the power device are proportional. By minimizing power losses, the thermal stress can be reduced and thus the lifetime of the inverter can be improved. Moreover, reducing the power losses can extend the EV range since the power demands under a given loading conditions is reduced. The power losses reduction can be achieved via hardware improvements, but also great potential lies in the control and pulse width modulation (PWM) strategies as well, which are the focus of this thesis.

1.2 Problem Statement

The inverter is a key component in the EV. It is the energy conversion unit between the dc-bus and the ac traction motor. The requirements for inverter design in EV applications include low power losses to ensure good driving range, low cost, long life, and minimum size due to the limited space of the vehicle. The development of inverter which can improve these aspects is essential for the success of EV's. However, these requirements may contradict with each other. For instance, reducing the size and cost of the inverter requires reduction in the size and cost of the thermal management system. Meanwhile, a properly designed thermal management system is necessary to maintain the components temperatures within a safe limit and to meet the targeted lifetime. In EV applications, there is a trend to replace the current liquid cooling system with a cheaper and smaller air cooling system. To make this possible, new developments in the control strategy, packaging, and components are necessary to compensate for the reduced performance of the air cooling system (Morya et al., 2019; Azar & Tavassoli, 2014).

Apart from the thermal management system, the power loss reduction represents another possibility to reduce the thermal stress and to improve the lifetime of the power converter. The inverter power losses depend on the dc-bus voltage. With the aid of the dc-dc converter, the inverter power losses can be reduced by dynamically adjusting the dc-bus voltage as a function of the motor operating conditions. Considerable research has been carried out to show the impact of variable dc-bus voltage control (VVC) on the inverter power losses (Roche, Shabbir, & Evangelou, 2017; Najmabadi, Humphries, &

Boulet, 2016; Estima & Cardoso, 2012; Prabhakar et al., 2016), but only limited verification has been carried out to show its effect on the lifetime improvement. In (Lemmens et al., 2013), the impact of the VVC on the thermal stress of the inverter power devices is investigated and compared with the conventional constant dc-bus voltage control (CVC). It is Concluded that the thermal stress can be significantly reduced with the aid of VVC. Nevertheless, the advantage of reduced thermal stress is not discussed in terms of lifetime.

The effect of VVC on the inverter power losses becomes less evident as the speed increases. Therefore, in order to reduce the power losses, especially at high speed, other strategies should be considered. The power losses of the inverter depend also on the modulation strategy and the switching frequency, which can be exploited through the PWM strategy. Replacing the conventional space vector PWM (CSVPWM) with an advanced modulation strategy like discontinuous PWM (DPWM) (Asiminoaei, Rodriguez, & Blaabjerg, 2008), or reducing the average switching frequency through variable switching frequency (VSF) scheme (Jiang & Wang, 2013) can contribute considerable amount of power losses reduction without adding extra cost to the system. However, these strategies may also have negative impact on the quality of the current waveform compared to the CSVPWM. In fact, bad current quality increases the motor harmonic losses, which decreases the operational efficiency of the motor, especially at low torque levels, where the harmonic losses due to PWM becomes dominant in the total electrical losses. The traction motor in EV applications works frequently at low torque conditions. Therefore, high harmonic losses can adversely affect the driving range of the vehicle (Miyama et al., 2016; Yamazaki, Togashi, Ikemi, Ohki, & Mizokami, 2019). In this regard, several modified PWM strategies which take current quality into consideration are presented. These strategies can be classified into two types. The first type employs DPWM instead of CSVPWM whenever it has higher current quality (Das, Narayanan, & Pandey, 2014), whereas the second type applies VSF under the current quality constraints of the CSVPWM (Bhattacharya, Sharma, Mascarella, & Joós, 2017). These two types can achieve good amount of inverter power losses saving at high speed. Although However, the performance can be improved if the switching frequency and the modulation strategy are simultaneously controlled, which has not been considered for research according to the review of the literature.

1.3 Thesis Objectives

This research aims to achieve the following objectives:

i. To evaluate the inverter lifetime using variable dc-bus voltage control and constant dc-bus voltage control under different driving conditions.

ii. To propose a new PWM strategy called variable switching frequency modified PWM (VSF-MPWM) for the inverter in electric vehicle applications.

iii. To analyse the inverter power losses under the proposed PWM strategy, conventional PWM strategy, and existing modified PWM strategies.

1.4 Thesis Contribution

Following are the key contributions of this research:

i. A detailed comparison study between VVC and CVC regarding their effect on the inverter lifetime is conducted. The CVC also represents the configuration where the battery directly supplies the inverter. Therefore, this study presents the advantage of having an additional dc-dc converter on the inverter lifetime. The lifetime analysis with these two control strategies is conducted under urban and highway driving conditions. This adds more accuracy and credibility to the comparison since it considers the effect of different driving behaviours and road conditions on the thermal stress of the power devices.

ii. A new VSF-MPWM strategy for the inverter in EV applications is proposed in this thesis. This strategy is designed in such a way to combine both the first and second type of the modified strategies, which promises a significant power loss reduction at high speed due to the combined effect of the DPWM and VSF schemes. Meanwhile, it is designed to produce the same current quality as that of the CSVPWM.

All stages of this study are performed using MATLAB/Simulink, giving the advantage of a common simulation platform.

1.5 Thesis Outline

This thesis consists of five chapters. Chapter 1 includes the background, problem statement, thesis objectives, and thesis contribution.

Chapter 2 discusses the previous studies related to the objectives of the present research. The past and recent development of control and PWM strategies to reduce the inverter power losses are summarized and evaluated. In addition, this chapter provides a review of the literature concerning the models and concepts that helps to conduct this research. The vehicle modeling, motor control in EV applications, current quality evaluation, inverter topology, and power devices loss calculation, thermal modeling, and lifetime estimation are presented.

Chapter 3 presents the overall system and the required methods to achieve the objectives of this research. It is divided into three parts. The first part presents the drivetrain configuration and its control structure. In the second part, the steps for applying the lifetime estimation study is presented. Finally, the concept, design, and implementation of the proposed VSF-MPWM are explained in the third part.

Chapter 4 includes the results and discussion of the intended research. This chapter is also divided into three parts. the first part presents the behavior of the dc-bus voltage and the motor control under VVC. In the second part, the advantage of using VVC on the inverter lifetime is verified through detailed comparison with the conventional CVC. Finally, the effect of the proposed VSF-MPWM on the inverter power losses and current quality is investigated through comparison with the CSVPWM and existing modified PWM strategies.

Chapter 5 summarizes the research findings and gives recommendations for future work.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter starts with a brief discussion on the vehicle model design followed by an overview of the fundamental theory of motor control in electric vehicle applications. In addition, an overview of the most commercially accepted inverter topology, conventional PWM strategy, and current quality evaluation are presented. The next part of this chapter is related to power losses and reliability and it discusses briefly the main failure mechanism, thermal modelling, lifetime estimation, and power losses calculation for power devices in the inverter. Moreover, some control and PWM strategies proposed in the literature to reduce the inverter power losses are introduced and evaluated in detail.

2.2 Vehicle Model

To obtain similar operating conditions to the real world for the traction motor and power converters, it is very essential to consider a realistic vehicle load profile (driving cycle). However, such a profile is always given in terms of the velocity versus time. In this case, a vehicle model is required. The vehicle model is used to convert the vehicle driving cycle into torque-speed profile of the traction motor by considering the vehicle motion and dynamic equations. The vehicle motion can be determined by analyzing the forces acting on the vehicle in the direction of motion. The forces acting on a vehicle moving up a grade α are shown in Figure 2.1. Here, a vehicle of mass M moving at a velocity v is considered. The tractive effort (F_t) is the force generated by the traction motor to propel the vehicle. This force has to overcome the resisting forces, which includes the rolling resistance, aerodynamic drag, and grading resistance, and the force to accelerate the vehicle. The required tractive effort can be mathematically expressed as shown in Equation 2.1.

$$F_t = \left(F_r + F_{ad} + F_g\right) + M\frac{dv}{dt} \quad 2.1$$

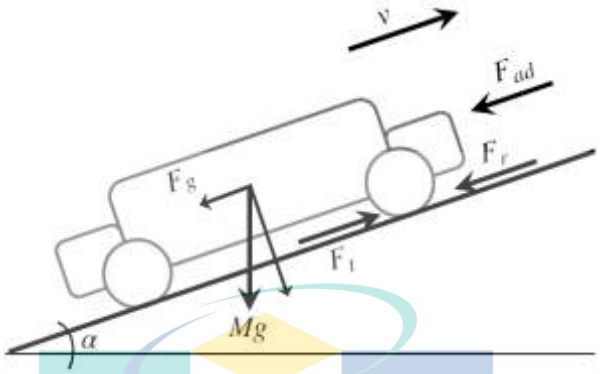

Figure 2.1 Vehicle model.
Source: Mi & Masrur (2017).

The resisting forces (F_R) are shown by the first three terms in Equation 2.1. The first term represents the rolling resistance (F_r), which mainly caused due to the interaction of the tire with the ground. This force depends on the rolling resistance coefficient (C_r), acceleration due to gravity (g), M, and α. The second term is the aerodynamic drag (F_{ad}), which is produced due to the air resistance. This force depends on the air density (ρ), aerodynamic drag coefficient (C_d), vehicle frontal area (A_f), and v. Finally, the grade resistance (F_g) is the force produced due the road grade, which depends on M, g, and α. These three terms can be rewritten as shown in Equation 2.2 (Mi & Masrur, 2017; Degrenne & Mollov, 2016).

$$F_R = C_r Mg\cos\left(\alpha\right) + 0.5\rho C_d A_f v^2 + Mg\sin\left(\alpha\right) \quad 2.2$$

For a traction motor-driven vehicle, the vehicle tractive effort comes from the motor shaft through a clutch, gearbox (transmission), possibly a differential gear, drive shaft, and driving wheels. Hence, the effective value of the motor torque (T) and speed (ω_m) can be expressed as shown in Equations 2.3 and 2.4, respectively (Ehsani et al., 2018).

$$T = \frac{F_t \times r_d}{i_g \times i_o \times \eta_t} \quad 2.3$$

$$\omega_m = \frac{v \times i_g \times i_o}{r_d} \quad 2.4$$

Where i_g is the gear ratio of the gearbox, i_o is the differential gear ratio, r_d is the radius of the wheel, and η_t is the transmission efficiency from the motor to the driving wheels. When Equations 2.1 to 2.4 are fed with a load profile, the torque-speed commands of the motor can be obtained.

2.3 Motor Control in EV Applications

The basic requirements for traction motors in EV applications includes high torque at low speed for starting and hill climbing, wide speed range, high efficiency, and minimum size. Because of this, permanent magnet synchronous motor (PMSM) are preferred as these motors have the highest torque density and efficiency to date (Sepulchre, Fadel, Pietrzak-David, & Porte, 2018). The dynamic model of a PMSM in the rotating *d-q* reference frame for the stator voltages and torque are shown in Equations 2.5 to 2.7.

$$V_{ds} = R_s i_{ds} + L_{ds} \frac{di_{ds}}{dt} - \omega_m i_{qs} L_{qs} \quad 2.5$$

$$V_{qs} = R_s i_{qs} + L_{qs} \frac{di_{qs}}{dt} + \omega_m i_{ds} L_{ds} + \omega_m \psi_{pm} \quad 2.6$$

$$T = \frac{3}{2} P \left(\psi_{pm} i_{qs} + \left(L_{ds} - L_{qs} \right) i_{ds} i_{qs} \right) \quad 2.7$$

Where "V_{ds}, V_{qs}'', "i_{ds}, i_{qs}", and "L_{ds}, L_{qs}" are the *d-q* stator voltages, stator currents, and winding inductances, respectively, R_s is the stator resistance, P is the number of pole pairs, and ψ_{pm} is the rotor flux produced by the permanent magnets. The control of traction motors in EV applications can be divided into two regions as follows: low-speed region and high-speed region.

2.3.1 Low-Speed Region

This region is also referred to as constant torque region since maximum torque can always be provided. In this region, the inverter feeding the motor has always enough

voltage to counteract the induced voltage due to the back-electromotive force (EMF), where the EMF generated is typically proportional to the motor speed. The control objective in this region is to produce the minimum stator current for a given torque value. This can be achieved using a convenient current control strategy, such as maximum torque per ampere (MTPA). The control structure in this region is depicted in Figure 2.2. In the outer loop, the motor speed is regulated. Then, the error between the reference speed (ω_m^*) and the measured speed is applied to speed regulator to generate the reference torque (T^*). Using Equation 2.7 and MTPA strategy, the reference torque is converted to *d-q* reference stator currents (i_{ds}^* and i_{qs}^*). In the inner control loop, the measured stator currents are individually regulated by two current regulators, which produce an output that are further decoupled into *d-q* reference voltages (V_{ds}^* and V_{qs}^*). Finally, using V_{ds}^*, V_{qs}^*, and the rotor position (θ_m), the three-phase reference voltages (V_{as}^*, V_{bs}^*, and V_{cs}^*) can be obtained and applied to PWM generator to produce the gating signals (S_a, S_b, and S_c) of the inverter (Abad, 2017).

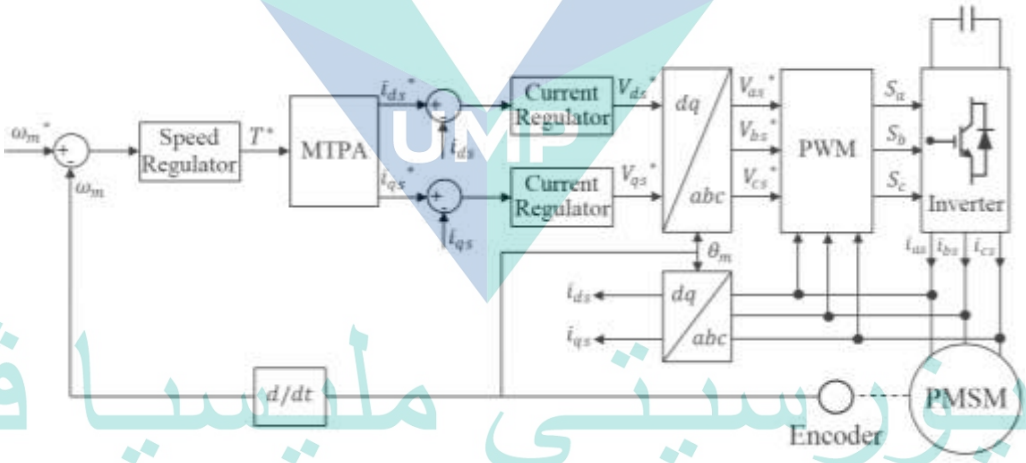

Figure 2.2 PMSM control block diagram.

2.3.2 High-Speed Region

As the speed increases and particularly at a speed called the base speed, the EMF approaches the maximum available voltage from the inverter. As a result, the speed can't be further increased as no voltage is left to produce current. However, it is possible to increase the speed further by adding extra negative *d*-axis current to reduce V_{qs} (see Equation 2.6) until the stator voltage matches the stator voltage limit. This process is known as flux weakening (FW) since the negative *d*-axis current creates a demagnetizing magnetomotive force (MMF) opposes the MMF established by the permanent magnets.

The extra negative *d*-axis current (Δi_{ds}^*) can be mathematically expressed as shown in Equation 2.8, with ω_{base} the base speed which can calculated as seen in Equation 2.9 (Li, 2014).

$$\Delta i_{ds}^{\ *} = \frac{\omega_{base}}{\omega_m}\frac{\psi_{pm}}{L_{ds}} - \frac{\psi_{pm}}{L_{ds}} \tag{2.8}$$

$$\omega_{base} = \frac{V_{s-limit}}{\sqrt{\left(i_{ds}L_{ds} + \psi_{pm}\right)^2 + \left(i_{qs}L_{qs}\right)^2}} \tag{2.9}$$

Where $V_{s\text{-}limit}$ is stator voltage limit. The FW operation can be implemented using feedback-based FW regulator as shown in Figure 2.3. The reference stator voltage (V_s^*) is compared with $V_{s\text{-}limit}$. If V_s^* is greater than $V_{s\text{-}limit}$, the FW regulator produce negative Δi_{ds}^* which is then added to i_{ds}^* provided by the MTPA strategy. This enables the speed to increase without exceeding $V_{s\text{-}limit}$. On the contrary, if the FW is not required ($\omega_m < \omega_{base}$), the FW regulator produce zero Δi_{ds}^* since V_s^* is less than $V_{s\text{-}limit}$. It is also seen that the controller imposes limitations to i_{qs}^* according to the new value of i_{ds}^* in order to keep the stator current within the stator current limit ($i_{s\text{-}limit}$). This limitation decreases the torque production capability since the *q*-axis current is responsible in most of torque production (Abad, 2017).

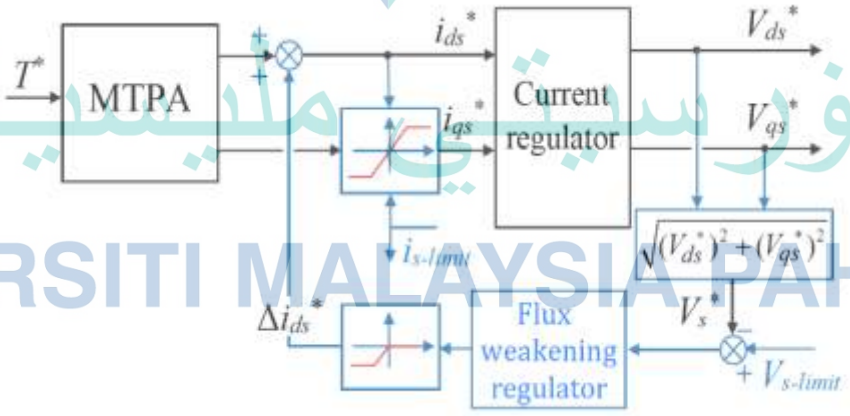

Figure 2.3 Flux weakening regulator.

Source: Abad (2017)

2.4 Inverter Topology and Conventional Pulse Width Modulation

Power electronic technology is an enabling technology for the development of EV systems. The selection of an appropriate topology and PWM strategy are an important issues to develop an efficient and high performance EV (Rajashekara, 2013). Regarding the dc-ac converter, the two-level voltage source inverter (VSI) is the most widely used inverter topology in EV applications. This is because of its advantages in terms of cost, reliability, and efficiency over other inverter topologies like current source inverter, Z-source inverter, and multi-level VSI (Ye, Yang, & Emadi, 2012). The three-phase two-level VSI is shown in Figure 2.4. This topology comprises of six power switches (S_1- S_6). Each two switches are connected in series to form an inverter leg and the terminals of the ac motor are connected at the mid-point of each leg.

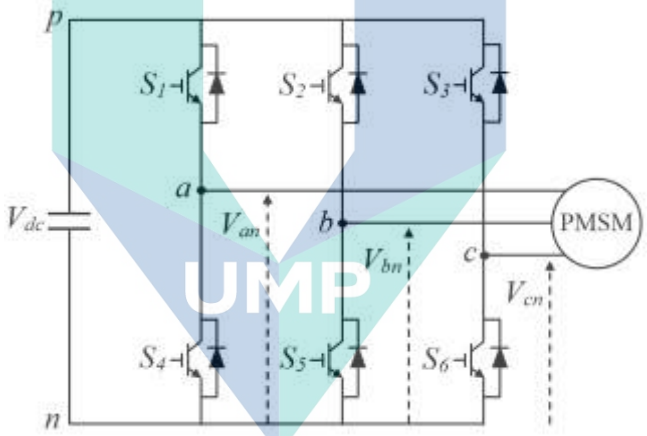

Figure 2.4 Three-phase two-level voltage source inverter (VSI).

In this topology, the output voltage from any phase (*a*, *b*, or *c*) to the negative dc-bus (*n*) can take only one out of two values, either the dc-bus voltage (V_{dc}) or 0. Talking phase-*a* as an example, V_{an} equals V_{dc} when S_1 is on and S_4 is off. On the other hand, V_{an} equals 0 when S_1 is off and S_4 is on. The desired states of the power switches (on or off) are determined through the gating signals, which takes the binary values "1" and "0" for an output voltage V_{dc} and 0, respectively. The output voltage vector (V_o) of the inverter can then be expressed as shown in Equation 2.10 (Kwak & Park, 2014).

$$V_o = \frac{2}{3} V_{dc} \left(S_a + S_b e^{j\left(\frac{2\pi}{3}\right)} + S_c e^{j\left(\frac{4\pi}{3}\right)} \right) \qquad 2.10$$

By substituting all possible combinations between S_a, S_b, and S_c into Equation 2.10, a total of eight possible voltage vectors (V_0 to V_7) can be produced as shown in Figure 2.5. The magnitudes are shown normalized with respect to $2/3V_{dc}$. The binary values shown alongside each voltage vector in brackets are the inverter states, which represent the gating signals as (S_a S_b S_c). The two zero states (000 and 111) produce voltage vectors (V_0 and V_7) of zero magnitude. On the other hand, each of the other six active states produce an active voltage vector of 1 p.u magnitude. These active vectors (V_1 to V_6) divide the space vector diagram into six equivalent sectors.

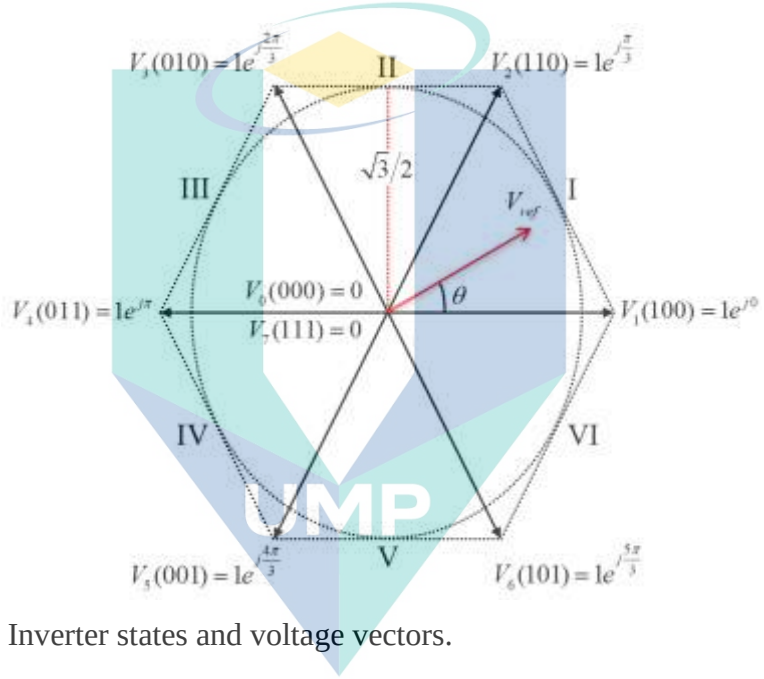

Figure 2.5 Inverter states and voltage vectors.

The required voltage vector and the time duration at which it is applied are determined in the motor control loop via the PWM strategy. One of the most efficient PWM strategies to do this is the space vector PWM. In space vector PWM, the vector sum of the three-phase reference voltages gives a revolving reference voltage vector of magnitude (V_{ref}) and angle (θ), where V_{ref} can take any value between 0 and $\sqrt{3}/2$ p.u. The maximum value of V_{ref} corresponds to the radius of the largest circle that can be contained within the hexagon as shown by the red dotted line in Figure 2.5. The resulting reference voltage vector is then synthesized in every sub-cycle duration (T_s) using the nearest two active vectors and the two zero vectors. However, the two zero vectors have the same magnitude and angle. Hence, one of them or both could be used. Given V_{ref} and θ in sector-I as shown in Figure 2.5, the active vector V_1 (100), active vector V_2 (110), and one or both of the two zero vectors (V_0 (000) and V_7 (111)) are applied, whereas there dwell

times in the sub-cycle are given by T_1, T_2, and T_3, respectively, in Equations 2.11 to 2.13 (Narayanan, Zhao, Krishnamurthy, Ayyanar, & Ranganathan, 2008).

$$T_1 = V_{ref} \frac{\sin(60-\theta)}{\sin(60)} T_s \quad 2.11$$

$$T_2 = V_{ref} \frac{\sin(\theta)}{\sin(60)} T_s \quad 2.12$$

$$T_3 = T_s - (T_1 + T_2) \quad 2.13$$

In conventional space vector PWM (CSVPWM), the time T_3 is equally divided between V_0 and V_7. To minimize the number of commutations, each phase should not switch more than once in every sub-cycle. Talking sector-I as an example, CSVPWM employs sequence $V_0V_1V_2V_7$ in one sub-cycle and sequence $V_7V_2V_1V_0$ in the next. This results in three switching instances in every sub-cycle and a total of six switching instances in two consecutive sub-cycles as shown in Figure 2.6. The time of two consecutive sub-cycles is also referred to as the switching cycle (T_{sw}). The CSVPWM is the most widely used PWM strategy for the inverter in EV applications (Menon, Azeez, Kadam, & Williamson, 2018; Choudhury, 2015). Hence, it's considered in this thesis as benchmark to evaluate all other PWM strategies.

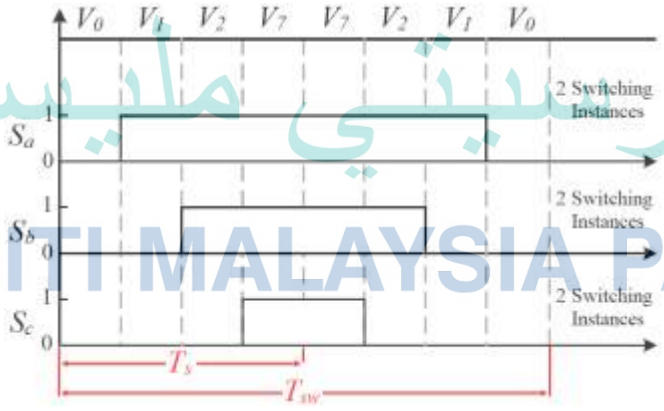

Figure 2.6 CSVPWM switching sequence.

It should be noticed that the same sequence in Figure 2.6 can be generated by using carrier based PWM (CBPWM). In conventional CBPWM (CCBPWM), the three phase reference voltages are compared with a common triangular carrier (m_{tri}) as shown in Figure 2.7(a). The frequency of the triangular carrier is called the switching frequency

(f_{sw}), which is equal to 1/ T_{sw}. Considering phase-*a*, when V_{as}^* is greater than m_{tri}, the gating signal S_a is equal to 1. On the other hand, when V_{as}^* is less than m_{tri}, the gating signal S_a is equal to 0. In this way, the switching sequence of the inverter can be generated. However, this process well not produce the same sequence of the CSVPWM since the time T_3 will not be equally divided between the two zero vectors. In order to generate the same sequence of the CSVPWM, a common mode voltage signal (m_{cmv}) must be added to V_{as}^*, V_{bs}^*, and V_{cs}^*. The common mode voltage signal is calculated as shown in Equation 2.14, while the resulting modulating signals (m_{as}^*, m_{bs}^*, and m_{cs}^*) are shown in Figure 2.7(b) (Kitidet & Kumsuwan, 2016).

$$m_{cmv} = -0.5\left(\max\left(V_{as}^*, V_{bs}^*, V_{cs}^*\right) + \min\left(V_{as}^*, V_{bs}^*, V_{cs}^*\right)\right) \quad 2.14$$

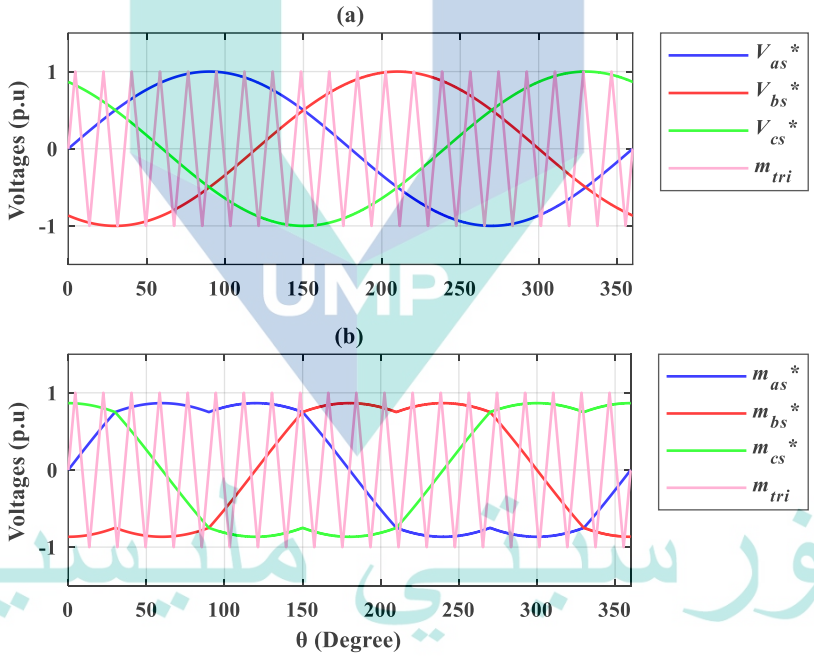

Figure 2.7 (a) CCBPWM (b) CSVPWM sequence generation with CBPWM.

2.5 Current Ripple and Harmonic Distortion

The operation of the inverter under PWM signal is highly efficient in controlling the motor power flow. However, since it has discrete switching states, the output voltage and current waveforms are not exactly sinusoidal. The PWM operation generate inverter output waveforms which contain a rich harmonic spectrum. This spectrum contains the desired fundamental component as well as other harmonic components at the integer multiples of the switching frequency. In motor drive applications, there is no strike

requirement on the harmonic components. However, the motor losses depend on the harmonics in the output current waveform. The exact relationship is beyond the scope of this thesis, but in general, higher current harmonics increase the motor losses (Sharma, 2016). Therefore, it is essential to evaluate the quality of the output current waveform under a PWM strategy prior the implementation in an actual system. In doing so, the current total harmonic distortion (CTHD) can be used. The CTHD can be calculated as shown in Equation 2.15, where I_1 is the RMS value of the fundamental current and I_n is the RMS value of the *nth* harmonic current component.

$$\mathrm{CTHD} = \frac{1}{I_1}\sqrt{\sum_{n\neq 1} I_n^{\,2}} \qquad 2.15$$

Alternatively, the output current quality can be evaluated using time domain analysis, rather than calculating every individual harmonic component, and thereby, the CTHD. In time domain analysis, the current ripple is estimated in every sub-cycle (or may be switching cycle) by integrating the error voltage vector, which represents the difference between the applied voltage vector and the reference voltage vector. For an inverter driving a PMSM, the current ripple (I_r) in a sub-cycle can be expressed as follows:

$$I_r = \frac{1}{L_s}\int_0^{T_s}\left(V_Z - V_{ref}\right)\ dt \qquad 2.16$$

Where L_s is the equivalent stator winding inductance and V_Z (Z= 0 to 7) is the applied voltage vector. Using Equation 2.16 and a given switching sequence, the RMS value of the current ripple over a sub-cycle and consequently over the whole fundamental cycle can be obtained (Narayanan et al., 2008). The RMS current ripple over a fundamental cycle is a measure of the CTHD, which can be effectively used to evaluate the current quality under any PWM strategy. The current ripple depends on the PWM strategy as well as the switching frequency. For instance, the CSVPWM leads to lower current ripple than the CCBPWM. In addition, higher switching frequency reduce the current ripple. The impact of the PWM strategy and the switching frequency on the current ripple (or CTHD) will be discussed in more detail in subsection 2.7.2.2.

2.6 Reliability of Power Devices in EV Applications

The reliability of power converters in EV applications has attracted considerable attention in recent years. In these applications, the power converters experience higher failure rate than other subsystems. As most power converters are not designed with redundancy, a malfunction of any component in the converter may prevent the vehicle to operate. The unexpected interruption causes safety concerns and results in high operation and maintenance cost (Song & Wang, 2013).

The reliability of the power converter can be determined by its most vulnerable elements. According to an industrial survey (S. Yang et al., 2011), the power devices were rated as the most components prone to failure in the power converter. The internal structure of a typical power device is shown in Figure 2.8. In such a device, the silicon (Si) chips are soldered to the upper surface of an electrically insulating ceramic direct bonded copper (DBC) substrate, which in turn attached to a copper (Cu) baseplate by solder. For the electrical connections between the chips and substrate, aluminum (Al) bond wires are typically used (L. Yang, Agyakwa, & Johnson, 2013).

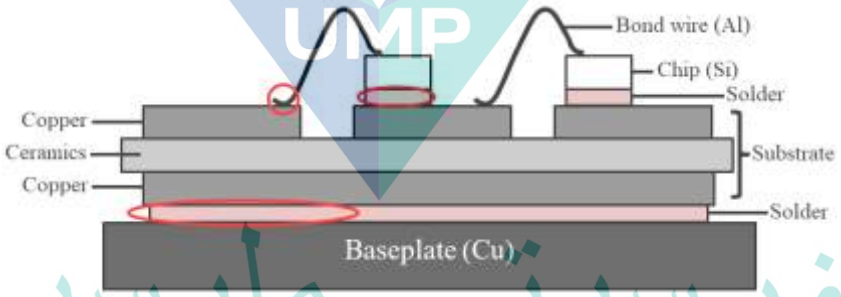

Figure 2.8 Internal structure of a typical power device.

The failure of the power devices can be attributed either to failure on the chip or failure on the packaging. The chip related failures are mainly caused by excessive stresses, such as transient over voltage and over current. These failures are not related to the age of the device and usually they are included in the protection circuit and excluded from the reliability studies (Wang et al., 2017). On the other hand, the package related failures are mainly driven by thermomechanical stresses experienced by the materials inside the power devices during temperature fluctuation (Falck, Felgemacher, Rojko, Liserre, & Zacharias, 2018). As shown in Figure 2.8, the path from chips to baseplate consists of different materials, where each has different coefficient of thermal expansion

(CTE). When exposed to temperature fluctuation, the power devices experience repeated thermal cycling, which creates mechanical stresses at different locations inside the device due to the difference in CTE. The parts more susceptible to thermal cycling are the bond wire, the solder between chip and substrate, and the solder between substrate and baseplate, which are shown highlighted in red in Figure 2.8. With frequent repetition of thermal cycles, the resulting stress leads to several failure mechanisms, such as bond wire lift-off and solder joints fatigue (Musallam, Yin, Bailey, & Johnson, 2015; Andresen et al., 2018). These failures are the basic of reliability studies and are the focus of this thesis.

2.6.1 Lifetime Model for Power Devices

The aim of lifetime estimation is to investigate the time period at which a component can perform its required function without expecting a failure. The lifetime of a power device based on the damage accumulated due to thermal cycling can be estimated using Coffin-Manson-Arrhenius model shown in Equation 2.17. The number of cycles to failure (N_f) is expressed in dependency of the device mean junction temperature (T_{jm}), thermal cycle amplitude (ΔT_j), Boltzmann constant (K_b = 1.381*10^{-23} J/K), and activation energy (E_a = 9.891*10^{-20} J). Other factors like a_1 and a_2 are determined from a data set of multiple reliability experiments, which have a value of 3.025*10^5 and -5.039, respectively, as illustrated in (Wintrich, Nicolai, Tursky, & Reimann, 2015).

$$N_f = a_1 \times \left(\Delta T_j\right)^{a_2} \times \exp\left(\frac{E_a}{K_b \times T_{jm}}\right) \quad 2.17$$

The lifetime model in Equation 2.17 can be employed to estimate the number of cycles to failure at a certain stress level (T_{jm} and ΔT_j). However, the vehicle operating conditions is usually irregular, which leads to irregular junction temperature in terms of amplitude and mean values over time. To overcome this issue, the irregular profile should be divided into several regular cycles. This can be achieved by using cycle counting algorithm, such as rainflow counting. The rainflow counting algorithm is a widely used technique and its available on Mathworks Web site (Nieslony, 2010). When this algorithm is employed to the junction temperature profile, a rainflow matrix can be obtained. The results of this matrix are the number of cycles (n_i) for each combination of the mean junction temperature and thermal cycle amplitude. Consequently, the Miner's

rule can be used to rate the impact of all cycles resulted from the rainflow counting algorithm as shown in Equation 2.18.

$$LC = \sum_i \frac{n_i}{N_{fi}} \tag{2.18}$$

Where LC is the lifetime consumption (or accumulated damage), n_i is the number of cycles at a certain stress level (T_{jm}, and ΔT_j), and N_{fi} is the number of cycles to failure calculated from Equation 2.17 at that stress level. When LC is accumulated to unity, the device reaches its end of life (Sangwongwanich, Yang, Sera, Blaabjerg, & Zhou, 2018).

2.6.2 Thermal Model of Power Devices

Information on junction temperature (T_j) is crucial for determining the lifetime of the power devices as shown in Equation 2.17. In this regard, a thermal model is required. The commonly used thermal model to obtain the junction temperature is based on single heat transfer path from chip to coolant. Figure 2.9 shows a simple thermal model for a single power device mounted on a heat sink through an interface, such as thermal grease. The values $Z_{j\text{-}c}$, $Z_{c\text{-}h}$, and $Z_{h\text{-}a}$ are the junction to case, case to heat sink, and heat sink to ambient thermal impedances, respectively, P_{loss} is the total power losses of the device, while T_h and T_a are the temperature of the heat sink and ambient, respectively. The $Z_{j\text{-}c}$ is shown herein as a four-layer foster R-C network as usually given in the manufacturer datasheet. Using this model, the junction temperature is mathematically expressed as shown in Equation 2.19 (Andresen, Schloh, Buticchi, & Liserre, 2016; Liu et al., 2018).

$$T_j = T_a + \left(Z_{j-c} + Z_{c-h} + Z_{h-a}\right) \times P_{loss} \tag{2.19}$$

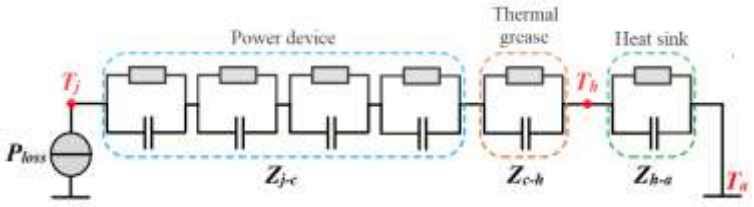

Figure 2.9 Thermal model of a single power device mounted on a heat sink.
Source: Liu (2018).

2.7 Inverter Power Losses

2.7.1 Power Loss Model for Power Devices

The inverter power devices losses calculation is a very important issue as it allows to calculate temperature within the device (see Equation 2.19) and provide a guideline for thermal management design and system efficiency improvement. Insulated gate bipolar transistors (IGBTs) are the commonly used power devices for inverters in electric vehicle applications. The IGBT is a unidirectional device, meaning it can only switch current in the forward direction. Therefore, in order to allow a bidirectional flow of current, each IGBT in the inverter are provided with an anti-parallel freewheeling diode (FWD). The total power loss (P_{loss}) for any of these two devices is the sum of two main sources, which are conduction loss and switching loss.

Conduction loss is the loss that occur in the power device when it is conducting current (on-state). For any inverter leg, the devices that are conducting depends on the direction of the phase current. For instance, when the phase current is positive, the upper IGBT and the lower FWD are switching on and off in a complementary fashion. When the phase current is negative, these two devices are always off and the other two devices (lower IGBT and upper FWD) are switching. The IGBT and FWD conduction loss for any of the upper switches of the inverter (S_{up}) can be calculated as shown in Equations 2.20 and 2.21, respectively (Lemmens, Vanassche, & Driesen, 2014).

$$P_{C,T}\left(S_{up}\right)=\begin{cases}\left|i_{xs}\right|\times V_{ce}\left(i_{xs},T_{j,T}\right)\times d_{xs}\left(S_{up}\right) & i_{xs}>0\\ 0 & i_{xs}\le 0\end{cases} \quad 2.20$$

$$P_{C,D}\left(S_{up}\right)=\begin{cases}0 & i_{xs}>0\\ \left|i_{xs}\right|\times V_{F}\left(i_{xs},T_{j,D}\right)\times d_{xs}\left(S_{up}\right) & i_{xs}\le 0\end{cases} \quad 2.21$$

Where "V_{ce}, V_F'' and "$T_{j,T}$, $T_{j,D}$" are the IGBT and FWD on-state voltage drop and junction temperature, respectively, i_{xs} ($x = a, b, c$) is the stator phase current, and d_{xs} (S_{up}) is duty ratio of the upper switch of phase-x, which can be calculated based on the corresponding modulating signal (m_{xs}^{*}) and the dc-bus voltage as shown in Equation 2.22.

$$d_{xs}\left(S_{up}\right)=\frac{1+\left(\frac{m_{xs}^{*}}{V_{dc}/2}\right)}{2} \tag{2.22}$$

On the other hand, the switching loss is the type of loss that occurs due to the non-ideal characteristic of the power device. During turn on, the device current increases from zero to the phase current and the voltage drops to almost zero. Since this transition does not occur instantaneously, both current and voltage are non-zero which causes some power to be dissipated. During turn off, the device behaves in vice versa (Khayamy & Chaoui, 2018). The IGBT and FWD switching loss for any of the upper switches can be calculated from Equations 2.23 and 2.24, respectively, where E_{on}, E_{off}, and E_{rr} are the turn on, turn off, and reverse recovery energy losses, respectively, and $V_{dc\text{-}ref}$ is the reference voltage given in the datasheet of the power device (Falck, Andresen, & Liserre, 2015).

$$P_{sw,T}\left(S_{up}\right)=\begin{cases}\left(E_{on}\left(i_{xs},T_{j,T}\right)+E_{off}\left(i_{xs},T_{j,T}\right)\right)\times f_{sw}\times\dfrac{V_{dc}}{V_{dc-ref}} & i_{xs}>0\\ 0 & i_{xs}\le 0\end{cases} \tag{2.23}$$

$$P_{sw,D}\left(S_{up}\right)=\begin{cases}0 & i_{xs}>0\\ E_{rr}\left(i_{xs},T_{j,D}\right)\times f_{sw}\times\dfrac{V_{dc}}{V_{dc-ref}} & i_{xs}\le 0\end{cases} \tag{2.24}$$

It can be seen that the switching loss of the device depends on the dc-bus voltage and the switching frequency. Higher dc-bus voltage and switching frequency increase the switching loss and vice versa. It is also worth mentioning that Equations 2.23 and 2.24 are valid if the inverter leg is switching. If not, the switching loss falls to zero. For instance, some PWM strategies like discontinuous PWM, which will be introduced in the next subsection, clamps an inverter leg continuously to the positive (p) or negative dc-bus for a period of time. In this case, the switching loss over that period is equal to zero regardless of the phase current direction (sign).

The conduction and switching losses for an IGBT and FWD in any of lower switches can be calculated in similar fashion. However, the only difference is that the lower devices dissipate power in the opposite direction of the phase current. For instance,

the IGBT in any of the lower switches dissipate power when the corresponding phase current is negative and for a duty ratio equal to 1-d_{xs} (S_{up}).

2.7.2 Control and PWM Strategies for Inverter Power Losses Reduction

Power losses reduction is one of the main requirements for inverters in EV applications. As shown in Equation 2.19, the power losses and junction temperature of the power device are proportional. By minimizing power losses, both amplitude and mean value of the junction temperature can be reduced, which reduces the lifetime consumption as shown in Equations 2.17 and 2.18. In addition, by minimizing the inverter losses, the power demands under a given loading condition is reduced and consequently, the EV range can be improved. The power losses of the power device include conduction and switching loss. Conduction loss is static and almost depends on the device technology. On the other hand, the switching loss depends on several factors, such as the dc-bus voltage, switching frequency, and phase current amplitude through the switch during commutation. Regarding the first factor, a variable dc-bus voltage control can be employed to reduce the switching loss. On the other hand, the other two factors can be exploited through the PWM technique. In the literature, several PWM methods were proposed to replace the CSVPWM, which include discontinuous PWM and variable switching frequency. Many of these PWM strategies can reduce the switching loss of the inverter. However, they may also have negative impact on the CTHD compared to CSVPWM, which can increase the motor losses. Therefore, it is of great interest to limit the raise on the CTHD when designing the PWM strategy. In this thesis, some PWM strategies that can reduce the inverter switching loss well be presented. In addition, their impact on the CTHD well be highlighted. A further details regarding the variable dc-bus voltage control and the PWM strategies are provided in the following sections.

2.7.2.1 Variable Dc-Bus Voltage Control (VVC)

With VVC, the dc-bus voltage can be adjusted to the required motor stator voltage, which in turn depends on the motor torque and speed operating point. Due to the speed-dependent EMF, the required stator voltage to control the motor at low speeds is less than at rated speed. Therefore, the switching loss of the inverter power devices at low speeds can be minimized by reducing the dc-bus voltage. However, this strategy can only be employed for such an application where a dc-dc converter is connected to the

terminals of the dc-bus. Moreover, it has no effect on the inverter losses at high-speed region as the maximum dc-bus voltage is required from the point where flux weakening is necessary (Prabhakar et al., 2016; Estima & Cardoso, 2012).

One of the main advantages of the VVC is the ability to provide considerable reduction of the junction temperature fluctuation within inverter power devices. This is due to the fact that the VVC can effectively reduce the inverter power losses at low speed and high torque region, which is considered as one of the most severe operating conditions for inverters in EV applications. Compared with the same torque level at high speed, the device junction temperature at low speed shows larger fluctuation and reach higher peak values. This is because, the junction temperature variation follows the load current during a fundamental cycle. When the fundamental frequency decreases, the heating and cooling times are higher and consequently, the thermal cycles are higher (Andresen & Liserre, 2014; Bryant, Mawby, Palmer, Santi, & Hudgins, 2008). The ability of the VVC to reduce the junction temperature fluctuation is investigated in (Lemmens et al., 2013). However, no verification has been carried out to show the effect of this reduction on the inverter lifetime, which is going to be explored in this thesis.

2.7.2.2 PWM Strategies for Inverter Switching Loss Reduction

The switching loss reduction can be achieved by using a unique modulation strategy called discontinuous PWM (DPWM). Unlike CSVPWM, DPWM uses only one zero vector for voltage vector synthesize. Considering a reference voltage vector in sector-I as shown in Figure 2.5, the active vectors that are used are active vector V_1 (100) and active vector V_2 (110). In these two vectors, the gating signal of phase-*a* is equal to one. Therefore, when V_7 (111) is used, S_a is clamped to one (see Figure 2.10(a)), and thus the phase-*a* inverter leg is clamped to the positive dc-bus. On the other hand, when V_0 (000) is considered, S_c is clamped to zero (see Figure 2.10(b)), and the phase-*c* inverter leg is clamped to the negative dc-bus. The DPWM strategies uses switching sequences with only two switching transitions over a sub-cycle, which results in 33 % reduction on the average switching frequency compared to CSVPWM. To ensure a comparison at the same average switching frequency, the switching frequency for the DPWM must be multiplied by a factor of 3/2 (Narayanan et al., 2008).

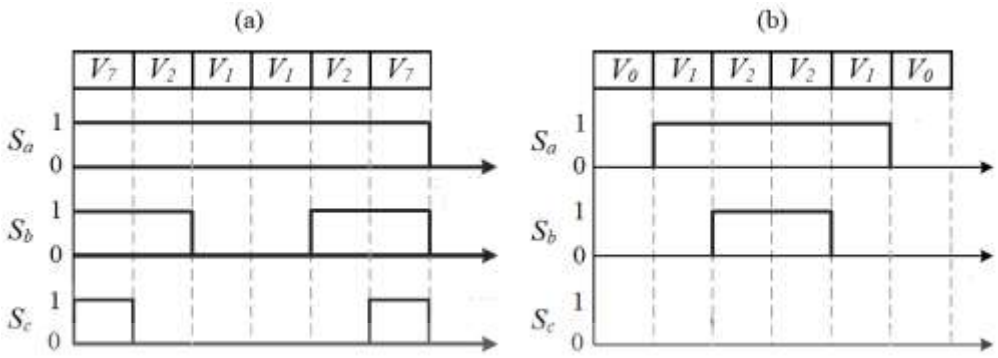

Figure 2.10 Gating signals of the inverter (a) using sequence $V_7V_2V_1$ or $V_1V_2V_7$, (b) using sequence $V_0V_1V_2$ or $V_2V_1V_0$.

With DPWM, every phase is clamped for 120° duration of the fundamental cycle divided equally between the positive and negative dc-bus. When the clamped regain perfectly align the current peak, a 25 % switching loss reduction can be achieved compared to CSVPWM. In this regard, several DPWM methods are proposed to Suit different load power factors. For instance, DPWM1 has the clamping duration at the voltage reference peak. Therefore, the maximum loss saving can be achieved for unity power factor load. Other DPWM strategies like DPWM0 and DPWM2 has the clamping duration shifted by -30° and +30°, respectively, with respect to DPWM1 (Aguirre, Madina, Poza, Aranburu, & Nieva, 2012). Hence, the DPWM0 and DPWM2 achieve maximum switching loss saving at 30° leading and 30° lagging power factor load, respectively. Using space vector PWM, these DPWM strategies can be realized by an appropriate selection of the zero voltage vector as shown in Figure 2.11. On the other hand, the modulating signals which produce the same DPWM strategies using CBPWM are shown for phase-*a* in Figure 2.12.

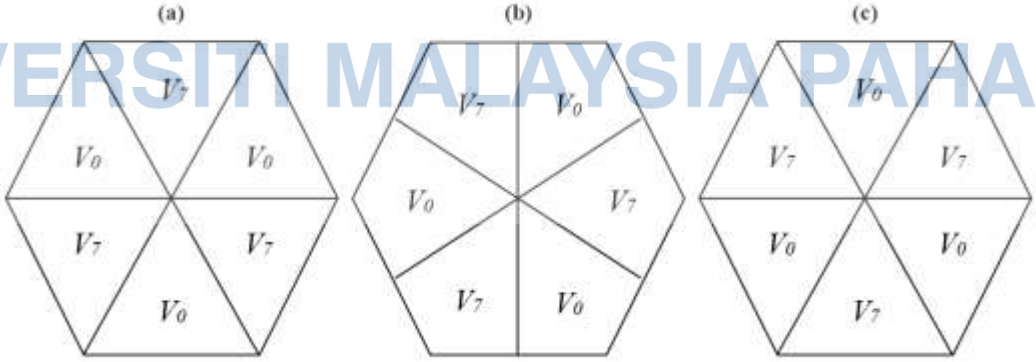

Figure 2.11 Zero voltage selection for (a) DPWM0, (b) DPWM1, (c) DPWM2.

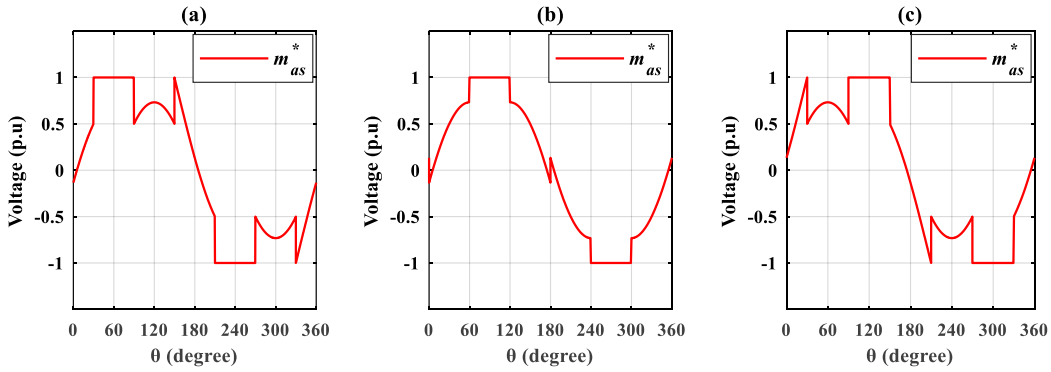

Figure 2.12 Phase-*a* modulating signals with (a) DPWM0, (b) DPWM1, (c) DPWM2.

The aforementioned DPWM are proposed for such an application where the operating power factor is approximately constant. In EV applications, the motor is subjected to operate with variable power factor (Choudhury, Pillay, & Williamson, 2016). Therefore, by applying one of the preceding DPWM schemes, the maximum loss saving can only be achieved in a small portion of the operating region. This problem is solved in (Nguyen, Hobraiche, Patin, Friedrich, & Vilain, 2011), where a generalized DPWM strategy is presented. Using the current feedback loop, the DPWM strategy is automatically changed in order to align the peak current duration. In this way, the maximum possible switching loss saving can always be achieved. However, in spite of their superior performance in terms of loss saving, these modulation schemes have poor CTHD compared to the CSVPWM at low and medium values of V_{ref}. To solve this issue, a modified PWM method called high performance-PWM (HP-PWM) is proposed in (Hava, Kerkman, & Lipo, 1998). In this method, the modulation strategy (DPWM or CSVPWM) is selected based on the RMS current ripple over a fundamental cycle. Therefore, the DPWM is only applied at high values of V_{ref}, where the RMS current ripple over a fundamental cycle of the DPWM is less than that of the CSVPWM.

To further reduce the switching loss of the inverter, an advanced DPWM (ADPWM) approach is proposed in the literature (Prasad & Narayanan, 2014; Das et al., 2014; Zhao, Hari, Narayanan, & Ayyanar, 2010). Similar to the DPWM, ADPWM also uses one zero vector. However, the only difference is that one of the active vectors is applied twice in a sub-cycle. In this regard, two additional sequences were presented, which are sequence $V_7V_2V_1V_2$ and $V_0V_1V_2V_1$. These two sequences have high loss saving abilities which can even surpass the preceding DPWM at some operating power factor.

However, they have extremely poorer CTHD compared to CSVPWM and DPWM schemes.

Instead of changing the modulation strategy and while still using CSVPWM, applying variable switching frequency (VSF) represents another degree of freedom to reduce the switching loss. In the literature, several VSF strategies are proposed to accomplish different purposes, such as acoustic noise reduction (Kumar, A. B., & Narayanan, 2016), conducted electromagnetic interference (EMI) reduction (Chen, Jiang, & Li, 2018), and switching loss reduction (F. Yang, Taylor, Bai, Cheng, & Khan, 2015). In this thesis, some of the VSF that can affect the inverter switching loss well be presented. In addition, their impact on the CTHD well be highlighted.

One possibility to design a VSF scheme is to vary the switching frequency randomly. This type of VSF schemes is mainly designed to reduce the acoustic and EMI noises. For instance, The universal space vector-random PWM (USV-RPWM) strategy in (Peyghambari, Dastfan, & Ahmadyfard, 2016) varies the switching frequency based on a random number within two predefined limits in order to eliminate the noise at a selected frequency from the voltage spectrum. The two limits have the same deviation above and below the switching frequency of the constant switching frequency (CSF) scheme, whereas the random number is selected from a limited set of numbers (k_{min} to k_{max}). The average switching frequency of the USV-RPWM depends on the switching frequency range (upper and lower limits), the set of numbers in which random number is selected, and the selected frequency for elimination from the voltage spectrum. Therefore, it can be concluded that, the USV-RPWM affects the inverter switching loss and CTHD depending on the average switching frequency. However, this effect is uncontrollable, which is also the case for many other random PWM methods proposed in the literature (Kumar, A. B., & Narayanan, 2016; Jiang & Wang, 2013).

Another approach is to vary the switching frequency in order to satisfy certain requirements on current ripple. With constant switching frequency (CSF) scheme, the current ripple shape is not fixed and it's varying with respect to V_{ref} and θ. Accordingly, two methods are proposed to vary the switching frequency. First, based on the peak current ripple (VSF1). Second, based the RMS current ripple (VSF2). Considering CSVPWM and a nominal switching frequency f_{nom}, the peak and RMS current ripple over the whole fundamental cycle are I_{rp} and I_{rms}, respectively. With VSF1, the peak current

ripple in every switching cycle (or may be sub-cycle) is maintained constant at I_{rp} by changing the switching frequency (Chen et al., 2018; F. Yang et al., 2015). In this case, the switching frequency varies considerably below f_{nom} at high values of V_{ref} where the current ripple variation is large and hence, an appreciable switching loss reduction can be achieved. However, this improvement is accompanied with significant CTHD increase compared to CSVPWM. On the contrary, VSF2 is able to maintain the same CTHD levels of the CSVPWM by considering I_{rms} as a constraint. In every sector, the RMS current ripple over a switching cycle is higher than I_{rms} at the middle of the sector while it becomes lower than I_{rms} at the two boundaries. Hence, the switching frequency is reduced below f_{nom} near the two boundaries and increased above f_{nom} around the middle of the sector. The required switching frequency deviation above f_{nom} is lower than the required deviation below f_{nom}, which results in a reduction on the avarage switching frequency (Kumar, A. B., & Narayanan, 2016). However, the reduction is small and thus the switching loss saving is not that much significant (Jiang & Wang, 2013).

To improve the performance of VSF1 in terms of CTHD, a modified PWM method called VSF space vector PWM (VSFSVPWM) is proposed in (Bhattacharya et al., 2017). This strategy employs a coefficient adjustment factor in order to limit the switching frequency variation with VSF1. This factor decreases the switching loss reduction capabilities. However, an acceptable CTHD compered to CSVPWM can be obtained in this case. Similarly, to improve the performance of VSF2 in terms of switching loss reduction, another modified PWM strategy known here as optimaized VSF were proposed in (Tran, Truong, & Le, 2016; Y. Xia, Roy, & Ayyanar, 2017; Onederra, Kortabarria, de Alegría, Andreu, & Gárate, 2017). The switching losses is also dependent on the line current amplitude. Therefore, the switching loss can be further reduced if high switching frequency is prevented during large current amplitude. In doing so, the RMS current ripple over a switching cycle is allowed to go above and below I_{rms}. However, the total RMS current ripple over a fundamental cycle should obey I_{rms}. This method is implemented using optimization. The results show that this method has the ability to maintain the same CTHD of the CSVPWM with good switching loss saving capabilities near unity power factor. Nevertheless, it shows large dependency on the power factor of the load as the switching loss reduction capabilities can be dramatically reduced at a slightly lower power factor.

To conclude this subsection, Table 2.1 provides summary for the advantages and disadvantages (or limitations) of the discussed PWM strategies in terms of their effect on the inverter switching loss and CTHD compared to the CSVPWM. The USV-RPWM is excluded from this table since it has uncontrollable effects. The rest of the PWM strategies are classified into two types. The first type depends on the modulation strategy to reduce the switching loss of the inverter, whereas the second type depends on the switching frequency control.

Table 2.1 Review of PWM strategies in terms of inverter power losses and CTHD

Type	**Method**	**Advantages**	**Disadvantages/ Limitations**
Modulation Strategy Selection	DPWM	High switching loss saving	High CTHD
	ADPWM	High switching loss saving	High CTHD
	HP-PWM	High switching loss saving at high values of V_{ref} with good CTHD	The performance in terms of switching loss saving can be improved if the switching frequency is also controlled
Switching Frequency Control	VSF1	High switching loss saving at high values of V_{ref}	High CTHD
	VSF2	Certain amount of switching loss saving at high values of V_{ref} with good CTHD	The switching loss saving is small
	Optimized VSF	High switching loss saving at unity power factor with good CTHD	The switching loss saving is very sensitive to the variation in the load power factor
	VSFSVPWM	Good switching loss saving at high values of V_{ref} with good CTHD	The performance in terms of switching loss saving can be improved if the modulation strategy is also controlled

From both types, the DPWM, ADPWM, and VSF1 can provide significant amount of switching loss saving, but their performance regarding the CTHD is bad compared to that of the CSVPWM. The VSF2 can solve the issue of VSF1 in terms of CTHD. However, this comes at the expense of considerably reduced switching loss saving capabilities. The performance of the modified PWM strategies, such as HP-PWM, VSFSVPWM, and optimized VSF are as follows. First, the optimized VSF has the ability to maintain the same CTHD of the CSVPWM with good switching loss saving abilities

which can reach up to 19 % near unity power factor according to (Onederra et al., 2017). However, the switching loss saving reduces only to 5 % when the power factor is around 0.93 lagging, which makes it inappropriate method for EV applications where the power factor changes considerably with respect to motor torque and speed. Second, the HP-PWM and VSFSVPWM can provide good amount of power losses saving at high motor speed (high values of V_{ref}) without affecting the CTHD by controlling either the modulation strategy or the switching frequency based on the RMS current ripple of the CSVPWM. However, the performance can be improved if the switching frequency and the modulation strategy are simultaneously controlled.

2.8 Summary

In this chapter, different principles are Summarized like vehicle mathematical modelling, motor control, and current ripple evaluation. Although, the main focus has been given to the inverter and particularly to the power losses and reliability of the power devices. Regarding reliability, the main cause of failure has been identified as the thermal stress and consequently, an overview of lifetime model that explore the link between the temperature of the device and lifetime consumption has been summarized. To reduce the power losses, the variable dc-bus voltage control as well as the PWM strategies like discontinuous PWM and variable switching frequency have been presented and evaluated. The side effects of the PWM strategies on current quality and the limitation of the VVC in terms of availability are highlighted as well. This chapter also addresses two main issues. First, no work has been found in the literature regarding the impact of the VVC on the inverter lifetime. Second, the discussed PWM strategies that are proposed to replace the CSVPWM either do not take CTHD into consideration or their performance in terms of switching loss saving can be further improved. This chapter has addressed these issues to fill the gap, and this will be discussed in the following chapters.

CHAPTER 3

METHODOLOGY

3.1 Introduction

This chapter presents the overall system and the required methods to achieve the objectives of this study. The design and control of the selected drivetrain configuration is discussed in section 3.2. In section 3.3, the steps for applying the lifetime estimation study are presented. This chapter also introduces a new variable switching frequency modified PWM (VSF-MPWM) strategy for three-phase two level VSI. The aim of this strategy is to minimize the inverter switching loss as possible while still obtaining similar CTHD as that of the CSVPWM. This trade-off is achieved by controlling both the switching frequency and the modulation strategy (either CSVPWM or DPWM) based on the RMS current ripple. The principle and design of this strategy is explained in detail in section 3.4. In addition, a flowchart showing the steps for applying the proposed strategy is presented in the same section.

3.2 System Description

The schematic diagram of Figure 3.1 shows the drivetrain configuration and its control structure, which is implemented using MATLAB Simulink environment. The drivetrain includes a battery, dc-dc converter, inverter, and traction motor. On the other hand, the control structure includes two control loops. The upper loop for dc-bus voltage regulation and the lower loop for motor control. The specifications are detailed in subsections 3.2.1 and 3.2.2.

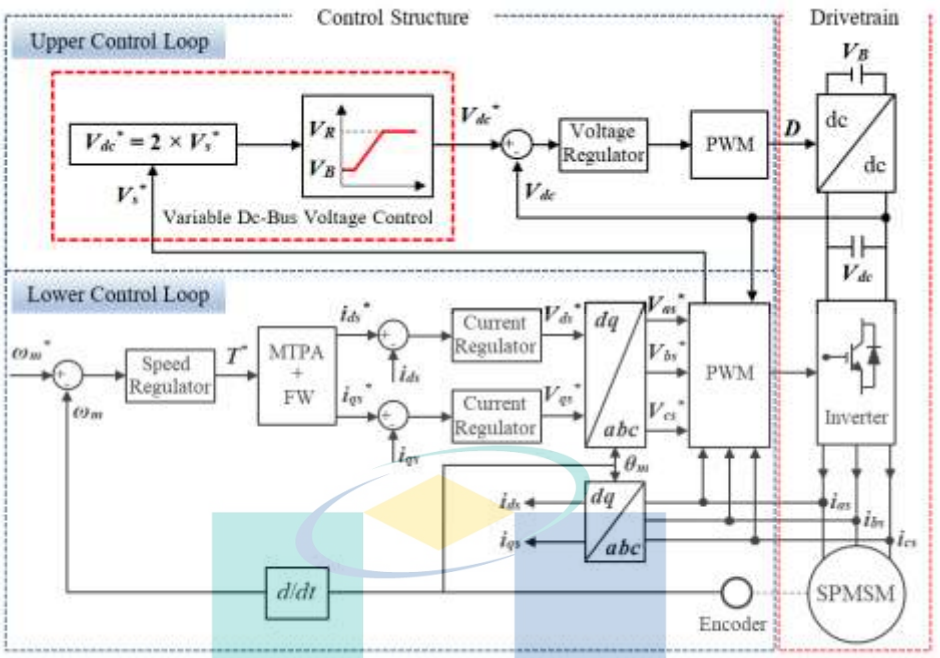

Figure 3.1 Drivetrain configuration and its control structure.

3.2.1 Drivetrain Configuration

Starting with the traction motor, a surface type permanent magnet synchronous motor (SPMSM) is selected. The ratings of the SPMSM are listed in Table 3.1. Regarding the input voltage of the system, a battery voltage (V_B) of 200 V is used, which can be amplified by the dc-dc converter into a maximum of 400 V. To control the SPMSM, a three-phase two-level VSI, which consists of six power devices, is used (see Figure 2.4). The switching operation of the power devices in this inverter topology is explained in section 2.4. Regarding the ratings, the inverter power devices should be selected so that the rated voltage is higher than the maximum dc-bus voltage of the system, and the rated current is higher than the motor stator current at the rated torque. In this regard, an IGBT module from Infineon with a product part number of FF400R07KE4 is chosen as the inverter power devices. The voltage and current ratings of this module are 650 V and 400 A, respectively, whereas a detailed specification regarding the switching energy loss, on-state voltage drop, thermal impedances, and maximum junction temperature can be found in the datasheet in the Appendix.

Table 3.1 SPMSM ratings

Parameter	Value
Rated power	$P_{o\ (rated)}$ = 70 kW
Rated torque	T_{rated} = 210 Nm
Rated speed	$n_{m\ (rated)}$ = 3200 RPM
Permanent magnets flux linkage	Ψ_{pm} = 0.1039 V.s
d-axis inductance	L_{ds} = 0.25 mH
q-axis inductance	L_{qs} = 0.25 mH
Number of pole pairs	P = 4
Stator resistance	R_s = 0.05 Ω

3.2.2 Control Structure

The control structure contains two control loops as shown in Figure 3.1. In the lower control loop, the motor speed and torque are controlled through the inverter. This process is described in detail in section 2.3. On the other hand, the upper control loop is used to regulate the dc-bus voltage through the dc-dc converter. The control of the dc-bus voltage can be achieved using CVC or VVC. Under CVC, the dc-dc converter directly supplies the inverter with the rated dc-bus voltage of 400 V. Regarding VVC, the dc-bus voltage is adjusted according to the motor stator voltage. The control of the dc-bus voltage using VVC can be described as follows: when applying PWM signal to the inverter, the dc-bus voltage is converted to three-phase stator voltages to drive the traction motor. The relationship between the reference stator voltage and the dc-bus voltage is shown in Equation 3.1.

$$V_s^* = \frac{2 \times V_{dc} \times V_{ref}}{3} \quad 3.1$$

When the dc-bus voltage is held constant at its rated value, the reference voltage vector changes with respect to the reference stator voltage. On the other hand, using VVC, the dc-dc converter is controlled to impose a dc-bus voltage that keeps the reference voltage vector near its maximum value. In this thesis, the reference voltage vector is fixed at 0.75 p.u rather than its maximal value, which is √3/2 p.u, in order to avoid pulse dropping caused by the ripple in the reference command. The control strategy is illustrated in Figure 3.1. The reference stator voltage is sent to the dc-bus voltage regulation loop. Using Equation 3.1 and assuming V_{ref} = 0.75 p.u, the reference dc-bus voltage (V_{dc}^*) is calculated and sent to voltage regulator and PWM generator to obtain

the gating signal (D) of the dc-dc converter. However, when the required stator voltage is very low, V_{dc}^* will be the lowest voltage of the dc-dc converter, which is imposed by the battery voltage. Under this condition, the reference voltage vector will drop below 0.75 p.u. On the other hand, V_{dc}^* is upper bounded by the rated dc-bus voltage (V_R) (Estima & Cardoso, 2012).

3.3 Lifetime Estimation

The lifetime of the inverter power devices can be significantly affected by the operating conditions of the system. For instance, the torque and speed of the vehicle determine the operating conditions of the inverter, which will be finally translated into thermal stress of the power devices. This thermal stress can lead to the device failure after a certain number of thermal cycles (Sangwongwanich et al., 2018). Therefore, considering a realistic vehicle operating conditions is an essential step for accurate lifetime estimation. The required torque and speed of the vehicle depend on several factors, such as the driving behavior and road conditions. Knowing exactly beforehand the driving patterns of the vehicle under all circumstances is quite challenging. Fortunately, many countries have developed several driving cycles like the NEDC, FTP-72, Artemis, and US06 in order to assess the performance of the vehicle. Using some of these driving cycles, the typical road conditions that are commonly encountered can be taken into consideration (Mi & Masrur, 2017). In this thesis, the Artemis urban and US06 driving cycles shown in Figure 3.2(a) and (b), respectively, are selected. The Artemis urban is used to simulate the urban driving conditions, whereas the US06 is used to simulate the highway driving conditions.

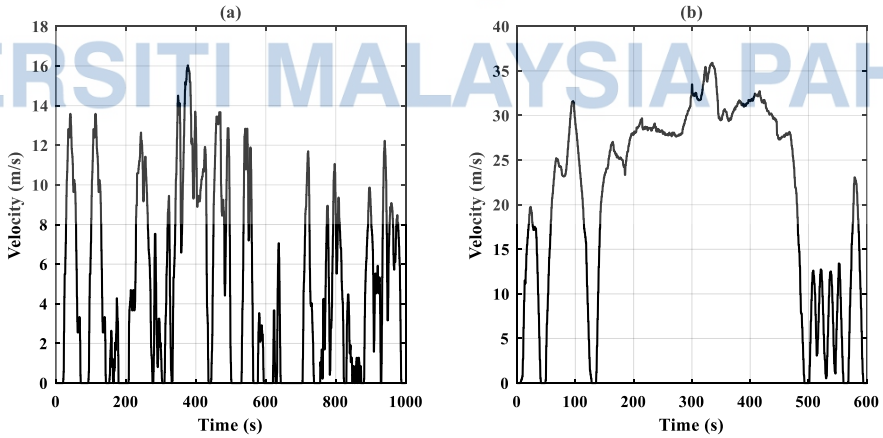

Figure 3.2 (a) Artemis urban, (b) US06 driving cycles.

In Figure 3.3, a flow diagram showing the steps for estimating the lifetime of the inverter power devices is indicated. As shown, five functional models like the vehicle model, motor model, loss model, thermal model, and lifetime model are included in order to estimate the lifetime consumption under a given driving cycle.

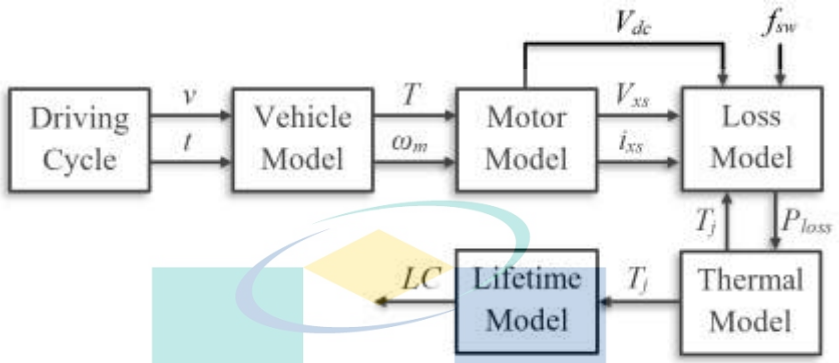

Figure 3.3 Flow diagram for lifetime estimation of the inverter power devices.

The driving cycle generates a sequences of vehicle velocities over time, which are utilized by a vehicle model (see Equations 2.1 to 2.4) to determine the required torque and speed that needs to be satisfied by the SPMSM. The required torque and speed depend on the vehicle parameters, aerodynamic drag coefficient, and rolling resistance coefficient. Herein, these parameters are obtained from the literature (Soldati, Pietrini, Dalboni, & Concari, 2018; Ehsani et al., 2018) and are shown summarized in Table 3.2. The road angle in this model is assumed zero since the driving cycle do not provide the trajectory followed by the vehicle.

Table 3.2 Parameters of the vehicle model

Parameter	Value
Vehicle mass	M =1180 kg
Vehicle Frontal area	A_f = 2 m^2
Rolling resistance coefficient	C_r = 0.01
Aerodynamic drag coefficient	C_d = 0.3
Wheel Radius	r_d = 0.343
Gearbox ratio	i_g = 6.5
Differential gear	i_o = 1
Air density	ρ = 1.29 kg/m^3
Gravitational acceleration	g = 9.8 m/s^2
Transmission efficiency	η_t = 0.9

The next step is to determine the stator voltages and currents at a given values of T and ω_m. Unfortunately, the detailed system model in Figure 3.1 can't be used herein to acquire these information's. The small sampling time of this model and the large amount

of data generated under a certain driving cycle represent a real problem. With this model, the simulation hangs after tens of seconds, which makes it impossible to be used for long-term simulation lasting up to 1000 second as shown in Figure 3.2. To solve this issue, a simplified motor model is built based on the mathematical representations of the SPMSM in the *d-q* reference frame. Using the obtained values from the vehicle model, the motor model computes directly the *d-q* stator currents and voltages based on Equations 2.5 to 2.9 as well as the stator voltage and current limits. The voltage limit is determined based on the rated dc-bus voltage and a reference voltage vector of 0.75 p.u. On the other hand, the current limit is calculated from the stator current at the rated torque of the SPMSM. Then, the stator voltages and currents in the *d-q* reference frame are converted into equivalent values in the *abc* reference frame (V_{xs} ($x = a, b, c$) and i_{xs}) using inverse park transformation. Finally, the dc-bus voltage under VVC can be obtained by using Equation 3.1 at V_{ref} = 0.75 p.u and the dc-bus voltage limit given by V_B and V_R. It should be noticed that the selected traction motor should be able to meet the performance requirements of the vehicle, which mainly includes maximum speed, gradeability, and the required acceleration time from low speed (usually zero) to a certain speed under a given vehicle parameters (Mi & Masrur, 2017). In this thesis, the SPMSM ratings in Table 3.1 are selected so that a sufficient torque is ensured under the vehicle parameters in Table 3.2 and the driving cycles in Figure 3.2.

Afterwards, using the obtained stator voltages, stator currents, and dc-bus voltage as well as other factors like the switching frequency and device junction temperature, the total power losses (P_{loss}) in any power device in the inverter (IGBT and FWD) can be calculated as described in subsection 2.7.1 and the information given in the manufacturer datasheet. The FF400R07KE4 datasheet provides the switching energy loss and the on-state voltage drop as a function of the load current at 125 °C and 150 °C junction temperatures. In order to take current and temperature dependencies into consideration, the datasheet values are stored in lookup tables (LUT's). In this study, the switching energy loss and the on-state voltage drop are stored in two different LUT's, where each LUT contains two curves at 125 °C and 150 °C junction temperatures. The accuracy of the curves is increased by considering the values of the switching energy loss and the on-state voltage drop at 10 different values of the load current in the range from 0 to 600 A. It should be noticed that the power losses in the lifetime estimation study are calculated based on a 10 kHz switching frequency and using CSVPWM as the modulation strategy.

Once P_{loss} is calculated, the junction temperature profile can be obtained from the thermal model of the power device (see Equation 2.19). As described in subsection 2.6.2, the thermal impedances from junction to case, case to heat sink, and heat sink to ambient should be obtained in order to build the thermal model. The junction to case and case to heat sink thermal impedances can be extracted from the FF400R07KE4 datasheet, whereas the heat sink to ambient thermal impedance is related to the design of the heat sink, which is an application dependent. In this thesis, the analysis is simplified by assuming constant heat sink temperature at 70 °C. This assumption is valid since practical vehicles are usually provided with a dedicated liquid cooling system, which can guarantee stable base temperature for the power converters and motor. In this case, the heat sink to ambient thermal impedance is not necessarily known (Lemmens et al., 2014; Stupar, Bortis, Drofenik, & Kolar, 2010). Finally, by applying the obtained junction temperature profile to the lifetime model as described in subsection 2.6.1, the lifetime consumption of the inverter power devices can be estimated.

3.4 Proposed Variable Switching Frequency Modified PWM (VSF-MPWM)

The switching loss of the power devices can be minimized by reducing the switching frequency. In addition, replacing the CSVPWM with DPWM is another degree of freedom to reduce the switching loss. The proposed VSF-MPWM aims to minimize the switching loss through both the switching frequency and the modulation strategy. However, in order to achieve an acceptable CTHD, the VSF-MPWM updates the switching frequency and the modulation strategy (either CSVPWM or DPWM) in every sub-cycle so that the RMS current ripple of the CSVPWM over a fundamental cycle is not exceeded. In doing so, the VSF-MPWM includes three main steps. First, RMS current ripple prediction. Second, modulating strategy selection. Finally, switching frequency control. These three steps will be elaborated in detail in subsections 3.4.1 to 3.4.3. In addition, a flowchart showing the complete steps is provided in subsection 3.4.4.

3.4.1 RMS Current Ripple Prediction

In a two-level VSI, the reference voltage vector is formed using eight discrete voltage vectors (V_0 *to* V_7). The deviation between the applied voltage vector (V_Z (Z = 0 to 7)) and the reference voltage vector (V_{ref}) is the error voltage vector (V_Z-V_{ref}), which result in the output current ripple. For a given reference voltage vector in sector-I, the error

voltage vectors due to the application of vectors V_0, V_1, V_2, and V_7 are indicated by red colours in Figure 3.4(a). Using Equation 2.16 and a given switching sequence, the RMS current ripple over a sub-cycle (T_s) can be analyzed in α-β (C. Xia et al., 2017), *abc* (Grandi, Loncarski, & Dordevic, 2015; Jiang & Wang, 2014), or in the *d*-*q* reference frame (Das & Narayanan, 2014). In this thesis, the analysis in the *d*-*q* reference frame will be considered due to its simplicity, where the *q*-axis is aligned to V_{ref} and the *d*-axis is 90° apart from the *q*-axis component as seen in Figure 3.4(a).

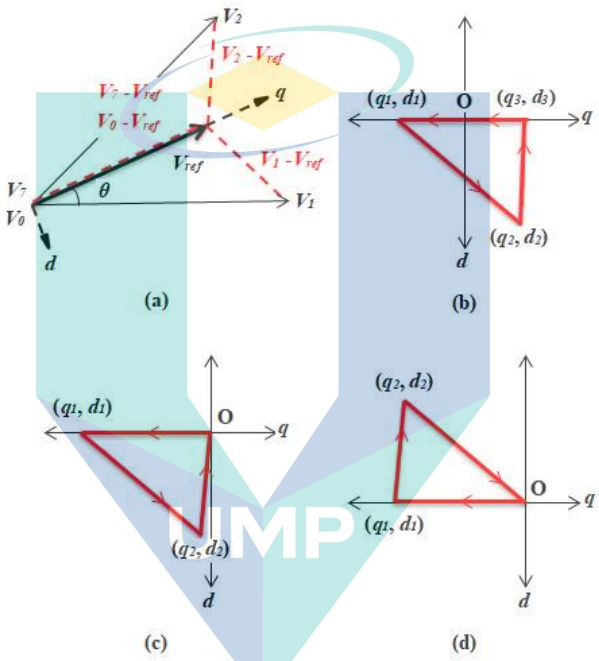

Figure 3.4 (a) Error voltage vectors in sector-1, (b) current ripple trajectory for sequence $V_0V_1V_2V_7$ (c) current ripple trajectory for sequence $V_7V_2V_1$, (d) current ripple trajectory for sequence $V_0V_1V_2$.

Considering CSVPWM and a reference voltage vector in sector-I, the switching sequence $V_0V_1V_2V_7$ or $V_7V_2V_1V_0$ is employed in a sub-cycle. These two sequences have the same effect on the current ripple. Therefore, only one sequence can be considered. The current ripple trajectory corresponding to sequence $V_0V_1V_2V_7$ is shown in Figure 3.4(b). At the beginning of the sub-cycle, assuming t = 0, the tip of the current ripple vector is located at the origin point O. When $t \in (0, T_3/2]$, V_0 is used to synthesize V_{ref}. Hence, the current ripple vector moves in a direction similar to V_0-V_{ref} from point O to point (q_1, d_1). similarly, when $t \in (T_3/2, T_3/2+T_1]$, V_1 is used to synthesize V_{ref}, and thus the current ripple vector moves in the same direction of V_1-V_{ref} from point (q_1, d_1) to point (q_2, d_2). When $t \in (T_3/2+T_1, T_s-T_3/2]$, V_2 is used to synthesize V_{ref}, and the current ripple vector moves in the same direction of V_2-V_{ref} to point (q_3, d_3). Finally, when V_7 is

applied, the current ripple vector returns to the origin point at the end of the sub-cycle. In the same manner, the current ripple trajectories corresponding to sequences $V_0V_1V_2$ and $V_7V_2V_1$ are created as shown in Figure 3.4(c) and (d), respectively. The corner points of the current ripple trajectory (q_y, d_y; y = 1,2,3) corresponding to the CSVPWM ($V_0V_1V_2V_7$) and DPWM ($V_0V_1V_2$ and $V_7V_2V_1$) switching sequences are provided in Table 3.3, while the RMS current ripple over a sub-cycle can be numerically approximated as shown in Equation 3.2.

$$I^2_{(\text{sequence})} = \frac{1}{3T_s}\sum_y T_y \times \left[q_y{}^2 + q_{y+1}{}^2 + d_y{}^2 + d_{y+1}{}^2 + q_y q_{y+1} + d_y d_{y+1} \right] \quad 3.2$$

Table 3.3 Corner points of the current ripple trajectory corresponding to CSVPWM and DPWM switching sequences

Switching sequence	Corner points
$V_0V_1V_2V_7$	$(q_1, d_1) = \{-V_{ref} \times T_3/2, 0\}$
	$(q_2, d_2) = \{\cos(\theta)T_1 - V_{ref}(T_1 + T_3/2), \sin(\theta)T_1\}$
	$(q_3, d_3) = \{V_{ref} \times T_3/2, 0\}$
$V_7V_2V_1$	$(q_1, d_1) = \{-V_{ref} \times T_3, 0\}$
	$(q_2, d_2) = \{\cos(60-\theta)T_2 - V_{ref}(T_2 + T_3), -\sin(60-\theta)T_2\}$
$V_0V_1V_2$	$(q_1, d_1) = \{-V_{ref} \times T_3, 0\}$
	$(q_2, d_2) = \{\cos(\theta)T_1 - V_{ref}(T_1 + T_3), \sin(\theta)T_1\}$

The next step is to determine the RMS current ripple of the CSVPWM over a fundamental cycle, which represents the constraints that should be obeyed in every sub-cycle using the proposed VSF-MPWM. The RMS current ripple over a fundamental cycle for CSVPWM (I_{rms}) can be obtained as shown in Equation 3.3, where $I^2_{(\text{CSVPWM})}$ is the RMS current ripple over a sub-cycle for the CSVPWM. The resulting I_{rms} is graphically illustrated in Figure 3.5 as a function of V_{ref}.

$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} I^2_{(\text{CSVPWM})} \; d\theta} \quad 3.3$$

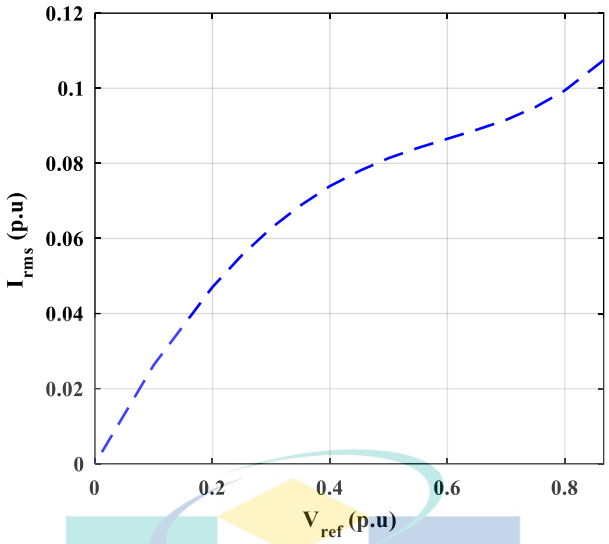

Figure 3.5 RMS current ripple over a fundamental cycle for CSVPWM as a function of V_{ref}.

3.4.2 Modulation Strategy Selection

When DPWM or CSVPWM is used as a modulation strategy, the RMS current ripple over a sub-cycle will follow a known shape, which can be predicted by inserting Table 3.3 data into Equation 3.2. A will-known feature for the DPWM scheme over CSVPWM is that the number of switching transitions during each sub-cycle is reduced from 3 to 2. Hence, to compare both schemes at the same average switching frequency, a sub-cycle duration T_s = (2/3) $T_{s,nom}$ has been considered for DPWM, while $T_s = T_{s,nom}$ for CSVPWM. The value $T_{s,nom}$ is the nominal sub-cycle duration. It is also known that the operating power factor of the motor in EV application is subjected to frequent variation. Hence, the proposed VSF-MPWM should be able to adjust the clamping duration of the DPWM to align the phase current with the peak value in order to maximize switching loss saving. However, varying the location of the clamping duration result in various DPWM schemes, which result in different RMS current ripple. In fact, DPWM1 has slightly higher RMS current ripple compared to all other DPWM strategies. Therefore, in order to ensure that the RMS current ripple of the selected modulation strategy will always stay within I_{rms}, the RMS current ripple over a sub-cycle for the DPWM herein is calculated based on DPWM1, which employs sequence $V_7V_2V_1$ and $V_0V_1V_2$ in the first and second half of sector-I, respectively.

Figure 3.6 presents the variation of $I^2_{(CSVPWM)}$ and $I^2_{(DPWM)}$ with the spatial angle θ at V_{ref} = 0.75 p.u in sector-I. The terms $I^2_{(CSVPWM)}$ and $I^2_{(DPWM)}$ are used to donate the

RMS current ripple over a sub-cycle for the CSVPWM and the DPWM, respectively. It worth mentioning that the values $I^2_{(CSVPWM)}$ and $I^2_{(DPWM)}$ are computed here in only one sector since the subsequent sectors will have the same variation as well. The VSF-MPWM selects the modulation strategy Based on $I^2_{(CSVPWM)}$ and $I^2_{(DPWM)}$. If $I^2_{(CSVPWM)}$ is less than $I^2_{(DPWM)}$, CSVPWM will be selected, otherwise, DPWM is selected.

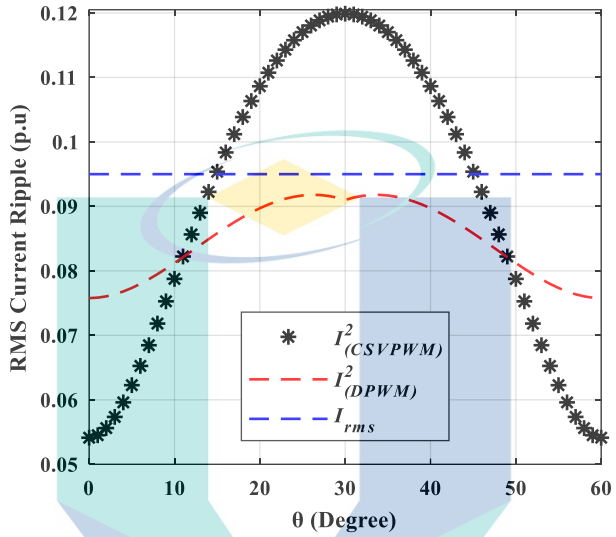

Figure 3.6 Variation of the RMS current ripple over a sub-cycle at V_{ref} = 0.75 p.u in sector-I.

According to the previous step, the DPWM will be applied when $I^2_{(DPWM)}$ is less than $I^2_{(CSVPWM)}$. Under this condition, the clamping duration should be adjusted to align the phase current with the peak value. This is achieved by using the reference stator currents (i_{as}^*, i_{bs}^*, and i_{cs}^*) and Table 3.4. In each sector there are only two phases that can be clamped. Talking sector-I as an example, phase-*a* can be clamped to the positive bus using sequence $V_7V_2V_1$. Simultaneously, phase-*c* can be clamped to the negative bus if sequence $V_0V_1V_2$ is used. Therefore, the selection of the zero voltage vector V_0 or V_7 should be based on i_{as}^* and i_{cs}^*. If $|i_{as}^*|$ is higher than $|i_{cs}^*|$, V_7 is selected and sequence $V_7V_2V_1$ is employed. On the other hand, if $|i_{cs}^*|$ is higher than $|i_{as}^*|$, V_0 is selected and sequence $V_0V_1V_2$ is employed. The subsequent sectors can be treated in a similar fashion as shown in Table 3.4. In this way, the maximum possible switching loss saving can always be achieved at any power factor, where the clamping duration can be even adjusted between two different DPWM strategies.

Table 3.4 Zero voltage vector and DPWM switching sequence selection

Sector number	Condition	Switching sequence
1	$\|i_{as}^*\| > \|i_{cs}^*\|$	$V_7V_2V_1$
	$\|i_{as}^*\| \leq \|i_{cs}^*\|$	$V_0V_1V_2$
2	$\|i_{bs}^*\| > \|i_{cs}^*\|$	$V_7V_2V_3$
	$\|i_{bs}^*\| \leq \|i_{cs}^*\|$	$V_0V_3V_2$
3	$\|i_{bs}^*\| > \|i_{as}^*\|$	$V_7V_4V_3$
	$\|i_{bs}^*\| \leq \|i_{as}^*\|$	$V_0V_3V_4$
4	$\|i_{cs}^*\| > \|i_{as}^*\|$	$V_7V_4V_5$
	$\|i_{cs}^*\| \leq \|i_{as}^*\|$	$V_0V_5V_4$
5	$\|i_{cs}^*\| > \|i_{bs}^*\|$	$V_7V_6V_5$
	$\|i_{cs}^*\| \leq \|i_{bs}^*\|$	$V_0V_5V_6$
6	$\|i_{as}^*\| > \|i_{bs}^*\|$	$V_7V_6V_1$
	$\|i_{as}^*\| \leq \|i_{bs}^*\|$	$V_0V_1V_6$

3.4.3 Switching Frequency Control

The RMS current ripple over a sub-cycle for both DPWM and CSVPWM is not constant and keeps changing with respect to V_{ref} and θ (see Figure 3.6). Therefore, the switching frequency (f_{sw}) is allowed to be changed above and below the nominal switching frequency (f_{nom}), such that the RMS current ripple in every sub-cycle follows I_{rms}, which is shown in the blue dashed line in Figure 3.6 at V_{ref} = 0.75 p.u. Accordingly, the switching frequency coefficient (K_f) that is used to calculate f_{sw} in every sub-cycle can be defined as follows:

If $I^2_{(\text{DPWM})} \leq I^2_{(\text{CSVPWM})}$

$$K_f\left(V_{ref},\theta\right) = \frac{3}{2}\frac{I^2_{(\text{DPWM})}}{I_{rms}} \quad 3.4$$

If $I^2_{(\text{DPWM})} > I^2_{(\text{CSVPWM})}$

$$K_f\left(V_{ref},\theta\right) = \frac{I^2_{(\text{CSVPWM})}}{I_{rms}} \quad 3.5$$

Figure 3.7 shows K_f variation over one fundamental cycle at V_{ref} = 0.75 p.u. It is clearly seen that there is an instantaneous change on the switching frequency coefficient in every 60° of the fundamental cycle due to the 3/2 factor during transmutation from CSVPWM into DPWM. Figure 3.7 also indicates a large decrease on the average

switching frequency due to two different reasons. First, when variable switching frequency is applied on CSVPWM alone, K_f decreases below 1 when $I^2_{(CSVPWM)}$ is less than I_{rms} around both the boundaries, while it goes above 1 when $I^2_{(CSVPWM)}$ is higher than I_{rms} around θ = 30° (see Figure 3.6). Due to this action, the reduction in the average switching frequency is not going to be that much significant. However, because of the hybrid scheme in the proposed VSF-MPWM, the DPWM will be selected around θ = 30°, which describes why K_f is always maintained below 1 in Figure 3.7 when CSVPWM is applied. Second, the required K_f when DPWM is applied is always less than 3/2. This is due to the fact that $I^2_{(DPWM)}$ at this value of V_{ref} is always lower than I_{rms} (see Figure 3.6). Therefore, a significant improvement on the switching loss saving capabilities is expected due to the reduction in the average switching frequency.

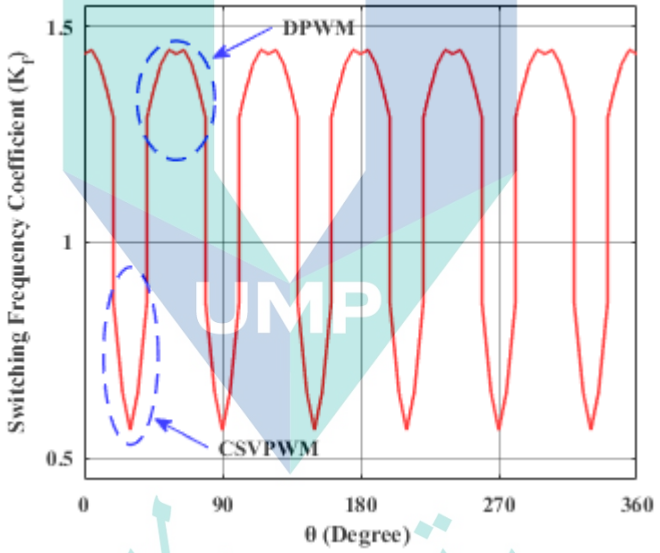

Figure 3.7 K_f variation over one fundamental cycle at V_{ref} = 0.75 p.u.

3.4.4 Flowchart of the Proposed VSF-MPWM

Figure 3.8 shows a flowchart of the proposed VSF-MPWM. The RMS current ripple values $I^2_{(CSVPWM)}$ and $I^2_{(DPWM)}$ are calculated off-line using Equation 3.2 over the entire V_{ref} and θ range and stored in two LUT's, whereas I_{rms} is calculated using Equation 3.3 and stored in another LUT. From the three-phase reference voltages, the instantaneous values of V_{ref} and θ are determined and sent to the LUT's. Then, the output values $I^2_{(CSVPWM)}$ and $I^2_{(DPWM)}$ are sent to a conditional statement block to determine which modulation strategy is going to be adopted and to vary f_{sw}. In the case when the output of the conditional statement is true, f_{sw} is calculated as the multiplication between f_{nom} and

the switching frequency coefficient given in Equation 3.4. This value is then used to determine the dwell times (T_1, T_2, and T_3). Finally, the DPWM is used to generate the gating signals (S_a, S_b, and S_c) of the power devices. The switching sequence of the DPWM strategy is determined based on Table 3.4 and the three-phase reference currents. On the other hand, when the output of the conditional statement is false, the same procedure is adopted. However, the value f_{sw} this time is determined as the multiplication between Equation 3.5 and f_{nom}, while CSVPWM is used to apply the gating signals of the power devices.

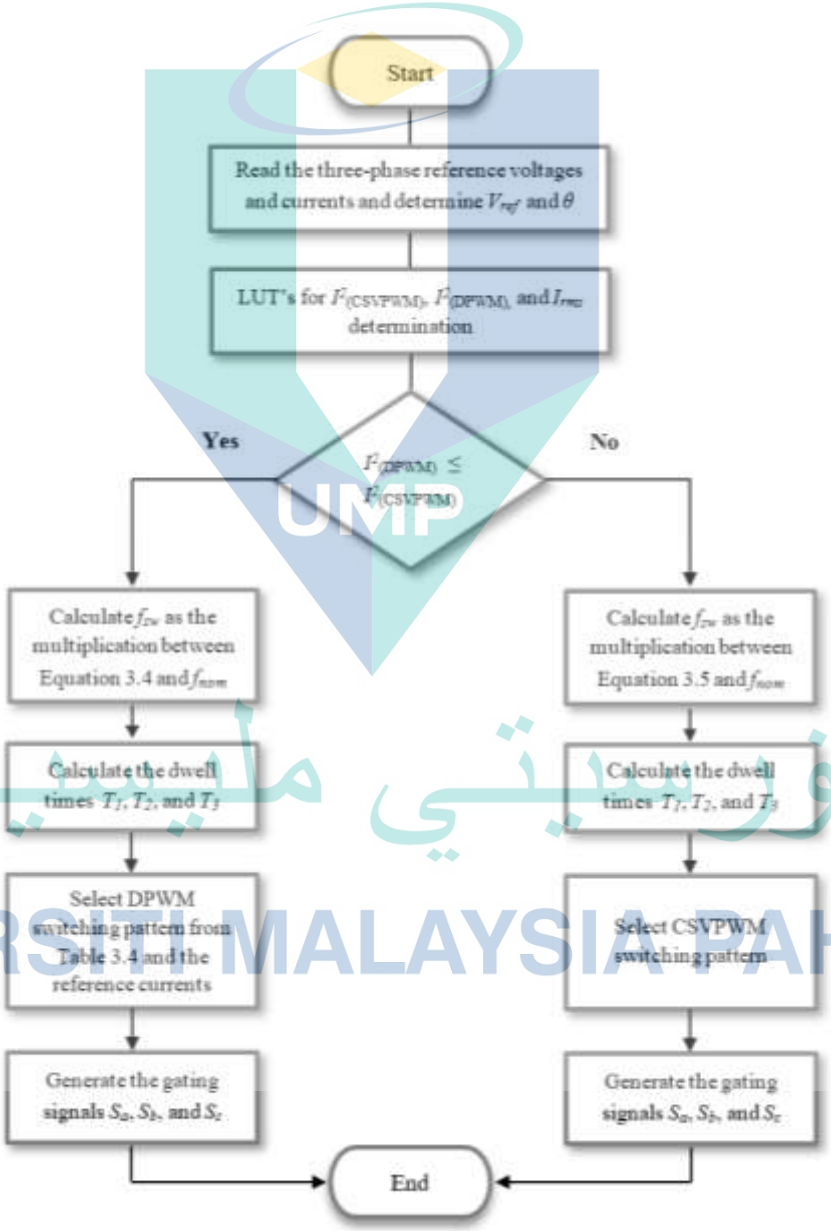

Figure 3.8 Flowchart of the proposed VSF-MPWM.

3.5 Summary

In this chapter, the control structure of the drivetrain under VVC and the flow diagram for lifetime consumption estimation of the inverter power devices is presented. In addition, a new VSF-MPWM for three-phase two-level VSI is developed. Using a predefined mathematical representation of the RMS current ripple in every sub-cycle, the modulation strategy (either DPWM or CSVPWM) with lower RMS current ripple is selected. Consequently, the switching frequency is updated in order to keep the RMS current ripple of the selected PWM strategy within the fundamental cycle RMS current ripple of the CSVPWM. In this way, a considerable switching loss saving can be achieved due to both the clamping duration and the average switching frequency reduction. Meanwhile, an acceptable CTHD can be obtained due to the imposed constraints on the current ripple.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Introduction

In this chapter, the impact of the VVC on the inverter lifetime and the proposed VSF-MPWM on the inverter power losses and CTHD are investigated through MATLAB Simulink. In doing so, the behavior of the dc-bus voltage and motor control loop under VVC are first presented in section 4.2. Then, a comparison study between VVC and CVC regarding their effect on the lifetime of the inverter is presented in section 4.3. The lifetime analysis is conducted using the same procedures in section 3.3. In section 4.4, the effectiveness of the proposed VSF-MPWM is validated through comparison with the conventional and existing modified PWM strategies. The study is conducted over a wide torque-speed range so that the detailed behavior of the proposed strategy is investigated.

4.2 System Behaviour

In this section, the behavior of the dc-bus voltage and the motor control loop under VVC are presented. Figure 4.1 shows the variation of the dc-bus voltage and the reference voltage vector when the mechanical speed of the SPMSM changes from 1000 to 5000 RPM at 100 Nm load torque. When the mechanical speed is less than 1900 RPM, the dc-bus voltage is kept constant at 200 V since the desired voltage to maintain constant V_{ref} at 0.75 p.u is less than the battery voltage. Under these conditions, V_{ref} is less than 0.75 p.u. As the speed increases above 1900 RPM, the variable dc-bus voltage control is enabled and V_{ref} settles around 0.75 p.u. As shown in the figure, the dc-bus voltage in this region keeps on increasing with the mechanical speed until it reaches 400 V, which represents the rated dc-bus voltage.

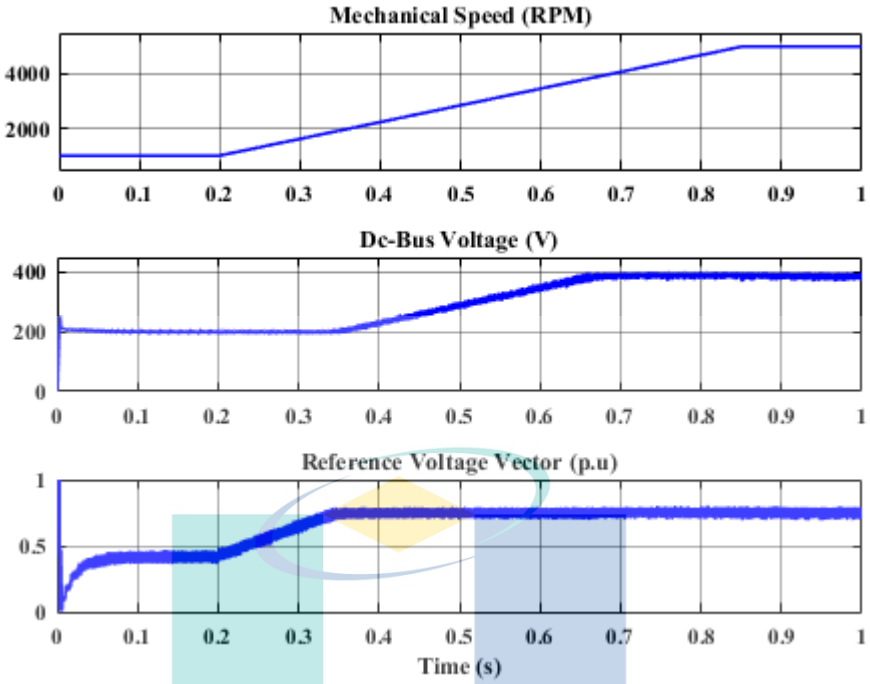

Figure 4.1 Behavior of the dc-bus voltage and reference voltage vector when the mechanical speed of the SPMSM changes from 1000 to 5000 RPM at 100 Nm load torque.

The second test is performed to show the behavior of the *d*-*q* reference stator currents, reference stator voltage, and power factor angle as a function of the motor speed. Figure 4.2 introduces a change on the reference speed from 3000 to 6500 RPM with an input load torque of 100 Nm. Since the motor used in this thesis is a SPMSM, the *d* and *q*-axis inductances are equal as shown in Table 3.1. Hence, according to Equation 2.7 only the *q*-axis current contributes to torque production. In this case, the MTPA can be achieved by making $i_{ds}^{*} = 0$. This clearly shown in Figure 4.2. When the mechanical speed is less than 4000 RPM (base speed at 100 Nm), the reference *d*-axis current is set to zero and the *q*-axis current is set to 161 A, which corresponds to 100 Nm torque and the parameters in Table 3.1. Under these conditions, the power factor angle is around 20.5°. As the mechanical speed increases above 4000 RPM, the stator voltage limit that corresponds to rated dc-bus voltage of 400 V is reached. Hence, in order to increase the speed further, a negative *d*-axis current is required as shown in the figure. As the *d*-axis current increases with the speed, the power factor angle improves to unity and then goes leading until it reaches -12.5° at 6500 RPM.

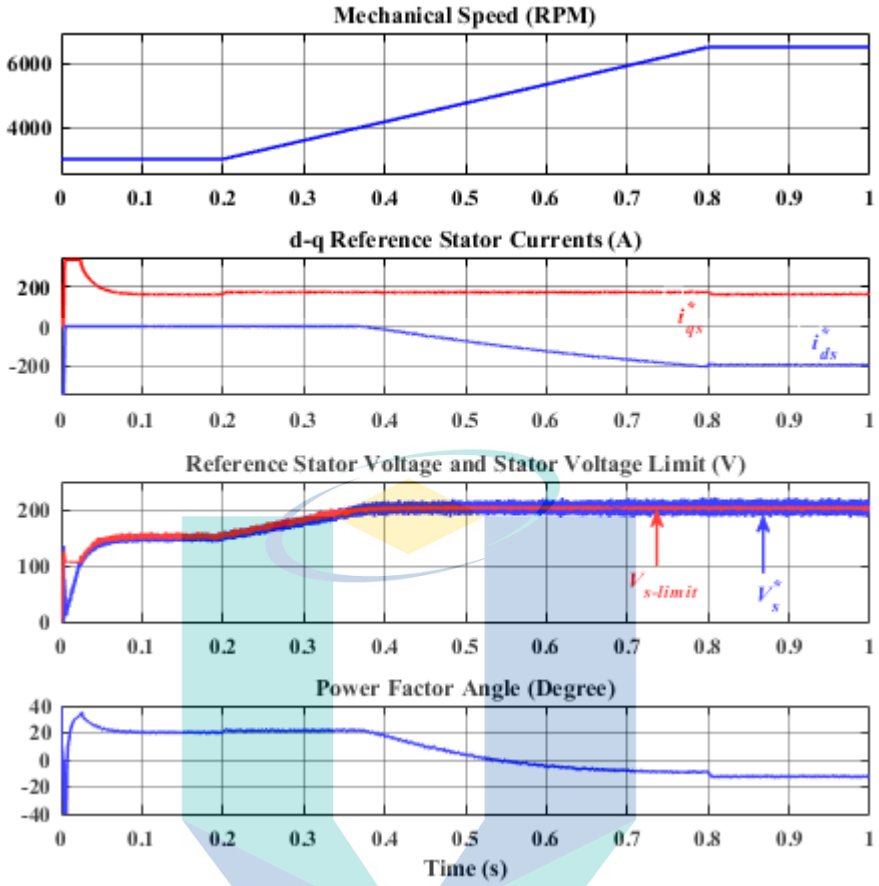

Figure 4.2 Behavior of the *d-q* reference stator currents, reference stator voltage, and power factor angle when the mechanical speed of the SPMSM changes from 3000 to 6500 RPM at 100 Nm load torque.

4.3 Impact of Variable DC-Bus Voltage Control on the Inverter Lifetime

According to the lifetime estimation method presented in Section 3.3, a simulation study is conducted herein to compare the effect of VVC and CVC on the inverter lifetime. This section is divided into two parts. The first part provides analysis in terms of power losses and thermal loading, while the second shows the impact of both strategies on the lifetime consumption.

4.3.1 Power Losses and Thermal Loading Generation of the Power Devices

The torque-speed profiles are first obtained by applying the driving cycle to the vehicle model. The results using the Artemis urban and US06 driving cycles are shown in Figure 4.3(a) and (b), respectively. It can be seen that the torque profile is varying considerably in the 1000 second period of Figure 4.3(a) and at the boundaries of Figure

4.3(b). This variation has a direct impact on the inverter loading, which will in return contribute to large fluctuation in the IGBT's and FWD's junction temperatures.

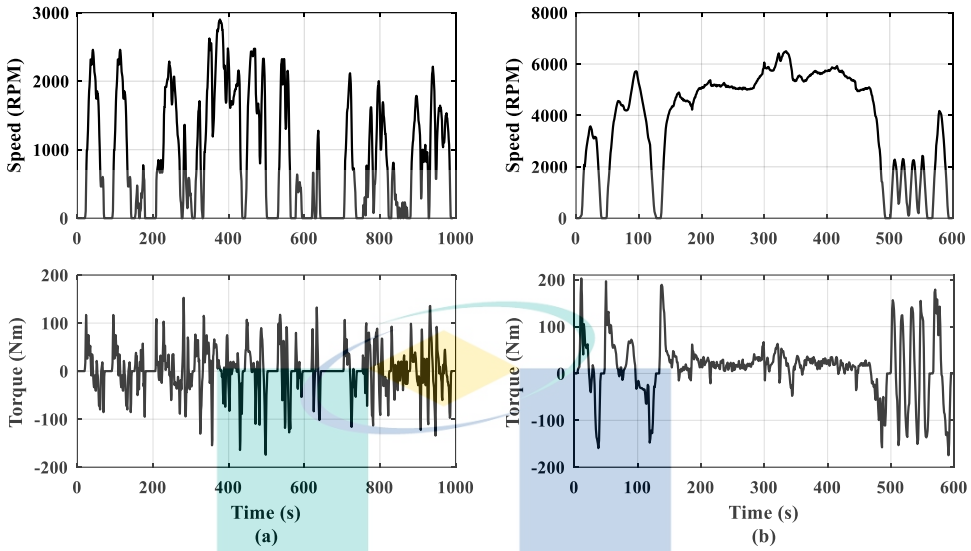

Figure 4.3 Torque and speed profiles under (a) Artemis urban, (b) US06 driving cycle.

Afterwards, using the motor and loss models, the power losses of the IGBTs and FWDs can be obtained. During inverter normal operation, the losses of the six IGBTs and FWDs do not differ significantly because of equal loading. Hence, the losses of one IGBT and one FWD is considered. Using the Artemis urban driving cycle as an input, the inverter IGBT and FWD power losses under CVC and VVC are shown in Figure 4.4(a). It can be noticed that the power losses for both IGBT and FWD under VVC is significantly reduced compared to that under CVC. This is due to the fact that the SPMSM under the Artemis urban driving cycle always operate below the rated speed (below 3200 RPM) as shown in Figure 4.3(a). As a result, the dc-bus voltage using VVC is always less than the rated voltage as seen in Figure 4.5(a), which reduces the power losses in the IGBT and FWD due to the incrementally linear relation between the dc-bus voltage and the switching loss of the power devices.

Similarly, the IGBT and FWD power losses under CVC and VVC using the US06 driving cycle are obtained as shown in Figure 4.4(b). It is clearly seen that the power losses at both the boundaries is reduced considerably under VVC compared to that under CVC. However, compared to the Artemis urban driving cycle the overall reduction over the entire profile is less pronounced. This is because, the SPMSM under the US06 driving cycle operate frequently at high speeds in which the dc-bus voltage is close to its upper

limit as shown in Figure 4.5(b). Therefore, with regard to the power loss reduction, the VVC strategy is more suitable under urban driving conditions.

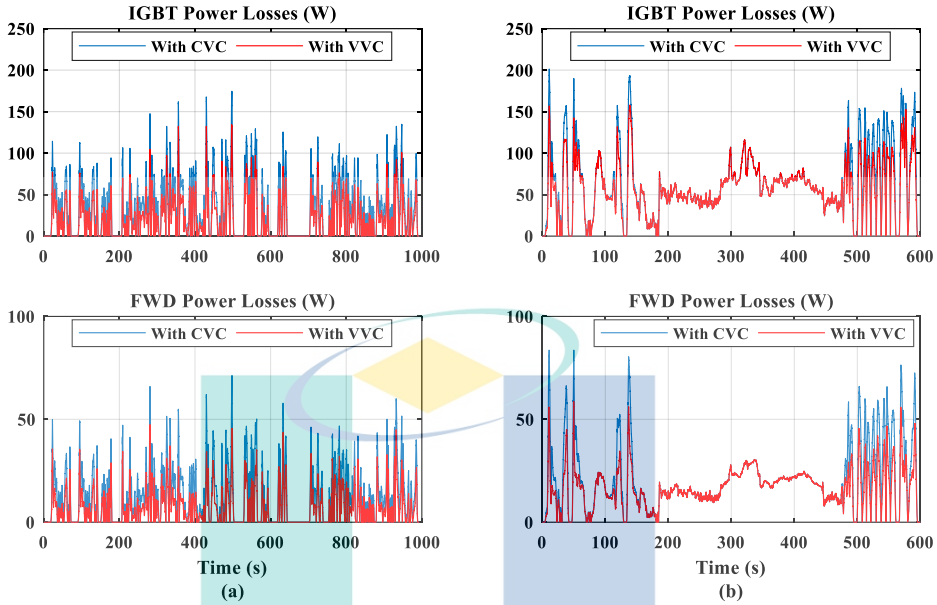

Figure 4.4 IGBT and FWD power losses with CVC and VVC under (a) Artemis urban, (b) US06 driving cycle.

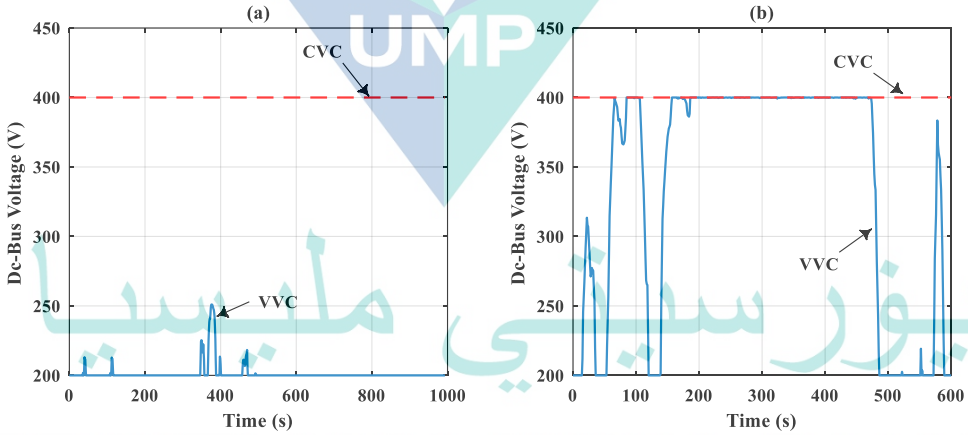

Figure 4.5 Dc-bus voltage with CVC and VVC under (a) Artemis urban, (b) US06 driving cycle.

After calculating the power losses of the power devices, the junction temperature can be easily obtained using the device thermal model. The inverter IGBT and FWD junction temperatures with CVC and VVC under the Artemis urban and US06 driving cycles are shown in Figure 4.6(a) and (b), respectively. With both driving cycles, the junction temperature fluctuation for the IGBT and FWD under VVC is reduced considerably below the rated speed due to the large power loss reduction at this region.

This can effectively improve the lifetime of the inverter since the junction temperature at this region has the largest fluctuation and peak values. To show the impact of this reduction on the inverter lifetime, the junction temperature profiles are applied to the lifetime model as explained in the next subsection.

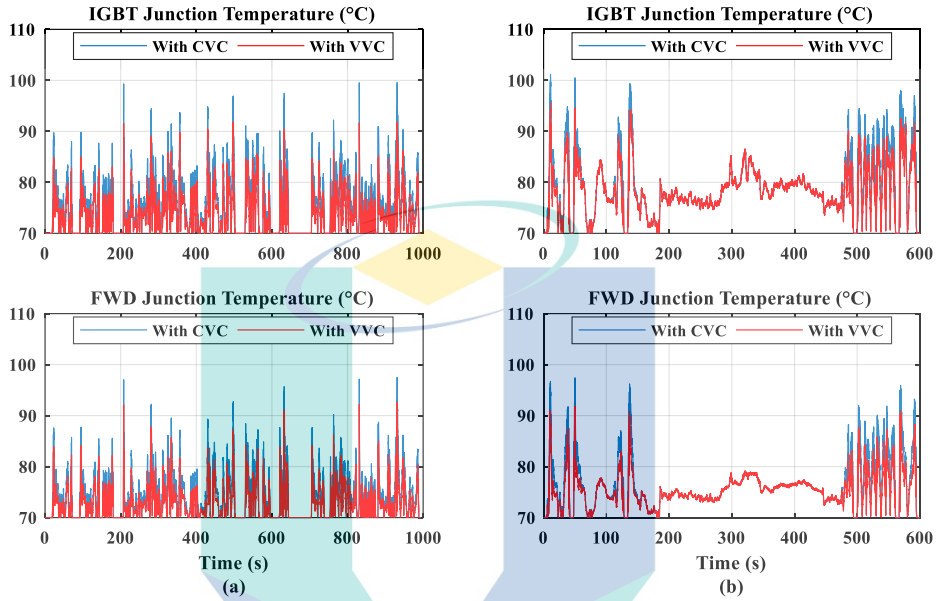

Figure 4.6 IGBT and FWD junction temperature with CVC and VVC under (a) Artemis urban, (b) US06 driving cycle.

4.3.2 Lifetime Consumption Estimation

A rainflow cycle counting algorithm was then applied to the IGBT junction temperature profile in Figure 4.6(a). The resulting number of cycles (n_i) as a function of mean temperature (T_{jm}) and thermal cycle amplitude (ΔT_j) for CVC and VVC are shown in Figure 4.7(a) and (b), respectively. Herein, the thermal cycles with amplitude lower than 3 °C are omitted since they do not have any influence on the component lifetime. It can be observed from Figure 4.7 that the thermal cycle amplitude under VVC are shifted to lower magnitudes. For instance, the total number of cycles with amplitude higher than 15 °C using CVC is 60 cycles while its only 18 cycles using VVC. This indicates the superiority of the VVC as these thermal cycles with high amplitude represents the major cause of failure in the IGBT module. To investigate the impact of this thermal cycling reduction on the lifetime consumption (*LC*), the rainflow cycle counting result is applied to the lifetime model in Equations 2.17 and 2.18. By doing so, the resultant *LC* after one-hour operation under Artemis urban driving cycle is $7.685*10^{-6}$ using CVC and $1.52*10^{-6}$ using VVC. Notably, the *LC* under VVC is reduced significantly compared to CVC,

which results in higher lifetime of the inverter. It should be noticed that the *LC* per one-hour is obtained by running the driving cycle for several times. For instance, the Artemis urban driving cycle duration is 1000 second. Therefore, the *LC* per one-hour is obtained using 3.6 cycles.

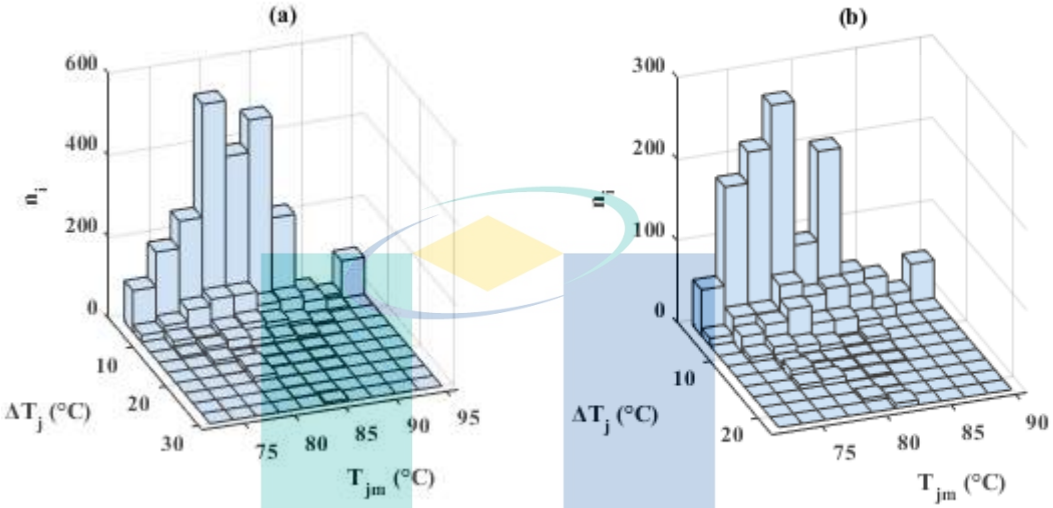

Figure 4.7 Number of cycles (n_i) against mean temperature (T_{jm}) and thermal cycle amplitude (ΔT_j) for the IGBT under Artemis urban driving cycle using (a) CVC, (b) VVC.

The *LC* under the US06 driving cycle can be obtained in the same fashion. Using CVC and VVC, the *LC* after one-hour operation under the Artemis urban and US06 driving cycles for both IGBT and FWD are shown summarized in Table 4.1. The lifetime of the inverter can be determined by the weakest component in the system. According to the result in Table 4.1, the IGBT has always higher *LC* than the FWD. Therefore, considering the IGBT, the lifetime of the inverter due to the VVC has improved by a factor of 5.06 and 3.43 under the Artemis urban and US06 driving cycles, respectively.

Table 4.1 Lifetime consumption per one-hour operation

Driving cycle	Power device	*LC* with CVC (/ hour)	*LC* with VVC (/ hour)
Artemis urban	IGBT	$7.685*10^{-6}$	$1.520*10^{-6}$
	FWD	$4.023*10^{-6}$	$1.156*10^{-6}$
US06	IGBT	$9.626*10^{-6}$	$2.805*10^{-6}$
	FWD	$4.554*10^{-6}$	$1.240*10^{-6}$

4.4 Impact of the Proposed VSF-MPWM on CTHD and Inverter Power Losses

In this section, the impact of the proposed VSF-MPWM strategy on the CTHD and inverter power losses well be presented. In doing so, a comparison between the proposed VSF-MPWM and the CSVPWM in terms of the produced stator CTHD is first presented. Then, a comparison with the CSVPWM, HP-PWM (Hava et al., 1998), and VSFSVPWM (Bhattacharya et al., 2017) in terms of power loss saving well be discussed. The HP-PWM and VSFSVPWM are previously described in subsection 2.7.2.2. These two methods are selected for comparison since they result in large power losses saving and comparable current quality compared to the CSVPWM, which makes them a good choice to investigate the effectiveness of the proposed strategy. The PWM strategies well be tested on the system shown in Figure 3.1 under VVC.

4.4.1 Analysis of Stator CTHD

First, the impact of the proposed VSF-MPWM strategy on the frequency spectra is investigated. Figure 4.8 shows the frequency spectra of the measured phase-*a* stator current at f_{nom} = 10 kHz, T = 100 Nm, and n_m = 3000 RPM (V_{ref} = 0.75 p.u). Figure 4.8(a) corresponds to CSVPWM, whereas Figure 4.8(b) is related to the proposed VSF-MPWM. With CSVPWM, the harmonic components are only concentrated as discrete tonal components around 10 kHz switching frequency and its multiples. In case of the proposed VSF-MPWM, the harmonic components are widely distributed along the frequency spectrum. Nevertheless, the dominant frequency components exist above the 10 kHz and its multiples. For instance, the first harmonic components around 10 kHz with CSVPWM is distributed over a wider range with VSF-MPWM, where the dominant frequency components exist in the range from 13 kHz to 14.5 kHz. This is reasonable since the region at which DPWM is employed with VSF-MPWM at V_{ref} = 0.75 p.u is larger (see Figure 3.6), which means that most of the frequency components are shifted by a factor of 3/2 (see Equation 3.4). It is also seen that the amplitude of the harmonic components in Figure 4.8(a) are mitigated in Figure 4.8(b) because of the wider harmonic distribution. For instance, the larger harmonic component using CSVPWM is around 1.32 A while it is reduced to 0.83 A in the case of VSF-MPWM.

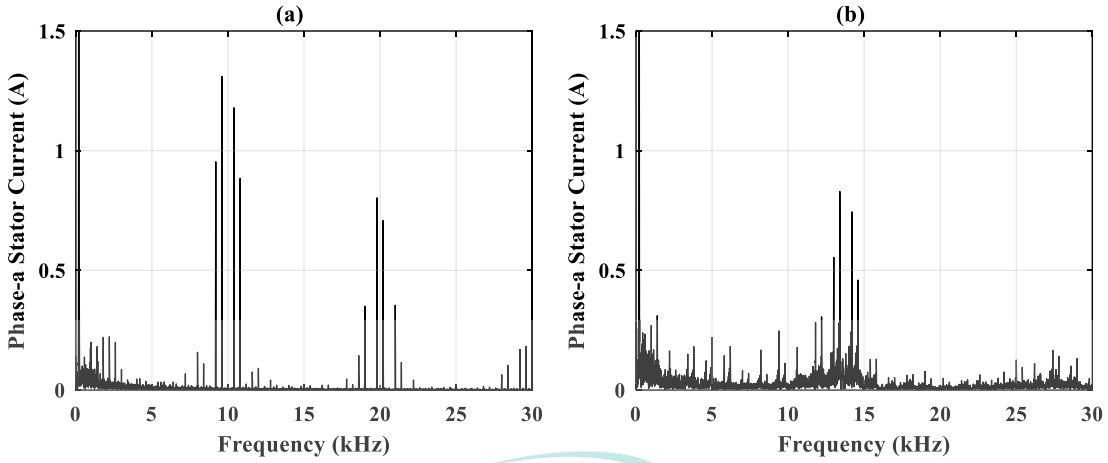

Figure 4.8 Frequency spectra of the measured phase-*a* stator current at f_{nom} = 10 kHz, T = 100 Nm, and n_m = 3000 RPM for (a) CSVPWM, (b) VSF-MPWM.

The corresponding current waveforms for the frequency spectrums in Figure 4.8 are shown in Figure 4.9. The calculated CTHD is 2.5 % for CSVPWM (see Figure 4.9(a)) and 2.55 % in the case of VSF-MPWM (see Figure 4.9(b)). It can be noticed that the CTHD of the proposed VSF-MPWM is approximately similar to that of CSVPWM, where the difference in the CTHD is only 2 %.

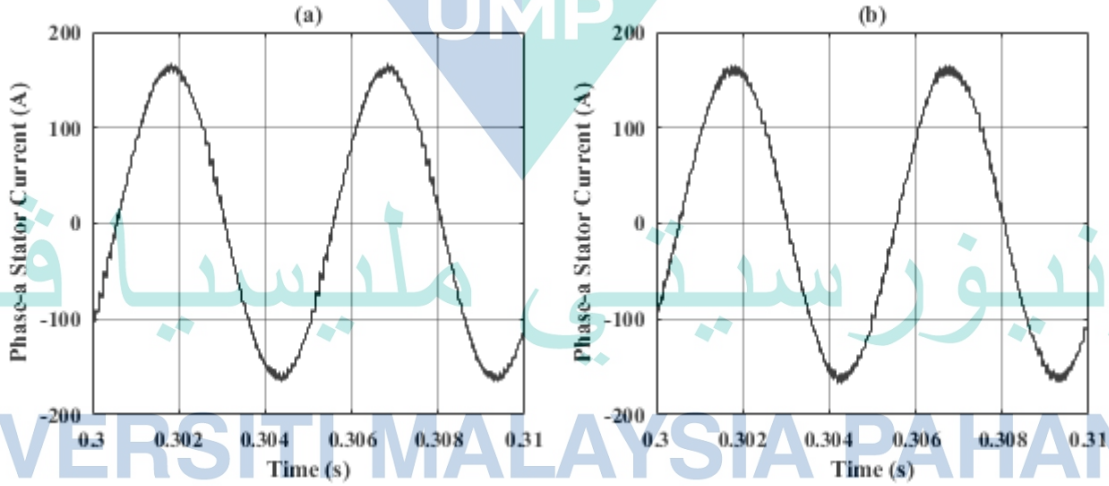

Figure 4.9 Phase-*a* stator current waveform at f_{nom} = 10 kHz, T = 100 Nm, and n_m = 3000 RPM for (a) CSVPWM, (b) VSF-MPWM.

A further investigation of the resulting stator CTHD over a wide range of speed and torque values is shown in Figure 4.10. Figure 4.10(a) shows the CTHD values when the torque changes from 10 to 100 Nm at a constant speed of 3000 RPM, whereas in Figure 4.10(b) the torque is kept constant at 20 Nm and the speed changes from 500 to 7000 RPM. As seen in both figures, the resulting CTHD using the proposed VSF-MPWM

is very close to that using CSVPWM. With the proposed strategy, the increase in the CTHD is always less than 6 %, which is small enough to be neglected. Hence, it can be concluded that, the proposed VSF-MPWM does not have negative effect on the current waveform quality.

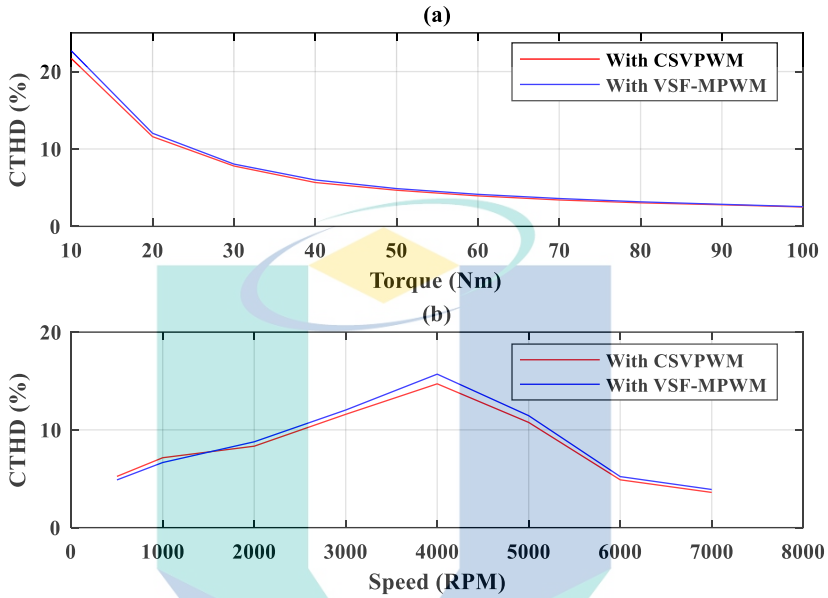

Figure 4.10 CTHD using CSVPWM and VSF-MPWM when (a) T changes from 10 to 100 Nm at n_m = 3000 RPM, (b) n_m changes from 500 to 7000 RPM at T = 20 Nm.

4.4.2 Analysis of Inverter Power Losses

In this part, the impact of the proposed strategy on the inverter switching loss and the total power losses are investigated. The switching loss reduction in the proposed VSF-MPWM is achieved by reducing the number of commutations through the switching frequency control and by using DPWM, which has a clamping duration that can be adjusted to align the phase current peak. To show the impact of the proposed strategy on the clamping duration and the average switching frequency, the following two tests are performed:

The first test is conducted to show the advantage of the proposed VSF-MPWM in terms of the average switching frequency reduction. In doing so, a comparison is made with the CSVPWM. Figure 4.11 compares the switching instances in one of the switching devices (S_1) for the two mentioned PWM strategies during half fundamental cycle, T = 100 Nm, and n_m = 3000 RPM (V_{ref} = 0.75 p.u, and fundamental frequency = 200 Hz). Figure 4.11(a) corresponds to CSVPWM, whereas Figure 4.11(b) is related to the

proposed VSF-MPWM. For more clarity, f_{nom} in this graph is stepped down to 5 kHz. It's seen that the CSVPWM results in 25 switching instances in half fundamental cycle. On the contrary, the proposed VSF-MPWM results in only 20 switching instances during the same period leading to 20 % reduction on the average switching frequency and consequently, a large switching loss reduction.

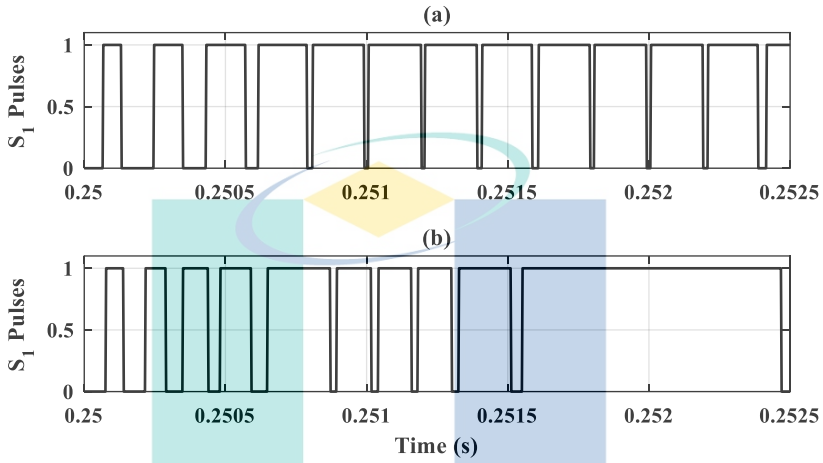

Figure 4.11 Switching instances for the device S_1 during half fundamental cycle, f_{nom} = 5 kHz, T = 100 Nm, and n_m = 3000 RPM for (a) CSVPWM, (b) VSF-MPWM.

Second, the behavior of the VSF-MPWM in terms of the clamping duration adjustment is illustrated in Figure 4.12 in which the equivalent modulating signal (m_{as}^*) and the reference phase-*a* stator current (i_{as}^*) are shown at different speed and torque levels. In this test, the CSVPWM in the proposed strategy is disabled in order to provide a clearer vision. Figure 4.12(a) shows m_{as}^* and i_{as}^* when the values of T and n_m are set to 100 Nm and 3000 RPM, respectively. The power factor angle in this case is around 20.5° lagging as seen in Figure 4.2. Therefore, in order to maximize loss saving, the VSF-MPWM automatically places the clamping duration between DPWM1 and DPWM2 so that the phase leg is not switching at the phase current peak. In Figure 4.12(b), the m_{as}^* and i_{as}^* are shown when the speed increases to 6500 RPM at 100 Nm torque. In this case, the motor goes deep in the flux weakening region and thus the power factor angle improves to 12.5° leading (see Figure 4.2). Accordingly, the VSF-MPWM automatically change the clamping duration between DPWM1 and DPWM0 in order to align the phase current peak. In Figure 4.12(c), the situation is quite different. The values of T and n_m are set to 30 Nm and 6500 RPM, respectively, which results in a power factor angle of around 55° leading. Under this condition, the clamping duration can't be exactly aligned to the

phase current peak. This is because when the power factor angle goes outside 30° lagging to 30° leading range, the phase current with the peak value becomes gradually belongs to the modulating signal that can't be clamped. Talking sector-I as an example, phase-*a* and *c* are the only phases that can be clamped. When the power factor angle is 55° leading, the stator current i_{bs}^* is the peak current for 25° duration of the sector (from 35° to 60°). Since the modulating signal of phase-*b* can't be clamped in sector-I, the VSF-MPWM clamps the modulating signal that belongs to the current with the second peak value and thus the switching loss saving due to the DPWM well be lower than the previous two cases.

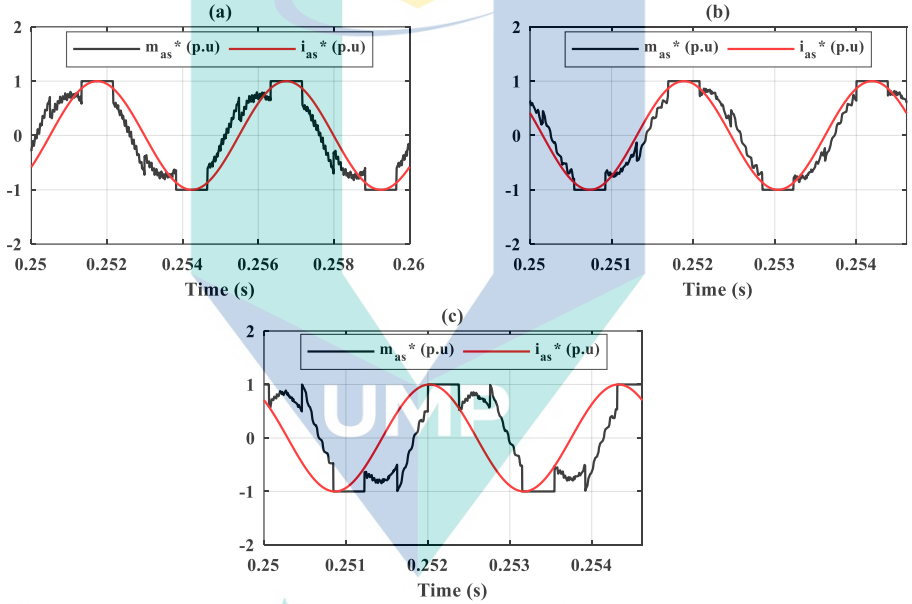

Figure 4.12 Behavior of the VSF-MPWM in terms of the clamping duration adjustment when (a) T = 100 Nm, n_m = 3000 RPM, (b) T = 100 Nm, n_m = 6500 RPM, (c) T = 30 Nm, n_m = 6500 RPM.

The next step is to show the ability of the proposed VSF-MPWM in terms of switching and power loss saving. Figure 4.13 shows the normalized switching loss saving as a function of V_{ref} for the HP-PWM, VSFSVPWM, and the proposed VSF-MPWM with respect to the CSVPWM. The three PWM strategies are tested under 10 Nm torque and over a speed range from 700 to 2300 RPM in order to change the reference voltage vector from 0.25 to 0.75 p.u as shown in the figure. In this speed range, the power factor angle is around 3° and thus the clamping durations of the HP-PWM and VSF-MPWM are aligned to the phase current peak. The HP-PWM selects the modulation strategy (either DPWM or CSVPWM) based on the RMS current ripple over a fundamental cycle. When

V_{ref} > 0.68 p.u, the DPWM results in lower RMS current ripple over a fundamental cycle than the CSVPWM. Hence, a 25 % switching loss saving can be achieved since the DPWM will be applied. As V_{ref} goes down below 0.68 p.u, the RMS current ripple over a fundamental cycle of the CSVPWM becomes lower than that of the DPWM. Therefore, the switching loss saving capabilities of HP-PWM reduces to 0 %. With regard to the VSFSVPWM, the switching frequency is controlled based on the peak current ripple and 0.5 coefficient adjustment factor. When V_{ref} < 0.57 p.u, the VSFSVPWM results in a very small saving on the switching loss. This is due to the fact that the current ripple variation at low values of V_{ref} is very small. However, when V_{ref} increases, the switching loss saving gradually increases until it reaches 14 % at V_{ref} = 0.75 p.u. On the contrary, the proposed VSF-MPWM updates both the switching frequency and the modulation strategy based on the RMS current ripple over a sub-cycle, which allows for higher switching loss saving at high values of V_{ref}. Similar to the VSFSVPWM, the switching loss saving of VSF-MPWM can be divided into two regions. First, when V_{ref} < 0.57 p.u, only 1-4 % switching loss saving can be achieved. This is because the RMS current ripple over a sub-cycle for the CSVPWM is always less than its DPWM counterpart. Second, when V_{ref} > 0.57 p.u, the proposed VSF-MPWM is able to achieve the highest switching loss saving, which can reach up to 35 % at V_{ref} = 0.75 p.u. The high switching loss saving when V_{ref} > 0.57 p.u is due to the gradual increase in the region at which the DPWM is applied. In addition, the high ripple region of the CSVPWM (around θ = 30°) becomes gradually covered by the DPWM strategy as V_{ref} increases, which leads to reduction in the average switching frequency and consequently a further reduction in the switching loss.

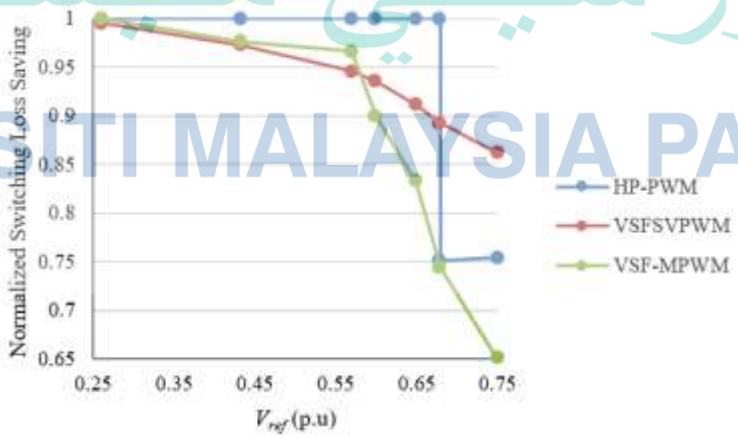

Figure 4.13 Normalized switching loss saving for HP-PWM, VSFSVPWM, and the proposed VSF-MPWM with respect to the CSVPWM as a function of the V_{ref}.

The switching loss saving of the HP-PWM and the proposed VSF-MPWM depends on the clamping duration. At high speed and very low torque, the power factor angle decreases significantly and thus the switching loss saving capabilities of HP-PWM and VSF-MPWM reduces since the clamping duration can no longer align the current peak (see Figure 4.12). Therefore, in order to make a fair comparison with VSFSVPWM, the test should be also conducted under this condition. In this regard, Table 4.2 shows the switching loss saving of the three PWM strategies with respect to the CSVPWM at 10 Nm torque and when the speed changes from 3000 to 9000 RPM. The power factor angle under this condition changes from 3° at 3000 RPM until it reaches -75° at 9000 RPM. It can be seen that the VSFSVPWM has almost steady power loss saving. On the other hand, the switching loss saving of HP-PWM and VSF-MPWM decreases as the speed increases. In conclusion, considering the results in Figure 4.13 and Table 4.2, the proposed VSF-MPWM is able to achieve 10-16 % and 10-21 % higher than the switching loss saving of HP-PWM and VSFSVPWM, respectively, when the speed is greater than 2300 RPM (V_{ref} = 0.75 p.u).

Table 4.2 Switching loss saving of HP-PWM, VSFSVPWM, and VSF-MPWM with respect to the CSVPWM at 10 Nm torque and when the speed changes from 3000 to 9000 RPM

Speed (RPM)	Switching loss saving (%)		
	HP-PWM	VSFSVPWM	VSF-MPWM
3000	23.6	13.88	34.88
5000	13.96	12.87	30
7000	7.22	12.18	23.45
9000	7.08	13.44	23.36

In Figure 4.14, the switching loss and total power losses saving for the proposed VSF-MPWM with respect to CSVPWM is investigated over a speed range from 0 to 7000 RPM and torque range from 10 to 100 Nm. It can be seen from Figure 4.14(a) that the switching loss saving of the proposed strategy vary depending on the speed and torque level. For instance, when the speed is less than 1450 RPM, the reference voltage vector is always less than 0.57 p.u and thus the switching loss saving is limited to 5%. As the speed increases above 1450 RPM, the switching loss saving increases significantly. For speeds above 2300 RPM, the reference voltage vector is fixed at 0.75 p.u over the entire torque region. Consequently, the proposed strategy is able to achieve a very high saving, which ranges from 23.5 to 35.4 %. On the other hand, the total power losses saving is shown over the same speed and torque range in Figure 4.14(b). When the speed is higher

than 2300 RPM, the proposed strategy can reduce the power loss by 14.4 to 23.8 %. This well effectively improve the vehicle performance at highways where the vehicle in most cases operates at high speeds.

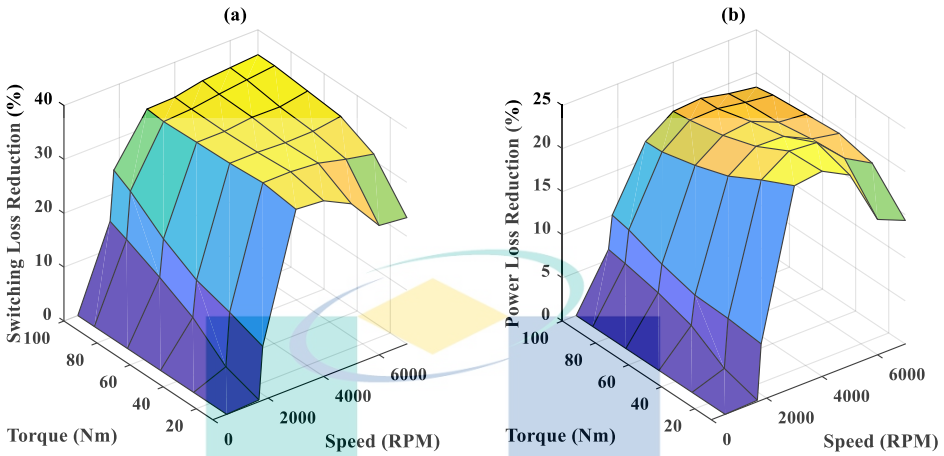

Figure 4.14 (a) Switching loss, (b) total power losses saving for the proposed VSF-MPWM with respect to CSVPWM over a speed range from 0 to 7000 RPM and torque range from 10 to 100 Nm.

4.5 Summary

In this chapter, the impact of VVC on the inverter lifetime is verified through comparison with CVC on an IGBT module subjected to a thermal loading acquired from the Artemis urban and US06 driving cycles. With the aid of VVC, the thermal cycles with large amplitude are reduced significantly. As a result, the inverter lifetime is improved by a factor of 5.06 and 3.43 under the Artemis urban and US06 driving cycles, respectively. This chapter also validate the effectiveness of the proposed VSF-MPWM through comparison with the CSVPWM, HP-PWM, and VSFSVPWM. It is concluded that the proposed VSF-MPWM is able to achieve the highest switching and power loss saving at high speeds when $V_{ref} > 0.57$ p.u. The switching and power losses saving can reach up to 35.4 % and 23.8 %, respectively, compared to the CSVPWM. Meanwhile, the stator CTHD are kept the same as that of CSVPWM.

CHAPTER 5

CONCLUSION

5.1 Conclusion

In this thesis, the advantage of using VVC on the inverter lifetime has been investigated through comparison with the conventional CVC. Using the Artemis urban and US06 driving cycles, the power losses, thermal loading, and lifetime of the inverter power devices under VVC and CVC are obtained. The result shows that the power losses and junction temperature fluctuation under VVC are reduced considerably compared to that under CVC when the speed is less than 3200 RPM. As a result, the inverter lifetime with VVC is improved by a factor of 5.06 and 3.43 under the Artemis urban and US06 driving cycles, respectively, which is proven using MATLAB Simulink. Therefore, it can be concluded that, adding a dc-dc converter to the drivetrain configuration in order to enable the VVC is extremely beneficial for improving the lifetime of the inverter.

This thesis also proposes a new VSF-MPWM strategy to further reduce the inverter power losses. The proposed VSF-MPWM updates the modulation strategy (DPWM or CSVPWM) and the switching frequency in every sub-cycle based on the fundamental cycle RMS current ripple of the CSVPWM. In addition, it adjusts the clamping duration of the DPWM strategy to align the current peak using the reference stator currents. Beyond the possibility of minimizing the power losses due to the DPWM scheme, the theoretical analysis and simulation results shows that when two modulation strategies are considered in the design, a significant reduction in the average switching frequency and consequently a further reduction in the power losses can be achieved at high values of the reference voltage vector (V_{ref} > 0.57 p.u). The VSF-MPWM is tested for torque and speed up to 100 Nm and 9000 RPM, respectively, and compared to the CSVPWM as well as the existing modified HP-PWM and VSFSVPWM under VVC using MATLAB Simulink. The result shows that the proposed strategy is able to achieve from 23.5 to 35.4 % saving of switching loss compared to the CSVPWM, and around 10-16 % and 10-21 % higher than the switching loss saving of HP-PWM and VSFSVPWM,

respectively, when the speed is greater than 2300 RPM. Meanwhile, the proposed strategy can obtain similar stator CTHD compared to the CSVPWM.

5.2 Recommendations for Future Research

The following suggestions are made to be considered for future research;

i. The research on wide bandgap semiconductor (WBG) devices is developing Rapidly. Replacing the current silicon (Si) devices with gallium nitride (GaN) or silicon carbide (SiC) have been widely investigated in the literature as an effective solution to reduce the power losses and to increase the maximum operating temperature of the power electronic converter. An appropriate power loss and thermal models for these devices have been also discussed in the literature. However, in the field of reliability analysis these power devices still have no available lifetime model that can be used to predict the number of cycles to failure in relation to the device temperature. Such model can be designed with the aid of experimental power cycling testing. In this test, different devices are stressed until failure using different stress conditions (e.g., thermal cycle amplitude, mean value, and cycle duration), and the number of cycles to failure is recorded for each stress condition. The test data can then be fitted to a lifetime model (e.g., Coffin-Manson-Arrhenius model) to find the appropriate parameters values (e.g., a_1 and a_2). The design of lifetime model for the new generation WBG devices is an important topic for future research.

ii. In this thesis, the inverter power devices lifetime has been investigated under VVC and CVC strategies. For future work, the lifetime of the dc-dc converter power devices under these two control strategies will be studied. In addition, the overall reliability of the inverter and the dc-dc converter will also be investigated.

iii. The impact of the proposed VSF-MPWM on the inverter power losses as a function of the torque and speed has been investigated in this thesis. However, its impact on the overall power consumption and the inverter lifetime under a certain driving cycles in urban and highway areas is not investigated, which can be considered in future research.

iv. In this thesis, the VSF-MPWM is developed in order to minimize the power losses of the inverter without affecting the motor losses. Alternatively, searching for minimum losses of the inverter and the traction motor together can lead to better results. In fact, the carrier harmonic iron loss can account for more than 40 % of the total motor losses at low torque conditions. Knowing that the harmonic copper and iron losses of the traction motor depends on the switching frequency, an optimization can be made in order to find the switching frequency that minimizes the total losses including harmonic copper, harmonic iron, and inverter switching loss. This idea can be addressed for future research.

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APPENDIX

FF400R07KE4 IGBT module datasheet.

IGBT,Wechselrichter / IGBT,Inverter

Höchstzulässige Werte / Maximum Rated Values

Kollektor-Emitter-Sperrspannung Collector-emitter voltage	T_{vj} = 25°C	V_{CES}	650		V
Kollektor-Dauergleichstrom Continuous DC collector current	T_C = 70°C, $T_{vj\,max}$ = 175°C T_C = 25°C, $T_{vj\,max}$ = 175°C	$I_{C\,nom}$ I_C	400 485		A A
Periodischer Kollektor-Spitzenstrom Repetitive peak collector current	t_P = 1 ms	I_{CRM}	800		A
Gesamt-Verlustleistung Total power dissipation	T_C = 25°C, $T_{vj\,max}$ = 175°C	P_{tot}	1250		W

Charakteristische Werte / Characteristic Values

			min.	typ.	max.	
Kollektor-Emitter-Sättigungsspannung Collector-emitter saturation voltage	I_C = 400 A, V_{GE} = 15 V, T_{vj} = 25°C I_C = 400 A, V_{GE} = 15 V, T_{vj} = 125°C I_C = 400 A, V_{GE} = 15 V, T_{vj} = 150°C	$V_{CE\,sat}$		1,55 1,70 1,75	1,95	V V V
Gate-Schwellenspannung Gate threshold voltage	I_C = 6,40 mA, V_{CE} = V_{GE}, T_{vj} = 25°C	V_{GEth}	5,1	5,8	6,5	V
Einschaltverlustenergie pro Puls Turn-on energy loss per pulse	I_C = 400 A, V_{CE} = 300 V, L_S = 35 nH, T_{vj} = 25°C V_{GE} = ±15 V, di/dt = 6500 A/µs (T_{vj} = 150°C), T_{vj} = 125°C R_{Gon} = 0,82 Ω, T_{vj} = 150°C	E_{on}		2,10 3,55 4,00		mJ mJ mJ
Abschaltverlustenergie pro Puls Turn-off energy loss per pulse	I_C = 400 A, V_{CE} = 300 V, L_S = 35 nH, T_{vj} = 25°C V_{GE} = ±15 V, du/dt = 3300 V/µs (T_{vj} = 150°C), T_{vj} = 125°C R_{Goff} = 0,82 Ω, T_{vj} = 150°C	E_{off}		16,0 20,5 21,5		mJ mJ mJ
Wärmewiderstand, Chip bis Gehäuse Thermal resistance, junction to case	pro IGBT / per IGBT	R_{thJC}			0,12	K/W
Wärmewiderstand, Gehäuse bis Kühlkörper Thermal resistance, case to heatsink	pro IGBT / per IGBT λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)	R_{thCH}		0,03		K/W
Temperatur im Schaltbetrieb Temperature under switching conditions		$T_{vj\,op}$	-40		150	°C

Diode, Wechselrichter / Diode, Inverter

Höchstzulässige Werte / Maximum Rated Values

Periodische Spitzensperrspannung Repetitive peak reverse voltage	T_{vj} = 25°C	V_{RRM}	650		V
Dauergleichstrom Continuous DC forward current		I_F	400		A
Periodischer Spitzenstrom Repetitive peak forward current	t_P = 1 ms	I_{FRM}	800		A

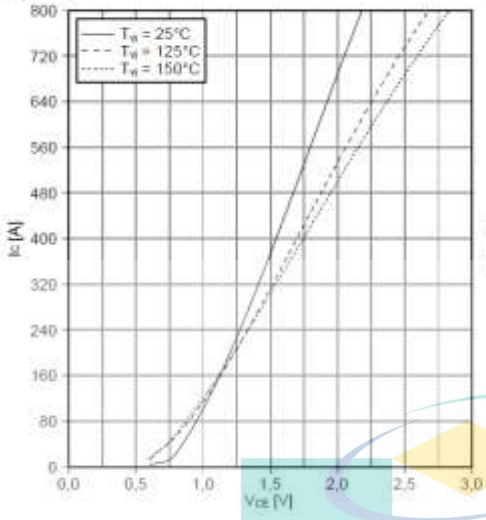
Charakteristische Werte / Characteristic Values

			min.	typ.	max.	
Durchlassspannung Forward voltage	I_F = 400 A, V_{GE} = 0 V, T_{vj} = 25°C I_F = 400 A, V_{GE} = 0 V, T_{vj} = 125°C I_F = 400 A, V_{GE} = 0 V, T_{vj} = 150°C	V_F		1,55 1,50 1,45	1,95	V V V
Abschaltenergie pro Puls Reverse recovery energy	I_F = 400 A, - di_F/dt = 6500 A/µs (T_{vj}=150°C), T_{vj} = 25°C V_R = 300 V, T_{vj} = 125°C V_{GE} = -15 V, T_{vj} = 150°C	E_{rec}		4,35 8,60 9,95		mJ mJ mJ
Wärmewiderstand, Chip bis Gehäuse Thermal resistance, junction to case	pro Diode / per diode	R_{thJC}			0,22	K/W
Wärmewiderstand, Gehäuse bis Kühlkörper Thermal resistance, case to heatsink	pro Diode / per diode λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)	R_{thCH}		0,06		K/W
Temperatur im Schaltbetrieb Temperature under switching conditions		$T_{vj\,op}$	-40		150	°C

output characteristic IGBT,Inverter (typical)

$I_C = f(V_{CE})$

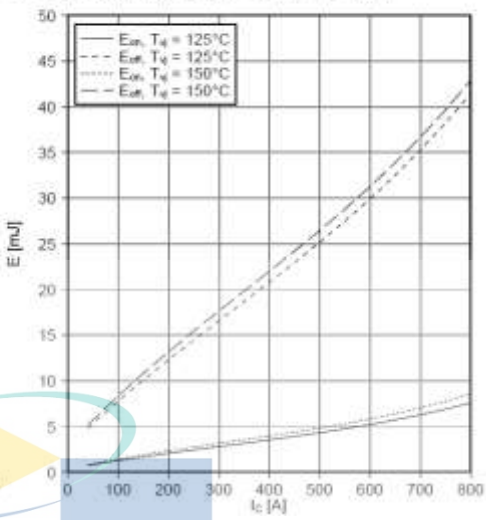
V_{GE} = 15 V



switching losses IGBT,Inverter (typical)

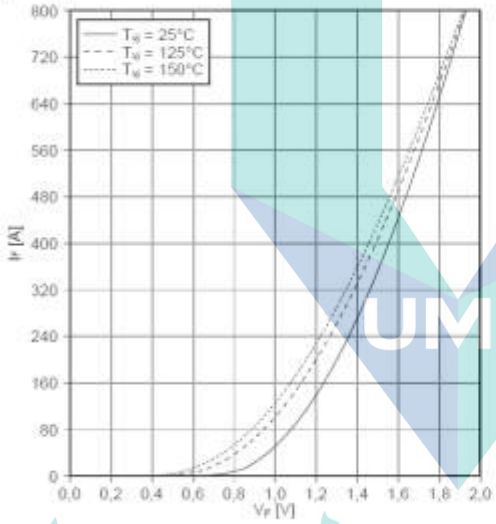
$E_{on} = f(I_C)$, $E_{off} = f(I_C)$

V_{GE} = ±15 V, R_{Gon} = 0.82 Ω, R_{Goff} = 0.82 Ω, V_{CE} = 300 V



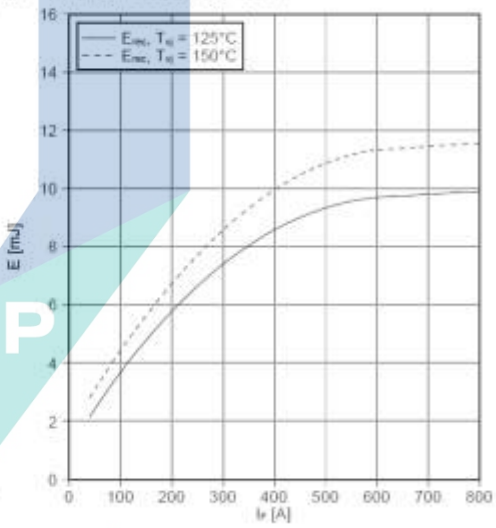
forward characteristic of Diode, Inverter (typical)

$I_F = f(V_F)$



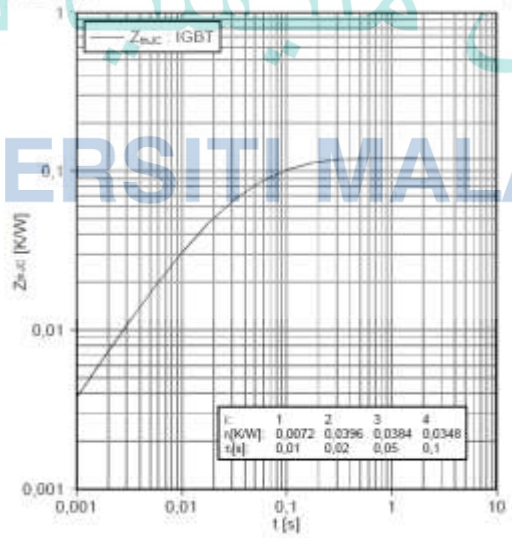
switching losses Diode, Inverter (typical)

$E_{rec} = f(I_F)$, R_{Gon} = 0.82 Ω, V_{CE} = 300 V



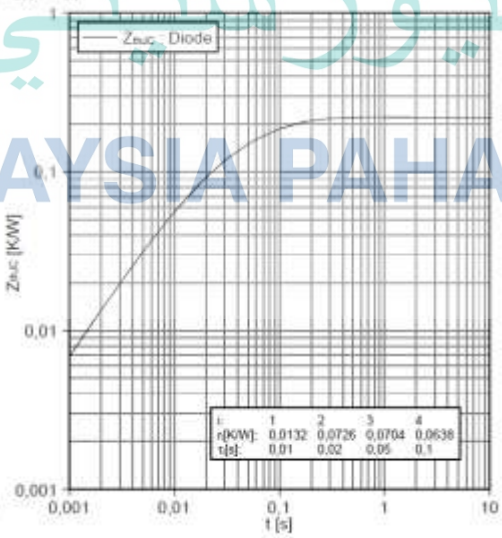
transient thermal impedance IGBT,Inverter

$Z_{thJC} = f(t)$



transient thermal impedance Diode, Inverter

$Z_{thJC} = f(t)$



LIST OF PUBLICATIONS

Journal:

Ibrahim, A., & Sujod, M. Z. (2020). Variable switching frequency hybrid PWM technique for switching loss reduction in a three-phase two-level voltage source inverter. *Measurement, vol. 151*, p. 107192. https://doi.org/10.1016/j.measurement.2019.107192.

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Ibrahim, A., & Sujod, M. Z. (2020). The Impact of Variable DC-Bus Voltage Control on the Inverter Lifetime in Electric Vehicle Applications. In *2020 IEEE Symposium on Industrial Electronics & Applications (ISIEA)* (pp. 1–6). IEEE. DOI: 10.1109/ISIEA49364.2020.9188096.