ELECTRICAL AND TEMPERATURE CHARACTERISATION OF SILICON AND GERMANIUM NANOWIRE TRANSISTORS BASED ON CHANNEL DIMENSIONS

HANI TAHA ABD ASSAMAD AL ARIQI

MASTER OF SCIENCE

UNIVERSITI MALAYSIA PAHANG

SUPERVISOR'S DECLARATION

We at this moment declare that we have checked this thesis and in my opinion, this thesis is adequate in terms of scope and quality for the award of the degree of Master of Science.

_____

(Supervisor's Signature)

Full Name : Ts. Dr. WAHEB ABDUL JABBAR SHAIF ABDULLAH

Position : SENIOR LECTURER

Date : 07 SEPTEMBER 2020

_____

(Co-supervisors Signature)

Full Name : ASSOC. PROF. TS. DR. HADI BIN MANAP

Position : ASSOCIATE PROFESSOR

Date : 07 SEPTEMBER 2020

STUDENT'S DECLARATION

I hereby declare that the work in this thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at Universiti Malaysia Pahang or any other institutions.

_____

(Student's Signature)

Full Name : HANI TAHA ABD ASSAMAD AL ARIQI

ID Number : MET 17012

Date : 07 SEPTEMBER 2020

ELECTRICAL AND TEMPERATURE CHARACTERISATION OF SILICON AND GERMANIUM NANOWIRE TRANSISTORS BASED ON CHANNEL DIMENSIONS

HANI TAHA ABD ASSAMAD AL ARIQI

Thesis submitted in fulfilment of the requirements
for the award of the degree of
Master of Science

Faculty of Electrical & Electronic Engineering Technology

UNIVERSITI MALAYSIA PAHANG

SEPTEMBER 2020

ACKNOWLEDGEMENT

All praise be to Allah Almighty, Lord of the worlds, the most gracious and merciful, and peace be upon His messenger.

I thank my supervisor, Ts. Dr. Waheb Abdul Jabbar Al-Areeqi, for his unlimited guidance, unparalleled patience, kindness, thoughtful comments, attention to detail and encouragement. I thank him for his invaluable advice and assistance and for leaving his mark on this thesis. I also thank my co-supervisor, Assoc. Prof. Ts. Dr. Hadi Bin Manap, and Dr. Yasir Hashim, for their guidance, support and suggestions. I also extend my thanks to Universiti Malaysia Pahang and the staff of the Faculty of Electrical & Electronics Engineering Technology for their help in this research.

I wish to express my deep gratitude to my parents, my wife and my lovely children, for their support and continuous encouragement throughout my years of study and during my writing of this thesis. The completion of this thesis would not have been possible without them.

.

.

ABSTRAK

Antara pelbagai teknik, pengesanan berdasarkan transistor kesan medan (FET) telah menarik perhatian pihak industri dan akademik. Disebabkan ciri-ciri unik seperti saiz yang kecil, ringan, murah, fleksibiliti, pantas respon, stabil, dan keupayaan untuk menurun skala, nanowire transistor (NWTs) boleh berfungsi sebagai pengesan nano yang ideal. Mereka adalah peneraju untuk peranti nano berasaskan FET. Oleh kerana dimensi (panjang, diameter dan ketebalan oksida) saluran NWT berkurangan, ciri elektrik dan suhu NWTs terjejas dan merendahkan prestasi. Walaupun penggunaan NWTs sebagai pengesan biologi atau kimia diterokai secara meluas, kurang penekanan transistor tersebut sebagai pengesan suhu. Maka, penyelidikan ini bertujuan untuk menyiasat kesan dimensi keratan rentas Silikon Nanowire Transistor (SiNWT) dan Germanium Nanowire Transistor (GeNWT) terhadap ciri elektrik dan suhu mereka. Seterusnya menilai dan membandingkan prestasi nanowires dan kebolehgunaannya sebagai pengesan suhu nano untuk pemantauan suhu berterusan dengan keupayaan pengesanan yang unggul, tinggi fleksibiliti dan rendah kos. Kajian perbandingan berasaskan simulasi dijalankan bergantung pada Enam parameter, iaitu panjang get (L_g), diameter saluran (D_{ch}), ketebalan oksida (T_{ox}), suhu persekitaran (T), Voltan pincang get (V_g), dan voltan pincang salir (V_{DD}). Kesan mengubah parameter yang dinyatakan pada prestasi SiNWT dan GeNWT dinilai berdasarkan ciri elektrik dan suhu. Alat simulasi MuGFET untuk struktur FET pelbagai get skala nano digunakan untuk menjalankan simulasi dengan syarat tertentu. Pelbagai parameter disimulasikan dalam Tiga senario simulasi utama termasuk 21 voltan operasi dan peningkatan suhu persekitaran dari 225 ke 450 K dengan langkauan 25 K. Senario pertama menguji variasi panjang get (L_g = 25, 45, 65, 85 dan 105 nm), manakala senario kedua memberi tumpuan kepada variasi diameter saluran (D_{ch} = 10, 20, 40 dan 80 nm) dan yang terakhir membezakan ketebalan saluran oksida (T_{ox} = 1, 2, 3 , 4 dan 5 nm). Empat metrik penilaian digunakan termasuk Subthreshold Swing (SS), Voltan ambang (V_{th}), Induksi Salir Penghalang Rendah (DIBL) dan kadar variasi arus saliran, ΔId sebagai penunjuk kepekaan suhu. Kebiasaannya, prestasi terbaik NWTs boleh dicapai pada voltan operasi optimum dengan nilai SS lebih dekat keadaan ideal, tahap DIBL rendah dan nilai voltan ambang tinggi. Hasil simulasi SiNWT dan GeNWT menunjukkan kesan dimensi saluran berbeza (L_g, D_{ch}, T_{ox}) pada suhu dan ciri-ciri elektrik. Kepekaan suhu (ΔI_d) telah meningkat dengan meningkatkan pelbagai dimensi saluran dan suhu operasi untuk kedua-dua SiNWT dan GeNWT dan voltan operasi optimum telah dikenalpasti bagi setiap NWT. SiNWT menunjukkan lebih kestabilan dalam variasi suhu persekitaran berbanding GeNWT yang stabil dalam semua senario. SiNWT juga mengatasi GeNWT dari segi SS dan V_{th}, maka ia dapat meningkatkan kelajuan pensuisan dan mengurangkan kebocoran arus kerana SS sangat dekat dengan keadaan ideal dan voltan ambang adalah tinggi berbanding dengan GeNWT. SiNWT mencapai tahap DIBL yang lebih tinggi dalam kes tertentu, tetapi ia boleh diterima untuk kebanyakan dimensi saluran. Kesan perubahan panjang get adalah sangat jelas pada operasi NWTs dan impak terendah dapat dilihat dari pelbagai ketebalan oksida. SiNWT mempunyai lebih kebolehgunaan sebagai pengesan suhu nano kerana kestabilan ciri elektrik dan suhunya.

ABSTRACT

Amongst various sensing and monitoring technologies, sensors based on field effect transistors (FETs) have attracted considerable attention from both the industry and academia. Owing to their unique characteristics such as their small size, lightweight, low cost, flexibility, fast response, stability and ability for further downscaling, nanowire transistors (NWTs) can serve as ideal nanosensors and successors to FET-based nanoscale devices. However, as the dimensions (length, diameter and oxide thickness) of NWT channels are shrinking down, the electrical and temperature characteristics of NWTs are affected, thereby degrading the transistor performance. Although the applications of NWTs as biological and/or chemical sensors have been extensively explored in the literature, the use of these transistors as temperature sensors has been largely ignored. Consequently, this research investigates the impact of the cross-sectional dimensions of silicon nanowire transistors (SiNWTs) and germanium nanowire transistors (GeNWTs) on their electrical and temperature characteristics. Accordingly, evaluate and compare the performance of the considered nanowires and their potential applicability as temperature nanosensors for continuous temperature monitoring with good detection capability, high flexibility and low cost. A comprehensive simulation-based comparative study is performed by using six variable parameters, namely, gate length (L_g), channel diameter (D_{ch}), oxide thickness (T_{ox}), ambient temperature (T), gate bias voltage (V_g) and drain bias voltage (V_{DD}). The impact of changes in these parameters on the electrical and temperature characteristics of SiNWTs and GeNWTs is then evaluated. The well-known MuGFET simulation tool for nanoscale multi-gate FET structure is used for the experimental simulations. A wide range of variable parameters are simulated in three simulation-based case studies, which cover 21 operating voltages and an ambient temperature increasing from 225 K to 450 K by a step of 25 K. The first case study considers the variation in gate length (L_g = 25, 45, 65, 85 and 105 nm), the second focuses on the variation in channel diameter (D_{ch} = 10, 20, 40 and 80 nm) and the third focuses on the variation in channel oxide thickness (T_{ox} = 1, 2, 3, 4 and 5 nm). Four performance evaluation metrics are considered, namely, subthreshold swing (SS), threshold voltage (V_{th}), drain-induced barrier lowering (DIBL) and drain current variation rate, ΔI_d, which serves as an indicator of temperature sensitivity. The optimal stability- and sensitivity-based performance of NWTs can be achieved at certain optimal operating voltages with the SS values closer to the ideal state, a lower DIBL level and higher voltage threshold values. The simulation results for SiNWTs and GeNWTs highlight the effects of varying the channel dimensions (L_g, D_{ch}, and T_{ox}) on their temperature and electrical characteristics. Specifically, the temperature sensitivity (ΔI_d) of SiNWTs and GeNWTs significantly increased along with various channel dimensions and operating temperatures, and the optimal operating voltages are identified for each NWT. According to their temperature characteristics, SiNWTs show higher stability to ambient temperature variations compared with GeNWTs, which in turn demonstrate a higher sensitivity in all cases compared with SiNWT. In addition, SiNWTs outperform GeNWTs in terms of SS and V_{th} and demonstrate a faster switching speed and lower leakage current given that the values of SS are very close to the ideal state and high threshold voltages. SiNWTs also achieve a high DIBL level in certain cases, which is considered acceptable for most channel dimensions. The impact of changing the gate length on the behaviour of NWTs is very obvious, and varying the oxide thickness demonstrates the lowest impact. SiNWTs have high potential to be applied as temperature nanosensors due to their electrical and temperature stability.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS

C	Capacitors
I	Current
I-V	Current-voltage
V_{DD}	Drain DC voltage source
I_{ds}	Drain to source current
I_d	Drain current
V_{DS}	Drain to source voltage
V_g	Gate voltage
V_{GS}	Gate to source voltage
I_{OFF}	OFF current
I_{ON}	ON current
R_{out}	Transistor resistance
T	Temperature
V	Voltage

LIST OF ABBREVIATIONS

AFM	Atomic Force Microscope
AM	Accumulation Mode
ABMS	Agent Based Modelling and Simulation
B2H6	Diborane
BE	Ballistic Efficiency
Cal.Tech	California Institute of Technology
CVD	Chemical Vapour Deposition
CMOS	Complementary Metal Oxide Semiconductor
ρC	Contact Resistivity
di	Diode
DG-FET	Double-Gate Field-Effect Transistor
D_{ch}	Channel Diameter
DIBL	Drain Induced Barrier Lowering
EELS	Electron Energy Loss Spectroscopy
FinFET	Fin-Shaped Field Effect Transistor
GAA	Gate All Around
L_g	Gate Lengths
NMH	High-State Noise Margins
IC	Integrated Circuits
ITRS	International Technology Roadmap for Semiconductors
IGZO	Indium Gallium Zinc Oxide
IoT	Internet of Things
NML	Low-State Noise Margins
MOS diode	Metal Oxide Semiconductor Diode
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MuGFET	Multi Gate Field Effect Transistor
Ni-nGe	Nickle – Germanium N-Type
Nm	Nanometer
NO2	Nitrogen Dioxide
NW	Nanowire

NWT	Nanowire Transistor
NIST	National Institute of Standards and Technology
NNI	National Nanotechnology Initiative
NMOS	N-Channel Metal Oxide Semiconductor
NRs	Nanorods
PEDOT: PSS	Poly(3,4-Ethylenedioxythiophene) Polystyrene Sulfonate
PNWTs	Pentagonal
PH3	Phosphine
PN junction	P- Type and N- Type Junction
SEM	Scanning Electron Microscope
STM	Scanning Tunnelling Microscope
SCE	Short Channel Effect
SiNWFET	Silicon Nanowire Field Effect Transistor
SG	Single-Gate
R_{sh}	Sheet Resistance
SOI	Silicon On Insulator
SWCNT	Single-Walled Carbon Nanotube
SS	Sub Threshold Slope
T_{ox}	Oxide Thickness
TCAD	Technology Computer Aided Design
V_{th}	Threshold Voltage
TEM	Transmission Electron Microscope
TrNWTs	Trapezoidal
TLM	Transmission Length Model
VNWFET	Vertical Nanowire Field Effect Transistor
VLS	Vapour Liquid Solid
VLSI	Very Large Scale Integration
ZnO	Zinc Oxide

REFERENCES

Abar, S., Theodoropoulos, G. K., Lemarinier, P., & O'Hare, G. M. (2017). Agent Based Modelling and Simulation tools: A review of the state-of-art software. *Computer Science Review, 24*, 13-33.

Ahmed, N., Bhargav, P. B., Rayerfrancis, A., Chandra, B., & Ramasamy, P. (2018). Study the effect of plasma power density and gold catalyst thickness on Silicon Nanowires growth by Plasma Enhanced Chemical Vapour Deposition. *Materials Letters, 219*, 127-130.

Ahn, J.-H., Choi, S.-J., Im, M., Kim, S., Kim, C.-H., Kim, J.-Y., . . . Choi, Y.-K. (2017). Charge and dielectric effects of biomolecules on electrical characteristics of nanowire FET biosensors. *Applied Physics Letters, 111*(11), 113701.

Archimedes. (2019). Retrieved from http://www.gnu.org/software/archimedes/

Assaderaghi, F., Chen, J., Solomon, R., Chian, T.-Y., Ko, P. K., & Hu, C. (1991). Transient behavior of subthreshold characteristics of fully depleted SOI MOSFETs. *IEEE Electron Device Letters, 12*(10), 518-520.

Auth, C., Allen, C., Blattner, A., Bergstrom, D., Brazier, M., Bost, M., . . . Glassman, T. (2012). *A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors.* Paper presented at the 2012 symposium on VLSI technology (VLSIT).

Bhat, T. A., Mustafa, M., & Beigh, M. (2015). Study of Short Channel Effects in n-FinFET Structure for Si, GaAs, GaSb and GaN Channel Materials. *J. Nano-Electron. Phys.*

Bradley, D. (2018). *Mechatronics: electronics in products and processes*: Routledge.

Brouzet, V., Salem, B., Periwal, P., Alcotte, R., Chouchane, F., Bassani, F., . . . Ghibaudo, G. (2016). Fabrication and electrical characterization of homo-and hetero-structure Si/SiGe nanowire Tunnel Field Effect Transistor grown by vapor–liquid–solid mechanism. *Solid-State Electronics, 118*, 26-29.

Buyukbas-Ulusan, A., Altındal-Yerişkin, S., & Tataroğlu, A. (2018). Forward and reverse bias current–voltage (I–V) characteristics in the metal–ferroelectric–semiconductor (Au/SrTiO 3/n-Si) structures at room temperature. *Journal of Materials Science: Materials in Electronics, 29*(19), 16740-16746.

Chandra, N. (2014). *Nanowire Specialty Diodes for Integrated Applications*: Arizona State University.

Chaudhry, A., & Kumar, M. J. (2004). Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: a review. *IEEE Transactions on Device and Materials Reliability, 4*(1), 99-109.

Chung, W., Wu, H., Wu, W., Si, M., & Peide, D. Y. (2019). Experimental Extraction of Ballisticity in Germanium Nanowire nMOSFETs. *IEEE Transactions on Electron Devices, 66*(8), 3541-3548.

Ciuti, G., Ricotti, L., Menciassi, A., & Dario, P. (2015). MEMS sensor technologies for human centred applications in healthcare, physical activities, safety and environmental sensing: a review on research activities in Italy. *Sensors, 15*(3), 6441-6468.

Clarke, P. (2005). Intel enters billion-transistor processor era. EE Times, 14 October.

Colinge, J.-P., Lee, C.-W., Afzalian, A., Akhavan, N. D., Yan, R., Ferain, I., . . . White, M. (2010). Nanowire transistors without junctions. *Nature nanotechnology, 5*(3), 225.

Constantinou, M. (2017). *Nanowire field-effect transistors for gas sensor applications.* University of Surrey (United Kingdom),

Cui, Y., Duan, X., Hu, J., & Lieber, C. M. (2000). Doping and electrical transport in silicon nanowires. *The Journal of Physical Chemistry B, 104*(22), 5213-5216.

Cui, Y., & Lieber, C. M. (2001). Functional nanoscale electronic devices assembled using silicon nanowire building blocks. *Science, 291*(5505), 851-853.

Davies, J. C. (2017). *Oversight of Next Generation Nano te chno logy*: Woodrow Wilson International Center for Scholars.

Deen, M. J., & Yan, Z. (1992). DIBL in short-channel NMOS devices at 77 K. *IEEE Transactions on Electron Devices, 39*(4), 908-915.

Delaurenti, M. (1999). Design and optimization techniques for high speed VLSI circuits. *Politecnico di Torino*.

Dey, J. K., Das, S., & Mawlong, L. G. (2018). Nanotechnology and its Importance in Micronutrient Fertilization. *Int. J. Curr. Microbiol. App. Sci, 7 Number 05 (2018)*, 20.

Doghish, M. Y., & Ho, F. D. (1993). A comprehensive analytical model for metal-insulator-semiconductor (MIS) devices: A solar cell application. *IEEE Transactions on Electron Devices, 40*(8), 1446-1454.

Dorf, R. C. (2016). *Sensors, Nanoscience, Biomedical Engineering, and Instruments* (C. press. Ed.): CRC press.

Doucey, M.-A., & Carrara, S. (2019). Nanowire sensors in cancer. *Trends in biotechnology, 37*(1), 86-99.

Duoc, V. T., Le, D. T. T., Hoa, N. D., Van Duy, N., Hung, C. M., Nguyen, H., & Van Hieu, N. (2019). New Design of ZnO Nanorod-and Nanowire-Based NO2 Room-Temperature Sensors Prepared by Hydrothermal Method. *Journal of Nanomaterials, 2019*.

Emadi, A. (2017). *Handbook of automotive power electronics and motor drives*: CRC press.

Fan, J.-C., & Lee, S.-F. (2016). *Effect of oxide layer in metal-oxide-semiconductor systems.* Paper presented at the MATEC Web of Conferences.

Fieldhouse, N. (2009). How To Make Nano Practical Nanotechnology. Retrieved from https://sites.google.com/a/psu.edu/nano-materials/current-products

Gadomski, A. M., Balducelli, C., Bologna, S., & DiCostanzo, G. (1998). *Integrated parellel bottom-up and top-down approach to the development of agent-based intelligent DSSs for emergency management.* Paper presented at the Proceedings of the International Emergency Management Society Conf. TIEMS.

Gao, A., Lu, N., Wang, Y., Dai, P., Li, T., Gao, X., . . . Fan, C. (2012). Enhanced sensing of nucleic acids with silicon nanowire field effect transistor biosensors. *Nano letters, 12*(10), 5262-5268.

Garnett, E. C., & Yang, P. (2008). Silicon nanowire radial p− n junction solar cells. *Journal of the American Chemical Society, 130*(29), 9224-9225.

Georgiev, V. P., Mirza, M. M., Dochioiu, A.-I., Adamu-Lema, F., Amoroso, S. M., Towie, E., . . . Paul, D. J. (2017). Experimental and simulation study of silicon nanowire transistors using heavily doped channels. *IEEE Transactions on Nanotechnology, 16*(5), 727-735.

Gill, S. S., Kaushik, J., & Kaur, N. (2016). Performance Analysis of 20 nm Pentagonal and Trapezoidal NanoWire Transistor with Si and Ge Channel. *International Journal of Circuits and Electronics, 1*, 174-184.

Gluschke, J. G., Seidl, J., Burke, A., Lyttleton, R. W., Carrad, D. J., Ullah, A. R., . . . Micolich, A. P. (2018). Achieving short high-quality gate-all-around structures for horizontal nanowire field-effect transistors. *NANOTECHNOLOGY, 30*(6), 064001.

Gold_Standard_Simulations. (2019). Retrieved from http://www.goldstandardsimulations.com/

Greytak, A. B., Lauhon, L. J., Gudiksen, M. S., & Lieber, C. M. (2004). Growth and transport properties of complementary germanium nanowire field-effect transistors. *Applied Physics Letters, 84*(21), 4176-4178.

Halté, C., Delapierre, G., Costa, G., Fournier, T., Buckley, J., Gely, M., . . . Vinet, F. (2008). Rapid top-down fabrication of Si nanowire and fully automated test platform: application to pH, in pHealth. In: Valencia.

Hashim, Y. (2015). A Review on Transistors in Nano Dimensions. *International Journal of Engineering Technology and Sciences (IJETS), 4*(1), 8-18.

Hashim, Y., & Sidek, O. (2011). *Temperature effect on IV characteristics of Si nanowire transistor.* Paper presented at the 2011 IEEE Colloquium on Humanities, Science and Engineering.

Hashim, Y., & Sidek, O. (2012). Effect of temperature on the characteristics of silicon nanowire transistor. *Journal of nanoscience and nanotechnology, 12*(10), 7849-7852.

Hashim, Y., & Sidek, O. (2013). *Dimensional Effect on DIBL in Silicon Nanowire Transistors.* Paper presented at the Advanced Materials Research.

Huang, Y., Duan, X., Cui, Y., Lauhon, L. J., Kim, K.-H., & Lieber, C. M. (2001). Logic gates and computation from assembled nanowire building blocks. *Science, 294*(5545), 1313-1317.

Ioffe. (2019). Retrieved from http://www.ioffe.ru/SvA/NSM/Semicond/

Iwai, H., Natori, K., Shiraishi, K., Iwata, J.-i., Oshiyama, A., Yamada, K., . . . Ahmet, P. (2011). Si nanowire FET and its modeling. *Science China information sciences, 54*(5), 1004-1011.

Jang, M.-G., Kim, Y.-Y., Jun, M.-S., Choi, C.-J., Kim, T.-Y., Park, B.-C., & Lee, S.-J. (2006). Schottky Barrier MOSFETs with High Current Drivability for Nano-regime Applications. *JSTS: Journal of Semiconductor Technology and Science, 6*(1), 10-15.

Jayaswal, N., Raman, A., Kumar, N., & Singh, S. (2019). Design and analysis of electrostatic-charge plasma based dopingless IGZO vertical nanowire FET for ammonia gas sensing. *Superlattices and Microstructures, 125*, 256-270.

Jia, C., Lin, Z., Huang, Y., & Duan, X. (2019). Nanowire Electronics: From Nanoscale to Macroscale. *Chemical reviews, 119*(15), 9074-9135.

Khan, H., Razmjou, A., Ebrahimi Warkiani, M., Kottapalli, A., & Asadnia, M. (2018). Sensitive and flexible polymeric strain sensor for accurate human motion monitoring. *Sensors, 18*(2), 418.

Klimeck, G., McLennan, M., Brophy, S. P., Adams III, G. B., & Lundstrom, M. S. (2008). nanohub. org: Advancing education and research in nanotechnology. *Computing in Science & Engineering, 10*(5), 17.

L. A., H., H. (2002). what is nanotechnology. Retrieved from https://www.nano.gov/nanotech-101/what/definition

Lah, N. A., Zubir, M. N., Mahendran, A., & Samykano, L. (2018). Engineered Nanomaterial in Electronics and Electrical Industries. In *Handbook of nanomaterials for industrial applications* (pp. 324-364): Elsevier.

Liao, C., Chen, C., & Tu, K. (1999). Thermoelectric characterization of Si thin films in silicon-on-insulator wafers. *Journal of applied physics, 86*(6), 3204-3208.

Liao, Y.-B., Chiang, M.-H., Kim, K., & Hsu, W.-C. (2012). Assessment of structure variation in silicon nanowire FETs and impact on SRAM. *Microelectronics Journal, 43*(5), 300-304.

Lim, C.-M., Lee, I.-K., Lee, K. J., Oh, Y. K., Shin, Y.-B., & Cho, W.-J. (2017). Improved sensing characteristics of dual-gate transistor sensor using silicon nanowire arrays defined by nanoimprint lithography. *Science and Technology of advanced MaTerialS, 18*(1), 17-25.

Liu, M., Jin, P., Xu, Z., Hanaor, D. A., Gan, Y., & Chen, C. (2016). Two-dimensional modeling of the self-limiting oxidation in silicon and tungsten nanowires. *Theoretical and Applied Mechanics Letters, 6*(5), 195-199.

Lu, C.-C., Huang, J.-J., Luo, W.-C., Hou, T.-H., & Lei, T.-F. (2010). Strained silicon technology: mobility enhancement and improved short channel effect performance by stress memorization technique on nFET devices. *Journal of the Electrochemical Society, 157*(5), H497-H500.

Lupan, O., Postica, V., Labat, F., Ciofini, I., Pauporté, T., & Adelung, R. (2018). Ultra-sensitive and selective hydrogen nanosensor with fast response at room temperature based on a single Pd/ZnO nanowire. *Sensors and Actuators B: Chemical, 254*, 1259-1270.

Malits, M., Brouk, I., & Nemirovsky, Y. (2018). Study of CMOS-SOI Integrated Temperature Sensing Circuits for On-Chip Temperature Monitoring. *Sensors, 18*(5), 1629.

Martin, S., Baboux, N., Albertini, D., & Gautier, B. (2017). A new technique based on current measurement for nanoscale ferroelectricity assessment: Nano-positive up negative down. *Review of Scientific Instruments, 88*(2), 023901.

Meijer, G. C., Wang, G., & Fruett, F. (2001). Temperature sensors and voltage references implemented in CMOS technology. *IEEE sensors journal, 1*(3), 225-234.

Meyyappan, M. (2018). *Nanoscale vacuum electronics and large-scale silicon nanowire array fabrication for various applications (Conference Presentation).* Paper presented at the Quantum Sensing and Nano Electronics and Photonics XV.

Mikolajick, T., Heinzig, A., Trommer, J., Pregl, S., Grube, M., Cuniberti, G., & Weber, W. M. (2013). Silicon nanowires–a versatile technology platform. *physica status solidi (RRL)–Rapid Research Letters, 7*(10), 793-799.

Mirza, M. M., Schupp, F. J., Mol, J. A., MacLaren, D. A., Briggs, G. A. D., & Paul, D. J. (2017). One dimensional transport in silicon nanowire junction-less field effect transistors. *Scientific reports, 7*(1), 3004.

Mobarakeh, M. S., Omrani, S., Vali, M., Bayani, A., & Omrani, N. (2018). Theoretical logic performance estimation of Silicon, Germanium and SiGe nanowire Fin-Field Effect Transistor. *Superlattices and Microstructures, 120*, 578-587.

Musick, K. M., Wendt, J. R., Resnick, P. J., Sinclair, M. B., & Burckel, D. B. (2018). Assessing the manufacturing tolerances and uniformity of CMOS compatible metamaterial fabrication. *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena, 36*(1), 011208.

nanoHUB. (2019). Retrieved from https://nanohub.org/

Neizvestny, I. G. (2006). *Trends in Development of Modern Silicon Nanoelectronics.* Paper presented at the International Workshops and Tutorials on Electron Devices and Materials.

Oakley, B. (Producer). (2014). Learning How to Learn. Retrieved from https://www.youtube.com/watch?v=O96fE1E-rf8&feature=youtu.be

Oh, J. H., Hong, S. Y., Park, H., Jin, S. W., Jeong, Y. R., Oh, S. Y., . . . Ha, J. S. (2018). Fabrication of high-sensitivity skin-attachable temperature sensors with bioinspired microstructured adhesive. *ACS applied materials & interfaces, 10*(8), 7263-7270.

Park, H.-H., Zeng, L., Buresh, M., Wang, S., Klimeck, G., Mehrotra, S. R., . . . Haley, B. P. (2006). Nanowire.

Rachmady, W., Metz, M. V., Le, V. H., Kavalieros, J. T., & Gardner, S. K. (2019). Ge nano wire transistor with GaAs as the sacrificial layer. In: Google Patents.

Ramsden, J. (2018). *Applied nanotechnology: the conversion of research results to products*: William Andrew.

Rangasamy, M. (2011). Nano technology: a review. *Journal of Applied Pharmaceutical Science, 1*(2), 8-16.

Rani, D., Pachauri, V., & Ingebrandt, S. (2018). Silicon Nanowire Field-Effect Biosensors. In *Label-free Biosensing* (pp. 27-57): Springer.

Ratnakumar, K. (1982). Short-channel MOST threshold voltage model. *IEEE Journal of Solid-State Circuits, 17*(5), 937-948.

Reta, N., Saint, C. P., Michelmore, A., Prieto-Simon, B., & Voelcker, N. H. (2018). Nanostructured electrochemical biosensors for label-free detection of water-and food-borne pathogens. *ACS applied materials & interfaces, 10*(7), 6055-6072.

Reverter, F., Perpiñà, X., León, J., Vellvehi, M., Jordà, X., & Altet, J. (2015). Characterization of MOSFET temperature sensors for on-chip dynamic thermal measurements. *Procedia engineering, 120*, 836-839.

Rony, M. W. (2016). *Short channel effects suppression and process variability in a dual-gate Gate-All-Around Si nanowire transistor*: Lamar University-Beaumont.

Schwalbach, E., & Voorhees, P. W. (2009). Doping nanowires grown by the vapor-liquid-solid mechanism. *Applied Physics Letters, 95*(6), 063105.

Schwartz, M., Nguyen, T. C., Vu, X. T., Wagner, P., Thoelen, R., & Ingebrandt, S. (2018). Impedimetric Sensing of DNA with Silicon Nanowire Transistors as Alternative Transducer Principle. *physica status solidi (a), 215*(15), 1700740.

Selberherr, S., & Langer, E. (1989). *Low temperature MOS device modeling.* Paper presented at the Proceedings of the Workshop on Low Temperature Semiconductor Electronics.

Sellier, J. M., Fonseca, J. E., & Klimeck, G. (2012). *Archimedes, the free Monte Carlo simulator: A GNU package for submicron semiconductor devices on nanoHUB.* Paper presented at the 2012 15th International Workshop on Computational Electronics.

Shi, W., Yu, X., Zheng, Y., & Yu, J. (2016). DNA based chemical sensor for the detection of nitrogen dioxide enabled by organic field-effect transistor. *Sensors and Actuators B: Chemical, 222*, 1003-1011.

Silvaco. (2019). Retrieved from https://www.silvaco.com/

Singh, A., Dubey, S., & Dubey, H. K. (2019). NANOTECHNOLOGY: THE FUTURE ENGINEERING. *NANOTECHNOLOGY, 6*(2).

Singh, N., Buddharaju, K. D., Manhas, S., Agarwal, A., Rustagi, S. C., Lo, G., . . . Kwong, D.-L. (2008). Si, SiGe nanowire devices by top–down technology and their applications. *IEEE Transactions on Electron Devices, 55*(11), 3107-3118.

Singh, S., & Chauhan, S. S. (2017). *TCAD simulations of double gate tunnel field effect transistor with spacer drain overlap base on vertical Tunneling.* Paper presented at the Electronics, Communication and Aerospace Technology (ICECA), 2017 International conference of.

Sze, S. M., & Ng, K. K. (2006). *Physics of semiconductor devices*: John wiley & sons.

Taniguchi, N. (1974). *Japan society of precision engineering.* Paper presented at the On the Basic Concept of Nanotechnology: Proc. Intern. Conf. of Production Engineering.

Tran, D. P., Pham, T. T. T., Wolfrum, B., Offenhäusser, A., & Thierry, B. (2018). CMOS-compatible silicon nanowire field-effect transistor biosensor: Technology development toward commercialization. *Materials, 11*(5), 785.

Turzynski, M., & Kulesza, W. J. (2015). A simplified behavioral mosfet model based on parameters extraction for circuit simulations. *IEEE Transactions on Power Electronics, 31*(4), 3096-3105.

Ullah, A., Carrad, D., Krogstrup, P., Nygård, J., & Micolich, A. (2018). Near-thermal limit gating in heavily doped III-V semiconductor nanowires using polymer electrolytes. *Physical Review Materials, 2*(2), 025601.

Vallett, A. L., Minassian, S., Kaszuba, P., Datta, S., Redwing, J. M., & Mayer, T. S. (2010). Fabrication and characterization of axially doped silicon nanowire tunnel field-effect transistors. *Nano letters, 10*(12), 4813-4818.

ViennaSHE. (2019). Retrieved from http://viennashe.sourceforge.net/

Vikesland, P. J. (2018). Nanosensors for water quality monitoring. *Nature nanotechnology, 13*(8), 651-660.

Wang, A.-P., Hou, C.-E., & Hung, S.-W. (2018). Exploration of the evolution of nanotechnology from a patent co-classification perspective. *Nanotechnology Reviews, 7*(3), 233-245.

Wang, J. (2005). *Device physics and simulation of silicon nanowire transistors.* Citeseer,

Wang, J., Polizzi, E., & Lundstrom, M. (2004). A three-dimensional quantum simulation of silicon nanowire transistors with the effective-mass approximation. *Journal of applied physics, 96*(4), 2192-2203.

Watson, J., & Castro, G. (2015). A review of high-temperature electronics technology and applications. *Journal of Materials Science: Materials in Electronics, 26*(12), 9226-9235.

Webster, J. G., & Eren, H. (2016). *Measurement, instrumentation, and sensors handbook: spatial, mechanical, thermal, and radiation measurement*: CRC press.

Weinbub, J. (2014). *Frameworks for Micro-and Nanoelectronics Device Simulation.* Dissertation TU Wien,

Williams, R. K., Darwish, M. N., Blanchard, R. A., Siemieniec, R., Rutter, P., & Kawaguchi, Y. (2017). The trench power MOSFET—Part II: Application specific VDMOS, LDMOS, packaging, and reliability. *IEEE Transactions on Electron Devices, 64*(3), 692-712.

Wu, S.-H., Yu, C.-L., Yu, C.-H., & Su, P. (2016). Theoretical investigation of DIBL characteristics for scaled Tri-gate InGaAs-OI n-MOSFETs including sensitivity to process variations. *IEEE Journal of the Electron Devices Society, 5*(1), 45-52.

Yan, H., Choe, H. S., Nam, S., Hu, Y., Das, S., Klemic, J. F., . . . Lieber, C. M. (2011). Programmable nanowire circuits for nanoprocessors. *Nature, 470*(7333), 240.

Zafar, S., D'Emic, C., Jagtiani, A., Kratschmer, E., Miao, X., Zhu, Y., . . . Shahidi, G. (2018). Silicon Nanowire Field Effect Transistor Sensors with Minimal Sensor-to-Sensor Variations and Enhanced Sensing Characteristics. *ACS nano, 12*(7), 6577-6587.