

ANALYSIS AND STUDY OF POWER-
EFFICIENT SAR ADC FOR ACTIVE RFID
SENSOR

AHMAD AZZREEN BIN DALAWI

MASTER OF SCIENCE

UNIVERSITI MALAYSIA PAHANG

SUPERVISOR'S DECLARATION

We hereby declare that we have checked this thesis and in our opinion, this thesis is adequate in terms of scope and quality for the award of the degree of Master of Science.



(Supervisor's Signature)

Full Name : IR. DR. FAHMI BIN SAMSURI

Position : ASSOCIATE PROFESSOR

Date : 28 JUNE 2021



(Co-supervisor's Signature)


Full Name : IR. DR. AYIB ROSDI BIN ZAINUN

Position : SENIOR LECTURER

Date : 28 JUNE 2021

STUDENT'S DECLARATION

I hereby declare that the work in this thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at Universiti Malaysia Pahang or any other institutions.



(Student's Signature)

Full Name : AHMAD AZZREEN BIN DALAWI

ID Number : MEL14004

Date : 21 JUNE 2021

ANALYSIS AND STUDY OF POWER-EFFICIENT SAR ADC FOR ACTIVE
RFID SENSOR

AHMAD AZZREEN BIN DALAWI

Thesis submitted in fulfillment of the requirements
for the award of the degree of
Master of Science

College of Engineering
UNIVERSITI MALAYSIA PAHANG

AUGUST 2021

ACKNOWLEDGEMENTS

Alhamdulillah, the highest thanks to God because with His will, I was able to finally completed my master's degree. It was long overdue and better late than never. I would like to express my greatest gratitude and sincere appreciation to everyone who is involved directly or indirectly in completing this research. Honestly, without their invaluable support and guidance, my research would not have been completed.

My greatest and deepest appreciation and gratitude goes to my research supervisor and co-supervisor, Associate Professor Ir. Dr. Fahmi Bin Samsuri and Ir. Dr. Ayib Rosdi Bin Zainun respectively as their guidance and untiring support throughout my research. With their visionary advice and patient mentoring, this research was executed with success.

And finally, I would like to extend my appreciation to my family members for their financial and moral support from the start of this journey until the end. Thank you.

ABSTRAK

Tesis ini memperkenalkan daftar anggaran berturut-turut (SAR) penukar analog-ke-digital (ADC) cekap tenaga istimewa untuk sensor aktif bagi sistem tag pengenalan frekuensi radio rendah (RFID). Sebagai sebahagian daripada transformasi perkara Internet (IoT), RFID digunakan secara meluas. Dalam aplikasi di mana bekalan kuasa adalah terhad, penggunaan kuasa sentiasa menjadi kriteria yang ketara seperti litar analog seperti litar ADC, litar pengawal selia, litar penerus dan frekuensi radio (RF) adalah komponen yang biasa memerlukan kuasa dalam sistem. Biasanya, keperluan untuk prestasi bateri yang lebih lama berkait rapat dengan penggunaan kuasa rendah. Bagi sensor RFID aktif aplikasi yang memerlukan resolusi rendah dan sederhana serta penggunaan kuasa rendah, SAR ADC biasanya digunakan kerana ianya sebahagian daripada litar ADC. Oleh itu, SAR ADC yang cekap kuasa dibentangkan dalam kerja ini. Blok ADC SAR seperti blok pembanding, blok penukar digital-untuk-analog (DAC), dan blok sampler direka untuk memenuhi keperluan pengukuran prestasi penggunaan kuasa rendah. Tesis ini pada mulanya akan meneroka perbezaan antara teknik ADC dalam kerja-kerja sebelumnya. SAR ADC yang dicadangkan dibentangkan untuk meningkatkan penggunaan kuasa SAR ADC dalam aplikasi sensor RFID aktif menerusi pelaksanaan satu komparator input tunggal dengan DAC kapasitor beralih. Dalam bentuk seni bina ini, hanya terdapat satu input kepada komparator, dan hanya satu set dan kapasitor pensampelan berasingan dalam DAC kapasitor yang ditukar untuk menghasilkan paras rujukan yang diperlukan. Perbezaan voltan input dan output SAR SAR yang dicadangkan adalah petunjuk untuk reka bentuk kuasa rendah. Pengaruh kapasitansi parasit dikurangkan sehingga menjadi bukan faktor. Parameter SAR ADC adalah resolusi 8-bit, frekuensi persampelan 500 kHz, voltan bekalan 1 V dan 0.18 μm semikonduktor-logam-oksida pelengkap. Penggunaan kuasa ADC SAR yang dicadangkan adalah 2.3 μW di mana peningkatan 25.8% daripada kerja sebelumnya. Permintaan untuk penggunaan kuasa rendah RFID aktif sensor diperiksa dengan baik. Kesahihan reka bentuk yang dicadangkan telah dibuktikan oleh hasil simulasi.

ABSTRACT

Abstract— This thesis introduced an energy-efficient successive-approximation-register (SAR) analog-to-digital converter (ADC) specialized to the active sensors for low-power radio frequency identification (RFID) tag system. As part of the Internet of Things (IoT) transformation, RFID is widely used. In the application where the power supply is limited, power consumption is always a notable criterion as analog circuits such as the ADC circuit, regulator circuit, rectifier circuit and radio frequency (RF) are the common power demanding parts in the system. Normally, the requirement for a longer battery performance is closely related to low-power consumption. For the application active RFID sensor in which requires low to moderate resolution and speed as well as low-power consumption, SAR is usually used as its part of the ADC circuit. Therefore, the power-efficient SAR ADC is presented in this work. The block of SAR ADCs such as the comparator block, digital-to-analog converter (DAC) block, and sampler block is designed to meet the requirement of a low-power consumption performance measurement. This thesis at first will explore the differences between multiple ADC techniques in the previous works. The proposed SAR ADC is presented to enhance the power consumption of SAR ADC in the active RFID sensor application through the implementation of a single-input comparator with the switched-capacitor DAC. In this form of architecture, there is only one input to the comparator, and only one set and a split sampling capacitor in the switched capacitor DAC to generate the required reference levels. The difference in input and output voltage of the proposed SAR ADC is the indication for the low-power design. The influence of parasitic capacitance is reduced to the extent of becoming a non-factor. The parameters of the SAR ADC are the resolution of 8-bit, the sampling frequency of 500 kHz, the supply voltage of 1 V, and the 0.18 μm complementary metal-oxide-semiconductor (CMOS) technology. The power consumption of the proposed SAR ADC is 2.3 μW which is estimated at around 25.8% improvement from the previous work. The demands for low-power consumption of RFID active sensor is well examined. The validity of the proposed design has been proven by the simulation results.

TABLE OF CONTENT

DECLARATION	
TITLE PAGE	
ACKNOWLEDGEMENTS	ii
ABSTRAK	iii
ABSTRACT	iv
TABLE OF CONTENT	v
LIST OF TABLES	viii
LIST OF FIGURES	ix
LIST OF SYMBOLS	xi
LIST OF ABBREVIATIONS	xii
CHAPTER 1 INTRODUCTION	1
1.1 Motivation	1
1.2 Problem statement	5
1.3 Objectives	6
1.4 Scope of the work	7
1.5 Organization of the thesis	9
CHAPTER 2 LITERATURE REVIEW	10
2.1 Introduction	10
2.1 RFID Sensor Integration	10
2.2 SAR ADC Architecture	13
2.3 Summary	21

CHAPTER 3 METHODOLOGY	22
3.1 Introduction	22
3.2 Proposed SAR ADC	25
3.2.1 Design of proposed comparator	27
3.2.2 Design of the proposed DAC	33
3.2.3 Design of the proposed sampler	43
3.3 Configuration in Cadence Virtuoso	45
3.4 Summary	47
CHAPTER 4 RESULTS AND DISCUSSION	49
4.1 Introduction	49
4.2 Simulation result of sampler	49
4.2.1 Input test of the sampler sine wave	50
4.3 Simulation result of the comparator	52
4.3.1 Various input of the supply voltage	53
4.3.2 Ramp test of the comparator	57
4.3.3 Stress test of the comparator	58
4.4 Simulation result of DAC	59
4.4.1 Binary-weighted test of the DAC	60
4.4.2 Stress test of DAC	66
4.5 Simulation result of SAR ADC power consumption	67
4.6 Summary	71
CHAPTER 5 CONCLUSION	74
5.1 Introduction	74
5.2 Conclusion	74

5.3 Future Work 75

REFERENCES 77

LIST OF TABLES

Table 1.1	The working frequency of RFID	8
Table 2.1	Comparison between previous literature review of SAR ADCs	16
Table 4.1	The gain errors and output slopes comparison between traditional SAR ADC and proposed design SAR ADC	70
Table 4.2	Comparison between previous literature review of SAR ADCs and this work	73

LIST OF FIGURES

Figure 1.1	Global RFID market report analysis from 2014 - 2025	2
Figure 2.1	The block diagram of the RFID tag (not equipped with sensor)	11
Figure 2.2	The block diagram of the RFID tag sensor	14
Figure 2.3	The block diagram of the data-driven noise-reduction	18
Figure 2.4	The implementation of the there-level comparator method	19
Figure 2.5	The implementation of 3-bit capacitor swapping DAC	20
Figure 3.1	The block diagram of the RFID sensor	23
Figure 3.2	The overall process block diagram of the SAR ADC	24
Figure 3.3	The overall process flow-chart of the proposed design	25
Figure 3.4	The overall architecture of the proposed SAR ADC	26
Figure 3.5	The schematic of the proposed SAR ADC	27
Figure 3.6	The operation flow-chart of the proposed SAR ADC	28
Figure 3.7	The block diagram of the traditional SAR ADC circuit	29
Figure 3.8	The implementation of the proposed SAR ADC circuit	31
Figure 3.9	The architecture of the proposed DAC	33
Figure 3.10	The conversion procedure of the proposed circuit	34
Figure 3.11	The reset state of the proposed DAC	36
Figure 3.12	The recharging state of the proposed DAC	37
Figure 3.13	The charge-disposing state of the proposed DAC	38
Figure 3.14	The conversion of the proposed DAC in step 5	40
Figure 3.15	The conversion of the proposed DAC in step 7	41
Figure 3.16	The design of the internal switches of the sampler	43
Figure 3.17	The architecture of the proposed sampler	45
Figure 3.18	Block diagram of the library path connection configuration	46
Figure 3.19	Selection of the connect rule	46
Figure 3.20	The block diagram of the selection of connect rule	47
Figure 3.21	Connect rule values setting	47
Figure 4.1	The schematic of the sampler test bench	50
Figure 4.2	The result of the sampler sine waveform	51
Figure 4.3	The result of the enlarged sampler sine waveform	52
Figure 4.4	The schematic of the comparator test bench	53
Figure 4.5	The result of the comparator with the supply voltage of 100mV	54
Figure 4.6	The result of the comparator with the supply voltage of -100mV	55

Figure 4.7	The result of the comparator with the supply voltage of -10mV	55
Figure 4.8	The result of the comparator with the supply voltage of 10mV	56
Figure 4.9	The result of the comparator with the supply voltage of 2mV	57
Figure 4.10	The result of the comparator with the supply voltage of -2mV	57
Figure 4.11	The result of the comparator ramp test	58
Figure 4.12	The result of the comparator stress test	59
Figure 4.13	The schematic of the DAC test bench	60
Figure 4.14	The result of reference level ~ 865mV, input voltage = 870mV, reference binary = 11011110	61
Figure 4.15	The result of reference level ~ 865mV, input voltage = 750mV, reference binary = 11011110	62
Figure 4.16	The result of the reference level of ~ 505mV, input voltage of 700mV, and reference binary of 10000001.	62
Figure 4.17	The result of the reference level of ~ 505mV, input voltage of 400mV, and reference binary of 10000001.	63
Figure 4.18	The result of the reference level of ~ 255mV, input voltage of 400mV, and reference binary of 01000001.	63
Figure 4.19	The result of the reference level of ~ 255mV, input voltage of 200mV, and reference binary of 01000001.	64
Figure 4.20	The result of the reference level of ~ 85mV, input voltage of 200mV, and reference binary of 00010101.	64
Figure 4.21	The result of the reference level of ~ 85mV, input voltage of 75mV, and reference binary of 00010101.	65
Figure 4.22	The result of the reference level of ~ 620mV, input voltage of 630mV, and reference binary of 10011111.	65
Figure 4.23	The result of the reference level of ~ 620 mV, input voltage of 500 mV, and reference binary of 10011111.	66
Figure 4.24	The result of the DAC stress test	67
Figure 4.25	The result of the proposed SAR ADC	68
(a)	The traditional SNDR value for ADC output	69
	Source: (Wang et al., 2010)	69
(b)	The proposed method SNDR value for ADC output	69
Figure 4.26	Difference between the traditional (a) (Wang et al., 2010) and the proposed method (b) in the estimated energy dissipation for ADC output.	69

REFERENCES

- Barnett, R. E., & Liu, J. (2008). An EEPROM Programming Controller for Passive UHF RFID Transponders with Gated Clock Regulation Loop and Current Surge Control. *IEEE Journal of Solid-State Circuits*, 43(August).
- Bhattacharyya, R., Kalansuriya, P., Sarma, S., & Karmakar, N. (2012). Towards SCARS : a chipless RFID sensor for pervasive surface crack detection. *2012 IEEE International Conference on RFID Technologies and Applications*, 46–51.
- Caizzone, S., & DiGiampaolo, E. (2015). Wireless Passive RFID Crack Width Sensor for Structural Health Monitoring. *IEEE Sensors Journal*, 15(12), 6767–6774. <https://doi.org/10.1109/JSEN.2015.2457455>
- Cardullo, M. W., & Parks, W. L. (1973). *Transponder Apparatus and System*.
- Catarinucci, L., Colella, R., & Tarricone, L. (2009). A cost-effective UHF RFID tag for transmission of generic sensor data in wireless sensor networks. *IEEE Transactions on Microwave Theory and Techniques*, 57(5), 1291–1296. <https://doi.org/10.1109/TMTT.2009.2017296>
- Chang, S. Il, & Yoon, E. (2009). A low-power area-efficient 8 bit SAR ADC using dual capacitor arrays for neural microsystems. *Proceedings of the 31st Annual International Conference of the IEEE Engineering in Medicine and Biology Society: Engineering the Future of Biomedicine, EMBC 2009*, 1647–1650. <https://doi.org/10.1109/IEMBS.2009.5333068>
- Cho, Y.-K., Jeon, Y.-D., Nam, J.-W., & Kwon, J.-K. (2010). A 9-bit 80 MSs Successive Approximation Register Analog-to-Digital Converter With a Capacitor Reduction Technique. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 57(7), 502–506. <https://doi.org/10.1109/TCSII.2010.2048387>
- Choi, B. S., Lee, J. W., Lee, J. J., & Park, K. T. (2011). A hierarchical algorithm for indoor mobile robot localization using RFID sensor fusion. *IEEE Transactions on Industrial Electronics*, 58(6), 2226–2235. <https://doi.org/10.1109/TIE.2011.2109330>
- Curty, J.-P., Joehl, N., Krummenacher, F., Dehollain, C., & Dehollain, C. (2005). A model for μ -power rectifier analysis and design. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 52(12), 2771–2779. <https://doi.org/10.1109/TCSI.2005.854294>

- De Donno, D., Catarinucci, L., Di Serio, A., & Tarricone, L. (2013). A long-range computational RFID tag for temperature and acceleration sensing applications. *Progress In Electromagnetics Research C*, 45(October), 223–235. <https://doi.org/10.2528/PIERC13101904>
- De Donno, D., Catarinucci, L., & Tarricone, L. (2014). RAMSES: RFID augmented module for smart environmental sensing. *IEEE Transactions on Instrumentation and Measurement*, 63(7), 1701–1708. <https://doi.org/10.1109/TIM.2014.2298692>
- Dey, S., Saha, J. K., & Karmakar, N. C. (2015). Smart Sensing: Chipless RFID Solutions for the Internet of Everything. *IEEE Microwave Magazine*, 16(10), 26–39. <https://doi.org/10.1109/MMM.2015.2465711>
- Gasco, F., Feraboli, P., Braun, J., Smith, J., Stickler, P., & Deoto, L. (2011). Wireless strain measurement for structural testing and health monitoring of carbon fiber composites. *Composites Part A: Applied Science and Manufacturing*, 42(9), 1263–1274. <https://doi.org/10.1016/j.compositesa.2011.05.008>
- Glidden, R., Bockorick, C., Cooper, S., Diorio, C., Dressler, D., Gutnik, V., Hagen, C., Hara, D., Hass, T., Humes, T., Hyde, J., Pesavento, A., Oliver, R., Onen, O., Sundstrom, K., & Thomas, M. (2004). Design of ultra-low-cost UHF RFID tags for supply chain applications. *IEEE Communications Magazine*, 42(8), 140–151. <https://doi.org/10.1109/MCOM.2004.1321406>
- Harpe, P. (2016). Successive Approximation Analog-to-Digital Converters Improving Power Efficiency and Conversion Speed. *IEEE Solid-State Circuits Magazine*, 8(4), 64–73. <https://doi.org/10.1109/MSSC.2016.2573978>
- Harpe, P., Cantatore, E., & Roermund, A. van. (2013). A 10b/12b 40 kS/s SAR ADC With Data-Driven Noise Reduction Achieving up to 10.1b ENOB at 2.2 fJ/Conversion-Step. *IEEE Journal of Solid-State Circuits*, 48(12), 3011–3018. <https://doi.org/10.1109/JSSC.2013.2278471>
- Harpe, P., Cantatore, E., & Roermund, A. van. (2014). 11.1 An oversampled 12/14b SAR ADC with noise reduction and linearity enhancements achieving up to 79.1dB SNDR. *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 11, 194–196. <https://doi.org/10.1109/ISSCC.2014.6757396>
- Harpe, P., Zhou, C., Wang, X., Dolmans, G., & Groot, H. de. (2010). A 30fJ/conversion-step 8b 0-to-10MS/s asynchronous SAR ADC in 90nm CMOS. *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, 388–389.

<https://doi.org/10.1109/ISSCC.2010.5433967>

- Juels, A. (2006). RFID security and privacy: A research survey. *IEEE Journal on Selected Areas in Communications*, 24(2), 381–394.
<https://doi.org/10.1109/JSAC.2005.861395>
- Karthaus, U., & Fischer, M. (2003). Fully Integrated Passive UHF RFID Transponder IC with 16.7- μ W Minimum RF Input Power. *IEEE Journal of Solid-State Circuits*, 38(10), 1602–1608. <https://doi.org/10.1109/JSSC.2003.817249>
- Kim, H., Min, Y., Kim, Y., & Kim, S. (2008). A low power consumption 10-bit rail-to-rail SAR ADC using a C-2C capacitor array. *2008 IEEE International Conference on Electron Devices and Solid-State Circuits, December*, 1–4. <https://doi.org/978-1-4244-2539-6>
- Kocer, F., & Flynn, M. P. (2005). A new transponder architecture for long-range telemetry applications. *Proceedings of the 2005 European Conference on Circuit Theory and Design*, 2(5), 177–180. <https://doi.org/10.1109/ECCTD.2005.1523022>
- Kotani, K., Sasaki, A., & Ito, T. (2009). High-Efficiency Differential-Drive CMOS Rectifier for UHF RFID. *IEEE Journal of Solid-State Circuits*, 44(11), 3011–3018. <https://doi.org/10.1109/JSSC.2009.2028955>
- Lakafosis, V., Rida, A., Vyas, R., Yang, L., Nikolaou, S., & Tentzeris, M. M. (2010). Progress towards the first wireless sensor networks consisting of inkjet-printed, paper-based RFID-enabled sensor tags. *Proceedings of the IEEE*, 98(9), 1601–1609. <https://doi.org/10.1109/JPROC.2010.2049622>
- Landt, J. (2005). The history of RFID. *IEEE Potentials*, 24(4), 8–11. <https://doi.org/10.1109/MP.2005.1549751>
- Leon-Salas, W. D., & Halmen, C. (2016). A RFID Sensor for Corrosion Monitoring in Concrete. *IEEE Sensors Journal*, 16(1), 32–42. <https://doi.org/10.1109/JSEN.2015.2476997>
- Li, Z., & Meng, Z. (2016). A review of the radio frequency non-destructive testing for carbon-fibre composites. *Measurement Science Review*, 16(2), 68–76. <https://doi.org/10.1515/msr-2016-0010>
- Lien, W. L., Choke, T. Y., Tan, Y. C., Kong, M., Low, E. C., Li, D. P., Jin, L., Zhang,

- H., Leow, C. H., Chew, S. L., Dasgupta, U., Shana'A, O., Yong, C. H., Gao, T. B., Ong, G. T., Tan, W. G., Shu, W., & Heng, C. L. (2014). 9.1 A self-calibrating NFC SoC with a triple-mode reconfigurable PLL and a single-path PICC-PCD receiver in 0.11 μ m CMOS. *IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 158–159. <https://doi.org/10.1109/ISSCC.2014.6757380>
- Liew, W.-S., Yao, L., & Lian, Y. (2008). A moving binary search SAR-ADC for low power biomedical data acquisition system. *APCCAS 2008 - 2008 IEEE Asia Pacific Conference on Circuits and Systems, December*, 646–649. <https://doi.org/10.1109/APCCAS.2008.4746106>
- Liew, W.-S., Zou, X., Yao, L., & Lian, Y. (2009). A 1-V 60- μ W 16-channel interface chip for implantable neural recording. *2009 IEEE Custom Integrated Circuits Conference, October*, 507–510. <https://doi.org/10.1109/CICC.2009.5280795>
- Liu, C. C., Chang, S. J., Huang, G. Y., & Lin, Y. Z. (2010). A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure. *IEEE Journal of Solid-State Circuits*, 45(4), 731–740. <https://doi.org/10.1109/JSSC.2010.2042254>
- López-Soriano, S., & Parrón, J. (2015). Wearable RFID tag antenna for healthcare applications. *2015 IEEE-APS Topical Conference on Antennas and Propagation in Wireless Communications (APWC), October*, 287–290. <https://doi.org/10.1109/APWC.2015.7300156>
- Mahmoud, S. A., & Nazzal, T. B. (2015). Sample and hold circuits for low-frequency signals in analog-to-digital converter. *2015 International Conference on Information and Communication Technology Research (ICTRC)*. <https://doi.org/10.1109/ICTRC.2015.7156415>
- Meng, Z., & Lu, J. (2016). A Rule-based Service Customization Strategy for Smart Home Context-Aware Automation. *IEEE Transactions on Mobile Computing*, 15(3), 558–571. <https://doi.org/10.1109/TMC.2015.2424427>
- NFC Forum. (2011). *Type 4 tag operation specification*. http://apps4android.org/nfc-specifications/NFCForum-TS-Type-4-Tag_2.0.pdf
- Nguyen, S. D., Pham, T. T., Blanc, E. F., Le, N. N., Dang, C. M., & Tedjini, S. (2013). Approach for quality detection of food by RFID-based wireless sensor tag. *Electronics Letters*, 49(25), 1588–1589. <https://doi.org/10.1049/el.2013.3328>

- Occhiuzzi, C., Paggi, C., & Marrocco, G. (2011). Passive RFID strain-sensor based on meander-line antennas. *IEEE Transactions on Antennas and Propagation*, 59(12), 4836–4840. <https://doi.org/10.1109/TAP.2011.2165517>
- Potyrailo, R. A., Nagraj, N., Tang, Z., Mondello, F. J., Surman, C., & Morris, W. (2012). Battery-free radio frequency identification (RFID) sensors for food quality and safety. *Journal of Agriculture and Food Chemistry*, 60(35), 8535–8543. <https://doi.org/10.1021/jf302416y>
- Rabuske, T., Rabuske, F., Fernandes, J., & Rodrigues, C. (2015). An 8-bit 0.35-V 5.04-fJ/Conversion-Step SAR with Background Self-Calibration. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 23(7), 1–7. <https://doi.org/1557-9999>
- Radio Frequency Identification Technology Market Size, Share & Trends Analysis Report By Product (RFID Tags, RFID Readers, and Middleware), By Frequency, By Application, By Region, And Segment Forecasts, 2018 - 2025.* (2017).
- Robert, P.-Y., Gosselin, B., Ayoub, A. E., & Sawan, M. (2006). An Ultra-Low-Power Successive-Approximation-Based ADC for Implantable Sensing Devices. *2006 49th IEEE International Midwest Symposium on Circuits and Systems*, 7–11. <https://doi.org/10.1109/MWSCAS.2006.381981>
- Sekimoto, R., Shikata, A., Yoshioka, K., Kuroda, T., & Ishikuro, H. (2012). A 40nm CMOS full asynchronous nano-watt SAR ADC with 98% leakage power reduction by boosted self power gating. *2012 IEEE Asian Solid State Circuits Conference (A-SSCC)*, 6, 161–164. <https://doi.org/10.1109/IPEC.2012.6522650>
- Shikata, A., Sekimoto, R., Kuroda, T., & Ishikuro, H. (2014). A 0.5 V 1.1 MS/sec 6.3 fJ/Conversion-Step SAR-ADC With Tri-Level Comparator in 40 nm CMOS. *IEEE Journal of Solid-State Circuits*, 47(4), 1022–1030. <https://doi.org/10.1109/JSSC.2012.2185352>
- Sunny, A. I., Tian, G. Y., Zhang, J., & Pal, M. (2016). Low frequency (LF) RFID sensors and selective transient feature extraction for corrosion characterisation. *Sensors and Actuators, A: Physical*, 241, 34–43. <https://doi.org/10.1016/j.sna.2016.02.010>
- Verma, D., Shehzad, K., Khan, D., Kim, S. J., Pu, Y. G., Yoo, S. S., Hwang, K. C., Yang, Y., & Lee, K. Y. (2020). A design of low-power 10-bit 1-MS/s asynchronous SAR ADC for DSRC application. *Electronics (Switzerland)*, 9(7), 1–11. <https://doi.org/10.3390/electronics9071100>

- Wang, H., Yen, M., & Zhang, C. (2010). Low power analog circuit design for RFID sensing circuits. *2010 IEEE International Conference on RFID (IEEE RFID 2010)*, May, 16–21. <https://doi.org/10.1109/RFID.2010.5467279>
- Weinstein, R. (2005). RFID: A technical overview and its application to the enterprise. *IT Professional*, 7(3), 27–33. <https://doi.org/10.1109/MITP.2005.69>
- Wu, M.-H., Chung, Y.-H., & Li, H.-S. (2012). A 12-bit 8.47-fJ/conversion-step 1-MS/s SAR ADC using capacitor-swapping technique. *2012 IEEE Asian Solid State Circuits Conference (A-SSCC)*, 6, 157–160. <https://doi.org/10.1109/IPEC.2012.6522649>
- Yakoub, M. E. M. A., Sawan, M., & Thibeault, C. (2009). A neuromimetic ultra low-power ADC for bio-sensing applications. *2009 Joint IEEE North-East Workshop on Circuits and Systems and TAISA Conference, October*, 1–4. <https://doi.org/10.1109/NEWCAS.2009.5290440>
- Yang, X., Zhou, Y., Zhao, M., Huang, Z., Deng, L., & Wu, X. (2014). A 0.9V 12-bit 200-kS/s 1.07 μ W SAR ADC with Ladder-based Reconfigurable Time-Domain Comparator. *2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 105–108. <https://doi.org/10.1109/MWSCAS.2014.6908363>
- Zhang, Y., & Bai, L. (2015). Rapid structural condition assessment using radio frequency identification (RFID) based wireless strain sensor. *Automation in Construction*, 54, 1–11. <https://doi.org/10.1016/j.autcon.2015.02.013>
- Zhiheng Cao, Yan, S., & Li, Y. (2008). A 32mW 1.25GSs 6b 2bstep SAR ADC in 0.13 μ m CMOS. *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, 542–634. <https://doi.org/10.1109/ISSCC.2008.4523297>