PATTERN LAYOUT OPTIMIZATION FOR LOW SERIES RESISTANCE AND CAPACITANCE IN GAN SCHOTTKY BARRIER DIODES

by

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ABSTRACT

Rectenna, which stands for rectifying antenna, is used to capture and convert the microwave power to the direct current. Applications of the rectenna are mainly focused between remote areas, where the physical power connections are not feasible for transferring power [29]. In this rectenna system, one of the important elements is Schottky barrier diode. This diode plays as a rectifier. This diode has to possess the following characteristics, such as low series resistance, R_S, low zero-biased junction capacitance, C_0 , low turn-on voltage, V_{ON} , and high breakdown voltage, V_{BR} in order to obtain a higher efficiency of conversion [1]. power However, the commercially-available Si and GaAs-based diodes have suffered from their low breakdown voltage which consequently allows them to be applicable only for low power transmission system. Thus, GaN is one of the candidates to replace these two materials due to its high breakdown voltage [4]. In this study, we introduced an Ultra-finger diode as this structure owned a longer Schottky perimeter. From this study, the trade-off relation between and series resistance and capacitance was revealed as the series resistance significantly decreased by expanding the perimeter of the Schottky contacts even at the similar Schottky area. This ultra-finger diode exhibited lower time constant, τ value than the conventional circular diode. The value of time constant is minimized by maximizing the value of Schottky perimeter multiplied with the area. From this investigation, we propose the ultra-finger diode as an alternative solution for better optimization for low series resistance and capacitance.

CHAPTER 1 : INTRODUCTION

1.1 Research Background

Rectenna, which stands for rectifying antenna, is used to capture and convert the microwave power to the direct current. It is one of the essential devices for the wireless power transmission (WPT) system [28]. Applications of the rectenna are mainly focused between remote areas, where the physical power connections are not feasible for transferring power [29]. For instance, it can be used for space-to-space, space-to-ground, ground-to-space and ground-to-ground power transmission [30]. A rectenna consists of antenna for receiving microwave power, filters for suppressing the energy loss and a diode as a rectifying component [31]. A simple block diagram of rectenna proposed by McSpadden is presented in Fig. 1 [26].



Fig. 1.1 Block diagram of rectenna

This diode is the main part of the rectifying circuit; it changes the AC microwave signal into a DC signal. In this circuit, in order to obtain high efficiency for a power c_{000} .

conversion, a diode has to possess the following characteristics, such as low series resistance, R_S , low zero-biased junction capacitance, C_0 , low turn-on voltage, V_{ON} , and high breakdown voltage, V_{BR} [1]. Fig. 2 shows the IV & CV characteristics of diode required for high efficiency rectenna applications.



Fig. 1.2 Characteristics of diode required for high efficiency rectenna applications

Company	Material	Model	$V_{ON}[V]$	$R_{s}[\Omega]$	C ₀ [pF]	$V_{BR}[V]$
Skyworks	Si	SMS7630	0.34	20	0.14	2
MA-COM	GaAs	MA4E1317	0.7	4	0.02	7
MA-COM	Si	MA4E2054-1141T	0.4	11	0.13	5
Avago Tech.	Si/GaAs	HSMS2860	0.35	6	0.18	7
Avago Tech.	Si/GaAs	HSMS-286C	0.35	6	0.18	7
Avago Tech.	GaAs	HSCH-9201	0.7	6	0.04	4.5

Table 1 Commercial available Schottky barrier diode

Many works have been reported regarding to high-efficiency rectenna and most of them used commercially available Schottky diode based on GaAs or Si. Table 1 shows several models of Si and GaAs Schottky barrier diode (SBD) which are available in the world market [36] [37] [38] [39] [40]. For instance, Chang et al. used MA-COM's commercial GaAs Schottky barrier diode, MA4E1317 in their circuits and gained 76% to 84.4% of efficiencies with input power of approximately 100 mW in their works [31] [32] [33] [29]. However, the maximum output voltage, V_0 is restricted due to the low breakdown voltage of GaAs. Theoretically, V_0 is limited to the half of diode's breakdown voltage [27]. Consequently, allows it to be applicable only for low power transmission system.

Thus, a diode based on another alternative material replacing Si and GaAs with a high breakdown voltage is needed. GaN is one of the candidates to replace these two materials [4]. With a relatively high breakdown voltage, GaN device application on high power of wireless transmission is expected. Recently, several studies of GaN Schottky diodes for microwave application have been reported [1] [2]. Takahashi and Lin groups proposed GaN diodes with $R_S = 25.6 \ \Omega$, $C_0=0.29 \ pF$ and $R_S = 19.5 \ \Omega$, $C_0=1.4 \ pF$, respectively. Even their capacitance values are considered small but the resistances are still high, which definitely leads to the increase of power consumption. Up to now, no studies regarding to an optimization of low R_S and C_0 in GaN SBD have ever been reported. In general, R_S is reduced by scale-up the Schottky electrode's size but in parallel, C_0 will proportionally increase. Here, intensive investigations are needed to reveal this trade-off relation so that low R_S and C_0 can be feasibly optimized in parallel.

1.2 Objective of this work

In this study, in order to reduce the series resistance and simultaneously maintains the capacitance to be low, several patterns are investigated to find the best optimization of this trade-off.

1.3 Research motivation

Many research groups used conventional circular SBD as their in their reports. From this circular structure, we designed several patterns within the same area by modifying the Schottky electrode's structure. Finally, we found the pattern that owned the longest perimeter. This pattern is called Ultra-finger diode as shown in Fig. 1.3 below. Blue and red color are defined as ohmic and Schottky contacts, respectively.



Fig. 1.3 The idea flow of Ultra-finger diode

For padding metallization, a conventional air-bridge technology is applied for connection between padding metal and Schottky finger or active Schottky metal [1]. This structure requires the epitaxial to be etched until high resistivity buffered layer or substrate. Then, the metal bridge is built on it. However, since this system was not developed in our laboratory, we introduced the multi-step mesa structure as an alternative for metal interconnection. An insulator is required between padding metal and buffered layer to make sure that the parasitic capacitance was totally suppressed. Fig. 1.4 below presents the schematic of an air-bridge and multiple-step mesa cross-sectional structure.



Fig. 1.4 Air-bridge and multi-step mesa cross-sectional structure

1.4 Organization of the thesis

Chapter 1 describes some briefing about rectenna background, the importance of the SBD diode in this system and the purpose of this work. Chapter 2 discusses the introduction of metal-semiconductor contacts and the theory of GaN Schottky barrier.

Chapter 3 explains the rectenna element theory of operation proposed by Kai Chang group as the calculation model of power conversion efficiency. Chapter 4 deals with the experimental procedures for the fabrication of this ultra-finger diode. All processes will be explained starting from the pattern layout until device measurements.

Chapter 5 deals with the results obtained and discussions regarding to the series resistance, capacitance, breakdown voltage and expected conversion efficiency and chapter 6 is the conclusion of the thesis.

CHAPTER 2 : METAL-SEMICONDUCTOR CONTACTS

2.1 Introduction

The Schottky contact is an important element in many GaN devices. It is essential for studying the electrical properties of a semiconductor material. The Schottky barrier is also used to study the bulk defects and interface properties of a metal-semiconductor system. For the performance of FETs the size and placement of the gate is a critical factor. The physics involved in metal-semiconductor contact is described in this section. The energy band diagrams for a metal and an n-type semiconductor material are shown in Figure 2.1 a. Both metal and semiconductor are electrically isolated from each other.



Fig. 2.1 Energy band diagram for a metal and an n-type semiconductor

In Figure 2.1, the cross-hatching signifies allowed states that are almost completely filled with electrons, whereas the vertical line represents the surface. The horizontal line

at the top is called the vacuum level, E_i , which denotes the minimum energy an electron must possess to completely free itself from the surface of the material. The metal work function, Φ_M , is defined as the minimum energy required to raise an electron from the metal surface into free space. Each metal has a constant metal work function. The work functions of various metals are given in Table 2.1 below [24] [25].

Metal	Work function. $\Phi_m(eV)$	Metal	Work function $\Phi_m(eV)$
Ag	4.26	Ni	5.15
Al	4.28	Pd	5.12
Au	5.1	Pt	5.65
Cr	4.5	Ti	4.33
Мо	4.6	Zr	4.03

 Table 2.1
 Work function of some metals

Table 2.2 Electron affinity of some semiconductors

element	electron affinity, $\chi_{s}(eV)$
Ge	4.13
Si	4.01
GaAs	4.07
GaN	4.1

The work function (ϕ_s) of a semiconductor material is the energy difference between the vacuum level and the Fermi energy level. The semiconductor work function, ϕ_s , is composed of two distinct parts; that is

$$\Phi_{\rm s} = \chi_{\rm s} + (E_{\rm c} - E_{\rm F}) \tag{2.1}$$

Where χ_s is the electron affinity, and is given by $\chi_s = (E_i - E_c)|$ surface. The electron affinities of several semiconductors are shown in Table 2.2 above [24] [25].



Fig. 2.2 Energy band diagram for Schottky contact after contact formation

Figure 2.2 shows energy band diagrams for a metal and n-type semiconductor system after contact formation. The work function of the semiconductor is less than that of the metal, i.e., $\phi_M > \phi_S$ which is the necessary condition for the formation of Schottky barriers between a metal and an n-type semiconductor. Figure 2.2(a) shows the condition when the metal comes into contact with the semiconductor. Since the Fermi level of the semiconductor is above that of the metal, the system is not in equilibrium. For the system to be under equilibrium, the Fermi energy level must be invariant with position throughout the structure.

Consequently, a short time after the contact formation, electrons from the semiconductor will flow into the lower energy states in the metal. The net loss of electrons from the semiconductor creates a surface depletion region and as a result the potential barrier seen by the electron, from the semiconductor to the metal increases. This phenomenon will continue until the Fermi level E_F is the same throughout the structure. The net equilibrium band diagram for an ideal $\phi_M > \phi_S$ metal to n-type semiconductor contact is shown in the Figure 2.2(b).

The barrier height for an ideal metal-semiconductor Schottky contact is equal to the difference between the work function of a metal ϕ_{M} and the electron affinity χ_{s} of a semiconductor. In other words it is the potential barrier seen by the electrons in the metal trying to move to the semiconductor. For a metal/n-type semiconductor Schottky contact this is given by

$$\phi_{\rm Bn} = \chi_{\rm M} - \chi_{\rm S} \tag{2.2}$$

The barrier seen by the electrons in the conduction band trying to move into the metal is known as the built-in potential and is denoted by V_{bi} and is given by

$$\mathbf{V}_{\mathbf{b}\mathbf{i}} = \mathbf{e}\mathbf{V}_{\mathbf{d}} = \mathbf{\phi}_{\mathbf{M}} - \mathbf{\phi}_{\mathbf{S}} \tag{2.3}$$

2.2 Schottky Barrier



Fig. 2.3 Response of bias voltage to a Schottky diode

When a forward bias voltage V > 0 is applied to the Schottky contact, the electrons in the semiconductor are attracted towards the metal. The Fermi level of the metal is lower than the Fermi level of the semiconductor. As a result, the barrier seen by the electrons in the semiconductor is reduced and therefore there is a net flow of electrons from the semiconductor to the metal. Increasing the forward bias voltage leads to a rapidly rising forward bias current, since an exponentially increasing number of electrons from the semiconductor are able to surmount the surface barrier. The current density determined by the electrons flow from the semiconductor to the metal is given as equation below.

$$J_{S \to M} = A^* T^2 \exp\left(\frac{-q(\phi_{Bn} - V)}{kT}\right)$$
(2.4)

where

$$A^{*} = \frac{4\pi q m^{*} k^{2}}{h^{3}}$$
(2.5)

is the effective Richardson constant for thermionic emission. For GaN case, the Richardson constant A is calculated as $26.7 \text{ Acm}^{-2} \text{K}^{-2}$.

On the other hand, when a reverse bias voltage V < 0 is applied as shown in Figure 2.4 (b), the Fermi level in the metal is above. As a result, the flow of electrons from the semiconductor to the metal is blocked. Though some electrons will be able to overcome the barrier, the associated reverse-bias current is small. Since the barrier height for electrons moving from the metal into the semiconductor remains the same under bias, the current flowing into the semiconductor is thus unaffected by the applied voltage. It must therefore be equal to the current flowing from the semiconductor into the metal

when thermal equilibrium prevails (i.e., V=0). This corresponding current density is obtained from Eq. 2.4 by setting V=0,

$$\mathbf{J}_{\mathbf{M}\to\mathbf{S}} = -\mathbf{A}^* \,\mathbf{T}^2 \exp\left(-\frac{\mathbf{q} \phi_{\mathbf{B}\mathbf{n}}}{\mathbf{k}\mathbf{T}}\right) \tag{2.6}$$

Hence, the total current density is derived by the sum of Eqs. (2.4) and (2.6).

$$J = \left[A^{*}T^{2}\exp\left(-\frac{q\varphi_{Bn}}{kT}\right)\right] \left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$
$$= J_{0}\left[\exp\left(\frac{qV}{kT}\right) - 1\right]$$
(2.7)

where J_0 is the saturation current density obtained by extrapolating the current density from the log-linear plot to V=0 as given by,

$$J_0 = A^* T^2 \exp\left(-\frac{q \Phi_{g_m}}{kT}\right)$$
(2.8)

From this equation, the Schottky barrier, ϕ_{Bn} , can be obtained as,

$$\Phi_{Bn} = \frac{kT}{q} \ln \frac{AT^2}{J_0}$$
(2.9)

Here, from Eqs. 2.7, the forward J-V characteristics with $V > \frac{3kT}{q}$ case, the total current density can be conveniently expressed as,

$$J = J_0 \left[\exp\left(\frac{qV}{nkT}\right) \right]$$
(2.10)

where n is the ideality factor which can be extracted from the slope plotted from the log-linear region in the J-V characteristics given by,

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$$\frac{1}{n} = \frac{kT}{q} \frac{d(\ln f)}{dV}$$
(2.11)

and ideality factor, n can be expressed as,

$$n = \frac{q}{kT} \frac{dV}{d(\ln J)}$$
(2.12)

CHAPTER 3 : RECTENNA ELEMENT THEORY OF OPERATION [26] [27]



Fig. 3.1 The five main rectenna element components: antenna, input low-pass filter, rectifying diode, output filter and resistive load.

Fig. 3.1 shows the main components of the rectenna element. A half-wave dipole attaches to a low-pass filter, which transforms the dipole impedance to the diode impedance and rejects higher order diode harmonics from radiating through the dipole. A diode placed in shunt across the transmission line is the rectifier. The output filter consisting of a large capacitor effectively shorts the RF energy and passes the dc power. The distance between the diode and output capacitor is used to resonate the capacitive reactance of the diode. Both input and output filters are used to store RF energy during the off period of the diode. A resistor is then placed across the output terminals to act as the load for measuring the output dc power. Finally, a reflecting metal plane is then placed behind the rectenna.

The typical operation of a rectenna element can be better understood by analyzing the diode's dc characteristics with an impressed RF signal. Fig. 3.2 shows an idealized RF voltage waveform operating across the diode and the diode junction voltage [13], [14].

This simple model assumes that the harmonic impedances seen by the diode are either infinite or zero to avoid power loss by the harmonics. Thus, the fundamental voltage wave is not corrupted by higher order harmonic components. The rectenna conversion efficiency then depends only on the diode electrical parameters and the circuit losses at the fundamental frequency and dc. A mathematical model of the diode efficiency has been derived under this condition [13] and expanded to account for varying input power levels.



Fig. 3.2 Rectification cycle represented by the input fundamental and diode junction voltage waveforms impressed on the diode IV curve. This model assumes there are no losses in the harmonics and $\theta = \omega t - \phi$.

The applied voltage waveform can be expressed as

$$\mathbf{V} = -\mathbf{V}_{\mathbf{0}} + \mathbf{V}_{\mathbf{1}} \cos \omega \mathbf{t} \tag{3.1}$$

where V_0 is the output self-bias dc voltage across the resistive load and V_1 is the peak voltage amplitude of the incident microwave signal. Similar to mixers, the rectenna is a self-biasing circuit. As the incident power increases, the output dc voltage becomes more reversed biased.

The junction voltage is

$$\mathbf{V}_{\mathbf{d}} = \begin{cases} -\mathbf{V}_{\mathbf{d}0} + \mathbf{V}_{\mathbf{d}1} \cos(\omega t - \phi), \text{ if diode is off} \\ \mathbf{V}_{\mathbf{b}i} & \text{if diode is on} \end{cases}$$
(3.2)

where V_{d0} and V_{d1} are the dc and fundamental frequency components of the diode junction voltage, and V_{bi} is the diode's built-in voltage in the forward bias region. Also shown in Fig. 2 are the forward-bias turn-on angles θ_{on} of \underline{V}_{d} and the phase difference ϕ between V and V_{d} .

Fig. 3.3 shows the equivalent circuit of the diode used for the derivation of the mathematical model. The diode parasitic reactive elements are not included in the equivalent circuit. Instead, it is assumed they belong to the rectenna's environment circuit. The environment circuit is defined as the circuit around the diode that consists of linear-circuit elements. The diode model consists of a series resistance R_s , a nonlinear junction resistance R_j described by its dc IV characteristics, and a nonlinear junction

capacitance C_j . A dc load resistor is connected in parallel to the diode along a dc path represented by a dotted line to complete the dc circuit. The junction resistance R_j is assumed to be zero for forward bias and infinite for reverse bias. By applying Kirchoff's voltage law, closed-form equations for the diode's efficiency and input impedance are determined.



Fig. 3.3 Circuit model of the rectifying circuit

To solve for the turn-on angle θ_{on} , several steps are taken. The output dc voltage V_0 can be related to the diode junction dc voltage by

$$-V_0 = V_{d,dc} \frac{R_L}{R_s + R_L}$$
(3.3)

In one cycle, the output voltage is determined from the rectified voltage wave V_d . The average value of V_d in one cycle is

$$V_{ddc} = \frac{1}{2\pi} \int_{-\theta_{on}}^{\theta_{on}} V_{bi} d\theta + \frac{1}{2\pi} \int_{\theta_{on}}^{2\pi - \theta_{on}} (-V_{d0} + V_{d1} \cos \theta) d\theta \qquad (3.4)$$

By solving the integrals, it will give as

$$V_{d,de} = \frac{\theta_{on}}{\pi} V_{bi} - V_{d0} \left(1 - \frac{\theta_{on}}{\pi} \right) - \frac{V_{d1}}{\pi} \sin \theta_{on}$$
(3.5)

When the diode switches from off-state to on-state, V_d is equal to the diode's built-in voltage. Equaling both equations in (3.2) gives

$$-\mathbf{V}_{d0} + \mathbf{V}_{d1} \cos \theta_{on} = \mathbf{V}_{b\bar{s}}$$
(3.6)

The expression for current flowing through R_S when the diode is switched off is

$$I = \frac{dQ}{dt} = \frac{d(C_j V_d)}{dt} = \frac{(V - V_d)}{R_s}$$
(3.7)

where C_j is a monotically increasing function of V_d and it can be expanded with Fourier series as follows

$$C_{j} = C_{0} + C_{1} \cos(\omega t - \phi) + C_{2} \cos(2\omega t - 2\phi) \dots$$
 (3.8)

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Substituting (8) into (7) results in

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$$\omega R_{s}(C_{1}V_{d0} - C_{0}V_{d1})\sin\theta = V_{d0} - V_{0} + (V_{1}\cos\phi - V_{d1})\cos\theta - V_{1}\sin\phi\sin\theta (3.9)$$

where $\omega t - \phi$ is replaced to θ for simplicity. Since the above equation holds also for the

off period of the diode, each term can be separated as

$$\mathbf{V}_{\mathbf{d}\mathbf{0}} = \mathbf{V}_{\mathbf{0}} \tag{3.10}$$

$$\mathbf{V_{d1}} = \mathbf{V_1} \cos \mathbf{\Phi} \tag{3.11}$$

$$-\mathbf{V}_{i}\sin\phi = \omega\mathbf{R}_{s}(\mathbf{C}_{i}\mathbf{V}_{d0} - \mathbf{C}_{0}\mathbf{V}_{d1})$$
(3.12)

Applying (3.10) and (3.3) into (3.5) provides

$$\frac{R_{\rm s}}{R_{\rm L}} = \frac{V_{\rm d1}}{V_0} \frac{1}{\pi} \sin \theta_{\rm on} - \frac{\theta_{\rm on}}{\pi} \left(1 + \frac{V_{\rm bi}}{V_0} \right) \tag{3.13}$$

Futhermore, ϕ in (3.11) can be approximated to be zero so that the variable $\theta = \omega t$ is applied in all integrations. Using this approximation (V_{d1}=V₁) and (3.12) both into (3.6) will determine the V₁ as

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$$V_1 = \frac{V_0 + V_{bi}}{\cos \theta_{on}}$$
(3.14)

Therefore, applying (3.14) into (3.13) allows θ_{on} to be given as

$$\tan \theta_{on} - \theta_{on} = \frac{\pi R_{S}}{R_{L} \left(1 + \frac{V_{h\bar{i}}}{V_{0}}\right)}$$
(3.15)

From here, we can understand that is a dynamic variable dependent on the diode's input power.