DEVELOPMENT OF WIRELESS DATA TRANSMISSION USING 8051 MICROCONTROLLER

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JUDUL: **DEVELOPMENT OF WIRELESS DATA TRANSMISSON USING 8051 MICROCONTROLLER**

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Date : 28 APRIL 2006

To my beloved father and mother

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Alhamdulillah, I’m grateful to the creator Allah S.W.T because of His regards I finally finish this final year project. Without His blessing it is difficult for me to overcome and face all problems while completing this project. I also would like to express thousand of thank to my supervisor, Mr Md. Rizal B. Othman who give highly encouragement, supporting and guideline in order to finish this task.

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ABSTRACT

As a human being we sometime in habit of lost an item such as keys, TV remote and so on. So we need devices that have ability searching to the lost item and save our time. By doing a research, I have found a device which meets this specification. Development board of wireless data transmission can be used to solve this matter. This board also can be used for other application such as to control the thing located in a small place which is difficult to us to enter as well as it can be used to control something located in a danger place such as ultraviolet wave. For trial, I do implement this board to locate and item. The main part of this board is microcontroller and interface with keypad and LCD display together with the requirement of radio frequency .The keypad is used to enter the names of the item and select the item. The user can then select the desired item and press the button to transmit the RF. The LCD will then will display the name of the item according to the key being pressed in keypad. Overall, this project consist of both hardware and software design. The microcontroller plays an important role to control the overall system design.

ABSTRAK

Sebagai manusia biasa, kita kadang kala mempunyai suatu habit kehilangan barang seperti kunci, alat kawalan tv dan sebagainya. Disebabkan oleh itu, kita memerlukan sejenis alat yang boleh membantu kita mencari barang yang hilang dan menjimatkan masa. Berdasarkan kajian yang telah dibuat, saya telah menjumpai sejenis alat yang menepati ciri-ciri yang telah dinyatakan. Alat penghantar data tanpa wayar boleh digunakan bagi mengatasi masalah ini. Walau bagaimanapun, alat ini juga boleh digunakan untuk aplikasi lain seperti untuk mengawal sesuatu yang berada di suatu tempat yang susah dicapai oleh manusia atau untuk mengawal sesuatu yang berada di kawasan merbahaya seperti radioaktif. Sebagai percubaan, alat ini digunakan untuk mencari objek yang hilang. Penghantaran data tanpa wayar ini dikawal oleh sejenis alat kawalan-mikro dan disambungkan kepada pad kekunci dan pemancar LCD bersama-sama dengan radio frekuensi. Pad kekunci digunakan untuk menyimpan nama-nama barang yang hilang, memilih barang yang hendak dicari dan menyimpan nombor ID barang yang hendak dicari. Apabila, pengguna ingin mencari barang yang hilang, mereka hanya perlu menekan “alert button” supaya signal radio frekuensi dapat dihantar. Pemancar LCD akan memancarkan nama-nama barang yang hendak dicari berdasarkan kekunci yang ditekan pada pad kekunci. Secara keseluruhannya, projek ini terdiri daripada dua bahagian utama iaitu alatan dan perisian. Alat pengawal-mikro memainkan peranan penting untuk mengawal keseluruhan system ini.

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LIST OF ABBREVIATION

RF	**Radio Frequency**
LCD	**Liquid Crystal Display**
TV	**Television**
CPU	**Central Processing Unit**
ROM	**Read Only Memory**
RAM	**Random Access Memory**
EPROM	**Erasable Programmable Read Only Memory**
DPTR	**Data Pointer**
I/O	**Input/Output**
SP	**Stack Pointer**
LSB	**Least Significant Bit**
MSB	**Most Significant Bit**

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CHAPTER1

INTRODUCTION

1.1 Background

The idea behind this project is to build a development board of wireless data transmission by using 8051 microcontroller. There are various type of microcontroller. The 8051 microcontroller originally developed by Intel in 1980. The purpose of choosing 8051 microcontroller is, it is the world's most popular microcontroller core, become the industry standard for embedded control and made by many independent manufacturers (truly multi-sourced), so it can easily get in the market. It is also simple and has enough features to meet with this project.

Wireless data transmissions are widely used in modern technology. The signal or data being transmitted wirelessly by mean of radio frequency. The data can be transmitting in several ranges depending on the frequency of radio frequency being used. There are many applications using RF such as object tracking, access control, remote control and so on. The development of wireless data transmission which I build can be use for such application for future.

1.2 Objective:

The main objectives of this project are to:

1. Build hardware design for development of wireless data transmission using microcontroller 8051 interface with LCD screen and keypad

2. Write an assembly language to program the system

1.3 Scope

These devise can operate over very long distances depending on the designation of radio frequency being used. For trial I decide to use ultra high frequency which has range frequency of 300MHz to 3GHz and able to transmit signal about 1m to 100mm. Notes that the greater the frequency the smaller the distance.

This project consists of two parts, hardware and software. The hardware is microcontroller based interfacing with LCD and keypad while the software part will writing by using an assembly language.

1.4 Problem statement

As I mention earlier that one of the application of wireless data transmissions using radio frequency is object tracking. We need a device which can help us finding an item if we are in the habit of often misplacing small items around us. We need the device that saves our precious time to find the lost item. Development of wireless data transmission using which I develop can be used to solve this matter.

I believe that this project will help and benefit to those people that have multiple items in their home that tend to get lost on a regular basis. They will no longer have to spend time searching their household or other items that are used and misplaced regularly. This device will end the frustration of having to search one's home repeatedly for lost items.

CHAPTER 2

LITERATURE REVIEWS

This chapter describe about the primary and the secondary source which I refer in order to complete this project. I have found in the internet sources the same project which is designed by Steve Yessa from Bradley University College of Engineering and Technology, Department of Electrical and Computer Engineering. It be my main source since his project consist of microcontroller,keypad, LCD and Radio Frequency. Actually this project is not going to solve the problem, but more on a study about the microcontroller and how it work, also how to interface it with some other device such as keypad and LCD display and finally study about the application of the radio frequency in daily life. In his final report, he did not describe more on keypad and LCD interface, so to get the information I have to refer to the several reference books.

2.1 Microcontroller

Microcontroller is a general purpose device, but one that is meant to read data, performs limited calculations on that data, and control its environment based on those calculations. The prime use of a microcontroller is to control the operation of a system using a fixed program that is stored in ROM and that does not change over the lifetime of the system. The detail explanation about microcontroller will be described in the next chapter.

2.2 Keypad Interface

Interfaces to keypads are common for microcontroller-based design. Keypad input is an economical choice for a user interface and often adequate for complex applications. The detail explanation will be described in the next chapter.

2.3 LCD display Interface

LCD can be add in any application in term of providing a useful interface for the user, debugging an application or just giving it a professional look. Using this interface is often not attempted by inexperience of the designer because it is difficult to find good documentation on the interface, initializing the interface can be problem and the display themselves are expensive. Further information about LCD module described in next chapter.

2.4 Radio Frequency

Radio frequency is the best idea to be used to transmit data or signal my mean of wireless transmission. The signal can be transmit in different range depending on the frequency being used by the user. It is widely used in modern technology such as in object tracking, access control and so on.

CHAPTER 3

METHODOLOGY

3.1 Introduction

In Methodology topic, I describe about the method being used in order to finish this project as well as the component needed. These projects follow the step as listed below.

i. Project Identification
ii. System Planning
iii. System Analysis
iv. System Design
v. System Implementation
vi. Troubleshooting

3.2 Project Identification

Resources such as from a journal, reference book and internet are the first thing should be done in order to go further and completing this project. All the data and information regarding to this project can be easily get from the primary source. From the research state that wireless data transmission are widely used in modern technology.It can be aply in may area including object tracking,access control and so on.

As a human being,sometime we tend to lost an item such as key, remote tv and etc. As a solution for this matter, the lost item can be found easily by using RF tansmission . However, as I do mention earlier, finding object is just one of the application of RF transmission. It can be used in other application by mean of wireless transmission.

3.3 System Planning

The purpose of the planning phase is to identify clearly the scope of this project. It is also to detect the weakness and lack of the project development which is needed to troubleshoot. This phase is one of the important parts because it involve with time to develop both hardware and software. It is about how to manage the time efficiently. For that particular, Gantt chart is used to organize planning for overall process and activity that will followed, refer on appendices A.

3.4 System Analysis

The purpose of the system analysis phase is to understand the requirement and features of the project for both hardware and software design. Figure 3.4(a) show the four major steps to fulfill system analysis.

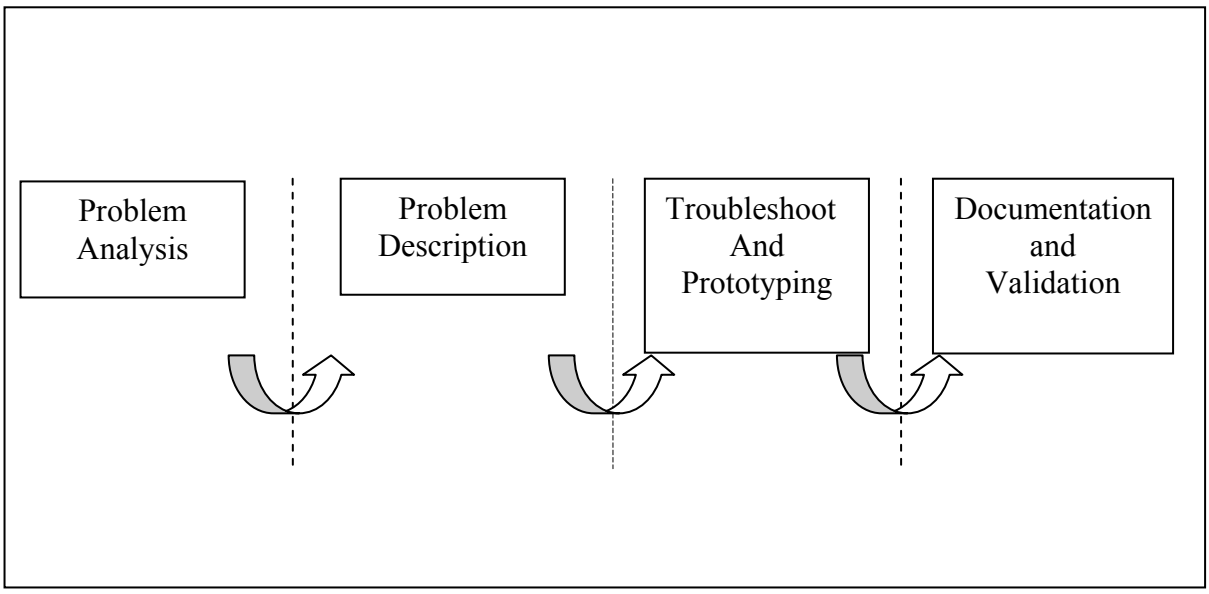

Figure 3.4: System Analysis Phase

3.4.1 Hardware Requirements

The hardware requirement on this project refers to the several of electronic components, devices and tools. There are electronic devices that it's recommended to use which is suitable. Electronic components requirements for the development of wireless data transmission are listed below:

i. Microcontroller
ii. Keypad
iii. LCD Display
iv. Buffer
v. Keypad Encoder
vi. Decoder
vii. Latch
viii. MAX233
ix. NAND gate
x. External RAM
xi. EPROM
xii. AND gate
xiii. Resistor

xiv. Capacitor
xv. Light Emitting Diode (LED)
xvi. Tact Switch

The detail explanation about each component and tools will be discuss in Session 3.8

3.4.2 Software requirement

The software requirement of the application actually refers to the software that could be used to access the application and run it smoothly. For this project I use an assembly language.

Assembly Language is a low level language which is used to program microcontroller based system so that it can function according to the user's desire. Generally, a microcontroller system executes instruction in the form of machine codes which is represented by logic 1 and 0. However, it is difficult to program it based on the machine codes since it is complicated and takes a long time. So, assembly language is the solution to solve this problem. Each program in an assembly language will be translated automatically to machine codes by software named 'assembler'. Furthermore the structure of an assembly language is very simple

i. Creating Source Code

Type the program using NOTEPAD text editor. The program should be named as follows: filename.ASM. This is to enable the Assembler to recognize the program as source file or source code. After the program is written, it must be translated to machine codes in the binary form 1 and 0.Figure 3.4.2(a) below show an example of source code file.

```
        $MOD51
        ORG     8000H
        MOV     P1,#0
AGAIN:  MOV     DPTR,#TABLE
NEXT:   CLR     A
        MOVC    A,@A+DPTR
        JZ      AGAIN
        MOV     P1,A
        INC     DPTR
DELAY:  MOV     R2,#8
INLP1:  MOV     R1,#255
INLP2:  MOV     R0,#255
INLP3:  DJNZ    R0,INLP3
        DJNZ    R1,INLP2
        DJNZ    R2,INLP1
        SJMP    NEXT
TABLE:
        DB      86H,88H,0C0H,0A4H,0C0H,82H,99H

        END
```

Figure 3.4.2 (a) Example of source code file

ii. Assemble the source code

Save the program when it is complete and exit from NOTEPAD text editor to DOS command. The following command being used to assemble the program into machine codes.

D:\PSM> asm51 filename.ASM -L filename.LST -H filename.HEX

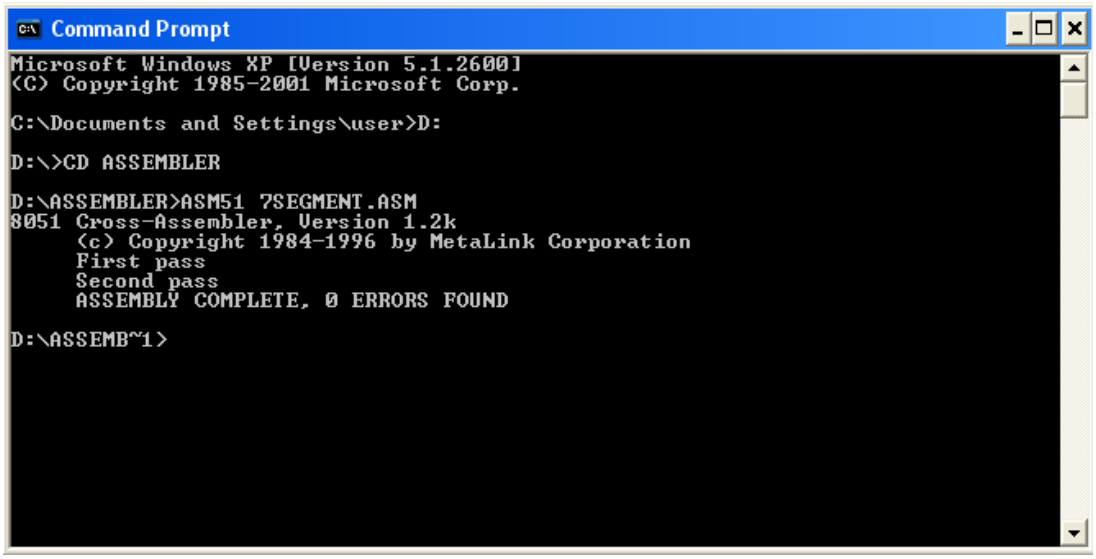

Figure 3.4.2 (b) Assembler

By executing the above command, another two files was created:

- Listing File ie. filename.lst
- Hex File ie. filename.hex

If there is any error in the program, it is easy to check the error inside the Listing File and then modify the error in the source file. From the contents of the Listing File, at the left field of the file shows the address and machine codes (opcode and operand) for each line of the instruction which has been translated by X-ASM. The Hex File contains machine codes information in ASCII format.

```
                        1
                        2     ;testing program seven segment display
                        3     ;tarikh : 8 march 2006
                        4     ;name : zaleha salleh
                        5
                        6
                        7     ;########################################
                        8
                        9
                       10             $MOD51
8000                   11             ORG     8000H
8000 759000            12     PLTEST: MOV     P1,#0
8003 90801B            13     AGAIN:  MOV     DPTR,#TABLE
8006 E4                14     NEXT:   CLR     A
8007 93                15             MOVC    A,@A+DPTR
8008 60F9              16             JZ      AGAIN
800A F590              17             MOV     P1,A
800C A3                18             INC     DPTR
800D 7A08              19     DELAY:  MOV     R2,#8
800F 79FF              20     INLP1:  MOV     R1,#255
8011 78FF              21     INLP2:  MOV     R0,#255
8013 D8FE              22     INLP3:  DJNZ    R0,INLP3
8015 D9FA              23             DJNZ    R1,INLP2
8017 DAF6              24             DJNZ    R2,INLP1
8019 80EB              25             SJMP    NEXT
801B                   26     TABLE:
801B 8688C0A4          27             DB      86H,88H,0C0H,0A4H,0C0H,82H,99H
801F C08299
                       28
                       29             END

VERSION 1.2k ASSEMBLY COMPLETE, 0 ERRORS FOUND
07SEGMENT

AGAIN. . . . . .  C ADDR  8003H
DELAY. . . . . .  C ADDR  800DH  NOT USED
INLP1. . . . . .  C ADDR  800FH
INLP2. . . . . .  C ADDR  8011H
INLP3. . . . . .  C ADDR  8013H
NEXT . . . . . .  C ADDR  8006H
P1 . . . . . .  D ADDR  0090H  PREDEFINED
PLTEST . . . . . .  C ADDR  8000H  NOT USED
TABLE. . . . . .  C ADDR  801BH
```

Figure 3.4.2 (c) Example of LST File

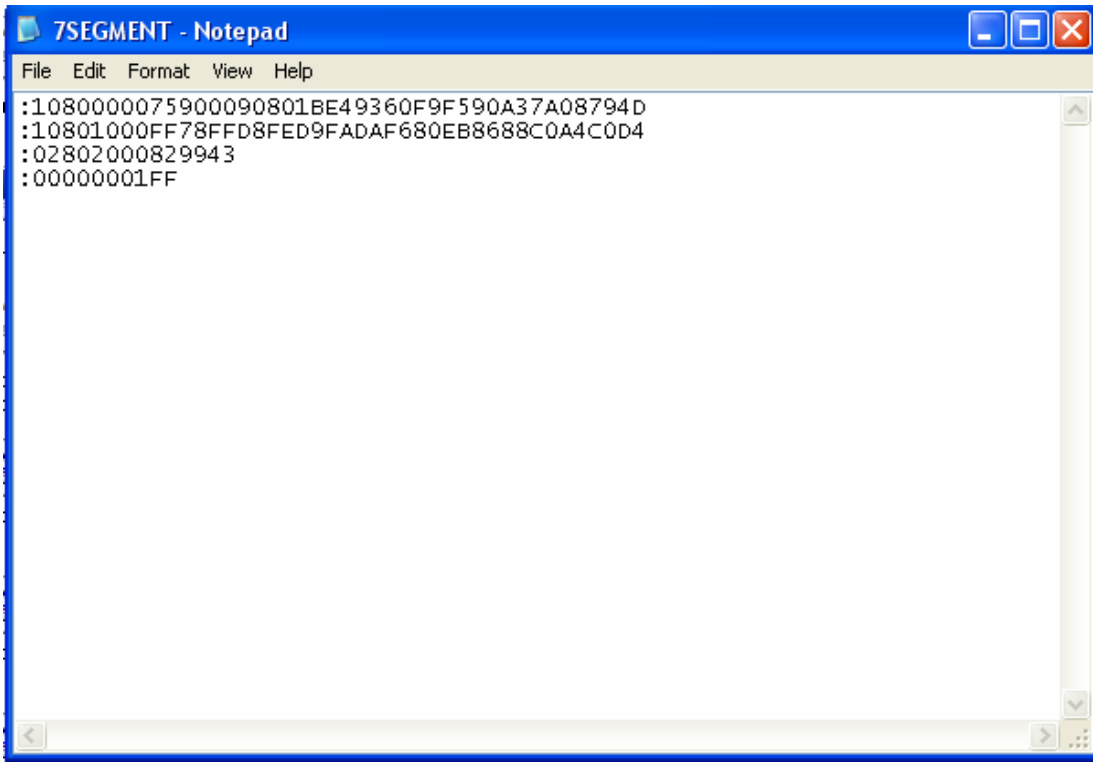

Figure 3.4.2(d) Example of HEX files (machine code)

iii. Burn the program into the external system memory (EPROM).

The last step is to save all the code from hex file into the system memory (EPROM). This can be done by using the EPROM programmer. The term EPROM stand for Erasable Programmable Read Only Memory. Erasable means that the chip can be erased and reused. An EPROM is erased in a device called an EPROM eraser. The eraser is a high intensity ultraviolet light source in a box. Programmable means that the EPROM can be programmed with a program, data or both. Read Only Memory means that the computer which is connected to the EPROM can only get information from the chip. In short, the EPROM is a memory part which will not forget its program or data when power is removed. It must be programmed by a special programming product called an EPROM or DEVICE programmer as mention earlier.

3.5 Design Phase

The purpose of system design is to develop a based unit of remote finder object that can be attach to the remote unit for further expand. During this phase, I will identify all the necessary input, output, interfaces as well as the process

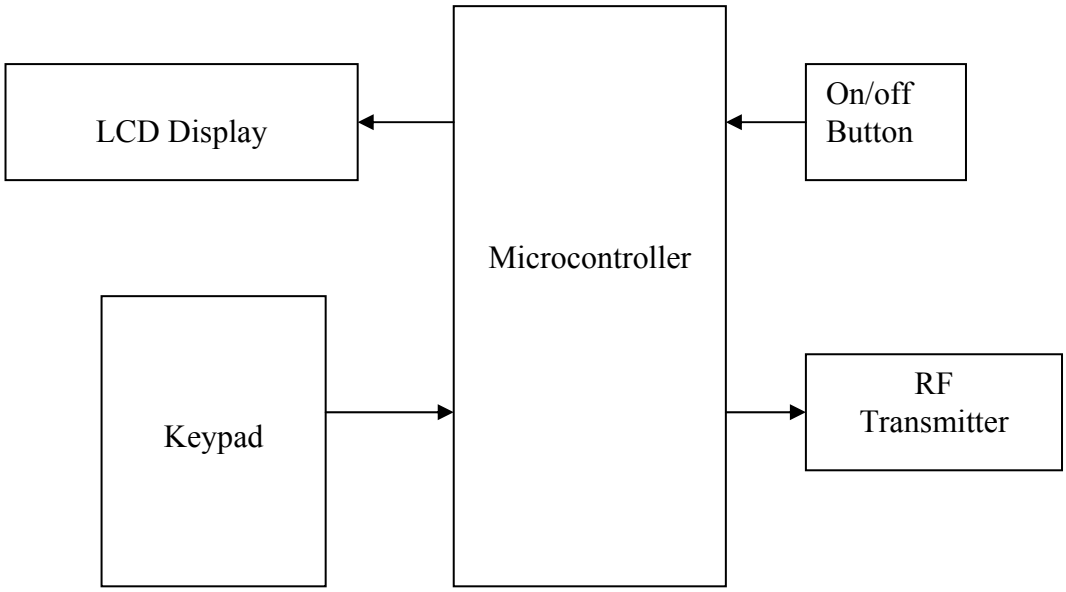

Figure 3.5 System Block Diagram

The base system was microcontroller based, utilizing a LCD and a keypad. The base unit is controlled by a user input from the keypad and output serial bit through a RF transmitter as shown in figure 3.5

3.6 System Implementation

The implementation phase of software development is the process of transforming a system specification into a functional hardware. During the implementation phase, the various element modules which are covering all elements in the based unit of remote finder object are coded. There will be a session of combining the module and determining the whole system function correctly. In this

situation, it might be any several of constraint and risk that need to be troubleshoot and cover continuously.

3.7 Troubleshooting

Hardware is the most critical part to troubleshoot, as it require knowledge, patience and effort to solve. Every error need to go through investigation to tackle in order to avoid unnecessary faulty to other component. The debugging is meant troubleshooting on the overall system which is the need of troubleshooting include wiring connection on the hardware, electronic circuit designed and software program.

3.8 Electronic Component

Now days, the production of the electronic components uses the modern and sophisticated technology. Using this technology we can produce components that are more complex, small and sizeable. This use of component enables the smaller equipment to be produced and can raise the equipment capability.

3.8.1 Microcontroller

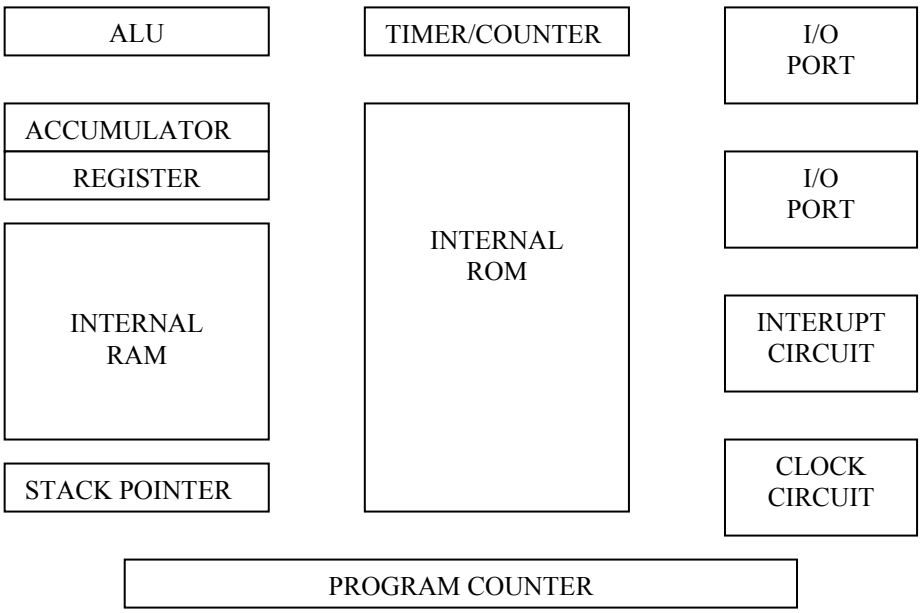

Figure 3.8.1 A Block Diagram of a Microcontroller

Figure above shows the block diagram of a typical microcontroller, which is a true computer on chip. The design incorporates all of the features found in the microprocessor CPU: ALU, PC, SP, and register. It is also has added the other features needed to make a complete computer which are ROM, RAM, parallel I/O, serial I/O, counter, and a clock circuit.

Like the microprocessor, a microcontroller is a general purpose device, but one that is meant to read data, performs limited calculations on that data, and control its environment based on those calculations. The prime use of a microcontroller is to control the operation of a system using a fixed program that is stored in ROM and that does not change over the lifetime of the system.

The design approach of the microcontroller mirrors that of the microprocessor: make a single design that can be used in as many applications as possible. The microprocessor design accomplishes this goal by having a very flexible and extensive repertoire of multi-byte instructions. This instruction work in hardware configuration that enable large amounts of memory and I/O to be connected to address and data bus pins on the integrated circuit package. Much of the activity in the microprocessor has to do with moving code and data to and from external

memory to the CPU. The architecture features working register that can be programmed to take part in the memory access process, and the instruction set is aimed at expediting this activity in order to improve throughput. The pins that connected the microprocessor to external memory are unique, each having a single function. Data is handled in word, double-word, or larger sizes.

The microcontroller design uses a much more limited set of instructions that are used to move code and data from internal memory to the ALU. Many instructions are coupled with pins on the integrated circuit package; the pins are “programmable” means it is capable of having several different functions depending on the wishes of the programmer.

The microcontroller is concerned with getting data from and to its own pins; the architecture and instruction set are optimized to handle data in bit, byte, and word size.

As a conclusion, the microprocessor is concerned with rapid movement of code and data from external addresses to the chip while a microcontroller is concerned with rapid movement of bits within the chip. The microcontroller can function as a computer with the addition of no external digital parts but the microprocessor must have many additional parts to be operational.

3.8.2 The 8051 Microcontroller

The 8051 is an 8 bit microcontroller originally developed by Intel in 1980. It has become the industry standard for embedded control. Intel offers a wide variety of 8051 versions with different configurations of on-board EPROM/ROM. The 8051 architecture consists these specific features:

- 8-bit CPU with register A (the accumulator) and B
- 16-bit program counter (PC) and data pointer (DPTR)
- 8-bit program status work (PSW)
- 8-bit stack pointer

- 4K Internal ROM
- Internal RAM of 128 byte
    - 4 register bank, each containing 8 registers
    - 16 bytes, which may be addressable at the bit level
    - 8 bytes of general purpose data memory
- 32 I/O pins arranged as four 8-bit port: P0 – P3
- Two 16-bit timer/counter: T0 and T1
- Full duplex serial data receiver/transmitter
- Control register
- Two external and three internal interrupt sources
- Oscillator and clock circuit.

One strong point of the 8051 is the way it handles interrupts. Vectoring to fixed 8-byte areas is convenient and efficient. Most interrupt routines are very short (or at least they should be), and generally can fit into the 8-byte area.

The 8051 instruction set is optimized for the one-bit operations so often desired in real- world, real-time control applications. The Boolean processor provides direct support for bit manipulation. This leads to more efficient programs that need to deal with binary input and output conditions inherent in digital-control problems. Bit addressing can be used for test pin monitoring or program control lags.

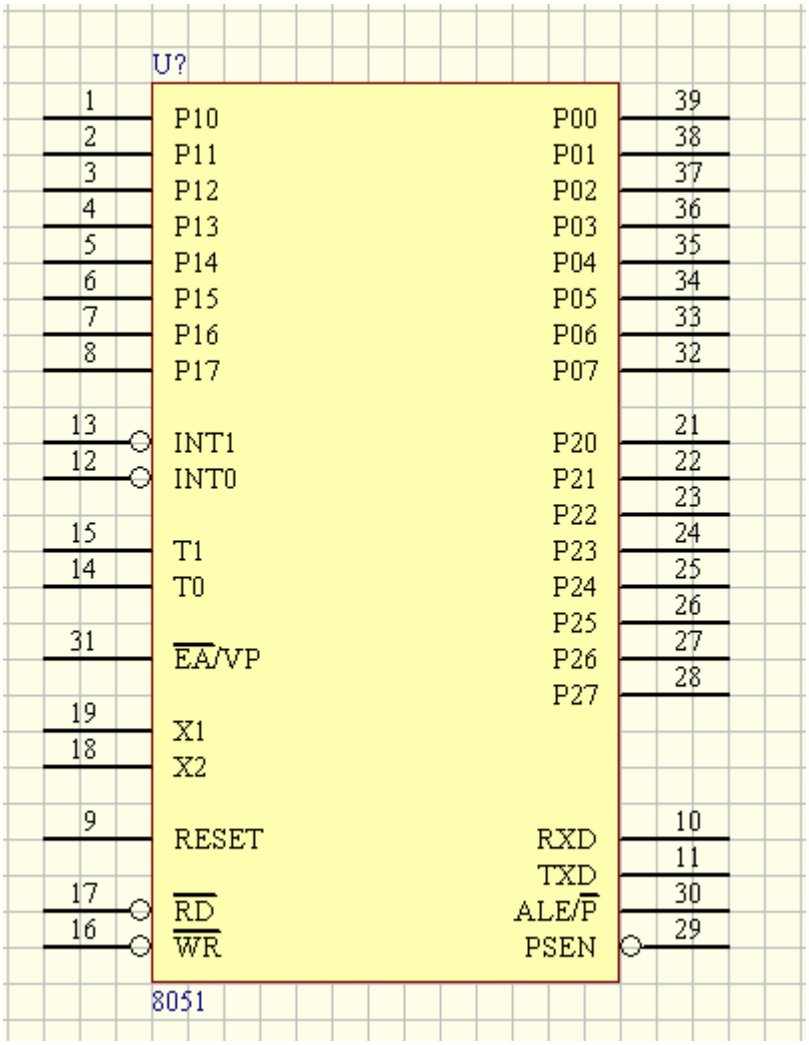

Figure 3.8.2 (a) 8051 Microcontroller Pin

3.8.2.1 Pin assignment:

This section introduces the 8051 hardware architecture from an external perspective. As shown in figure below, 32 of the 8051's 40 pins function as I/O port lines. However, 24 of these lines are duel-purpose which can operate as I/O or as a control line or part of the address or data bus.

3.8.2.1.1 Port 0

Port 0 is duel-purpose port on pins 32-39. In minimum component designs, it is used as a general purpose I/O port. However, for large designs with external memory, it becomes a multiplexed address and data bus.

3.8.2.1.2 Port 1

Port 1 is dedicated I/O port on pin1-8 which designated as P1.0, P1.1, P1.2, etc are available for interfacing to external devices as required. No alternate function are assign for Port 1 pins, thus it is used solely for interfacing to external devices.

3.8.2.1.3 Port 2

Port 2 is also a duel-purpose port on pins 21-28 as a general purpose I/O, pr as the high byte of the address bus for designs with external code memory or more than 256 bytes of external data memory.

3.8.2.1.4 Port 3

Port 3 is a duel-purpose port on pins 10-17. As well as general purpose I/O, these pins are multifunctional, with each having an alternate purpose related to special features of the 8051. The alternate feature of port 3 pins is summarized as table 3.8.2.

BIT	NAME	ALTERNATE FUNCTION
P3.0	RXD	Receive data for serial port
P3.1	TXD	Transmit data for serial port
P3.2	INT0*	External interrupt 0
P3.3	INT1*	External interrupt 1
P3.4	T0	Timer/Counter 0 external input
P3.5	T1	Timer/Counter 1 external input
P3.6	WR*	External data memory write strobe
P3.7	RD*	External data memory read strobe

Table 3.8.2 The alternate feature of port 3 pins

3.8.2.1.5 PSEN* (Program Strobe Enable)

The 8051 microcontroller has four dedicated bus control signals. Program Store Enable (PSEN*) is an output signal on pin 29. It is a control signal that enables external program (code) memory. It usually connects to an EPROM's (Erasable Programmable Read Only Memory) Output Enable (OE*) pin to permit reading of program bytes.

The PSEN* signal pulses low during the fetch stage of an instruction, which is stored in external program memory. The binary code of a program (opcodes) are read from EPROM, travel across the data bus, and are latched into the 8051's instruction register for decoding. When executing a program from internal ROM, PSEN* remains in the inactive (high) state.

3.8.2.1.6 ALE (Address Latch Enable)

The ALE output signal on pin 30. It is used for demultiplexing the address and data bus. When port 0 is used in its alternate mode (as data bus and the low byte of address bus), ALE is the signal that latches the address into an external register during the first half of a memory cycle. This done, the port 0 lines are then available

for data input or output during the second half of the memory cycle, when the data transfer takes place.

ALE signal pulses at $1/6^{th}$ on-chip oscillator frequency and can be used as a general purpose clock for the rest of the system. If the 8051 is clocked from a 12MHz crystal, the ALE signal oscillates at 2MHz. This pin also used for the programming input pulse for EPROM version of the 8051.

3.8.2.1.7 EA* (External Access)

The EA* input signal on pin 31 is generally tied high (+5V) or low (0V). If high, the 8051 executes program from internal ROM when executing in the lower 4K/8K of the memory. If low, program execute from external memory only (and PSEN* pulses low accordingly). If EA* is tied low on 8051, internal ROM is disable and programs execute from external EPROM.

3.8.2.1.8 RST (Reset)

The RST input on pin 9 is the master reset for 8051. When this signal is brought high for at least two machine cycles, the 8051 internal register are loaded with appropriate values for and orderly system start-up. For normal operation, RST is low.

3.8.2.1.9 On-Chip Oscillator Input

The heart of the 8051 is the circuitry that generates the clock pulses by which all internal operations are synchronized. Pins XTAL 1 and XTAL2 on pin 19 and 18 are provided for connecting a resonant network to perform and oscillator. Typically a quartz crystal and capacitors are employed. The crystal frequency is the basic internal clock frequency of the microcontroller. The nominal crystal frequency is 12MHz.

3.8.2.1.10 Power connection

The 8051 operates from a single +5V supply. The Vcc connection is on pin 40, and the Vss (ground) connection is on pin 20.

3.8.2.2 A and B CPU register

The 8051 contains 34 general-purpose register. Two of these, register A and B, holds results of many instruction, particularly math and logical operation of the 8051 central processing unit (CPU). The other 32 are arranged as part of internal RAM in four banks, B0 – B3 of eight register and comprise the mathematical core.

The A (accumulator) register is the most versatile of the two CPU registers and is used for many operations, including addition, subtraction, integer multiplication and division and Boolean bit manipulation. The A register is also used for all data transfer between the 8051 and any external memory. The B register is used with A register for multiplication and division operation and has no other function than as a location where data may be stored.

3.8.2.3 Program counter (PC) and data pointer (DPTR)

The 8051 contains two 16-bit register well known as program counter (PC) and data pointer (DPTR). Each is used to hold the address of a byte in memory.

Program instruction bytes are fetched from locations in memory that are addressed by PC. Program ROM may be on chip at addresses 0000H to 0FFFH, external to the chip for addresses that exceed 0FFFH, or totally external for all addresses from 0000H to FFFFH. The PC is automatically incremented after every instruction byte is fetched and may also be altered by certain instructions. The PC is the only register that does not have an internal address.

The DPTR register is made up of two 8-bit register named DPH and DPL, which are used to furnish memory address for internal and external code access and

external data access. The DPTR in under the control of program instruction and can be specified by its 16-bits name, DPTR, or by each individual byte name, DPH and DPL. DPTR does not have a single internal address; DPH and DPL are each assigned an address.

3.8.2.4 The Stack and the Stack Pointer

The term stack refers to an area of internal RAM that is used in conjunction with certain opcodes to store and retrieve data quickly. The 8-bit Stack Pointer (SP) register is used bt the 8051 to hold an internal RAM address that is called the top of the stack. The address held in the SP register is the location in internal RAM where the last byte of data was stored by the stack operation.

When data is to be placed on the stack, the SP increments before storing data on the stack so that the stack grows up as data stored. As data is retrieved from the stack, the byte is read from the stack, and then the SP decrements to point to the next available byte of stored data.

The stack is limited in height to the size of the internal RAM. The stack has the potential to overwrite valuable data in the register bank, bit addressable RAM, and scratch-PAD RAM areas. The stack is normally placed in the SP register, to avoid conflict with the register, bit, and scratch-pad internal RAM areas.

3.8.2.5 Internal RAM

The 128-byte internal RAM, which is shown generally in figure 3.8.2 (b) is organized into three distinct areas:

i. 32-byte from address 00H to 1FH that make up 32 working registers organized as four banks of eight registers each. The four register banks are numbered 0 to 3 and are made up of eight registers named R0 to R7. Each register can be addresses by name or by its RAM address. Register banks not selected can be used as general-purpose RAM. Bank 0 is selected on reset.

ii. A bit-addressable area of 16 bytes occupies RAM byte addresses 20H to 2F, forming a total of 128 addressable bits. An addressable bit may be specified by its bit address of 00H to 7FH, or 8 bits may form any byte address from 20H to 2FH. Addressable bit are useful when the program need only remember a binary event (switch on, light off, etc)

iii. A general purpose RAM area above the bit area, from 30H to 7FH, addressable able as bytes.

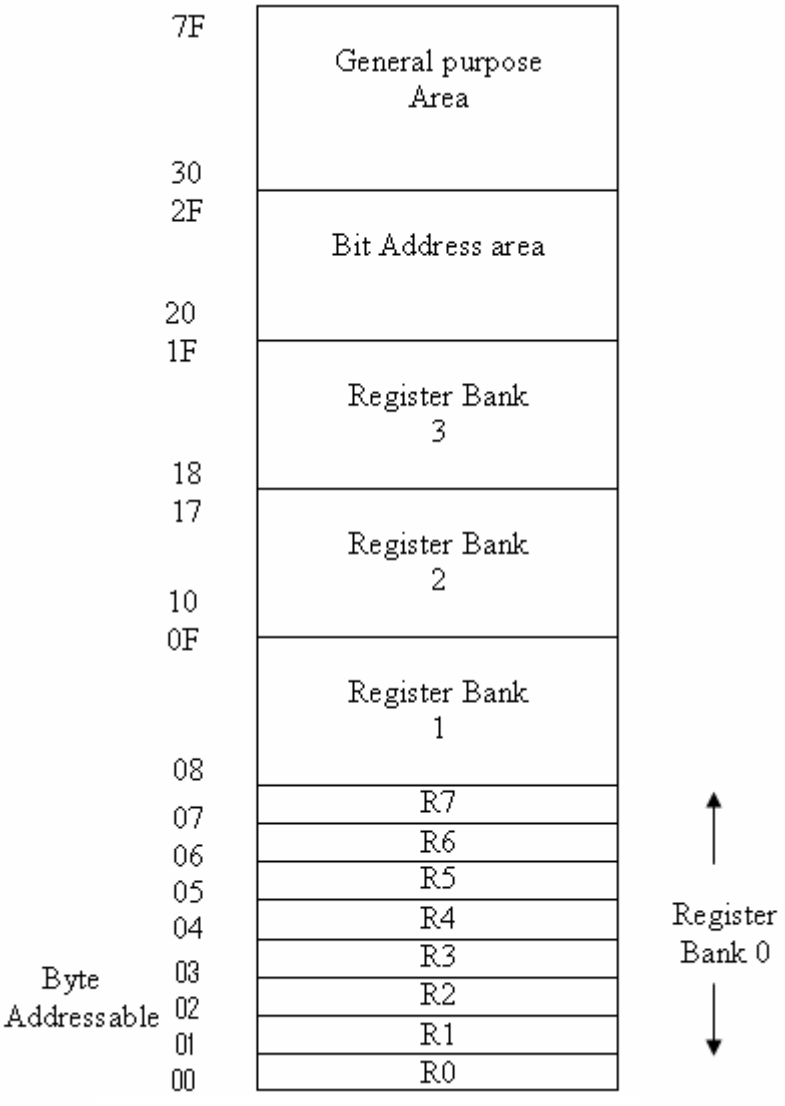

Figure 3.8.2 (b) Internal RAM

3.8.3 Keypad

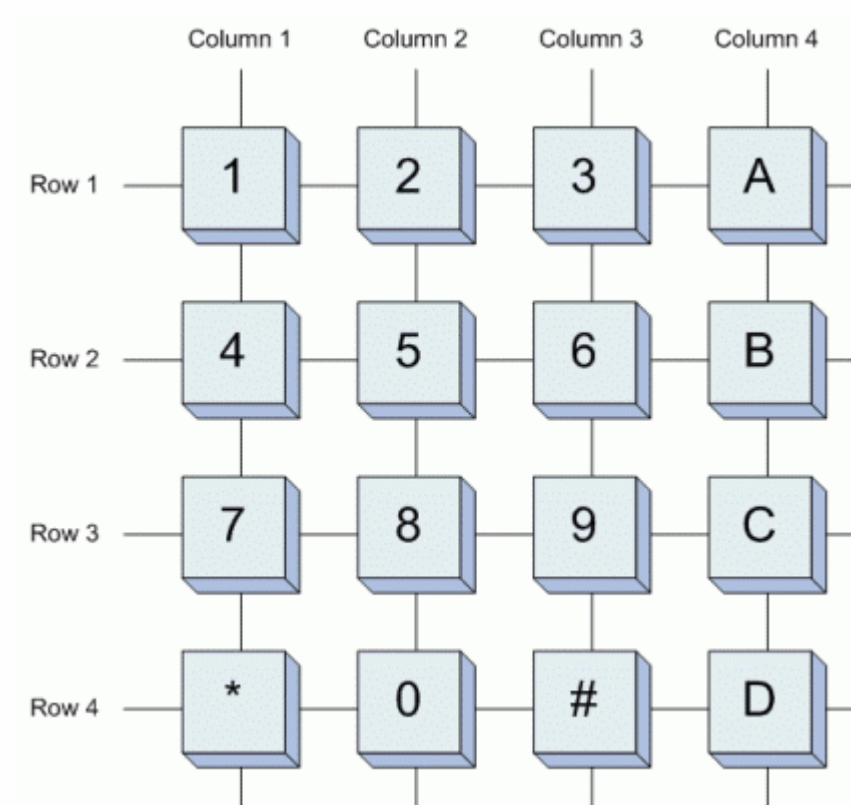

Figure 3.8.3(a) Keypad Configuration

Interfaces to keypads are common for microcontroller-based design. Keypad input is an economical choice for a user interface and often adequate for complex applications. There are various type of keypad such as 12 keys and 16 keys and a common type is matrix type. However, for this project I choose keypad with 16 keys which is use to enter the names of the items, select the item and store the ID number of the locators. The keypad contains 16 keys arranged in four rows and four columns. Each key has a momentary contact switch that is connected to an intersection of row and column wires. When a key is release (break), an open circuit exists between all wires/terminal. When a key is pressed, the contact closure connects the row and column wire. Thus, a short circuit exists between row and column wires when any key is pressed. To determine which key is pressed, a microcontroller must scan the rows and columns to identify the row and column intersection of the short circuit.

These keypad connected to it keypad encoder (74c922) and buffer (74HC244) before it is connected to the microcontroller as shown in figure 3.8.3 (b) .Table 3.8.3 below show the intersection of row and column for each key.

	COLUMN				ROW			
KEY	**C1**	**C2**	**C3**	**C4**	**R1**	**R2**	**R3**	**R4**
0	0	1	0	0	0	0	0	1
1	1	0	0	0	1	0	0	0
2	0	1	0	0	1	0	0	0
3	0	0	1	0	1	0	0	0
4	1	0	0	0	0	1	0	0
5	0	1	0	0	0	1	0	0
6	0	0	1	0	0	1	0	0
7	1	0	0	0	0	0	1	0
8	0	1	0	0	0	0	1	0
9	0	0	1	0	0	0	1	0
A	0	0	0	1	1	0	0	0
B	0	0	0	1	0	1	0	0
C	0	0	0	1	0	0	1	0
D	0	0	0	1	0	0	0	1
*	1	0	0	0	0	0	0	1
#	0	0	1	0	0	0	0	1

Table 3.8.3 Intersection of row and column

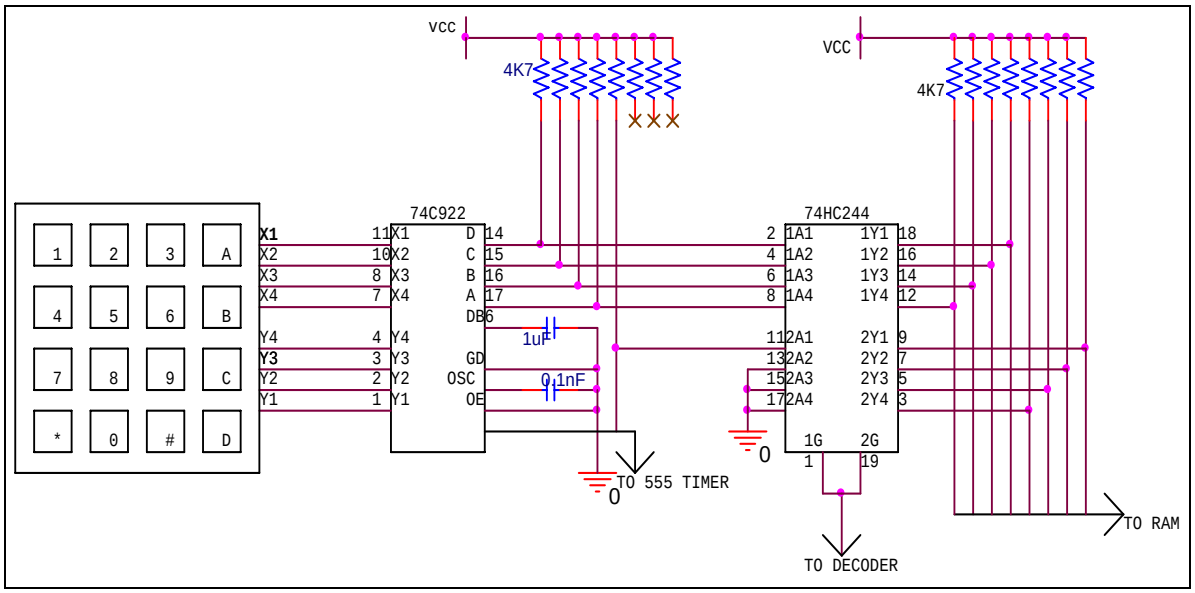

Figure 3.8.3 (b) Schematic circuit for keypad

3.8.4 LCD Display

LCD is stand for Liquid Crystal Display. It is used in term of providing an useful interface for user, debugging an application or just giving it a professional look. We can found an application of LCD such as in calculator.

An LCD is made with either a passive matrix or an active matrix display display grid. The active matrix LCD is also known as a thin film transistor (TFT) display. The passive matrix LCD has a grid of conductors with pixels located at each intersection in the grid. A current is sent across two conductors on the grid to control the light for any pixel. An active matrix has a transistor located at each pixel intersection, requiring less current to control the luminance of a pixel. For this reason, the current in an active matrix display can be switched on and off more frequently, improving the screen refresh
Some passive matrix LCD's have dual scanning, meaning that they scan the grid twice with current in the same time that it took for one scan in the original technology. However, active matrix is still a superior technolog

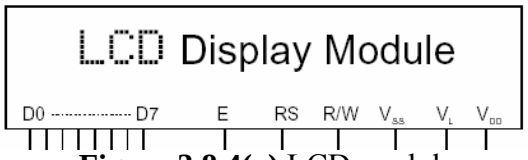

Figure 3.8.4(a) LCD module

3.8.4.1 Pin Assignment

The pin assignment shown below is an industry standard for small alphanumeric LCD - modules.

Pin number	Symbol	I/O	Function
1	Vss	-	Power supply (GND)
2	Vcc	-	Power supply (+5V)
3	Vee	-	Contrast adjust
4	RS	I	0 = Command input/output 1 = Data input/output
5	R/W	I	0 = Write to LCD module 1 = Read from LCD module
6	E	I	Enable signal (Data strobe)
7	D0	I/O	Data bus line 0 (LSB)
8	D1	I/O	Data bus line 1
9	D2	I/O	Data bus line 2
10	D3	I/O	Data bus line 3
11	D4	I/O	Data bus line 4
12	D5	I/O	Data bus line 5
13	D6	I/O	Data bus line 6
14	D7	I/O	Data bus line 7 (MSB)

The LCD module requires 3 control lines and either 4 or 8 I/O lines for the data bus. The user may select whether the LCD is to operate with a 4-bit data bus or an 8-bit data bus. If a 4-bit data bus is used, the LCD will require a total of 7 data lines (3 control lines plus the 4 lines for the data bus). If an 8-bit data bus is used, the LCD will require a total of 11 data lines (3 control lines plus the 8 lines for the data bus). The three control lines are referred to as E, RS, and R/W.

The E line is called "Enable." This control line is used to tell the LCD that we are sending it data. To send data to the LCD, the program should first set this line high (1) and then set the other two control lines (RS & RW) and put data on the data bus (DB0-DB8). When the other lines are completely ready, bring E low (0) again. The 1→ 0 transition tells the LCD to take the data currently found on the other control lines and on the data bus and to treat it as a command.

The RS line is the "Register Select" line. When RS is low (0), the data is to be treated as a command or special instruction (such as clear screen, position cursor, etc.). When RS is high (1), the data being sent is text data which should be displayed on the LCD screen. For example, to display the letter "T" on the screen you would set RS high.

The RW line is the "Read/Write" control line. When RW is low (0), the information on the data bus is being written to the LCD. When RW is high (1), the program is effectively querying (or reading) the LCD.

Finally, the data bus consists of 4 or 8 lines (depending on the mode of operation selected by the user). In the case of an 8-bit data bus, the lines are referred to as D0, D1, D2, D3, D4, D5, D6, and D7.

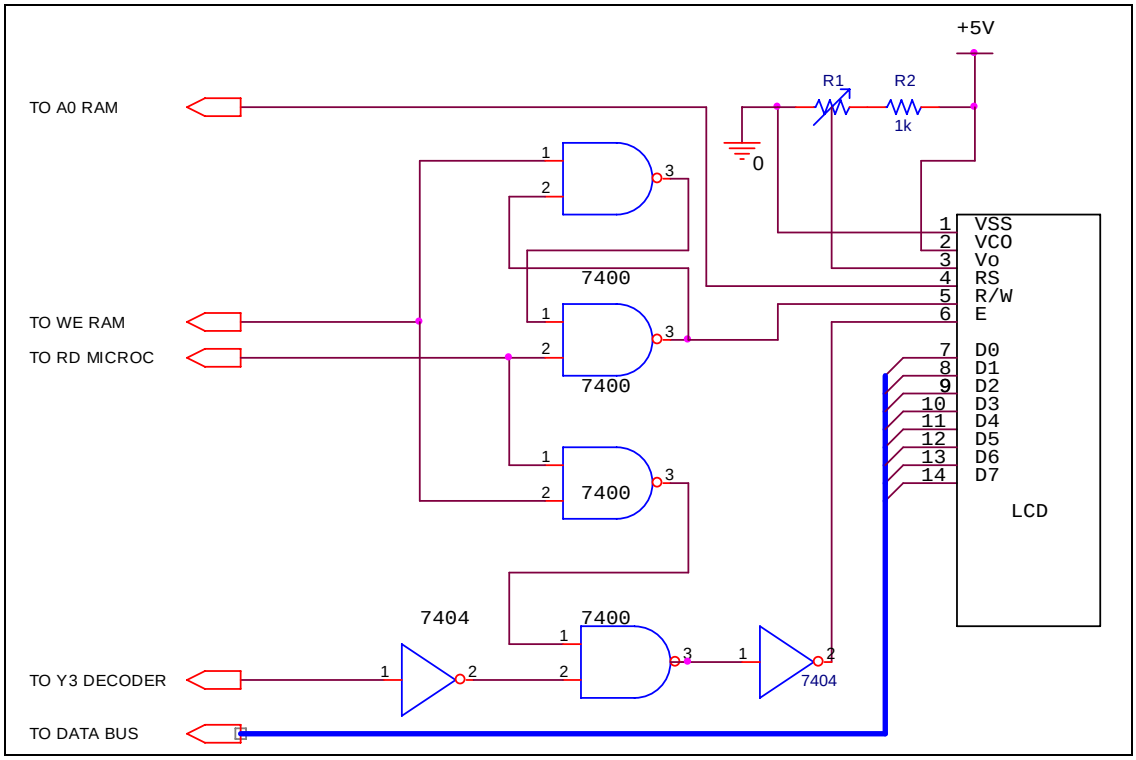

Figure 3.8.4 (b) Schematic Circuit for LCD Display

3.8.5 Resistor

Figure 3.8.5 (a) Resistor

Resistor is used to restrict the flow of current and measured in ohms (Ω) They are composed of graphite mixed with clay and either painted or covered with an insulating coating of ceramic. The resistance value may be obtained from the colour code marking on the body.

Colour	No 1	No 2	No 3	No 4
Black	0	0	10^0	0
Brown	1	1	10^1	± 1 %
Red	2	2	10^2	± 2 %
Orange	3	3	10^3	
Yellow	4	4	10^4	
Green	5	5	10^5	
Blue	6	6	10^6	
Violet	7	7	10^7	
Grey	8	8	10^8	
White	9	9	10^9	
Gold				± 5 %
Silver				± 10 %
None				± 20 %

Table 3.8.5(a) Colour Code for carbon film

Colour	No 1	No 2	No 3	No 4
Black	0	0	10^0	0
Brown	1	1	10^1	± 1 %
Red	2	2	10^2	± 2 %
Orange	3	3	10^3	
Yellow	4	4	10^4	
Green	5	5	10^5	
Blue	6	6	10^6	
Violet	7	7	10^7	
Grey	8	8	10^8	
White	9	9	10^9	
Gold				± 5 %
Silver				± 10 %
None				± 20 %

Table 3.8.5(b) Colour Code for Metal Oxide

Colour	No 1	No 2	No 3	No 4	No 5
Black	0	0	0	10^0	
Brown	1	1	1	10^1	± 1 %
Red	2	2	2	10^2	± 2 %
Orange	3	3	3	10^3	
Yellow	4	4	4	10^4	
Green	5	5	5	10^5	± 0.5 %
Blue	6	6	6	10^6	± 0.25 %
Violet	7	7	7	10^7	± 0.1 %
Grey	8	8	8	10^8	
White	9	9	9	10^9	
Gold					± 5 %
Silver					
None					

Table 3.8.5(c) Colour Code for Metal Film

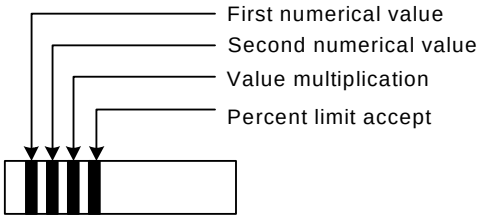

Figure 3.8.5 (b) Configuration

3.8.6 Capacitor

Capacitor acts as storage for electrical charge, not allowing the direct current but the alternating current to pass through. The charge stored is called capacitance. There are many types and varies shapes of capacitor which are made from materials like paper, oil, ceramic, Mylar, electrolic, styrol and tantalum. The unit of capacitance is measured in farad (F). The range voltage of every capacitor is written on its body and the capacitor will damage if the voltage source exceed this limit.

The capacitors consist of 2 metal electrodes with positive and negative polarity. There are 3 non-polarized capacitors, i.e. the paper, ceramic and mica capacitors. The polarity of the terminals of these type capacitors are not fixed and thus they may be connected to the circuit without observing the correct polarity.

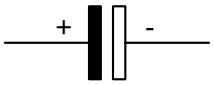

Figure 3.8.6 (a) Symbol of a polarized capacitor

:-

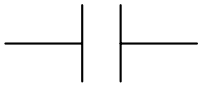

Figure 3.8.6 (b) Symbol of a non-polarized capacitor

3.8.7 Light emitting diode (LED)

Figure 3.8.7 Light Emitting Diode (LED)

LED are frequently used in electronic equipment to show the presence of current. It allows only a one-way flow of current. Usually there are three colours of LED lights, red, yellow and green. We can test LED like the regular diode. The advantages of LED are small in size and consume only a small amount of electricity and long lasting as there aren't any filaments. The anode (positive) is longer and the cathode (negative) is shorter. LED can be damaged by heat when soldering, but the risk is small.

3.8.8 Tact switches

Figure 3.8.8 Tact switches

The tact switch function as a reset button which is used to send a pulse input

3.8.9 IC Base

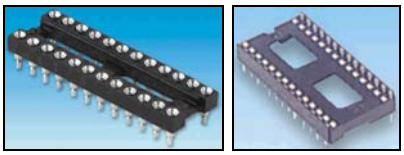

Figure 3.8.9 IC Base

They are used for holding IC in place and keep the IC from overheating.

3.8.10 On/Off Button

Figure 3.8.10 On/Off Button

They are used to on and off the circuit (system)

3.9 Tools

This section discusses on tools that being used in order to complete this project. Without these tools it is difficult to start the hardware design.

3.9.1 Long nose

Figure 3.9.1 Long nose pliers

They are used for:-

i. Holding, inserting or taking out small items in restricted space.

ii. Cutting electric wire.

iii. Shaping electronic component leads.

Parts of the pliers:-

Part	Function
Long nose	For reaching small items in restricted space other than holding and shaping.
Cutting edge	For cutting electric wire.

3.9.2 General Purpose Pliers (combination pliers)

Figure 3.9.2 General Purpose Pliers

They are used for holding or gripping, cutting, bending and shaping wire and component leads.

Parts of the pliers :-

Part	Function
Concave or curved surface	For holding or gripping rounded rod
Flat surface	For bending and shaping wire
Cutting edge	For cutting wire

3.9.3 Side Cutting Pliers (Cutter)

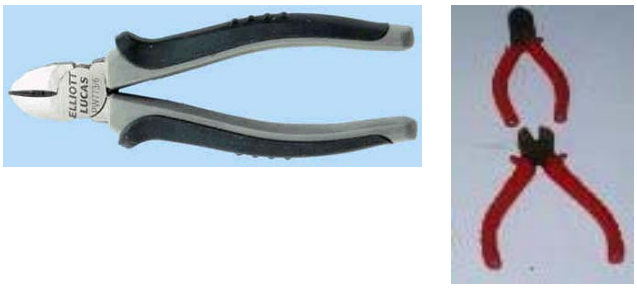

Figure 3.9.3 Side Cutting Pliers

They are used for:-

i. Cutting wires up to 16 gauges in size.

ii. Cutting and twining fine wires

3.9.4 Test Pens

Figure 3.9.4 Test Pen

They are used for :-

i. Detecting electrical leaks and live wire.

ii. Turning small screws (the end of the pens).

The neon in the pen will light up when the end of the pen comes into contact with a live wire or source of electric current. They are only used to detect between 50V to 500V

3.9.5 Soldering Iron and stand

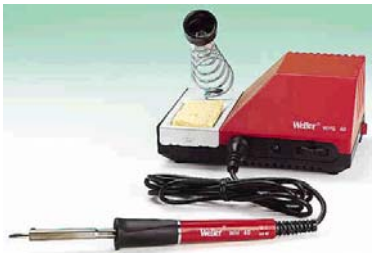

Figure 3.9.5 Soldering Irons and soldering iron stand

They are used to complete an electronic circuit by soldering the ends of the wire and leads. It also generates heat to melt the solder and transfer the melted solder to the desired targets.

Parts of the Iron :-

Part	Function
Supply wire	A cable that carries current to the heating elements
Handle	The part that one holds during soldering work
Heating elements	The part that heats the bit
Bit	The part that melts the solder during soldering

3.9.6 Soldering Core

Figure 3.9.6 Solder core

Is an alloy made which able to connect wiring or component leads in circuit boards. It will melt upon contact with the hot bit.

3.9.7 Digital Multimeter

Figure 3.9.7 Digital Multimeter

Digital multimeter is used to measure the most basic electrical quantities such as Voltage, current and resistance. In addition of measuring these quantities, many multimeter are capable of making a variety of more complex tests and measurements. The basic multimeter is a descendant of the volt-ohm-miliammmeter. (VOM).

3.10 Radio Frequency

RF technology is used in many different applications, such as television, radio, cellular phones, radar, and automatic identification systems. The term RFID (radio frequency identification) describes the use of radio frequency signals to provide automatic identification of items. RF is not only can be used for this project but it is widely used in many applications such as:

• Electronic toll collection (ETC)
• Railway car identification and tracking
• Intermodal container identification
• Asset identification and tracking
• Item management for retail, health care, and logistics applications
• Access control
• Animal identification
• Fuel dispensing loyalty pro g r a m s
• Automobile immobilizing (security)

Radio frequency (RF) refers to electromagnetic waves that have a wavelength suited for use in radio communication.Radio waves are classified by their frequencies, which are expressed in kilohertz, megahertz, or gigahert z .The RF spectrum is divided into several ranges or bands. With the exception of the lowest frequency segment, each band represent an increase of frequency corresponding to an order of magnitude (power of 10). The table below depicts the bands in the RF spectrum, showing frequency and bandwidth ranges.

Designation	**Abbreviation**	**Frequencies**	**Free-space wavelengths**
Very low frequency	VLF	9kHz – 30kHz	33km – 10km
Low frequency	LF	30kHz – 300kHz	10km – 1km
Medium frequency	MF	300kHz – 3MHz	1km – 100m
High frequency	HF	3MHz – 30MHz	100m – 10m
Ultra high frequency	UHF	300MHZ – 3GHz	1m – 100mm
Super high frequency	SHF	3GHz – 30GHz	100mm – 10mm

Table 3.10 Radio Frequency Ranges

Note that, increasing the frequency will cause the free space wavelength become smaller

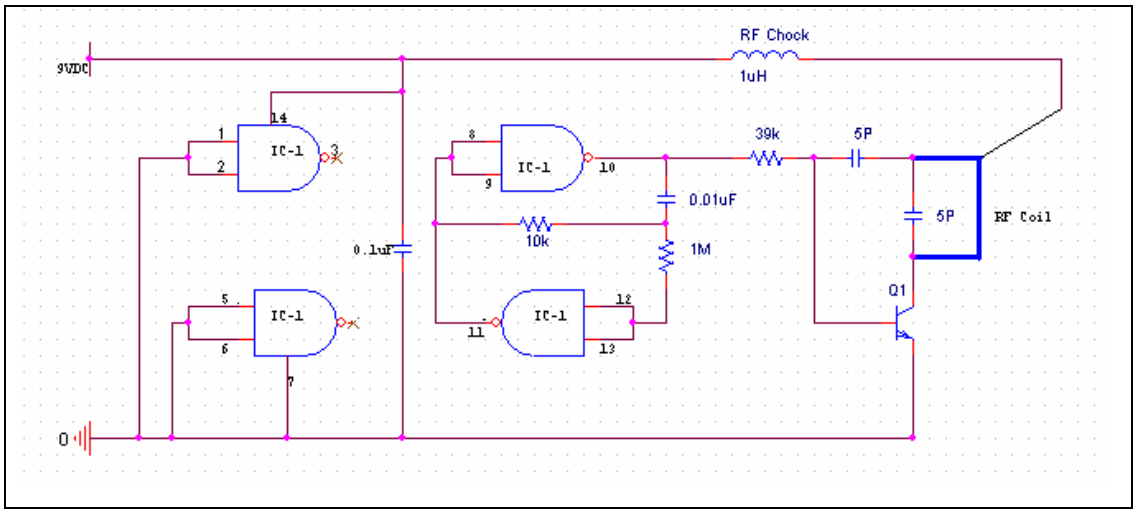

Figure 3.10 (a) Schematic circuit of Radio Frequency Transmitter

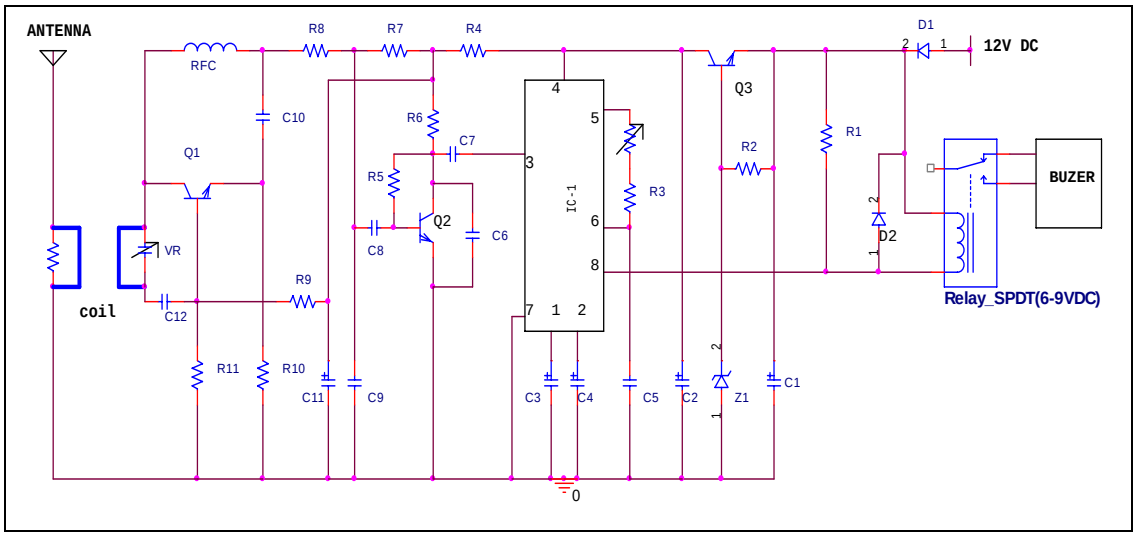

Figure 3.10 (b) Schematic circuits for Radio Frequency Receiver

CHAPTER 4

RESULT & DISCUSSION

This project competes with troubleshoot and testing each part that come out for result. All result can be seen by programming using assembly language.

4.1 Testing Hardware

Before the microcontroller interface to the keypad and LCD screen, I do test my Development board with a simple program by using seven segment display. The seven segment will display my matrix number which is EA02064. From this result, I can say that my development board is functionally and able to interface with other application which is keypad and LCD. The software writing to test the seven segment display is shown in the appendix B.

4.2 Keypad

The keypad is the first device that interfaces with user for this project. In order to test the functionality of the keypad, there is some adjustment of the programming for seven segment display. In other word, the seven segments displayed my matrix number

once one of any key is being pressed. Appendix C show the software writing of keypad and seven segment display.

4.3 LCD Display

LCD will display the name of the item to be locate according to the keypad key being pressed. However, in this project LCD not function properly, due to high sensitivity and easy to get blow. In order to display I finally decide to use a dot matrix.

4.4 Radio Frequency Transmitter and Receiver

Before connecting the RF to the microcontroller, it was tested my manual. The maximum range data can be transmit is about 3.5m. The step to test the RF transmitter and RF receiver describe as below

Tone frequency alignment:

a) The transmitter boards are placed close to the receiver board.
b) The PTT button was pressed and VR1 (variable resistor) was adjusted until LED lighted.
c) The PTT button the being pressed for a few times and the relay responded each time the button depressed cause the buzzer to function.

RF alignment:

a) The transmitter board are moved 30 – 50 cm away from the receiver board.
b) The PTT button on transmitter board is pressed and holds.
c) The trimmer cap VC (variable capacitor) then is adjusted slowly in either direction until the relay is actuated.
d) The range can be increased by moving the transmitter board until got the maximum range.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

After completing this project, I have learned more about both part hardware and software design. Furthermore, I'm now become familiar with the microcontroller and able to interface it with keypad and LCD display. I gain lot of lesson while doing this task, the first lesson is how to manage the time efficiently, secondly how to work under pressure and be more patient because it is not easy to work with an electronic component. I believe this project able to help for those who want to know about microcontroller and interface with keypad and LCD and Radio frequency. As a conclusion, these projects are not fully successful functions as determine in previous chapter

5.2 Recommendation

This is the simple project of applying radio frequency transmission with limited range. For future, recommendation we can expend the range by changing the frequency of the radio frequency. Beside that, we may not only transmit the signal but also the data so that data being transmit can be read in the receiver path and it might require complex software to run the system

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APPENDICES

APPENDIX A

		December				January				Febuary				March				April			
NO	**ACTIVITIES**	**1**	**2**	**3**	**4**	**1**	**2**	**3**	**4**	**1**	**2**	**3**	**4**	**1**	**2**	**3**	**4**	**1**	**2**	**3**	**4**
1	**Literature review**																				
	Internet																				
	Books																				
	Jurnal																				
2	**Bulid Hardware design**																				
3	**Troubleshooting and**																				
	testing hardware																				
4	**Software writing**																				
5	**Debug any problem with**																				
	written software																				
6	**Begin thesis writing**																				
7	**Presentation/demo**																				
8	**Submit thesis**																				

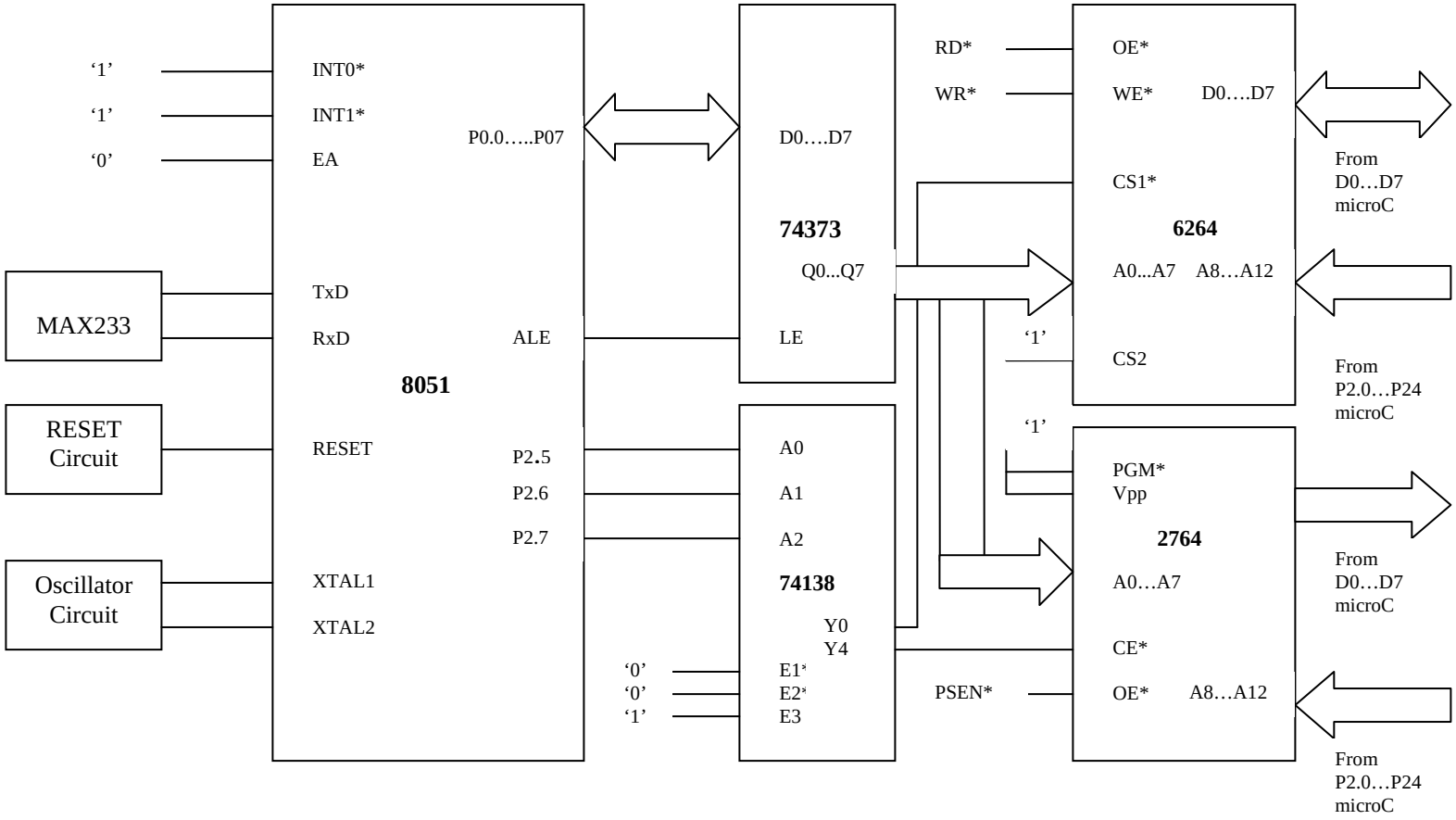
APPENDIX B

```
                          1
                          2     ;testing program seven segment display
                          3     ;tarikh : 8 march 2006
                          4     ;name : zaleha salleh
                          5
                          6
                          7     ;########################################
                          8
                          9
                         10             $MOD51
8000                     11             ORG      8000H
8000 759000              12     PLTEST: MOV      P1,#0
8003 90801B              13     AGAIN:  MOV      DPTR,#TABLE
8006 E4                  14     NEXT:   CLR      A
8007 93                  15             MOVC     A,@A+DPTR
8008 60F9                16             JZ       AGAIN
800A F590                17             MOV      P1,A
800C A3                  18             INC      DPTR
800D 7A08                19     DELAY:  MOV      R2,#8
800F 79FF                20     INLP1:  MOV      R1,#255
8011 78FF                21     INLP2:  MOV      R0,#255
8013 D8FE                22     INLP3:  DJNZ     R0,INLP3
8015 D9FA                23             DJNZ     R1,INLP2
8017 DAF6                24             DJNZ     R2,INLP1
8019 80EB                25             SJMP     NEXT
801B                     26     TABLE:
801B 8688C0A4            27             DB       86H,88H,0C0H,0A4H,0C0H,82H,99H
801F C08299
                         28
                         29             END

VERSION 1.2k ASSEMBLY COMPLETE, 0 ERRORS FOUND
07SEGMENT

AGAIN. . . . . .  C ADDR  8003H
DELAY. . . . . .  C ADDR  800DH  NOT USED
INLP1. . . . . .  C ADDR  800FH
INLP2. . . . . .  C ADDR  8011H
INLP3. . . . . .  C ADDR  8013H
NEXT . . . . . .  C ADDR  8006H
P1 . . . . . .  D ADDR  0090H  PREDEFINED
PLTEST . . . . . .  C ADDR  8000H  NOT USED
TABLE. . . . . .  C ADDR  801BH
```

APPENDIX C

```
$MOD51

KEYPAD  EQU     4000H
;LCD    EQU     6000H
;LCD1    EQU     6001H

        ORG     8000H
        MOV     SP,#5FH

;       MOV     20H,#00H        ;20H GANTI R5
;       MOV     21H,#01H        ;21H GANTI R6

;       LCALL   INIT_LCD        ;INITIALIZED LCD
;       LCALL   CLEAR_LCD       ;CLEAR LCD DISPLAY

;******************TEST WHICH KEY IS PRESSED**************************

;START: LCALL   DELAY
KEY:    MOV     DPTR,#KEYPAD
        MOVX    A,@DPTR
ONE:    CJNE    A,#8FH,KEY      ;KEY 1
        MOV     A,#1
        LCALL   PLTEST

PLTEST: MOV     P1,#0
AGAIN:  MOV     DPTR,#TABLE
NEXT:   CLR     A
        MOVC    A,@A+DPTR
        JZ      AGAIN
        MOV     P1,A
        INC     DPTR
DELAY:  MOV     R2,#8
INLP1:  MOV     R1,#255
INLP2:  MOV     R0,#255
INLP3:  DJNZ    R0,INLP3
        DJNZ    R1,INLP2
        DJNZ    R2,INLP1
        SJMP    NEXT
TABLE:
        DB      86H,88H,0C0H,0A4H,0C0H,82H,99H


;*******************************************************************

        END
```

APPENDIX D



SIMPLE BLOCK DIAGRAM FOR 8051 BASE SYSTEM

APPENDIX E

MM74C922 • MM74C923
16-Key Encoder • 20-Key Encoder

General Description

The MM74C922 and MM74C923 CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50 kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two-key roll-over is provided between any two switches.

An internal register remembers the last key pressed even after the key is released. The 3-STATE outputs provide for easy expansion and bus operation and are LPTTL compatible.

Features

- 50 kΩ maximum switch on resistance
- On or off chip clock
- On-chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- 3-STATE output LPTTL compatible
- Wide supply range: 3V to 15V
- Low power consumption

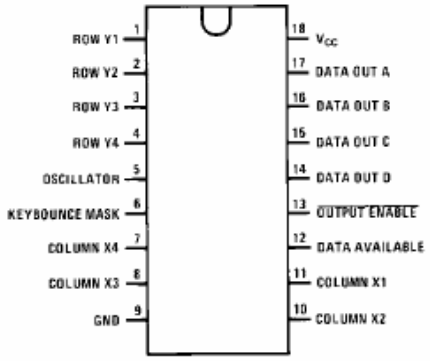
Ordering Code:

Order Number	Package Number	Package Description
MM74C922N	N18A	18-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74C922WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74C923WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74C923N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

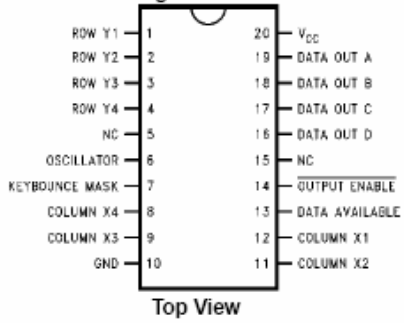
Connection Diagrams

Pin Assignment for DIP



Top View
MM94C922

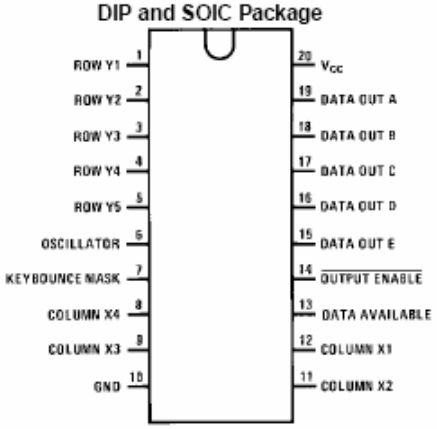
Pin Assignment for SOIC



Top View
MM74C922

Connection Diagrams (Continued)

Pin Assignment for
DIP and SOIC Package



Top View
MM74C923

Truth Tables

(Pins 0 through 11)

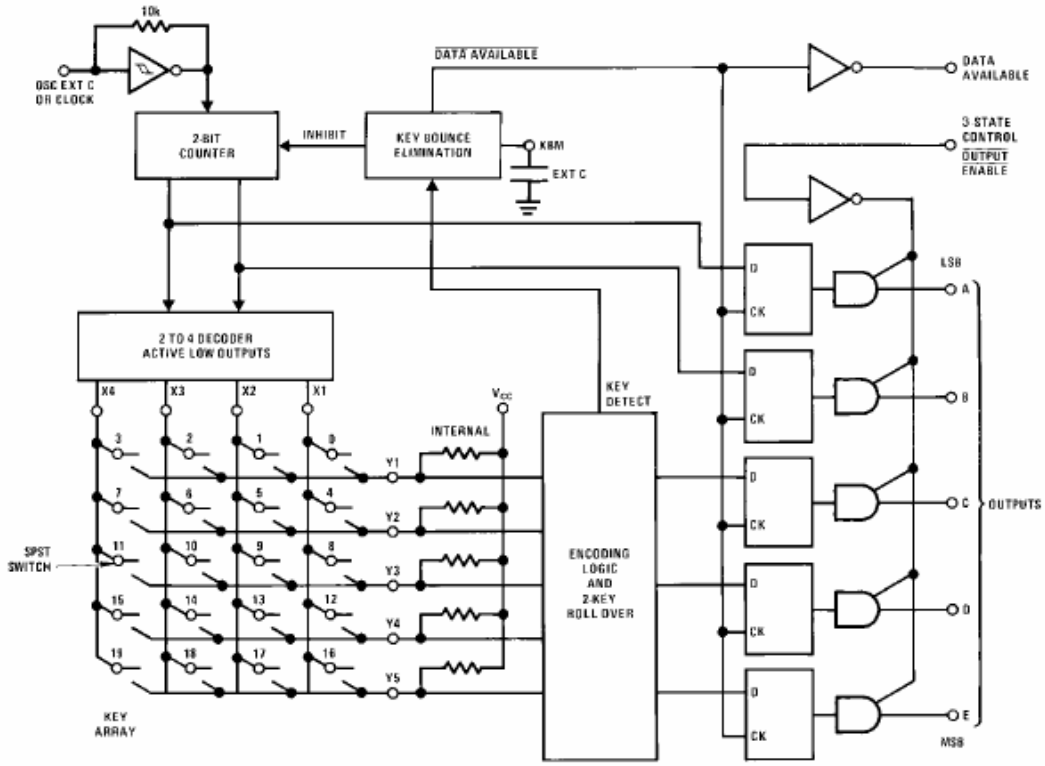
Switch Position	0 Y1,X1	1 Y1,X2	2 Y1,X3	3 Y1,X4	4 Y2,X1	5 Y2,X2	6 Y2,X3	7 Y2,X4	8 Y3,X1	9 Y3,X2	10 Y3,X3	11 Y3,X4
DATA A	0	1	0	1	0	1	0	1	0	1	0	1
DATA B	0	0	1	1	0	0	1	1	0	0	1	1
DATA C	0	0	0	0	1	1	1	1	0	0	0	0
DATA D	0	0	0	0	0	0	0	0	1	1	1	1
DATA E (Note 1)	0	0	0	0	0	0	0	0	0	0	0	0

(Pins 12 through 19)

Switch Position	12 Y4,X1	13 Y4,X2	14 Y4,X3	15 Y4,X4	16 Y5(Note 1), X1	17 Y5 (Note 1), X2	18 Y5 (Note 1), X3	19 Y5 (Note 1), X4
DATA A	0	1	0	1	0	1	0	1
DATA B	0	0	1	1	0	0	1	1
DATA C	1	1	1	1	0	0	0	0
DATA D	1	1	1	1	0	0	0	0
DATA E (Note 1)	0	0	0	0	1	1	1	1

Note 1: Omit for MM74C922

Block Diagram



Absolute Maximum Ratings (Note 2)

Voltage at Any Pin	V_{CC} − 0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM74C922, MM74C923	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
V_{CC}	18V
Lead Temperature	
(Soldering, 10 seconds)	260°C

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
V_{T+}	Positive-Going Threshold Voltage	V_{CC} = 5V, $I_{IN} \geq$ 0.7 mA	3.0	3.6	4.3	V
	at Osc and KBM Inputs	V_{CC} = 10V, $I_{IN} \geq$ 1.4 mA	6.0	6.8	8.6	V
		V_{CC} = 15V, $I_{IN} \geq$ 2.1 mA	9.0	10	12.9	V
V_{T-}	Negative-Going Threshold Voltage	V_{CC} = 5V, $I_{IN} \geq$ 0.7 mA	0.7	1.4	2.0	V
	at Osc and KBM Inputs	V_{CC} = 10V, $I_{IN} \geq$ 1.4 mA	1.4	3.2	4.0	V
		V_{CC} = 15V, $I_{IN} \geq$ 2.1 mA	2.1	5	6.0	V
$V_{IN(1)}$	Logical "1" Input Voltage,	V_{CC} = 5V	3.5	4.5		V
	Except Osc and KBM Inputs	V_{CC} = 10V	8.0	9		V
		V_{CC} = 15V	12.5	13.5		V
$V_{IN(0)}$	Logical "0" Input Voltage,	V_{CC} = 5V		0.5	1.5	V
	Except Osc and KBM Inputs	V_{CC} = 10V		1	2	V
		V_{CC} = 15V		1.5	2.5	V
I_{rp}	Row Pull-Up Current at Y1, Y2,	V_{CC} = 5V, V_{IN} = 0.1 V_{CC}		–2	–5	µA
	Y3, Y4 and Y5 Inputs	V_{CC} = 10V		–10	–20	µA
		V_{CC} = 15V		–22	–45	µA
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = –10 µA	4.5			V
		V_{CC} = 10V, I_O = –10 µA	9			V
		V_{CC} = 15V, I_O = –10 µA	13.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10 µA			0.5	V
		V_{CC} = 10V, I_O = 10 µA			1	V
		V_{CC} = 15V, I_O = 10 µA			1.5	V
R_{on}	Column "ON" Resistance at	V_{CC} = 5V, V_O = 0.5V		500	1400	Ω
	X1, X2, X3 and X4 Outputs	V_{CC} = 10V, V_O = 1V		300	700	Ω
		V_{CC} = 15V, V_O = 1.5V		200	500	Ω
I_{CC}	Supply Current	V_{CC} = 5V		0.55	1.1	mA
	Osc at 0V, (one Y low)	V_{CC} = 10V		1.1	1.9	mA
		V_{CC} = 15V		1.7	2.6	mA
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	µA
	at $\overline{\text{Output Enable}}$					
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	–1.0	–0.005		µA
	at $\overline{\text{Output Enable}}$					
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Except Osc and KBM Inputs	V_{CC} = 4.75V	V_{CC} – 1.5			V
$V_{IN(0)}$	Except Osc and KBM Inputs	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = –360 µA				
		V_{CC} = 4.75V	2.4			V
		I_O = –360 µA				
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = –360 µA				
		V_{CC} = 4.75V			0.4	V
		I_O = –360 µA				

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8	16		mA

AC Electrical Characteristics (Note 3)

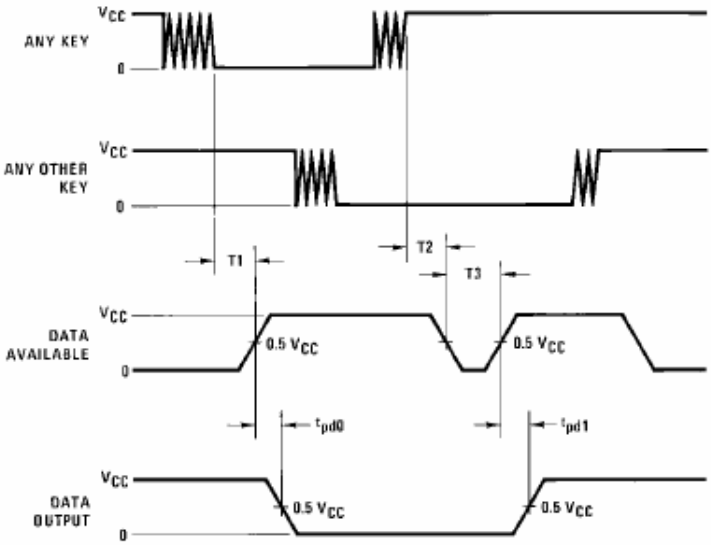
T_A = 25°C, C_L = 50 pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to	C_L = 50 pF (Figure 1)				
	Logical "0" or Logical "1"	V_{CC} = 5V		60	150	ns
	from D.A.	V_{CC} = 10V		35	80	ns
		V_{CC} = 15V		25	60	ns
t_{0H}, t_{1H}	Propagation Delay Time from	R_L = 10k, C_L = 10 pF (Figure 2)				
	Logical "0" or Logical "1"	V_{CC} = 5V, R_L = 10k		80	200	ns
	into High Impedance State	V_{CC} = 10V, C_L = 10 pF		65	150	ns
		V_{CC} = 15V		50	110	ns
t_{H0}, t_{H1}	Propagation Delay Time from	R_L = 10k, C_L = 50 pF (Figure 2)				
	High Impedance State to a	V_{CC} = 5V, R_L = 10k		100	250	ns
	Logical "0" or Logical "1"	V_{CC} = 10V, C_L = 50 pF		55	125	ns
		V_{CC} = 15V		40	90	ns
C_{IN}	Input Capacitance	Any Input (Note 4)		5	7.5	pF
C_{OUT}	3-STATE Output Capacitance	Any Output (Note 4)		10		pF

Note 3: AC Parameters are guaranteed by DC correlated testing.

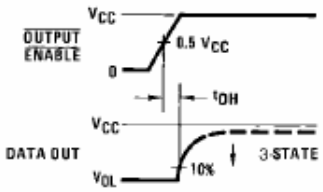
Note 4: Capacitance is guaranteed by periodic testing.

Switching Time Waveforms



T1 ≈ T2 ≈ RC, T3 ≈ 0.7 RC, where R ≈ 10k and C is external capacitor at KBM input.

FIGURE 1.



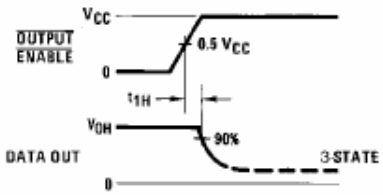
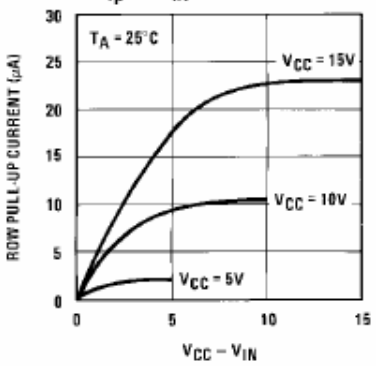


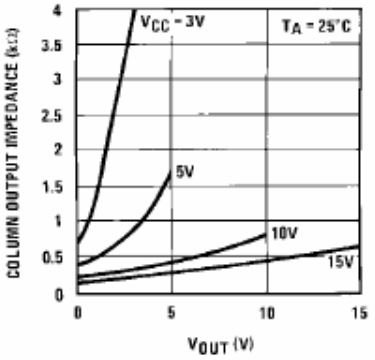
FIGURE 2.

Typical Performance Characteristics

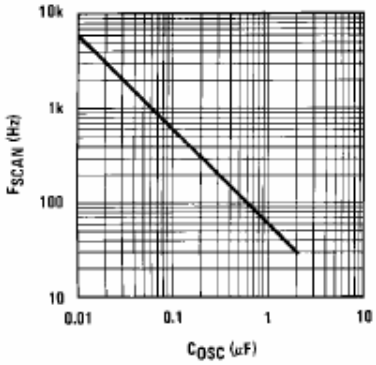
Typical I_{rp} vs V_{IN} at Any Y Input



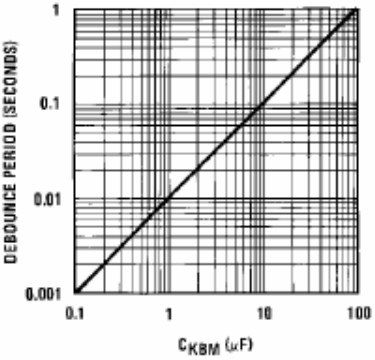
Typical R_{on} vs V_{OUT} at Any X Output



Typical F_{SCAN} vs C_{OSC}

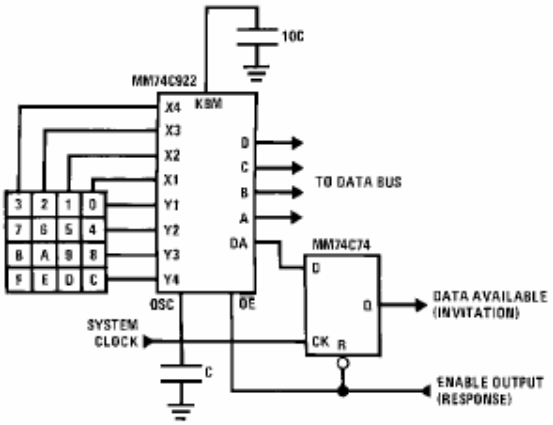


Typical Debounce Period vs C_{KBM}



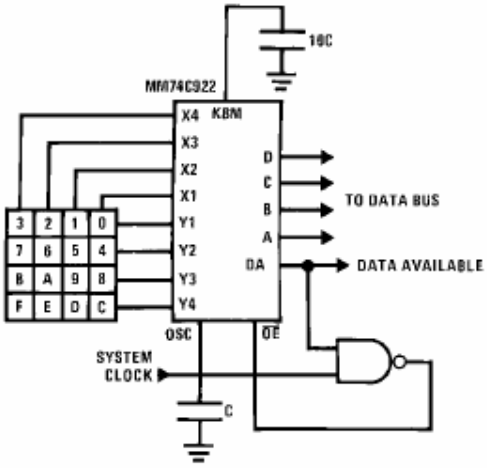
Typical Applications

Synchronous Handshake (MM74C922)



The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz

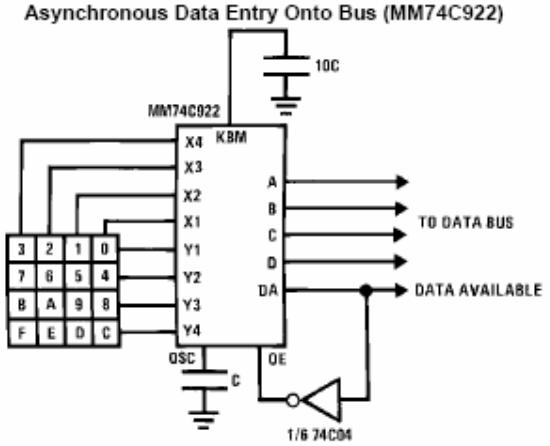
Synchronous Data Entry Onto Bus (MM74C922)



Outputs are enabled when valid entry is made and go into 3-STATE when key is released.

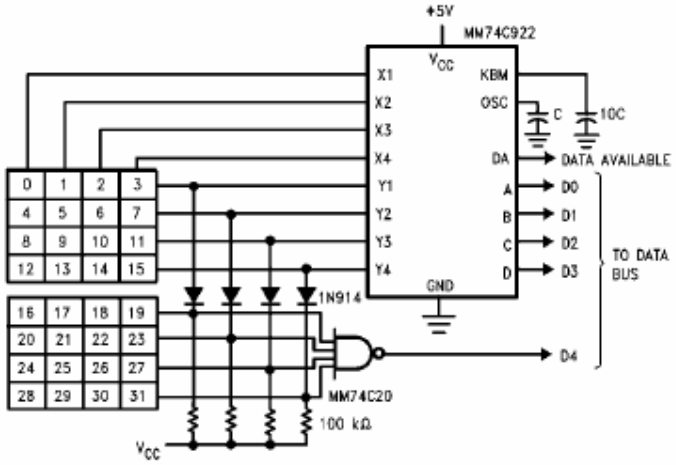
The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz

Asynchronous Data Entry Onto Bus (MM74C922)



Outputs are in 3-STATE until key is pressed, then data is placed on bus. When key is released, outputs return to 3-STATE.

Expansion to 32 Key Encoder (MM74C922)



Theory of Operation

The MM74C922/MM74C923 Keyboard Encoders implement all the logic necessary to interface a 16 or 20 SPST key switch matrix to a digital system. The encoder will convert a key switch closer to a 4(MM74C922) or 5(MM74C923) bit nibble. The designer can control both the keyboard scan rate and the key debounce period by altering the oscillator capacitor, C_{OSE}, and the key bounce mask capacitor, C_{MSK}. Thus, the MM74C922/MM74C923's performance can be optimized for many keyboards.

The keyboard encoders connect to a switch matrix that is 4 rows by 4 columns (MM74C922) or 5 rows by 4 columns (MM74C923). When no keys are depressed, the row inputs are pulled high by internal pull-ups and the column outputs sequentially output a logic "0". These outputs are open drain and are therefore low for 25% of the time and otherwise off. The column scan rate is controlled by the oscillator input, which consists of a Schmitt trigger oscillator, a 2-bit counter, and a 2–4-bit decoder.

When a key is depressed, key 0, for example, nothing will happen when the X1 input is off, since Y1 will remain high. When the X1 column is scanned, X1 goes low and Y1 will go low. This disables the counter and keeps X1 low. Y1 going low also initiates the key bounce circuit timing and locks out the other Y inputs. The key code to be output is a combination of the frozen counter value and the decoded Y inputs. Once the key bounce circuit times out, the data is latched, and the Data Available (DAV) output goes high.

If, during the key closure the switch bounces, Y1 input will go high again, restarting the scan and resetting the key bounce circuitry. The key may bounce several times, but as soon as the switch stays low for a debounce period, the closure is assumed valid and the data is latched.

A key may also bounce when it is released. To ensure that the encoder does not recognize this bounce as another key closure, the debounce circuit must time out before another closure is recognized.

The two-key roll-over feature can be illustrated by assuming a key is depressed, and then a second key is depressed. Since all scanning has stopped, and all other Y inputs are disabled, the second key is not recognized until the first key is lifted and the key bounce circuitry has reset.

The output latches feed 3-STATE, which is enabled when the Output Enable ($\overline{OE}$) input is taken low.

SN74LS240, SN74LS244

Octal Buffer/Line Driver with 3-State Outputs

The SN74LS240 and SN74LS244 are Octal Buffers and Line Drivers designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC board density.

- Hysteresis at Inputs to Improve Noise Margins
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Input Clamp Diodes Limit High-Speed Termination Effects

GUARANTEED OPERATING RANGES

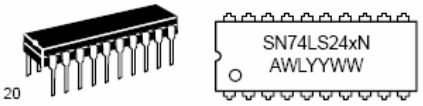
Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–3.0	mA
				–15	mA
I_{OL}	Output Current – Low			24	mA

ON Semiconductor

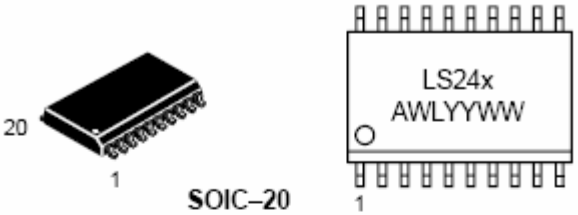
http://onsemi.com

LOW POWER SCHOTTKY

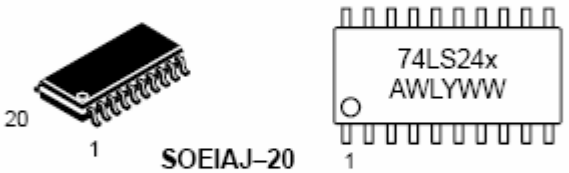
MARKING DIAGRAMS



PDIP–20
N SUFFIX
CASE 738



SOIC–20
DW SUFFIX
CASE 751D



SOEIAJ–20
M SUFFIX
CASE 967

x = 0 or 4
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

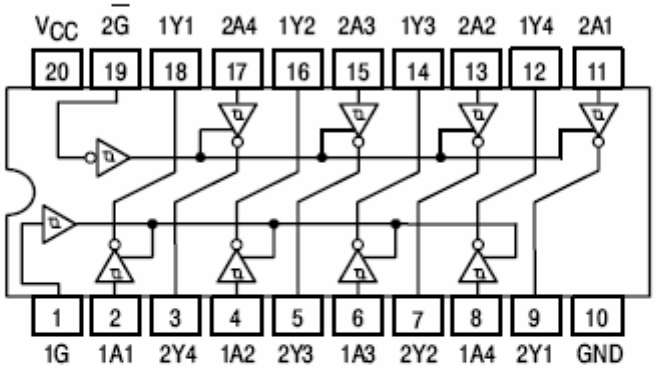
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

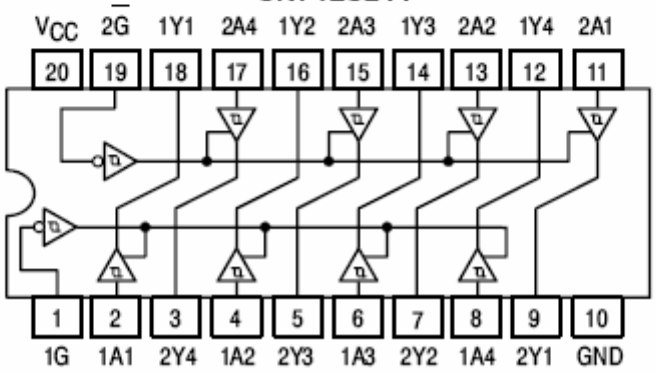
SN74LS240, SN74LS244

LOGIC AND CONNECTION DIAGRAMS DIP (TOP VIEW)

SN74LS240



SN74LS244



TRUTH TABLES

SN74LS240

INPUTS		OUTPUT
$\overline{1G}$, $\overline{2G}$	D	
L	L	H
L	H	L
H	X	(Z)

SN74LS244

INPUTS		OUTPUT
$\overline{1G}$, $\overline{2G}$	D	
L	L	L
L	H	H
H	X	(Z)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = HIGH Impedance

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
$V_{T+}-V_{T-}$	Hysteresis	0.2	0.4		V	V_{CC} = MIN
V_{IK}	Input Clamp Diode Voltage		–0.65	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA
V_{OH}	Output HIGH Voltage	2.4	3.4		V	V_{CC} = MIN, I_{OH} = –3.0 mA
		2.0			V	V_{CC} = MIN, I_{OH} = MAX
V_{OL}	Output LOW Voltage		0.25	0.4	V	I_{OL} = 12 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			0.35	0.5	V	I_{OL} = 24 mA
I_{OZH}	Output Off Current HIGH			20	µA	V_{CC} = MAX, V_{OUT} = 2.7 V
I_{OZL}	Output Off Current LOW			–20	µA	V_{CC} = MAX, V_{OUT} = 0.4 V
I_{IH}	Input HIGH Current			20	µA	V_{CC} = MAX, V_{IN} = 2.7 V
				0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current			–0.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 1)	–40		–225	mA	V_{CC} = MAX
I_{CC}	Power Supply Current Total, Output HIGH			27	mA	V_{CC} = MAX
	Total, Output LOW LS240			44		
	Total, Output LOW LS244			46		
	Total at HIGH Z LS240			50		
	Total at HIGH Z LS244			54		

1. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_{PLH} t_{PHL}	Propagation Delay, Data to Output LS240		9.0 12	14 18	ns	C_L = 45 pF, R_L = 667 Ω
t_{PLH} t_{PHL}	Propagation Delay, Data to Output LS244		12 12	18 18	ns	
t_{PZH}	Output Enable Time to HIGH Level		15	23	ns	
t_{PZL}	Output Enable Time to LOW Level		20	30	ns	
t_{PLZ}	Output Disable Time from LOW Level		15	25	ns	C_L = 5.0 pF, R_L = 667 Ω
t_{PHZ}	Output Disable Time from HIGH Level		10	18	ns	

FAIRCHILD
SEMICONDUCTOR™

January 1999

NMC27C64
65,536-Bit (8192 x 8) CMOS EPROM

General Description

The NMC27C64 is a 64K UV erasable, electrically reprogrammable and one-time programmable (OTP) CMOS EPROM ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C64 is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over extended and military temperature ranges.

The NMC27C64Q is packaged in a 28-pin dual-in-line package with a quartz window. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

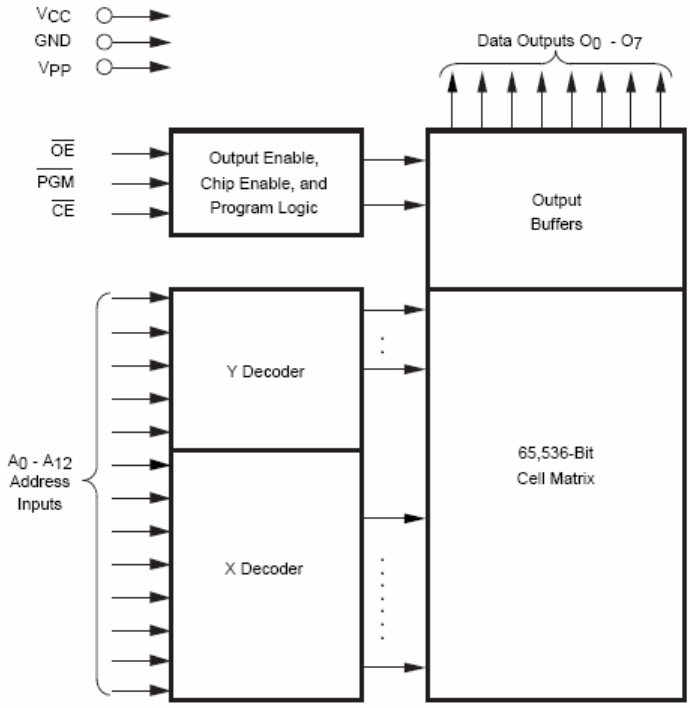
The NMC27C64N is packaged in a 28-pin dual-in-line plastic molded package without a transparent lid. This part is ideally suited for high volume production applications where cost is an important factor and programming only needs to be done once.

This family of EPROMs are fabricated with Fairchild's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- High performance CMOS
  - —150 ns access time
- JEDEC standard pin configuration
  - —28-pin Plastic DIP package
  - —28-pin CERDIP package
- Drop-in replacement for 27C64 or 2764
- Manufacturers identification code

Block Diagram



DS008634-1

Connection Diagram

27C512 27512	27C256 27256	27C128 27128	27C32 2732	27C16 2716					27C16 2716	27C32 2732	27C128 27128	27C256 27256	27C512 27512
A15	VPP	VPP			VPP	1	28	VCC			VCC	VCC	VCC
A12	A12	A12			A12	2	27	PGM			PGM	A14	A14
A7	A7	A7	A7	A7	A7	3	26	NC	VCC	VCC	A13	A13	A13
A6	A6	A6	A6	A6	A6	4	25	A8	A8	A8	A8	A8	A8
A5	A5	A5	A5	A5	A5	5	24	A9	A9	A9	A9	A9	A9
A4	A4	A4	A4	A4	A4	6	23	A11	VPP	A11	A11	A11	A11
A3	A3	A3	A3	A3	A3	7	22	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$/VPP	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$/VPP
A2	A2	A2	A2	A2	A2	8	21	A10	A10	A10	A10	A10	A10
A1	A1	A1	A1	A1	A1	9	20	$\overline{CE}$	$\overline{CE}$/PGM	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$/PGM	$\overline{CE}$
A0	A0	A0	A0	A0	A0	10	19	O7	O7	O7	O7	O7	O7
O0	O0	O0	O0	O0	O0	11	18	O6	O6	O6	O6	O6	O6
O1	O1	O1	O1	O1	O1	12	17	O5	O5	O5	O5	O5	O5
O2	O2	O2	O2	O2	O2	13	16	O4	O4	O4	O4	O4	O4
GND	GND	GND	GND	GND	GND	14	15	O3	O3	O3	O3	O3	O3

NMC27C64

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C64 pins.

DS008634-2

Pin Names

A0–A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0 –O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect
V_{PP}	Programming Voltage
V_{CC}	Power Supply
GND	Ground

Commercial Temperature Range V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64Q, N 150	150
NMC27C64Q, N 200	200

Extended Temp Range (-40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64QE, NE200	200

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to -0.6V
All Output Voltages with Respect to Ground (Note 10) V_{CC}	+1.0V to GND -0.6V
V_{PP} Supply Voltage and A_9 with Respect to Ground During Programming	+14.0V to -0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to -0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range NMC27C64Q 150, 200 NMC27C64N 150, 200	0°C to +70°C
NMC27C64QE 200 NMC27C64NE 200	-40°C to +85°C
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	µA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f=5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		5	20	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	µA
I_{PP}	VPP Load Current	$V_{PP} = V_{CC}$		10	µA	
V_{IL}	Input Low Voltage		-0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} +1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 µA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 µA	V_{CC} - 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C64				Units
			150		200, E200		
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		60	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		ns

FAIRCHILD
SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS138 • DM74LS139
Decoder/Demultiplexer

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The DM74LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The DM74LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

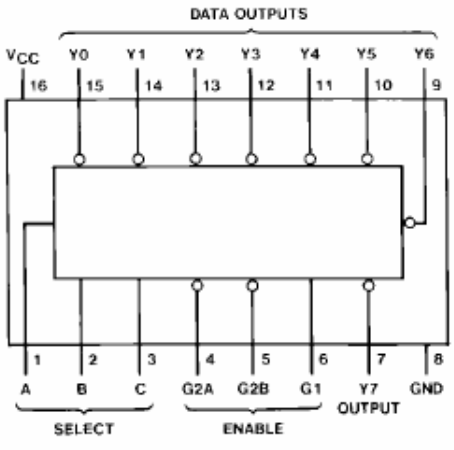
All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

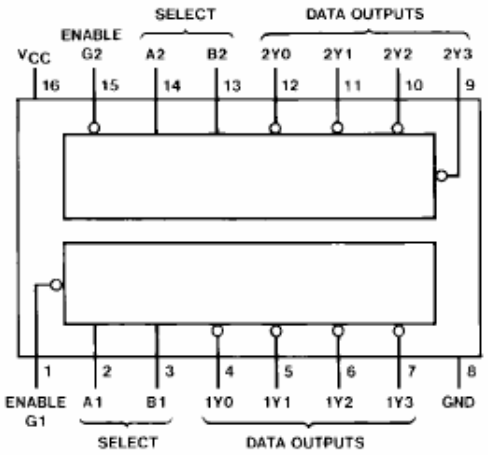
- Designed specifically for high speed:
  - Memory decoders
  - Data transmission systems
- DM74LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- DM74LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)
  - DM74LS138 21 ns
  - DM74LS139 21 ns
- Typical power dissipation
  - DM74LS138 32 mW
  - DM74LS139 34 mW

Connection Diagrams

DM74LS138



DM74LS139



Function Tables

DM74LS138

Inputs					Outputs							
Enable		Select										
G1	G2 (Note 1)	C	B	A	YO	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

DM74LS139

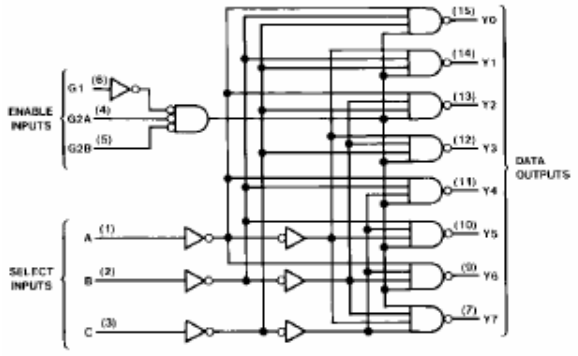
Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Level
L = LOW Level
X = Don't Care

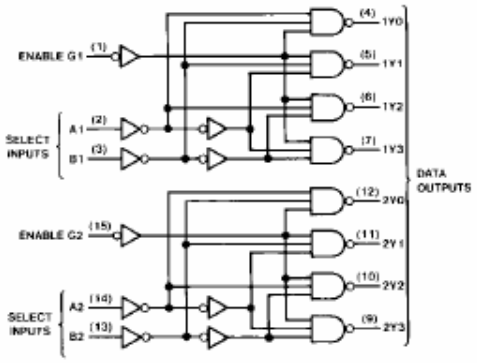
Note 1: G2 = G2A + G2B

Logic Diagrams

DM74LS138



DM74LS139



DM74LS139 Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			–0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

DM74LS139 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 6)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = –18 mA			–1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			–0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 7)	–20		–100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 8)		6.8	11	mA

Note 6: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 7: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 8: I_{CC} is measured with all outputs enabled and OPEN.

DM74LS139 Switching Characteristics

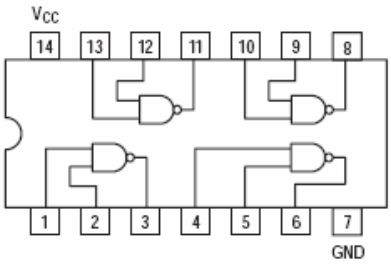
at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Select to Output		18		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Select to Output		27		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Enable to Output		18		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Enable to Output		24		40	ns

SN74LS00

Quad 2-Input NAND Gate

- ESD > 3500 Volts



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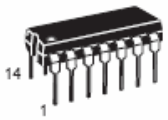
LOW POWER SCHOTTKY



PLASTIC
N SUFFIX
CASE 646

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–0.4	mA
I_{OL}	Output Current – Low			8.0	mA

SN74LS00

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage		–0.65	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage	2.7	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current			20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
				0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current			–0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)	–20		–100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH			1.6	mA	V_{CC} = MAX	
	Total, Output LOW			4.4			

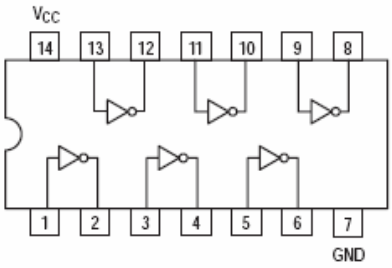
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_{PLH}	Turn–Off Delay, Input to Output		9.0	15	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn–On Delay, Input to Output		10	15	ns	

SN74LS04

Hex Inverter



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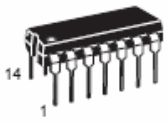
LOW POWER SCHOTTKY



PLASTIC
N SUFFIX
CASE 646

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–0.4	mA
I_{OL}	Output Current – Low			8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage		–0.65	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage	2.7	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current			20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
				0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current			–0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)	–20		–100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH			2.4	mA	V_{CC} = MAX	
	Total, Output LOW			6.6			

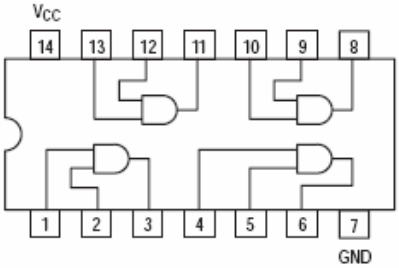
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_{PLH}	Turn–Off Delay, Input to Output		9.0	15	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn–On Delay, Input to Output		10	15	ns	

SN74LS08

Quad 2-Input AND Gate



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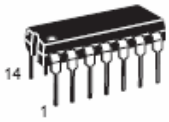
LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–0.4	mA
I_{OL}	Output Current – Low			8.0	mA



PLASTIC
N SUFFIX
CASE 646

SN74LS08

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage		–0.65	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage	2.7	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current			20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
				0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current			–0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)	–20		–100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH			4.8	mA	V_{CC} = MAX	
	Total, Output LOW			8.8			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Limits Typ	Limits Max	Unit	Test Conditions
t_{PLH}	Turn–Off Delay, Input to Output		8.0	15	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn–On Delay, Input to Output		10	20	ns	

SN74LS373 SN74LS374

Octal Transparent Latch with 3-State Outputs; Octal D-Type Flip-Flop with 3-State Output

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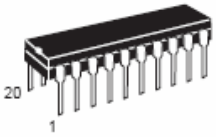
LOW POWER SCHOTTKY

The SN74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

The SN74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all ON Semiconductor TTL families.



PLASTIC
N SUFFIX
CASE 738

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Hysteresis on Latch Enable
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects

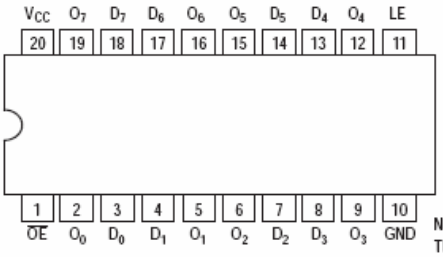
GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–2.6	mA
I_{OL}	Output Current – Low			24	mA

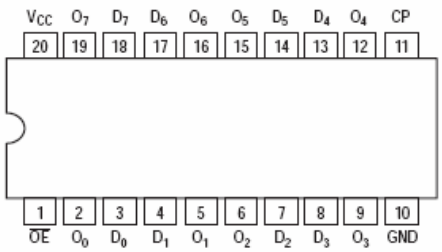
SN74LS373 SN74LS374

CONNECTION DIAGRAM DIP (TOP VIEW)

SN74LS373



SN74LS374



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$D_0 - D_7$	Data Inputs	0.5 U.L.	0.25 U.L.
LE	Latch Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{OE}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$O_0 - O_7$	Outputs	65 U.L.	15 U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.

TRUTH TABLE

LS373

D_n	LE	$\overline{OE}$	O_n
H	H	L	H
L	H	L	L
X	L	L	Q_0
X	X	H	Z*

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

LS374

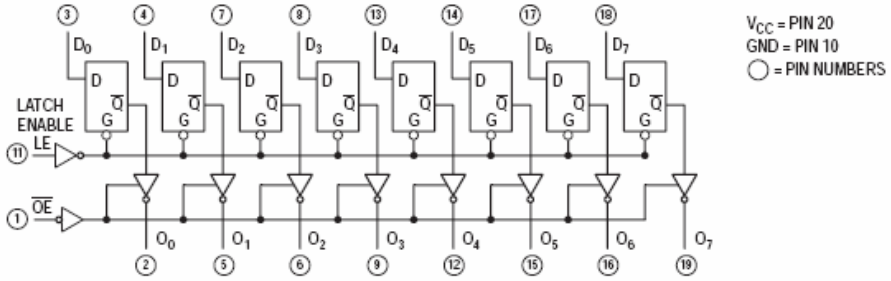
D_n	LE	$\overline{OE}$	O_n
H	⎍	L	H
L	⎍	L	L
X	X	H	Z*

* Note: Contents of flip-flops unaffected by the state of the Output Enable input ($\overline{OE}$).

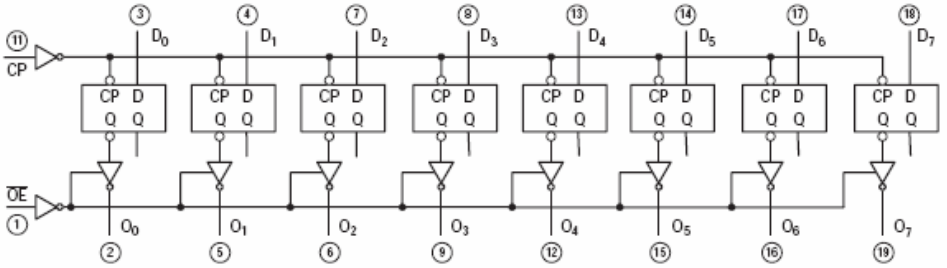
SN74LS373 SN74LS374

LOGIC DIAGRAMS

SN74LS373



SN74LS374



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
V_{IK}	Input Clamp Diode Voltage		−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	2.4	3.1		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
V_{OL}	Output LOW Voltage		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
			0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH			20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current LOW			−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
				0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)	−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current			40	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.