DEVELOPMENT OF EARTH LEAKAGE CIRCUIT BREAKER WITH AN AUTO RE-CLOSER UNIT

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This thesis is submitted as partial fulfillment of the requirements for the award of the Bachelor of Electrical Engineering (Power System)

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Specially dedicated to my beloved family and those people who have guided and inspired me throughout my journey of education

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ABSTRACT

Power system protection is the most important requirement before the power system is put into operation. Electrical energy has caused dangers both to the human and the machines. Protection system is mostly controlled by the Earth Leakage Circuit Breaker (ELCB). This device is the brain of the protection system that monitors input current from power line by it sensor Zero phase Current Transformer (ZCT), then sending the signals to the mechanical switch to tripped the circuit breaker. ELCB is widely applied by consumer weather it is for resident, factory, laboratory and also power distribution. Power system protection can be implemented at various stages and various types of protection devices. Because industrial operation requires protection of their Equipment from the lightning, short-circuit and also over-current, so the ELCB will serve the purpose as the protection of their system. This project will attempt to improve and design the currently ELCB by using PIC microcontroller so that it have the ability to identify the fault, act accordingly, display the fault and also to re-close it back to normal. The PIC micro controller will cause the ELCB to trip when there is unbalance current from power line flow through life line and neutral line is ≥100mA. In order to design it, first thing of the current from the power line need to be measure in order to monitor it using ZCT including testing the fault (over current, lightning and short circuit) and when such condition arise, it will isolate the load from power line in the shortest time possible without harming the any other electrical devices. In this project PIC microcontroller will be used to control and operate the SSR, thus replacing the current mechanical switch.

ABSTRAK

Perlindungan sistem kuasa adalah keperluan yang paling penting sebelum ia di masukkan ke dalam operasi. Tenaga Elektrik telah menyebabkan bahaya kepada manusia dan juga mesin-mesin. Sistem perlindungan biasanya di kawal oleh Pemutus Litar Bocor Kebumi (ELCB). Peralatan ini adalah otak bagi sistem perlindungan dimana ia bertindak sebagai pemerhati arus masukan daripada talian kuasa oleh pengesan Zero Pengubah Tanpa Arus Fasa (ZCT), kemudiannya ia menghantar signal tersebut ke suis mekanikal untuk terpelantikkan pemutus litar. ELCB digunakan secara menyeluruh oleh pengguna sama ada untuk kediaman, kilang, makmal dan juga pembahagian kuasa. Perlindungan system kuasa boleh digunakan di banyak peringkat oleh banyak jenis peralatan perlindungan. Oleh kerana operasi industri memerlukan perlindungan mesin mereka daripada kilat, litar pintas dan juga lebihan arus, maka ELCB ini akan digunakan bagi tujuan perlindungan kepada system mereka. Projek ini adalah cubaan bagi menambah baikan dan juga mencipta semula ELCB yang sedia ada dengan menggunakan PIC pengawal mikro supaya ELCB itu nanti mempunyai keupayaan untuk mengenalpasti kesilapan, bertindak sepatutnya, menunjukkan kesilapan dan juga menyambung kembali litar ELCB yang telah terpelantik kepada asal. PIC pengawal mikro akan menyebabkan ELCB itu terpelantik sekiranya terdapat arus yang tidak stabil daripada talian kuasa yang melalui talian Life dan neutral adalah ≥100mA. Bagi mencipta ELCB ini pertama sekali, arus daripada talian kuasa perlu di periksa supaya ZCT dapat memerhatikan dan termasuk memeriksa kesalahan (lebihan arus, kilat dan litar pintas) dan apabila semua criteria ini dipenuhi, ELCB tadi akan bertindak memutuskan sambungan barangan elektrik daripada talian kuasa dalam sepantas mungkin tanpa merosakkan mana-mana peralatan elektrik. Dalam projek ini, PIC pengawal mikro digunakan bagi mengawal Relay keadaan tetap (SSR), yang mana telah ditukarkan daripada suis mekanikal asal.

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LIST OF ABBREVIATIONS

AC	–	Alternate Current
ADC	–	Analog to Digital Converter
DC	–	Direct Current
I_i	–	Input Current
Io	–	Output Current
LED	–	Light Emitting Diode
LCD	–	Liquid Crystal Display
PIC	–	Programmable Intelligent Computer
SSR	–	Solid State Relay
V	–	Voltage
V_{in}	–	Input Voltage
V_o	–	Output Voltage
ZCT	–	Zero phase Current Transformer
Ω	–	Ohm

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CHAPTER 1

INTRODUCTION

1.1 Project Background

This project is focused on improving the current ELCB that is using mechanical switch into a new ELCB that using electronic switch. Nowadays ELCB is manually controlled by mechanical switch and have a limited function which are cannot distinguished and notify either permanent or temporary fault that occurred. The problem comes when there is no resident at house whenever the fault or tripping occurred. The electrical equipment power will be disconnected will cause some trouble for the resident. We can take an example if there is no resident currently in the house for a while and the ELCB in the resident is currently trip, some Electrical equipment like refrigerator and water pump for aquarium will become malfunction. Thus the fresh vegetable and meat in the fridge will expired and smelly meanwhile the fish in the aquarium may die because lack of oxygen. This may seems unimportant, but if we can solve this problem we can make human life a bit easier. As a future engineer who is a problem solver, we need to solve this problem as our first task. The focus of this project is to design and improving the current ELCB to a new ELCB with an auto re-closer unit. The new ELCB function does not limited at the auto switching, but it also can differentiate and display the type of fault so that the user is aware of the situation.

There are two types of fault normally detected by ELCB, which are permanent fault and temporary fault. Permanents fault is type of fault that occurred because of short-circuits between both life wire and neutral wire or ground wire, meanwhile temporary fault is type of fault that occurred from the effect of surge current from the lightning. The basic concept of the ELCB is if there are fault occurred, ZCT will sense the fault and send the signal to the ELCB to cut the power to the load (tripped). After 10 second the ELCB will connect back the power to the load, after that if the ELCB is remain connected with the load that means the fault is temporary like lightning. Meanwhile if after the ELCB is connected back to the load and it still detect any fault, it will re-close back. The cycle will be repeated for 3 times, if the fault is still detected, the ELCB will isolated the power from the load and it will display the fault is permanents like short-circuit or over-current. Until the fault is correct by the user, the ELCB will remain tripped and the user need to manually switch on the ELCB after the fault is correct to avoid electrical hazard. In this project the PIC microcontroller has been chosen as a control element, and the Solid State Relay (SSR) is selected as switching device.

The first problem we need to be clear in this project is to understand and know the differentiation between permanent fault and temporary fault. All aspect must be considered and we cannot neglect even a little for the safety of human life. The second problem is how to convert mechanical switch from original ELCB to a new electronic ELCB. Original ELCB used the principal of magnetic, and we need to change the signal of magnetic to electrical signal for the new ELCB. The third problem need to be clear is sensing element that can be use to send the fault signal to the PIC. For all this to operate together, we need to choose suitable components with rating current and voltage that is suitable to operate together and then start designing the suitable circuit that connect all the system.

1.2 Objectives:

The objectives of this project are:

i. To design an ELCB with an auto re-closer unit.
ii. To implement the use of Micro-C and power electronic switch in designing hardware.
iii. To notify user either the fault mode is temporary or permanents.

1.3 Scope of project

i. To improve the currently Earth Leakage Circuit Breaker (ELCB) into a new ELCB which have the ability to automatically trigger on back after being trip.
ii. The new ELCB can also distinguish either it is permanent fault or temporary fault that occur and it will only trigger on when necessary.
iii. To ensure this project work perfectly, the use of PIC18F4550 and P-Spice software will be implement.

1.4 Literature Review

An Earth Leakage Circuit Breaker (ELCB) is a device with two earth terminals used to directly detect currents leaking to earth from an installation and cut the power. They were mainly used on TT earthing systems. By having the assumption of the presence of current in the earth line, it means there is any leaking current from the main incoming live cable, thus the power has to be cut off to ensure the safety. The state of the ELCB when it cuts the power is known as being tripped. Every time the ELCB is tripped, it can be reset (connected back the power line) by resetting the trip button. Originally there are two types of ELCBs, the voltage operated device and the differential current operated device vELCB and iELCB. vELCBs were first introduced about sixty years ago and iELCB were first introduced about forty years ago [3].

The principle of operation of the vELCB is as follows. Under normal conditions the closed contacts of the vELCB feed the supply current to the load. The load is protected by a metal frame, such as in an electric cooker. The vELCB also has a relay coil, one end of which is connected to the metal frame and one end connected directly to ground. A shock risk will arise if a breakdown in the insulation occurs in the load which causes the metal frame to rise to a voltage above earth. A resultant current will flow from the metalwork through the relay coil to earth and when the frame voltage reaches a dangerous level, e.g. 50 volts, the current flowing through the relay coil will be sufficient to activate the relay thereby causing opening of the supply contacts and removal of the shock risk [3].

ELCB is essentially a voltage sensing device intended to detect dangerous voltage and current fault. The level of shock protection provided by the vELCB was somewhat limited as these devices would not provide shock protection in the event of direct contact with a live part. An additional problem with the vELCB was its tendency to be tripped by earth currents originating in other installations [3].

For many years, the voltage operated ELCB and the differential current operated ELCB were both referred to as ELCBs because it was a simpler name to remember. However, the use of a common name for two different devices gave rise to considerable confusion in the electrical industry. If the wrong type was used on an installation, the level of protection given could be substantially less than that intended. To remove this confusion, IEC decided to apply the term Residual Current Device (RCD) to differential current operated ELCBs. Residual current refers to any current over and above the load current.

Through early research that have been done and the guidelines from articles, it states that the development of ELCB is focused to only development of better device and not to improve the system of ELCB cause there are no articles that give the idea how to add the function and system to this ELCB. Until today what the article said is the type, function and process of each component in ELCB. So it is important to struggle and combine all knowledge to design something new for this device [4].

1.5 Thesis Outline

This thesis contains 5 chapters which is every chapter have its own purpose. After viewing the entire chapter in this thesis, hopefully the viewer can understand the whole system design for this project.

Chapter 1 describe on the background of the project, objectives, scope of the project and the literature review that referred to in the development of Earth Leakage Circuit Breaker with an auto re-closer unit.

Chapter 2 is focused to the theory of the Earth Leakage Circuit Breaker (ELCB), where it described about problems, ELCB design, the components inside ELCB and the operation of this device.

Chapter 3 elaborated more on the designing and operation of the new ELCB with an auto re-closer unit system. Besides it also describe the functions of each components used in the circuit especially on the second stage circuit.

Chapter 4 is focused to the control element circuit which is the most important part of the system. It described about the system of microcontroller detailed from the hardware until the software that has been used in this project.

Chapter 5 presents the data and experimental result while in development process. The result of this project is also accompanied by the discussions for each problem statements.

Lastly is Chapter 6, in this chapter the conclusion have been made for the project from the whole aspect and there are also suggestions to improve the new ELCB in the future, in case for the commercialization. The costing stated to produce the ELCB is also included.

CHAPTER 2

EARTH LEAKAGE CIRCUIT BREAKER

2.1 Introduction

An Earth Leakage Circuit Breaker (ELCB) is a device used to directly detect currents leaking to earth from an installation and cut the power. Early ELCBs responded to sine wave fault currents, but not to rectified fault current. Over time, filtering against nuisance trips has also improved. Early ELCBs thus offer a little less safety and higher risk of nuisance trip. The ability to distinguish between a fault condition and non-risk conditions is called discrimination. Many electrical installations have relatively high earth impedance. This may be due to the use of a local earth rod (TT systems), or to dry local ground conditions.

This type of installation is dangerous and a safety risk if a live to earth fault current flows. Because of earth impedance is high:

i. Not enough current exists to trip a fuse or circuit breaker, so the condition persists unclear indefinitely.
ii. The high impedance earth cannot keep the voltage of all exposed metal to a safe voltage, all such metalwork may rise to close to live conductor voltage.

These dangers can be drastically reduced by the use of an ELCB or Residual-current device (RCD).

The ELCB makes such installations much safer by cutting the power if these dangerous conditions occur. This approach to electrical safety is called EEBAD. In Britain EEBAD domestic installations became standard in the 1950s.

In non-technical terms if a person touches something, typically a metal part on faulty electrical equipment, which is at a significant voltage relative to the earth, electrical current will flow through him/her to the earth. The current that flows is too small to trip an electrical fuse which could disconnect the electricity supply, but can be enough to kill. An ELCB detects even a small current (ZCT sensitivity) to earth (Earth Leakage) and disconnects the equipment (Circuit Breaker).

This chapter describe about detail of ELCB and about its operation so that the reader will get a clear idea how the ELCB is working. To achieve that first we need to study more about ELCB and doing some research about the ELCB operation

The objectives of this chapter are:

i. To know the system of basic Earth Leakage Circuit Breaker
ii. To know the components of Earth Leakage Circuit Breaker and know the function of each component.
iii. To understand how the device work

2.2 Problems of nowadays ELCB

Earth Leakage Circuit Breaker is one type of electrical equipment that used as a protection device. The main purpose of this type of equipment is to cut off the power when the problem occurred. But the problem is will the device back to normally condition and function if the error occurred and there are no a human that can switch on back the device due to many reasons.

The device is using mechanical switch that must be switch on manually, after ELCB is being tripped it will stay off until the user push it back to the on condition although the problem that occurred is temporary fault and occurred in one millisecond.

The device also can not differentiate whether the fault is temporary or permanent fault where there are the differentiations between these two types. It also does not act differently for these two types of faulty.

2.3 Electrical faults

A fault is any abnormal situation in an electrical system in which the electrical current may or may not flow through the intended parts. Equipment failure also attributable to some defect in the circuit, example is loose connection, insulation failure or short circuit etc. The ype of faults in a distribution network that is detected by an ELCB is:

i) Over-Current Fault
ii) Short-Circuit Fault
iii) Lightning Fault

2.3.1 Over-current Fault

The National Electrical Code defines over current as any current in excess of the rated current of equipment or the ampacity of a conductor. It may result from overload, short circuit, or ground fault. Current flow in a conductor always generates heat. The greater the current flow, the hotter the conductor. Excess heat is damaging to electrical components. For that reason, conductors have a rated continuous current carrying capacity or ampacity. Over current protection devices are used to protect conductors from excessive current flow. These protective devices are designed to keep the flow of current in a circuit at a safe level to prevent the circuit conductors from overheating. Figure 2.1 shows that the current flow during over-current condition.

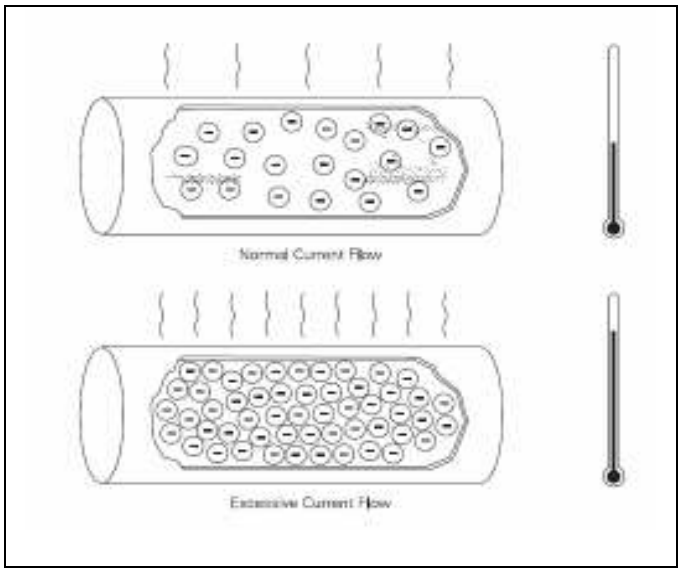


Figure 2.1: Over Current Flow

In term of over-current fault when a current greater than that which a circuit or a fuse is designed to carry, the fuse or wire may melt or damage the other elements of the circuit.

2.3.2 Short-Circuit Fault

A short circuit in an electrical circuit is one that allows a current to travel along a different path from the one originally intended. The electrical opposite of a short circuit is an "open circuit", which is an infinite resistance between two nodes. It is an abnormal low-resistance connection between two nodes of an electrical circuit that are meant to be at different voltages. This result in an excessive electric current (over-current) and potentially causes circuit damage, overheating, fire or explosion. Although usually the result of a fault, there are cases where short circuits are caused intentionally, for example, for the purpose of voltage-sensing crowbar circuit protectors.

In circuit analysis, the term short circuit is used by analogy to designate a zero-impedance connection between two nodes. This forces the two nodes to be at the same voltage. In an ideal short circuit, this means there is no resistance and no voltage drop across the short. In simple circuit analysis, wires are considered to be shorts. In real circuits, the result is a connection of nearly zero impedance, and almost no resistance. In such a case, the current drawn is limited by the rest of the circuit. Figure 2.2 show the Normal and short circuit condition, meanwhile figure 2.3 shows about short circuit due to broken insulation.

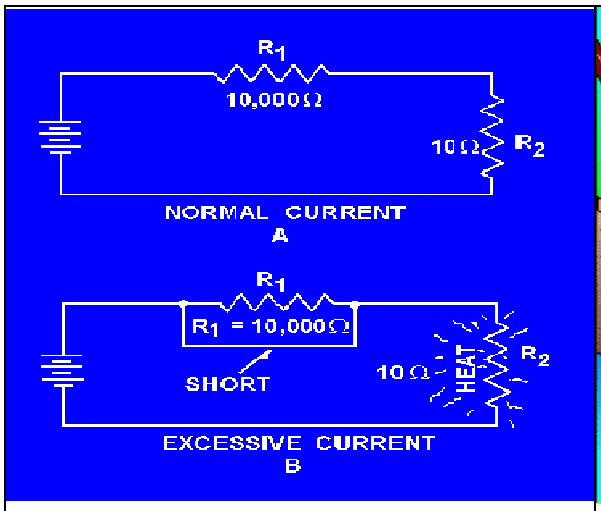


Figure 2.2: Normal & short circuit

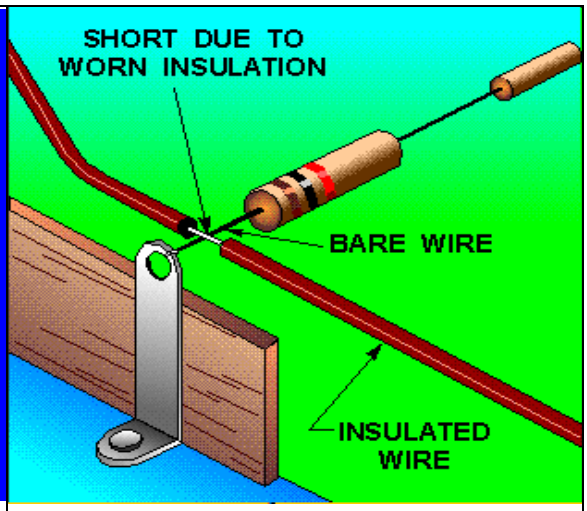


Figure 2.3: Short due to broken insulation

In mains circuits, short circuits are most likely to occur between two phases, between a phase and neutral or between a phase and earth (ground). Such short circuits are likely to result in a very high current and therefore quickly trigger an over-current protection device. However, it is possible for short circuits to arise between neutral and earth conductors, and between two conductors of the same phase. Such short circuits can be dangerous, particularly as they may not immediately result in a large current and are therefore less likely to be detected. Possible effects include unexpected energisation of a circuit presumed to be isolated. To help reduce the negative effects of short circuits, power distribution transformers are deliberately designed to have a certain amount of leakage reactance. The leakage reactance (usually about 5 to 10% of the full load impedance) helps limit both the magnitude and rate of rise of the fault current.

2.3.3 Lightning Fault

Lightning is the visible discharge of static electricity within a cloud, between clouds, or between the earth and a cloud. Scientists still do not fully understand what causes lightning, but most experts believe that different kinds of ice interact in a cloud. Updrafts in the clouds separate charges, so that positive charges flow towards the top of the cloud and the negative charges flow to the bottom of the cloud. When the negative charge moves downwards, a”stepped leader” is created. The leader rushes towards the earth in 150-foot discrete steps, producing an ionized path in the air. The major part of the lightning discharge current is carried in the return stroke, which flows along the ionized path [4]. Figure 2.4 show the lightning protection in a house and Figure 2.5 show the how the lightning stepped occurred.

Figure2.4: Lightning and Protection

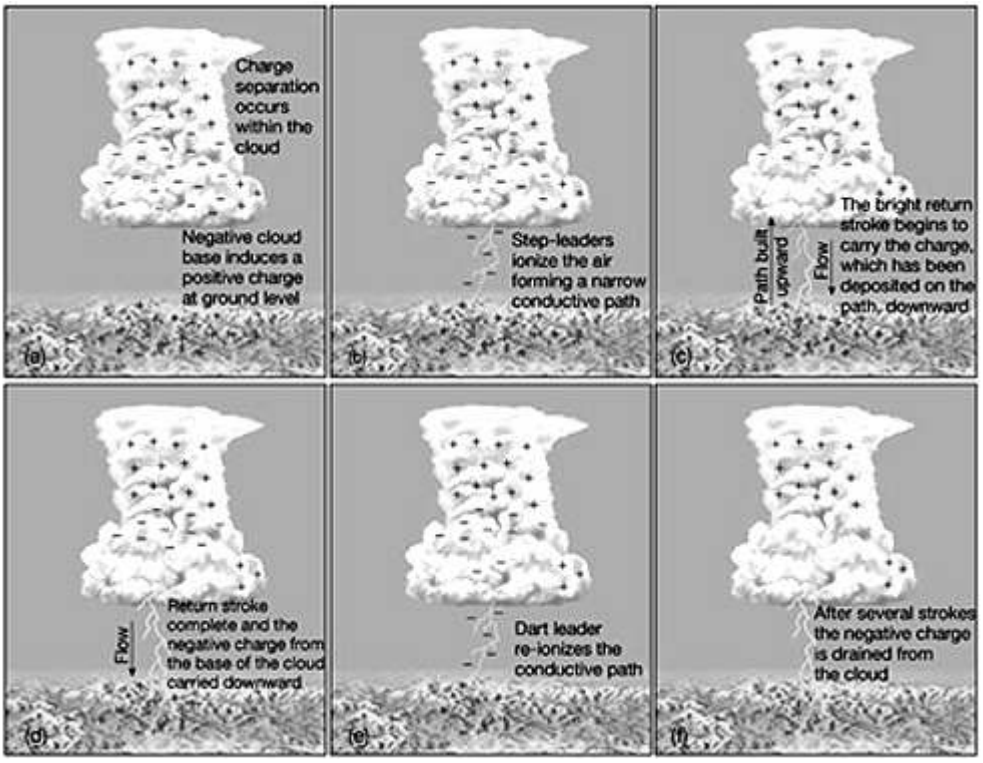


Figure 2.5: lightning stepped

Most faults on transmission lines of 100kV and higher are caused by lightning, which results in the flash over of insulators. Transmission lines faults are caused by, lightning, storm, fallen trees, Snow. One of the temporary faulty is cause by direst lightning phenomena. Where example of permanent fault is faults on electrical equipment.

2.4 ELCB Features

Figure 2.6 shows the ELCB inner build and cover, the function of this housing as the human protection for the circuit.

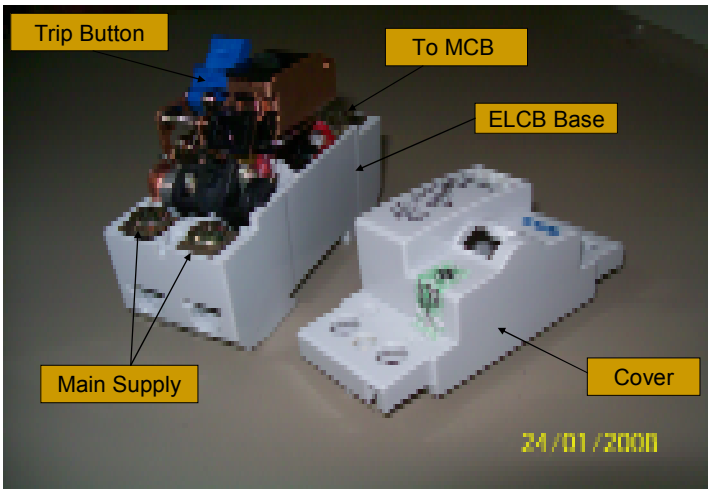


Figure 2.6: ELCB inner build and Cover.

Figure 2.7 shows the structure of ELCB that has been separated from its cover. From the figure we can see that ZCT act as the Sensor that connected to coil in the black box that which are part of the mechanical switch.

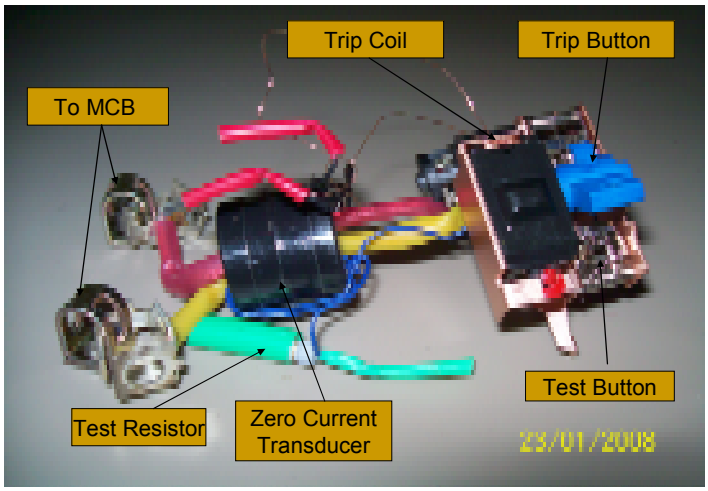


Figure 2.7: ELCB Structure

2.5 Operation of ELCB

Figure 2.8 shows the schematic design of ELCB, the design consists of mechanical switch, ZCT, coil, test resistor and the reset button. Mechanical switch is connected to the contact of black box. The function of this black box is to induced magnetic and then de-energize the magnetic coil in the black box. Then it will disconnect the mechanical switch so that it can cut off the power with cut off the life and neutral line together. The function of test resistor is to test whether ELCB is operational or not by providing a short circuit within internal ELCB life and neutral. By providing a new current path during test condition (assuming Kirchhoff current law), current flow through life wire is divided. The current in the neutral is less than the current in the life wire when the reset button is pushed.

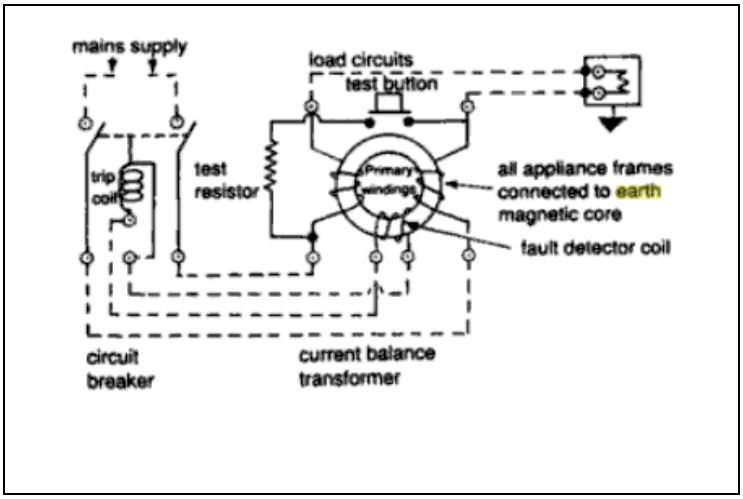


Figure 2.8: Earth Leakage Circuit Breaker design schematic

The function of ZCT is to detect the unbalance current from life and neutral or life with ground. The tripping of an ELCB is depending on the sensitivity of the ZCT. For resident, usually ELCB that is being used is 0.1A that means if there is any unbalance current ≥100mA, the ZCT will induced current and then de-energize the magnetic coil in the black box, so that the mechanical switch can be disconnected.

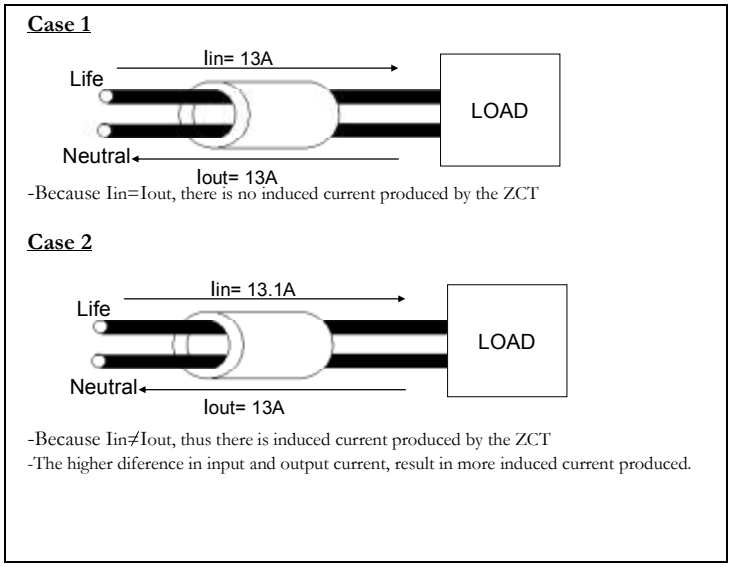


Figure 2.9: Operation of ZCT

Figure 2.9 shows the operation of the ZCT. Operation of ZCT is same like the Clamp Meter that is used to detect current in a line. In case 1, when the current flow through life and neutral line is same, there is no unbalance current detect in the ZCT thus there is no induced current produced by the ZCT. In case 2, when there is unbalance current between life and neutral line, ZCT will produced an induced current and then it will send to the signal to the magnetic coil resulting in tripping of the ELCB.

2.6 Summary

From this chapter, we can see that nowadays ELCB is already flawless in protection for human being from fatality hazard. Factor that effect the tripping of an ELCB is the sensitivity of the ZCT. Because the safety regulation of the ELCB from IEEE itself, we need to use these default setting of 100mA in our project, and only modified on switching and the circuit for the improving. This chapter gives a clear idea about what is need in this project. There is need to utilize ELCB with microprocessor as its brain, so that it can be operated with much more efficient. To develop this project, the knowledge about the controller which is ‘the brain’ for this system is very important. This project will use PIC micro controller as the processor. Thus, this will be discussed later in chapter 3 in detail.

CHAPTER 3

DEVELOPMENT OF EARTH LEAKAGE CIRCUIT BREAKER WITH AN AUTO RE-CLOSER UNIT

3.1 Introduction

This chapter explains how to design the Earth Leakage Circuit Breaker with an Auto Re-closer unit including project flow, circuit design, and hardware and software implementation. This chapter also will cover about designing the basic PIC circuit, keypad and LCD, current sensor circuit, interfacing PIC to circuit breaker and PIC programming.

This chapter also describes about final hardware design of auto re-closer circuit breaker, the advantages and the function of each circuit. The suitable modification is also being considered in order to make the ELCB can be integrated with PIC microcontroller and the hardware circuit. To make the new ELCB effective, several changed has been made so that the size and the cost is acceptable for commercial purpose.

3.2 Project Flow

This project starts with study the basic design of an ELCB. This is done by operating the original ELCB and takes a look at each component and their function. The next stage is to think what can be modified in order to change the ELCB function from mechanical switching to Electronic switching. Next is to identify where the suitable part to use the PIC microcontroller is. For this to happen, the first thing do is, by designing the basic of the circuit which are power supply circuit. Then follow by designing the controller circuit which is for PIC microcontroller to be operated. The next step is designing the electronic switching circuit which needs to be used instead of original mechanical switch. The last circuit need to be design is the sensor circuit that can sense any fault that occurred. Finally for the hardware need to be completed, all circuit need to be combined altogether and then troubleshooting can be made. After hardware is finished, programming can be made so that the ELCB function as auto Re-closer unit can be seen. Then the new Auto Re-closer ELCB was tested in laboratory using different method, when there were problems occur, the hardware is troubleshoot and the problem is correct. The process was done again until the hardware fully functions and meets the requirement of an ELCB.

3.3 ELCB Hardware Design

From the Figure 3.1 the basic build of an ELCB only consist 4 basic components, which are ZCT, “Black box”, Mechanical switch and Test Resistor. Functions of ZCT are to detect imbalance current in life and neutral wire that is installed through ZCT. If there are any unbalance current detected in ZCT, ZCT will induced current and then the induced current will be sent to “black box”. “Black box” basic build is a magnetic coil that is round by copper wire. When the Induced current from ZCT entered “Black Box”, magnetic coil in the “black box” is de-energized and then it will trigger the tripping mechanical switch.

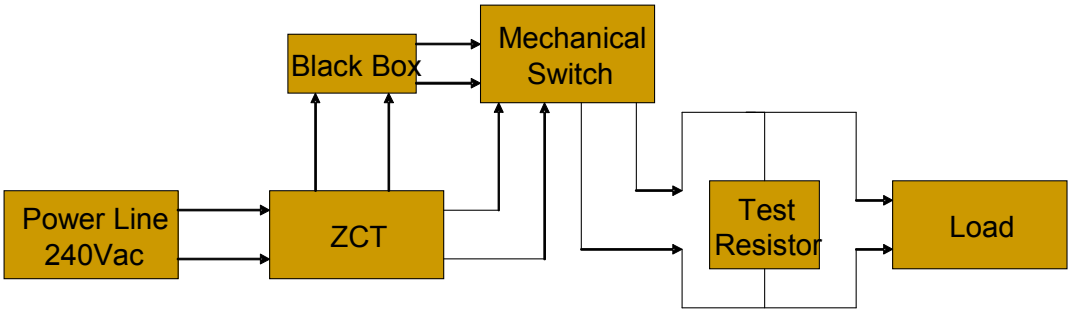


Figure 3.1: Component and Structure of ELCB

3.4 ELCB with an Auto Re-Closer Unit Hardware Design

From the Figure 3.2, the hardware is the improved design from basic ELCB in Figure 3.1 above. The Solid State Relay (SSR) replaced the function of mechanical switch in old ELCB. Function of Zero Current Transducer (ZCT) still the same which are to detect the unbalanced current between life and neutral line. Transformer 240/15 V ac is used and then it will be converting from 240 volt ac from power line to 5 volt dc by using full wave rectifier circuit. The 5 volt dc is used to energize PIC microcontroller, SSR, LCD (Liquid Crystal Display) and Operational Amplifier (op-Amp). As an early protection at control supply line, the fuse was used to blow the fuse over time if over-current occurs before entering circuit 5 volt dc supply.

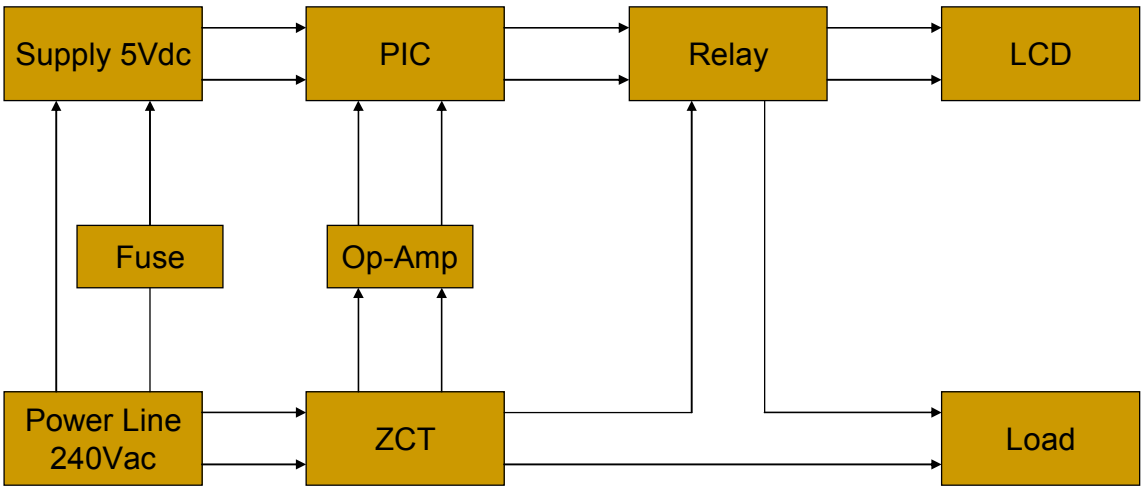


Figure 3.2: Component and Structure of ELCB with an Auto Re-closer unit

For IC Voltage Regulator, the model of LM7805 was used to step down the voltage from 15V of Transformer to 5V for PIC, LCD, Op-Amp and SSR. The function of current transducer is to detect the different current between life and neutral wire and then send the signal to the microcontroller in shape of induced current.

For the control component, PIC that is used is PIC18F4550. SSR is selected as switching is because the reliability of the SSR itself as Electronic switch that can be operated at high voltage and current. For sensing circuit, LM358 Op-Amp is selected as current to voltage converter. LM358 will detect the current from ZCT and then it will convert to voltage signal to send it to PIC18F4550.

3.5 Stage 1 Circuit

Refer to the Figure 3.3 it is 5 volt power supply circuit, this circuit is the combination from one transformer 240Vac/12Vac, Bridge Rectifier, LM7805, capacitor 470uF and capacitor 10uF. The LM7805 was used in voltage regulator circuit, it is to produce $5V_{dc}$ output to supply the power to PIC microcontroller circuit, LCD, SSR and sensing circuit. The detailed will be explained later in chapter 4.

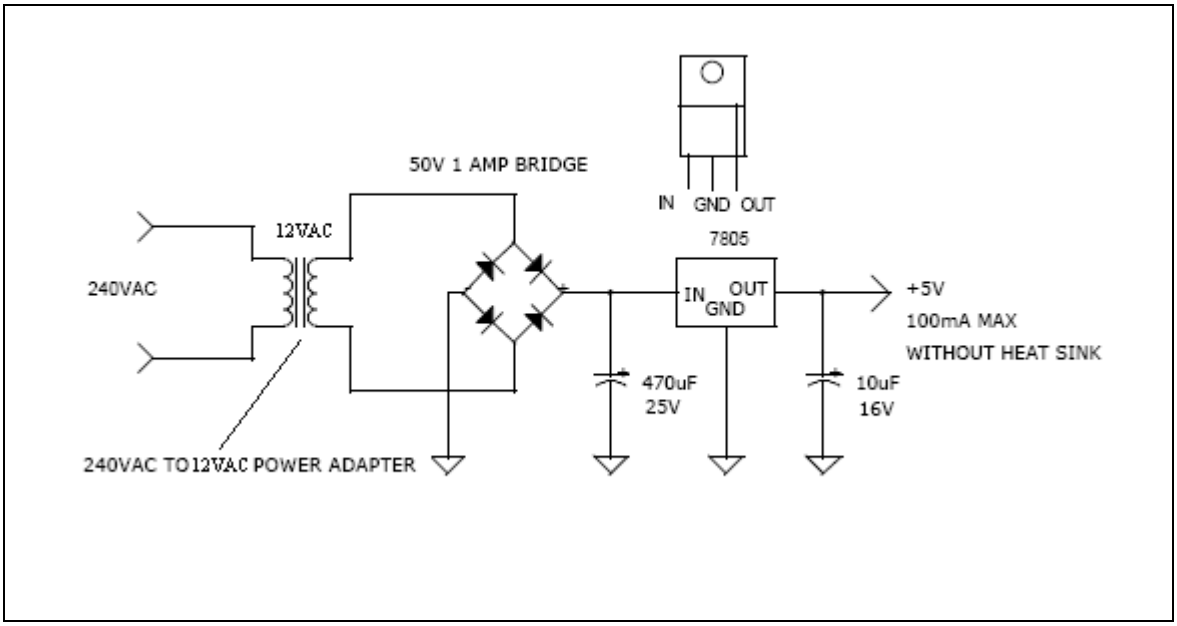


Figure 3.3: 5Vdc Power Supply Circuit

3.6 Stage 2 Circuit

Refer to the Figure 3.4 it is control element circuit for PIC microcontroller and LCD display, this circuit is the combination from one PIC18f4550 microprocessor and JHD162A LCD. Figure 3.5 show the pin connection between PIC18F4550 and LCD. PIC18F4550 act as the brain of the system, meanwhile JHD162A act as display for information from PIC. For PIC driver 20MHz crystal is used to control the clock cycle of the system. Both PIC and LCD used 5 Volt dc as supply voltage which can be connect to power supply circuit that have been design in page before. Capacitor 1nF is used as to filter the voltage came from sensing circuit. The detailed is described in Chapter 4.

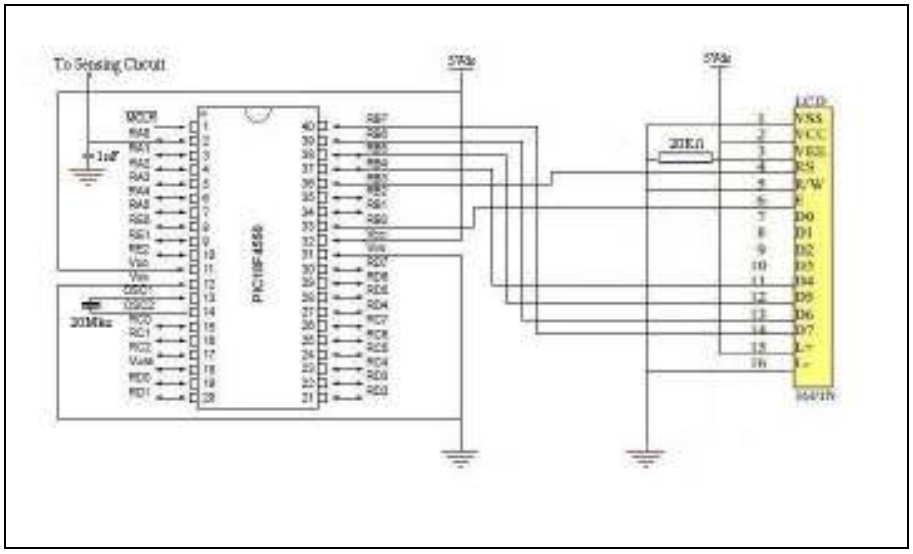


Figure 3.4: PIC Microcontroller and LCD circuit

Table 3.5: Pin connected to PIC16F877A over current relay system

Pin Name	Pin No.	Description	Application
VDD	11, 32	Positive supply (+5V)	Power supply to PIC
VSS	12, 31	Ground references	Ground references
MCLR	1	Input	For reset button
OSC1,OSC2	13, 14	For oscillator	Connected to 20MHz crystal
RA0/AN0	2	Analog input	Analog input from Sensing Circuit LM358
RB0, RB3-RB7	33, 36, 37, 38, 39, 40	Output	Connected to LCD data (DB0-DB7)
RB2	35	Output to 5V relay	To trip circuit breaker
RD1	20	Output	To on Buzzer

Tables 3.5 show the connection pin use for PIC18F4550 microcontroller. The total pin used for PIC18F4550 is 15-pin. Pin 11 and 13 is used for receiving 5V supply meanwhile pin 12 and 31 is connected to the ground. Pin 1 is used for master reset, this pin mainly used to reset the PIC18F4550 microcontroller operation. OSC1 and OSC2 is connected to the oscillator 20MHz which are the clock for the PIC18F4550 microcontroller. RA0 is the pin for the analog input, this pin used to convert the analog signal from sensing circuit to the digital signal so that PIC18F4550 can make the conversion. Port B and Pin for Port D is as the output pin for LCD, buzzer and Solid State Relay.

3.7 Stage 3 Circuit

Refer to the Figure 3.6 it is sensing circuit for the new ELCB. This circuit is operated based on current to voltage converter using LM358 Op-Amp. Resistor 150Ω is used to convert the induced current from ZCT to induced voltage. Variable resistor 20K is used to vary the output voltage LM358 with the induced current. The detail will be explained later in chapter 4.

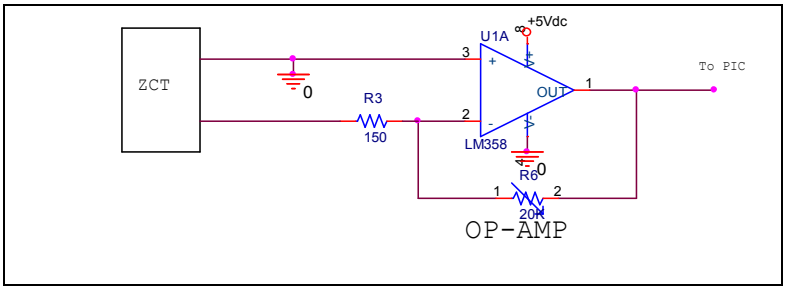


Figure 3.6: Current to Voltage Converter using LM358

3.7.1 Solid State Relay

Refer to the Figure 3.7 the Solid State Relays (SSR) which is an electronic switch, which, unlike an electromechanical relay, contains no moving parts. A SSR is a semiconductor device that can be used in place of a mechanical relay to switch electricity to a load in many applications. SSRR are purely electronic, normally composed of a low current “control” side (equivalent to the coil on an electromechanical relay) and a high-current load side (equivalent to the contact on a conventional relay). SSR typically also feature electrical isolation to several thousand volts between the control and load sides. Because of this isolation, the load side of the relay is actually powered by the switched line, both line voltage and a load must be present for the relay to operate.

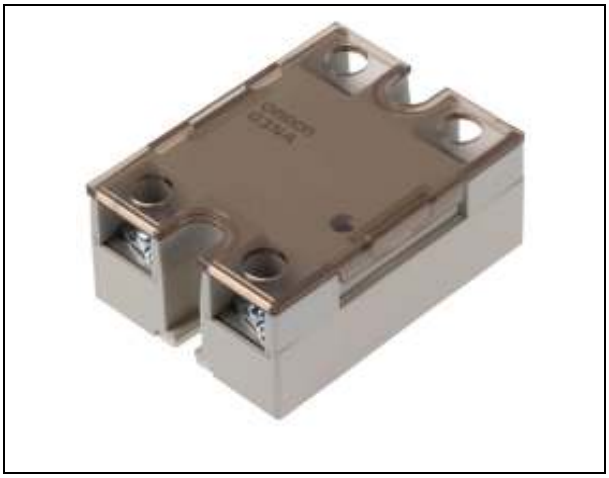


Figure 3.7: Solid State Relay (SSR)

SSR are faster than electromechanical relays; their switching time is dependent on the time needed to power the LED on and off, on the order of microseconds to milliseconds. SSR increased lifetime due to the fact that there are no moving parts, and thus no wear. SSR also decreased electrical noise when switching with totally silent operation.

There are many applications that require a moderate amount of power (W to kW) to be switched on and off fairly rapidly. A good example would be the operation of a heater element in a controlled-temperature system. Typically, the amount of heat put into the system is regulated using pulse-width modulation turning a fixed-power heating element on and off for time periods ranging from seconds to minutes. Mechanical relays have a finite cycle life, as their components tend to wear out over thousands to millions of cycles. SSR do not have this problem; in the proper application, they could be operated almost infinitely.

This project the use the SSR with specification:

Description

- Solid-State Panel Mount Relay
- Series:G3NA
- Control Voltage Type: DC
- Load Current RMS Max:40A
- Load Voltage RMS Max:240VAC
- Load Voltage RMS Min:24VAC
- Contacts: SPST-NO
- Control Voltage Max:24V
- Control Voltage Min:5V

3.7.2 Zero phase Current Transformers (ZCT)

Figure 3.8 shows the ZCT, A zero-phase current transformer for use as a leakage current detecting element in a leakage current interrupter in which two magnetic materials of different permeabilities are provided so as to eliminate a range where the leakage current interrupter is inoperable without lowering its ability to distinguish noise components. The different magnetic materials may be provided as a single core constructed by mixing the materials of different permeabilities. Otherwise, the materials can be provided as annually-shaped magnetic pieces stacked one on top of the other. Still further, the materials of different magnetic permeability may be provided as bands of materials interwound to form alternating layers or one of the materials may be provided as at least a portion of a protective case. For this project, the sensitivity of ZCT is 100mA.

Figure 3.8: Zero phase Current Transformers

3.7.3 Centre tap Transformer 240Vac/12Vac

Figure 3.9 shows the centre tap Transformer, it is one type of transformer that used to reduce the voltage from 230Vac to 12Vac and supply the voltage to the power supply circuit. It is the most comprehensive choice of secondary voltages. It also is flame retardant bobbins and shrouds. Besides, fully shrouded construction

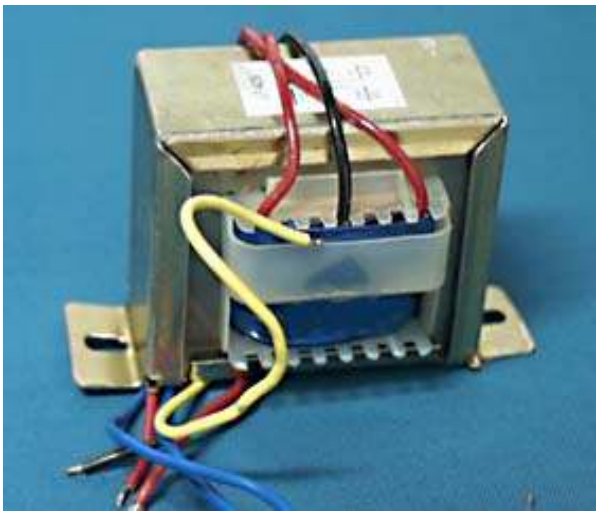


Figure 3.9: Centre Tap Transformer

3.7.4 Voltage Regulator LM7805

Figure 3.10 shows the model of UTC LM 7805. The UTC LM78XX family is monolithic fixed voltage regulator integrated circuit. They are suitable for applications that required supply current up to 1 A.

Figure 3.10: LM7805

The UTC LM79XX series of three-terminal negative regulators are available in TO-220 package and with several fixed output voltage, making them useful in a wide range of application. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible.

3.7.5 Bridge

Refer to the Figure 3.11 it is the KBPC6005PBF Bridge model, it is used to rectify the voltage from AC supply to DC power supply for IC voltage regulator device.

Figure 3.11: Bridge

3.7.6 Toggle Switch

Figure 3.12 shows the toggle Switch, it is the main switch for the whole circuit. The function of this Main switch is to open and closed the whole system. This switch functions manually.

Figure 3.12: Toggle Switch

3.7.7 Operational Amplifier LM358

Figure 3.13 shows the Operational Amplifier or Op-Amp LM358, the LM358 model is a high performance monolithic operational amplifier constructed on a single silicon chip. It is intended for a wide range of analog applications, example:

a) AC coupled Inverting Amplifier
b) AC coupled Non-Inverting Amplifier
c) Non-inverting DC Amplifier
d) DC Summing Amplifier
e) High Input Impedance, DC deferential Amplifier
f) Active Band-Pass Filter
g) Low Drift Peak Detector
h) Current to voltage converter
i) Voltage to current converter

The LM358 is the high gain and wide ranges of operating voltages provide superior performances in integrator, summing amplifier and general feedback applications. The internal compensation network (6dB/ octave) insures stability in closed loop circuits. Figure 3.13 shows that LM358 from MOTOROLLA family.

Figure 3.13: LM358

The LM358 is the MOTOROLA model of Op-Amp that used in this ELCB circuit, it is used for current to voltage converter, the function of this circuit is to convert the current from zero phase current transformers (ZCT) to voltage and the voltage will be sent to PIC18F4550 microcontroller and the voltage classified as input for microcontroller element.

3.7.8 Light Emitting Diode

Figure 3.14 shows green and red light-emitting-diode (LED), LED is based on the semiconductor diode. When the diode is forward biased (switched on), electrons are able to recombine with holes and energy is released in the form of light. This effect is called electroluminescence and the color of the light is determined by the energy gap of the semiconductor.

Figure 3.14: Light Emitting Diode (LED)

In this project, the red LED was used to show that there are supply voltage entering the whole circuit. Meanwhile yellow LED used to indicate when the solid state relay is operated.

3.7.9 Liquid Crystal Display

A liquid crystal display (LCD) is an electronically-modulated optical device shaped into a thin, flat panel made up of any number of color or monochrome pixels filled with liquid crystals and arrayed in front of a light source (backlight) or reflector. It is often utilized in battery-powered electronic devices because it uses very small amounts of electric power. Figure 3.15 show the LCD model JHD162A SERIES that is used for this project.

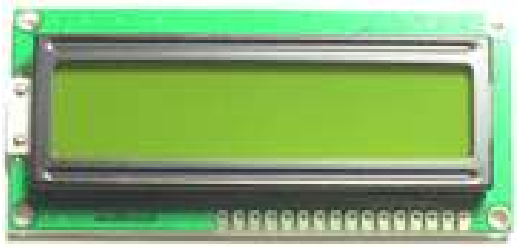


Figure 3.15: Liquid Crystal Display

Each pixel of an LCD typically consists of a layer of molecules aligned between two transparent electrodes, and two polarizing filters, the axes of transmission of which are (in most of the cases) perpendicular to each other. With no actual liquid crystal between the polarizing filters, light passing through the first filter would be blocked by the second (crossed) polarizer.

LCD with a small number of segments, such as those used in digital watches and pocket calculators, has individual electrical contacts for each segment. An external dedicated circuit supplies an electric charge to control each segment. This display structure is unwieldy for more than a few display elements.

3.8 Final Stage Circuit

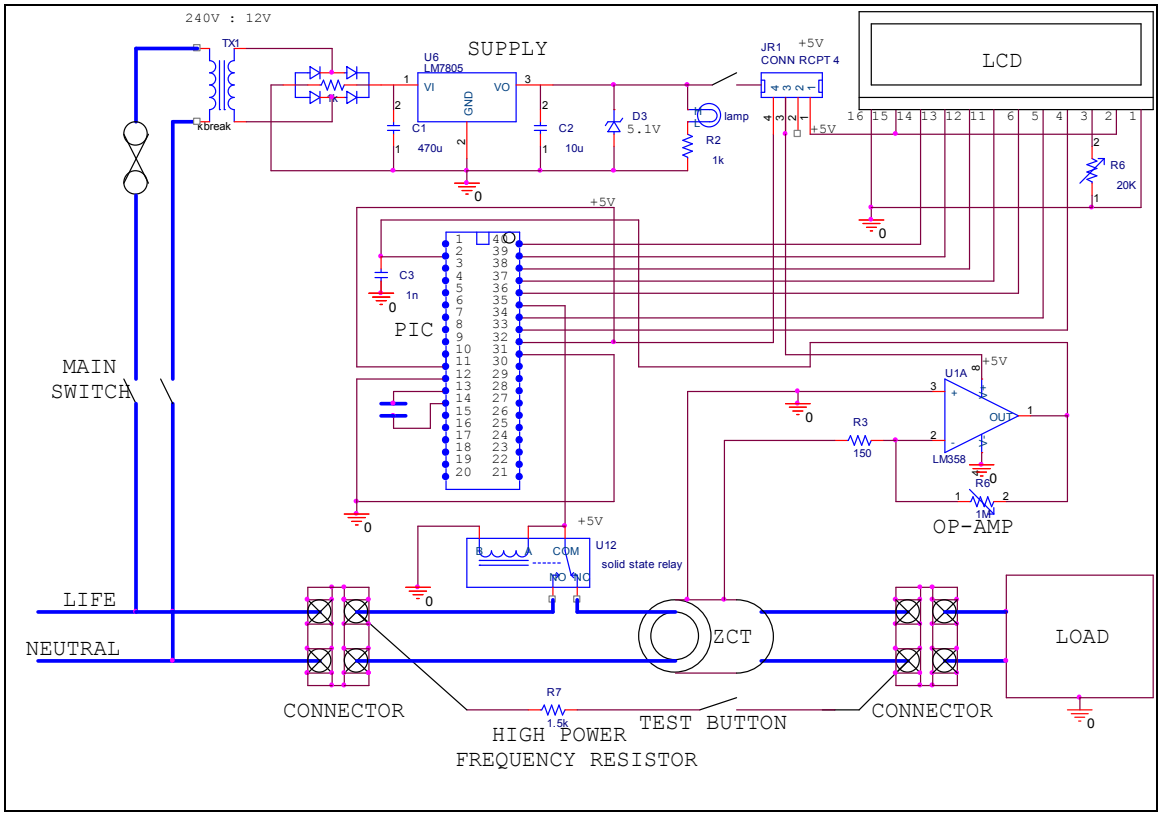


Figure 3.16: Final Stage Circuit

Figure 3.16 show the final stage circuit. By combining the entire component with all the earlier circuit, we get the final stage circuit which is the hardware design for ELCB with an auto re-closer unit. Every stage circuit can be integrating together, soon after the Hardware circuit is complete, and the hardware is test and being troubleshoot. By doing this, the Hardware can process can be done before entering the next phase which are programming.

It is important to have a finished hardware, so that the next phase can be done without problem that came from hardware that needs to be troubleshooting.

3.9 Flow Chart

Refer to the Figure 3.17, when a fault occur ZCT will sense the imbalance current and then it will induced a signal current. This signal then is send to the PIC microcontroller via sensing circuit. PIC microcontroller then will send signal to trip the ELCB. At this moment the counter in the PIC will start count as 1. After 10 second, the ELCB will automatically switch back to normal condition. If there is no fault detect after the ELCB is turn on the LCD will display temporary fault and the ELCB will stay connected until next fault occurred and the counter will be reset. Meanwhile if there is fault occurred instantly after the ELCB is turning back to on, the ZCT will detect the imbalance current and then will send back the signal to PIC. The ELCB then will turn on back after being trip. At this time PIC counter will count as 2, this process will be cycle until the counter reach 3. After PIC counter reach 3, PIC microcontroller will identify the fault as permanent fault such like short circuit and over-current. The ELCB then will be tripped as to isolated connection of load with power line.

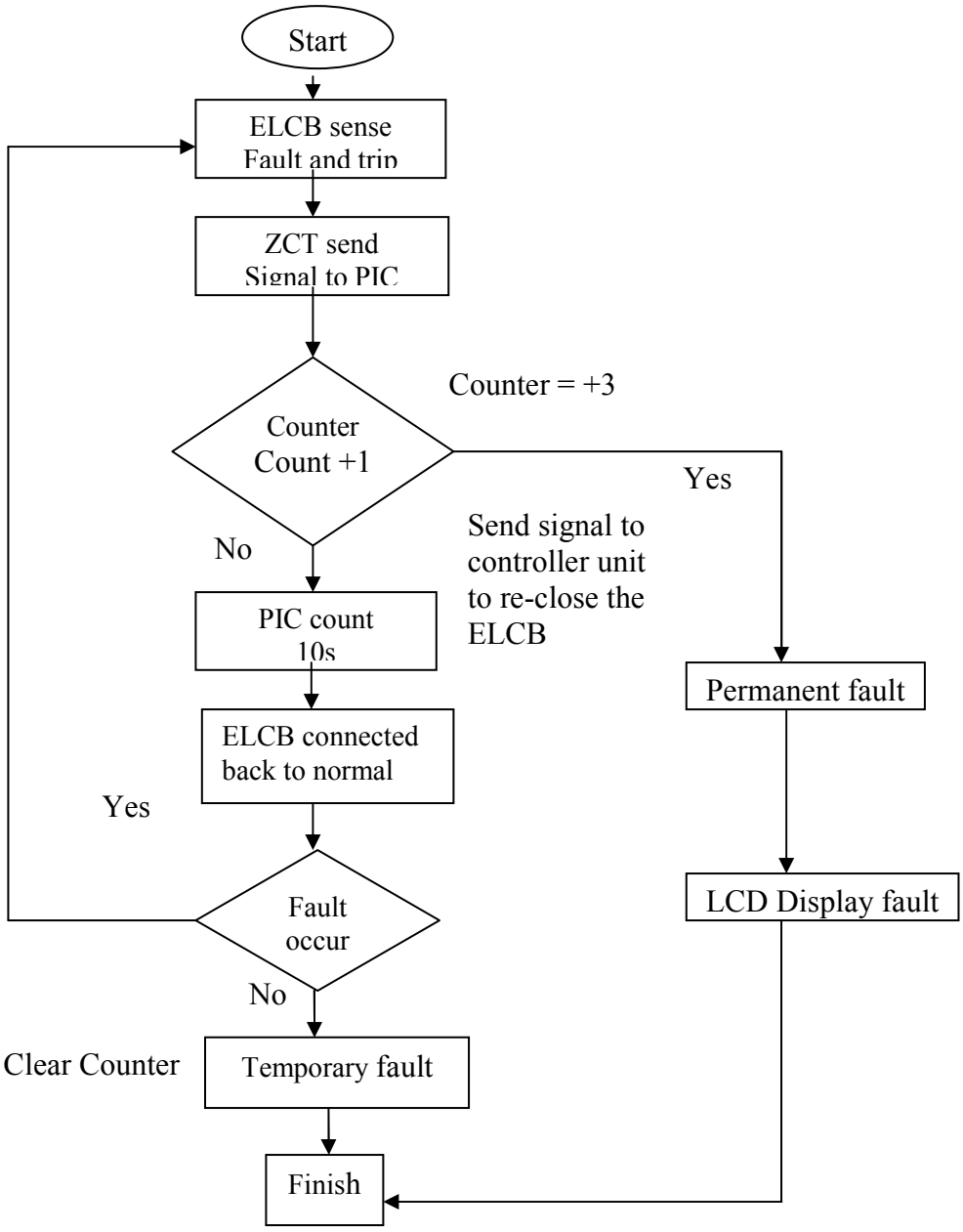


Figure 3.17: Flow chart of the system

3.10 Hardware Operation Process

From the flow on the Figure 3.18, started with the supply voltage from TNB, then the supply 240V ac is connect to the load through ZCT. ZCT used to detect imbalance current that flow from life and neutral power line. Supply voltage from TNB is also connected to power supply circuit which is to step down from 240V ac to 12V ac and the rectified and regulate it to be 5 V dc by using bridge and Voltage regulator. The 5 volt dc is used to energize PIC microcontroller, SSR, LCD and Operational Amplifier (op-Amp). From ZCT, if the unbalanced current between life and neutral line occurred and the value between them reached Δ100mA, ZCT will induced an induced current and then the current signal is convert to voltage signal by using Op-Amp current to voltage converter circuit. The value of the output from sensing circuit is depending on the value of Op-Amp gain. The more different current, the more current is induced by ZCT. The output voltage from Op-Amp is send to PIC microcontroller through ADC (Analog Digital Converter) port. As the ELCB main switching, Solid State Relay is connected from PIC port B. When fault occurred, PIC will detect the range of resolution that suitable for the condition of ELCB to trip when the imbalance current exceed Δ100mA, which is the minimum current value for the ELCB to trip. SSR then will be de-energized by the PIC and thus the ELCB is disconnected from the power line. During this time, LCD will be display the information of fault from the PIC microcontroller.

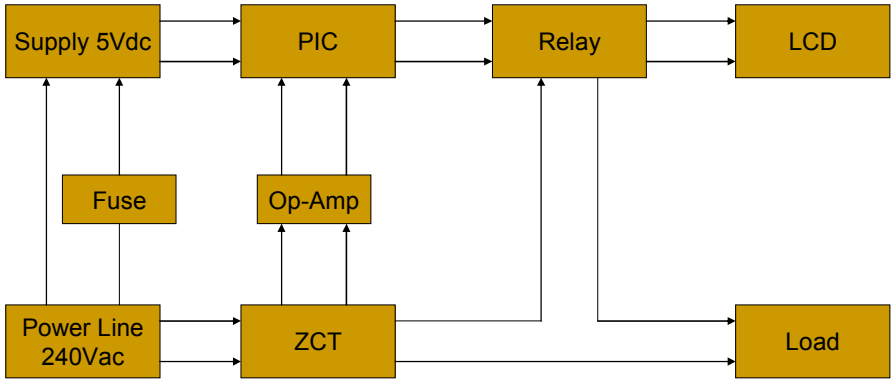


Figure 3.18: Hardware operation process of Auto Re-Closer ELCB

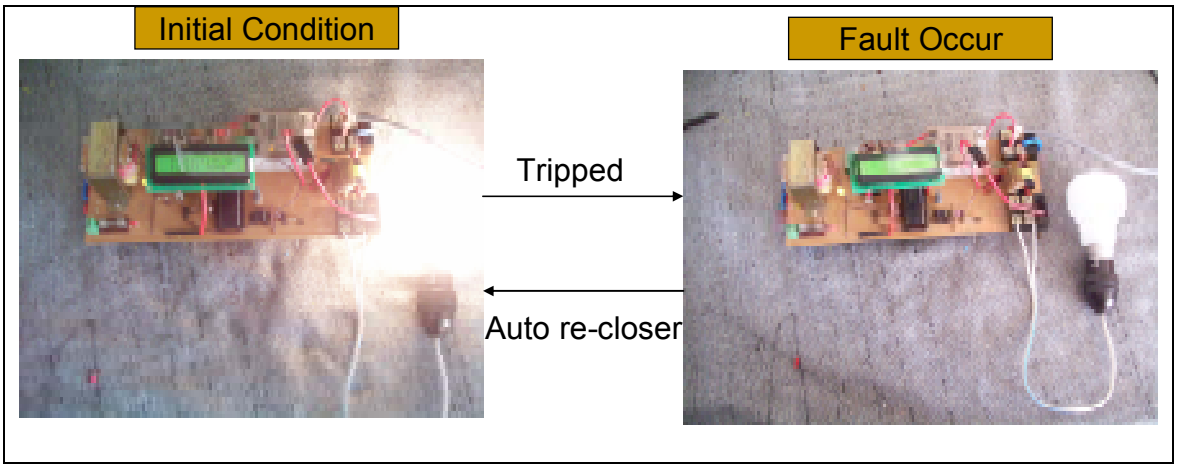


Figure 3.19: Operation of ELCB with an Auto Re-Closer unit.

3.11 Summary

The concept and method development of ELCB with an auto re-closer unit have been described in this chapter. ELCB is the main output of this project which is to isolate the faulty condition (fault current) while LCD will monitor and display the fault condition. All the circuit in this project will be controlled by PIC micro controller which acts as the processor in this project. The PIC micro controller will do the task and operate depend to the current that being sensed. It is very important to implement the hardware stage by stage so that it will be easy to troubleshoot if there's a problem. The most important thing is to make sure that the PIC micro controller can constantly operate and functioning so that it will keep all circuits runs.

CHAPTER 4

CONTROL ELEMENT CIRCUIT

4.1 Introduction

Control circuit act like the brain of the system. In this system the PIC18F4550 model has been selected as microcontroller. During earlier stage, PIC16F84A has been chosen because of the size and price but because it lack the input port for analog digital converter, so PIC18F4550 is the better choice. PIC18F4550 is 10-bit, up to 13-channel Analog-to-Digital Converter module (A/D) with Programmable Acquisition Time. PIC18F4550 microcontrollers use flash technology to allow rapid erasing and reprogramming to speed program debugging. PIC18F4550 offer twelve different oscillator options, allowing users a wide range of choices in developing application hardware. With the click of the mouse in the programming software, the flash PIC micro MCU can be instantly erased and then reprogrammed again and again. PIC18F4550 have large amounts of RAM memory for buffering and Enhanced Flash program memory thus make it ideal for embedded control and monitoring applications that require periodic connection with a (legacy free) personal computer via USB for data upload or download and firmware updates. Programming the PIC18F4550 is done by using C-language. Besides, Microcode Studio software has been used to write the programming coding of the PIC. Finally compile this type of programming language, the use of PIC Basic Compiler have been used.

4.2 Microcontroller Feature

PIC is a family of Harvard architecture microcontrollers made by Microchip Technology, derived from the PIC1640 originally developed by General Instrument's Microelectronics Division. The name PIC initially referred to "Programmable Interface Controller", but shortly thereafter was renamed "Programmable Intelligent Computer".

PIC are popular with developers and hobbyists alike due to their low cost, wide availability, large user base, extensive collection of application notes, availability of low cost or free development tools, and serial programming (and reprogramming with flash memory) capability.

PIC microcontrollers are frequently used in automatically controlled products and devices, such as automobile engine control systems, remote controls, office machines, appliances, power tools, and toys. By reducing the size, cost, and power consumption compared to a design using a separate microprocessor, memory, and input/output devices, microcontrollers make it economical to electronically control many more electrical and mechanical devices.

Figure 4.1, 4.2 and 4.3 shows the PIC18F4550 Pin PIC Microcontroller picture, except this type the PIC18F4550 44-Pin Thin Quad Flat Pack (TQFP) and 44-Pin Quad Flat No leads (QFN) also available. For this project the 40-pin plastic dual in-line package (PDip) microcontroller has been used.

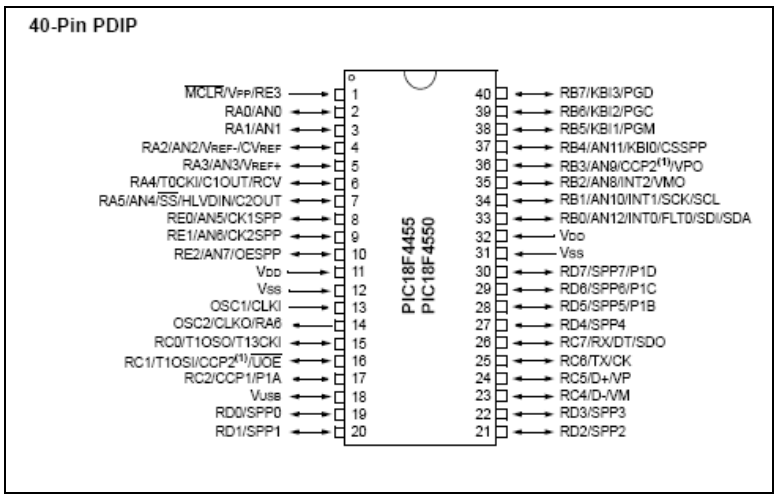


Figure 4.1: 40-Pin PDip Microcontroller

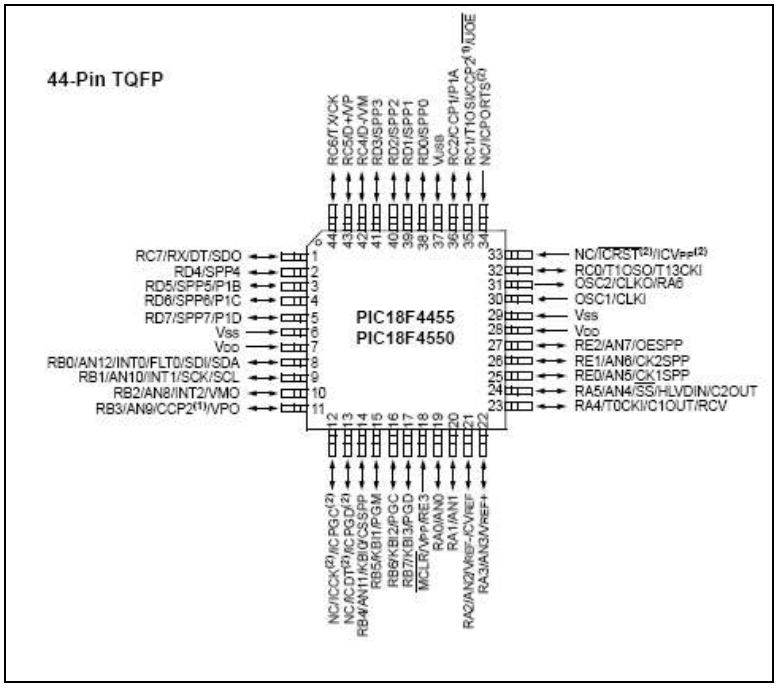


Figure 4.2: 44-Pin TQFP Microcontrollers

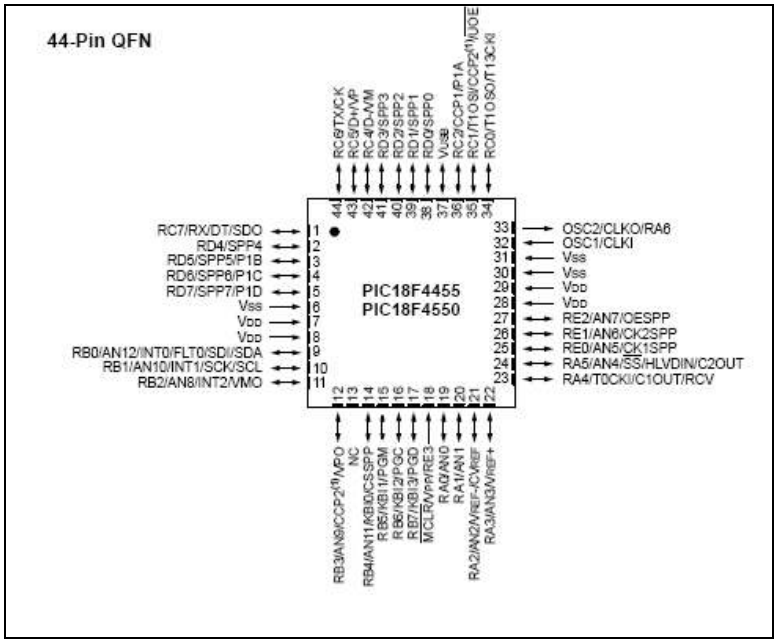


Figure 4.3: 44-Pin QFN Microcontrollers

4.2.1 PIC18F4550 Features

The features of the microcontroller are as follows:

- Full Speed USB 2.0 (12Mbit/s) interface
- 1K byte Dual Port RAM + 1K byte GP RAM
- Full Speed Transceiver
- 16 Endpoints (IN/OUT)
- Streaming Port
- Internal Pull Up resistors (D+/D-)
- 48 MHz performance (12 MIPS)

Figure 4.4: PIC18F4550 Microcontroller

Table 4.5: PIC18f4550 Features

Parameter Name	**Value**
Program Memory Type	Flash
Program Memory (KB)	32
CPU Speed (MIPS)	12
RAM Bytes	2,048
Data EEPROM (bytes)	256
Digital Communication Peripherals	1-A/E/USART, 1-MSSP(SPI/I2C)
Capture/Compare/PWM Peripherals	1 CCP, 1 ECCP
Timers	1 x 8-bit, 3 x 16-bit
ADC	13 ch, 10-bit
Comparators	2
USB (ch, speed, compliance)	1, Full Speed, USB 2.0
Temperature Range (C)	-40 to 85
Operating Voltage Range (V)	2 to 5.5
Pin Count	40
Packages	40 PDIP, 44 TQFP, 44 QFN
I/O pins	34

Table 4.6: PIC18f4550 pin used detail

Pin Name	Pin Number PDIP, SOIC	Pin Type	Buffer Type	Description
MCLR/VPP/RE3	1			Master Clear (input) or programming voltage (input).
MCLR		I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP		P		Programming voltage input.
RE3		I	ST	Digital input.
OSC1/CLKI	9			Oscillator crystal or external clock input.
OSC1		I	Analog	Oscillator crystal input or external clock source input.
CLKI		I	Analog	External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)
OSC2/CLKO/RA6	10			Oscillator crystal or clock output.
OSC2		O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO		O	—	In select modes, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6		I/O	TTL	General purpose I/O pin.
				PORTA is a bidirectional I/O port.
RA0/AN0	2			
RA0		I/O	TTL	Digital I/O.
AN0		I	Analog	Analog input 0.
RA1/AN1	3			
RA1		I/O	TTL	Digital I/O.
AN1		I	Analog	Analog input 1.
RA2/AN2/VREF-/CVREF	4			
RA2		I/O	TTL	Digital I/O.
AN2		I	Analog	Analog input 2.
VREF-		I	Analog	A/D reference voltage (low) input.
CVREF		O	Analog	Analog comparator reference output.
RA3/AN3/VREF+	5			
RA3		I/O	TTL	Digital I/O.
AN3		I	Analog	Analog input 3.
VREF+		I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/C1OUT/RCV	6			
RA4		I/O	ST	Digital I/O.
T0CKI		I	ST	Timer0 external clock input.
C1OUT		O	—	Comparator 1 output.
RCV		I	TTL	External USB transceiver RCV input.
RA5/AN4/SS/ HLVDIN/C2OUT	7			
RA5		I/O	TTL	Digital I/O.
AN4		I	Analog	Analog input 4.
SS		I	TTL	SPI slave select input.
HLVDIN		I	Analog	High/Low-Voltage Detect input.
C2OUT		O	—	Comparator 2 output.
RA6	—	—	—	See the OSC2/CLKO/RA6 pin.

4.2.2 Input and Output Port Used

This subchapter is described about the input port and output port that has been used in the development of ELCB project. PIC18F4550 have 5 ports which are port A, port B, port C, port D and port E. PIC18F4550 has advantage in term of port because we can assign any port as input or output. But the restriction is only on port B, C, D and E because port A is analog port. Currently there is only port A, port B and port D is used and The other port is currently unoccupied because it is reserve for future upgrade.

For port B, it is assign as an output for the LCD. Since there are 8 port B counts from RB0 to RB7, the LCD is easy to be configured by using port B. LCD is using port B0 as to connect to E, port B3 is connect to RS and port B4 to port B7 to connect to data port D4 to D7 on LCD. There is one port B used as an output to control Solid State Relay which is port B2.

For Port A, the only analog port that is used is port A1. This port is use as the input analog digital converter from output sensing circuit. In writing C-language for port A, we need to assign ADCIN and ADCON for the analog port to be active.

Lastly for port D, port D1 is used as an output for Buzzer. Whenever the ELCB is tripped this port D1 will send signal High as to turn on the buzzer and to notify the user that the ELCB is being tripped.

4.2.3 Crystal oscillator

Refer to Figure 4.7, crystal oscillator is an electronic circuit that uses the mechanical resonance of a vibrating crystal of piezoelectric material to create an electrical signal with a very precise frequency. This frequency is commonly used to keep track of time (as in quartz wristwatches), to provide a stable clock signal for digital integrated circuits, and to stabilize frequencies for radio transmitters and receivers. The most common type of piezoelectric resonator used is the quartz crystal. The suitable crystal for this project considered is 20 MHz.

Figure 4.7: Crystal oscillator

4.3 Software and Hardware Implementation

This section will discuss about software which has been implemented in this project which are PicBasic Pro Compilers (MicroCode Studio) for programming PIC18F4550, OrCAD Capture CIS for designing the circuit and PicBasic Pro Compilers (Micro Code Studio) for the programming and also Cytron Programmer for writing the programming language into the PICF4550.

4.3.1 Microcode Studio

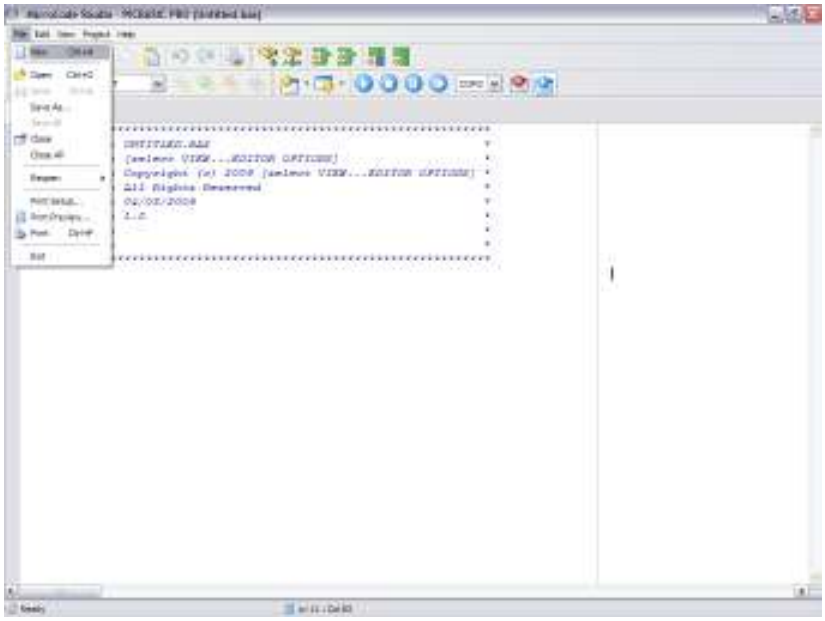
MicroCode Studio is a powerful, visual Integrated Development Environment (IDE) with In Circuit Debugging (ICD) capability designed specifically for microEngineering Labs PICBASIC™ and PICBASIC PRO™ compiler.

The main editor provides full syntax highlighting of your code with context sensitive keyword help and syntax hints. The code explorer allows you to automatically jump to include files, defines, constants, variables, aliases and modifiers, symbols and labels, which are contained within your source code. Full cut, copy, paste and undo is provided, together with search and replace features.

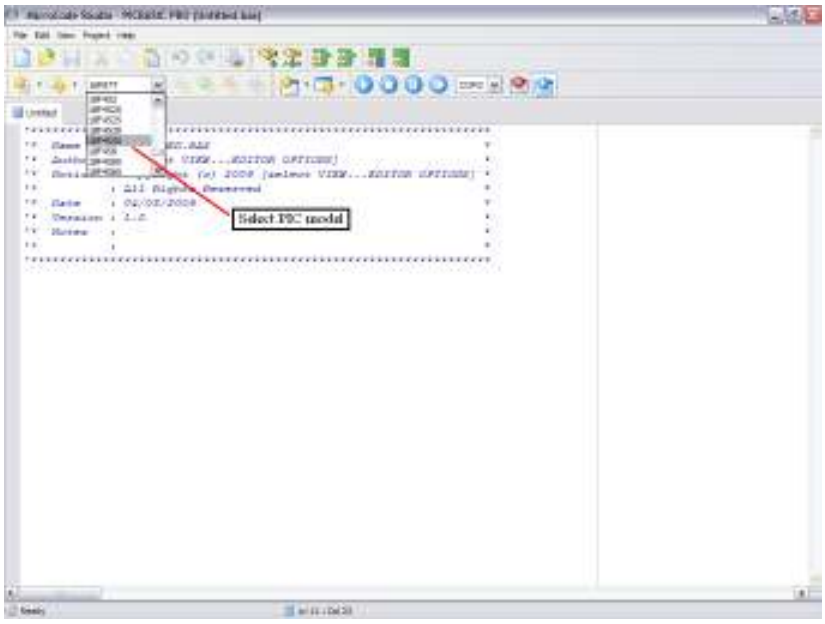
- Full syntax highlighting of your source code
- Quickly jump to include files, symbols, defines, variables and labels using the code explorer window
- Identify and correct compilation and assembler errors
- View serial output from your microcontroller
- Keyword based context sensitive help
- Support for MPASM

Below is the step to use the using MicroCode Studio software in ELCB project:

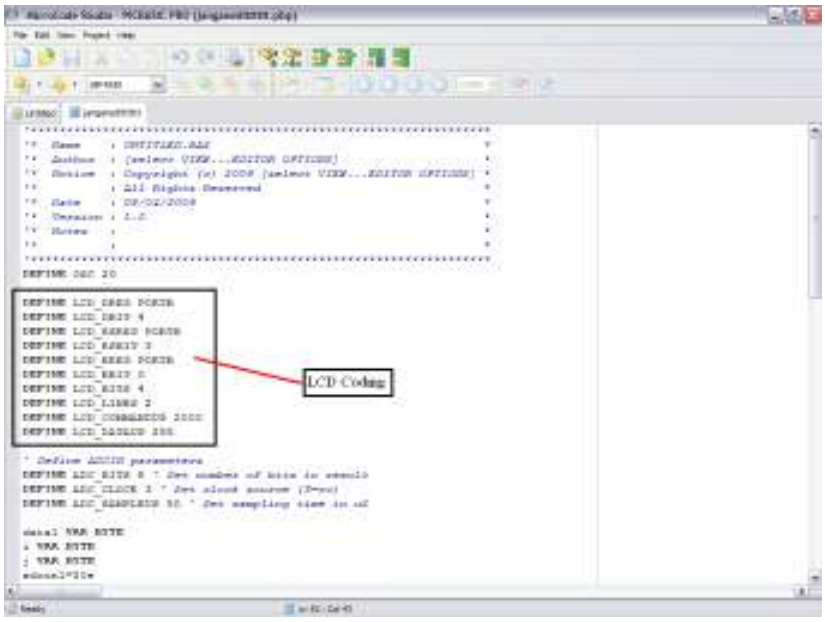
Step 1 : Opening New File



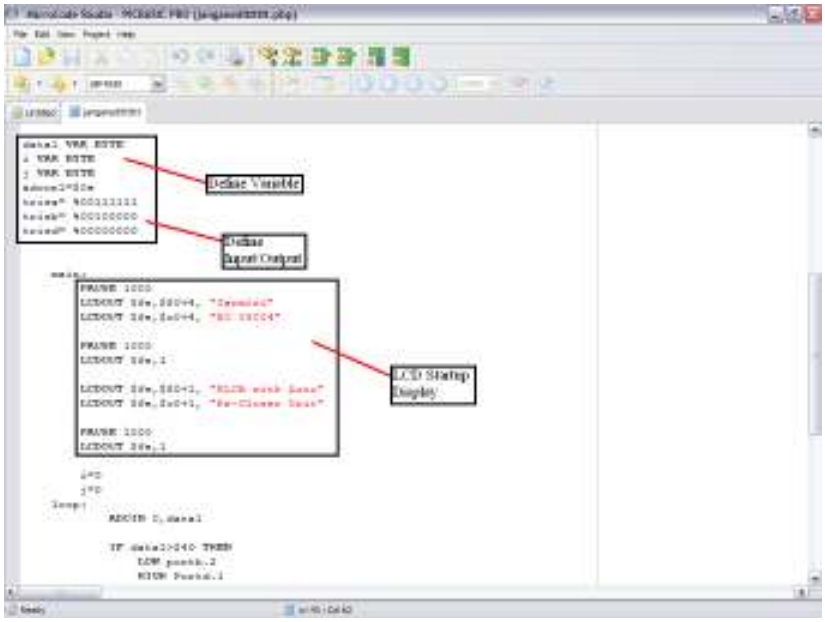
Step 2: Selecting PIC Model



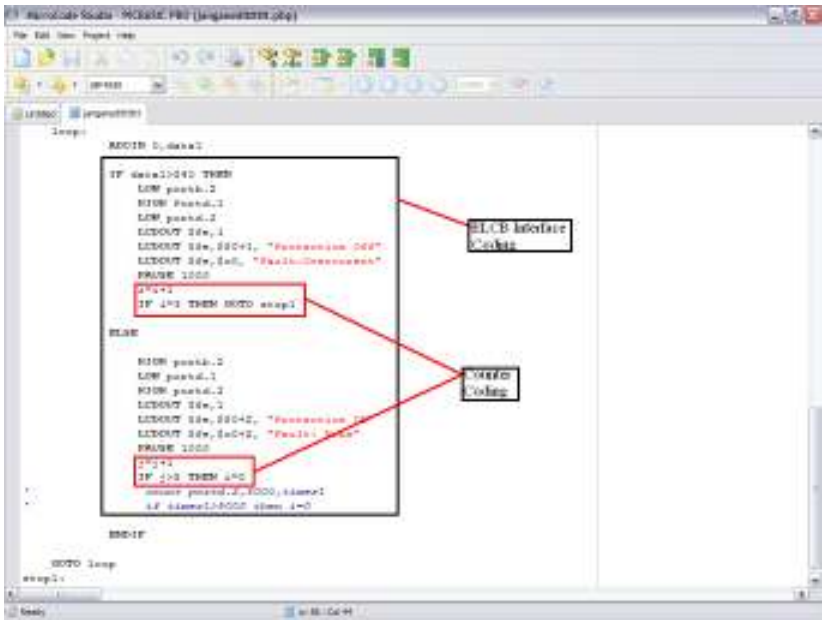
Step 3: LCD Coding



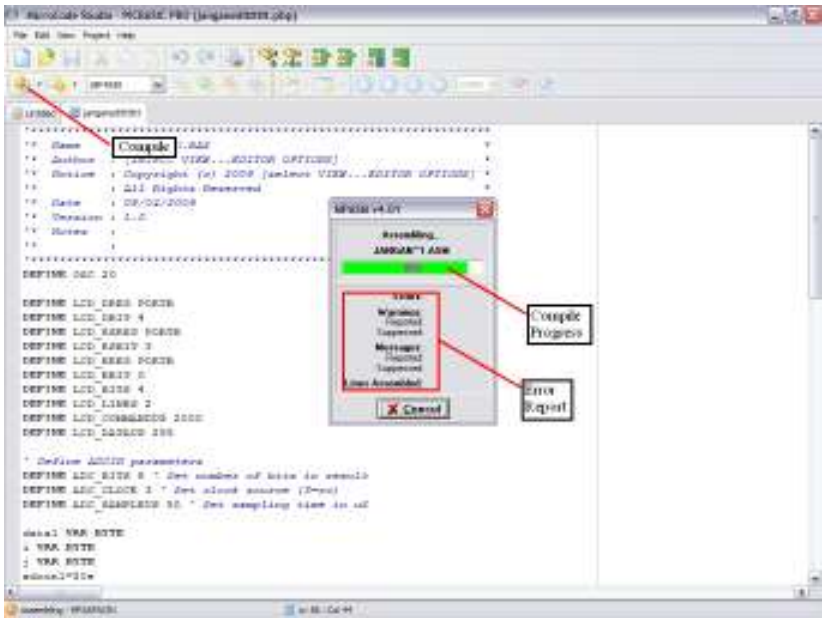
Step 4: Define Variable & LCD Display



Step 5: Programming ELCB & Counter



Step 6: Compile Program & Error Checking



After all steps above is done, the PIC is ready to write by using CYTRON USB Programmer.

4.3.2 CYTRON USB Programmer

UP00A model CYTRON USB programmer comes with PIC programmer hardware and also WinPic800 software. Both hardware and software are use as a medium to write the C-language in the PIC18F4550. CYTRON USB programmer UP00A provides an effective and low-cost solution in developing wide range of Microchip PIC microcontroller. It is a compact yet powerful programmer that can be used in either desktop PC or laptop with USB port and requires no external power supply.

The complete set of UP00A USB programmer is equipped with a 40 pin universal ZIF socket that provides a comfort and easy operation during plug in and plug out the chip. Besides ZIF socket, header pin for ICSP (In-Circuit Serial Programming) also provided. This header pin can be used for in-circuit programming and to program the PIC with different socket which is not supported by the ZIF-socket.

Features:

- Designed for Intel based PC, DO NOT support AMD based system.
- Fast, reliable and low-cost.
- Do not support Window Vista
- Require USB port only.
- Can be used in desktop PC and laptop.
- ZIF socket and ICSP header pin are prepared.
- The programmer can be used for Windows Me/NT/2000/XP.
- 12F, 16F and 18F PIC MCU are supported.
- USB cable, user manual and programming software are provided.

Package Including:

- UP00A Programmer Unit
- USB Cable
- User Manual and Programming software in CD Rom
- 6 months warranty against factory defect only

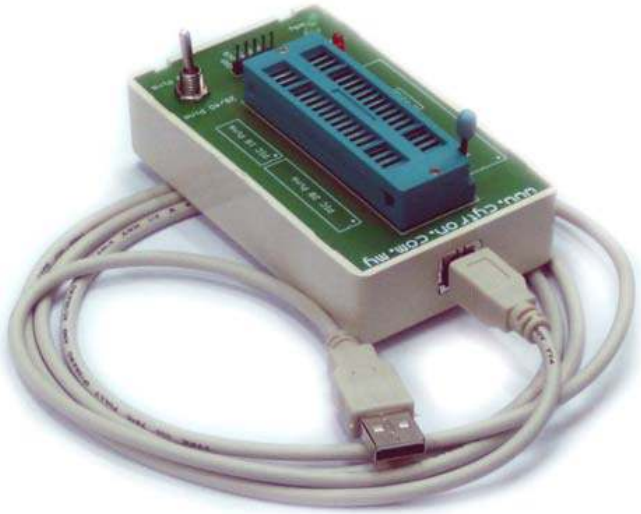


Figure 4.8: CYTRON USB Programmer

4.3.2.1 Plugging the Microcontroller

40-pin Microcontroller

- Plug in the microcontroller at the socket (indicated on the board) and push forward the toggle switch as shown.

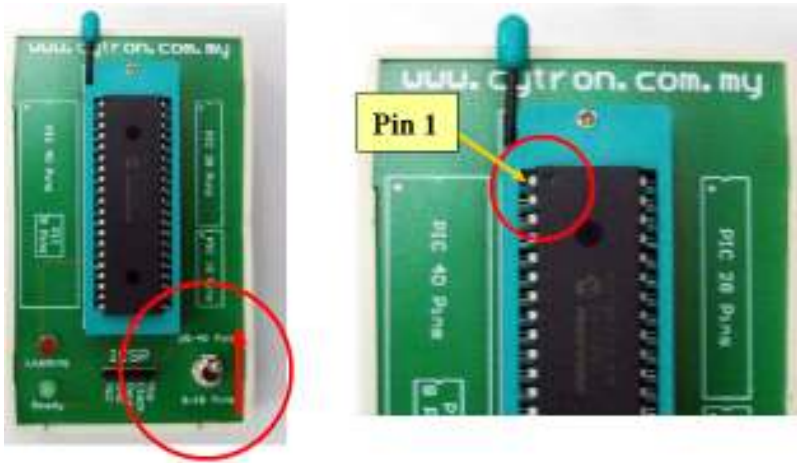
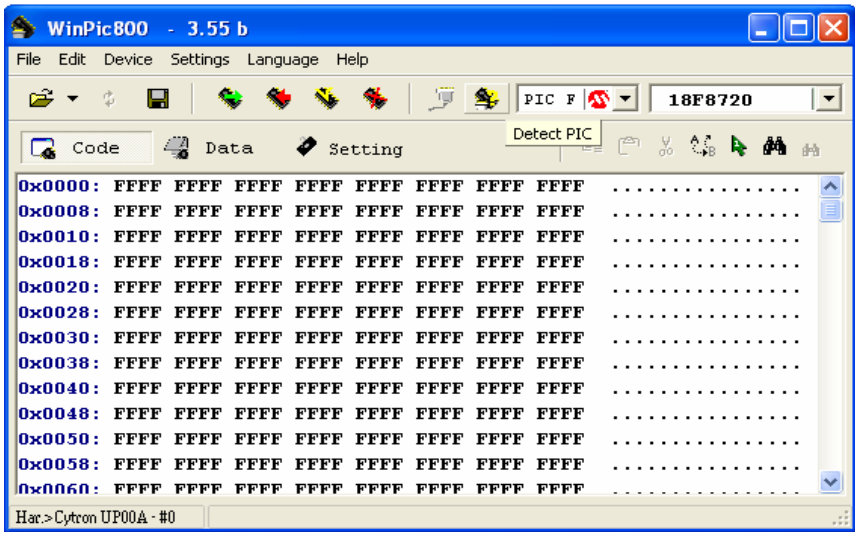


Figure 4.9: Plug-in 40-pin Microcontroller

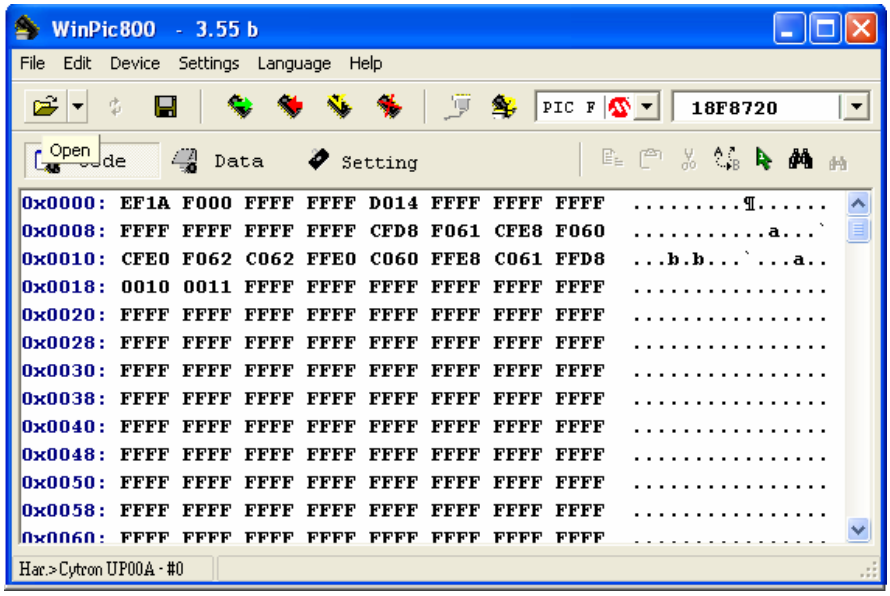
4.3.2.2 How To Program The PIC Microcontroller

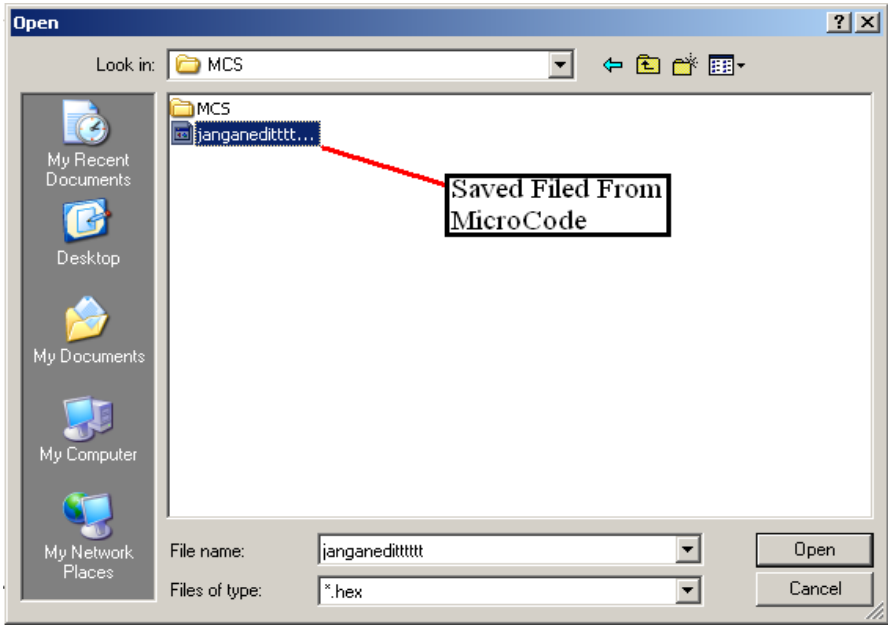
To start writing the C-language in PIC18F4550, first run WinPic800.exe software;

1. By clicking the icon shown, the programmer will detect the type of PIC on the Programmer.

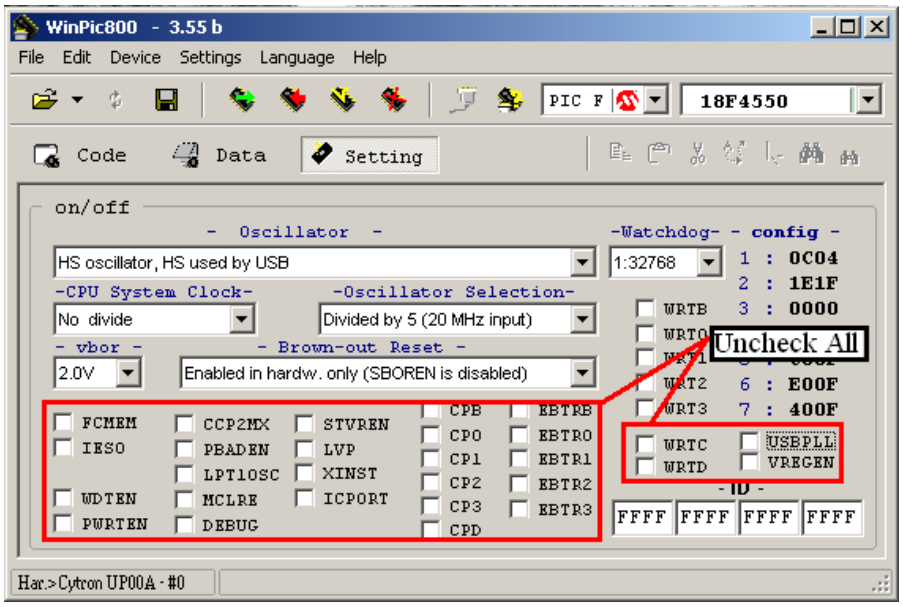


2. To write Hex code to PIC we must first open the hex file. By clicking the icon shown, a browse window will appear, open the hex file by clicking the file.

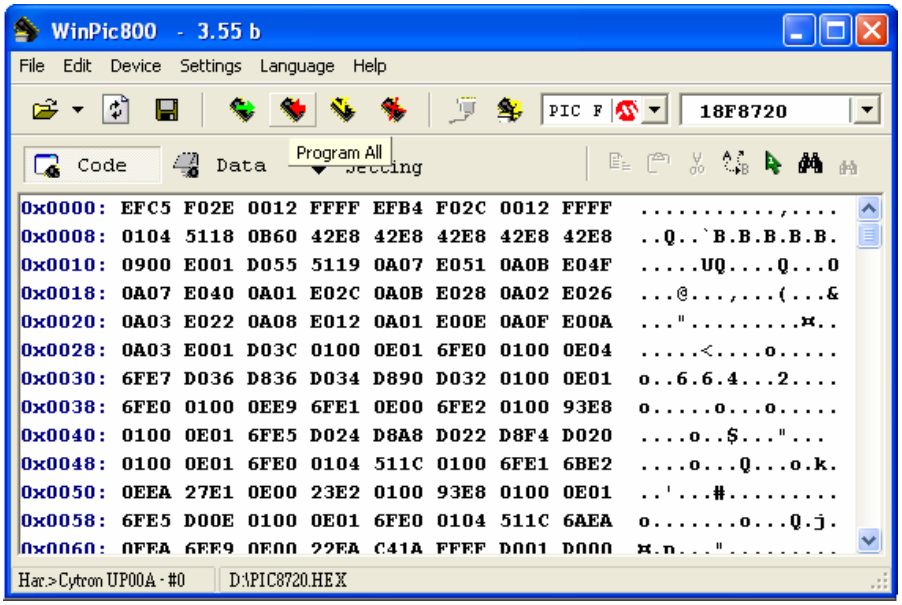




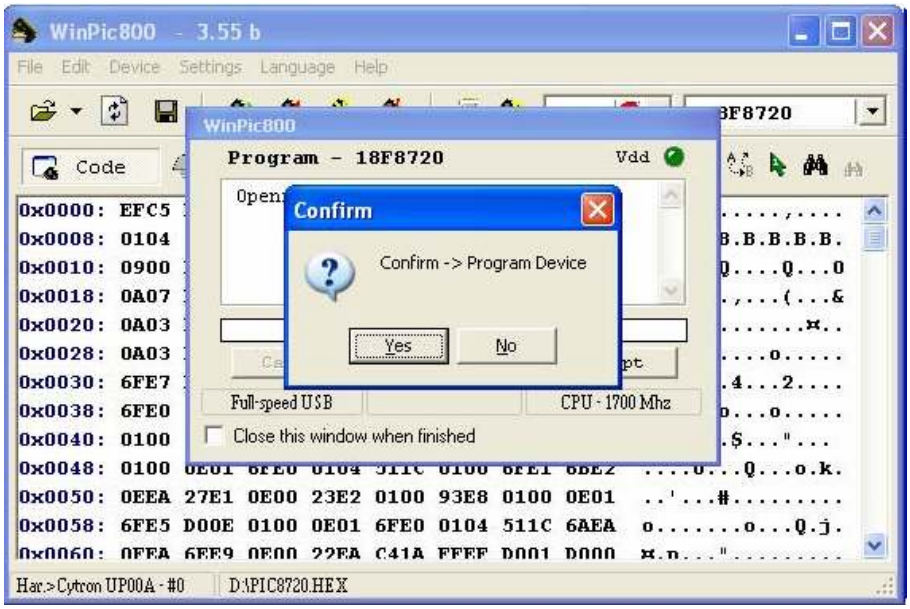
3. Configure the Setting

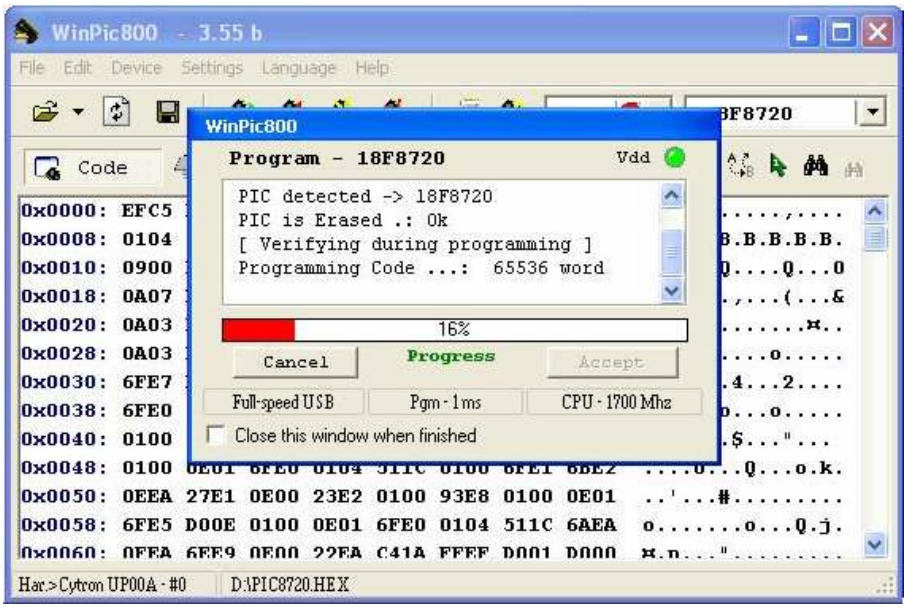


4. Program the file to PIC by clicking the icon shown.

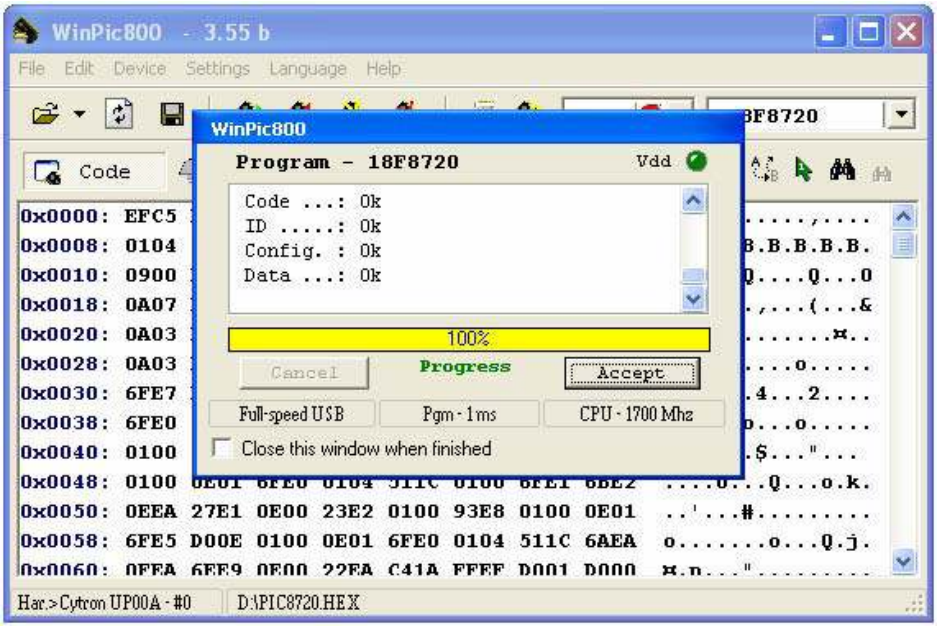


5. A confirmation window will appear, click *Yes* to proceed programming PIC.





6. When it is completed, the window will show the status. Click *Accept* and the PIC is ready to be plug out.



4.3.3 PIC Driver Circuit Hardware

Figure 4.10 shows the hardware circuit for driver PIC. These hardware been installed for AR-ELCB control element circuit. In this circuit there are consisted of Oscillator 20MHz, Capacitor to reduced ripple for ADC, Connector to LCD and also output relay and also input ADC. This driver circuit has fewer components than the actual PIC driver circuit. It has been test that by reducing the capacitor in the circuit, there is not much changing in the operation of the circuit. Because the 5Volt input voltage that have been supply to the driver circuit is already stable, and there is no reverse current from the Solid State Relay. So by using this driver circuit, the space and troubleshooting is easier to be done.

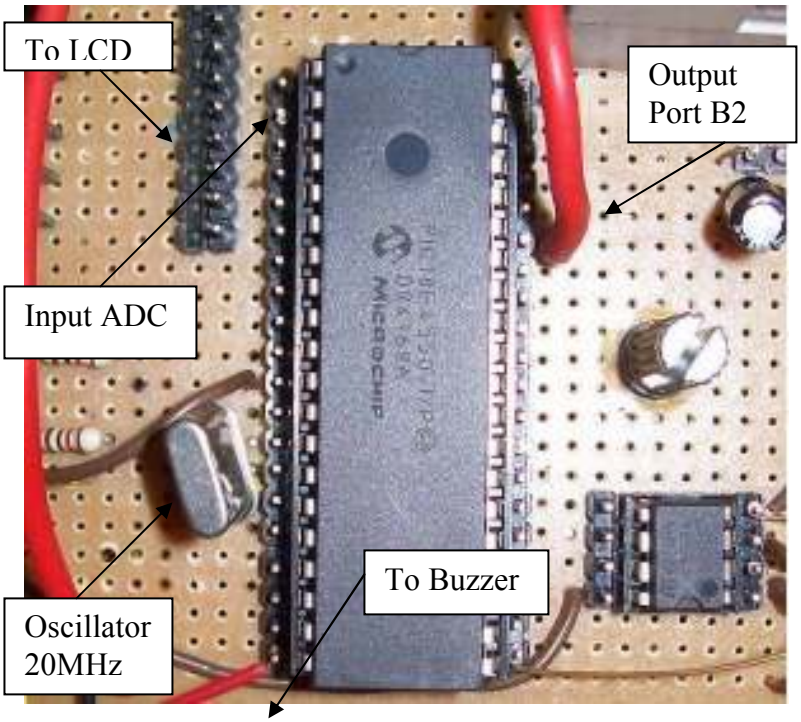


Figure 4.10: Control Element Circuit

4.4 Programming Flowchart

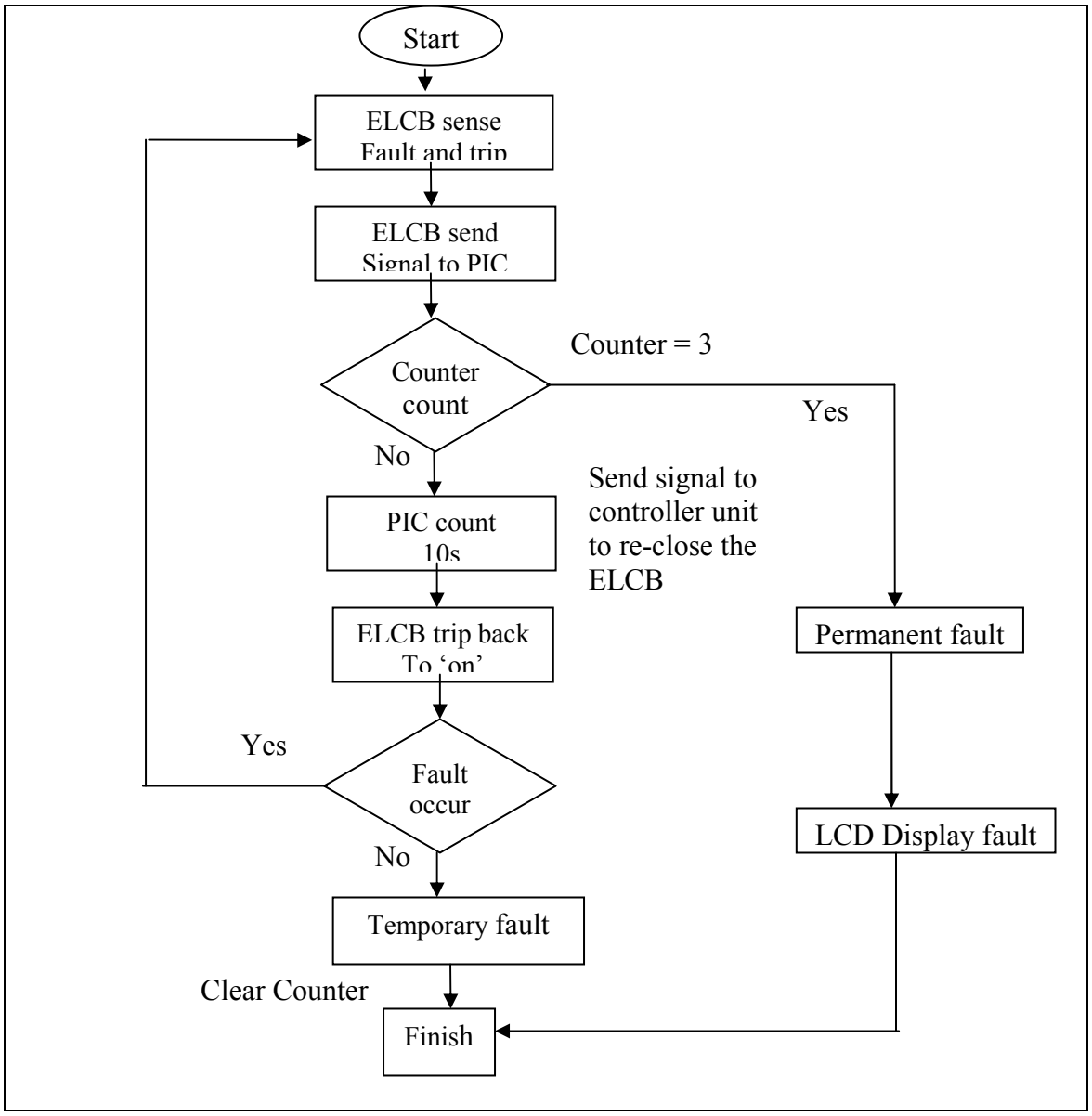


Figure 4.11: Flow of programming software

From Figure 4.11, When a fault occur ZCT will sense the imbalance current and then it will induced a signal current. This signal then is send to the PIC microcontroller via sensing circuit. PIC microcontroller then will send signal to trip the ELCB. At this moment the counter in the PIC will start count as 1. After 10 second, the ELCB will automatically switch back to normal condition. If there is no fault detect after the ELCB is turn on the LCD will display temporary fault and the ELCB will stay connected until next fault occurred and the counter will be reset. Meanwhile if there is fault occurred instantly after the ELCB is turning back to on, the ZCT will detect the imbalance current and then will send back the signal to PIC. The ELCB then will turn on back after being trip. At this time PIC counter will count as 2, this process will be cycle until the counter reach 3. After PIC counter reach 3, PIC microcontroller will identify the fault as permanent fault such like short circuit and over-current. The ELCB then will be tripped as to isolated connection of load with power line.

4.5 Programming Description

For starting programming PIC18f4550, Microcode Studio-PIC BASIC PRO chosen because this is simpler software and user friendly. Firstly, the oscillator must be defined according the crystal used in circuit. So, it set to 20. Then, LCD port and bit defined followed by define the analog-digital converter (ADC). In ADC, we must consider in define the number of bits, the clock source and the sampling time in microseconds. After that, the data to send to PIC must be identified by use VAR command. So, three data is identified to give some command in program which are data1, i and j. Volt use to set the program to operate at greater than $40 byte (1 volt in actual value). i and j use to make counter in program. Then, the output and input pin of PIC define by using command TRISA and TRISB mean port A and B used. So, 0 is set for the output, and 1 use as input.

Begin of the main part of program, IF use to make choice or comparison at two probability. The first counter i is used to count fault, meanwhile j is used to reset back counter i if data there is no data entering port A1 in delay of 5 second. When program start, i and j are 0 and the count did not start yet. During normal condition, where there is no fault port B2 is high and port D1 is low which indicated the solid state relay is in operation and the buzzer is off. Let say if there is permanent fault like short-circuit in network, port A1 will always detect voltage $40 byte because the short circuit is continuous. The counter i count from 1 and there are still detecting VOLT, because each fault detect is less than 5 second, thus counter j cannot count and cannot reset the counter i resulting in increment of counter i from 1 to 2 and from 2 to 3. After the counter i reach 3, PIC will recognize fault, LCD will display SHORTCIRCUIT, port B2 will be low and port D1 will be high which the port are for Solid State Relay and Buzzer. Meanwhile if lightning fault that occur, signal will be send to port A1 after the lightning strike and counter i will count as 1. Because there is no second lightning and if there is, the delay for voltage signal reach port A1 must be greater than 5 second, thus counter j will count to 5 and will reset back counter i to 0 and the LCD will display Lightning Fault. Then the operation of PIC will back to normal which port B2 will be high and port D1 will be low.

4.10 Summary

The use of PIC microcontroller has made the system more reliable, acting faster and there is always chances to modified the microcontroller soon especially if there are changes in hardware system. Besides it has reduces the cost and space of control circuit, compared to the use of fully mechanical controller components like 555 timer, portable counter and separate Analog to Digital Converter. The programming for PIC18F4550 also is easier with the existence of PicBasic Compiler (MicroCode Studio) and PIC USB programmer with WinPic800 especially for the programming that involve only one input port.

CHAPTER 5

RESULTS & DISCUSSIONS

5.1 Introduction

In this chapter results and discussion for the whole development of Earth Leakage Circuit Breaker with an Auto Re-closer Unit (AR-ELCB) process will be described. The result that will be discussed in this chapter is for the data measurement of Zero Phase Current Transformer (ZCT), calculation designing converter circuit and the result for the whole ELCB systems. The calculation in this chapter is depends on the result of measurement of ZCT. It is due to the ZCT function as the first sensing device in the system, only system with the accurate sensor and sensitivity can achieve the objectives. Because this project is based on protection system it is important to count every aspect of measurement in order to not mess with the original ELCB. Every discussion stated in this chapter also for the whole system problems, the better solution need to come-up in order to overcome every flaw and problems of this ELCB system.

5.2 Measurement of ZCT

The objectives of measurement ZCT is to get the output value of induced current from the coil of the ZCT. Because there is magnetic material build in ZCT whenever there is unbalance current flow through the ZCT, the coil that winding around the ZCT will induced current that is depend on the strength of the imbalance current. The induced current then will flow through the coil then it will flow to the sensing circuit. Because the induced current is Ac (Alternative current), the polarity of the current must be consider in order to avoid the effect of reverse current. This is very important in order to get a take measurement value while designing the current to voltage converter. Figure 5.1 show the operation of ZCT.

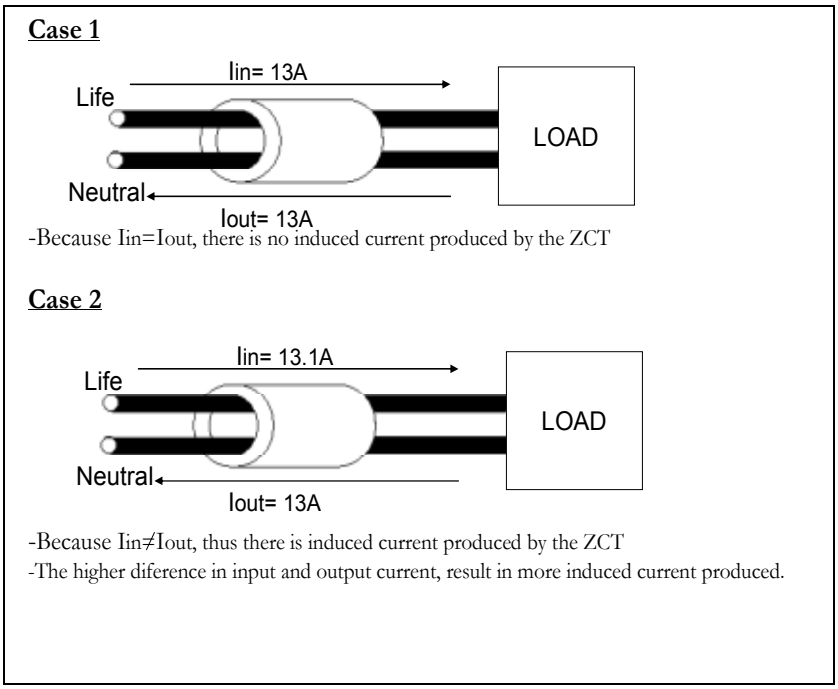


Figure 5.1: Operation of ZCT

The 6A 240Vac single phase Motor and 1A Bulb has been used as the load for this experiment. The advantage of using the motor is because motor drew high current during startup. This situation theoretically produced the surge current at the initially but soon after the current will be balance for the load. We can assume this condition of surge current from startup motor is approaching the condition of lightning. Even though the value of surge current of the lightning is too large and is over 100A, but the similarity can be consider since the sensitivity of the ZCT is 100mA. It has been proved that the induced current from ZCT by using this method is over 100mA which are the same of lightning that >100mA. The objective of this experiment is to find the average value of induced current that is produced by ZCT in 10 measurements so that it can be taken as reference value for the input signal PIC. Figure 5.2 and Figure 5.3 show the load bulb and motor that is use for the experiment.

Figure 5.2: 1A Bulb

Figure 5.3: 6A Motor

To measure the ZCT induced current, only live line supply is passed through the ZCT. Meanwhile the neutral line will not passed though it, so the ZCT will get a high imbalance current which are the values of current that flow through the live line itself.

Table 5.3: ZCT Induce Current

Bil.	With load 1A (lamp)	With load 6A (Motor)
1	26.5mA	684.1mA*
2	58.2mA	141.3mA*
3	29.8mA	67.3mA
4	28.6mA	301.4mA*
5	235.3mA*	381.2mA*
6	28.5mA	68.7mA
7	129.7mA*	208.3mA*
8	60.5mA	71.96mA
9	214.1mA*	68.11mA
10	29.3mA	106.9mA*
Note * =because the sensitivity of ZCT is 100mA, all the value over 100mA, will make the ELCB tripped. Note**=ZCT give different value because the induced current is surge current		

From the table above, it shows that the different between ZCT induced current when using 6A motor is higher than when using 1A bulb. The highest reading get is effect from the surge current of the load. The reason why motor induced more current is because motor draw more current at startup compare when it running. Data shows value from motor greater then value from the bulb because the current for the motor (6A) is greater than bulb (1A), so the coil will produce more electromagnetic field in ZCT. The experiment is done with two different loads to show the relationship between supplies current and induce current. In other word the supply current is directly proportional to the induced current. That's mean if we are going to use load with 10A current, it will induced more current from ZCT.

Another factor that is affecting the strength of the induced current is how much round the coil is wrapping around the ZCT. It has been proven by winding lot of wrapping wire around ZCT effect in higher value of induced current.

5.3 Measurement of Op-Amp Voltage Output

Output voltage from op-amp is use as input voltage signal to PIC. This voltage is variable because we can vary the PIC to operate at certain range voltage with different sensitivity. So, variable resistor used in order to control output voltage from the Op-amp.

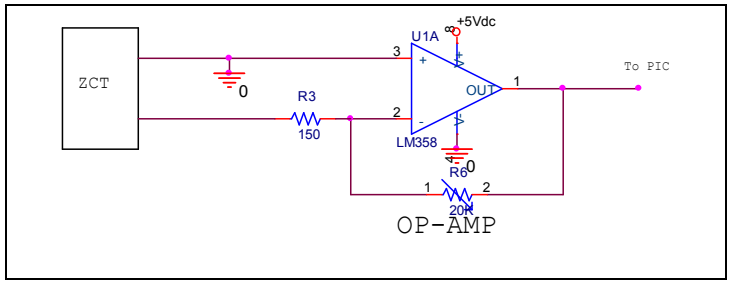


Figure 5.4: Op-amp Circuit

Input op-amp is current from ZCT that has been converting to voltage through the 150ohm resistor. It is then amplified by LM358 accompanied by 20k variable resistor. Motor run and reading taken after it show a constant reading. At one point the value of the output voltage is fixing and it cannot increase any more. It is because the LM358 Op-Amp has voltage limitation which is useful for low voltage application. Since the output voltage of Lm358 is lower than 5 volt, it need to be send to Analog to digital converter (ADC) because other port cannot read data value other than 0 volt and 5 volt. ADC will read the value of output Op-Amp in hexadecimal >$40 and then it will always make comparison between the reference value and the induced output voltage. Table below shows the voltage output from op-amp

Table 5.4: Output voltage from op-amp

Bil	RL (KΩ)	Op-Amp (V)
1	1	0.80
2	2	1.20
3	3	1.40
4	4	1.53
5	5	1.73
6	6	1.77
7	7	1.78
8	8	1.79
9	9	1.80
10	10	1.81

Output voltage of op-amp can be calculated by using the theory formula based on the gain of the amplifier circuit. Because PIC microcontroller can receive whatever value of input voltage in the ADC, this experiment shows the relation between current and voltage through the op-amp.

5.4 Arrangement of Fault Model

Fault model is very important in this project to demonstrate that this circuit is functioning and also so that reference Value can be made base on the model. For this experiment, the model is design by using a 6A motor and 1A bulb. Both is used but with different function. Bulb is used as an indicator to see weather the ELCB is tripped or not. Meanwhile the motor used to produce the induced current sufficient to trip the ELCB. To make it operated, the life line of the motor is passed through into the ZCT while neutral wire is place outside.

By doing so an unbalance current will be detected by the ZCT thus make it able to induced current. Meanwhile both two wire of load (lamp) will placed into ZCT to prove that when the motor is switch off there is no induced current, thus the ELCB will not tripped. For the simulation of temporary fault, the load line will on all the time to on the circuit system while the motor power supply will be turned on and turned off in that instant. It acts like the lightning which comes in only a few second or less than one second. So, the lamp will off when the motor on and then will be on back after the motor stop.

For the permanent fault model, the arrangement stills same but has a little different at time period of motor turned on. Motor will always switch on then the lamp will turn off along with the motor switch on. The PIC receives the voltage signal from sensing circuit and then it will on back the load (Bulb). Then the bulb will on back for a moment before it will turn of back because there is still signal voltage came from sensing circuit. This cycle will be continue for three cycle before PIC send signal to permanently switch off the bulb and the PIC will identify the fault is permanents fault. This is because permanent fault occur continuously unlike the temporary fault which is in only a moment. Figure 5.6 show the fault model arrangement circuit.

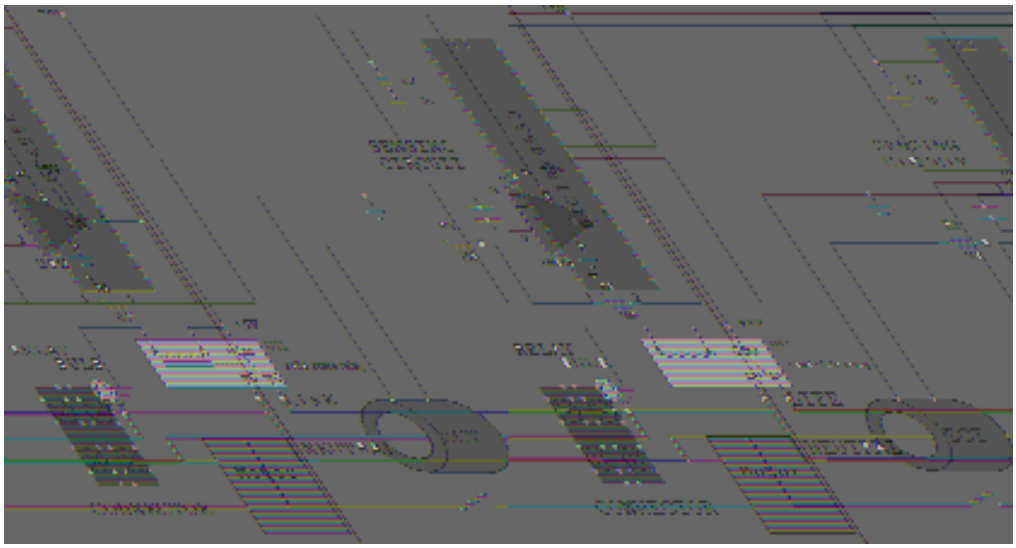


Figure 5.6: Fault model arrangement circuit

5.5 Project Results

Based on testing and experiment, the results of this project are show as below:

i. This Auto re-closer unit is operated accordingly and it can be integrated between controlled device and programming

ii. We were able to use the microcontroller to replace human to switch on or off the power ELCB.

iii. The new ELCB have successfully built, it operating just likes the command written and it can be differentiate between permanent and temporary fault.

iv. Zero Current Transducer must be sensitive enough to detect and produce induced current which are suitable to protect the Circuit @ Load.

v. The ELCB tripped the circuit for 5 second and followed and make the buzzer sound before it re-close back to the normal condition.

vi. The ELCB permanently disconnected the circuit if the circuit detects the leakage continuously. The ELCB will re-close for the cycle of 5 times before it will notify that the fault is permanent fault via the display of LCD and the sound of buzzer. The circuit will only back to normal condition after the user clear the permanents fault manually.

vii. LCD will display according to the fault that it identified weather types of fault exist, temporary and permanent.

viii. Zero phase current transformer produce enough current signal when it tested by using higher load current, that's mean it can be used in resident because maximum load in the resident is normally <30A and the minimum current it need to trigger the ELCB is 100mA.

5.6 Discussions

From this project, what we can discuss is:

i. Information about auto re-closer ELCB is not sufficient, because the development of this project is still and there currently no auto re-closer ELCB in the market. The process of measuring the ZCT does not have the guideline. Besides the sensitivity of 100mA is the standard use by IEEE, thus we need to use the current setting so that there is no fatal error or hazard occurs.

ii. Analysis the ZCT is pretty hard due to small sensitivity and small induced current. The device like power quality analyzer should be added in the laboratory so that it can used to detect the change in value of the induced current and can take one as the reference.

iii. The lack of source and references for his project in the development so everything that new must be creatively thinks how to solve although there just minor problem. The combination self measurement and datasheet information help a lot.

5.7 Summary

According on the results and discussions in this project, there are some important things that could be consider in order completing the whole auto re-closer ELCB system, it is the sensitivity of this system. Through the experiment of the Zero Phase Current Transducer (ZCT), the sensitivity of the product or device depends on the strength of the ZCT. There are currently 0.1A, 0.3A, 0.6A and also 1A sensitivity for nowadays ELCB but since most the resident application standard is 0.1A so the range sensitivity of 0.1A is picking so that any small change in unbalance current will result in tripping of the ELCB.

CHAPTER 6

CONCLUSIONS & SUGGESTIONS

6.1 Conclusions

The objectives of the development of Auto Re-closer Earth Leakage Circuit Breaker were successfully fulfilled. Which are first by designing an auto re-closer ELCB which can be operated better as the nowadays ELCB. The new ELCB can be operated with more efficient which are by making it automatic system that only required less human observation in order to operated it. Thus it makes human life easier that way. This project that utilized the use of PIC microcontroller, electronic switch, driver circuit and sensing circuit has successfully integrated between each other. In other word the synchronization between each circuit which is supply circuit, control circuit, sensing circuit, switching device and information display via LCD make it can operate with each other without any problems. The combination of analog electronics knowledge, autotronics knowledge, Microprocessor knowledge, power electronic knowledge and individual self skilled method to create the new circuit is important in order to make this project success.

The use of LM7805 voltage regulators have increase the efficiency and reduce the cost of the system compared to by using the transformerless circuit. The use of Solid State Relay compared to heavy power relay have increase the reliability and effectiveness of the project, even thought the cost of Solid State Relay is higher than the cost of Heavy Power Relay. So for simulation it better to use solid state relay because we can adept the system directly to the resident. The PIC18F4550 as a brain has made the system more reliable for modern technology and the input, output, timer and delay for the system can be adjusted by changing the programming command. This also has improved the ability of Earth Leakage Circuit Breaker with an Auto Re-closer unit. Then the system also can act accurately besides can be improved the function by reprogram the IC. The successful of this auto re-closer ELCB system has made the circuit can differentiate between permanent and temporary fault and acting differently between each type of fault.

6.2 Suggestions

There are several suggestions after the process for improvement AR-ELCB in the future:

i. For next improvement process the student must study the new auto re-closer ELCB in detailed and make sure to understand so that any flaw of this ELCB can be fix and thus a new upgrade can be done to make the ELCB more effective.

ii. In designing the circuit, choosing the correct component device is very important. The priority must be taken for the device spec, current rating, the device endurance and the operation of the component.

iii. Make a full analysis for the Zero Phase Current Transformer (ZCT) before designing the device for converter circuit. Make sure use power quality analyzer for analysis ZCT, the thing that must be measured is the sensitivity of the ZCT and the output induced current of the ZCT. To make it easier try to get the datasheet of ZCT from the device supplier.

iv. The use of Solid State Relay has already proven usefully, so in the future it is recommended using SSR but with different rating. Currently for this project, the rating of the SSR is 40A with input 5~24Vdc. So in the future it is better to use 30A with 5~24Vdc rating SSR because the resident usually does not consumed higher than 30A besides the cost of SSR with rating of 30A is totally differ with the cost of SSR with 40A rating.

v. Replace the bridge with 4 diode, array and connect it in the full wave rectifier connection, it will reduce the cost of bridge that is really expensive.

vi. For converter circuit the current LM358 Op-amp is already sufficient due to the 358 Op-amp just needs positive supply and ground to operate compared. But if there is need for improvement, the user might consider other Op-amp with the same spec but with higher range of output voltage such like LMC7111. Because the LM358 Op-amp output voltage is limited and it cannot go higher than 2Volt.

vii. Replace the 40 PIC18F4550 microcontrollers with 28 pin PIC18F2550 microcontroller. It is due to the PIC18F2550 have less port compare to PIC18F4550 which are 40-pin over 28-pin. Other than that the function of PIC 18F2550 is similar to PIC18F4550. Even though PIC 18F2550 have less port compare to PIC18F4550, but the port is sufficient to use in this project because for this project by using PIC18F4550 only 10 port for input and output signal. It is important to consider PIC18F4550 because we can save the cost along with the size.

viii. Beside that, I would suggest to use a current transducer, which could detect the current input through power line, and then compare the current with the initials current. With the use of current transducer, user might consider to replace the ZCT over Current Transducer or by using both to improve the reliability of the ELCB.

ix. Other than that, a keypad can be added which can display any other menu. The menu that can be display is current value, option to reset the ELCB and some minor calculations

x. The last future recommend that can be done is to design this driver in smaller size on control printed circuit board (PCB). By using software DXP Protell, The actual size of Vera board can be reduced to 1:10 from the original size of the PCB prototype.

6.3 Costing and Commercialization

This part will describe the parts and overall cost of fabricating the Over Current Protection Relay Using PIC micro Controller. This part also will explain the commercialization of project.

6.3.1 Costing

Tables 6.1 show the cost of the component and the total cost. The total cost of the development of Earth Leakage Circuit Breaker with an auto re-closer unit is RM 260.15. But the actual price of the whole ELCB circuit is only RM 245.15. It is due to the changing of component in the development process, besides there were the components that do not function and need to be replaced during the hardware circuit designing. The cost stated above is for the electronic and electric components that used and involve in this project. The cost for the ELCB can be reduced by following the suggestion stated in the suggestion section and also by buying the components in mass quantity.

Table 6.1: The cost of components

Device	**Qty**	**Model**	**Unit**	**Manufacture**	**Unit cost(RM)**	**Extended cost (RM)**
Transformer	1	T1201	-230V,50Hz -Vo : 12 - 0 - 12. Output -Power : 6 VA	TELETRON	10.00	10.00
Bridge Rectifier	1	KBPC6005PBF	-Vrrm:50V -Current Rating: 6A	INTERNATIONAL RECTIFIER	6.60	6.60
Capacitor	1		-470uF		0.15	0.15
Capacitor	1		-10uF		0.15	0.15
Capacitor	1		-1nF		0.15	0.15
Voltage Regulator	1	LM7805	-+5V dc		1.00	1.00
LED	2				0.10	0.20
Resistor	1		1kΩ		0.10	0.10
Resistor	1		150Ω		0.10	0.10
Variable Resistor	2		20kΩ		1.00	2.00
Zener Diode	1		5.1V		0.50	0.50
PCB Header	4				1.00	4.00
LCD	1	2X16 JHD16A			15.00	15.00
PIC	1	18F4550		Microchip	30.00	30.00
Connector	2				1.00	2.00
Solid State Relay	1	G3NA-240B	-Vo: 240Vac	Omron	169.00	169.00

			-Vin: 5-24Vdc			
Op-Amp	1	LM358		MOTOROLA	1.50	1.50
Fuse	1		-0.3A		0.20	0.20
Toggle Switch	1				1.00	1.00
PIC base	1				1.00	1.00
Op-Amp base	1				0.50	0.50
Wrapping Wire	1				15.00	15.00
					Total	260.15

6.3.2 Commercialization

This project can be commercialize by built the new ELCB that follow the feature that have been recommended in the suggestion section, it is due to the target cost of the recommended ELCB is more cheaper than this new invention one. The estimated cost should be around RM 200.00 only without buy components in bulk way.

The new AR-ELCB has the higher commercialize value because it can solve the currently existence of ELCB problems.

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APPENDIX A

AR-ELCB Programming

EARTH LEAKAGE CIRCUIT BREAKER WITH AN AUTO RE-CLOSER UNIT PROGRAMMING USING PICBASIC (MICROCODE STUDIO)

```
DEFINE OSC 20

DEFINE LCD_DREG PORTB
DEFINE LCD_DBIT 4
DEFINE LCD_RSREG PORTB
DEFINE LCD_RSBIT 3
DEFINE LCD_EREG PORTB
DEFINE LCD_EBIT 0
DEFINE LCD_BITS 4
DEFINE LCD_LINES 2
DEFINE LCD_COMMANDUS 2000
DEFINE LCD_DATAUS 255

' Define ADCIN parameters
Define ADC_BITS 8 ' Set number of bits in result
Define ADC_CLOCK 3 ' Set clock source (3=rc)
Define ADC_SAMPLEUS 50 ' Set sampling time in uS

data1 var byte
i var byte
j var byte
adcon1=$0e
trisa= %00111111
trisb= %00100000
trisd= %00000000


   main:
```

```
    pause 1000
    lcdout $fe,$80+4, "Tarmizi"
    lcdout $fe,$c0+4, "EC 05004"

    pause 1000
    lcdout $fe,1

    lcdout $fe,$80+1, "ELCB with Auto"
    lcdout $fe,$c0+1, "Re-Closer Unit"

    pause 1000
    lcdout $fe,1

    i=0
    j=0
loop:
      adcin 0,data1

      if data1>$40 then
        low portb.2
        HIGH Portd.1
        lcdout $fe,1
        lcdout $fe,$80+2, "Protection Off"
        lcdout $fe,$c0, "Fault:Overcurent"
        pause 1000
        i=i+1
        if i=3 then goto stop1

      else

        high portb.2
```

```
            low portd.1
            lcdout $fe,1
            lcdout $fe,$80+2, "Protection ON"
            lcdout $fe,$c0+2, "Fault: None"
            pause 1000
            j=j+1
            if j>5 then i=0
'            count portd.2,5000,timer1
'            if timer1>5000 then i=0

        endif

   goto loop
stop1:
end
```

APPENDIX B

PIC18F4550 Microcontroller, Addressing Modes, and Instruction Set

PIC18F4550 MICROCONTROLLER, ADDRESSING MODES AND INSTRUCTION SET

MICROCHIP PIC18F2455/2550/4455/4550

28/40/44-Pin, High-Performance, Enhanced Flash, USB Microcontrollers with nanoWatt Technology

Universal Serial Bus Features:

- USB V2.0 Compliant
- Low Speed (1.5 Mb/s) and Full Speed (12 Mb/s)
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- Supports up to 32 Endpoints (16 bidirectional)
- 1-Kbyte Dual Access RAM for USB
- On-Chip USB Transceiver with On-Chip Voltage Regulator
- Interface for Off-Chip USB Transceiver
- Streaming Parallel Port (SPP) for USB streaming transfers (40/44-pin devices only)

Power-Managed Modes:

- Run: CPU on, peripherals on
- Idle: CPU off, peripherals on
- Sleep: CPU off, peripherals off
- Idle mode currents down to 5.8 µA typical
- Sleep mode currents down to 0.1 µA typical
- Timer1 Oscillator: 1.1 µA typical, 32 kHz, 2V
- Watchdog Timer: 2.1 µA typical
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Four Crystal modes, including High Precision PLL for USB
- Two External Clock modes, up to 48 MHz
- Internal Oscillator Block:
  - 8 user-selectable frequencies, from 31 kHz to 8 MHz
  - User-tunable to compensate for frequency drift
- Secondary Oscillator using Timer1 @ 32 kHz
- Dual Oscillator options allow microcontroller and USB module to run at different clock speeds
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if any clock stops

Peripheral Highlights:

- High-Current Sink/Source: 25 mA/25 mA
- Three External Interrupts
- Four Timer modules (Timer0 to Timer3)
- Up to 2 Capture/Compare/PWM (CCP) modules:
  - Capture is 16-bit, max. resolution 5.2 ns (TCY/16)
  - Compare is 16-bit, max. resolution 83.3 ns (TCY)
  - PWM output: PWM resolution is 1 to 10-bit
- Enhanced Capture/Compare/PWM (ECCP) module:
  - Multiple output modes
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
- Enhanced USART module:
  - LIN bus support
- Master Synchronous Serial Port (MSSP) module supporting 3-wire SPI (all 4 modes) and I^2C™ Master and Slave modes
- 10-bit, up to 13-channel Analog-to-Digital Converter module (A/D) with Programmable Acquisition Time
- Dual Analog Comparators with Input Multiplexing

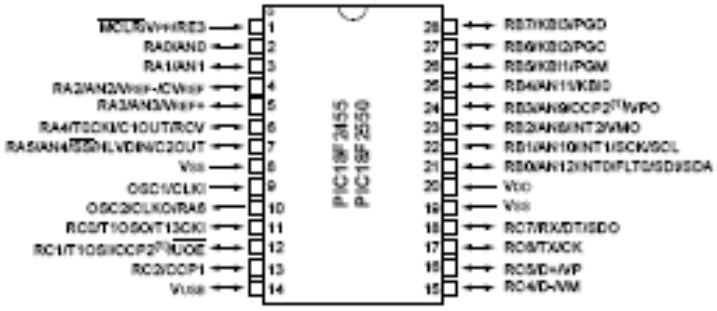
Special Microcontroller Features:

- C Compiler Optimized Architecture with optional Extended Instruction Set
- 100,000 Erase/Write Cycle Enhanced Flash Program Memory typical
- 1,000,000 Erase/Write Cycle Data EEPROM Memory typical
- Flash/Data EEPROM Retention: > 40 years
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 41 ms to 131s
- Programmable Code Protection
- Single-Supply 5V In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via two pins
- Optional dedicated ICD/ICSP port (44-pin devices only)
- Wide Operating Voltage Range (2.0V to 5.5V)

Device	Program Memory		Data Memory		I/O	10-Bit A/D (ch)	CCP/ECCP (PWM)	SPP	MSSP		EAUSART	Comparators	Timers 8/16-Bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)					SPI	Master I^2C™			
PIC18F2455	24K	12288	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F2550	32K	16384	2048	256	24	10	2/0	No	Y	Y	1	2	1/3
PIC18F4455	24K	12288	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3
PIC18F4550	32K	16384	2048	256	35	13	1/1	Yes	Y	Y	1	2	1/3

Pin Diagrams

28-Pin PDIP, SOIC



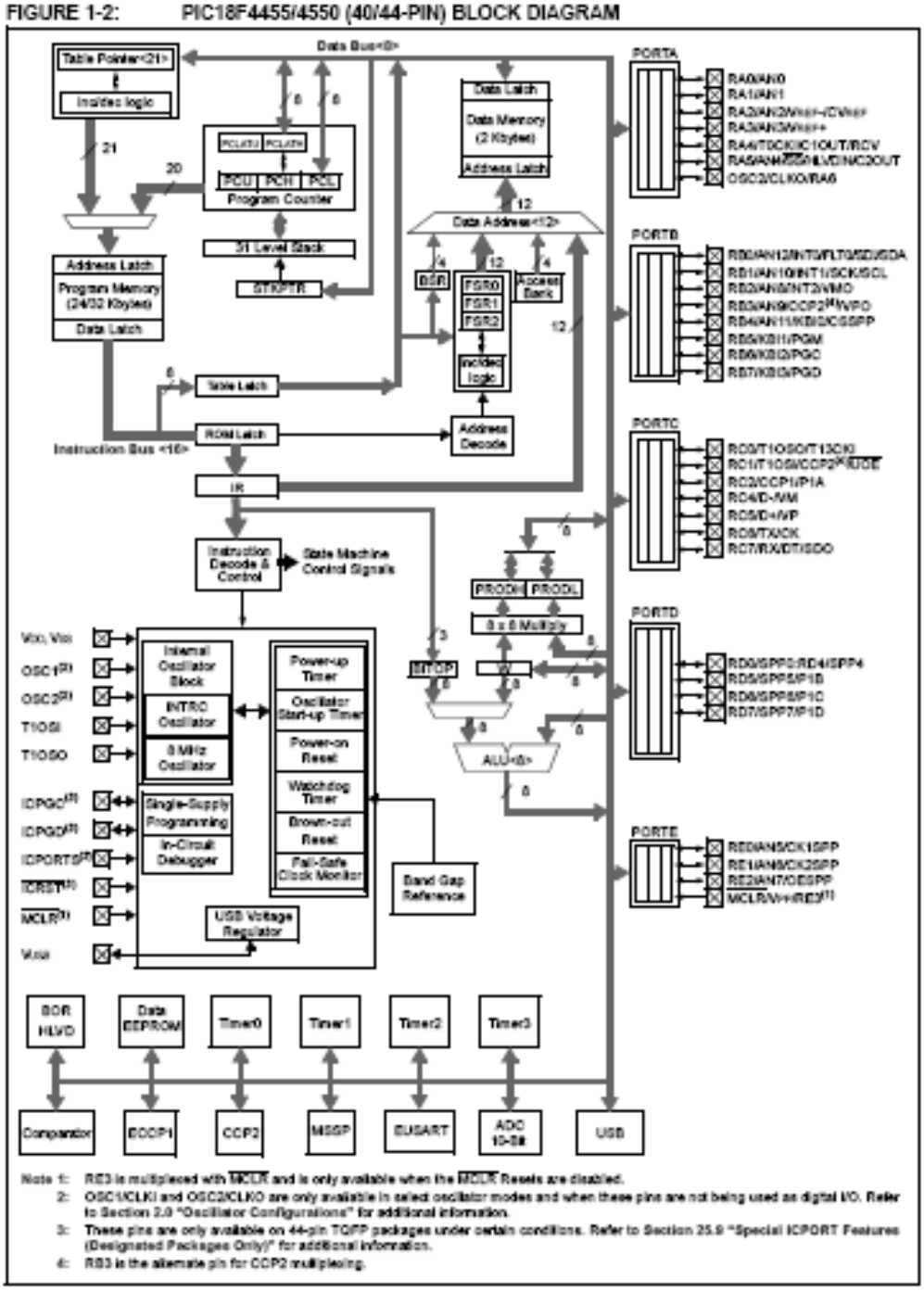
40-Pin PDIP

Note 1: RB3 is the alternate pin for CCP2 multiplexing.

TABLE 1-1: DEVICE FEATURES

Features	PIC18F2455	PIC18F2550	PIC18F4455	PIC18F4550
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	24576	32768	24576	32768
Program Memory (Instructions)	12288	16384	12288	16384
Data Memory (Bytes)	2048	2048	2048	2048
Data EEPROM Memory (Bytes)	256	256	256	256
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Timers	4	4	4	4
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/ Compare/PWM Modules	0	0	1	1
Serial Communications	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART	MSSP, Enhanced USART
Universal Serial Bus (USB) Module	1	1	1	1
Streaming Parallel Port (SPP)	No	No	Yes	Yes
10-Bit Analog-to-Digital Module	10 Input Channels	10 Input Channels	13 Input Channels	13 Input Channels
Comparators	2	2	2	2
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST), MCLR (optional), WDT
Programmable Low-Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled	75 Instructions; 83 with Extended Instruction Set enabled
Packages	28-pin PDIP 28-pin SOIC	28-pin PDIP 28-pin SOIC	40-pin PDIP 44-pin QFN 44-pin TQFP	40-pin PDIP 44-pin QFN 44-pin TQFP

FIGURE 1-2: PIC18F4455/4550 (40/44-PIN) BLOCK DIAGRAM



Note 1: RE3 is multiplexed with MCLR and is only available when the MCLR Resets are disabled.
2: OSC1/CLKI and OSC2/CLKO are only available in select oscillator modes and when these pins are not being used as digital I/O. Refer to Section 2.0 "Oscillator Configurations" for additional information.
3: These pins are only available on 44-pin TQFP packages under certain conditions. Refer to Section 25.9 "Special ICPORT Features (Designated Packages Only)" for additional information.
4: RB3 is the alternate pin for CCP2 multiplexing.

TABLE 1-2: PIC18F2455/2550 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	PDIP, SOIC			
MCLR/VPP/RE3	1			Master Clear (input) or programming voltage (input).
MCLR		I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP		P		Programming voltage input.
RE3		I	ST	Digital input.
OSC1/CLKI	9			Oscillator crystal or external clock input.
OSC1		I	Analog	Oscillator crystal input or external clock source input.
CLKI		I	Analog	External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)
OSC2/CLKO/RA6	10			Oscillator crystal or clock output.
OSC2		O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO		O	—	In select modes, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6		I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
MCLR/VPP/RE3	1	18	18			Master Clear (Input) or programming voltage (input).
MCLR				I	ST	Master Clear (Reset) input. This pin is an active-low Reset to the device.
VPP				P		Programming voltage input.
RE3				I	ST	Digital input.
OSC1/CLKI	13	32	30			Oscillator crystal or external clock input.
OSC1				I	Analog	Oscillator crystal input or external clock source input.
CLKI				I	Analog	External clock source input. Always associated with pin function OSC1. (See OSC2/CLKO pin.)
OSC2/CLKO/RA6	14	33	31			Oscillator crystal or clock output.
OSC2				O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO				O	—	In RC mode, OSC2 pin outputs CLKO which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6				I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTA is a bidirectional I/O port.
RA0/AN0	2	19	19			
RA0				I/O	TTL	Digital I/O.
AN0				I	Analog	Analog input 0.
RA1/AN1	3	20	20			
RA1				I/O	TTL	Digital I/O.
AN1				I	Analog	Analog input 1.
RA2/AN2/VREF-/CVREF	4	21	21			
RA2				I/O	TTL	Digital I/O.
AN2				I	Analog	Analog input 2.
VREF-				I	Analog	A/D reference voltage (low) input.
CVREF				O	Analog	Analog comparator reference output.
RA3/AN3/VREF+	5	22	22			
RA3				I/O	TTL	Digital I/O.
AN3				I	Analog	Analog input 3.
VREF+				I	Analog	A/D reference voltage (high) input.
RA4/T0CKI/C1OUT/RCV	6	23	23			
RA4				I/O	ST	Digital I/O.
T0CKI				I	ST	Timer0 external clock input.
C1OUT				O	—	Comparator 1 output.
RCV				I	TTL	External USB transceiver RCV input.
RA5/AN4/$\overline{SS}$/HLVDIN/C2OUT	7	24	24			
RA5				I/O	TTL	Digital I/O.
AN4				I	Analog	Analog input 4.
$\overline{SS}$				I	TTL	SPI slave select input.
HLVDIN				I	Analog	High/Low-Voltage Detect input.
C2OUT				O	—	Comparator 2 output.
RA6	—	—	—	—	—	See the OSC2/CLKO/RA6 pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/AN12/INT0/FLT0/SDI/SDA	33	9	8			
RB0				I/O	TTL	Digital I/O.
AN12				I	Analog	Analog Input 12.
INT0				I	ST	External Interrupt 0.
FLT0				I	ST	Enhanced PWM Fault Input (ECCP1 module).
SDI				I	ST	SPI data in.
SDA				I/O	ST	I^2C™ data I/O.
RB1/AN10/INT1/SCK/SCL	34	10	9			
RB1				I/O	TTL	Digital I/O.
AN10				I	Analog	Analog Input 10.
INT1				I	ST	External Interrupt 1.
SCK				I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL				I/O	ST	Synchronous serial clock input/output for I^2C mode.
RB2/AN8/INT2/VMO	35	11	10			
RB2				I/O	TTL	Digital I/O.
AN8				I	Analog	Analog Input 8.
INT2				I	ST	External Interrupt 2.
VMO				O	—	External USB transceiver VMO output.
RB3/AN9/CCP2/VPO	36	12	11			
RB3				I/O	TTL	Digital I/O.
AN9				I	Analog	Analog Input 9.
CCP2(1)				I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
VPO				O	—	External USB transceiver VPO output.
RB4/AN11/KBI0/CSSPP	37	14	14			
RB4				I/O	TTL	Digital I/O.
AN11				I	Analog	Analog Input 11.
KBI0				I	TTL	Interrupt-on-change pin.
CSSPP				O	—	SPP chip select control output.
RB5/KBI1/PGM	38	15	15			
RB5				I/O	TTL	Digital I/O.
KBI1				I	TTL	Interrupt-on-change pin.
PGM				I/O	ST	Low-Voltage ICSP™ Programming enable pin.
RB6/KBI2/PGC	39	16	16			
RB6				I/O	TTL	Digital I/O.
KBI2				I	TTL	Interrupt-on-change pin.
PGC				I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	40	17	17			
RB7				I/O	TTL	Digital I/O.
KBI3				I	TTL	Interrupt-on-change pin.
PGD				I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTC is a bidirectional I/O port.
RC0/T1OSO/T13CKI	15	34	32			
RC0				I/O	ST	Digital I/O.
T1OSO				O	—	Timer1 oscillator output.
T13CKI				I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2/ $\overline{UOE}$	16	35	35			
RC1				I/O	ST	Digital I/O.
T1OSI				I	CMOS	Timer1 oscillator input.
CCP2(2)				I/O	ST	Capture 2 input/Compare 2 output/PWM 2 output.
$\overline{UOE}$				O	—	External USB transceiver $\overline{OE}$ output.
RC2/CCP1/P1A	17	36	36			
RC2				I/O	ST	Digital I/O.
CCP1				I/O	ST	Capture 1 input/Compare 1 output/PWM 1 output.
P1A				O	TTL	Enhanced CCP1 PWM output, channel A.
RC4/D-/VM	23	42	42			
RC4				I	TTL	Digital input.
D-				I/O	—	USB differential minus line (input/output).
VM				I	TTL	External USB transceiver VM input.
RC5/D+/VP	24	43	43			
RC5				I	TTL	Digital input.
D+				I/O	—	USB differential plus line (input/output).
VP				I	TTL	External USB transceiver VP input.
RC6/TX/CK	25	44	44			
RC6				I/O	ST	Digital I/O.
TX				O	—	EUSART asynchronous transmit.
CK				I/O	ST	EUSART synchronous clock (see RX/DT).
RC7/RX/DT/SDO	26	1	1			
RC7				I/O	ST	Digital I/O.
RX				I	ST	EUSART asynchronous receive.
DT				I/O	ST	EUSART synchronous data (see TX/CK).
SDO				O	—	SPI data out.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels; I = Input
O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the $\overline{ICPRT}$ Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the $\overline{DEBUG}$ Configuration bit is cleared.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTD is a bidirectional I/O port or a Streaming Parallel Port (SPP). These pins have TTL input buffers when the SPP module is enabled.
RD0/SPP0	19	38	38			
RD0				I/O	ST	Digital I/O.
SPP0				I/O	TTL	Streaming Parallel Port data.
RD1/SPP1	20	39	39			
RD1				I/O	ST	Digital I/O.
SPP1				I/O	TTL	Streaming Parallel Port data.
RD2/SPP2	21	40	40			
RD2				I/O	ST	Digital I/O.
SPP2				I/O	TTL	Streaming Parallel Port data.
RD3/SPP3	22	41	41			
RD3				I/O	ST	Digital I/O.
SPP3				I/O	TTL	Streaming Parallel Port data.
RD4/SPP4	27	2	2			
RD4				I/O	ST	Digital I/O.
SPP4				I/O	TTL	Streaming Parallel Port data.
RD5/SPP5/P1B	28	3	3			
RD5				I/O	ST	Digital I/O.
SPP5				I/O	TTL	Streaming Parallel Port data.
P1B				O	—	Enhanced CCP1 PWM output, channel B.
RD6/SPP6/P1C	29	4	4			
RD6				I/O	ST	Digital I/O.
SPP6				I/O	TTL	Streaming Parallel Port data.
P1C				O	—	Enhanced CCP1 PWM output, channel C.
RD7/SPP7/P1D	30	5	5			
RD7				I/O	ST	Digital I/O.
SPP7				I/O	TTL	Streaming Parallel Port data.
P1D				O	—	Enhanced CCP1 PWM output, channel D.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

TABLE 1-3: PIC18F4455/4550 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	QFN	TQFP			
						PORTE is a bidirectional I/O port.
RE0/AN5/CK1SPP	8	25	25			
RE0				I/O	ST	Digital I/O.
AN5				I	Analog	Analog input 5.
CK1SPP				O	—	SPP clock 1 output.
RE1/AN6/CK2SPP	9	26	26			
RE1				I/O	ST	Digital I/O.
AN6				I	Analog	Analog input 6.
CK2SPP				O	—	SPP clock 2 output.
RE2/AN7/OESPP	10	27	27			
RE2				I/O	ST	Digital I/O.
AN7				I	Analog	Analog input 7.
OESPP				O	—	SPP output enable output.
RE3	—	—	—	—	—	See $\overline{MCLR}$/VPP/RE3 pin.
VSS	12, 31	6, 30, 31	6, 29	P	—	Ground reference for logic and I/O pins.
VDD	11, 32	7, 8, 28, 29	7, 28	P	—	Positive supply for logic and I/O pins.
VUSB	18	37	37	O	—	Internal USB 3.3V voltage regulator output.
NC/ICCK/ICPGC[3]	—	—	12			No Connect or dedicated ICD/ICSP™ port clock.
ICCK				I/O	ST	In-Circuit Debugger clock.
ICPGC				I/O	ST	ICSP programming clock.
NC/ICDT/ICPGD[3]	—	—	13			No Connect or dedicated ICD/ICSP port clock.
ICDT				I/O	ST	In-Circuit Debugger data.
ICPGD				I/O	ST	ICSP programming data.
NC/$\overline{ICRST}$/ICVPP[3]	—	—	33			No Connect or dedicated ICD/ICSP port Reset.
$\overline{ICRST}$				I	—	Master Clear (Reset) input.
ICVPP				P	—	Programming voltage input.
NC/ICPORTS[3]	—	—	34	P	—	No Connect or 28-pin device emulation.
ICPORTS						Enable 28-pin device emulation when connected to VSS.
NC	—	13	—	—	—	No Connect.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: Alternate assignment for CCP2 when CCP2MX Configuration bit is cleared.

2: Default assignment for CCP2 when CCP2MX Configuration bit is set.

3: These pins are No Connect unless the ICPRT Configuration bit is set. For NC/ICPORTS, the pin is No Connect unless ICPRT is set and the DEBUG Configuration bit is cleared.

2.0 OSCILLATOR CONFIGURATIONS

2.1 Overview

Devices in the PIC18F2455/2550/4455/4550 family incorporate a different oscillator and microcontroller clock system than previous PIC18F devices. The addition of the USB module, with its unique requirements for a stable clock source, make it necessary to provide a separate clock source that is compliant with both USB low-speed and full-speed specifications.

To accommodate these requirements, PIC18F2455/2550/4455/4550 devices include a new clock branch to provide a 48 MHz clock for full-speed USB operation. Since it is driven from the primary clock source, an additional system of prescalers and postscalers has been added to accommodate a wide range of oscillator frequencies. An overview of the oscillator structure is shown in Figure 2-1.

Other oscillator features used in PIC18 enhanced microcontrollers, such as the Internal oscillator block and clock switching, remain the same. They are discussed later in this chapter.

2.1.1 OSCILLATOR CONTROL

The operation of the oscillator in PIC18F2455/2550/4455/4550 devices is controlled through two Configuration registers and two control registers. Configuration registers, CONFIG1L and CONFIG1H, select the oscillator mode and USB prescaler/postscaler options. As Configuration bits, these are set when the device is programmed and left in that configuration until the device is reprogrammed.

The OSCCON register (Register 2-2) selects the Active Clock mode; it is primarily used in controlling clock switching in power-managed modes. Its use is discussed in **Section 2.4.1 "Oscillator Control Register"**.

The OSCTUNE register (Register 2-1) is used to trim the INTRC frequency source, as well as select the low-frequency clock source that drives several special features. Its use is described in **Section 2.2.5.2 "OSCTUNE Register"**.

2.2 Oscillator Types

PIC18F2455/2550/4455/4550 devices can be operated in twelve distinct oscillator modes. In contrast with previous PIC18 enhanced microcontrollers, four of these modes involve the use of two oscillator types at once. Users can program the FOSC3:FOSC0 Configuration bits to select one of these modes:

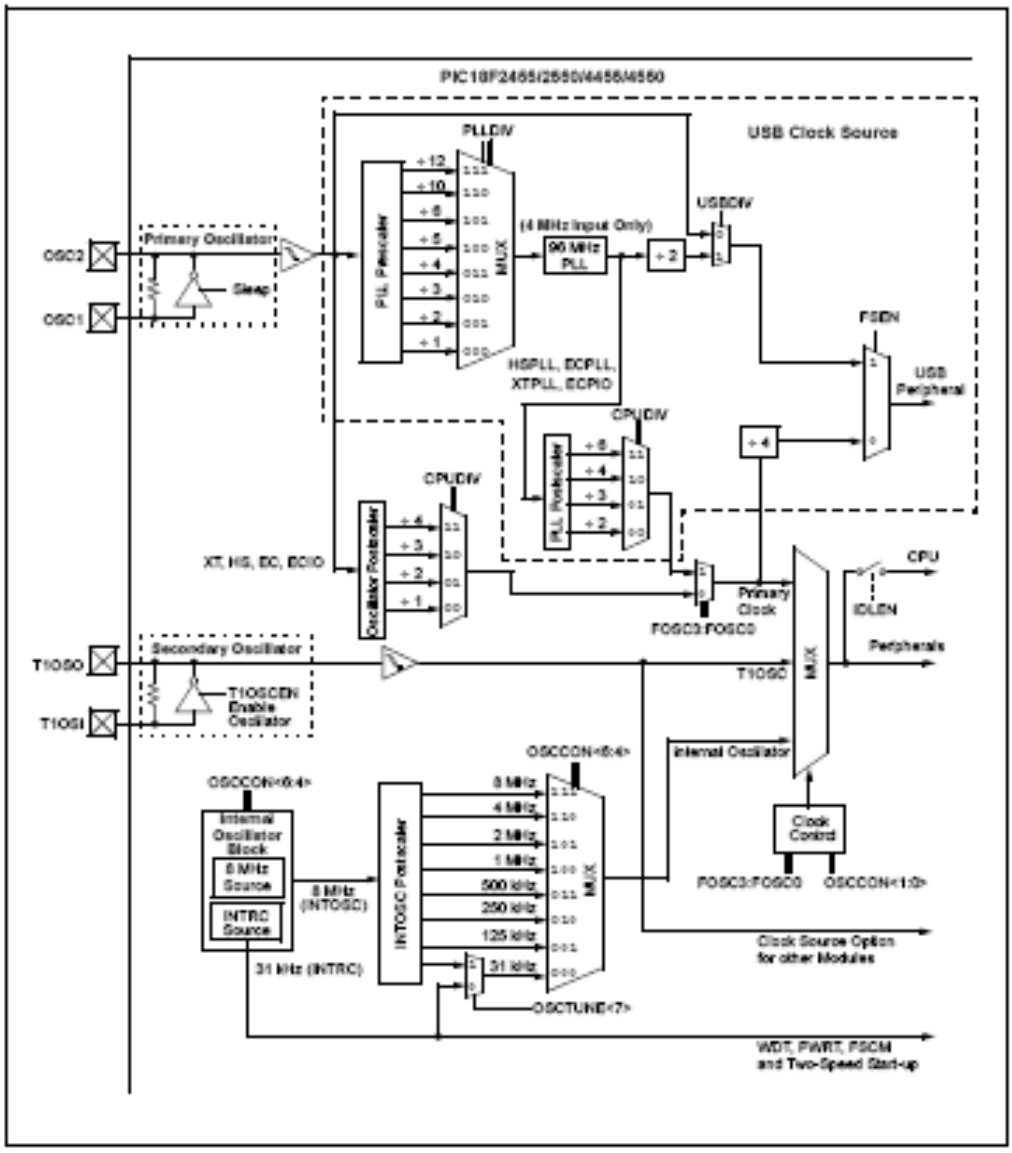
1. XT Crystal/Resonator
2. XTPLL Crystal/Resonator with PLL enabled
3. HS High-Speed Crystal/Resonator
4. HSPLL High-Speed Crystal/Resonator with PLL enabled
5. EC External Clock with Fosc/4 output
6. ECIO External Clock with I/O on RA6
7. ECPLL External Clock with PLL enabled and Fosc/4 output on RA6
8. ECPIO External Clock with PLL enabled, I/O on RA6
9. INTHS Internal Oscillator used as microcontroller clock source, HS Oscillator used as USB clock source
10. INTXT Internal Oscillator used as microcontroller clock source, XT Oscillator used as USB clock source
11. INTIO Internal Oscillator used as microcontroller clock source, EC Oscillator used as USB clock source, digital I/O on RA6
12. INTCKO Internal Oscillator used as microcontroller clock source, EC Oscillator used as USB clock source, Fosc/4 output on RA6

2.2.1 OSCILLATOR MODES AND USB OPERATION

Because of the unique requirements of the USB module, a different approach to clock operation is necessary. In previous PIC® devices, all core and peripheral clocks were driven by a single oscillator source; the usual sources were primary, secondary or the internal oscillator. With PIC18F2455/2550/4455/4550 devices, the primary oscillator becomes part of the USB module and cannot be associated to any other clock source. Thus, the USB module must be clocked from the primary clock source; however, the microcontroller core and other peripherals can be separately clocked from the secondary or internal oscillators as before.

Because of the timing requirements imposed by USB, an internal clock of either 6 MHz or 48 MHz is required while the USB module is enabled. Fortunately, the microcontroller and other peripherals are not required to run at this clock speed when using the primary oscillator. There are numerous options to achieve the USB module clock requirement and still provide flexibility for clocking the rest of the device from the primary oscillator source. These are detailed in **Section 2.3 "Oscillator Settings for USB"**.

FIGURE 2-1: PIC18F2455/2550/4455/4550 CLOCK DIAGRAM



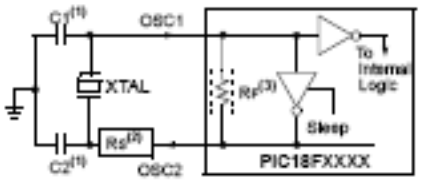
2.2.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In HS, HSPLL, XT and XTPLL Oscillator modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation. Figure 2-2 shows the pin connections.

The oscillator design requires the use of a parallel cut crystal.

Note:	Use of a series cut crystal may give a frequency out of the crystal manufacturer's specifications.

FIGURE 2-2: CRYSTAL/CERAMIC RESONATOR OPERATION (XT, HS OR HSPLL CONFIGURATION)



Note 1: See Table 2-1 and Table 2-2 for initial values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.
3: RF varies with the oscillator mode chosen.

TABLE 2-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Typical Capacitor Values Used:			
Mode	Freq	OSC1	OSC2
XT	4.0 MHz	33 pF	33 pF
HS	8.0 MHz	27 pF	27 pF
	16.0 MHz	22 pF	22 pF
Capacitor values are for design guidance only.			
These capacitors were tested with the resonators listed below for basic start-up and operation. **These values are not optimized.**			
Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.			
See the notes following Table 2-2 for additional information.			
Resonators Used:			
4.0 MHz			
8.0 MHz			
16.0 MHz			

TABLE 2-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

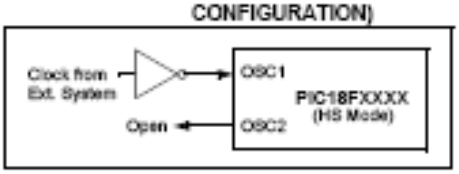
Osc Type	Crystal Freq	Typical Capacitor Values Tested:	
		C1	C2
XT	4 MHz	27 pF	27 pF
HS	4 MHz	27 pF	27 pF
	8 MHz	22 pF	22 pF
	20 MHz	15 pF	15 pF
Capacitor values are for design guidance only.			
These capacitors were tested with the crystals listed below for basic start-up and operation. **These values are not optimized.**			
Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.			
See the notes following this table for additional information.			
Crystals Used:			
4 MHz			
8 MHz			
20 MHz			

Note 1:	Higher capacitance increases the stability of oscillator but also increases the start-up time.
2:	When operating below 3V VDD, or when using certain ceramic resonators at any voltage, it may be necessary to use the HS mode or switch to a crystal oscillator.
3:	Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
4:	RS may be required to avoid overdriving crystals with low drive level specification.
5:	Always verify oscillator performance over the VDD and temperature range that is expected for the application.

An internal postscaler allows users to select a clock frequency other than that of the crystal or resonator. Frequency division is determined by the CPUDIV Configuration bits. Users may select a clock frequency of the oscillator frequency, or 1/2, 1/3 or 1/4 of the frequency.

An external clock may also be used when the microcontroller is in HS Oscillator mode. In this case, the OSC2/CLKO pin is left open (Figure 2-3).

FIGURE 2-3: EXTERNAL CLOCK INPUT OPERATION (HS OSC CONFIGURATION)



2.2.3 EXTERNAL CLOCK INPUT

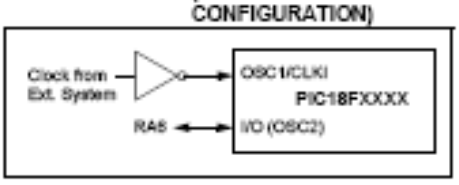
The EC, ECIO, ECPLL and ECPIO Oscillator modes require an external clock source to be connected to the OSC1 pin. There is no oscillator start-up time required after a Power-on Reset or after an exit from Sleep mode.

In the EC and ECPLL Oscillator modes, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic. Figure 2-4 shows the pin connections for the EC Oscillator mode.

FIGURE 2-4: EXTERNAL CLOCK INPUT OPERATION (EC AND ECPLL CONFIGURATION)

The ECIO and ECPIO Oscillator modes function like the EC and ECPLL modes, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6). Figure 2-5 shows the pin connections for the ECIO Oscillator mode.

FIGURE 2-5: EXTERNAL CLOCK INPUT OPERATION (ECIO AND ECPIO CONFIGURATION)



The internal postscaler for reducing clock frequency in XT and HS modes is also available in EC and ECIO modes.

2.2.4 PLL FREQUENCY MULTIPLIER

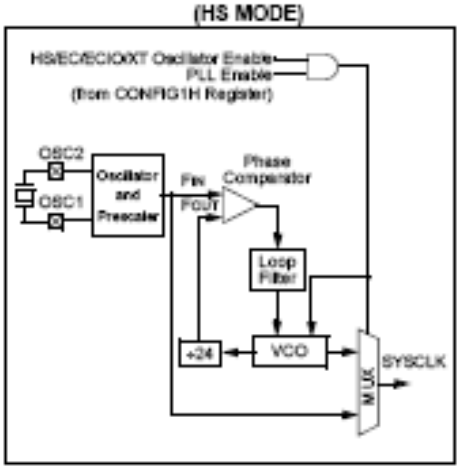
PIC18F2455/2550/4255/4550 devices include a Phase Locked Loop (PLL) circuit. This is provided specifically for USB applications with lower speed oscillators and can also be used as a microcontroller clock source.

The PLL is enabled in HSPLL, XTPLL, ECPLL and ECPIO Oscillator modes. It is designed to produce a fixed 96 MHz reference clock from a fixed 4 MHz input. The output can then be divided and used for both the USB and the microcontroller core clock. Because the PLL has a fixed frequency input and output, there are eight prescaling options to match the oscillator input frequency to the PLL.

There is also a separate postscaler option for deriving the microcontroller clock from the PLL. This allows the USB peripheral and microcontroller to use the same oscillator input and still operate at different clock speeds. In contrast to the postscaler for XT, HS and EC modes, the available options are 1/2, 1/3, 1/4 and 1/6 of the PLL output.

The HSPLL, ECPLL and ECPIO modes make use of the HS mode oscillator for frequencies up to 48 MHz. The prescaler divides the oscillator input by up to 12 to produce the 4 MHz drive for the PLL. The XTPLL mode can only use an input frequency of 4 MHz which drives the PLL directly.

FIGURE 2-6: PLL BLOCK DIAGRAM (HS MODE)



4.0 RESET

The PIC18F2455/2550/4455/4550 devices differentiate between various kinds of Reset:

a) Power-on Reset (POR)
b) MCLR Reset during normal operation
c) MCLR Reset during power-managed modes
d) Watchdog Timer (WDT) Reset (during execution)
e) Programmable Brown-out Reset (BOR)
f) RESET Instruction
g) Stack Full Reset
h) Stack Underflow Reset

This section discusses Resets generated by MCLR, POR and BOR and covers the operation of the various start-up timers. Stack Reset events are covered in **Section 6.1.2.4 "Stack Full and Underflow Resets"**. WDT Resets are covered in **Section 25.2 "Watchdog Timer (WDT)"**.

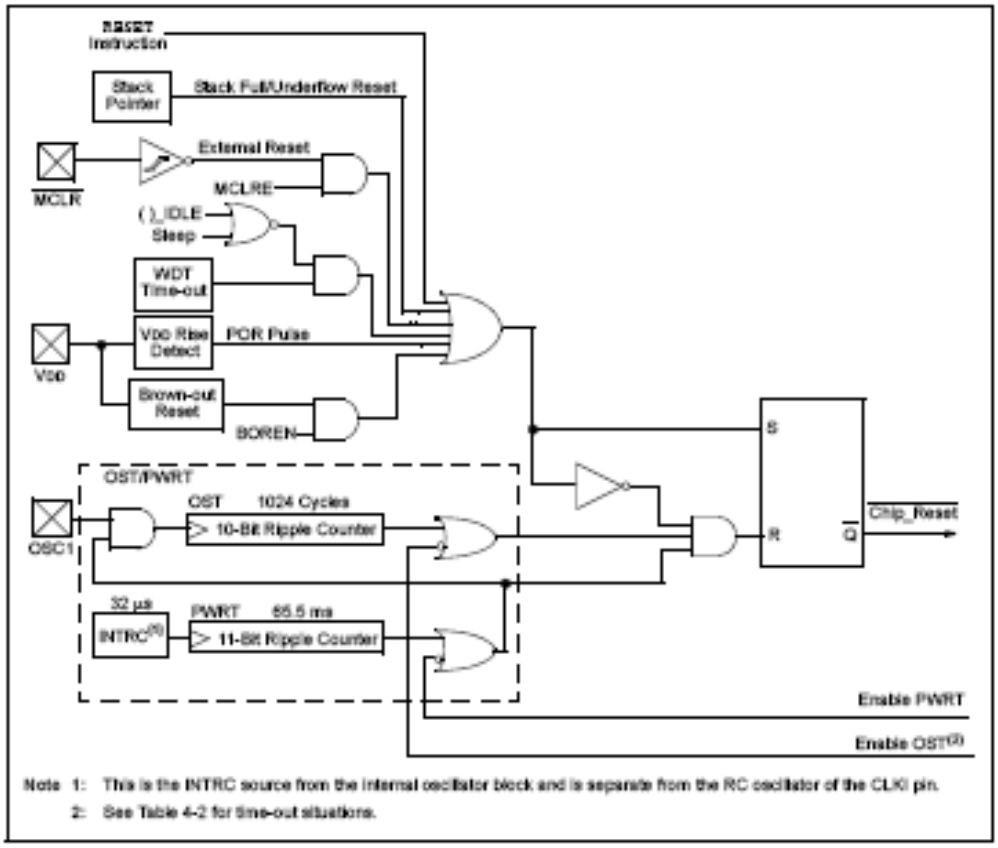
A simplified block diagram of the on-chip Reset circuit is shown in Figure 4-1.

4.1 RCON Register

Device Reset events are tracked through the RCON register (Register 4-1). The lower five bits of the register indicate that a specific Reset event has occurred. In most cases, these bits can only be cleared by the event and must be set by the application after the event. The state of these flag bits, taken together, can be read to indicate the type of Reset that just occurred. This is described in more detail in **Section 4.6 "Reset State of Registers"**.

The RCON register also has control bits for setting interrupt priority (IPEN) and software control of the BOR (SBOREN). Interrupt priority is discussed in **Section 9.0 "Interrupts"**. BOR is covered in **Section 4.4 "Brown-out Reset (BOR)"**.

FIGURE 4-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: This is the INTRC source from the internal oscillator block and is separate from the RC oscillator of the CLKI pin.
2: See Table 4-2 for time-out situations.

4.2 Master Clear Reset (MCLR)

The MCLR pin provides a method for triggering an external Reset of the device. A Reset is generated by holding the pin low. These devices have a noise filter in the MCLR Reset path which detects and ignores small pulses.

The MCLR pin is not driven low by any internal Resets, including the WDT.

In PIC18F2455/2550/4455/4550 devices, the MCLR input can be disabled with the MCLRE Configuration bit. When MCLR is disabled, the pin becomes a digital input. See **Section 10.6 "PORTE, TRISE and LATE Registers"** for more information.

4.3 Power-on Reset (POR)

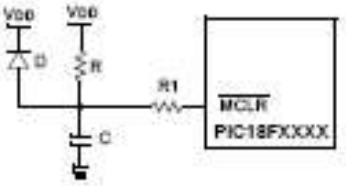
A Power-on Reset pulse is generated on-chip whenever VDD rises above a certain threshold. This allows the device to start in the initialized state when VDD is adequate for operation.

To take advantage of the POR circuitry, tie the MCLR pin through a resistor (1 kΩ to 10 kΩ) to VDD. This will eliminate external RC components usually needed to create a Power-on Reset delay. A minimum rise rate for VDD is specified (parameter D004, **Section 28.1 "DC Characteristics"**). For a slow rise time, see Figure 4-2.

When the device starts normal operation (i.e., exits the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

POR events are captured by the POR bit (RCON<1>). The state of the bit is set to '0' whenever a POR occurs; it does not change for any other Reset event. POR is not reset to '1' by any hardware event. To capture multiple events, the user manually resets the bit to '1' in software following any POR.

FIGURE 4-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



Note 1: External Power-on Reset circuit is required only if the VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.

2: R < 40 kΩ is recommended to make sure that the voltage drop across R does not violate the device's electrical specification.

3: R1 ≥ 1 kΩ will limit any current flowing into MCLR from external capacitor C, in the event of MCLR/VPP pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

5.0 MEMORY ORGANIZATION

There are three types of memory in PIC18 enhanced microcontroller devices:

- Program Memory
- Data RAM
- Data EEPROM

As Harvard architecture devices, the data and program memories use separate busses; this allows for concurrent access of the two memory spaces. The data EEPROM, for practical purposes, can be regarded as a peripheral device, since it is addressed and accessed through a set of control registers.

Additional detailed information on the operation of the Flash program memory is provided in **Section 6.0 "Flash Program Memory"**. Data EEPROM is discussed separately in **Section 7.0 "Data EEPROM Memory"**.

5.1 Program Memory Organization

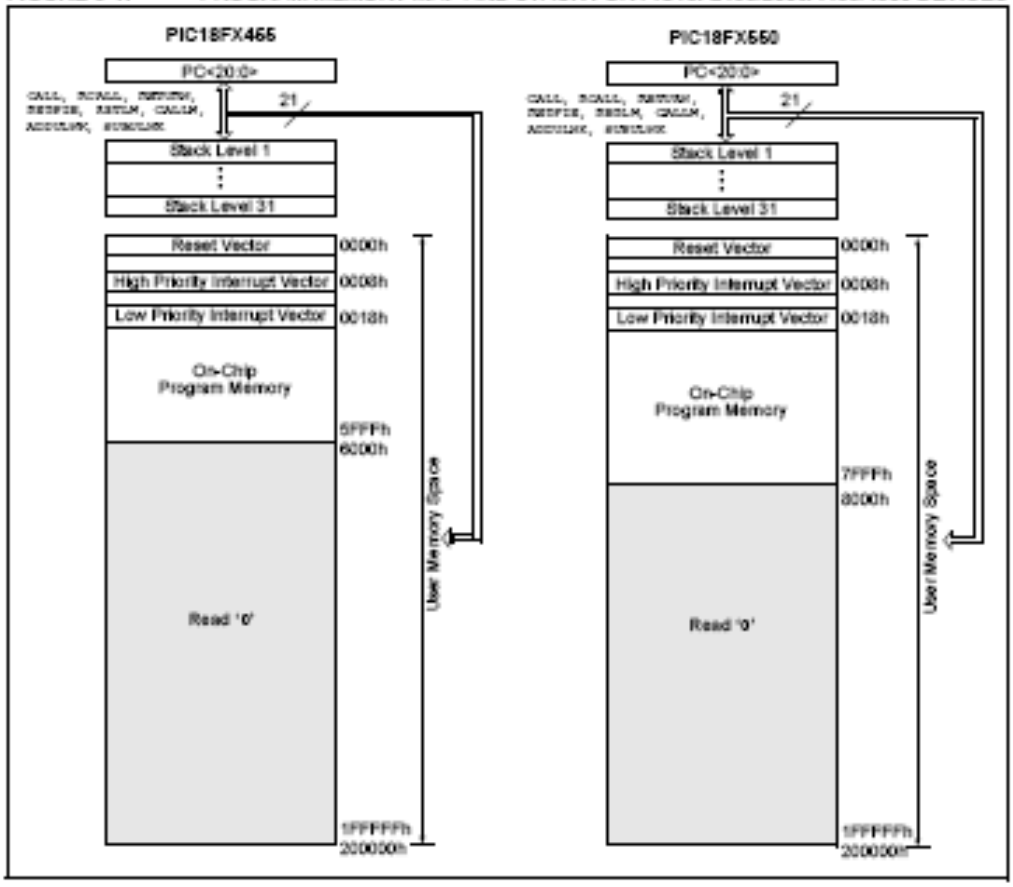
PIC18 microcontrollers implement a 21-bit program counter which is capable of addressing a 2-Mbyte program memory space. Accessing a location between the upper boundary of the physically implemented memory and the 2-Mbyte address will return all '0's (a NOP instruction).

The PIC18F2455 and PIC18F4455 each have 24 Kbytes of Flash memory and can store up to 12,288 single-word instructions. The PIC18F2550 and PIC18F4550 each have 32 Kbytes of Flash memory and can store up to 16,384 single-word instructions.

PIC18 devices have two interrupt vectors. The Reset vector address is at 0000h and the interrupt vector addresses are at 0008h and 0018h.

The program memory maps for PIC18FX455 and PIC18FX550 devices are shown in Figure 5-1.

FIGURE 5-1: PROGRAM MEMORY MAP AND STACK FOR PIC18F2455/2550/4455/4550 DEVICES



5.1.1 PROGRAM COUNTER

The Program Counter (PC) specifies the address of the instruction to fetch for execution. The PC is 21 bits wide and is contained in three separate 8-bit registers. The low byte, known as the PCL register, is both readable and writable. The high byte, or PCH register, contains the PC<15:8> bits; it is not directly readable or writable. Updates to the PCH register are performed through the PCLATH register. The upper byte is called PCU. This register contains the PC<20:16> bits; it is also not directly readable or writable. Updates to the PCU register are performed through the PCLATU register.

The contents of PCLATH and PCLATU are transferred to the program counter by any operation that writes PCL. Similarly, the upper two bytes of the program counter are transferred to PCLATH and PCLATU by an operation that reads PCL. This is useful for computed offsets to the PC (see **Section 5.1.4.1 "Computed GOTO"**).

The PC addresses bytes in the program memory. To prevent the PC from becoming misaligned with word instructions, the Least Significant bit of PCL is fixed to a value of '0'. The PC increments by 2 to address sequential instructions in the program memory.

The CALL, RCALL and GOTO program branch instructions write to the program counter directly. For these instructions, the contents of PCLATH and PCLATU are not transferred to the program counter.

5.1.2 RETURN ADDRESS STACK

The return address stack allows any combination of up to 31 program calls and interrupts to occur. The PC is pushed onto the stack when a CALL or RCALL instruction is executed or an interrupt is Acknowledged. The PC value is pulled off the stack on a RETURN, RETLW or a RETFIE instruction. PCLATU and PCLATH are not affected by any of the RETURN or CALL instructions.

The stack operates as a 31-word by 21-bit RAM and a 5-bit Stack Pointer, STKPTR. The stack space is not part of either program or data space. The Stack Pointer is readable and writable and the address on the top of the stack is readable and writable through the Top-of-Stack Special Function Registers. Data can also be pushed to, or popped from the stack, using these registers.

A CALL type instruction causes a push onto the stack. The Stack Pointer is first incremented and the location pointed to by the Stack Pointer is written with the contents of the PC (already pointing to the instruction following the CALL). A RETURN type instruction causes a pop from the stack. The contents of the location pointed to by the STKPTR are transferred to the PC and then the Stack Pointer is decremented.

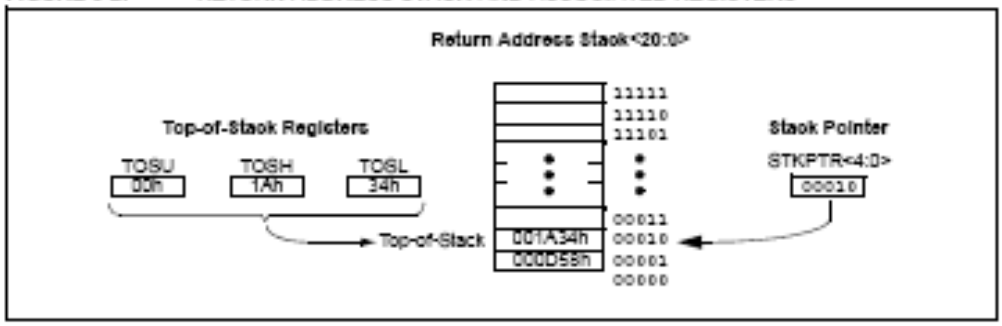
The Stack Pointer is initialized to '00000' after all Resets. There is no RAM associated with the location corresponding to a Stack Pointer value of '00000'; this is only a Reset value. Status bits indicate if the stack is full, has overflowed or has underflowed.

5.1.2.1 Top-of-Stack Access

Only the top of the return address stack (TOS) is readable and writable. A set of three registers, TOSU:TOSH:TOSL, hold the contents of the stack location pointed to by the STKPTR register (Figure 5-2). This allows users to implement a software stack if necessary. After a CALL, RCALL or interrupt, the software can read the pushed value by reading the TOSU:TOSH:TOSL registers. These values can be placed on a user-defined software stack. At return time, the software can return these values to TOSU:TOSH:TOSL and do a return.

The user must disable the global interrupt enable bits while accessing the stack to prevent inadvertent stack corruption.

FIGURE 5-2: RETURN ADDRESS STACK AND ASSOCIATED REGISTERS



5.2 PIC18 Instruction Cycle

5.2.1 CLOCKING SCHEME

The microcontroller clock input, whether from an internal or external source, is internally divided by four to generate four non-overlapping quadrature clocks (Q1, Q2, Q3 and Q4). Internally, the program counter is incremented on every Q1; the instruction is fetched from the program memory and latched into the Instruction Register (IR) during Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 5-3.

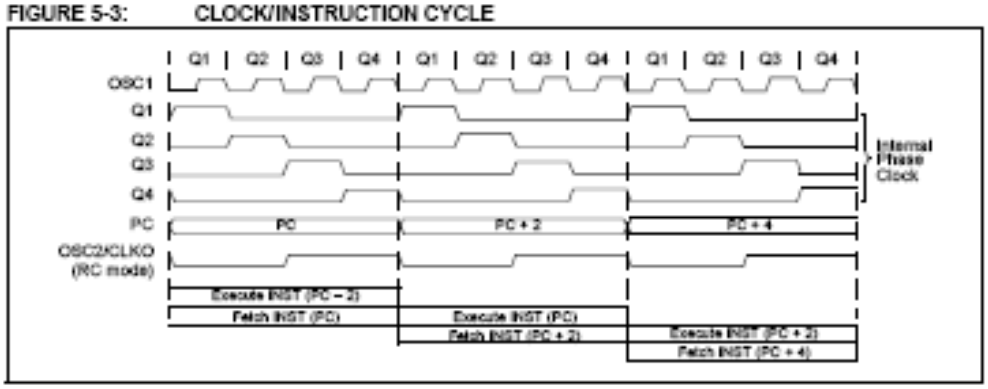
5.2.2 INSTRUCTION FLOW/PIPELINING

An "Instruction Cycle" consists of four Q cycles: Q1 through Q4. The instruction fetch and execute are pipelined in such a manner that a fetch takes one instruction cycle, while the decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 5-3).

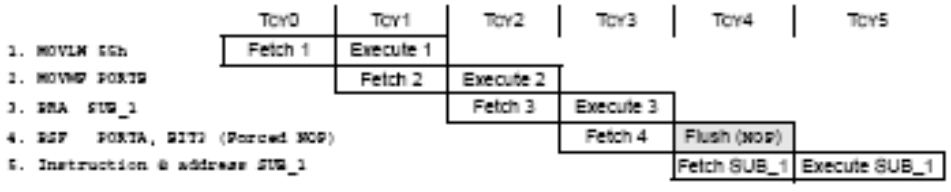
A fetch cycle begins with the Program Counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 5-3: CLOCK/INSTRUCTION CYCLE



EXAMPLE 5-3: INSTRUCTION PIPELINE FLOW



Note: All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

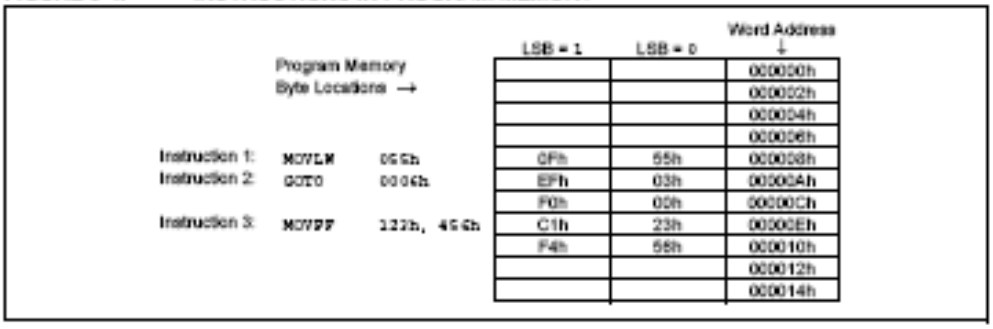
5.2.3 INSTRUCTIONS IN PROGRAM MEMORY

The program memory is addressed in bytes. Instructions are stored as two bytes or four bytes in program memory. The Least Significant Byte of an instruction word is always stored in a program memory location with an even address (LSb = 0). To maintain alignment with instruction boundaries, the PC increments in steps of 2 and the LSb will always read '0' (see **Section 6.1.1 "Program Counter"**).

Figure 5-4 shows an example of how instruction words are stored in the program memory.

The CALL and GOTO instructions have the absolute program memory address embedded into the instruction. Since instructions are always stored on word boundaries, the data contained in the instruction is a word address. The word address is written to PC<20:1>, which accesses the desired byte address in program memory. Instruction #2 in Figure 5-4 shows how the instruction, GOTO 0006h, is encoded in the program memory. Program branch instructions, which encode a relative address offset, operate in the same manner. The offset value stored in a branch instruction represents the number of single-word instructions that the PC will be offset by. **Section 28.0 "Instruction Set Summary"** provides further details of the instruction set.

FIGURE 5-4: INSTRUCTIONS IN PROGRAM MEMORY



5.2.4 TWO-WORD INSTRUCTIONS

The standard PIC18 instruction set has four two-word instructions: CALL, MOVFF, GOTO and LSFR. In all cases, the second word of the instructions always has '1111' as its four Most Significant bits; the other 12 bits are literal data, usually a data memory address.

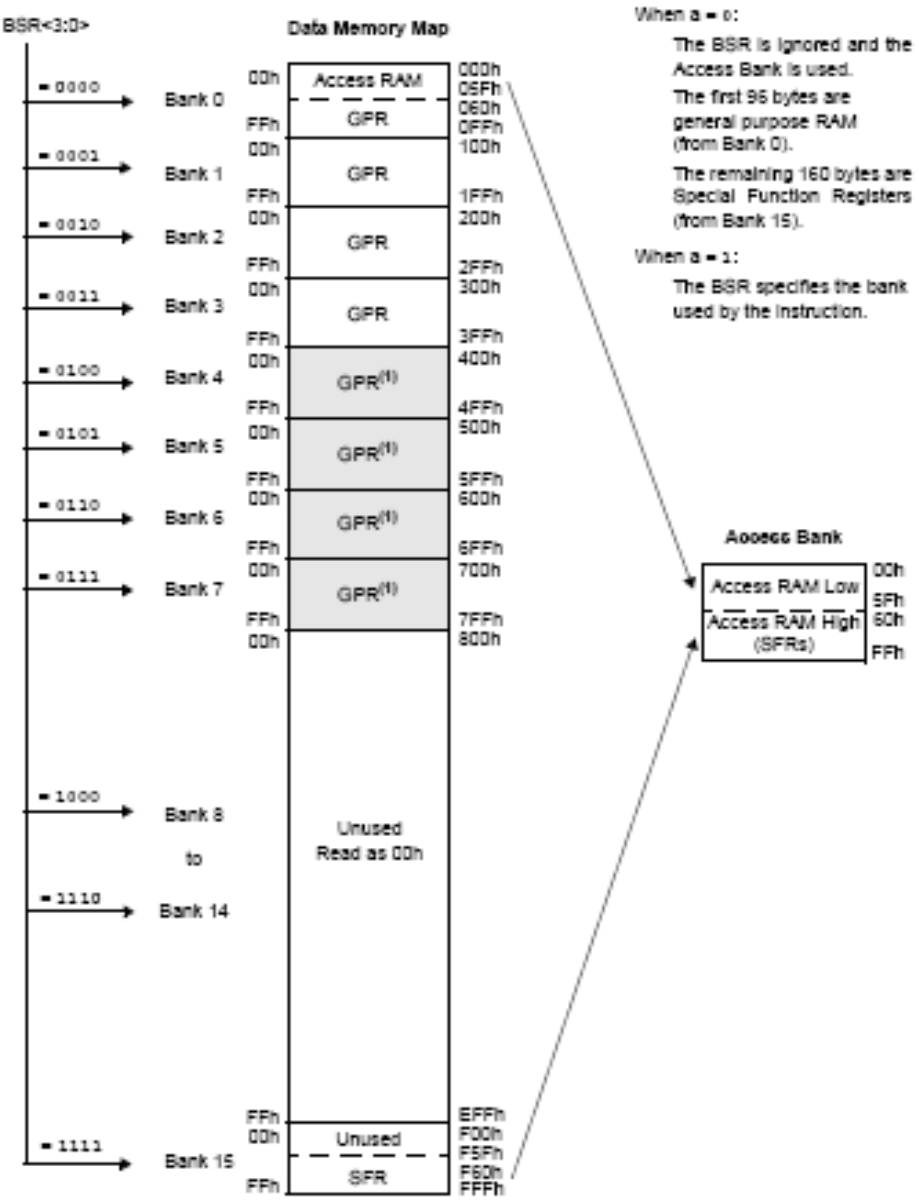
The use of '1111' in the 4 MSbs of an instruction specifies a special form of NOP. If the instruction is executed in proper sequence, immediately after the first word, the data in the second word is accessed and used by the instruction sequence. If the first word is skipped for some reason and the second word is executed by itself, a NOP is executed instead. This is necessary for cases when the two-word instruction is preceded by a conditional instruction that changes the PC. Example 5-4 shows how this works.

Note:	See **Section 6.5 "Program Memory and the Extended Instruction Set"** for information on two-word instruction in the extended instruction set.

EXAMPLE 5-4: TWO-WORD INSTRUCTIONS

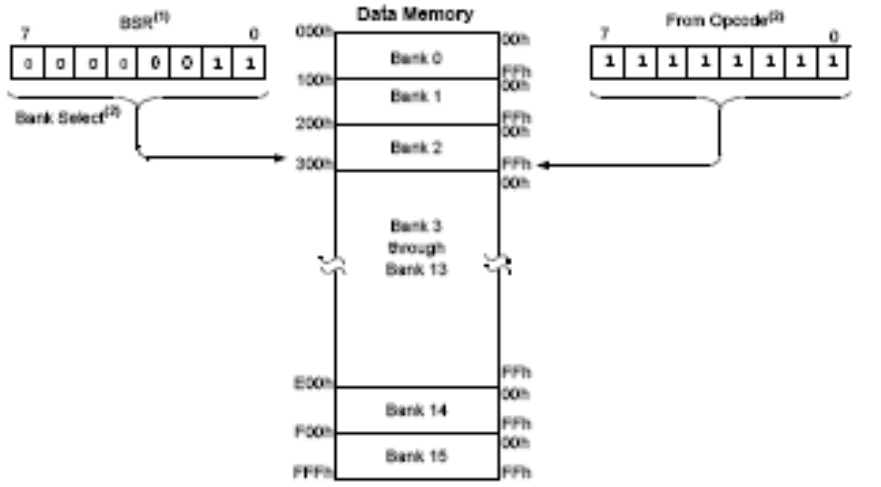
CASE 1:			
Object Code	**Source Code**		
0110 0110 0000 0000	TSTFSZ	REG1	; is RAM location 0?
1100 0001 0010 0011	MOVFF	REG1, REG2	; No, skip this word
1111 0100 0101 0110			; Execute this word as a NOP
0010 0100 0000 0000	ADDWF	REG1	; continue code
CASE 2:			
Object Code	**Source Code**		
0110 0110 0000 0000	TSTFSZ	REG1	; is RAM location 0?
1100 0001 0010 0011	MOVFF	REG1, REG2	; Yes, execute this word
1111 0100 0101 0110			; 2nd word of instruction
0010 0100 0000 0000	ADDWF	REG1	; continue code

FIGURE 5-5: DATA MEMORY MAP FOR PIC18F2455/2550/4455/4550 DEVICES



Note 1: These banks also serve as RAM buffer for USB operation. See Section 6.8.1 "USB RAM" for more information.

FIGURE 5-6: USE OF THE BANK SELECT REGISTER (DIRECT ADDRESSING)



Note 1: The Access RAM bit of the instruction can be used to force an override of the selected bank (BSR<3:0>) to the registers of the Access Bank.

2: The MOVFF instruction embeds the entire 12-bit address in the instruction.

5.3.3 ACCESS BANK

While the use of the BSR, with an embedded 8-bit address, allows users to address the entire range of data memory, it also means that the user must always ensure that the correct bank is selected. Otherwise, data may be read from or written to the wrong location. This can be disastrous if a GPR is the intended target of an operation but an SFR is written to instead. Verifying and/or changing the BSR for each read or write to data memory can become very inefficient.

To streamline access for the most commonly used data memory locations, the data memory is configured with an Access Bank, which allows users to access a mapped block of memory without specifying a BSR. The Access Bank consists of the first 96 bytes of memory (000h-5Fh) in Bank 0 and the last 160 bytes of memory (60h-FFh) in Block 15. The lower half is known as the "Access RAM" and is composed of GPRs. The upper half is where the device's SFRs are mapped. These two areas are mapped contiguously in the Access Bank and can be addressed in a linear fashion by an 8-bit address (Figure 5-5).

The Access Bank is used by core PIC18 instructions that include the Access RAM bit (the 'a' parameter in the instruction). When 'a' is equal to '1', the instruction uses the BSR and the 8-bit address included in the opcode for the data memory address. When 'a' is '0', however, the instruction is forced to use the Access Bank address map; the current value of the BSR is ignored entirely.

Using this "forced" addressing allows the instruction to operate on a data address in a single cycle without updating the BSR first. For 8-bit addresses of 60h and above, this means that users can evaluate and operate on SFRs more efficiently. The Access RAM below 60h is a good place for data values that the user might need to access rapidly, such as immediate computational results or common program variables. Access RAM also allows for faster and more code efficient context saving and switching of variables.

The mapping of the Access Bank is slightly different when the extended instruction set is enabled (XINST Configuration bit = 1). This is discussed in more detail in **Section 5.6.3 "Mapping the Access Bank in Indexed Literal Offset Mode"**.

5.3.4 GENERAL PURPOSE REGISTER FILE

PIC18 devices may have banked memory in the GPR area. This is data RAM which is available for use by all instructions. GPRs start at the bottom of Bank 0 (address 000h) and grow upwards towards the bottom of the SFR area. GPRs are not initialized by a Power-on Reset and are unchanged on all other Resets.

10.0 I/O PORTS

Depending on the device selected and features enabled, there are up to five ports available. Some pins of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

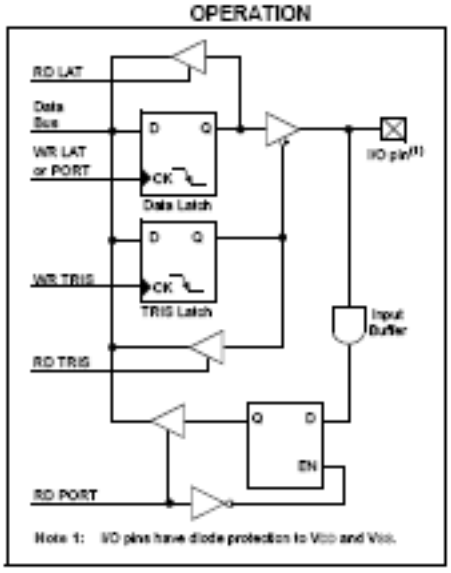
Each port has three registers for its operation. These registers are:

- TRIS register (data direction register)
- PORT register (reads the levels on the pins of the device)
- LAT register (output latch)

The Data Latch register (LATA) is useful for read-modify-write operations on the value driven by the I/O pins.

A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 10-1.

FIGURE 10-1: GENERIC I/O PORT OPERATION



Note 1: I/O pins have diode protection to VDD and VSS.

10.1 PORTA, TRISA and LATA Registers

PORTA is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins; writing to it will write to the port latch.

The Data Latch register (LATA) is also memory mapped. Read-modify-write operations on the LATA register read and write the latched output value for PORTA.

The RA4 pin is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA6 pin is multiplexed with the main oscillator pin; it is enabled as an oscillator or I/O pin by the selection of the main oscillator in Configuration Register 1H (see **Section 25.1 "Configuration Bits"** for details). When not used as a port pin, RA6 and its associated TRIS and LAT bits are read as '0'.

RA4 is also multiplexed with the USB module; it serves as a receiver input from an external USB transceiver. For details on configuration of the USB module, see **Section 17.2 "USB Status and Control"**.

Several PORTA pins are multiplexed with analog inputs, the analog VREF+ and VREF- inputs and the comparator voltage reference output. The operation of pins RA5 and RA3:RA0 as A/D converter inputs is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register 1).

Note:	On a Power-on Reset, RA5 and RA3:RA0 are configured as analog inputs and read as '0'. RA4 is configured as a digital input.

All other PORTA pins have TTL input levels and full CMOS output drivers.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE 10-1: INITIALIZING PORTA

```
CLRF    PORTA   ; Initialize PORTA by
                ; clearing output
                ; data latches
CLRF    LATA    ; Alternate method
                ; to clear output
                ; data latches
MOVLW   0Fh     ; Configure A/D
MOVWF   ADCON1  ; for digital inputs
MOVLW   07h     ; Configure comparators
MOVWF   CMCON   ; for digital input
MOVLW   0CFh    ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISA   ; Set RA<3:0> as inputs
                ; RA<5:4> as outputs
```

TABLE 10-1: PORTA I/O SUMMARY

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RA0/AN0	RA0	0	OUT	DIG	LATA<0> data output; not affected by analog input.
		1	IN	TTL	PORTA<0> data input; disabled when analog input enabled.
	AN0	1	IN	ANA	A/D input channel 0 and Comparator C1- input. Default configuration on POR; does not affect digital output.
RA1/AN1	RA1	0	OUT	DIG	LATA<1> data output; not affected by analog input.
		1	IN	TTL	PORTA<1> data input; reads '0' on POR.
	AN1	1	IN	ANA	A/D input channel 1 and Comparator C2- input. Default configuration on POR; does not affect digital output.
RA2/AN2/ VREF-/CVREF	RA2	0	OUT	DIG	LATA<2> data output; not affected by analog input. Disabled when CVREF output enabled.
		1	IN	TTL	PORTA<2> data input. Disabled when analog functions enabled; disabled when CVREF output enabled.
	AN2	1	IN	ANA	A/D input channel 2 and Comparator C2+ input. Default configuration on POR; not affected by analog output.
	VREF-	1	IN	ANA	A/D and comparator voltage reference low input.
	CVREF	x	OUT	ANA	Comparator voltage reference output. Enabling this feature disables digital I/O.
RA3/AN3/ VREF+	RA3	0	OUT	DIG	LATA<3> data output; not affected by analog input.
		1	IN	TTL	PORTA<3> data input; disabled when analog input enabled.
	AN3	1	IN	ANA	A/D input channel 3 and Comparator C1+ input. Default configuration on POR.
	VREF+	1	IN	ANA	A/D and comparator voltage reference high input.
RA4/T0CKI/ C1OUT/RCV	RA4	0	OUT	DIG	LATA<4> data output; not affected by analog input.
		1	IN	ST	PORTA<4> data input; disabled when analog input enabled.
	T0CKI	1	IN	ST	Timer0 clock input.
	C1OUT	0	OUT	DIG	Comparator 1 output; takes priority over port data.
	RCV	x	IN	TTL	External USB transceiver RCV input.
RA5/AN4/$\overline{SS}$/ HLVDIN/C2OUT	RA5	0	OUT	DIG	LATA<5> data output; not affected by analog input.
		1	IN	TTL	PORTA<5> data input; disabled when analog input enabled.
	AN4	1	IN	ANA	A/D input channel 4. Default configuration on POR.
	$\overline{SS}$	1	IN	TTL	Slave select input for SSP (MSSP module).
	HLVDIN	1	IN	ANA	High/Low-Voltage Detect external trip point input.
	C2OUT	0	OUT	DIG	Comparator 2 output; takes priority over port data.
OSC2/CLKO/ RA6	OSC2	x	OUT	ANA	Main oscillator feedback output connection (all XT and HS modes).
	CLKO	x	OUT	DIG	System cycle clock output (Fosc/4); available in EC, ECPLL and INTCKO modes.
	RA6	0	OUT	DIG	LATA<6> data output. Available only in ECIO, ECPIO and INTIO modes; otherwise, reads as '0'.
		1	IN	TTL	PORTA<6> data input. Available only in ECIO, ECPIO and INTIO modes; otherwise, reads as '0'.

Legend: OUT = Output, IN = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option)

10.2 PORTB, TRISB and LATB Registers

PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

The Data Latch register (LATB) is also memory mapped. Read-modify-write operations on the LATB register read and write the latched output value for PORTB.

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit, RBPU (INTCON2<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Note:	On a Power-on Reset, RB4:RB0 are configured as analog inputs by default and read as '0'; RB7:RB5 are configured as digital inputs. By programming the Configuration bit, PBADEN (CONFIG3H<1>), RB4:RB0 will alternatively be configured as digital inputs on POR.

Four of the PORTB pins (RB7:RB4) have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur. Any RB7:RB4 pin configured as an output is excluded from the interrupt-on-change comparison. The pins are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are ORed together to generate the RB Port Change Interrupt with Flag bit, RBIF (INTCON<0>).

The interrupt-on-change can be used to wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

a) Any read or write of PORTB (except with the `MOVFF (ANY), PORTB` instruction). This will end the mismatch condition.

b) Clear flag bit, RBIF.

A mismatch condition will continue to set flag bit, RBIF. Reading PORTB will end the mismatch condition and allow flag bit, RBIF, to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

Pins, RB2 and RB3, are multiplexed with the USB peripheral and serve as the differential signal outputs for an external USB transceiver (TRIS configuration). Refer to **Section 17.2.2.2 "External Transceiver"** for additional information on configuring the USB module for operation with an external transceiver.

RB4 is multiplexed with CSSPP, the chip select function for the Streaming Parallel Port (SPP) – TRIS setting. Details of its operation are discussed in **Section 18.0 "Streaming Parallel Port"**.

EXAMPLE 10-2: INITIALIZING PORTB

```
CLRF    PORTB   ; Initialize PORTB by
                ; clearing output
                ; data latches
CLRF    LATB    ; Alternate method
                ; to clear output
                ; data latches
MOVLW   0Eh     ; Set RB<4:0> as
MOVWF   ADCON1  ; digital I/O pins
                ; (required if config bit
                ; PBADEN is set)
MOVLW   0CFh    ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISB   ; Set RB<3:0> as inputs
                ; RB<5:4> as outputs
                ; RB<7:6> as inputs
```

TABLE 10-3: PORTB I/O SUMMARY (CONTINUED)

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RB6/KBI2/ PGC	RB6	0	OUT	DIG	LATB<6> data output.
		1	IN	TTL	PORTB<6> data input; weak pull-up when RBPU bit is cleared.
	KBI2	1	IN	TTL	Interrupt-on-pin change.
	PGC	x	IN	ST	Serial execution (ICSP™) clock input for ICSP and ICD operation.(3)
RB7/KBI3/ PGD	RB7	0	OUT	DIG	LATB<7> data output.
		1	IN	TTL	PORTB<7> data input; weak pull-up when RBPU bit is cleared.
	KBI3	1	IN	TTL	Interrupt-on-pin change.
	PGD	x	OUT	DIG	Serial execution data output for ICSP and ICD operation.(3)
		x	IN	ST	Serial execution data input for ICSP and ICD operation.(3)

Legend: OUT = Output, IN = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, I²C/SMB = I²C/SMBus input buffer, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option)

Note 1: Configuration on POR is determined by PBADEN Configuration bit. Pins are configured as analog inputs when PBADEN is set and digital inputs when PBADEN is cleared.

2: Alternate pin assignment for CCP2 when CCP2MX = 0. Default assignment is RC1.

3: All other pin functions are disabled when ICSP™ or ICD operation is enabled.

4: 40/44-pin devices only.

TABLE 10-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	54
LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	54
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	54
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RBIP	51
INTCON3	INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF	51
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	52
SPPCON(1)	—	—	—	—	—	—	SPPOWN	SPPEN	55
SPPCFG(1)	CLKCFG1	CLKCFG0	CSEN	CLK1EN	WS3	WS2	WS1	WS0	55
UCON	—	PPBRST	SE0	PKTDIS	USBEN	RESUME	SUSPND	—	55

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTB.

Note 1: These registers are unimplemented on 28-pin devices.

TABLE 10-3: PORTB I/O SUMMARY (CONTINUED)

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RB6/KBI2/ PGC	RB6	0	OUT	DIG	LATB<6> data output.
		1	IN	TTL	PORTB<6> data input; weak pull-up when RBPU bit is cleared.
	KBI2	1	IN	TTL	Interrupt-on-pin change.
	PGC	x	IN	ST	Serial execution (ICSP™) clock input for ICSP and ICD operation.(3)
RB7/KBI3/ PGD	RB7	0	OUT	DIG	LATB<7> data output.
		1	IN	TTL	PORTB<7> data input; weak pull-up when RBPU bit is cleared.
	KBI3	1	IN	TTL	Interrupt-on-pin change.
	PGD	x	OUT	DIG	Serial execution data output for ICSP and ICD operation.(3)
		x	IN	ST	Serial execution data input for ICSP and ICD operation.(3)

Legend: OUT = Output, IN = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, I^2C/SMB = I^2C/SMBus input buffer, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option)

Note 1: Configuration on POR is determined by PBADEN Configuration bit. Pins are configured as analog inputs when PBADEN is set and digital inputs when PBADEN is cleared.

2: Alternate pin assignment for CCP2 when CCP2MX = 0. Default assignment is RC1.

3: All other pin functions are disabled when ICSP™ or ICD operation is enabled.

4: 40/44-pin devices only.

TABLE 10-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	54
LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	54
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	54
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	51
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2	—	TMR0IP	—	RBIP	51
INTCON3	INT2IP	INT1IP	—	INT2IE	INT1IE	—	INT2IF	INT1IF	51
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	52
SPPCON(1)	—	—	—	—	—	—	SPPOWN	SPPEN	55
SPPCFG(1)	CLKCFG1	CLKCFG0	CSEN	CLK1EN	WS3	WS2	WS1	WS0	55
UCON	—	PPBRST	SE0	PKTDIS	USBEN	RESUME	SUSPND	—	55

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PORTB.

Note 1: These registers are unimplemented on 28-pin devices.

21.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) converter module has 10 inputs for the 28-pin devices and 13 for the 40/44-pin devices. This module allows conversion of an analog input signal to a corresponding 10-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)

The ADCON0 register, shown in Register 21-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 21-2, configures the functions of the port pins. The ADCON2 register, shown in Register 21-3, configures the A/D clock source, programmed acquisition time and justification.

REGISTER 21-1: ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS3:CHS0:** Analog Channel Select bits

0000 = Channel 0 (AN0)
0001 = Channel 1 (AN1)
0010 = Channel 2 (AN2)
0011 = Channel 3 (AN3)
0100 = Channel 4 (AN4)
0101 = Channel 5 (AN5)(1,2)
0110 = Channel 6 (AN6)(1,2)
0111 = Channel 7 (AN7)(1,2)
1000 = Channel 8 (AN8)
1001 = Channel 9 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
1100 = Channel 12 (AN12)
1101 = Unimplemented(2)
1110 = Unimplemented(2)
1111 = Unimplemented(2)

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

When ADON = 1:
1 = A/D conversion in progress
0 = A/D Idle

bit 0 **ADON:** A/D On bit

1 = A/D converter module is enabled
0 = A/D converter module is disabled

Note 1: These channels are not implemented on 28-pin devices.
2: Performing a conversion on unimplemented channels will return a floating input measurement.

REGISTER 21-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0(1)	R/W(1)	R/W(1)	R/W(1)
—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **VCFG1:** Voltage Reference Configuration bit (V_{REF-} source)
1 = V_{REF-} (AN2)
0 = V_{SS}

bit 4 **VCFG0:** Voltage Reference Configuration bit (V_{REF+} source)
1 = V_{REF+} (AN3)
0 = V_{DD}

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits:

PCFG3: PCFG0	AN12	AN11	AN10	AN9	AN8	AN7(2)	AN6(2)	AN5(2)	AN4	AN3	AN2	AN1	AN0
0000(1)	A	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A	A
0011	D	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	D	A	A	A	A	A	A	A	A	A
0111(1)	D	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input D = Digital I/O

Note 1: The POR value of the PCFG bits depends on the value of the PBADEN Configuration bit. When PBADEN = 1, PCFG<3:0> = 0000; when PBADEN = 0, PCFG<3:0> = 0111.
2: AN5 through AN7 are available only on 40/44-pin devices.

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (VDD and VSS) or the voltage level on the RA3/AN3/VREF+ and RA2/AN2/VREF-/CVREF pins.

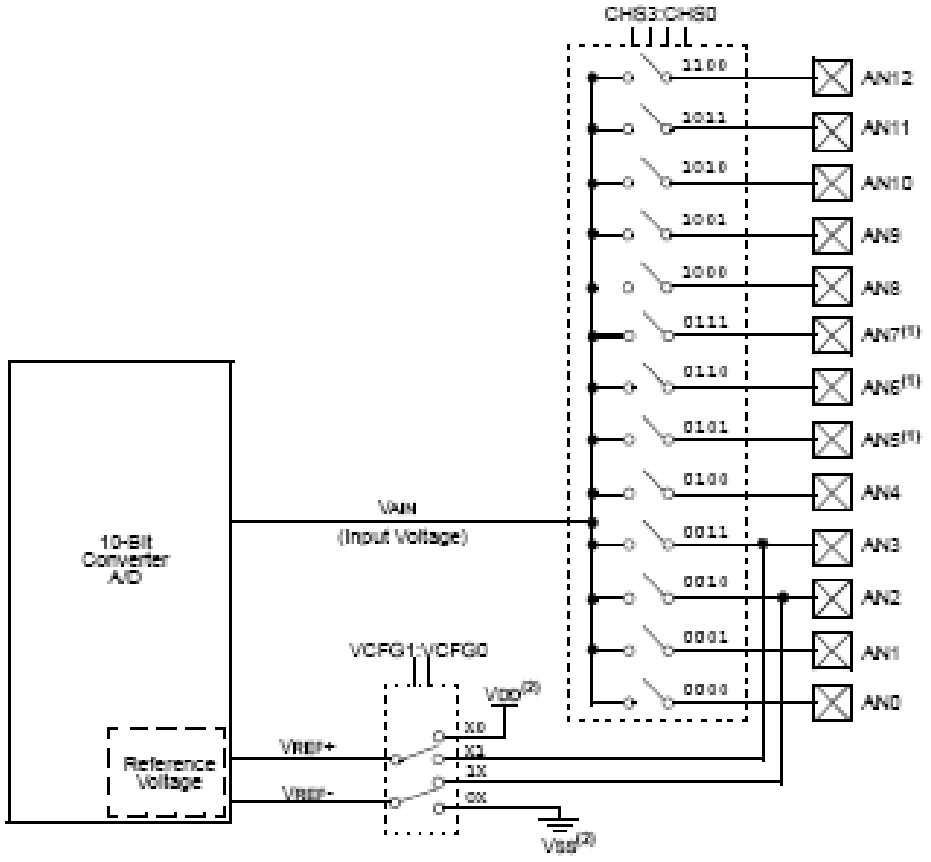
The A/D converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device Reset forces all registers to their Reset state. This forces the A/D module to be turned off and any conversion in progress is aborted.

Each port pin associated with the A/D converter can be configured as an analog input or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0 register) is cleared and A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 21-1.

FIGURE 21-1: A/D BLOCK DIAGRAM



Note 1: Channels AN5 through AN7 are not available on 28-pin devices.
2: I/O pins have diode protection to VDD and VSS.

APPENDIX C

LM358 Op-Amp Datasheet

LM158,A-LM258,A
LM358,A

LOW POWER DUAL OPERATIONAL AMPLIFIERS

- INTERNALLY FREQUENCY COMPENSATED
- LARGE DC VOLTAGE GAIN: 100dB
- WIDE BANDWIDTH (unity gain): 1.1MHz (temperature compensated)
- VERY LOW SUPPLY CURRENT/OP (500µA) ESSENTIALLY INDEPENDENT OF SUPPLY VOLTAGE
- LOW INPUT BIAS CURRENT: 20nA (temperature compensated)
- LOW INPUT OFFSET VOLTAGE: 2mV
- LOW INPUT OFFSET CURRENT: 2nA
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- DIFFERENTIAL INPUT VOLTAGE RANGE EQUAL TO THE POWER SUPPLY VOLTAGE
- LARGE OUTPUT VOLTAGE SWING 0V TO (Vcc - 1.5V)

N
DIP8
(Plastic Package)

D & S
SO8 & miniSO8
(Plastic Micropackage)

P
TSSOP8
(Thin Shrink Small Outline Package)

DESCRIPTION

These circuits consist of two independent, high gain, internally frequency compensated which were designed specifically to operate from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op-amp circuits which now can be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with the standard +5V which is used in logic systems and will easily provide the required interface electronics without requiring any additional power supply.

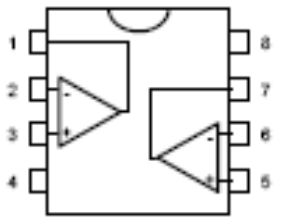
Inthe linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

ORDER CODE

Part Number	Temperature Range	Package			
		N	S	D	P
LM158,A	-55°C, +125°C	•		•	•
LM258,A	-40°C, +105°C	•		•	•
LM358,A	0°C, +70°C	•	•	•	•
Example : LM258N					

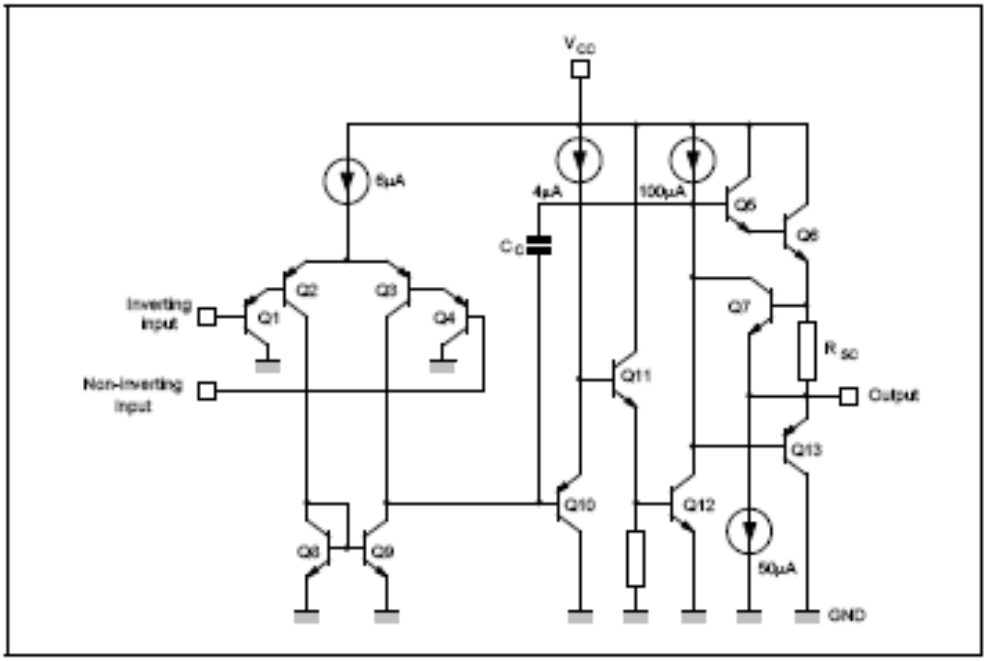
N = Dual in Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)
S = Small Outline Package (miniSO) only available in Tape & Reel (DT)
P = Thin Shrink Small Outline Package (TSSOP) - only available in Tape &Reel (PT)

PIN CONNECTIONS (top view)



1 - Output 1
2 - Inverting Input
3 - Non-inverting Input
4 - V_{CC}^-
5 - Non-inverting Input 2
6 - Inverting Input 2
7 - Output 2
8 - V_{CC}^+

SCHEMATIC DIAGRAM (1/2 LM158)



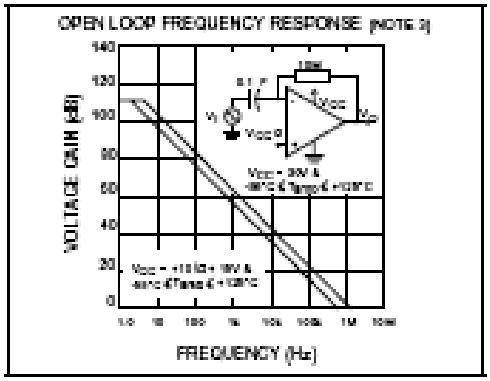
ABSOLUTE MAXIMUM RATINGS

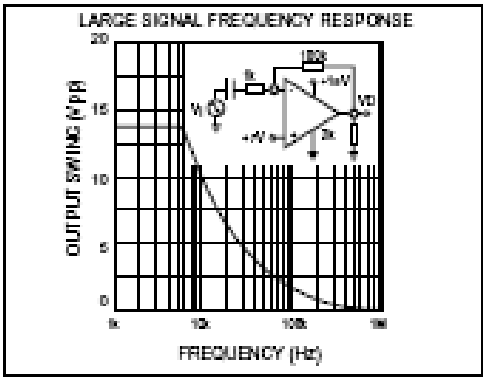
Symbol	Parameter	LM158,A	LM258,A	LM358,A	Unit
V_{CC}	Supply voltage	+/-16 or 32			V
V_i	Input Voltage	-0.3 to +32			V
V_{id}	Differential Input Voltage	+32			V
P_{tot}	Power Dissipation [1]	500			mW
	Output Short-circuit Duration [2]	Infinite			
I_{in}	Input Current [3]	50			mA
T_{oper}	Operating Free-air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to +150			°C

1. Power dissipation must be considered to ensure maximum junction temperature (T_j) is not exceeded.
2. Short-circuits from the output to V_{CC} can cause excessive heating if V_{CC} > 15V. The maximum output current is approximately 40mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuit on all amplifiers.
3. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diodes clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. this transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time duration than an input is driven negative.
This is not destructive and normal output will set up again for input voltage higher than -0.3V.

Symbol	Parameter	LM158A-LM258A LM358A			LM158-LM258 LM358			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	High Level Output Voltage (V_{CC}+ = 30V) T_{amb} = +25°C R_L = 2kΩ $T_{min} \le T_{amb} \le T_{max}$ T_{amb} = +25°C R_L = 10kΩ $T_{min} \le T_{amb} \le T_{max}$	26 26 27 27	27 28		26 26 27 27	27 28		V
V_{OL}	Low Level Output Voltage (R_L = 10kΩ) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		5	20 20		5	20 20	mV
SR	Slew Rate V_{CC} = 15V, V_i = 0.5 to 3V, R_L = 2kΩ, C_L = 100pF, unity Gain	0.3	0.6		0.3	0.6		V/µs
GBP	Gain Bandwidth Product V_{CC} = 30V, f =100kHz,V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF	0.7	1.1		0.7	1.1		MHz
THD	Total Harmonic Distortion f = 1kHz, A_V = 20dB, R_L = 2kΩ, V_o = $2V_{pp}$, C_L = 100pF, V_O = 2Vpp		0.02			0.02		%
e_n	Equivalent Input Noise Voltage f = 1kHz, R_s = 100Ω, V_{CC} = 30V		55			55		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input Offset Voltage Drift		7	15		7	30	µV/°C
DI_{io}	Input Offset Current Drift		10	200		10	300	pA/°C
V_{O1}/V_{O2}	Channel Separation - note 4) 1kHz ≤ f ≤ 20kHZ		120			120		dB

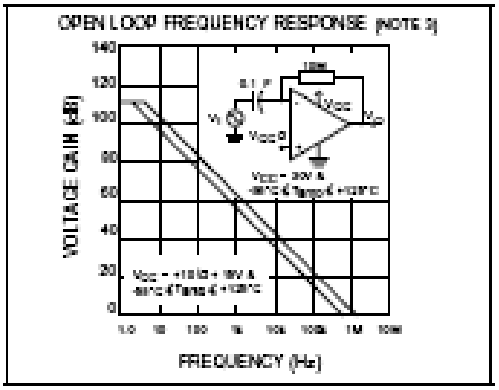
1. V_o = 1.4V, R_s = 0Ω, 5V < V_{CC}+ < 30V, 0 < V_{ic} < V_{CC}+ - 1.5V
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC}+ - 1.5V, but either or both inputs can go to +32V without damage.
4. Due to the proximity of external components insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

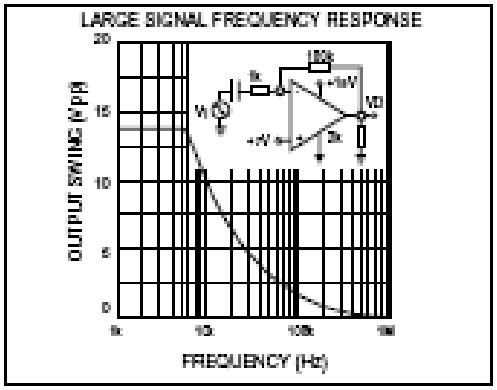


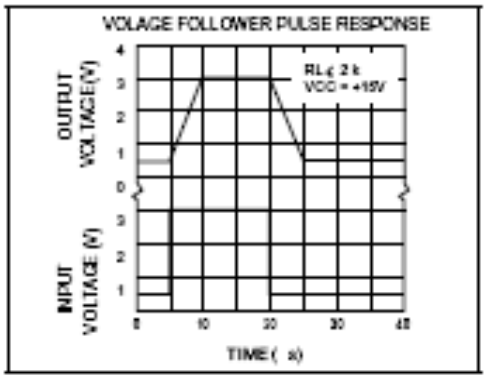


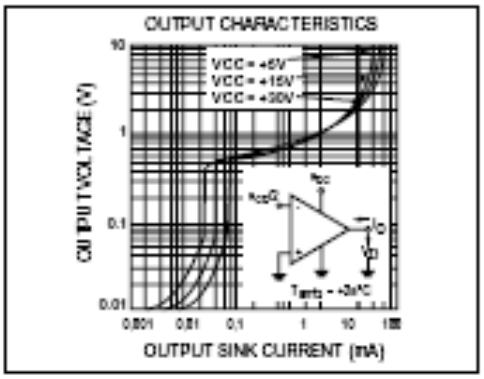
Symbol	Parameter	LM158A-LM258A LM358A			LM158-LM258 LM358			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	High Level Output Voltage (V_{CC}+ = 30V) T_{amb} = +25°C R_L = 2kΩ $T_{min} \le T_{amb} \le T_{max}$ T_{amb} = +25°C R_L = 10kΩ $T_{min} \le T_{amb} \le T_{max}$	26 26 27 27	27 28 		26 26 27 27	27 28 		V
V_{OL}	Low Level Output Voltage (R_L = 10kΩ) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		5	20 20		5	20 20	mV
SR	Slew Rate V_{CC} = 15V, V_i = 0.5 to 3V, R_L = 2kΩ, C_L = 100pF, unity Gain	0.3	0.6		0.3	0.6		V/µs
GBP	Gain Bandwidth Product V_{CC} = 30V, f =100kHz,V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF	0.7	1.1		0.7	1.1		MHz
THD	Total Harmonic Distortion f = 1kHz, A_V = 20dB, R_L = 2kΩ, V_o = $2V_{pp}$, C_L = 100pF, V_O = 2Vpp		0.02			0.02		%
e_n	Equivalent Input Noise Voltage f = 1kHz, R_s = 100Ω, V_{CC} = 30V		55			55		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input Offset Voltage Drift		7	15		7	30	µV/°C
DI_{io}	Input Offset Current Drift		10	200		10	300	pA/°C
V_{o1}/V_{o2}	Channel Separation - note 4) 1kHz ≤ f ≤ 20kHZ		120			120		dB

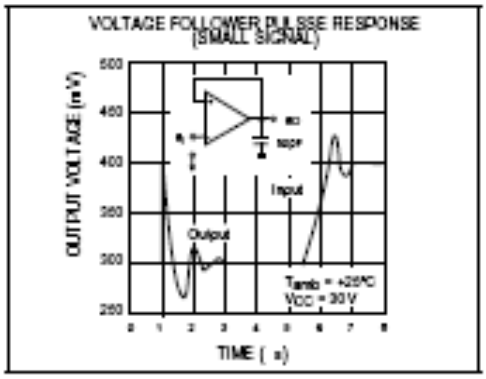
1. V_o = 1.4V, R_s = 0Ω, 5V < V_{CC}+ < 30V, 0 < V_{ic} < V_{CC}+ - 1.5V
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC}+ - 1.5V, but either or both inputs can go to +32V without damage.
4. Due to the proximity of external components insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

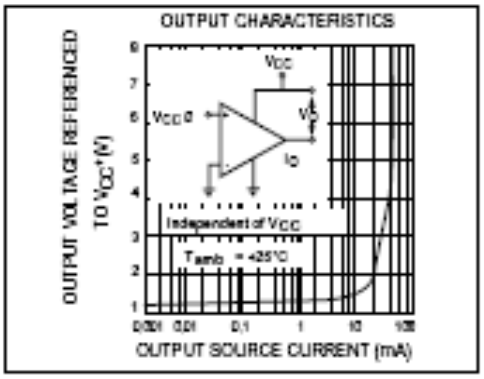


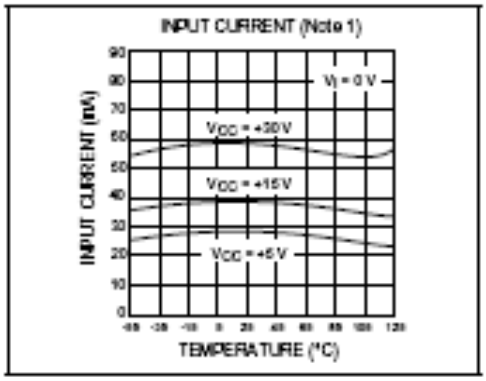


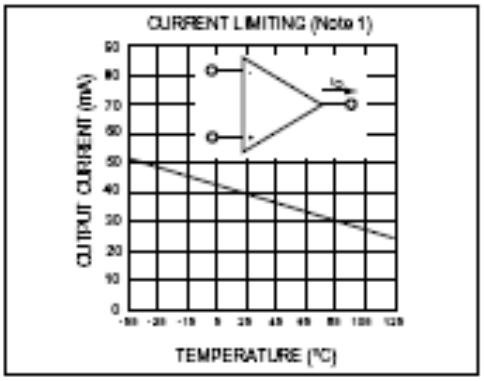

VOLAGE FOLLOWER PULSE RESPONSE
OUTPUT VOLTAGE(V)
INPUT VOLTAGE (V)
RL≥ 2 k
VCC = +15V
TIME (s)

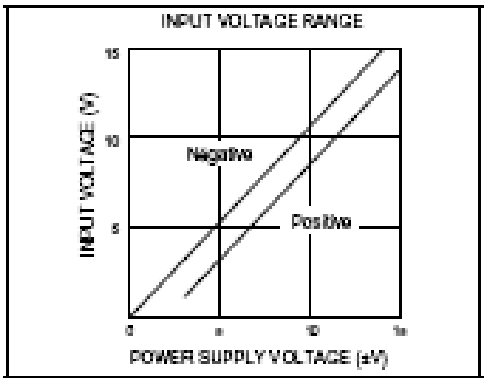

OUTPUT CHARACTERISTICS
VCC = +5V
VCC = +15V
VCC = +30V
OUTPUT VOLTAGE (V)
OUTPUT SINK CURRENT (mA)

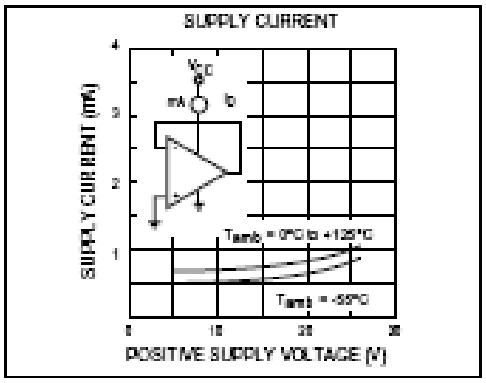

VOLTAGE FOLLOWER PULSE RESPONSE
(SMALL SIGNAL)
OUTPUT VOLTAGE (mV)
100pF
Input
Output
Tamb = +25°C
VCC = 30V
TIME (s)

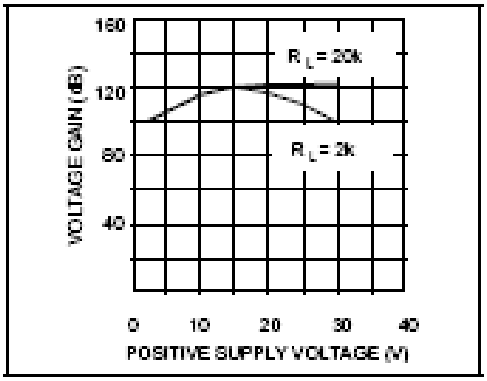

OUTPUT CHARACTERISTICS
OUTPUT VOLTAGE REFERENCED TO VCC+ (V)
VCC
Vo
Io
Independent of VCC
Tamb = +25°C
OUTPUT SOURCE CURRENT (mA)

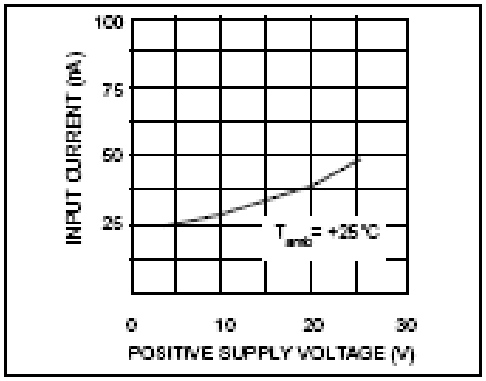

INPUT CURRENT (Note 1)
INPUT CURRENT (mA)
Vi = 0 V
VCC = +30V
VCC = +15V
VCC = +5 V
TEMPERATURE (°C)

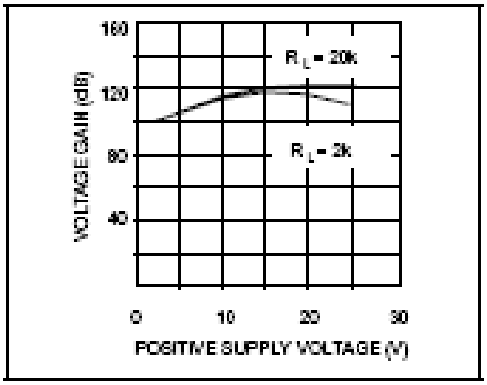

CURRENT LIMITING (Note 1)
OUTPUT CURRENT (mA)
TEMPERATURE (°C)

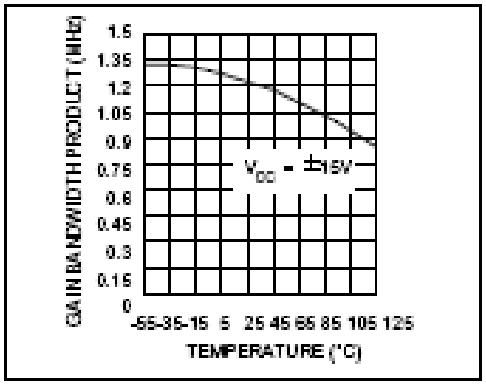

INPUT VOLTAGE RANGE
INPUT VOLTAGE (V)
Negative
Positive
POWER SUPPLY VOLTAGE (±V)

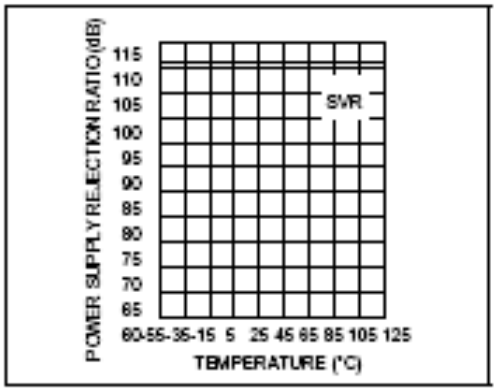

SUPPLY CURRENT
SUPPLY CURRENT (mA)
Tamb = 0°C to +125°C
Tamb = -55°C
POSITIVE SUPPLY VOLTAGE (V)

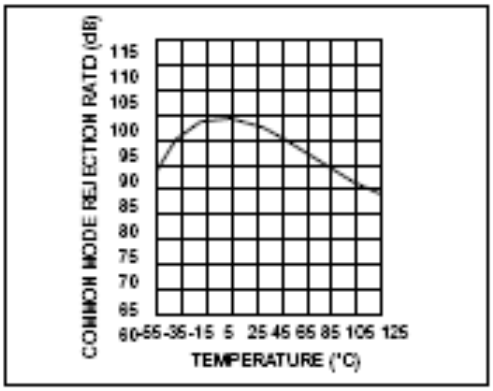

VOLTAGE GAIN (dB)
RL = 20k
RL = 2k
POSITIVE SUPPLY VOLTAGE (V)


INPUT CURRENT (nA)
Tamb = +25°C
POSITIVE SUPPLY VOLTAGE (V)


VOLTAGE GAIN (dB)
RL = 20k
RL = 2k
POSITIVE SUPPLY VOLTAGE (V)

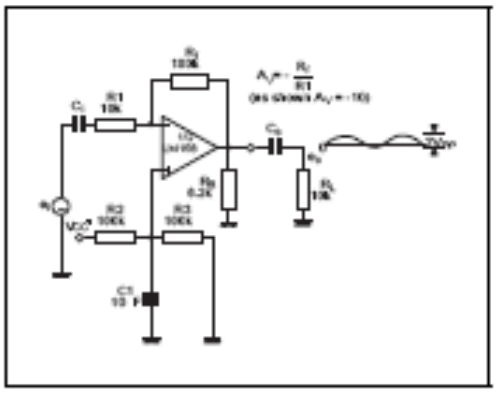

GAIN BANDWIDTH PRODUCT (MHz)
VCC = ±15V
TEMPERATURE (°C)



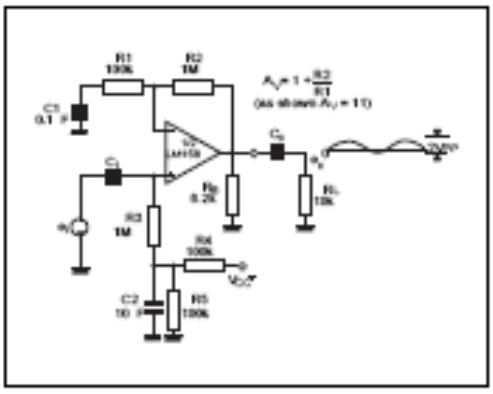


TYPICAL APPLICATIONS (single supply voltage) V_{cc} = +5V_{dc}

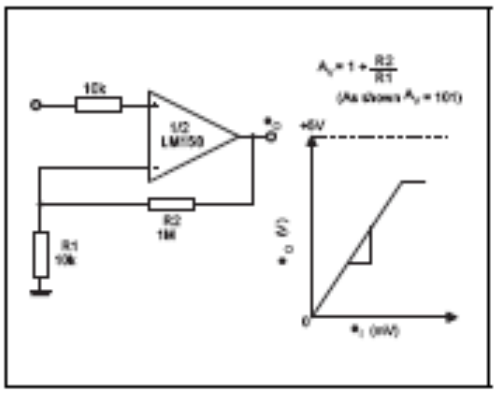
AC COUPLED INVERTING AMPLIFIER



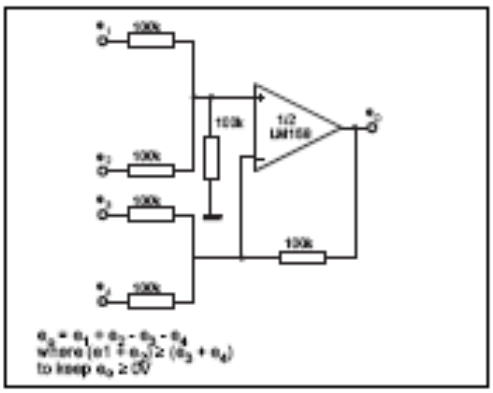
AC COUPLED NON-INVERTING AMPLIFIER



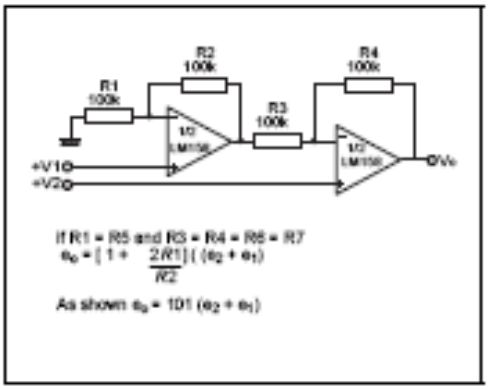
NON-INVERTING DC AMPLIFIER



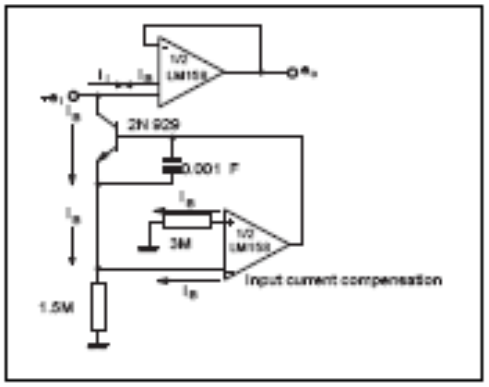
DC SUMMING AMPLIFIER



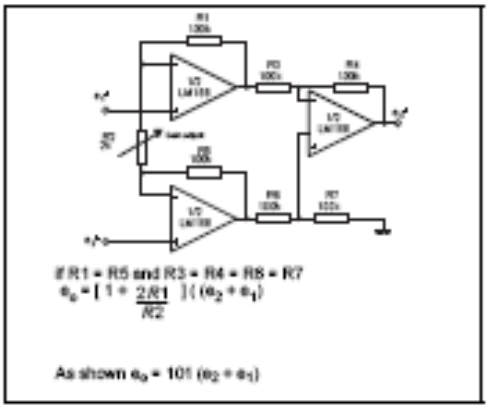
HIGH INPUT Z, DC DIFFERENTIAL AMPLIFIER



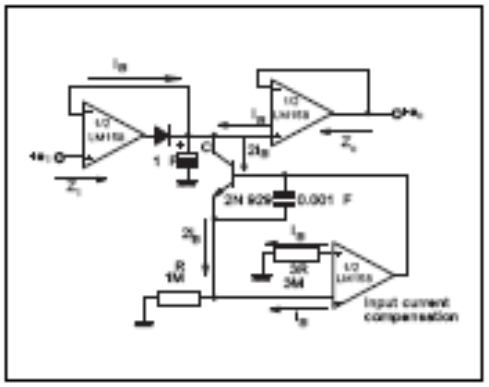
USING SYMMETRICAL AMPLIFIERS TO REDUCE INPUT CURRENT



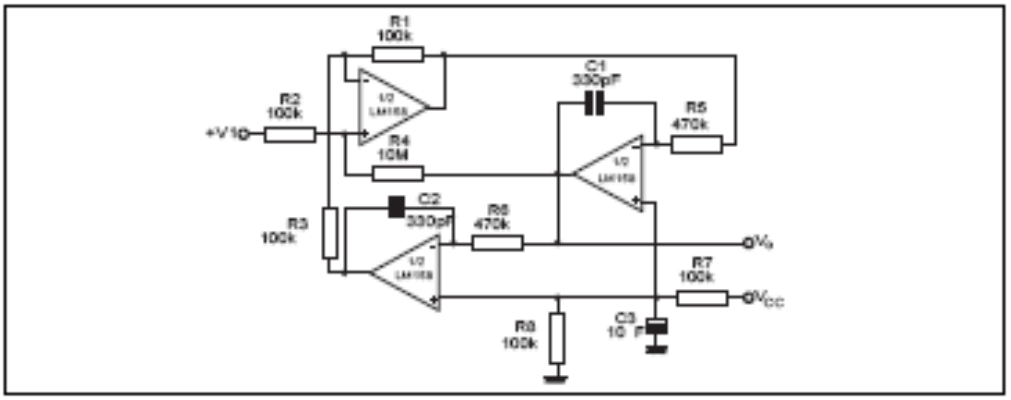
HIGH INPUT Z ADJUSTABLE GAIN DC INSTRUMENTATION AMPLIFIER



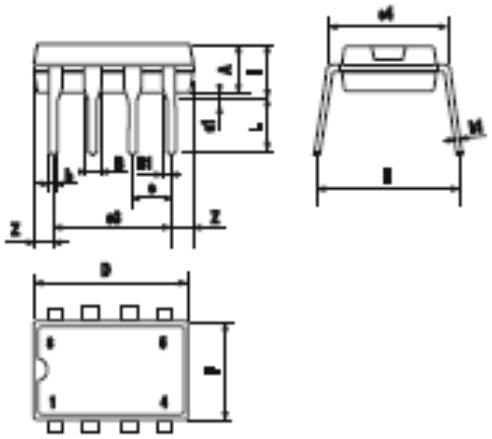
LOW DRIFT PEAK DETECTOR



ACTIVE BAND-PASS FILTER



PACKAGE MECHANICAL DATA
8 PINS - PLASTIC DIP



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

APPENDIX D

LM7805 Voltage Regulator Datasheet

FAIRCHILD
SEMICONDUCTOR®

March 2008

LM78XX/LM78XXA
3-Terminal 1A Positive Voltage Regulator

Features

- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

General Description

The LM78XX series of three terminal positive regulators are available in the TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

Ordering Information

Product Number	Output Voltage Tolerance	Package	Operating Temperature
LM7805CT	±4%	TO-220	-40°C to +125°C
LM7806CT			
LM7808CT			
LM7809CT			
LM7810CT			
LM7812CT			
LM7815CT			
LM7818CT			
LM7824CT			
LM7805ACT	±2%		0°C to +125°C
LM7806ACT			
LM7808ACT			
LM7809ACT			
LM7810ACT			
LM7812ACT			
LM7815ACT			
LM7818ACT			
LM7824ACT			

Block Diagram

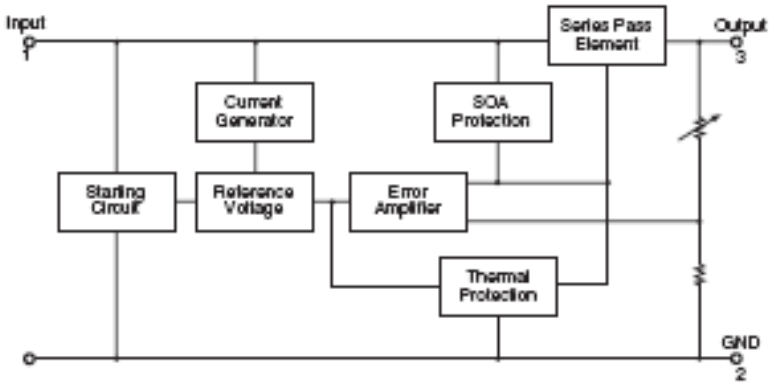


Figure 1.

Pin Assignment

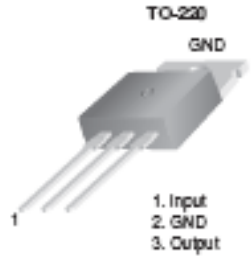


Figure 2.

Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Symbol	Parameter		Value	Unit
V_I	Input Voltage	V_O = 5V to 18V	35	V
		V_O = 24V	40	V
$R_{\theta JC}$	Thermal Resistance Junction-Cases (TO-220)		5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction-Air (TO-220)		65	°C/W
T_{OPR}	Operating Temperature Range	LM78xx	-40 to +125	°C
		LM78xxA	0 to +125	
T_{STG}	Storage Temperature Range		-65 to +150	°C

Electrical Characteristics (LM7805)

Refer to the test circuits. -40°C < T_J < 125°C, I_O = 500mA, V_I = 10V, C_I = 0.1µF, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_J = +25°C		4.8	5.0	5.2	V
		5mA ≤ I_O ≤ 1A, P_O ≤ 15W, V_I = 7V to 20V		4.75	5.0	5.25	
Regline	Line Regulation[1]	T_J = +25°C	V_O = 7V to 25V	–	4.0	100	mV
			V_I = 8V to 12V	–	1.6	50.0	
Regload	Load Regulation[1]	T_J = +25°C	I_O = 5mA to 1.5A	–	9.0	100	mV
			I_O = 250mA to 750mA	–	4.0	50.0	
I_Q	Quiescent Current	T_J = +25°C		–	5.0	8.0	mA
ΔI_Q	Quiescent Current Change	I_O = 5mA to 1A		–	0.03	0.5	mA
		V_I = 7V to 25V		–	0.3	1.3	
$\Delta V_O/\Delta T$	Output Voltage Drift[2]	I_O = 5mA		–	-0.8	–	mV/°C
V_N	Output Noise Voltage	f = 10Hz to 100kHz, T_A = +25°C		–	42.0	–	µV/V_O
RR	Ripple Rejection[2]	f = 120Hz, V_O = 8V to 18V		62.0	73.0	–	dB
V_{DROP}	Dropout Voltage	I_O = 1A, T_J = +25°C		–	2.0	–	V
r_O	Output Resistance[2]	f = 1kHz		–	15.0	–	mΩ
I_{SC}	Short Circuit Current	V_I = 35V, T_A = +25°C		–	230	–	mA
I_{PK}	Peak Current[2]	T_J = +25°C		–	2.2	–	A

Notes:

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.
2. These parameters, although guaranteed, are not 100% tested in production.

Electrical Characteristics (LM7805A) (Continued)

Refer to the test circuits. $0°C < T_J < 125°C$, I_O = 1A, V_I = 10V, C_I = 0.33µF, C_O = 0.1µF, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_J = +25°C		4.9	5.0	5.1	V
		I_O = 5mA to 1A, $P_O \leq$ 15W, V_I = 7.5V to 20V		4.8	5.0	5.2	
Regline	Line Regulation[19]	V_I = 7.5V to 25V, I_O = 500mA		–	5.0	50.0	mV
		V_I = 8V to 12V		–	3.0	50.0	
		T_J = +25°C	V_I = 7.3V to 20V	–	5.0	50.0	
			V_I = 8V to 12V	–	1.5	25.0	
Regload	Load Regulation[19]	T_J = +25°C, I_O = 5mA to 1.5A		–	9.0	100	mV
		I_O = 5mA to 1A		–	9.0	100	
		I_O = 250mA to 750mA		–	4.0	50.0	
I_Q	Quiescent Current	T_J = +25°C		–	5.0	6.0	mA
ΔI_Q	Quiescent Current Change	I_O = 5mA to 1A		–	–	0.5	mA
		V_I = 8V to 25V, I_O = 500mA		–	–	0.8	
		V_I = 7.5V to 20V, T_J = +25°C		–	–	0.8	
$\Delta V_O/\Delta T$	Output Voltage Drift[20]	I_O = 5mA		–	-0.8	–	mV/°C
V_N	Output Noise Voltage	f = 10Hz to 100kHz, T_A = +25°C		–	10.0	–	µV/V_O
RR	Ripple Rejection[20]	f = 120Hz, I_O = 500mA, V_I = 8V to 18V		–	68.0	–	dB
V_{DROP}	Dropout Voltage	I_O = 1A, T_J = +25°C		–	2.0	–	V
r_O	Output Resistance[20]	f = 1kHz		–	17.0	–	mΩ
I_{SC}	Short Circuit Current	V_I = 35V, T_A = +25°C		–	250	–	mA
I_{PK}	Peak Current[20]	T_J = +25°C		–	2.2	–	A

Notes:

19. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty is used.

20. These parameters, although guaranteed, are not 100% tested in production.

Typical Performance Characteristics

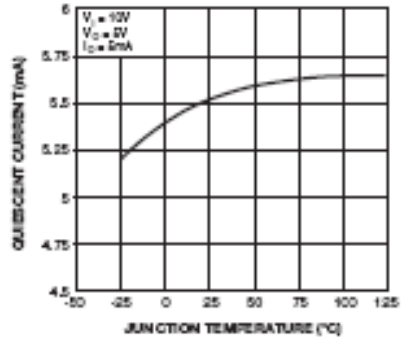


Figure 3. Quiescent Current

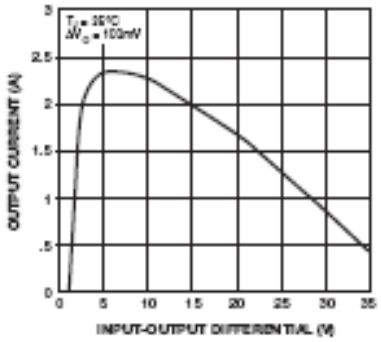


Figure 4. Peak Output Current

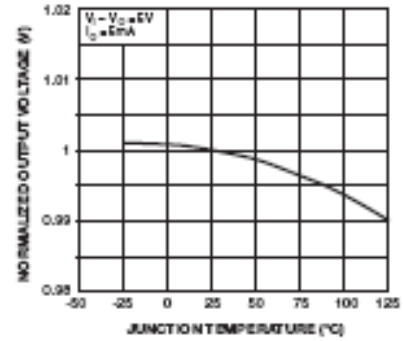


Figure 5. Output Voltage

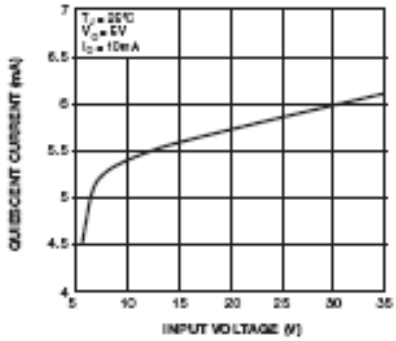


Figure 6. Quiescent Current

Typical Applications

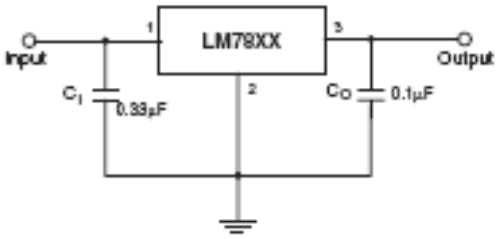


Figure 7. DC Parameters

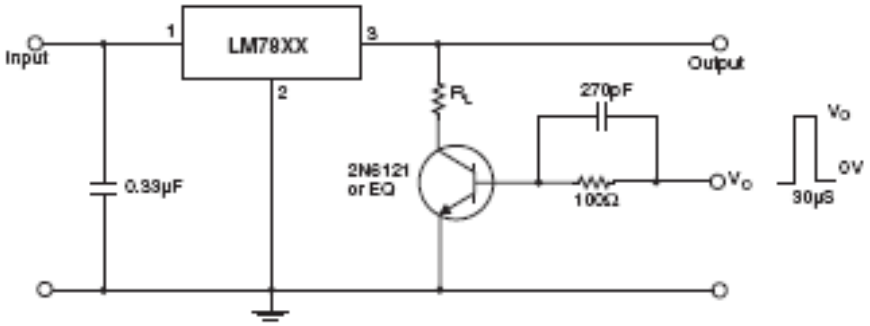


Figure 8. Load Regulation

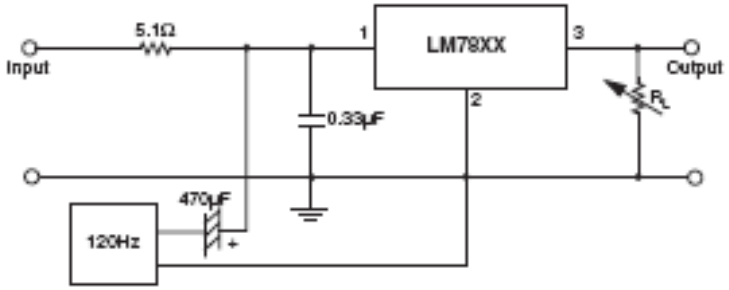


Figure 9. Ripple Rejection

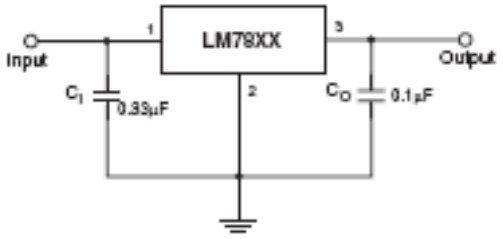
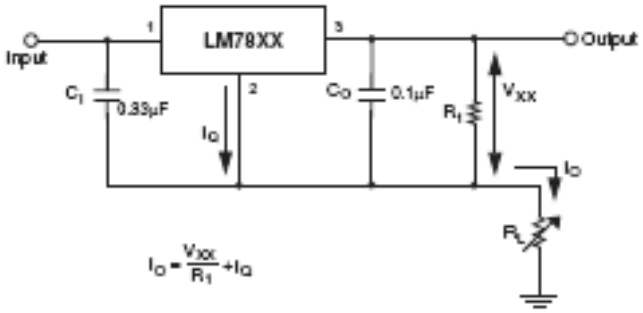


Figure 10. Fixed Output Regulator



Notes:
1. To specify an output voltage, substitute voltage value for "XX." A common ground is required between the input and the output voltage. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.
2. C_I is required if regulator is located an appreciable distance from power supply filter.
3. C_O improves stability and transient response.

Figure 11.

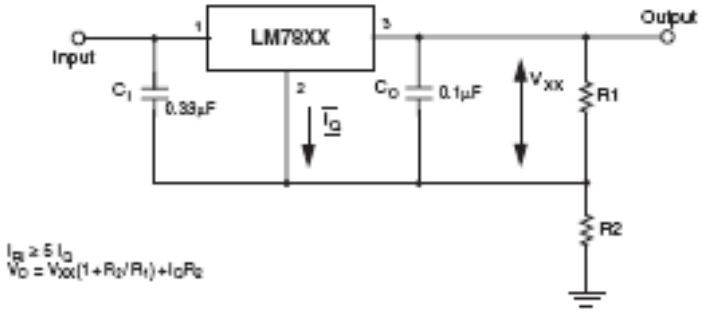
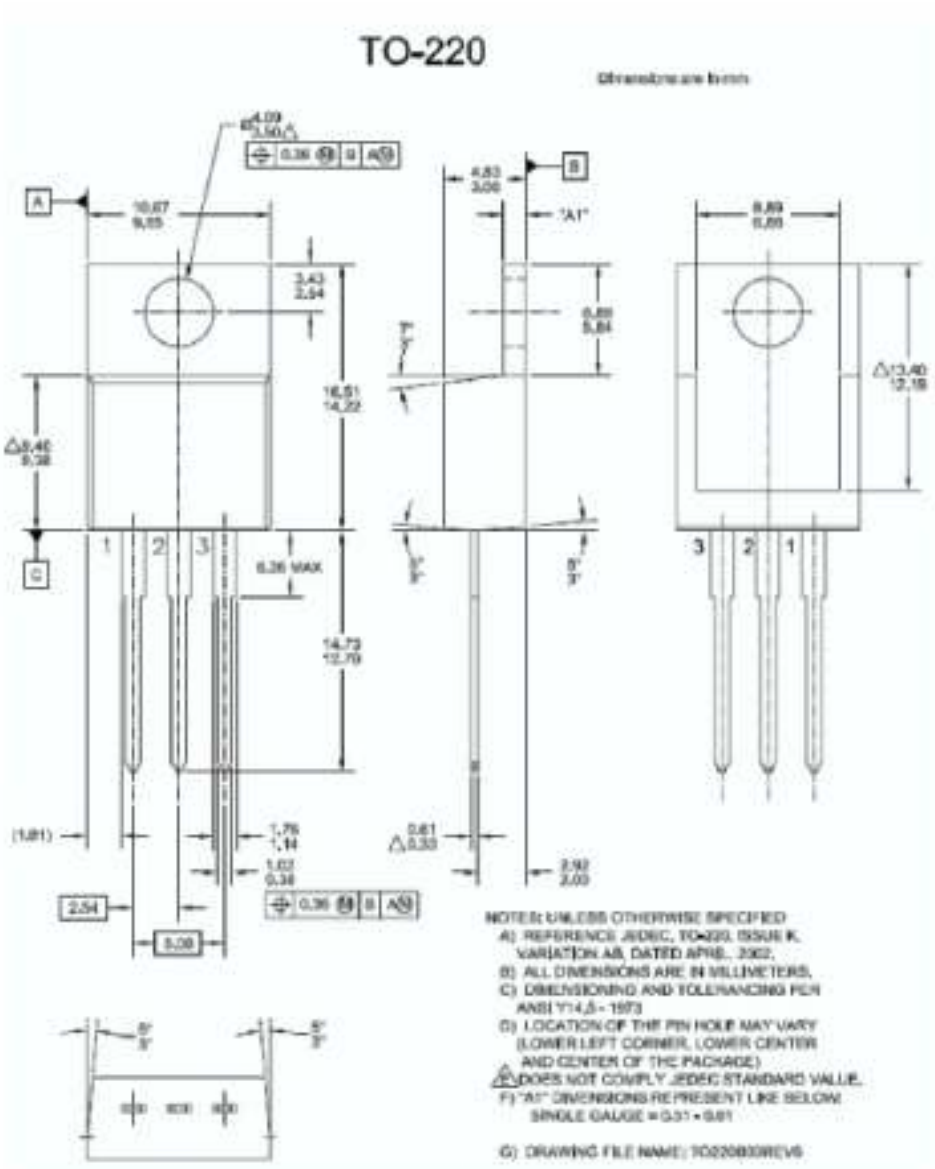


Figure 12. Circuit for Increasing Output Voltage

Mechanical Dimensions

Dimensions in millimeters



APPENDIX E

JHD162A Series Datasheet

JHD162A SERIES

• ..... DISPLAY CONTENT = 16 CHAR. x 2ROW

CHAR. DOTS= 5 x 8

DRIVING MODE= 1/16D

AVAILABLE TYPES= =

TN= STN(YELLOW GREEN= GREY= B/W)

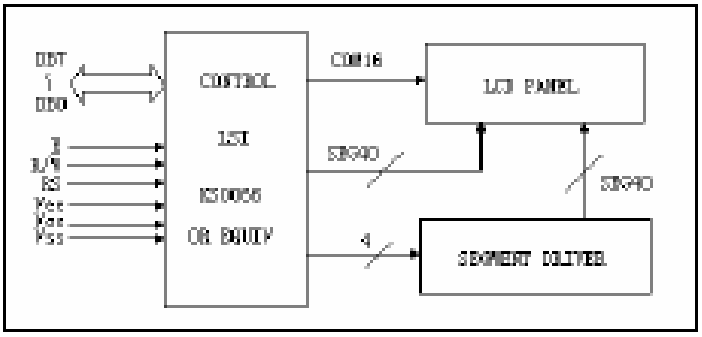
REFLECTIVE= WITH EL OR LED BACKLIGHT

EL/100VAC= 400HZ

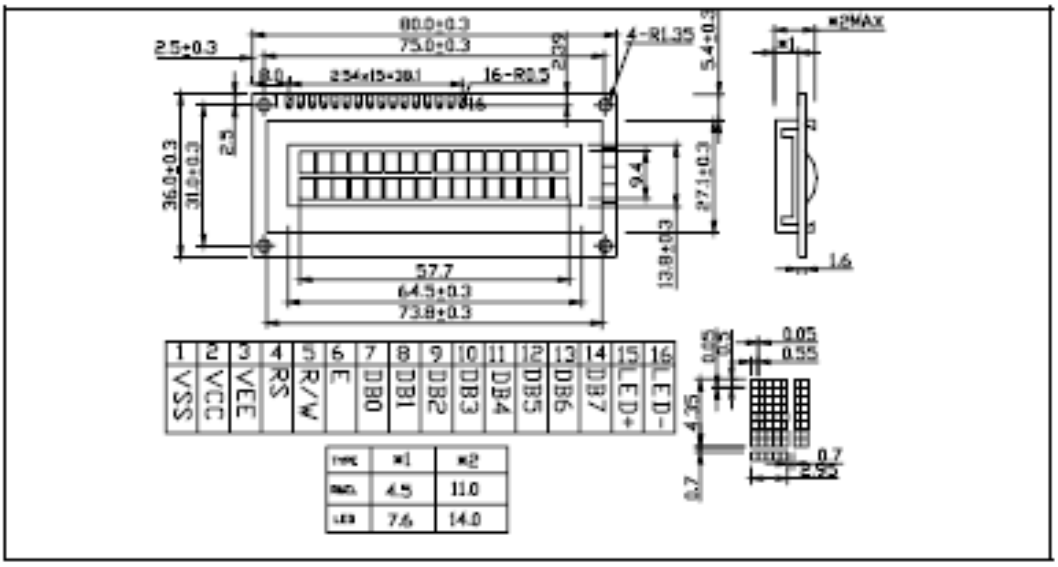
LED/4.2VDC

• .....

Parameter	Symbol	Testing Criteria	Standard Values			Unit
			Min.	Typ.	Max	
Supply voltage	V_{DD}-V_{SS}	-	4.5	5.0	5.5	V
Input high voltage	V_{IH}	-	2.2	-	V_{DD}	V
Input low voltage	V_{IL}	-	-0.3	-	0.6	V
Output high voltage	V_{OH}	-Io=0.2mA	2.4	-	-	V
Output low voltage	V_{OL}	Io=1.2mA	-	-	0.4	V
Operating voltage	I_{DD}	V_{DD}=5.0V	-	1.5	3.0	mA



• .....



	4.5	11.0
	7.6	14.0

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
VSS	VCC	VEE	RS	R/W	E	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	LED+	LED-

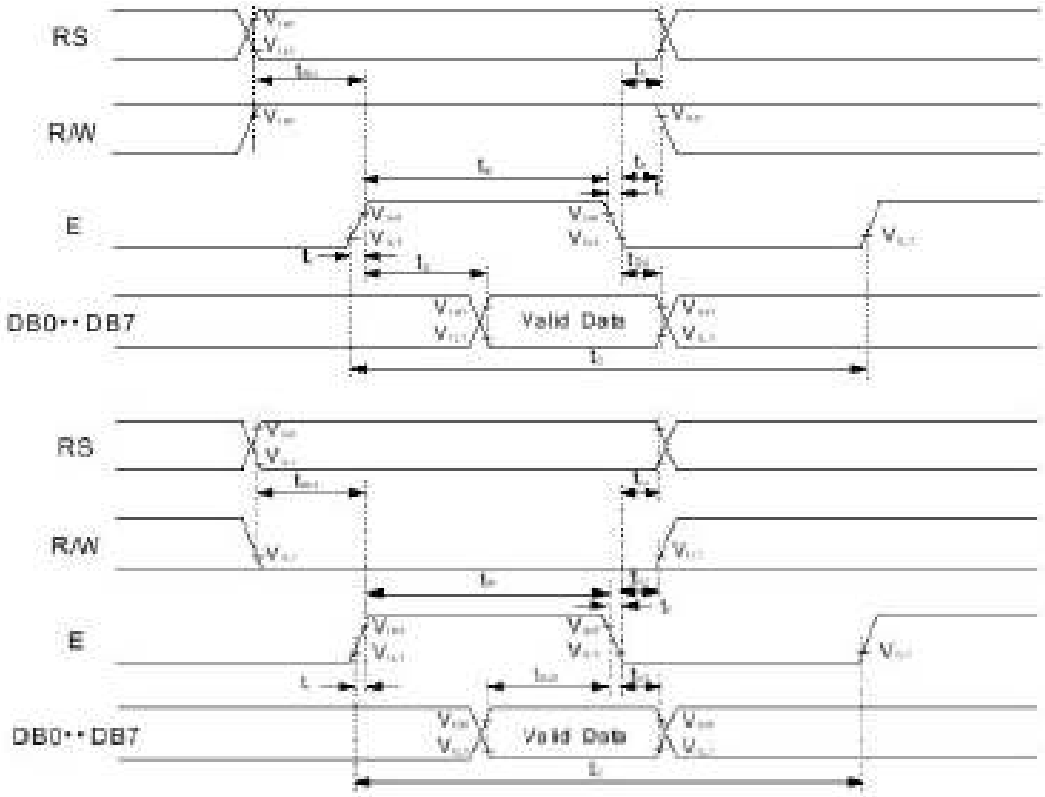
AC Characteristics Read Mode Timing Diagram

Table 12. AC Characteristics (V_{DD} = 4.5V ~ 5.5V, Ta = -30 ~ +85°C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode (Refer to Fig-6)	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu1	40	-	-	
	R/W and RS Hold Time	t_{H1}	10	-	-	
	Data Setup Time	tsu2	80	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode (Refer to Fig-7)	E Cycle Time	tc	500	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	20	
	E Pulse Width (High, Low)	tw	230	-	-	
	R/W and RS Setup Time	tsu	40	-	-	
	R/W and RS Hold Time	t_H	10	-	-	
	Data Output Delay Time	t_D	-	-	120	
	Data Hold Time	t_{DH}	5	-	-	

Table 13. AC Characteristics (V_{DD} =2.7V ~ 4.5V, Ta = -30 ~ +85°C)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode (Refer to Fig-6)	E Cycle Time	tc	1000	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu1	60	-	-	
	R/W and RS Hold Time	t_{H1}	20	-	-	
	Data Setup Time	tsu2	195	-	-	
	Data Hold Time	t_{H2}	10	-	-	
Read Mode (Refer to Fig-7)	E Cycle Time	tc	1000	-	-	ns
	E Rise / Fall Time	t_R,t_F	-	-	25	
	E Pulse Width (High, Low)	tw	450	-	-	
	R/W and RS Setup Time	tsu	60	-	-	
	R/W and RS Hold Time	t_H	20	-	-	
	Data Output Delay Time	t_D	-	-	360	
	Data Hold Time	t_{DH}	5	-	-	

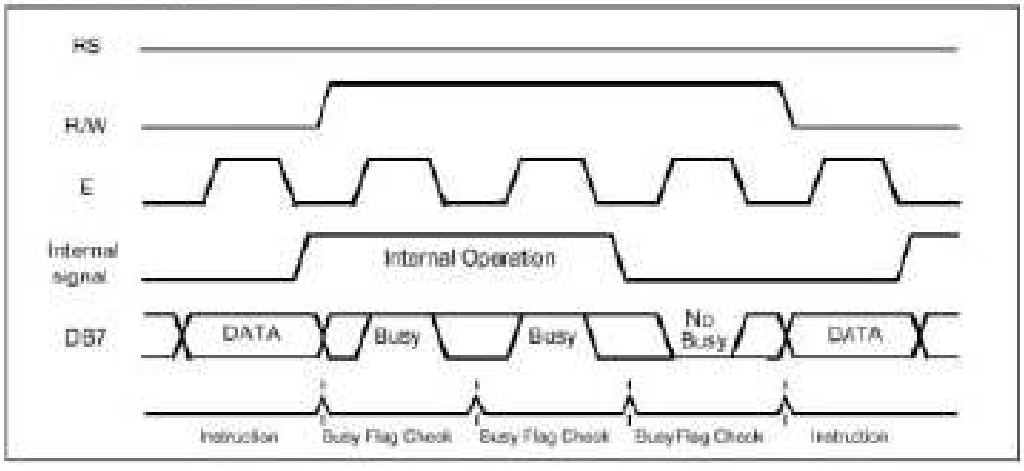


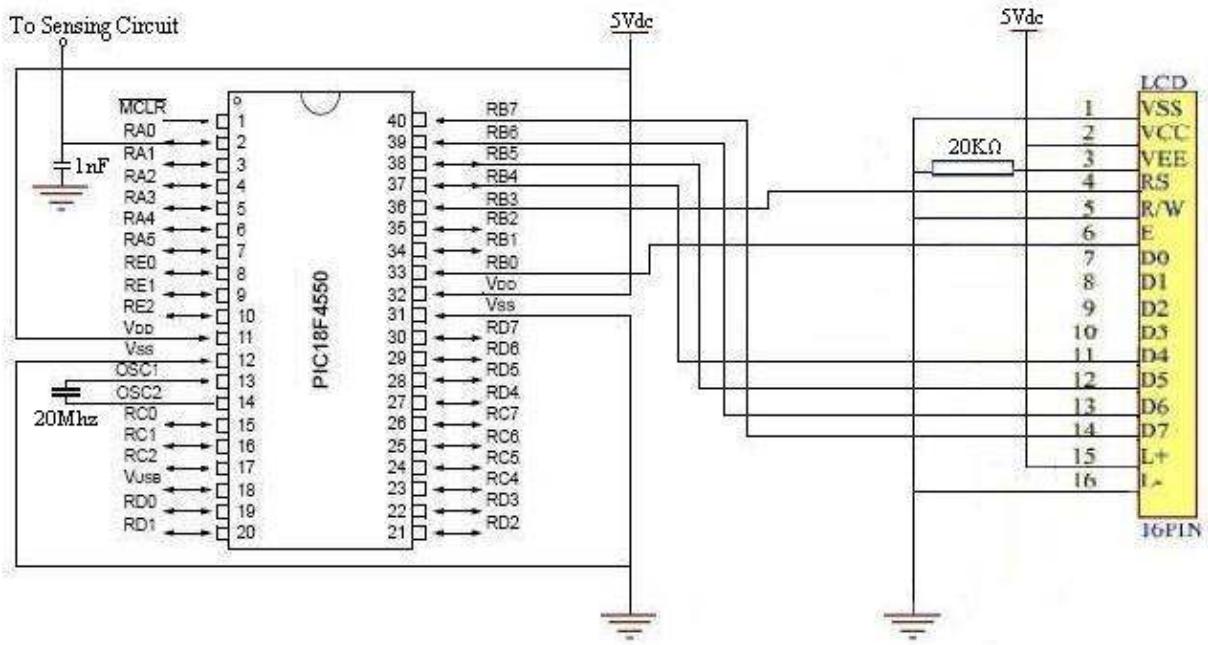
Write Mode Timing Diagram

Timing

1) Interface with 8-bit MPU

When interfacing data length are 8-bit, transfer is performed at a time through 8 ports, from DB0 to DB7. Example of timing sequence is shown below.




To Sensing Circuit
1nF
20Mhz
MCLR
RA0
RA1
RA2
RA3
RA4
RA5
RE0
RE1
RE2
VDD
VSS
OSC1
OSC2
RC0
RC1
RC2
VUSB
RD0
RD1
PIC18F4550
RB7
RB6
RB5
RB4
RB3
RB2
RB1
RB0
VDD
VSS
RD7
RD6
RD5
RD4
RC7
RC6
RC5
RC4
RD3
RD2
5Vdc
5Vdc
20KΩ
LCD
VSS
VCC
VEE
RS
R/W
E
D0
D1
D2
D3
D4
D5
D6
D7
L+
L-
16PIN

APPENDIX F

Omron G3NA-240B Solid State Relay

OMRON

Solid-state Relay

G3NA

A Wide Range of Models with 5- to 40-A Output Currents and Up to 480-VAC/200-VDC Output Voltages

- All models feature the same compact dimensions to provide a uniform mounting pitch.
- Built-in varistor effectively absorb external surges.
- Operation indicator (red LED) enables monitoring operation.
- Protective cover for greater safety.
- Standard models approved by UL/CSA and -UTU models by VDE (TÜV).

CE

Ordering Information

Isolation	Zero cross function	Indicator	Rated output load (Applicable output load)	Rated input voltage	Model
Phototriac	Yes	Yes	5 A at 24 to 240 VAC* (19 to 264 VAC)	5 to 24 VDC	G3NA-205B
Photocoupler				100 to 120 VAC	
				200 to 240 VAC	
Phototriac			10 A at 24 to 240 VAC* (19 to 264 VAC)	5 to 24 VDC	G3NA-210B
Photocoupler				100 to 120 VAC	
				200 to 240 VAC	
			10 A at 200 to 480 VAC* (180 to 528 VAC)	5 to 24 VDC	G3NA-410B
				100 to 240 VAC	
	—		10 A at 5 to 200 VDC* (4 to 220 VDC)	5 to 24 VDC	G3NA-D210B
				100 to 240 VAC	
Phototriac	Yes		20 A at 24 to 240 VAC* (19 to 264 VAC)	5 to 24 VDC	G3NA-220B
Photocoupler				100 to 120 VAC	
				200 to 240 VAC	
			20 A at 200 to 480 VAC* (180 to 528 VAC)	5 to 24 VDC	G3NA-420B
				100 to 240 VAC	
Phototriac			40 A at 24 to 240 VAC* (19 to 264 VAC)	5 to 24 VDC	G3NA-240B
Photocoupler				100 to 120 VAC	
				200 to 240 VAC	
			40 A at 200 to 480 VAC* (180 to 528 VAC)	5 to 24 VDC	G3NA-440B
				100 to 240 VAC	
			50 A at 200 to 480 VAC* (180 to 528 VAC)	5 to 24 VDC	G3NA-450B

*Loss time increases under 75 VAC. (Refer to page 148.)

Note: When ordering a TÜV-approved model, add "-UTU" to the model number as shown below.
Example: G3NA-210B-UTU

■ Accessories (Order Separately)

Heat Sink

The following heat sinks are thin and can be DIN-track mounted (except Y92B-P250).
See *Dimensions* for details.

Model	Applicable SSR
Y92B-N50	G3NA-205B, G3NA-210B, G3NA-D210B, G3NA-410B, G3NE-205T(L), G3NE-210T(L)
Y92B-N100	G3NA-220B, G3NA-420B, G3NE-220T(L)
Y92B-N150	G3NA-240B, G3NA-440B
Y92B-P250	G3NA-450B

Low-cost Models

Model	Applicable SSR
Y92B-A100	G3NA-205B, G3NA-210B, G3NA-D210B, G3NA-220B, G3NA-410B, G3NA-420B
Y92B-A150N	G3NA-240B, G3NA-440B
Y92B-A250	G3NA-440B

Mounting Bracket

Used to mount the G3NA with a mounting dimension of 56 mm.

Model	Applicable SSR
R99-11	G3NA-240B, G3NA-440B

See *Dimensions* for details. (Refer to page 148.)

Specifications

■ Ratings

Input (Ambient Temperature: 25°C)

Model	Rated voltage	Operating voltage	Impedance	Voltage level	
				Must operate voltage	Must release voltage
G3NA-2□□B	5 to 24 VDC	4 to 32 VDC	7 mA max.*	4 VDC max.	1 VDC min.
	100 to 120 VAC	75 to 132 VAC	36 kΩ±20%	75 VAC max.**	20 VAC min.**
	200 to 240 VAC	150 to 264 VAC	72 kΩ±20%	150 VAC max.**	40 VAC min.**
G3NA-4□□B	5 to 24 VDC	4 to 32 VDC	5 mA max.*	4 VDC max.	1 VDC min.
G3NA-D210B	100 to 240 VAC	75 to 264 VAC	72 kΩ±20%	75 VAC max.	20 VAC min.

Note: The input impedance is measured at the maximum value of the rated supply voltage (for example, with the model rated at 100 to 120 VAC, the input impedance is measured at 120 VAC).
*With constant current input circuit system. The impedance for the G3NA-□□□B-UTU is 15 mA max.
**Refer to the *Engineering Data* for further details.

Output

Model	Applicable load				
	Rated load voltage	Load voltage range	Load current		Inrush current
			With heat sink*	Without heat sink	
G3NA-205B	24 to 240 VAC	19 to 264 VAC	0.1 to 5 A	0.1 to 3 A	60 A (60 Hz, 1 cycle)
G3NA-210B			0.1 to 10 A	0.1 to 4 A	150 A (60 Hz, 1 cycle)
G3NA-410B	200 to 480 VAC	180 to 528 VAC	0.2 to 10 A	0.2 to 4 A	
G3NA-220B	24 to 240 VAC	19 to 264 VAC	0.1 to 20 A	0.1 to 4 A	220 A (60 Hz, 1 cycle)
G3NA-420B	200 to 480 VAC	180 to 528 VAC	0.2 to 20 A	0.2 to 4 A	
G3NA-240B	24 to 240 VAC	19 to 264 VAC	0.1 to 40 A	0.1 to 6 A	440 A (60 Hz, 1 cycle)
G3NA-440B	200 to 480 VAC	180 to 528 VAC	0.2 to 40 A	0.2 to 6 A	
G3NA-450B	200 to 480 VAC	180 to 528 VAC	0.2 to 50 A	0.2 to 6 A	
G3NA-D210B	5 to 200 VDC	4 to 220 VDC	0.1 to 10 A	0.1 to 4 A	20 A (10 ms)

*When OMRON's heat sink (refer to the accessories) or a heat sink of specified size is used.

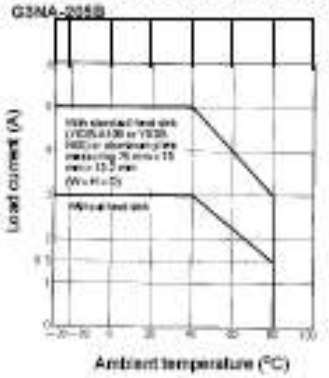
■ Characteristics

Item	G3NA-205B, -210B, -220B	G3NA-240B	G3NA-410B, -420B, -440B, -450B	G3NA-D210B
Operate time	1/2 of load power source cycle + 1 ms max. (DC input) 3/2 of load power source cycle + 1 ms max. (AC input)			1 ms max. (DC input) 30 ms max. (AC input)
Release time	1/2 of load power source cycle + 1 ms max. (DC input) 3/2 of load power source cycle + 1 ms max. (AC input)			5 ms max. (DC input) 30 ms max. (AC input)
Output ON voltage drop	1.6 V (RMS) max.		1.6 V (RMS) max.	1.5 V max.
Leakage current	5 mA max. (at 100 VAC) 10 mA max. (at 200 VAC)		10 mA max. (at 200 VAC) 20 mA max. (at 400 VAC)	5 mA max. (at 200 VDC)
Insulation resistance	100 MΩ min. (at 500 VDC)			
Dielectric strength	2,500 VAC, 50/60 Hz for 1 min			
Vibration resistance	Malfunction: 10 to 55 Hz, 1.5-mm double amplitude			
Shock resistance	Malfunction: 1,000 m/s^2			
Ambient temperature	Operating: −30°C to 80°C (with no icing or condensation) Storage: −30°C to 100°C (with no icing or condensation)			
Approved standards	UL508 File No.E84562/CSA C22.2 (No.0, No.14) File No.LR35535 TÜV R9151660 (EN60950)			
Ambient humidity	Operating: 45% to 85%			
Weight	Approx. 80 g	Approx. 70 g	Approx. 80 g	Approx. 70 g

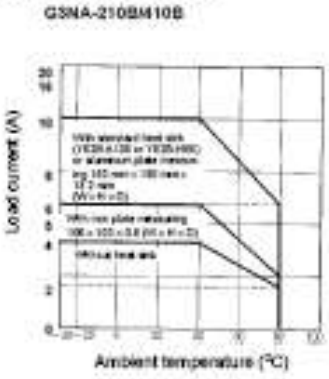
Engineering Data

Load Current vs. Ambient Temperature Characteristics

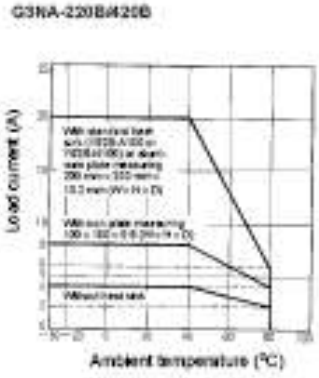
G3NA-205B



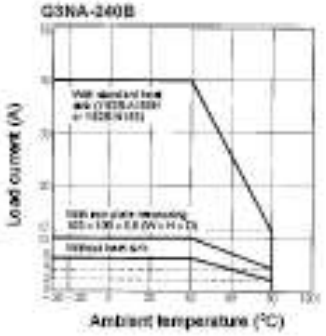
G3NA-210B/H10B



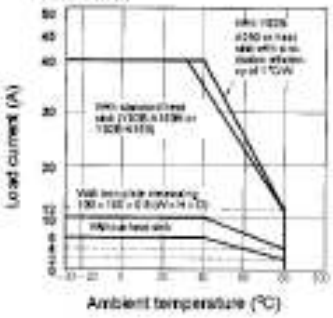
G3NA-220B/H20B



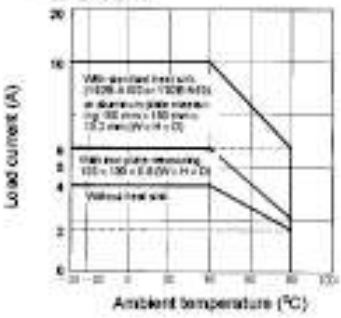
G3NA-240B



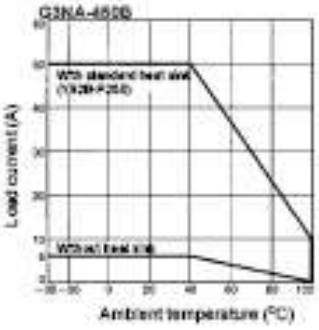
G3NA-440B



G3NA-D210B



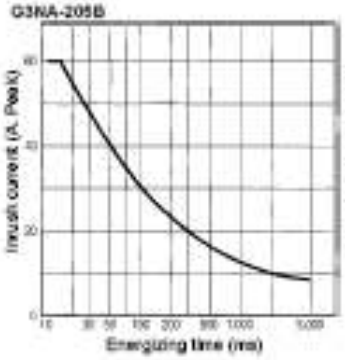
G3NA-450B



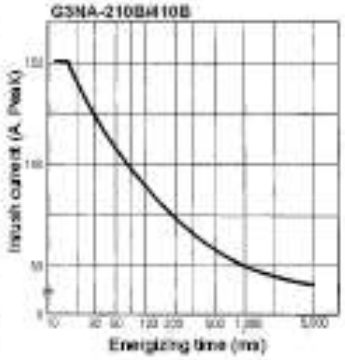
Inrush Current Resistivity

Non-repetitive (Keep the inrush current to half the rated value if it occurs repetitively.)

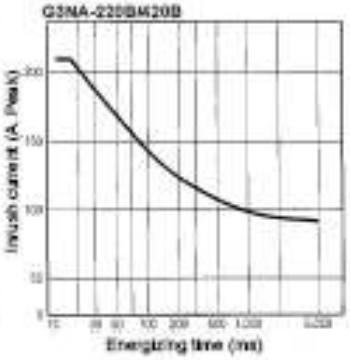
G3NA-205B



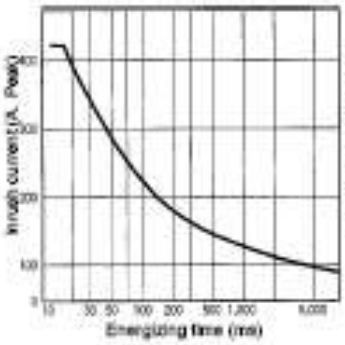
G3NA-210B/410B



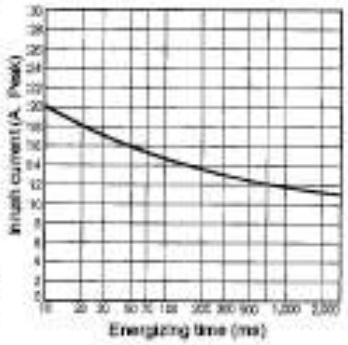
G3NA-220B/420B



G3NA-240B/440B/450B

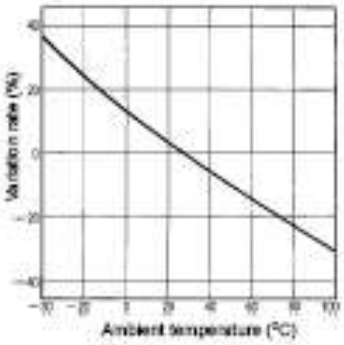


G3NA-D210B



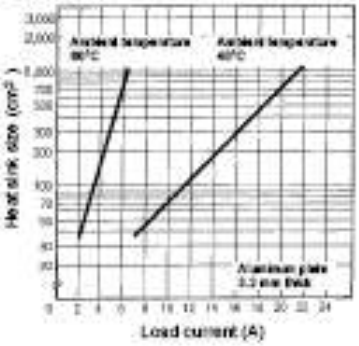
Temperature Characteristics (with Must Operate Voltage and Must Release Voltage)

G3NA-2□□B AC input



Heat Sink Size vs. Load Current

G3NA-220B



Note: The heat sink size refers to the combined area of the sides of the heat sink that radiate heat. For example, when a current of 15 A is allowed to flow through the SSR at 40°C, the graph shows that the heat sink size is about 450 cm². Therefore, if the heat sink is square, one side of the heat sink must be 15 cm ($15^2 \times 2 = 450$) or longer.

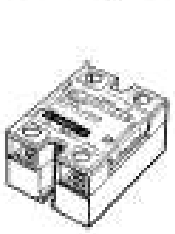
Dimensions

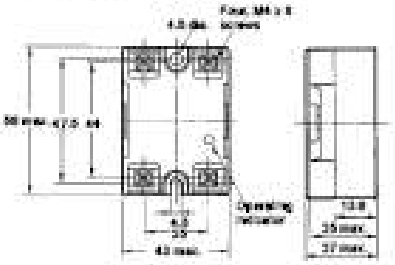
Note: All units are in millimeters unless otherwise indicated.

In the case of surface mounting, a 30% derating of the load current is required.

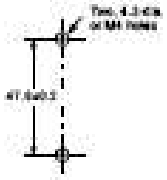
The orientation indicated by the external dimensions is not the correct mounting orientation. When opening mounting holes, refer to the mounting hole dimensions.

G3NA-205B, G3NA-210B, G3NA-220B, G3NA-410B, G3NA-420B

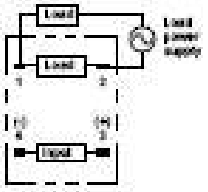




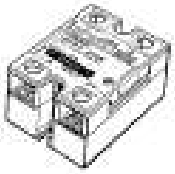
Mounting Holes

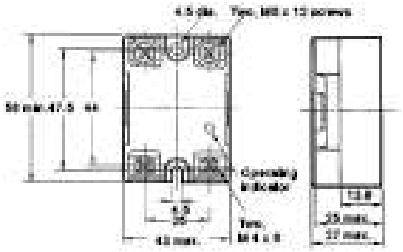


Terminal Arrangement/ Internal Connections (Top View)

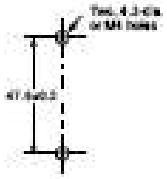


G3NA-240B, G3NA-440B, G3NA-450B

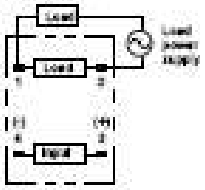




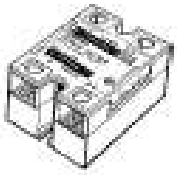
Mounting Holes

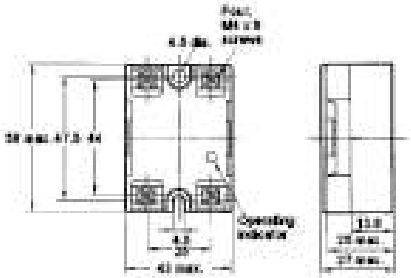


Terminal Arrangement/ Internal Connections (Top View)

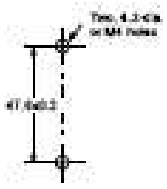


G3NA-D210B

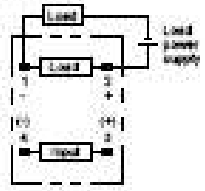




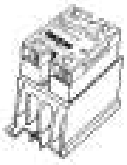
Mounting Holes

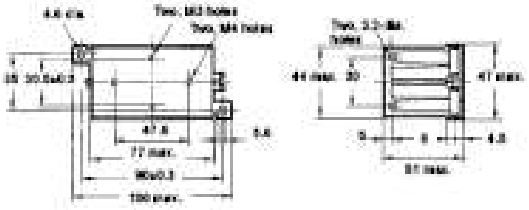


Terminal Arrangement/ Internal Connections (Top View)

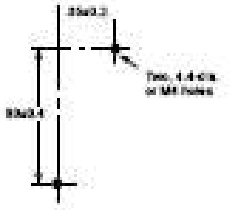


Heat Sink
Y92B-N50



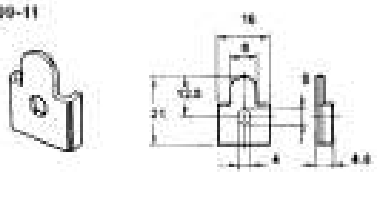


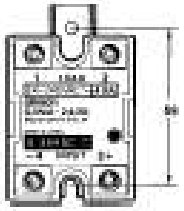
Mounting Holes



Weight: approx. 200 g

R89-11





Use Mounting Bracket R89-11 so that the G3NA-240B can be mounted with the same pitch as that of the G3N-240B.

Precautions

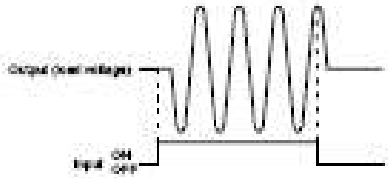
Refer to pages 11 to 19 for general precautions.

Load Connection

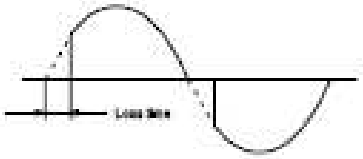
For an AC load, use a power supply rated at 50 or 60 Hz.
The maximum operating frequency is 10 Hz.
The G3NA has a built-in varistor for overvoltage protection.

Zero Cross Function

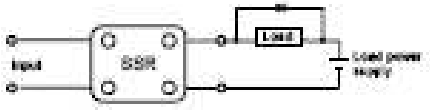
An SSR with a zero cross function operates when an AC load voltage reaches the zero point or its vicinity. This reduces clicking noises when the load is input, and minimizes the influence of an inductive load, such as a lamp, heater, or motor, on the power supply because the inrush current of the load is reduced. This can also minimize the scale of the inrush current protection circuit.



At a low applied voltage, such as 24 VAC, the load current is not fully supplied. When the Unit is switched ON, the voltage required to power the Unit deprives the output signal of the necessary voltage level and thus creates loss time. The lower the load voltage is, the greater the loss time is. This condition, however, will not create any serious problems.



For a DC or L load, a diode should be connected in parallel the load to absorb the counter electromotive force of the load.



When attaching a heat sink to the G3NA, apply Silicone Grease or equivalent heat conductive grease on the heat sink. (Toshiba Silicon, Shinetsu Silicon, etc.)

Tighten the mounting screws of the heat sink with a torque of 0.78 to 0.88 N • m.

EN55011 Measurement of Mains Terminal Disturbance Voltage

The G3NA-UTU conforms to EN55011 standards when a capacitor is connected to the load power supply as shown in the following circuit diagram.

Recommended Capacitor
Nissei Denki's MKT-series R40 (1 µF)

The output terminal side of the G3NA-D210B is connected to a built-in diode for protecting the SSR from damage that may result from reverse connection. The SSR, however, cannot withstand one minute or more if the wires are connected in reverse order. Therefore, pay the utmost attention not to make polarity mistakes on the load side.

ALL DIMENSIONS SHOWN ARE IN MILLIMETERS.
To convert millimeters into inches, multiply by 0.03937. To convert grams into ounces, multiply by 0.03527.

APPENDIX G

AR-ELCB Hardware Picture

Figure A1: Auto Re-closer ELCB with casing

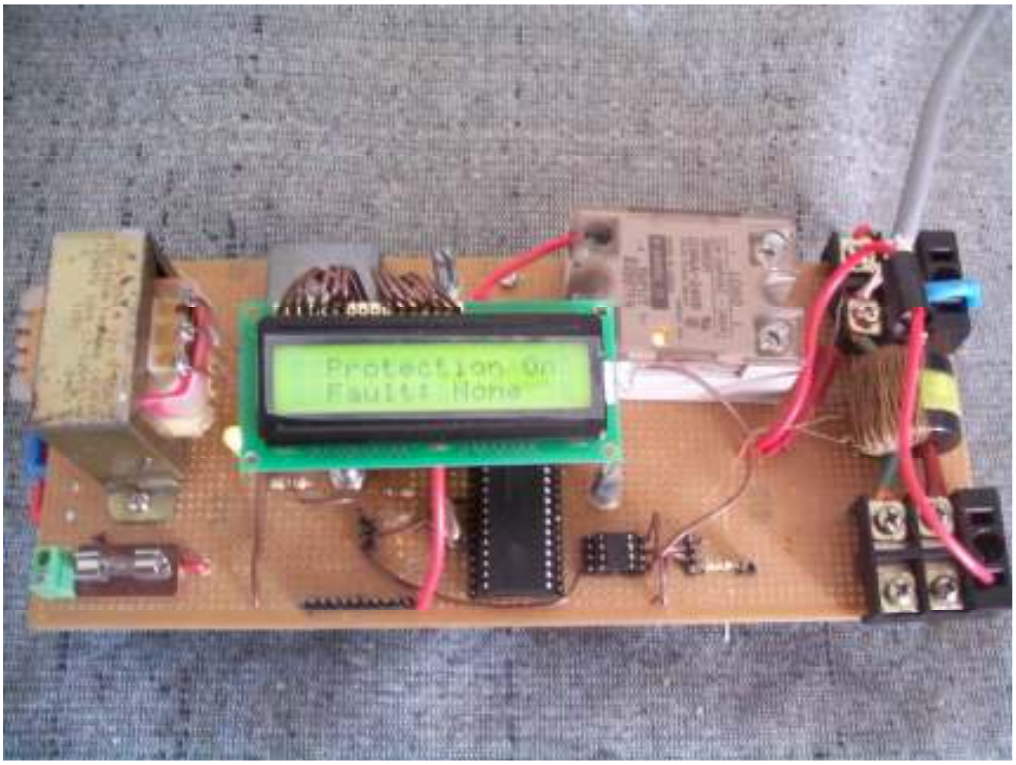


Figure A2: Auto Re-closer ELCB without casing

APPENDIX H

Biodata of the Author

AUTHOR'S BIODATA

Mohd Tarmizi bin Rahim was born on 10th September 1985 in Muadzam Shah, Pahang. His permanent address is at 226, Felda Keratong 9, 26700 Muadzam Shah, Pahang. He is an youngest brother from six siblings, he has one brother and four sister. His first education is Sekolah Rendah Perantau Damai. After 5 year searching for knowledge there, he enter his secondary education at Sekolah Mengah Perantau Damai. Soon after three year there, he got an opportunity to advance his study to technical school which are Sekolah Menengah Teknik Dungun. He completed his studies there in Electrical Engineering course at 2003. Then he has been accepted to study in Science physics course at Pahang Matriculation College from 9 May 2004 until 14 April 2005. He is currently (2009) a Bachelor's student in the Electrical Engineering (Power System), faculty of Electrical and Electronics Engineering, University Malaysia Pahang. His research fields are power electronics and power system. He is a student member of the IEM of Malaysia.