Selective Harmonic Elimination using MFO for a Reduced Switch Multi-level Inverter topology

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2022 IEEE Symposium on Industrial Electronics & Applications (ISIEA) | 978-1-6654-8012-3/22/$31.00 ©2022 IEEE | DOI: 10.1109/ISIEA54517.2022.9873761

***Abstract*—This research article proposed a new modified single-phase multi-level inverter topology with an optimal switching control strategy to reduce the inverter output harmonic distortion. The topology is configured to operate in asymmetric mode to generate eleven levels of output voltage steps. Additionally, a selective harmonic elimination technique has been deployed to minimize the switching loss and EMI. The Moth Flame Optimization (MFO) algorithm is deployed to compute the optimal switching angles. The proposed MLI topology is simulated in PSIM software using the optimized switching angles. The inverter performance parameters such as the total harmonic distortion (THD), harmonic amplitudes, switching, and conduction losses, were also analyzed and reported. The topology total harmonic distortion is 2.4%, hence satisfying the IEEE 519 standard.**

Keywords—Moth Flame Optimization, Total Harmonic Distortion, Selective Harmonic Elimination, Multi-level Converter Topology, Hardware-In-Loop testing

I. INTRODUCTION

Over the last decades, numerous researchers have developed robust multi-level inverter topologies deployed in both industrial and domestic sectors [1]. The most available conventional topologies are the Flying capacitors (FC), Neutral Point Clamp (NPC), Cascaded H-Bridge (CHB), T-type topology, and Modular Multi-level Converter (MMC). MLI's properties, characteristics, and drawbacks make them suitable for specific applications. A significant shortcoming of the MLI is the increase in device count as the number of output steps increases. To address this drawback, several MLI topologies and their control were developed [2]-[4].

Most researchers working in multi-level inverter topology are interested in enhancing the inverter power handling capability, increasing the output steps, and reducing the output harmonic contents [5]-[10]. However, additional power electronic switches and other peripheral devices are needed to increase the converter output power and number of steps [11]. This results in increased circuit complexity, size, and cost. Additionally, most of the switching techniques employed are done at high frequency [12]. However, low output harmonics are achieved at the expense of efficiency accrued due to high switching loss and, consequently, high Electromagnetic Interference (EMI) capable of destroying low signal-sensitive circuits [13],[14]. Little attention has been given to the possibility of increasing the converter output steps without necessarily increasing the number of components.

In this paper, an improved design of the cascaded topology is proposed, capable of generating higher output levels with reduced power switches and dc sources. The topology can be operated in symmetric or asymmetric modes depending on the required number of output voltage levels needed

II. METHODOLOGY

A. *Description and Analysis of the Proposed MLI Topology*

Figure 1 shows the circuit of the proposed multi-level inverter topology. It comprises of two input DC voltage sources (V_{Dc1}, V_{Dc2}) and ten fully controlled power electronic switches, out of which two are unidirectional (S_1, S_2) and eight bi-directional (S_{11} – S_{14} and S_{21} - S_{24}). These switches are assembled into two modules, namely, the level generator module (N_{fm}) having six (6) switches (S_1, S_2, and S_{11} – S_{14}) and the power transfer module (N_{sm}) having four (4) switches (S_{21} - S_{24}). To avoid short-circuiting within the inverter, the following switch pairs (S_1, S_2), (S_{11}, S_{12}), (S_{13}, S_{14}), (S_{21}, S_{22}), and (S_{23}, S_{24}) are operated in complementary. The output of both modules (N_{fm}, N_{sm}) is connected to the primary winding of two 1:1 turn ratio transformers. The advantages of the transformer are that it prevents short-circuiting at the DC link, provides isolation, and its reactance components function as an additional filter. The inverter output voltage is the summation of the transformer's secondary side voltages, achieved through the series connection of the secondary windings. In addition, a small-sized LC filter is designed for the output to filter out the remaining higher-order harmonics.

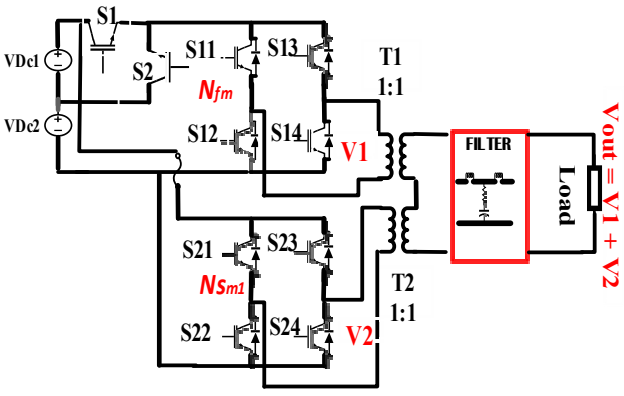

Fig. 1. Proposed multi-level inverter topology

B. *Asymmetrical Operation*

The circuit topology is configured and operated in an asymmetrical mode to increase the number of output steps of the proposed MLI. In this mode of operation, the magnitudes