MICROCONTROLLER BASED THREE-LEVEL ZERO VOLTAGE SWITCHING PULSE – WIDTH – MODULATION DC-TO-DC CONVERTER

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I declare that this thesis entitled 'Three-Level Zero Voltage Switching PWM DC-to-DC Converter controlled by Microcontroller' is the result of my own research except as cited in references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature :…….

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Date : November 17th, 2008

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DEDICATION

Special dedicated to my family, my friends, my fellow colleague,
and to all faculty members

For all your care, support, and believe in me.

ABSTRACT

The purpose of this project is to develop a Three-Level Zero Voltage Switching PWM DC-to-DC Converter controlled by Microcontroller. The scopes of works for this project include to convert DC to DC voltage, implement Zero Voltage Switching (ZVS) to increase the efficiency and lastly to apply the Microcontroller for switching. A zero-voltage-switching pulse-width-modulation three-level (ZVS PWM TL) converter realizes ZVS for the switches with the use of the leakage inductance (or external resonant inductance) and the output capacitors of the switches, however, the rectifier diodes suffer from reverse recovery which results in oscillation and voltage spike. In order to solve this problem, this paper proposes a novel ZVS PWM TL converter, which introduces two clamping diodes to the basic TL converter to eliminate the oscillation and clamp the rectified voltage to the reflected input voltage; microcontroller will generates PWM in order to operate MOSFETs so that the converter can be turn on. Meanwhile, all the switches keep realizing ZVS.

ABSTRAK

Tujuan projek ini adalah untuk menyiapkan “Tiga Sifar Paras Pensuisan Voltan Pemodulatan Lebar Denyut Penukar Dc Kepada Dc” yang dikawal oleh “Microcontroller”. Skop-skop kerja untuk projek ini termasuklah menurunkan nilai voltan arus terus, seterusnya mangaplikasikan pengsuisan sifar voltan untuk meningkatkan kecekapan penukar DC kepada DC voltan. Akhir sekali, “Microcontroller” digunakan untuk menghidupkan system. Tiga Sifar Paras Pensuisan Voltan Pemodulatan Lebar Denyut Penukar Dc Kepada Dc Voltan mempraktikkan sifar pengsuisan voltan kepada semua suis dengan penggunaan kebocoran aruhan dan ketidak tetapan voltan. Bagi menyelesaikan masalah ini, kertas kerja ini memperkenalkan pengapitan diod untuk digunakan supaya ayunan dapat dihapuskan. Diod ini juga akan mengapit voltan keluaran pada voltan masukan. “Microcontroller” akan menghasilkan pemodulatan lebar denyut untk menghidupkan MOSFETs supaya sistem dapat berfungsi. Sementara itu, semua suis pemperatikkan pengsuisan sifar voltan

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CHAPTER 1

INTRODUCTION

1.0 SWITCH MODE POWER SUPPLY

1.1 Introduction

In recent years, dc-to-dc converter circuits employ pulse-width-modulated signal are widely researched in high power conversion applications (Xuechao Liu and Bo Zhang, 2002). In all the pulse-width-modulated dc-to-dc, the controllable switches are operated in a switch mode where they are required to turn on and turn off the entire load current during each switching. In this switch-mode operation, the switches are subjected to high switching stress and high switching power loss that increase linearly with the switching frequency of PWM. Another significant drawback of the switch-mode operation is the EMI produced due to large di/dt and dv/dt caused by a switch-mode operation.

These shortcomings of switch-mode converters are exacerbated if the switching frequency is increased in order to reduce the converter size and weight and hence to increase the power density. Therefore, to realize high switching frequency in converter, the aforementioned shortcomings are minimized if each switch in a converter changes its status (from on to off of vice versa) when the voltage across it and/or the current through it is zero at the switching instant. The converter topologies and the switching strategies, which results in zero-voltage and/or zero-current switching can be implementing.

1.2 Background and alternative design

In order to overcome this problem while increase the efficiency and reduce the switching stress, weight and volume, several soft-switching Three-Level converters were proposed in recent years (Ruan et al., 2004). This Three-Level converter can be classified into two types, zero voltage switching (ZVS) pulse-width modulation (PWM) Three-Level converter and zero-voltage and zero-current-switching (ZVZVC) PWM TL converter.

Nevertheless, zero voltage switching (ZVS) pulse-width modulation (PWM) TL converter is more appropriate control strategy for high frequency resonant mode converters than ZCS control because of switching losses in semiconductor devices are zero, EMI is reduce during transition and at high input voltage system, the efficiency is high. However, there are some problems that faced by ZVS which is the off-state voltage across the switch is high and generally, they are regulated with variable frequency controller. In order to overcome this problem Full Bridge Microcontroller

Based Three-Level Zero Voltage Switching PWM with clamping diodes (TL-ZVS-PWM-CD) dc-to-dc was proposed.

1.3 Purpose and Significant of project

The objective of this project is to;

Design a Three-Level Zero Voltage Switching PWM DC-to-DC Converter controlled by Microcontroller.

1.4 Scopes of project

Scopes that need to be proposed for this project are:

i. To convert DC to DC power.
ii. Implement the zero voltage switching (ZVS) in this converter to increase the efficiency.
iii. Implement the microcontroller as a switching for this converter.

1.5 Thesis Outline

The thesis is divided into 5 chapters, the first of which (chapter 1) is an introduction which presents the nature and significance of the problem studied that comprise aspects of what needs to be implemented.

Chapter 2 discusses the building blocks of a switch mode power dc supply and presents an overview of dc-to-dc converters with electrical isolation and the method of control that is to be implemented upon completion of the thesis.

Chapter 3 through to half of chapter 4 is the beginning of a series of chapters that goes into the detail design procedures and operation of the various building blocks required to produce a working model.

Chapter 4 will discuss the outcome of which will be used to establish component parameters for the converter. The switch's timing characteristics needed for the establishment of the PWM command circuit will also be derived in chapter 3.the last part of chapter 4 will be the results of project and the discussion about the results.

Chapter 5 is the final and concluding chapter. The advantages and the disadvantages will be highlighted to the extent of what was achieved and the significance of the work that has been accomplished. Future proposed refinements will be suggested in order to further improve upon the system design and its features.

CHAPTER 2

LITERATURE REVIEW

2.0 INTEGRATE SYSTEM DESIGN

2.1 Introduction

In order to design Microcontroller Based Three-Level Zero Voltage Switching PWM DC-to-DC Converter, there are several parts that must be considerate. This system will be elaborate in detail in this chapter. Each part is important in order to complete this dc-to-dc converter.

This chapter aims is to expose the operating blocks of the switch-mode dc-to-dc converter, the requirement to establish the PWM scheme through appropriate circuit and driver circuit to drive the converter switches.

2.2 Switch-Mode DC Supplies

There are a number of general requirements that need to be met in the design of the proposed dc-to-dc converter. Such requirements include a regulated output voltage to operate the PWM and driver circuit to complete the ZVS dc to dc converter.

2.3 Block Diagram System Representation

Figure 2.1 shows a block-diagram of a switch-mode dc power supply. The various functions each block (unit) performs are as indicated on the schematic and where applicable the state of voltage throughout the system.

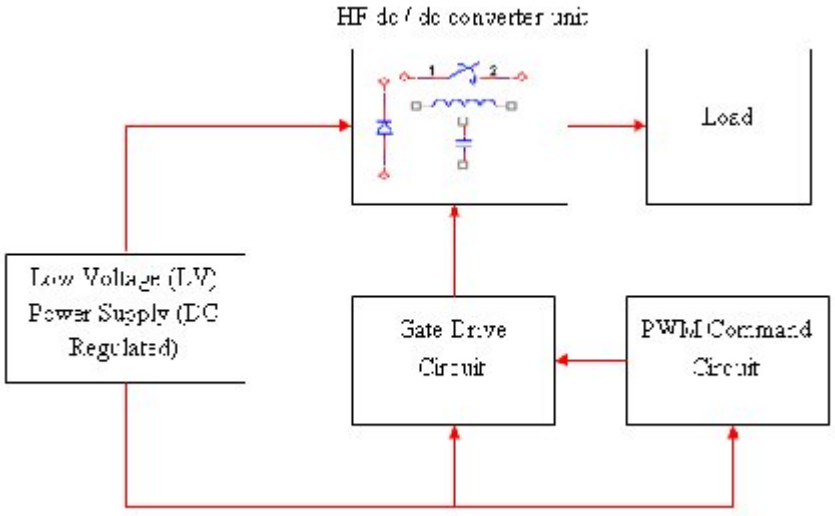

Figure 2.1: Simplified block diagram of a switch-mode dc power supply.

It can be seen that the diagram of Figure 2.1 is comprised of the following sub-system blocks:

i. HF dc / dc converter unit
ii. PWM command circuit
iii. Gate drive circuit
iv. Low-Voltage supply unit

As stated previously, it is the sub-system blocks that are the subject of analysis, design and implementation in the remainder of the chapters comprising this project report.

2.3.1 High Voltage DC to DC Converter Unit

The converter converts dc voltage from one voltage level to another. The voltage conversion is achieved by the high frequency switching that result in a high frequency ac square wave voltage as output voltage that is applied to the load.

Chapter 3 will provide more detail about this high frequency dc to dc converter unit (ZVS dc to dc converter) including the topology and operation of converter.

2.3.2 PWM Command and Gate Drive Circuit

The output voltage is depending on means of the PWM scheme to be implemented through the PWM command and drive circuits. There is only one command circuit central to the generation of the required switching characteristics and four associated gate drive circuitry, one for each MOSFET of the dc-to-dc converter circuit. Also, all gate-drives incorporate a high frequency signal transformer for electrical isolation.

2.3.2.1 PWM Based PIC Microcontroller

A pulse width modulation (PWM) waveform can be generated by the software of a microcomputer as per the requirements of converter-based circuit. Such a software program may also incorporate optimization features as us elimination of unwanted harmonics that required increasing the efficiency of the dc to dc converter (Moorthi, 2005).

By using PIC microcontroller, PWM waveform can be shape flexibility and it will simplify the hardware and reduces the overall cost (Moorthi, 2005). The PWM waveform base PIC microcontroller unit is shown in Figure 2.2.

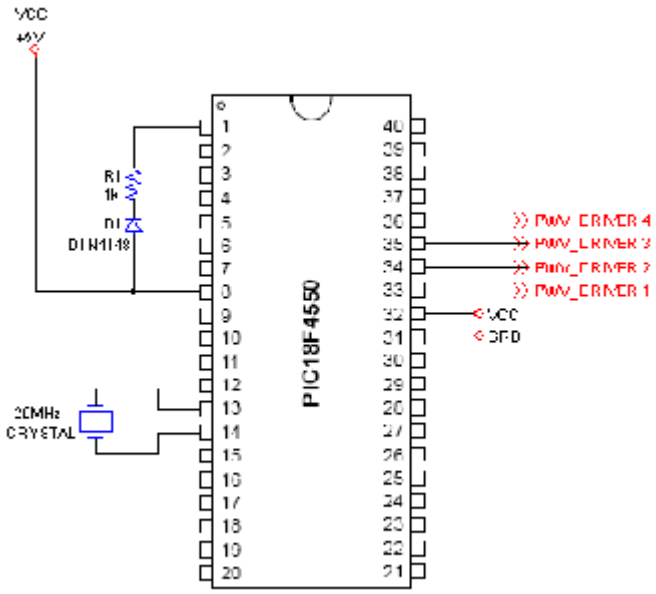

Figure 2.2: PWM Based PIC Microcontroller circuit

This circuit only contains four components in which a PIC microcontroller (PIC18F4550) 40 pins was used to provide direct duty ratio by programming the microcontroller. The PIC microcontroller is also capable of operating at switching frequencies well above 100 kHz, which is the operating frequency of the dc to dc converter.

2.3.2.2 Gate Drive Circuit

The output command signals generated by the PWM circuit are of small magnitude and are not capable of driving the converter switches. Thus a drive circuit is used to perform the required gating.

Figure 2.3: Circuit diagram of one drive circuit.

Figure 2.3 shows the circuit diagram for the drive circuit. This circuit contains sixth components. An IR2109 IC 8 pins was used as MOSFETs driver. A total of four identical gate-drive circuits are needed. Essentially these would be integrated on one complete circuit board. Each of the drive circuits is responsible for gating the four individual MOSFET.

2.3.3 Low-Voltage Supply Unit

There also exist low-voltage power supply units that serve to be input to the circuits that require low power levels. These circuits as shown on the schematic needing the low level voltage requirements comprise of the PWM command circuit and its associated gate drive circuits.

There are several low-voltage supplies that require operating the system which is:

i. $15V_{dc}$
ii. $12V_{dc}$
iii. $5V_{dc}$

15Vdc regulated output is necessary in operating drive circuit. Meanwhile 12Vdc regulated output is required as an input for HF dc to dc converter. Lastly, 5Vdc is required by PIC microcontroller circuit to generate PWM waveform that required by high frequency dc to dc converter. To fulfill this requirement, DC Power Supply Generator was used.

CHAPTER 3

METHODOLOGY

3.0 MICROCONTROLLER BASED THREE-LEVEL ZERO VOLTAGE SWITCHING PWM DC-TO-DC CONVERTER

3.1 Introduction

The purpose of this analysis is to derive analytical expressions for various design parameters for a 'Three-Level Zero-Voltage-Switching Pulse-Width-Modulated (TL-ZVS-PWM) DC-to-DC Converter' and to provide the necessary background for the design of such converters.

'PSPISE Evaluation Version 9.1' programming is used here to finding the analysis of this circuit. The result from analysis will been comparing to the theoretically predicted. This outcome will be guide to the actual analysis through hardware analysis.

The DC – to – DC converter introduced in this project will be applied zero voltage switching technique, operated in constant frequency, regulated by pulse width modulation signal that produced by PIC Microcontroller and low rms current stress upon power switches in which regulated output rated at 12V and 5A.

3.2 Circuit Description

A review of the TL- ZVS-PWM converter shown in Figure 3.1 has two stages which is input stage and output stage.

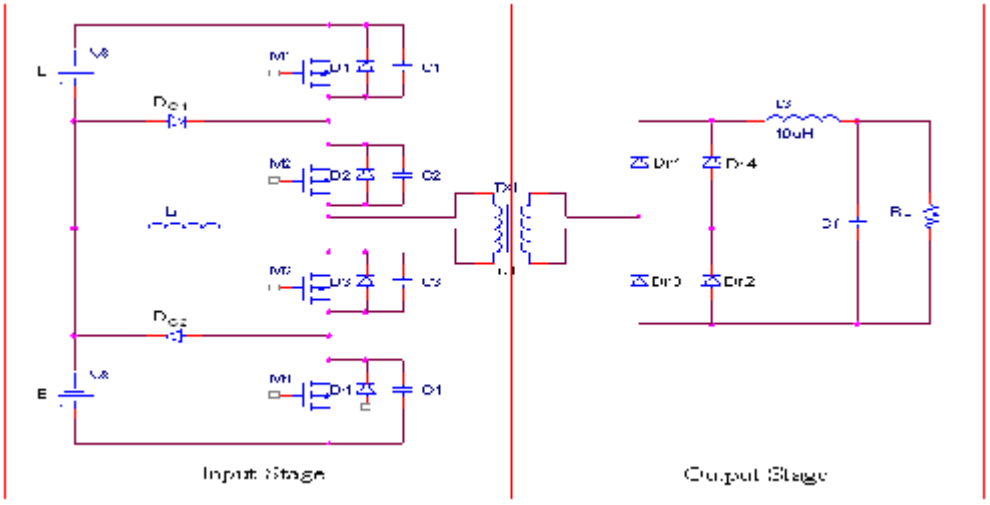

Figure 3.1: TL-ZVS-PWM DC-to-DC converter

3.2.1 Input Stage

The main commutation leg is formed by the four N-channel depletion-layer power metal oxide semiconductor field effect transistors (MOSFET switches) represented in the circuit diagram as M_1, M_2, M_3 and M_4. The drain, gate and source of the switches are as indicated.

Diodes D_1-D_4 are not external components however, but are the MOSFET's body diodes, while capacitors C_1-C_4 represent the intrinsic capacitance of the switches, employed to perform the commutation at zero voltage as will be seen later.

The commutation inductor is represented as L_r. This inductance will be treated in the analysis as if it is composed of the leakage inductance of the isolation transformer T_x and an external inductor. Also, D_{C1} and D_{C2} represent the clamping diode.

3.2.2 Output Stage

The output stage is composed of a single-phase full-bridge diode rectifier configuration represented by D_{r1}-D_{r4} coupled to a second order L-C filter represented by L_f and C_f respectively. The load resistance represented as R_L is connected across the filter capacitor C_f (see Figure 3.1). The load will be treated as a pure resistive load in the analysis to follow.

3.2.3 Input / Output Parameter

Table 3.1 lists the various input and output parameters of the TL-ZVS-PWM dc-to-dc converter design presented in this chapter. As it can be seen, the converter is to operate at a switching frequency of 100 kHz supplying a 60 W load at a rated voltage of $12V_{dc}$ at an average rated output current of 5A. Also, there are two input dc supply voltages E associated with the converter each to the magnitude of $12V_{dc}$. Thus the total input dc voltage is $24V_{dc}$.

Table 3.1: Input and output parameters of the dc-to-dc converter.

Parameter	Magnitude
Rated Output Power, $P_{out, ave}$ (W)	60
Rated Output Voltage, $V_{out, ave}$ (V)	12
Rated Output Current, $I_{out, ave}$ (A)	5
Half Input Voltage, E (V)	12
Total Input Voltage, 2E (V)	24
Switching Frequency, f_s (kHz)	100

3.2.4 Circuit Representation

The circuit in Figure 3.1 is re-drawn in figure 3.2 with the load including the second order filter now represented by a constant current source I_o equal in magnitude to the load current.

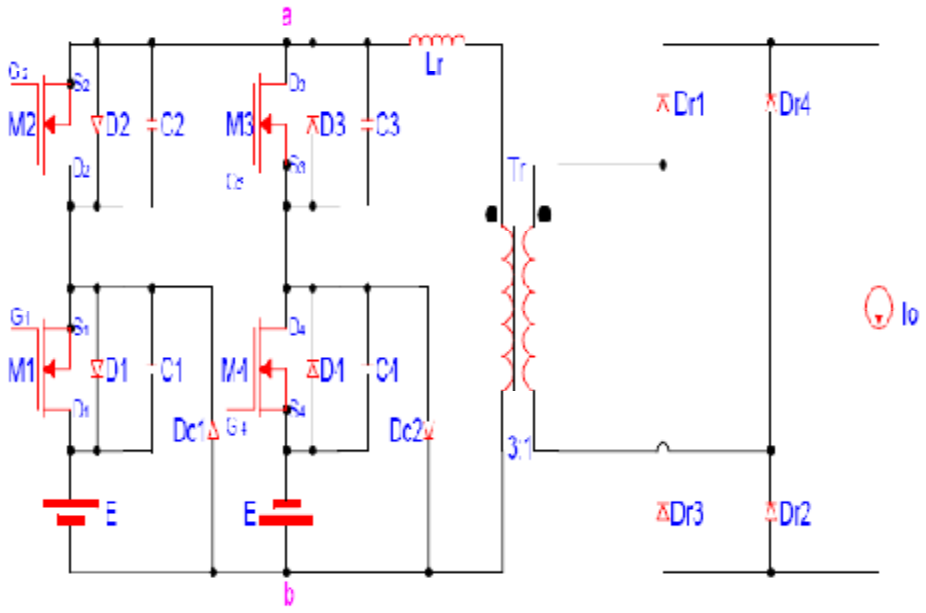

Figure 3.2: TL-ZVS-PWM dc-dc converter with load represented by a constant current source.

Although the circuit looks somewhat different, a closer examination reveals that the interconnection between components still holds. This circuit will be used hereon (i.e. in the topological stages) to demonstrate the current commutation throughout the converter. The main theoretical waveforms are depicted in Figure 3.3.

3.2.4.1 Theoretical Waveforms

The main theoretical waveforms depicted in figure 3.3, show the various voltage waveforms across certain nodes and elements of the circuits depicted in figure 3.2.

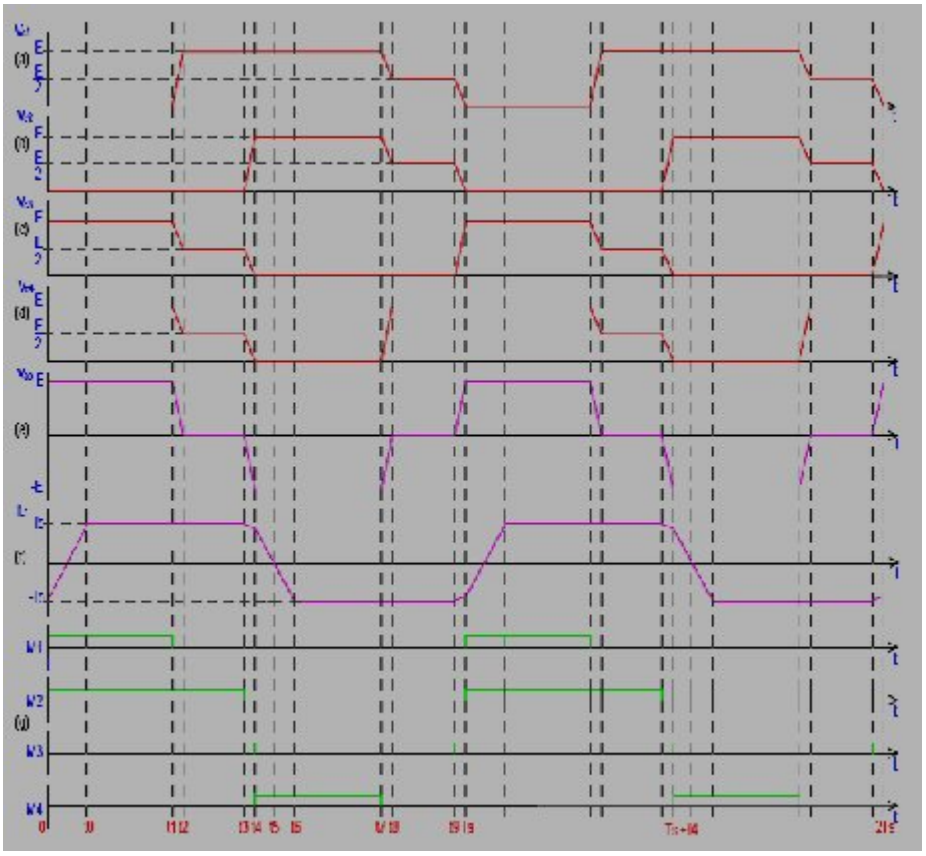

Figure 3.3: Main theoretical Waveforms.

Plot (a) to (d) are the voltage waveforms developing across the four independent capacitors C_1 to C_4 (i.e.-intrinsic capacitance of the MOSFETs) respectively.

Plot (e) and (f) represented the voltage waveform across node ‘a’ and node ‘b’ and the output current (i.e. load current) respectively. Finally, plot (g) show the

MOSFETs (i.e. switches) command signals (or switching signals) actuated by the PWM scheme to be implemented.

3.2.5 Topology Operation

It is stressed at this stage that constant reference to the main theoretical waveforms of Figure 3.3 should be made with the explanations given below in relation to the operation of the TL-ZVS-PWM dc-to-dc converter circuit.

The operation of the converter to follow will be examined stage by stage in accordance with the timing instants given that are shown on figure 3.3.

3.2.5.1 Stage Operation

The operation of the converter will be described stage by stage from time t = 0 to time t = Ts, in accordance with the timing instants shown on the waveforms in Figure 3.3 and the previous assumption made earlier. Along with a brief description of each stage, the circuit of Figure 3.2 is re-drawn for each time interval (ie stage operation) with the current highlighted to show the current commutation path throughout the circuit.

Stage 1-(t_0, t_1):

Current commutation during this interval is depicted in figure 3.4(a). During this period (t_0, t_1), $V_{C1}(t) = V_{C2}(t) = 0V$ while $V_{C3}(t) = V_{C4}(t) = E$. Here the load current I_o (where $i_{Lr}(t) = Io$) flows through M_1, M_2 and output rectifier diodes Dr_1 and Dr_2.

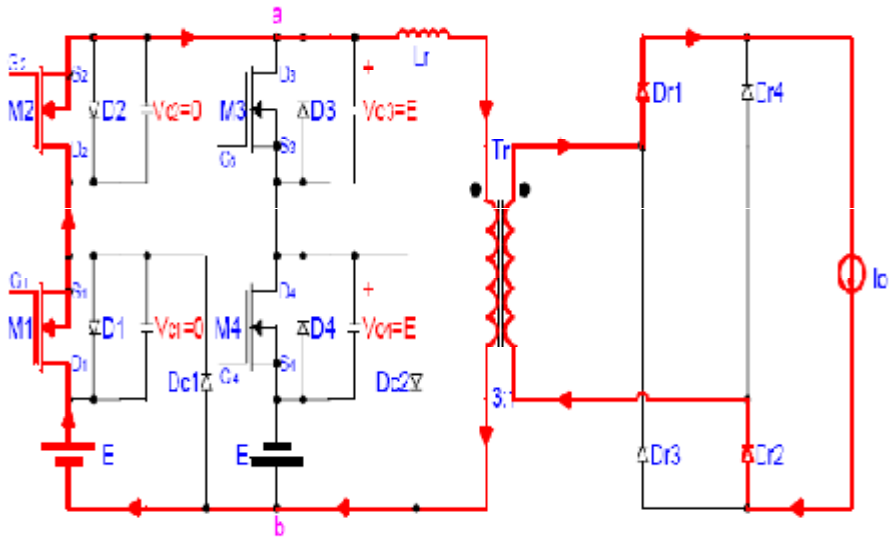

Figure 3.4(a): Stage 1 of the converter's operation.

Stage 2-(t_1, t_2):

Current commutation during this interval (t_1, t_2) is depicted in figure 4(b). At the beginning of this time period t_1, MOSFET M_1, is gated off and subsequently turns off in a soft switching manner.

The voltage across C_1 increases from 0V up to E (ie $V_{C1}(t) \rightarrow E$), while the voltage across C_3 and C_4 decrease from E to (1/2)E respectively (ie $(V_{C3}(t) + V_{C4}(t)) = 2E \rightarrow E$).

When D_{C1} becomes directly polarized at instant t_2 and begins to conduct the stage ends. During this time period (t_1, t_2) the load current Io (where $i_{LR}(t) = Io$) flows through output rectifier diodes Dr_1 and Dr_2.

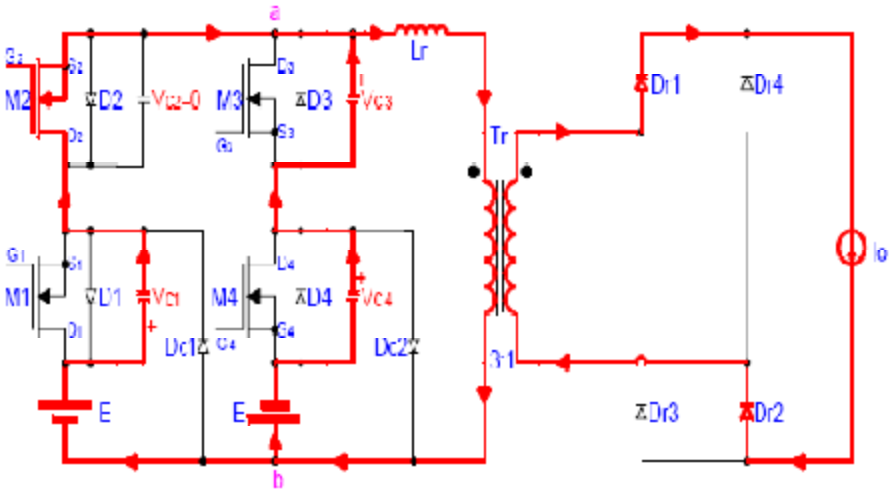

Figure 3.4(b): Stage 2 of the converter's operation.

Stage 3-(t_2, t_3):

Current commutation during this interval (t_2, t_3) is depicted in Figure 3.4(c). This is a freewheeling stage at which begins at instant t_2.

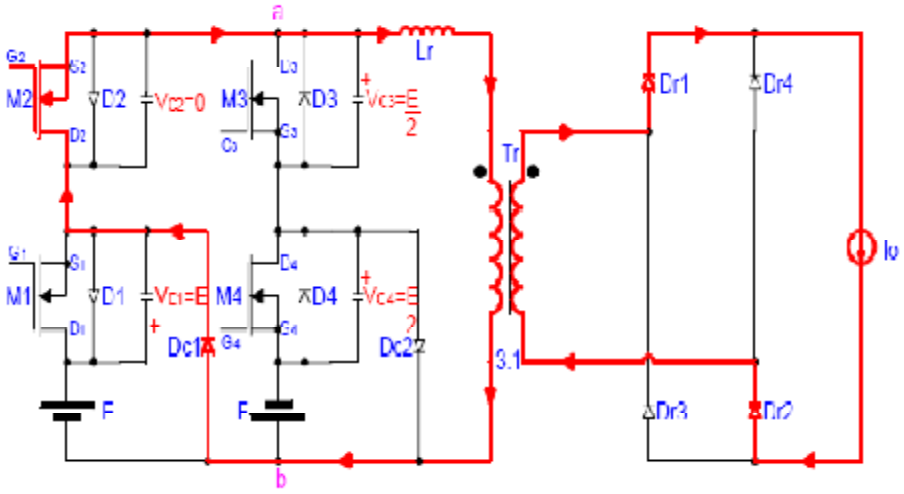

Figure 3.4(c): Stage 3 of the converter's operation.

The load current flows through the clamping diode D_{C1} as it was directly polarized at the end of the previous stage, M_2, the commutation inductor L_r and output rectifier diode D_{r1} and D_{r2}.

Stage 4-(t_3, t_4):

Current commutation during this interval (t_3, t_4) is depicted in Figure 4(d). At instant t_3, M_2 is gated off and subsequently turns off in a soft switching manner.

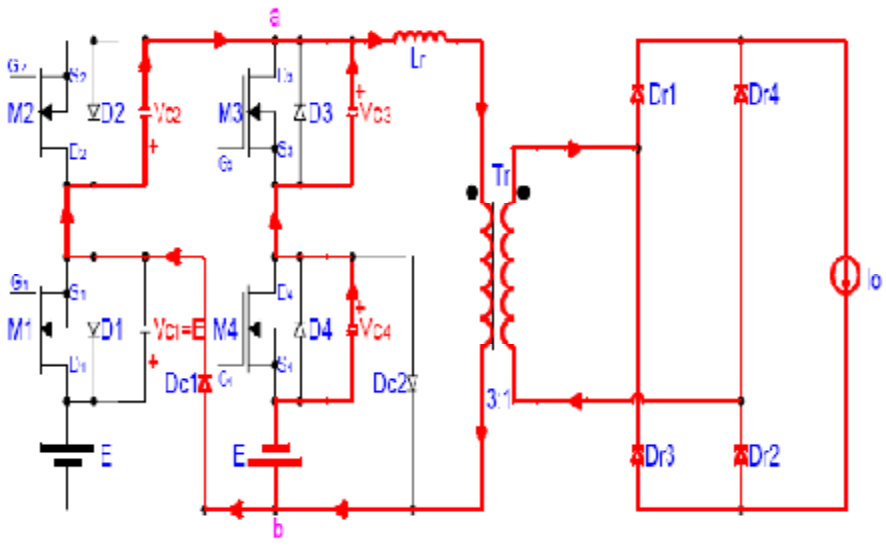

Figure 3.4(d): Stage 4 of the converter's operation.

The voltage across C_2 increases from zero to E (i.e. V_{C2} (t) → E), while the voltage across C_3 and C_4 decrease from (1/2) E to zero respectively (i.e. (V_{C3} (t) + V_{C4} (t)) = E → 0V). Also, all output diode rectifiers (D_{r1} – D_{r4}) are conducting thus short-circuiting the output stage.

Stage 5-(t_4, t_5):

Current commutation during this interval (t_4, t_5) is depicted in figure 4(e). In this time period the current i_{Lr}(t), flows through the MOSFET M_3 and M_4's intrinsic diode, D_3 and D_4 respectively and decreases linearly.

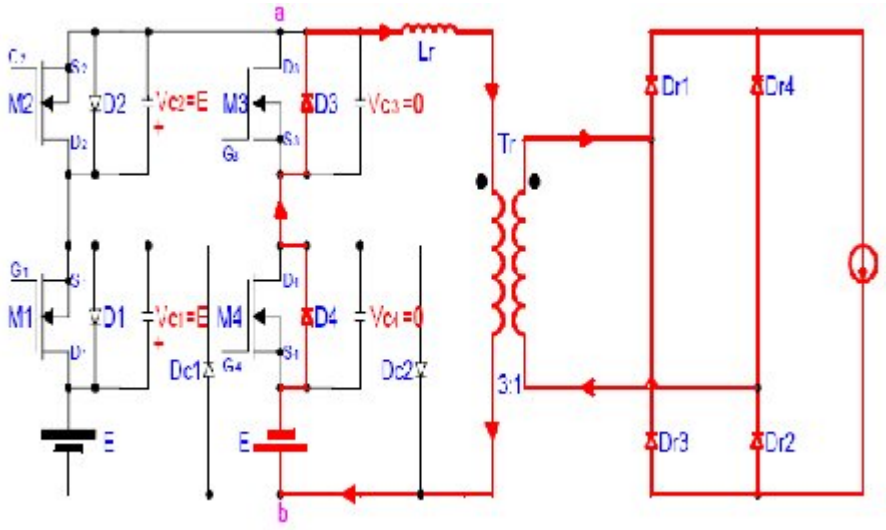

Figure 3.4(e): Stage 5 of the converter's operation.

While D_3 and D_4 are conducting both switches M_3 and M_4 are gated on at zero voltage and zero current.

Stage 6-(t_5, t_6):

Current commutation during this interval (t_5, t_6) is depicted in Figure 3.4(f). As $i_{Lr}(t)$ is decreasing linearly from the previous stage, D_3 and D_4 cease to conduct when $i_{Lr}(t)$ reaches zero at t_5.

Switches M_3 and M_4 (gated on at t_4) then begin to conduct and the current $i_{Lr}(t)$ increases linearly in the reverse direction as shown on the circuit diagram.

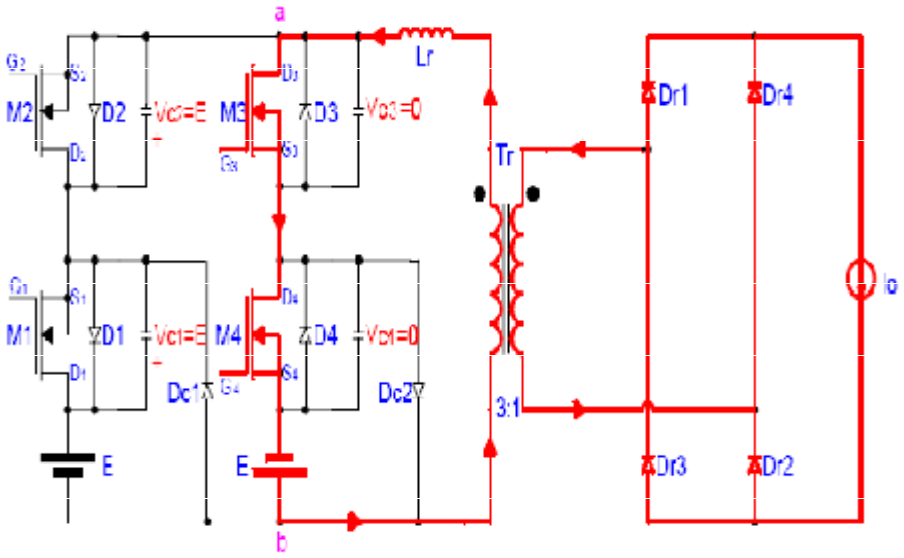

Figure 3.4(f): Stage 6 of the converter's operation.

Stage 7-(t_6, t_7):

Current commutation during this interval (t_6, t_7) is depicted in Figure 3.4(g). As the current is increasing in the reverse direction (as described in the previous time period), this stage starts at instant t6 when i_{Lr} (t) reaches load current I_o.

The output rectifier diodes Dr_1 and Dr_2 turn off naturally as the load current flows only through Dr_3 and Dr_4.

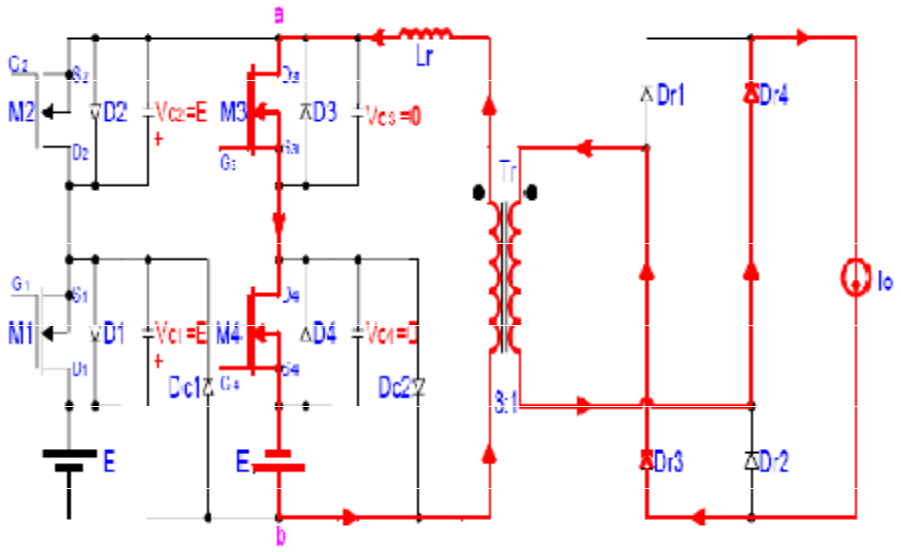

Figure 3.4(g): Stage 7 of the converter's operation.

3.3 Output Characteristic

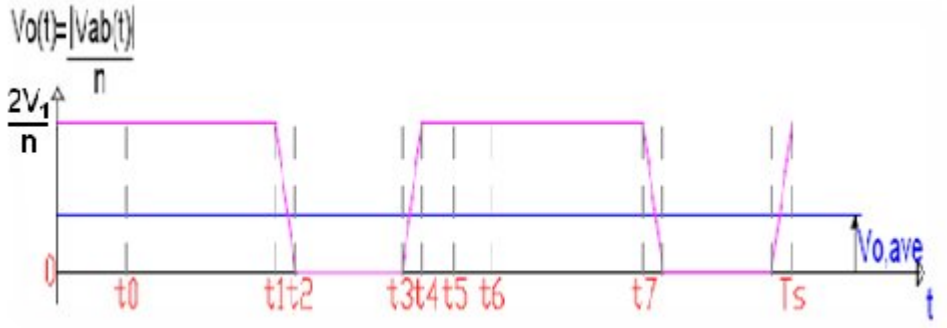

Figure 3.5: Output rectified voltage waveform of the TL-ZVS-PWM converter.

The average output voltage can be calculated from the following definition of average value.

$$V_{,} = \frac{1}{T} \quad V \quad (t)\, d(t) \qquad (1)$$

From Figure 3.5, it can be seen that the period T_o of the output rectified voltage waveform V_{out} (t) is half the period of the input voltage waveform V_{ab} (t) seen in figure 3.3(e). Also, the instantaneous output voltage can be seen to be equal to a third of the absolute value of the instantaneous input voltage due to the high frequency isolation transformer turns ratio n.

$$n = \frac{N}{N} = 0.5$$

$$V \quad (t) = \frac{|V \quad (t)|}{n} d(t)$$

Where

N1 = primary number of turns

N2 = secondary number of turns

V_{out} (t) = instantaneous output source voltage

V_{ab} (t) = instantaneous input source voltage

n = insulation transformer turns ratio

And

Substituting for T_o and V_{out} (t) in equation (1) and noting that the limits of integration is between t_0 and t_1 (as discussed in section 3.2.6) yields:

$$V \quad = \frac{2}{T} \quad \frac{|V \quad (t)|}{n} d(t) \qquad (2)$$

$$T \ = t \ = \frac{T}{2}$$

Where

T_o = period of instantaneous output voltage waveform

T_s = period of instantaneous input voltage waveform

Since the magnitude of V_{ab} (t) during the interval (t_0, t_1) is equal to V_I (the input dc supply voltage), this substitution can also be made to solve for equation (2).

$$V \quad , \ = \frac{2}{T} \quad \frac{E}{n} d(t)$$

$$V \quad , \ = \frac{2E}{nT}(t \ - t \ ) = \frac{E}{n} \ \frac{2t}{T} - \frac{2t}{T} \qquad (3)$$

Looking back at Figure 3.3(f) the plot of the theoretical load current reconstructed in Figure 3.6 for convenience, it can be seen that during the time interval (0, t_0), the current i_{Lr} (t) can be represented by a linear equation of the form y = mt + b.

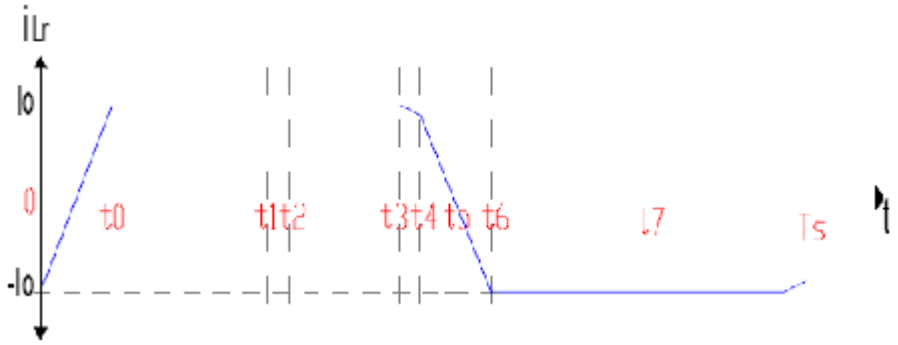

Figure 3.6: Theoretical plot of the current i_{Lr}.

This linear equation can be realized by inspecting the circuit of Figure 3.4(a) (the first stage of operation of the converter), and drawing an equivalent circuit model from the current commutation standpoint of view during this interval. This is shown in Figure 3.7. It is stressed again that this equivalent circuit applies only during the given interval $(0, t_0)$.

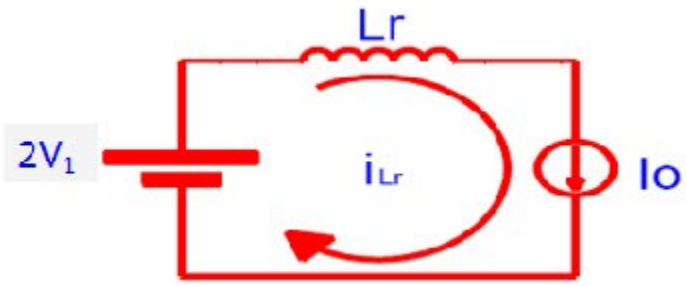

Figure 3.7: Equivalent circuit diagram of figure 3.4(a) from the current commutation standpoint of view through the converter during the interval $(0, t_0)$.

Based figure 3.7, KVL is applied:

$$-E + V\ (t) = 0\ V$$

$$-E + L\ \frac{di\ (t)}{dt} = 0\ V \qquad (4)$$

Rearranged equation (4)

$$di\ (t) = \frac{E}{L} dt \qquad (5)$$

Equation (5) can be evaluated to obtain $i_{Lr}(t)$ by integrating both the left hand side and right hand side, and also noting that the initial value of current flowing through the commutation inductor looking at Figure 6 is (i.e. $i_{Lr}(0) = -I_o$).

$$i\ (t) = \frac{E}{L} dt + i\ (0)$$

$$i\ (t) = \frac{E}{L} t + i\ (0) = \frac{E}{L} + I \qquad (6)$$

Equation (6) represents a linear equation of current $i_{Lr}(t)$ as previously discussed. Referring to Figure 3.6, it is noted that at time t_0, the current $i_{Lr}(t)$ is equal to the full load current.

Using equation (6) to make this substitution, t_0 can be evaluated for in terms of the commutation inductor L_r, the full load current I_o, and the dc input supply voltage, V_1.

At time $t = t_0$, $i_{Lr} = I_o$

Substituting in equation (6) and solving for t_0:

$$i\ (t\ ) = I\ = \frac{E}{L} t\ - I$$

$$t\ = \frac{2L\ I}{E} \qquad (7)$$

Substituting equation (7) into equation (3), an attempt is made such that the output voltage can be obtained in terms of the input dc source voltage and an effective duty cycle.

$$V\ \ ,\ = \frac{E}{n}\ \frac{2t}{T} - \frac{2t}{T}$$

$$V\ \ ,\ = \frac{E}{n}\ \frac{2t}{T} - \frac{2(2L\ I\ )}{ET}$$

$$V\ \ ,\ = \frac{E}{n}\ \frac{2t}{T} - \frac{4f\ L\ I}{E} \qquad (8)$$

As a result of equation (8), we can define two terms of duty cycle that will aid in describing the output voltage in terms of the given parameters of the dc-to-dc converter and its component values.

Define the control duty cycle to be:

$$D = \frac{2t}{T} \tag{9}$$

Now define the reduction of the control duty cycle due to the commutation inductor L_r to be:

$$\Delta D = \frac{4f\ L\ I}{E} \tag{10}$$

Substituting equation (9) and (10) into equation (8):

$$V_{,} = \frac{E}{n}(D - \Delta D) \tag{11}$$

Define the effective duty cycle:

$$D = (D - \Delta D) \tag{12}$$

Thus finally, equation (8) of the average output voltage can be written in terms of the effective duty cycle transformer turns ratio and the input dc supply voltage as follows.

$$V_{o}' = D_{eff}\frac{E}{n} \qquad (13)$$

With equation (13) the effective duty cycle can thus also be written in terms of the input and output voltages as follows.

$$D_{eff} = \frac{nV_{o}'}{E} = D - \frac{4f\ L\ I_{o}}{E} \qquad (14)$$

Equation (14) represents the voltage conversion ratio of the TL-ZVS-PWM converter. It can be seen that the larger the value of the commutation inductor L_r, the more the output voltage is reduced due to the reactive voltage drop that is due to the reduction in effective duty cycle, D_{eff}.

Using equation (14) the effective duty cycle can be evaluated.

$$D_{eff} = \frac{nV_{o}'}{E}$$

Where

$V_{out,ave}$ = 12 V

V_1 = 12 V

n = 0.5

Thus

$$D = \frac{0.5(12)}{(12)} = 0.5$$

In order to solve for the commutation inductance L_r, a value is selected such that a 25% reduction in control duty is tolerated as characterized by the following equation.

$$\Delta D = 0.25D \quad (15)$$