12V CAR BATTERY TO 230V AC POWER

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12V CAR BATTERY TO 230VAC POWER INVERTER

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This thesis is submitted as partial fulfillment of the requirements for the award of the Bachelor of Electrical Engineering (Electronics)

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DEDICATION

Specially dedicated to
My beloved parents, sisters
and all of my best friends.

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ABSTRACT

Power inverters, regardless of size, are typically constructed of a DC-AC converter. A pure sine wave output will be obtained through the use of a microcontroller and high frequency switching. The microcontroller will be used to digitally drive the transistors on the inverter side of the circuit. This will result in pulses at precise time intervals. The slope and magnitude of the output signal will be exact, as opposed to the unstable signal generated by other power inverters that use analog technology. Implementing the use of a microcontroller also allows for the different alarms and to ensure safety of the user. This power inverter will operate using high frequency switching technology. The harmonics that are produced using high frequency switching will include those near the range of the switching frequency, and those that are of a relatively higher order than the 50 Hz frequency. These harmonics can be isolated using a small low-pass filter. This translates into a much cleaner output signal. Also, the use of high frequency switching will minimize the size of parts used for the construction of the inverter. Future work could be done to further improve efficiency, total harmonic distortion, and size of the power inverter. With these additional improvements, the standard could be raised for future DC/AC power supplies.

ABSTRAK

Penyongsang kuasa, tanpa mengira saiz, adalah terdiri daripada penukar DC-AC. Gelombang sinus yang tulen akan diperoleh dengan mengunakan mikropengawal dan frekuensi pensuisan tinggi. Mikropengawal akan digunakan untuk menghidupkan transistor di dalam bahagian litar penyongsang. Ini akan menghasilkan denyut pada sela masa yang jitu. Maka terhasil kecerunan dan magnitude signal yang tepat, berbeza dengan signal keluaran tidak stabil yang dihasilkan oleh penyongsang kuasa lain dengan menggunakan teknologi analog. Penggunaan mikropengawal juga boleh menghasilkan perbezaan gera dan memastikan keselamatan pengguna. Operasi penyongsang kuasa ini menggunakan teknologi frekuensi pensuisan tinggi. Harmonik yang diperoleh dari frekuensi pensuisan tinggi adalah lebih tinngi dari 50 HZ frequency. Harmonik ini dapat dipencil dengan menggunakan penapis lepasan rendah. Ini akan manghasilkan signal keluaran yang jelas. Dengan mengunakan frekuensi pensuisan tinggi juga dapat minimum saiz penyongsang kuasa tersebut. Penbaik pulihkan dapat dijalankan pada masa depan terhadap kecekapan, herotan harmonic seluruh dan saiz penyongsang kuasa. Dengan pembaik pulihkan ini, piawai untuk penjana kuasa DC/AC dapat dinaikan pada masa depan.

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LIST OF SYMBOLS

DC	-	Direct Current
AC	-	Alternate Current
Hz	-	Hertz
kHz	-	kilo Hertz
MHz	-	mega Hertz
uF	-	micro Farad
kΩ	-	kilo Ohm
mH	-	mili Henry
V	-	Volt
I	-	Ampere
VA	-	apparent power

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CHAPTER 1

INTRODUCTION

1.1 Background

Mobility and versatility have become bigger issues with the advancement of technology. A person should not be limited to use an electronic tool or gadget at a fixed location due to power limitations. Overcoming the obstacle of having a mobile AC power source has led to the invention of DC/AC power inverters. In the market, inexpensive inverters are very inefficient due to a high harmonic content of the output signal and pure sine wave inverters have a high cost per watt ratio

In order to overcome the problem, a power inverter is develop so that it can produce a near perfect sine wave output. A power inverter of DC to AC type will be needed to convert 12 VDC to 230 VAC. The DC/AC inverter circuit will use a microprocessor to digitally pulse the transistors. This will allow it to produce a pure sine wave output.

1.2 Objective

The objective of this project is the development power inverter that can convert 12VDC into 230VAC and the development of power inverter will use of high frequency switching and implementation of a microprocessor to digitally pulse to the transistors.

1.3 Scope of Project

This project involves determining the characteristic of power inverter. The development the source code for microcontroller so that it can implementation of a microprocessor to digitally pulse to the power electronic. The development low pass filter for isolate the harmonic so that the inverter retain a 50 Hz fundamental frequency.

1.4 Problem Statement

Electronic mobility has always been an issue when it comes to our mobile environment. Therefore, a mobile means of providing AC voltage is needed. When these devices need to be used in a remote or mobile setting there is a problem. A power inverter of DC to AC type will be needed to convert 12 VDC to 230 VAC.

1.5 Methodology

In this project, the two main parts that are evaluated are the PIC18F452 and inverter. The testing includes the evaluation board before writing the software and developed the full-bridge inverter circuit that will convert DC voltage to AC voltage.

Overall steps taken to achieve the objectives are testing the PIC functionality by checking the program in the MPLAB. Simulate the power inverter circuit by using PSIM. The output signals from PIC and output voltage from power inverter are checked after the hardware is complete.

1.6 Thesis Outline

Chapter 1 discuss on the background of the project, objectives, scope of the project, problem statement, methodology and also the thesis outline.

Chapter 2 focuses on literature reviews of this project based on journals and other references.

Chapter 3 mainly discuss on the system design of the project. Details on the progress of the project are explained in this chapter.

Chapter 4 presents the results of the project. The discussion focused on the result based on the experiment.

Chapter 5 concludes overall about the project. Obstacle faces and future recommendation are also discussed in this chapter.

CHAPTER 2

LITERATURE REVIEW

2.1 DC and AC Current

In the world today there are currently two forms of electrical transmission, Direct Current (DC) and Alternating Current (AC), each with its own advantages and disadvantages. DC power is simply the application of a steady constant voltage across a circuit resulting in a constant current. A battery is the most common source of DC transmission as current flows from one end of a circuit to the other. Most digital circuitry today is run off of DC power as it carries the ability to provide either a constant high or constant low voltage, enabling digital logic to process code executions. Historically, electricity was first commercially transmitted by Thomas Edison, and was a DC power line. However, this electricity was low voltage, due to the inability to step up DC voltage at the time, and thus it was not capable of transmitting power over long distances [1].

$$V = IR$$
$$P = IV = I^2R \quad (1)$$

As can be seen in the equations above, power loss can be derived from the electrical current squared and the resistance of a transmission line. When the voltage is increased, the current decreases and concurrently the power loss decreases exponentially; therefore high voltage transmission reduces power loss. For this reasoning electricity was generated at power stations and delivered to homes and businesses through AC power. Alternating current, unlike DC, oscillates between two voltage values at a specified frequency, and it's ever changing current and voltage makes it easy to step up or down the voltage. For high voltage and long distance transmission situations all that is needed to step up or down the voltage is a transformer. Developed in 1886 by William Stanley Jr., the transformer made long distance electrical transmission using AC power possible [2].

Electrical transmission has therefore been mainly based upon AC power, supplying most American homes with a 120 volt AC source. It should be noted that since 1954 there have been many high voltage DC transmission systems implemented around the globe with the advent of DC/DC converters, allowing the easy stepping up and down of DC voltages [3].

Like DC power, there exist many devices such as power tools, radios and TV's that run off of AC power. It is therefore crucial that both forms of electricity transmission exist; the world cannot be powered with one simple form. It then becomes a vital matter for there to exist easy ways to transform DC to AC power and vice versa in an efficient manner. Without this ability people will be restricted to what electronic devices they use depending on the

electricity source available. Electrical AC/DC converters and DC/AC inverters allow people this freedom in transferring electrical power between the two.

2.2 Inverters and Applications

Power inverters are devices which can convert electrical energy of DC form into that of AC. They come in all shapes and sizes, from low power functions such as powering a car radio to that of backing up a building in case of power outage. Inverters can come in many different varieties, differing in price, power, efficiency and purpose. The purpose of a DC/AC power inverter is typically to take DC power supplied by a battery, such as a 12 volt car battery, and transform it into a 230 volt AC power source operating at 50 Hz, emulating the power available at an ordinary household electrical outlet.

Figure 2.1: Commercial 200 Watt Inverter

Figure 2.1 provides an idea of what a small power inverter looks like. Power inverters are used today for many tasks like powering appliances in a car such as cell phones, radios and televisions. They also come in handy for consumers who own camping vehicles, boats and at construction sites where an electric grid may not be as accessible to hook into. Inverters allow the user to provide AC power in areas where only batteries can be made available, allowing portability and freeing the user of long power cords. On the market today are two different types of power inverters, modified sine wave and pure sine wave generators. These inverters differ in their outputs, providing varying levels of efficiency and distortion that can affect electronic devices in different ways.

A modified sine wave is similar to a square wave but instead has a "stepping" look to it that relates more in shape to a sine wave. This can be seen in Figure 2.2, which displays how a modified sine wave tries to emulate the sine wave itself. The waveform is easy to produce because it is just the product of switching between 3 values at set frequencies, thereby leaving out the more complicated circuitry needed for a pure sine wave. The modified sine wave inverter provides a cheap and easy solution to powering devices that need AC power. It does have some drawbacks as not all devices work properly on a modified sine wave, products such as computers and medical equipment are not resistant to the distortion of the signal and must be run off of a pure sine wave power source.

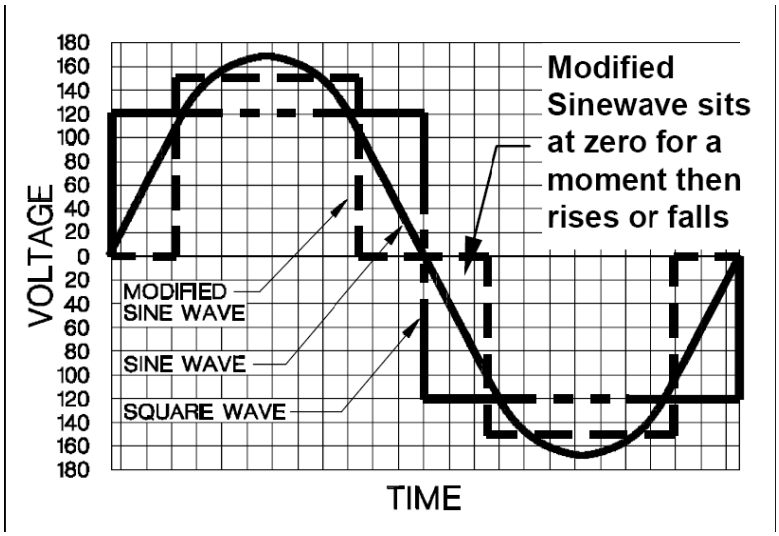

Figure 2.2: Square, Modified, and Pure Sine Wave

Pure sine wave inverters are able to simulate precisely the AC power that is delivered by a wall outlet. Usually sine wave inverters are more expensive then modified sine wave generators due to the added circuitry. This cost, however, is made up for in its ability to provide power to all AC electronic devices, allow inductive loads to run faster and quieter, and reduce the audible and electric noise in audio equipment, TV's and fluorescent lights. [3]

2.3 Microcontroller

A PIC18F452 would be able to do various task. It has 512 bytes of EEPROM and RAM while the ROM is disabled. This is a 8-bit microcontroller that have 5 ports that are Port A, Port B, Port C, Port D and Port E. Several of features are built-in in the PIC18F452 that contain high performance RISC CPU, power saving STOP and WAIT modes, wide operating voltage rate (2.0 – 5.5 Vdc), 1538 bytes of on-chip RAM, data retained during standby, 256 bytes of on-chip EEPROM with block protect for security, asynchronous non-return to zero (NRZ) serial communications interface (SCI), synchronous serial peripheral interface (SPI), 10-bit analog-to-digital (A/D) converter, 16-bit timer system, PWM output resolution is 1- to 10-bit, 8-bit pulse accumulator, real-time interrupt circuit, computer operating properly (COP) , 35 general-purpose input/output (I/O) pins.

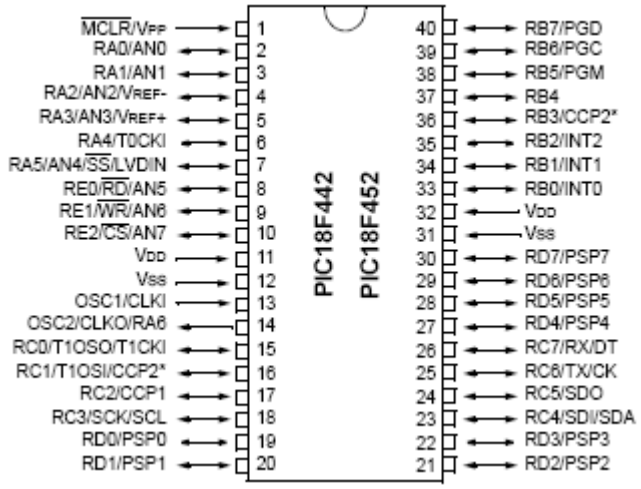

Figure 2.3 Architecture of PIC18F452 Series Port Functionality

A microcontroller is a highly integrated chip which performs controlling functions. A microcontroller, or embedded controller, is similar to a microprocessor as used in a personal computer, but with a great deal of additional functionality combined onto the same monolithic semiconductor substrate. Microcontrollers, sometimes referred to as one-chip microcomputers, are used to control a wide range of electrical and mechanical appliances. Since they were first introduced, microcontrollers have evolved to the point where they can use for increasing complex applications. Some microcontrollers in use today are also programmable, expanding the number of application in which they can be used. [4]

In this article, the use of a microcontroller is essential in a project of this nature. The microcontroller will be used to digitally drive the transistors on the inverter side of the circuit. This will result in pulses at precise time intervals. The slope and magnitude of the output signal will be exact, as opposed to the unstable signal generated by other power inverters that use analog technology. Implementing the use of a microprocessor also allows for the different alarms and tests which deal with the health and safety concerns.

2.4 Pulse Width Modulation (PWM)

In electronic power converters and motors, PWM is used extensively as a means of powering alternating current (AC) devices with an available direct current (DC) source or for advanced DC/AC conversion. Variation of duty cycle in the PWM signal to provide a DC voltage across the load in a specific pattern will appear to the load as an AC signal, or can control the speed of motors that would otherwise run only at full speed or off. This is further explained in this section. The pattern at which the duty cycle of a PWM signal varies can be created through simple analog components, a digital microcontroller, or specific PWM integrated circuits.

Analog PWM control requires the generation of both reference and carrier signals that feed into a comparator which creates output signals based on the difference between the signals. The reference signal is sinusoidal and at the frequency of the desired output signal, while the carrier signal is often either a sawtooth or triangular wave at a frequency significantly greater than the reference. When the carrier signal exceeds the reference, the comparator output signal is at one state, and when the reference is at a higher voltage, the output is at its second state. This process is shown in Figure 2.4 with the triangular carrier wave in red, sinusoidal reference wave in blue, and modulated and unmodulated sine pulses. [5]

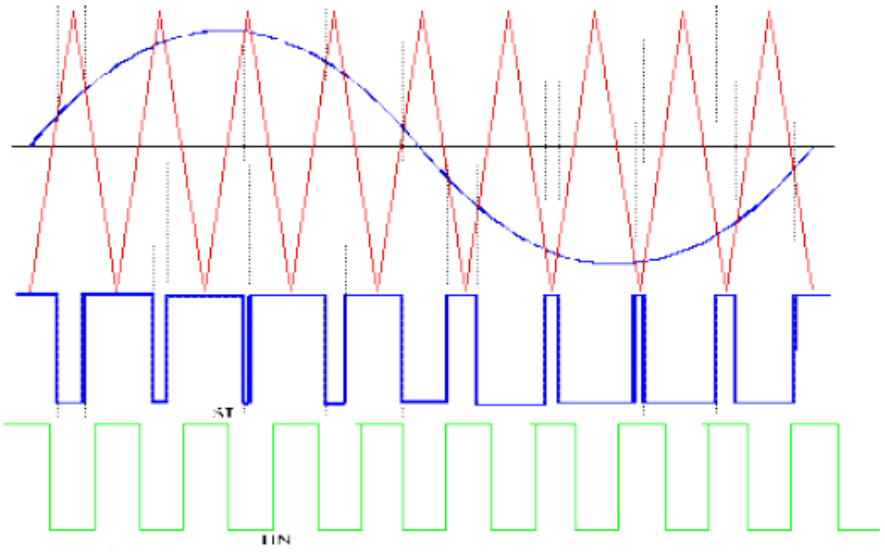

Figure 2.4: Pulse Width Modulation

In order to source an output with a PWM signal, transistor or other switching technologies are used to connect the source to the load when the signal is high or low. Full or half bridge configurations are common switching schemes used in power electronics. Full bridge configurations require the use of four switching devices and are often referred to as H-Bridges or full-bridge due to their orientation with respect to a load.

2.5 Driver Circuit

A driver circuit is use to interface between control (low power electronics) and (high power) switch. It main functions are amplifies control signal to a level required to drive power switch and provides electrical isolation between power switch and logic level. [6]

When utilizing N-Channel MOSFETs to switch a DC voltage across a load, the drain terminals of the high side MOSFETs are often connected to the highest voltage in the system. This creates a difficulty, as the gate terminal must be approximately 10V higher than the drain terminal for the MOSFET to conduct. Often, integrated circuit devices known as MOSFET drivers are utilized to achieve this difference through charge pumps or bootstrapping techniques. These chips are capable of quickly charging the input capacitance of the MOSFET (Cgiss) quickly before the potential difference is reached, causing the gate to source voltage to be the highest system voltage plus the capacitor voltage, allowing it to conduct. A diagram of an N-Channel MOSFET with gate, drain, and source terminals is shown in Figure 2.5.

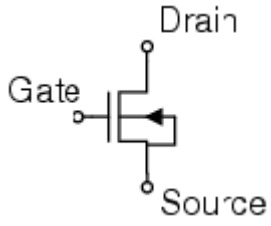

Figure 2.5: N-Channel MOSFET

There are many MOSFET drivers available to power N-Channel MOSFETs through level translation of low voltage control signals into voltages capable of supplying sufficient gate voltage. Advanced drivers contain circuitry for powering high and low side devices as well as N and P-Channel MOSFETs. In this design, two sets of MOSFET both P and N-Channel are used and are controlled by the antiphase.

2.6 Full-Bridge Inverter

An H-Bridge or full-bridge converter is a switching configuration composed of four switches in an arrangement that resembles an H. By controlling different switches in the bridge, a positive, negative, or zero potential voltage can be placed across a load. When this load is a motor, these states correspond to forward, reverse, and off. The use of an H-Bridge configuration to drive a motor is shown in Figure 2.6. [7]

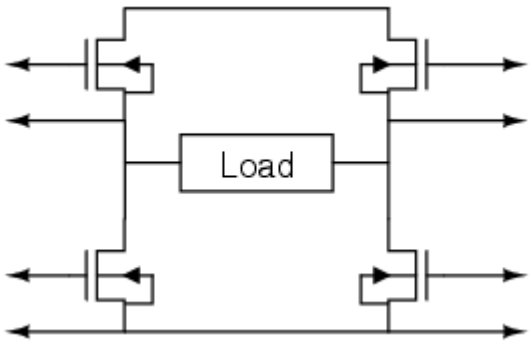

Figure 2.6: H-Bridge Configuration using N-Channel MOSFET

As shown in Figure 2.6 the H-Bridge circuit consists of four switches corresponding to high side left, high side right, low side left, and low side right. There are four possible switch positions that can be used to obtain voltages across the load. These positions are outlined in Table 1. Note that all other possibilities are omitted, as they would short circuit power to ground, potentially causing damage to the device or rapidly depleting the power supply.

Table 2.1: H-Bridge Switch States

High Side Left	High Side Right	Low Side Left	Low Side Right	Voltage Across Load
On	Off	Off	On	Positive
Off	On	On	Off	Negative
On	On	Off	Off	Zero Potential
Off	Off	On	On	Zero Potential

The switches used to implement an H-Bridge can be mechanical or built from solid state transistors. Selection of the proper switches varies greatly. The use of P-Channel MOSFETs on the high side and N-Channel MOSFETs on the low side is easier, but using all N-Channel MOSFETs and a FET driver, lower “on” resistance can be obtained resulting in reduced power loss. The use of all N-Channel MOSFET’s requires a driver, since in order to turn on a high side N-Channel MOSFET, there must be a voltage higher than the switching voltage (in the case of a power inverter, 170V). This difficulty is often overcome by driver circuits capable of charging an external capacitor to create additional potential.

2.7 Circuit Protection and Snubbers

One of the major factors in any electronic device is its ability to protect itself from surges that could damage the circuitry. In the case of the inverter, inductive loads can cause special problems because an inductor cannot instantly stop conducting current, it must be dampened or diverted so that the current does not try to flow through the open switch. If not dampened the surges can cause trouble in the MOSFETs used to produce the output sine wave; when a MOSFET is turned off the inductive load still wants to push current through the switch, as it has no where else to go. This action can cause the switch to be put under considerable stress, the high dV/dt, dI/dt, V and I associated with this problem can cause the MOSFETs to malfunction and break. [7]

To combat this problem snubber circuits can reduce or eliminate any severe voltages and currents. Composed of simply a resistor and capacitor placed across each switch it allows any current or voltage spikes to be suppressed by critically dampening the surge and protecting the switch from damage. The snubber can become more effective by the addition of a zener diode so that any large current surge the resistor-capacitor snubber cannot handle gets passed through to ground by the zener diode. The diagram in Figure 2.7 shows a simple representation of an inductive load (L) over a switch representation, Figure 2.8 and Figure 2.9 show how snubbers can be implemented so that a surge will be suppressed.

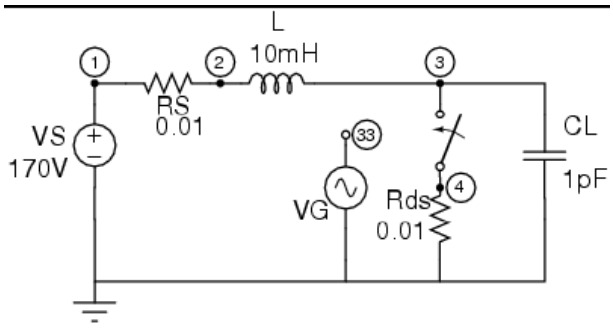

Figure 2.7: Inductive Load Circuit

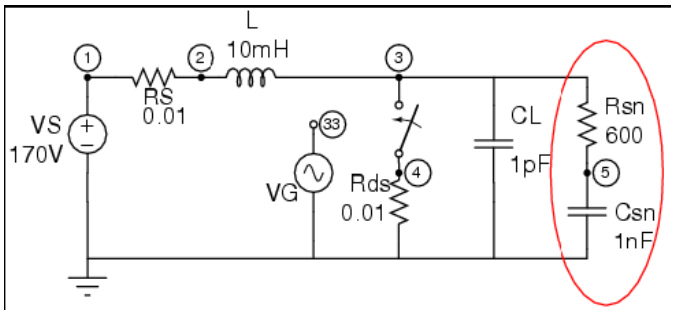

Figure 2.8: Inductive Load Circuit with Snubber

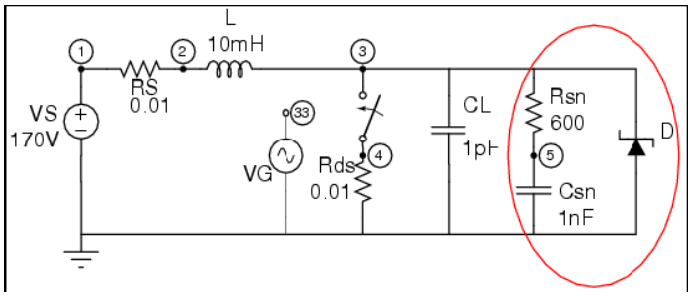

Figure 2.9: Inductive Load Circuit with Snubber and Zener Diode

2.8 Transformer

The transformer is the part of the circuit that is responsible for boosting the voltage. It does this by means of a ferrite core, primary, and secondary windings. It is important to note that the transformer does not create power; it merely transforms or transfers it. Ideally, power in is equal to power out, but in a real world case there is some power loss in the device. The transformer operates by inducing a magnetic flux on the core from the current flowing through the primary winding. This flux passing through the core is induced onto the secondary winding and current flows out of the device. [8]

The transformer used in this project is used to step up the voltage from the half-bridge converter to provide an approximate voltage of 240 VAC with an approximate frequency of 50 kHz.

2.9 Low-Pass Filter

This power inverter will operate using high frequency switching technology. The harmonics that are produced using high frequency switching will include those near the range of the switching frequency, and those that are of a relatively higher order than the 50 Hz frequency. Most of the harmonics will be the ones that are higher in order than the 50 Hz frequency. These harmonics can be isolated using a small low-pass filter. This translates into a much cleaner output signal. [9]

In order to eliminate the switching frequency and all multiples of the switching frequency, a low-pass filter had to be inserted after the output of the full-bridge inverter. A low-pass filter only allows frequencies below the cutoff-frequency to pass. The filter will reject any frequency above the cutoff frequency. The cutoff frequency can be set by the following formula:

$$F_{cutoff} = \frac{1}{2\pi\sqrt{LC}} \qquad (2)$$

Filters come in many different packages, with many different advantages – and disadvantages. For example, a digital filter is easily reconfigurable and can have almost any frequency response desired. If the response is simply low-pass/ high-pass/ band-pass behavior with a set frequency, an active filter can be made to have a very sharp edge at the cutoff, resulting in enormous reductions in noise and very little attenuation of the signal. These, however, require op-amps. Op-amps capable of filtering a 240V RMS sine wave exist, but are expensive, since the op-amp must be

able to source hundreds of watts, and must be very large to do so without burning. Digital filters have a similar drawback and, designed with TTL and CMOS technology, can only work with small signals. Lastly we come to a passive filter. Generally large in size and very resistive at low frequencies, these filters often seem to have more of a prototyping application, or perhaps use in a device where low cost is important, and efficiency is not. [9]

Given these choices, an application such as a high power sine inverter is left with only one viable option: the passive filter. This makes the design slightly more difficult to accomplish. Noting that passive filters introduce higher resistance at lower frequencies (due to the larger inductances, which require longer wires), the obvious choice is to switch at the highest possible frequency. The problem with this choice, however, is that the switching MOSFETs introduce more switching losses at higher frequencies. This would imply that we should switch slower to improve our switching efficiency, which contradicts the filter's need for a higher frequency.

CHAPTER 3

SYSTEM DESIGN

3.1 Overall System Design

One of the most important considerations in building a power inverter is the output signal. A block diagram of the power inverter is shown in Figure 3.1 below.

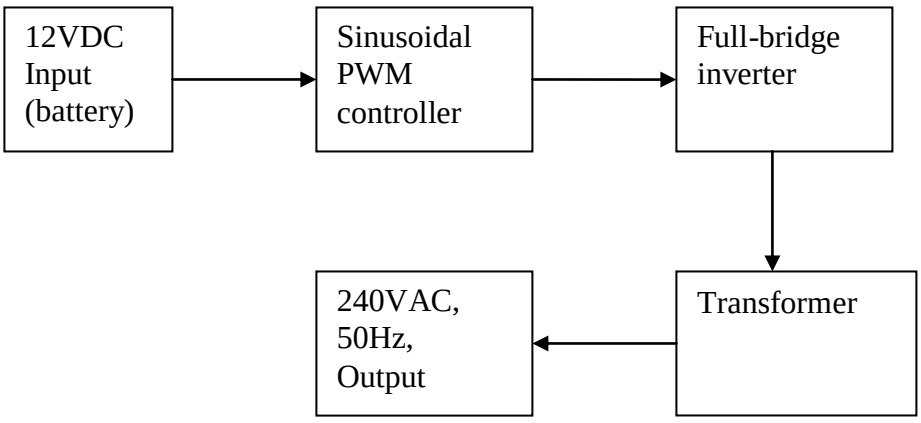

Figure 3.1: Power Inverter Block Diagram

3.2 Sinusoidal PWM Controller

Various PWM techniques have been used to create transistor drive circuits. Before microcontrollers became popular, varying PWM circuits usually consisted of analog-to-digital comparator circuits. These circuits compared a small voltage sinusoidal wave (reference signal) to a small voltage saw-tooth wave (control frequency signal). At each point where the sinusoidal and saw-tooth signals intersect, the output of the comparator toggles from a high state to a low state. To illustrate the theory behind sinusoidal PWM, Figure 3.2 shows the expected output of a sine wave compared to a saw-tooth wave. The duty cycle actually varies according to the time between sampling the reference sine wave.

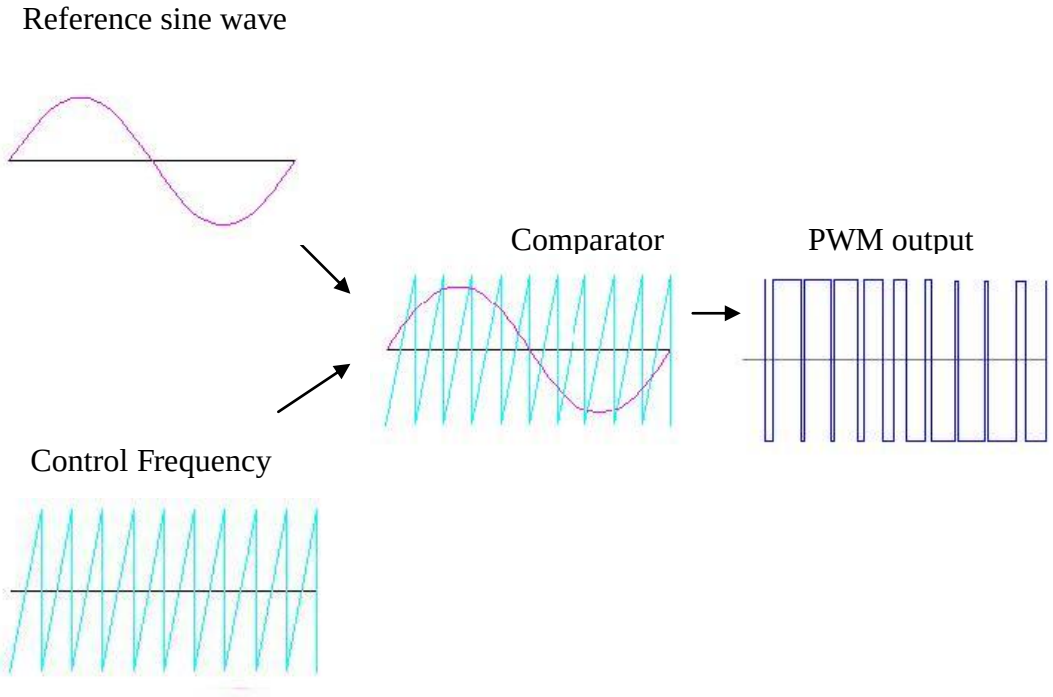

Figure 3.2: Theory of PWM Components

A schematic of the sinusoidal PWM controller circuit is shown in Figure 3.3 below. The major components for this circuit include a microcontroller, and an oscillator. This circuit produces two output pulses with varying duty cycles in order to drive the full-bridge inverter circuit.

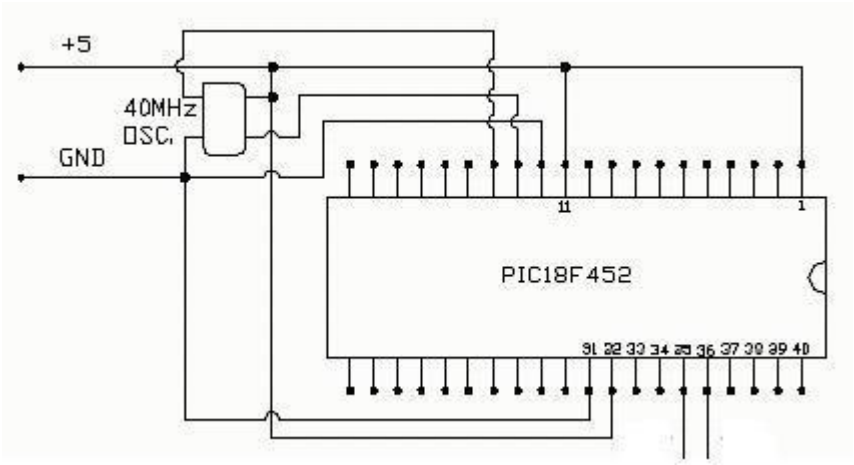

Figure 3.3: Sinusoidal PWM Controller Circuit

The microcontroller is utilized for storing pre-programmed duty cycles with its memory. This eliminated the need for large analog components which often have a tendency to become unstable. The microcontroller of choice for this project was Microchip's PIC18F252. The PIC18F252 was chosen primarily because it had enough on-board memory to store all of the necessary duty cycles values. Sufficient program memory will allow us to increase the number of duty cycles that make up one cycle of a 50 Hz sine wave. In turn, an increase number of duty cycles allows for a more precise resolution in the final output signal of the packaged product. Other advantages of the PIC18F252 were reflected by the low cost, fast processing speed, flash memory, and the ability to add extra features (such as low voltage alarms, extra phases, temperature sensors, etc.) in the future.

The following equations were used to calculate the modulation amplitude and modulation frequency for the PWM signal:

$$\text{Amplitude Modulation Ratio} = \frac{V_{control}}{V_{tri}} \quad (3)$$

$$\text{Frequency Modulation Ratio} = \frac{f_s}{f_1} \quad (4)$$

where, Vcontrol is the peak amplitude of the reference sine wave with frequency of f_1 and Vtri is the peak amplitude of the saw-tooth wave with frequency of f_s. By equations 3 and 4 the amplitude of the PWM pulse is directly proportional to Vcontrol and the frequency of the PWM pulse is directly proportional to f_s. A thorough discussion of the programming process involved in this project is located in the Software Design section of this document.

The amplitude ratio could not be changed in this case since the microcontroller was only capable of outputting a 5 volt logic signal. The frequency modulation ratio for this project came out to be approximately 400, which means that there were 400 completely different duty cycle values that make up a single half-cycle of the final output waveform. The frequency modulation was calculated by equation 4, where the reference sine wave (f_1) was set to 50 Hz and the saw-tooth wave (f_s) was set to 20 kHz. The switching frequency was set to 20 kHz in order to achieve a high resolution of the final output waveform.

3.3 The FET (field-effect transistor) Drive Circuit

The FET driver circuit plays two vital roles in creating drive pulses suitable for operation of a full-bridge inverter circuit. First of all, the transistor 2SC1815‘s amplify the 5-volt logic signals output by the microcontroller to obtain a 12 volt signal necessary to fully turn on the MOSFET of the full-bridge circuit. A transistor drive pulse of less than 12 volts could result in excessive heating which occurs when the transistors being driven are operating in the linear mode of operation, which by the physical transistor construction, happens to be the most resistive regions of operation.

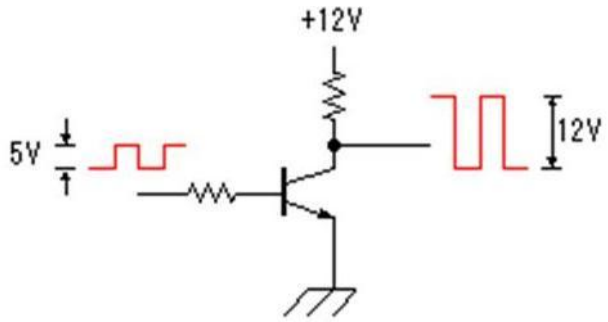

Figure 3.4: FET Drive Circuit

3.4 Full-Bridge Inverter

The full-bridge inverter circuit, as shown in Figure 3.5, is very simple to construct because it only consists of four switches. The function of the full-bridge inverter is to convert the 12 VDC link voltage supplied into a 240 VAC, 50 Hz sine wave. The transistors chosen for the full-bridge inverter circuit were the IRFP9140 and IRFP9150N. The IRFP9140 P-Channel Power MOSFET were chosen because they have the appropriate voltage and current ratings (Vdss = -100V, Id = -23A). The IRFP9150N N-Channel Power MOSFET were chosen because they have the appropriate voltage and current ratings (Vdss = 100V, Id = 44A).

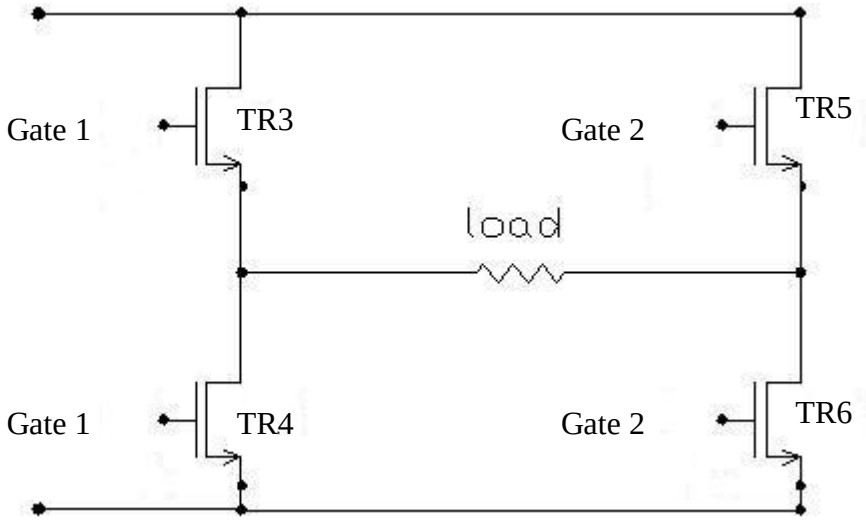

Figure 3.5: Full-Bridge Inverter Circuit

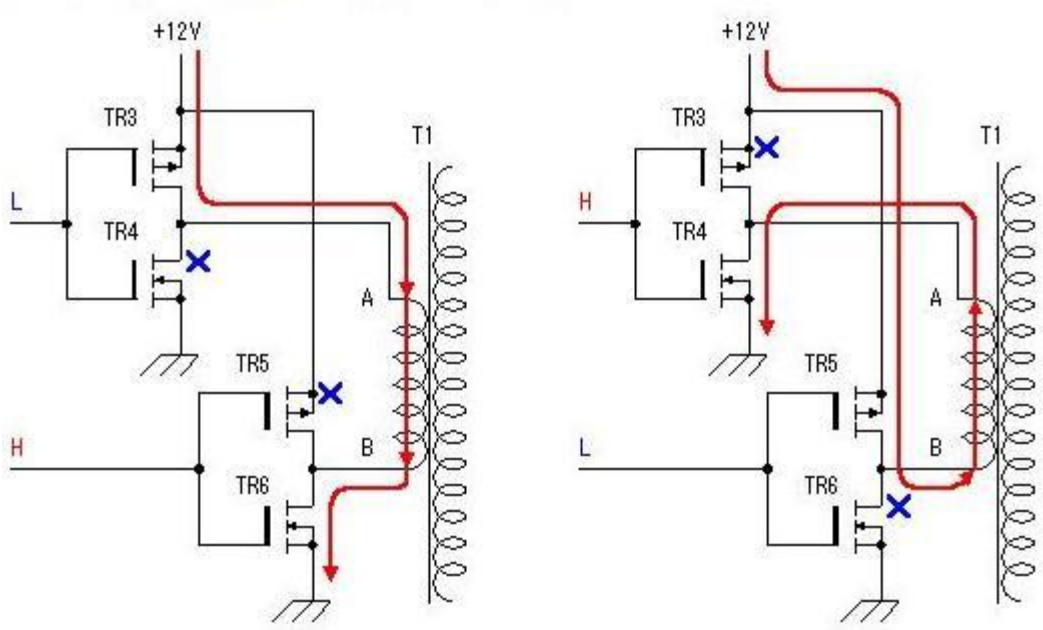

Figure 3.6: Function of Full-Bridge Inverter Circuit

In case of the input of TR3 and TR4 are L level and the input of TR5 and TR6 are H level, TR3 and TR6 become ON condition and TR4 and TR5 become OFF condition. Therefore, the electric current flows through the direction of A to B to the secondary coil(12V side) of the transformer.

When the input level is opposite, TR3 and TR6 become OFF condition and TR4 and TR5 become ON condition. Therefore, the electric current which flows through the transformer becomes contrary to the case of the above.

Either above-mentioned condition is continued when the oscillator stops. Therefore, the big electric current flows on the secondary side of the transformer. The fuse must be put to protect.

3.5 RCD Snubbers

In general, snubbers are used for minimize large over-currents through the device at turn-on and to minimize large over-voltages across the device during turn-off. The other function is stress reduction to shape the device switching waveform such that the voltage and current associated with the device are not high simultaneously.

The role of RCD snubber is to provide electrical isolation between the upper control pulses and the upper transistors of the full-bridge inverter circuit. Electrical isolation is extremely important in biasing the upper full-bridge transistors with the appropriate drive signal voltages.

Let the minimum switching time constant is $T = \frac{1}{20kHz}$ = 50usec.

Hence the RC should satisfy this time constant i.e RC = 50usec.

Let C = 0.01uF, then R = 500ohm.

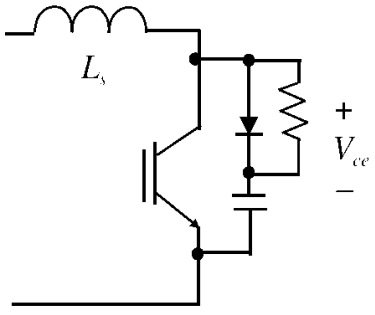

Figure 3.7: Snubber Circuit

3.6 Transformer

The transformer is the part of the circuit that is responsible for boosting the voltage. It does this by means of a ferrite core, primary, and secondary windings. It is important to note that the transformer does not create power; it merely transforms or transfers it. Ideally, power in is equal to power out, but in a real world case there is some power loss in the device. The transformer operates by inducing a magnetic flux on the core from the current flowing through the primary winding. This flux passing through the core is induced onto the secondary winding and current flows out of the device.

The transformer used in this project, which is also illustrated in Figure 3.8 below, is used to step up the voltage from the full-bridge converter to provide an approximate voltage of 240 VAC.

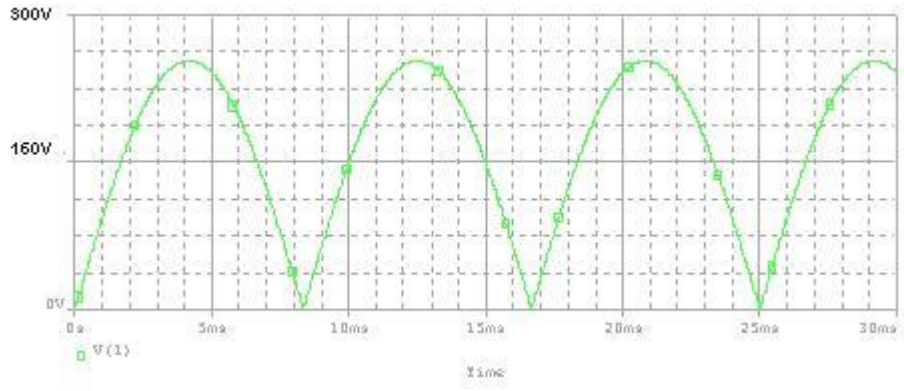

Figure 3.8: Simulation of Rectified Transformer Output (Before Filtering)

The output signal of the full-bridge inverter circuit will be a pulse waveform which contains the desired output waveform along with frequency components at or around harmonics of the switching frequency. This can be seen in Figure 3.9, which compares the unfiltered output of the final product to a simulation. The darker areas in Figure 3.9 represent the actual sine wave. A low-pass filter can be utilized to extract the desired output signal (50 Hz fundamental frequency) by separating it from the switching frequency.

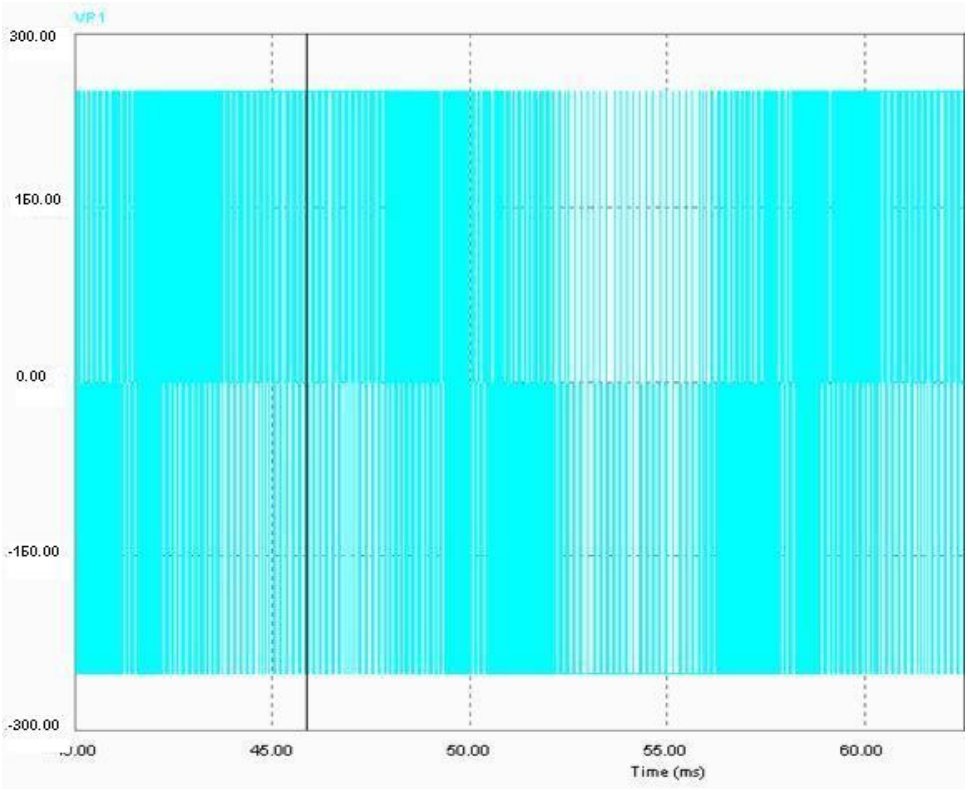

Figure 3.9: Unfiltered Output of the Power Inverter (Simulation)

3.7 Low-Pass Filter

In order to eliminate the switching frequency and all multiples of the switching frequency, a low-pass filter had to be inserted after the output of the full-bridge inverter. A low-pass filter only allows frequencies below the cutoff-frequency to pass. The filter will reject any frequency above the cutoff frequency. The cutoff frequency can be set by the following formula:

$$F_{cutoff} = \frac{1}{2\pi\sqrt{LC}} \quad (5)$$

Figure 3.8 shows the switching harmonics that resulted from a 20 kHz switching frequency. It should be noted that the harmonics are located at the switching frequency and multiples of the switching frequency. The switching frequency was intentionally set at 20 kHz so it would be rather distant from the 50 Hz fundamental frequency. This would allow for a high cutoff frequency, by using LC components. The large distance between the unwanted harmonics and the fundamental frequency is also beneficial because it allows for a large margin of error in the filter values.

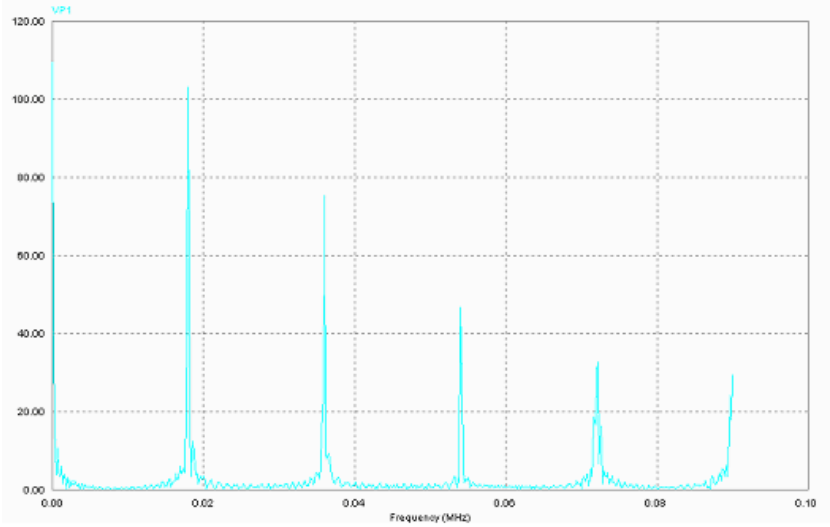

Figure 3.10: Frequency Spectrum of Unfiltered Full-Bridge Inverter Output

An L-C low-pass filter was chosen for the power inverter. This topology, as shown in Figure 3.10, is simple to build, contains few components, and can handle high currents.

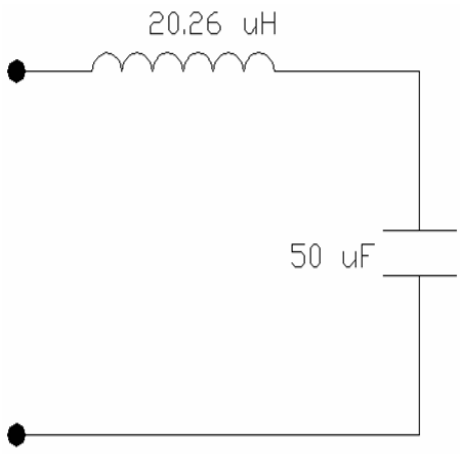

Figure 3.11: Low-Pass Filter Schematic

3.8 Software Design

Figure 3.10 illustrates the software flow diagram for PIC18F452 program. Basically the program uses pre-calculated duty cycle values which are stored in tables at the end of the program.

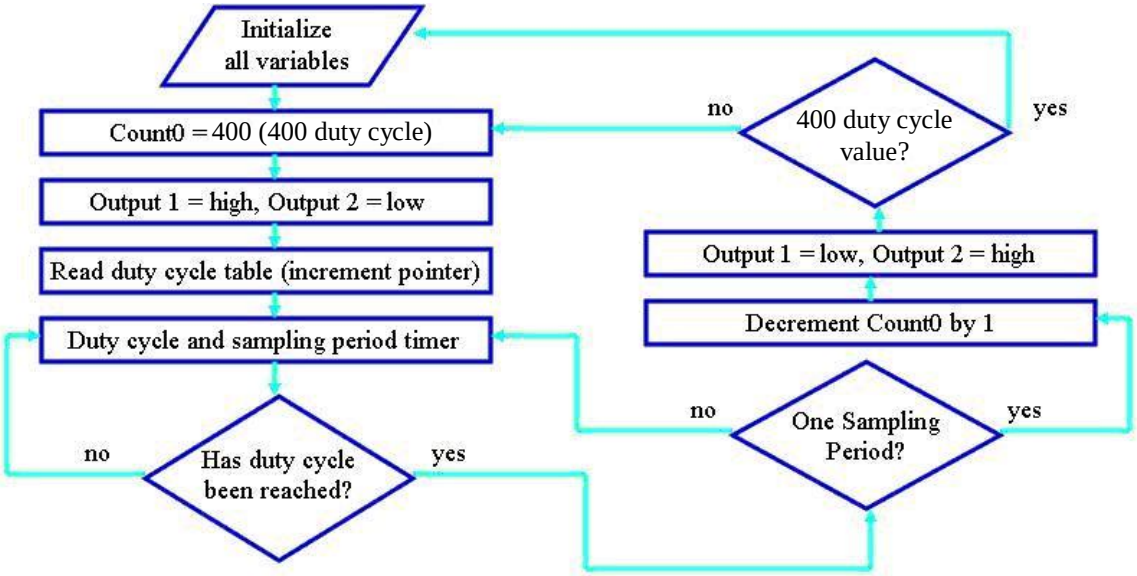

Figure 3.12: Software Flow Diagram for Full-Bridge Inverter Microcontroller

CHAPTER 4

RESULT

4.1 Software

4.1.1 MPLAB

MPLAB is emulation software that allows for compiling programs that are specifically written for MicroChip microcontrollers. MPLAB will be used to test that the assembly language code written for the microcontroller will execute properly. Once the code executes properly, it can be programmed into the PWM microcontroller. Since MPLAB supports flash memory, the program sent to the microcontroller can be erased by the click of a button. The following steps were taken to program the microcontroller. Firstly the microcontroller program is downloading to the MPLAB workspace. Then it will compile the program using the built-in compiler and check the program for any errors in syntax or parameterization. After successfully compiling the program, load it onto the microcontroller using the PICKIT v2 programmer.

4.1.2 Software Verification

To test the operation of the microcontroller, an oscilloscope will be used to observe the output waveforms of the microcontroller. The following step is the procedure of the test. Firstly**,** the circuit is connecting as shown in Figure 4.1. Secondly, power the microcontroller with 5Vdc from the bench power supply to pin 1, pin 11 and pin 32. Then connect pin 35 of the microcontroller to channel 1 of the oscilloscope and connect pin 36 of the microcontroller to channel 2 of the oscilloscope. Lastly, line the output waveforms one on top of the other and confirm that they are complement of one another as shown in Figure 4.2.

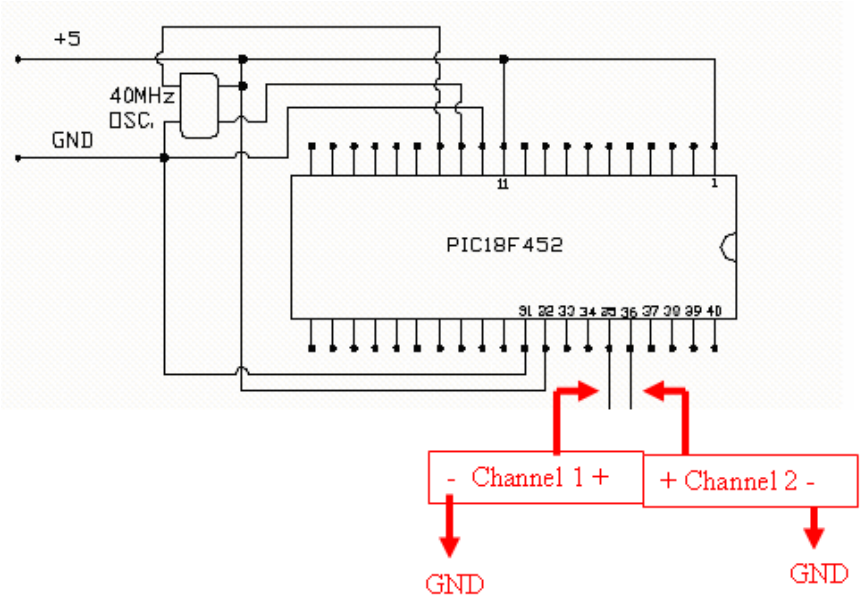

Figure 4.1: Software Testing Setup

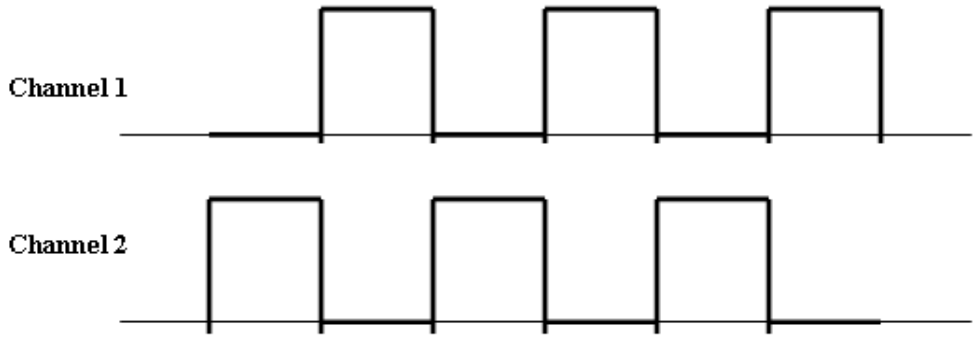

Figure 4.2: Output Waveforms of Microcontroller

4.2 Hardware

All individual hardware design is tested using an oscilloscope and a digital multi-meter. The key components of the overall power inverter are a PWM control circuit, a transformer, a sinusoidal PWM controller, a full-bridge inverter, and a low-pass filter. Each component was tested for the desired voltages, currents, efficiencies, and frequencies. The following sub-sections demonstrate the tests that were performed on the power inverter hardware.

4.2.1 The FET (field-effect transistor) Drive Circuit

The test setup for the FET drive circuit is illustrated in Figure 4.3. The following step is the procedure of the test. Firstly, setup the control circuit as shown in Figure 4.3. Then connect channel 1 of the oscilloscope across gate 1 and channel 2 across gate 2. Oscilloscope is use to verify the waveforms of the voltages are square pulses complimentary to each other with frequencies of 20 KHz and amplitudes of 12 V.

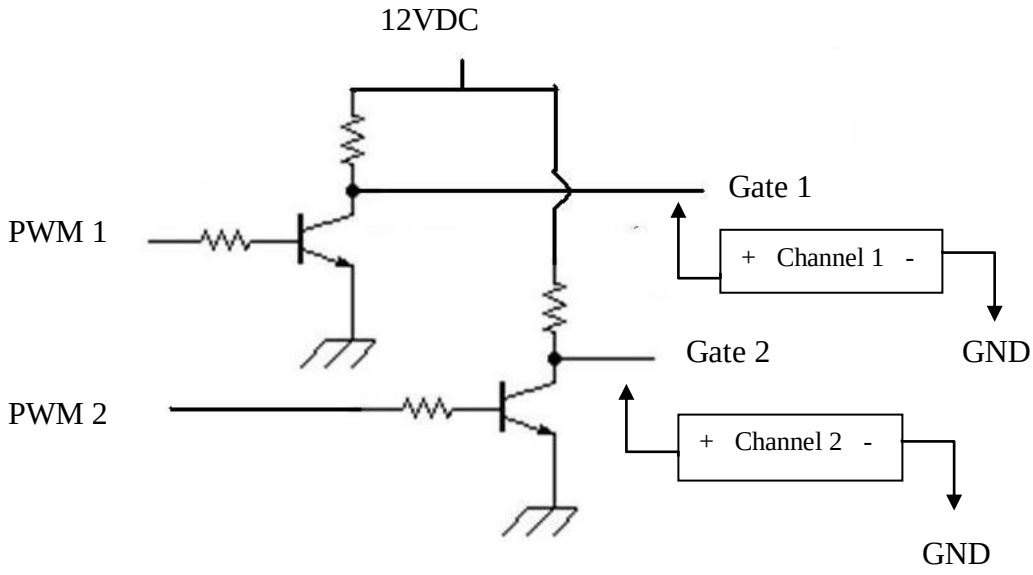

Figure 4.3: FET Drive Circuit Test Setup

4.2.2 Full Bridge Inverter

The test setup for the full bridge inverter is illustrated in Figure 4.4. The following step is the procedure of the test. Firstly**,** the circuit is connecting as shown in Figure 4.4. The voltage across the resistor is measure by using the oscilloscope. The 10X probes must be used when measuring voltages over 100 VAC. The output of the power inverter must verify that the voltage across the resistor is a PWM pulse that is 340V peak-to-peak with a frequency of 20 kHz and the output is 3A.

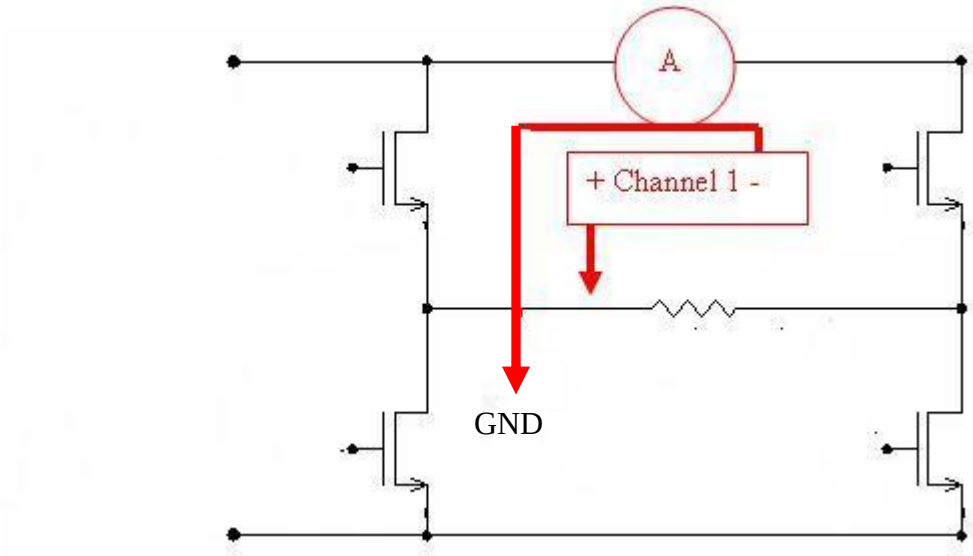

Figure 4.4: Full-Bridge Inverter Test Setup

4.2.3 Transformer

The test setup for the transformer is shown in Figure 18. Beneath the figure are the instructions for verifying proper transformer operation. The function generator is use to emulate the output square pulse of the full-bridge converter. The voltage is set to 12 V, the waveform to square wave, and the frequency to 100 kHz. The output of the function generator is feed into the primary side of the transformer. Channel 1 of the oscilloscope is connect to the secondary side of the transformer and verify that the output is a 240 V square wave with a 100 kHz frequency.

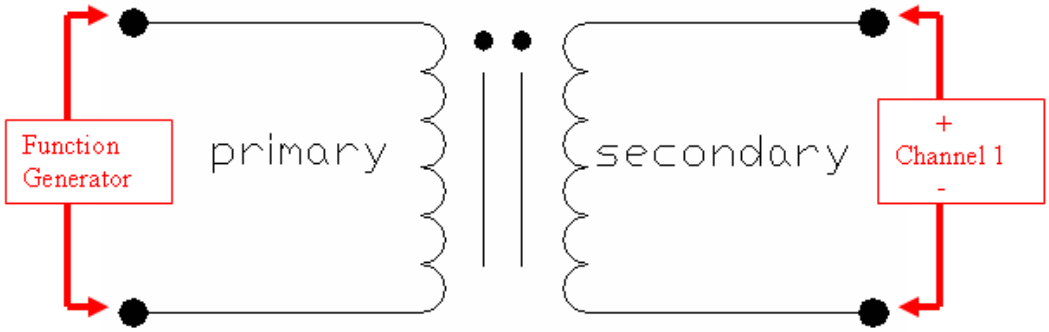

Figure 4.5: Transformer Test Setup

4.2.4 Low Pass Filter

The test setup for the low-pass filter is illustrated in Figure 4.5. The following step is the procedure of the test. Firstly, the circuit is connecting as shown in Figure 4.6. The 240 V peak-to-peak PWM pulse from the full-bridge inverter is feed to the LC filter. The voltages across the load are measured by using oscilloscope and verify that the output voltage is 240 V peak-to-peak with a frequency of 50 Hz.

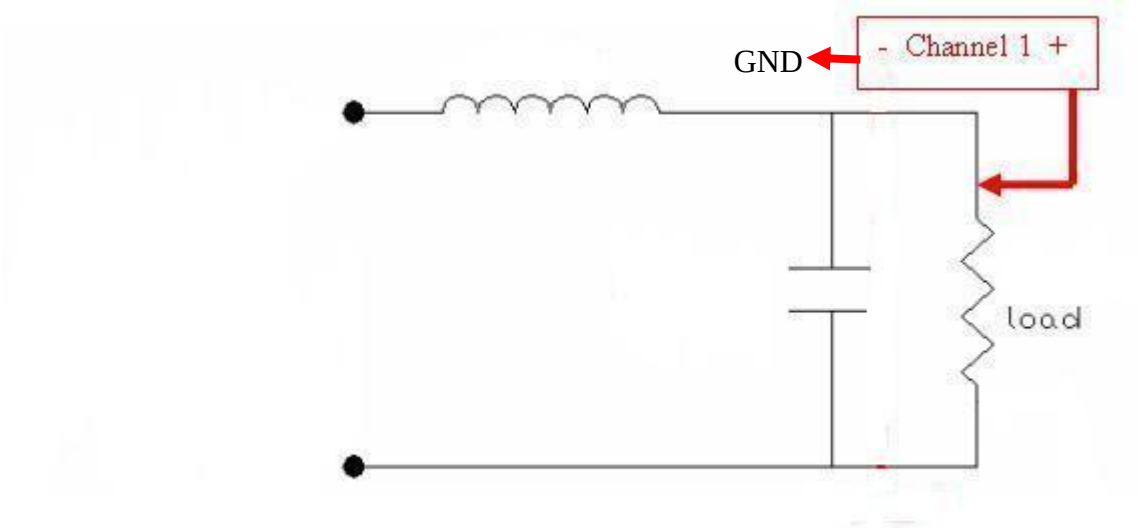

Figure 4.6: Low-Pass Filter Test Setup

4.3 Test Certification – Hardware

4.3.1 Sinusoidal PWM Inverter Control Circuit

The outputs of the sinusoidal PWM inverter control circuit are shown in Figure 4.7. The control circuit is expected to output two pulses with varying duty cycles that are 180º out of phase with a 20 kHz switching frequency. The oscilloscope probes were used in making the measurements. The results are very close to the expected values, which it produce 5V (peak-to-peak) and duty cycle 26.83%.

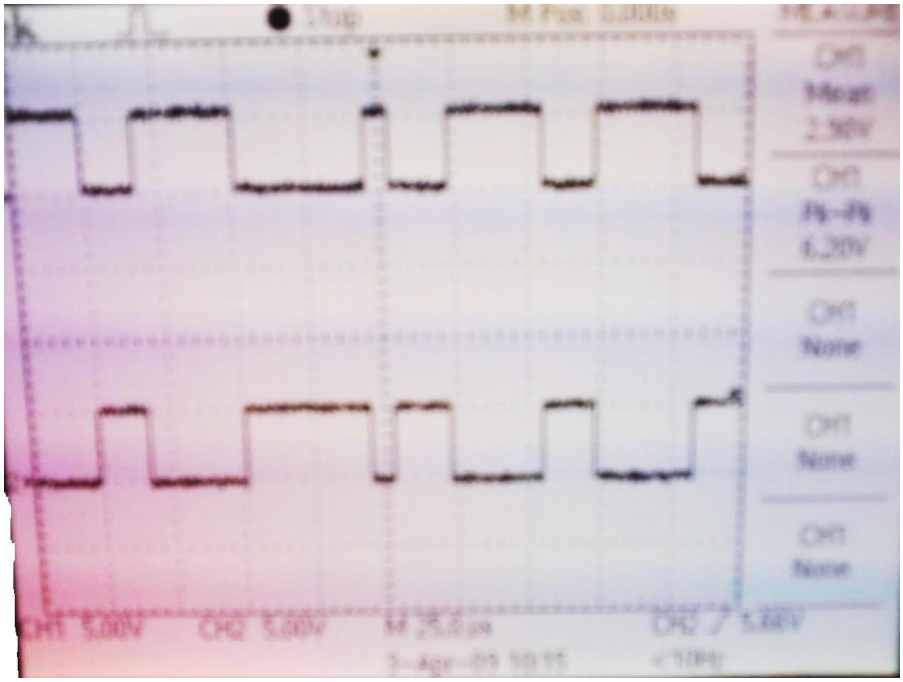

Figure 4.7: Sinusoidal PWM Inverter Control Circuit Pulses

4.3.2 The FET Drive Circuit

The outputs of the FET drive circuit are shown in Figure 4.8. The control circuit is expected to output two pulses with varying duty cycles that are 180º out of phase with a 20 kHz switching frequency. The oscilloscope probes were used in making the measurements. The results are very close to the expected values, which it produce 12V (peak-to-peak) and duty cycle 26.83%.

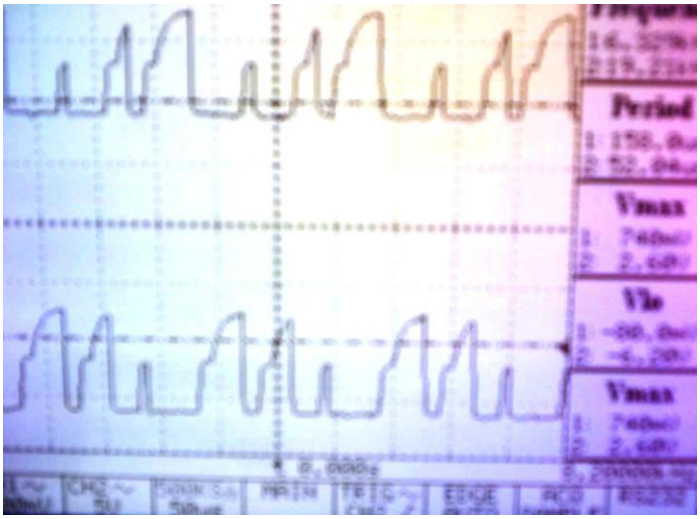

Figure 4.8: FET Drive Circuit Pulses

4.3.3 Low Pass Filter

Figure 4.9 illustrates the filtered version of the final power inverter output. The expected output after the low pass filter is a 240 VAC (peak-to-peak). The voltage amplitude is 245 VAC using the oscilloscope probes, which is at a desirable level. By closer examination, excessive voltage spikes are present and the waveform has much distortion. This shows that with properly matched filter components a low-pass filter will function properly.

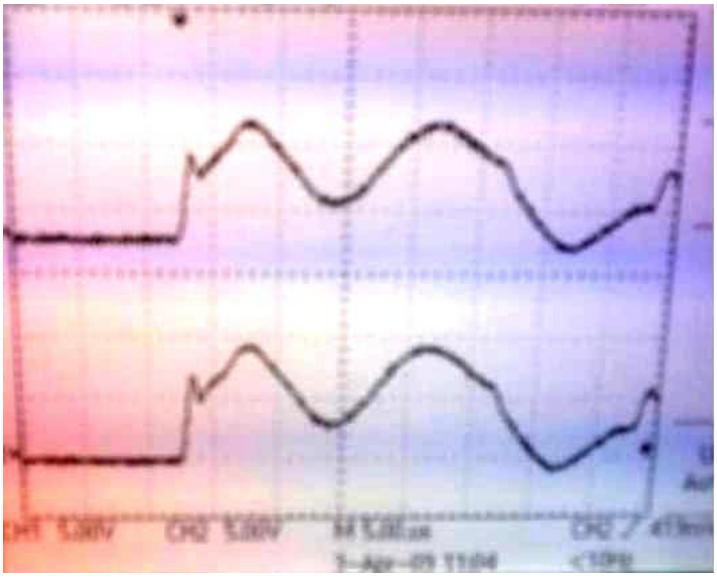

Figure 4.9: Filtered Low-Pass Filter Voltage Output Waveform

4.4 Test Certification – Simulation

The DC/AC power inverter was simulated in the PSIM environment. The entire project, the full-bridge sinusoidal PWM control circuit, was simulated using ideal parts in PSIM. The complexity of the PWM circuits was such that they could not be simulated effectively or exactly implemented using the available parts in PSIM. The test procedures written in the test specification section of this document were followed step by step in order to ensure that the power inverter worked according to theory. The major circuits tested in PSIM were the DC/AC inverter, which are discussed below.

4.4.1 DC/AC Inverter

Figure 4.10 shows the PSIM schematic that was used to simulate the output of the DC/AC inverter. The expected output of the DC/AC inverter is a 240 VAC, 50 Hz sine wave. Figure 4.11 shows the unfiltered 240 VAC (peak-to-peak) waveform that will be filtered to create the expected output. Figure 4.12 shows the filtered output and proves that DC/AC inverter should function properly. Figure 4.13 is an added simulation test result showing that only the 50 Hz fundamental frequency remains after filtering with a low-pass filter.

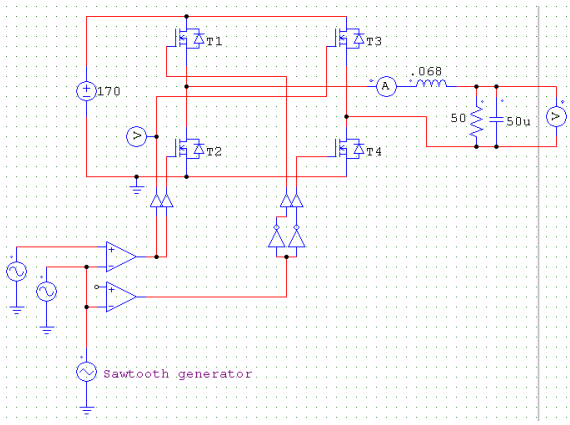

Figure 4.10: PSIM Schematic of DC/AC Inverter

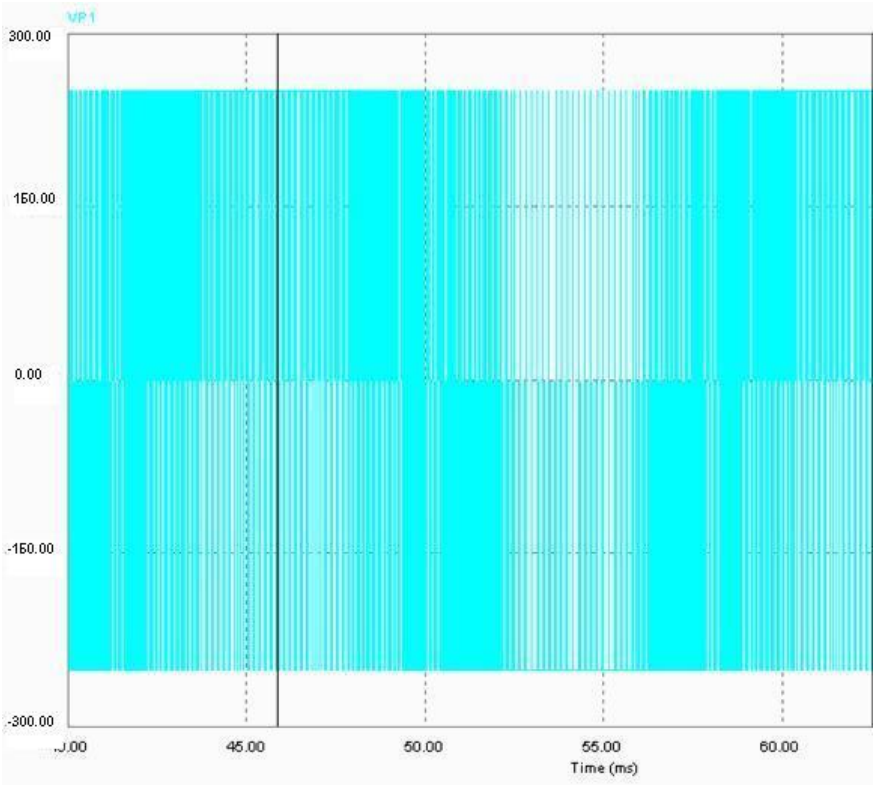

Figure 4.11: Simulation of Unfiltered DC/AC Inverter Output Voltage Waveform

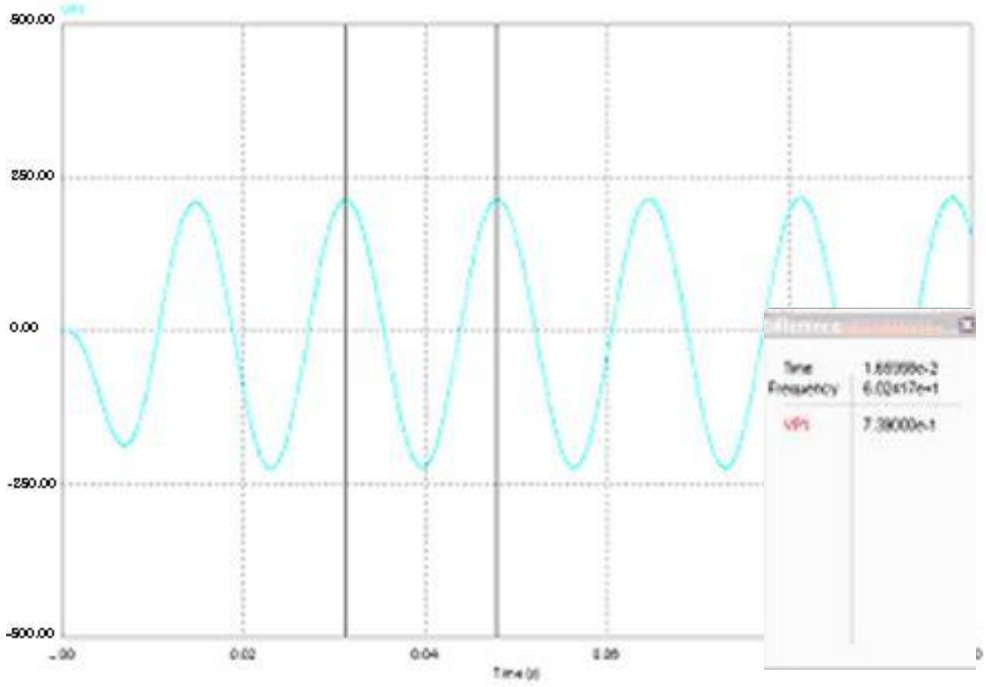

Figure 4.12: Simulation of Filtered DC/AC Inverter Output Voltage Waveform

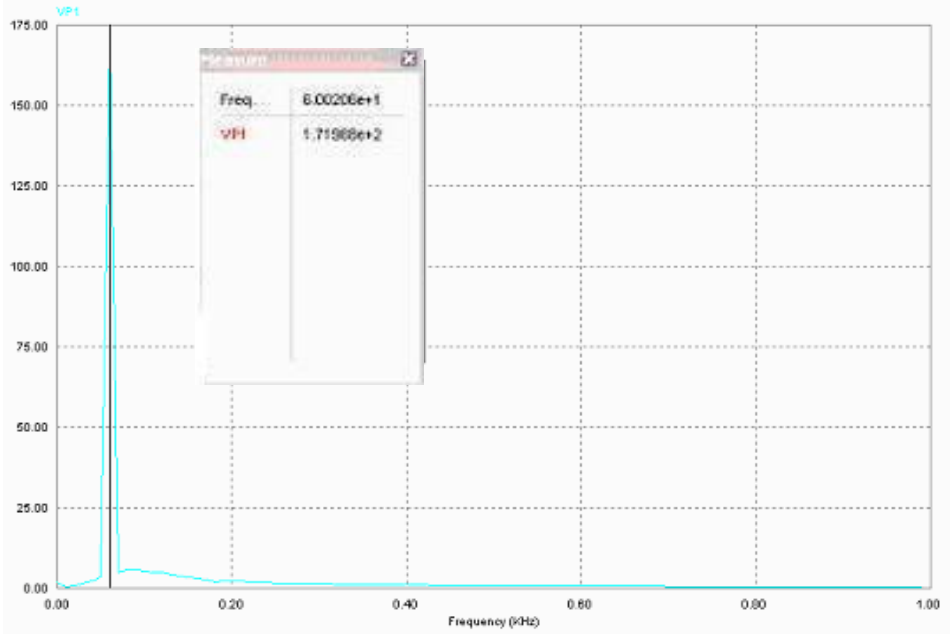

Figure 4.13: Simulation of Filtered DC/AC Inverter Frequency Spectrum

CHAPTER 5

CONCLUSION AND RECOMMEDATIONS

5.1 Conclusion

The goals for this project were to produce a pure sine wave DC/AC inverter that would output at 50 Hz, 230 VAC. The DC/AC inverter circuit will use a microprocessor to digitally pulse the transistors. This will allow it to produce a pure sine wave output.

In looking at how efficient this project is, there is no hard data that can be referred to as not enough time was available to collect it. In looking at the components selected and the simulations created before the actual construction of the inverter, everything was built in mind for the purpose of efficiency and keeping power losses to a minimum.

5.2 Recommendation

This project has successfully demonstrated a convert 12VDC to 230VAC. Future work on this project may include:

- PWM program that was used by microcontroller to digitally pulse MOSFETS of the full bridge inverter could be modified to more efficiently operate.

- Better layout the PCB. Some of the traces for the MOSFETS were longer than the others. This would lead to longer transit times and could be the cause of some of the voltage “spikes” that are present in output waveform.

- Add LCD for display the input and output voltage. By using ADC to convert any required readings to 0-5V DC (using the 5V as a reference). The microcontroller will receive input from the ADC and after convert it, it will sent to LCD for display the input and output voltage.

- Add alarm and auto shutdown program when the car battery is weak. By using LM399N (voltage comparator), it will compare the current voltage input and 12VDC as reference. When the inputs at 10.5VDC the alarm will be ON indicate the battery is weak. When the inputs at 10VDC the power inverter will automatically OFF.

- Introduce a closed loop monitoring system. This system would look at the output of the inverter and check to ensure that this is the correct output, if this output is not what it should be then this system has the power to go back and adjust the settings in the control circuit so that the output is the desired 230 VAC sine wave. A simple diagram shown below demonstrates the basic idea of a closed loop control system. The output would be scaled and compared to an ideal output reference, perhaps the sine wave reference in the microcontroller (control circuit), so that the change in voltage output can be accounted for. When this change is detected the amplification factor of the non-inverting amplifier for the sine wave reference could be adjusted thereby changing the PWM signal and effectively adjusting the output.

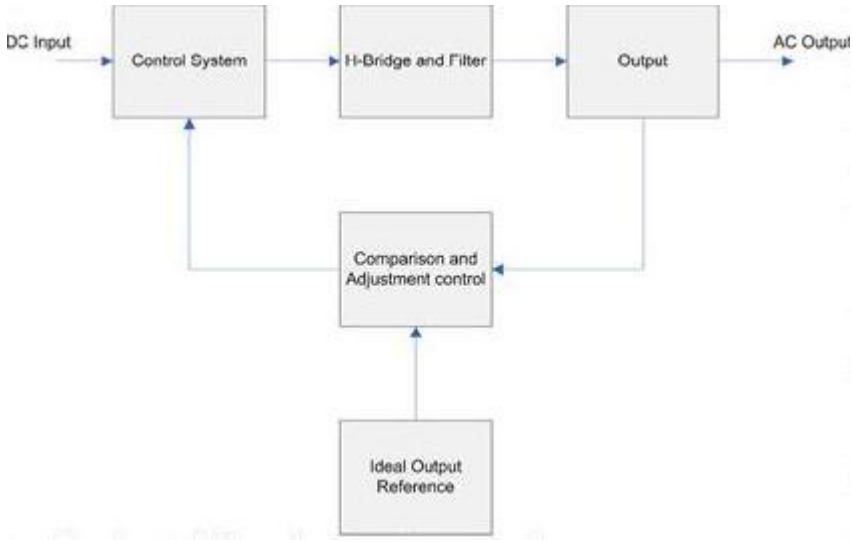

Figure 5.1: Closed Loop Flow Chart

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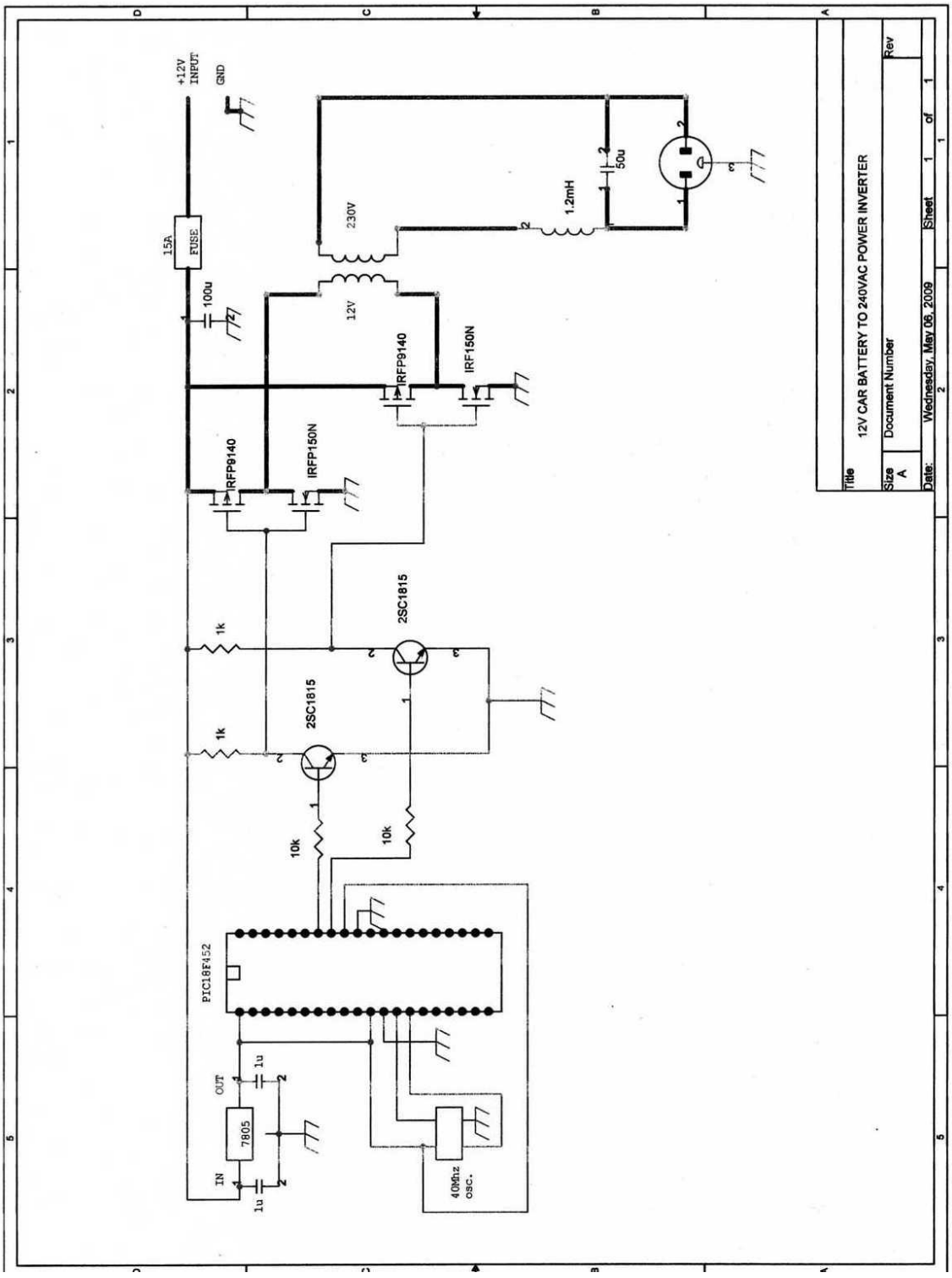
APPENDIX A

Power Inverter Schematic


+12V INPUT
GND
15A FUSE
100u
12V
230V
1.2mH
50u
IRFP9140
IRF150N
IRFP9140
IRFP150N
2SC1815
2SC1815
1k
1k
10k
10k
PIC18F452
OUT
IN
7805
1u
1u
40Mhz osc.
12V CAR BATTERY TO 240VAC POWER INVERTER
Document Number
Rev
Size A
Date: Wednesday, May 06, 2009
Sheet 1 of 1

APPENDIX B

Power Inverter Code Listings

```
;Power Inverter Group
;PWM Program


        list p=18c452, n=48, t=ON, st=OFF
        #include "p18c452.inc"

ScratchPadRam EQU     0x20

count1          EQU     ScratchPadRam+0
count2          EQU     ScratchPadRam+1
count2a         EQU     ScratchPadRam+11
count3          EQU     ScratchPadRam+2
count4          EQU     ScratchPadRam+3
DUTYA           EQU     ScratchPadRam+4
DUTYB           EQU     ScratchPadRam+5
DUTYC           EQU     ScratchPadRam+6
check           EQU     ScratchPadRam+7
TBLPTR          EQU     ScratchPadRam+8
TABLADDR        EQU     0x0003000
TABL1           EQU     0x0004000
TABL2           EQU     0x0005000
TABL3           EQU     0x0006000
four            EQU     ScratchPadRam+9
DCDUTY          EQU     ScratchPadRam+10


        org     0x000000
        bra     START
        org H'50'

START
        CLRF    check
        CLRF    TRISA

        clrf    PORTB
        clrf    DDRB

        movlw   0x04
        movwf   four

INFIN

        CLRF    count1
        CLRF    count2
        CLRF    count2a
        CLRF    count3
        CLRF    count4


        movlw   0x3C
        movwf   count1
LOOP1

        INCF    check


        movlw   UPPER(TABLADDR)
        movwf   TBLPTRU
        movlw   HIGH(TABLADDR)
        movwf   TBLPTRH
        movlw   LOW(TABLADDR)
        movwf   TBLPTRL
```

```
        movlw   0x00
        movwf   DUTYA
        movlw   0x00
        movwf   DUTYB
        movlw   0x00
        movwf   DUTYC

        movlw   0x4A
        movwf   count2
LOOP2

        bcf     PORTB,1
        bcf     PORTB,3
        bcf     PORTB,5
        bsf     PORTB,0
        bsf     PORTB,2
        bsf     PORTB,4

        tblrd*+
        movff   TABLAT,DUTYA

        movlw   0x00
        movwf   count3
LOOP3

        bsf     PORTB,6
        movlw   0x00

        ADDWF   count3,0
        CPFSEQ  DUTYA
        GOTO    NEXT1
        bcf     PORTB,0
        bsf     PORTB,1
NEXT1

        CPFSEQ  DUTYB
        GOTO    NEXT2
        bcf     PORTB,2
        bsf     PORTB,3
NEXT2

        CPFSEQ  DUTYC
        GOTO    NEXT3
        bcf     PORTB,4
        bsf     PORTB,5
NEXT3

        movlw   0x00
        ADDWF   count3,0
        ADDWF   four,0
        movwf   count3
        movlw   0x64
        CPFSEQ  count3
        GOTO    LOOP3

        DECFSZ  count2
```

```
        GOTO    LOOP2


        movlw   UPPER(TABL1)
        movwf   TBLPTRU
        movlw   HIGH(TABL1)
        movwf   TBLPTRH
        movlw   LOW(TABL1)
        movwf   TBLPTRL

        movlw   0x4A
        movwf   count2

LOOP2A

        bcf     PORTB,1
        bcf     PORTB,3
        bcf     PORTB,5
        bsf     PORTB,0
        bsf     PORTB,2
        bsf     PORTB,4

        tblrd*+
        movff   TABLAT,DUTYA


        movlw   0x00
        movwf   count3

LOOP3A

        bsf     PORTB,6
        movlw   0x00

        ADDWF   count3,0
        CPFSEQ  DUTYA
        GOTO    NEXT1A
        bcf     PORTB,0
        bsf     PORTB,1
NEXT1A

        CPFSEQ  DUTYB
        GOTO    NEXT2A
        bcf     PORTB,2
        bsf     PORTB,3
NEXT2A

        CPFSEQ  DUTYC
        GOTO    NEXT3A
        bcf     PORTB,4
        bsf     PORTB,5
NEXT3A

        movlw   0x00
        ADDWF   count3,0
        ADDWF   four,0
        movwf   count3
        movlw   0x64
        CPFSEQ  count3
        GOTO    LOOP3A

        DECFSZ  count2
        GOTO    LOOP2A
```

```
        movlw   UPPER(TABL2)
        movwf   TBLPTRU
        movlw   HIGH(TABL2)
        movwf   TBLPTRH
        movlw   LOW(TABL2)
        movwf   TBLPTRL


        movlw   0x4C
        movwf   count2

LOOP2B

        bcf     PORTB,1
        bcf     PORTB,3
        bcf     PORTB,5
        bsf     PORTB,0
        bsf     PORTB,2
        bsf     PORTB,4

        tblrd*+
        movff   TABLAT,DUTYA

        movlw   0x00
        movwf   count3

LOOP3B

        bsf     PORTB,6
        movlw   0x00

        ADDWF   count3,0
        CPFSEQ  DUTYA
        GOTO    NEXT1B
        bcf     PORTB,0
        bsf     PORTB,1
NEXT1B

        CPFSEQ  DUTYB
        GOTO    NEXT2B
        bcf     PORTB,2
        bsf     PORTB,3
NEXT2B

        CPFSEQ  DUTYC
        GOTO    NEXT3B
        bcf     PORTB,4
        bsf     PORTB,5
NEXT3B

        movlw   0x00
        ADDWF   count3,0
        ADDWF   four,0
        movwf   count3
        movlw   0x64
        CPFSEQ  count3
        GOTO    LOOP3B

        DECFSZ  count2
        GOTO    LOOP2B


        movlw   UPPER(TABL3)
```

```
        movwf   TBLPTRU
        movlw   HIGH(TABL3)
        movwf   TBLPTRH
        movlw   LOW(TABL3)
        movwf   TBLPTRL

        movlw   0x49
        movwf   count2

LOOP2C

        bcf     PORTB,1
        bcf     PORTB,3
        bcf     PORTB,5
        bsf     PORTB,0
        bsf     PORTB,2
        bsf     PORTB,4

        tblrd*+
        movff   TABLAT,DUTYA

        movlw   0x00
        movwf   count3

LOOP3C

        bsf     PORTB,6
        movlw   0x00

        ADDWF   count3,0
        CPFSEQ  DUTYA
        GOTO    NEXT1C
        bcf     PORTB,0
        bsf     PORTB,1
NEXT1C

        CPFSEQ  DUTYB
        GOTO    NEXT2C
        bcf     PORTB,2
        bsf     PORTB,3
NEXT2C

        CPFSEQ  DUTYC
        GOTO    NEXT3C
        bcf     PORTB,4
        bsf     PORTB,5
NEXT3C

        movlw   0x00
        ADDWF   count3,0
        ADDWF   four,0
        movwf   count3
        movlw   0x64
        CPFSEQ  count3
        GOTO    LOOP3C

        DECFSZ  count2
        GOTO    LOOP2C

        DECFSZ  count1
        GOTO    LOOP1


        org     TABLADDR
```

```
        DATA    0x1434,0x3450,0x5014,0x1434,0x3450,0x5014,0x1434,0x3850
        DATA    0x5010,0x1038,0x384C,0x4C10,0x1038,0x384C,0x4C10,0x1038
        DATA    0x3C4C,0x4C10,0x103C,0x3C4C,0x4C10,0x103C,0x3C48,0x4810
        DATA    0x1040,0x4048,0x4810,0x1040,0x4048,0x4810,0x1040,0x4048
        DATA    0x4410,0x1044,0x4444,0x4410,0x1044,0x4444,0x4410,0x1044
        DATA    0x4444,0x4010,0x1048,0x4840,0x4010,0x1048,0x4840,0x4010
        DATA    0x1048,0x4840,0x3C10,0x1048,0x4C3C,0x3C10,0x104C,0x4C3C
        DATA    0x3C10,0x104C,0x4C3C,0x3810,0x104C,0x4C38,0x3810,0x104C
        DATA    0x5038,0x3810,0x1050,0x5034,0x3414,0x1450,0x5034,0x3414
        DATA    0x1450,0x5034,0x3014,0x1450,0x5030,0x3014,0x1450,0x5030
        DATA    0x3014,0x1454,0x5430,0x2C14,0x1854,0x542C,0x2C18,0x1854
        DATA    0x542C,0x2C18,0x1854,0x5428,0x2818,0x1854,0x5428,0x2818
        DATA    0x1C54,0x5428,0x281C,0x1C54,0x5424,0x241C,0x1C54,0x5424
        DATA    0x241C,0x1C54,0x5424,0x2420,0x2054,0x5420,0x2020

TABAEND


        org     TABL1

        DATA    0x2054,0x5420,0x2020,0x2054,0x5420,0x2024,0x2454,0x541C
        DATA    0x1C24,0x2454,0x541C,0x1C24,0x2454,0x541C,0x1C28,0x2854
        DATA    0x541C,0x1828,0x2854,0x5418,0x1828,0x2C54,0x5418,0x182C
        DATA    0x2C54,0x5418,0x182C,0x2C54,0x5418,0x142C,0x3050,0x5014
        DATA    0x1430,0x3050,0x5014,0x1430,0x3050,0x5014,0x1434,0x3450
        DATA    0x5014,0x1434,0x3450,0x5014,0x1434,0x3850,0x4C10,0x1038
        DATA    0x384C,0x4C10,0x1038,0x384C,0x4C10,0x1038,0x3C4C,0x4C10
        DATA    0x103C,0x3C4C,0x4810,0x103C,0x3C48,0x4810,0x1040,0x4048
        DATA    0x4810,0x1040,0x4048,0x4810,0x1040,0x4044,0x4410,0x1044
        DATA    0x4444,0x4410,0x1044,0x4444,0x4410,0x1044,0x4440,0x4010
        DATA    0x1048,0x4840,0x4010,0x1048,0x4840,0x4010,0x1048,0x483C
        DATA    0x3C10,0x1048,0x4C3C,0x3C10,0x104C,0x4C3C,0x3C10,0x104C
        DATA    0x4C38,0x3810,0x104C,0x4C38,0x3810,0x104C,0x5038,0x3410
        DATA    0x1050,0x5034,0x3414,0x1450,0x5034,0x3414,0x1450

TAB1END

END
```

APPENDIX C

Datasheets

MICROCHIP

PIC18FXX2

28/40-pin High Performance, Enhanced FLASH Microcontrollers with 10-Bit A/D

High Performance RISC CPU:

- C compiler optimized architecture/instruction set
  - Source code compatible with the PIC16 and PIC17 instruction sets
- Linear program memory addressing to 32 Kbytes
- Linear data memory addressing to 1.5 Kbytes

Device	On-Chip Program Memory		On-Chip RAM (bytes)	Data EEPROM (bytes)
	FLASH (bytes)	# Single Word Instructions		
PIC18F242	16K	8192	768	256
PIC18F252	32K	16384	1536	256
PIC18F442	16K	8192	768	256
PIC18F452	32K	16384	1536	256

- Up to 10 MIPs operation:
  - DC - 40 MHz osc./clock input
  - 4 MHz - 10 MHz osc./clock input with PLL active
- 16-bit wide instructions, 8-bit wide data path
- Priority levels for interrupts
- 8 x 8 Single Cycle Hardware Multiplier

Peripheral Features:

- High current sink/source 25 mA/25 mA
- Three external interrupt pins
- Timer0 module: 8-bit/16-bit timer/counter with 8-bit programmable prescaler
- Timer1 module: 16-bit timer/counter
- Timer2 module: 8-bit timer/counter with 8-bit period register (time-base for PWM)
- Timer3 module: 16-bit timer/counter
- Secondary oscillator clock option - Timer1/Timer3
- Two Capture/Compare/PWM (CCP) modules. CCP pins that can be configured as:
  - Capture input: capture is 16-bit, max. resolution 6.25 ns (TCY/16)
  - Compare is 16-bit, max. resolution 100 ns (TCY)
  - PWM output: PWM resolution is 1- to 10-bit, max. PWM freq. @: 8-bit resolution = 156 kHz, 10-bit resolution = 39 kHz
- Master Synchronous Serial Port (MSSP) module, Two modes of operation:
  - 3-wire SPI™ (supports all 4 SPI modes)
  - I^2C™ Master and Slave mode

Peripheral Features (Continued):

- Addressable USART module:
  - Supports RS-485 and RS-232
- Parallel Slave Port (PSP) module

Analog Features:

- Compatible 10-bit Analog-to-Digital Converter module (A/D) with:
  - Fast sampling rate
  - Conversion available during SLEEP
  - Linearity ≤ 1 LSb
- Programmable Low Voltage Detection (PLVD)
  - Supports interrupt on-Low Voltage Detection
- Programmable Brown-out Reset (BOR)

Special Microcontroller Features:

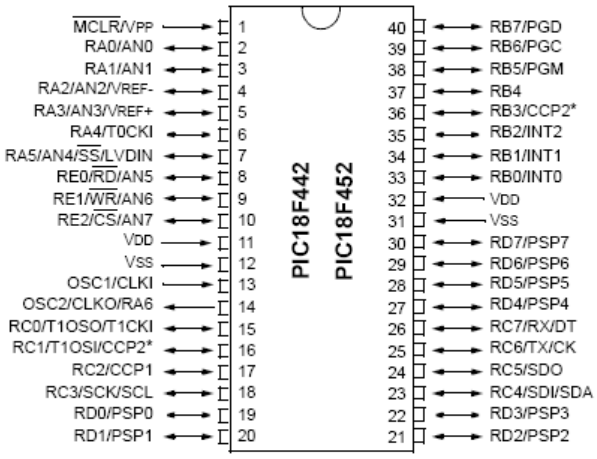
- 100,000 erase/write cycle Enhanced FLASH program memory typical
- 1,000,000 erase/write cycle Data EEPROM memory
- FLASH/Data EEPROM Retention: > 40 years
- Self-reprogrammable under software control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own On-Chip RC Oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options including:
  - 4X Phase Lock Loop (of primary oscillator)
  - Secondary Oscillator (32 kHz) clock input
- Single supply 5V In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via two pins

CMOS Technology:

- Low power, high speed FLASH/EEPROM technology
- Fully static design
- Wide operating voltage range (2.0V to 5.5V)
- Industrial and Extended temperature ranges
- Low power consumption:
  - < 1.6 mA typical @ 5V, 4 MHz
  - 25 µA typical @ 3V, 32 kHz
  - < 0.2 µA typical standby current

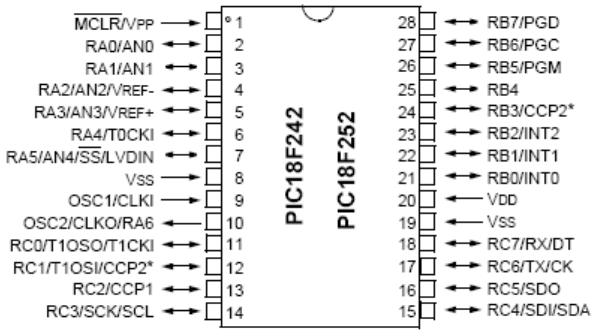
Pin Diagrams (Cont.'d)

DIP



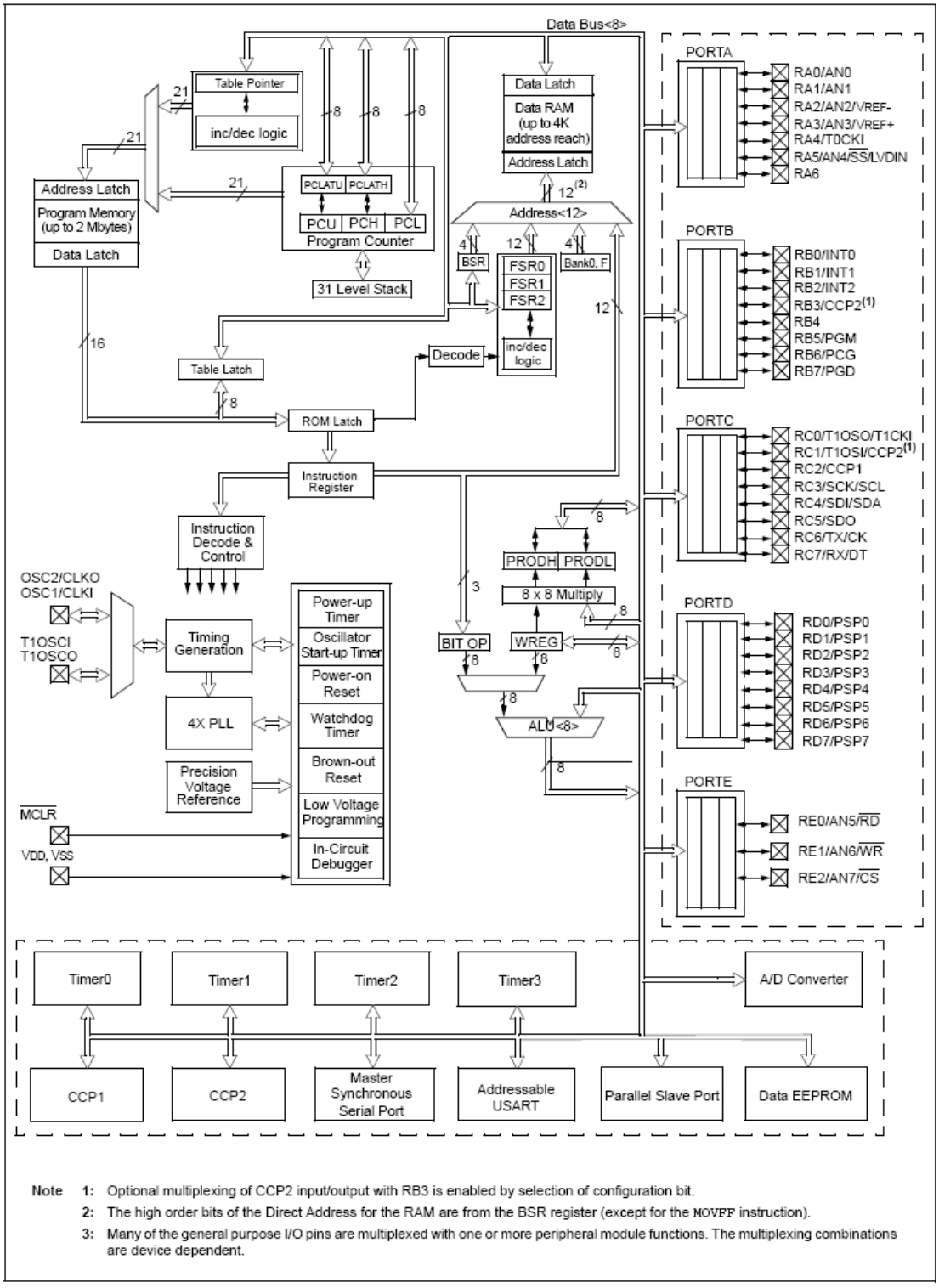
Note: Pin compatible with 40-pin PIC16C7X devices.

DIP, SOIC



* RB3 is the alternate pin for the CCP2 pin multiplexing.

FIGURE 1-2: PIC18F4X2 BLOCK DIAGRAM



Note 1: Optional multiplexing of CCP2 input/output with RB3 is enabled by selection of configuration bit.

2: The high order bits of the Direct Address for the RAM are from the BSR register (except for the MOVFF instruction).

3: Many of the general purpose I/O pins are multiplexed with one or more peripheral module functions. The multiplexing combinations are device dependent.

TOSHIBA 2SC1815

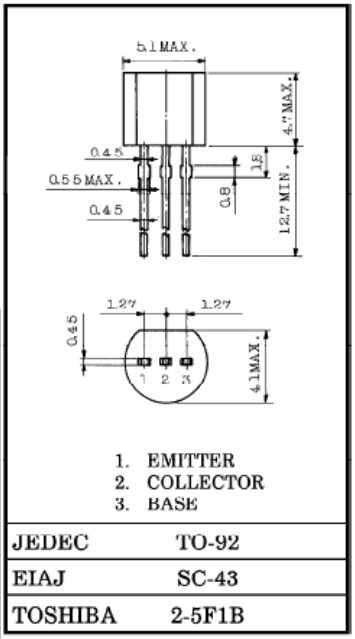
TOSHIBA TRANSISTOR SILICON NPN EPITAXIAL TYPE (PCT PROCESS)

2SC1815

AUDIO FREQUENCY GENERAL PURPOSE AMPLIFIER APPLICATIONS.
DRIVER STAGE AMPLIFIER APPLICATIONS.

- High Voltage and High Current
  : V_{CEO} = 50V (Min.), I_C = 150mA (Max.)
- Excellent h_{FE} Linearity
  : $h_{FE(2)}$ = 100 (Typ.) at V_{CE} = 6V, I_C = 150mA
  : h_{FE} (I_C = 0.1mA) / h_{FE} (I_C = 2mA) = 0.95 (Typ.)
- Low Noise : NF = 1dB (Typ.) at f = 1kHz
- Complementary to 2SA1015 (O, Y, GR class)

Unit in mm



1. EMITTER
2. COLLECTOR
3. BASE

JEDEC	TO-92
EIAJ	SC-43
TOSHIBA	2-5F1B

Weight : 0.21g

MAXIMUM RATINGS (Ta = 25°C)

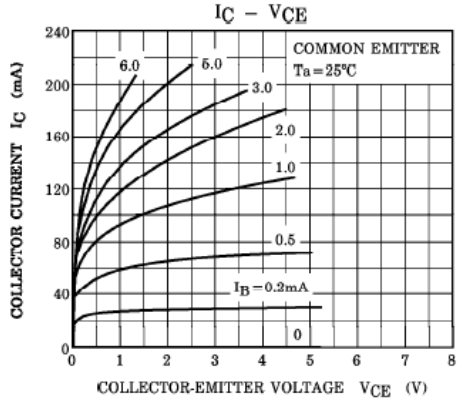
CHARACTERISTIC	SYMBOL	RATING	UNIT
Collector-Base Voltage	V_{CBO}	60	V
Collector-Emitter Voltage	V_{CEO}	50	V
Emitter-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	150	mA
Base Current	I_B	50	mA
Collector Power Dissipation	P_C	400	mW
Junction Temperature	T_j	125	°C
Storage Temperature Range	T_{stg}	−55~125	°C

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

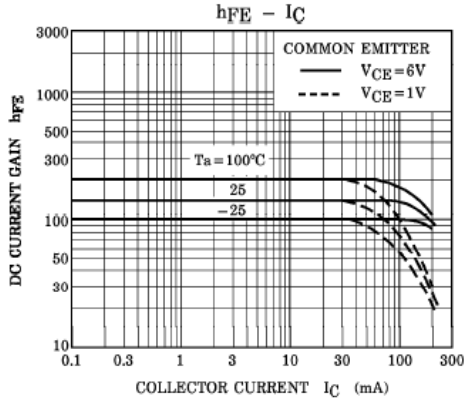
CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Collector Cut-off Current	I_{CBO}	V_{CB} = 60V, I_E = 0	—	—	0.1	μA
Emitter Cut-off Current	I_{EBO}	V_{EB} = 5V, I_C = 0	—	—	0.1	μA
DC Current Gain	$h_{FE(1)}$ (Note)	V_{CE} = 6V, I_C = 2mA	70	—	700	
	$h_{FE(2)}$	V_{CE} = 6V, I_C = 150mA	25	100	—	
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 100mA, I_B = 10mA	—	0.1	0.25	V
Base-Emitter Saturation Voltage	$V_{BE(sat)}$	I_C = 100mA, I_B = 10mA	—	—	1.0	V
Transition Frequency	f_T	V_{CE} = 10V, I_C = 1mA	80	—		MHz
Collector Ouput Capacitance	C_{ob}	V_{CB} = 10V, I_E = 0, f = 1MHz	—	2.0	3.5	pF
Base Intrinsic Resistance	$r_{bb'}$	V_{CE} = 10V, I_E = −1mA f = 30MHz	—	50	—	Ω
Noise Figure	NF	V_{CE} = 6V, I_C = 0.1mA f = 1kHz, R_G = 10kΩ	—	1.0	10	dB

Note : h_{FE} Classification O : 70~140 Y : 120~240 GR : 200~400 BL : 350~700

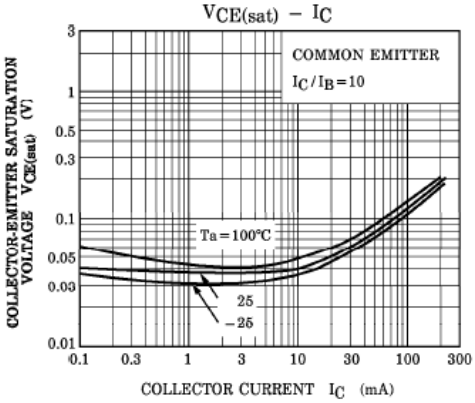
$I_C - V_{CE}$



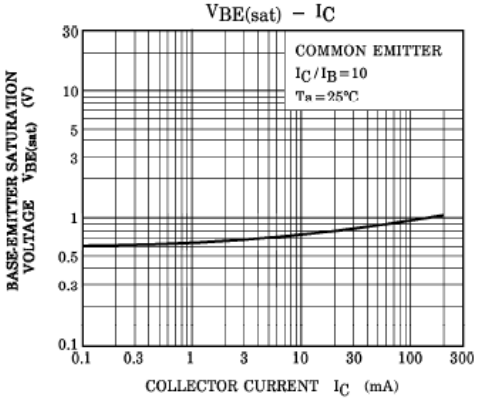
$h_{FE} - I_C$



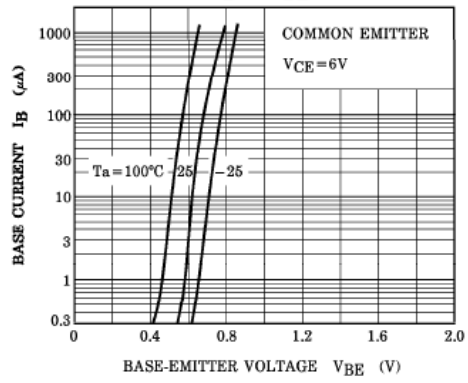
$V_{CE(sat)} - I_C$



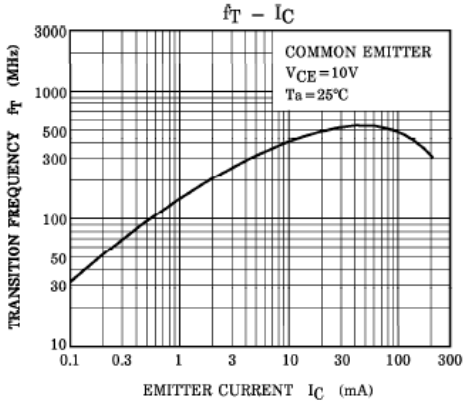
$V_{BE(sat)} - I_C$



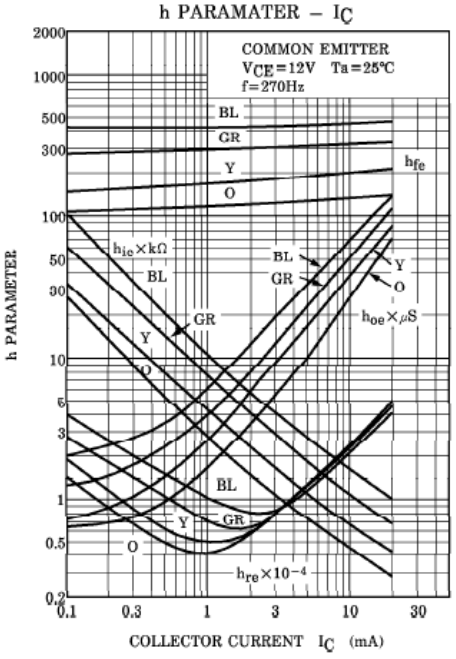
$I_B - V_{BE}$



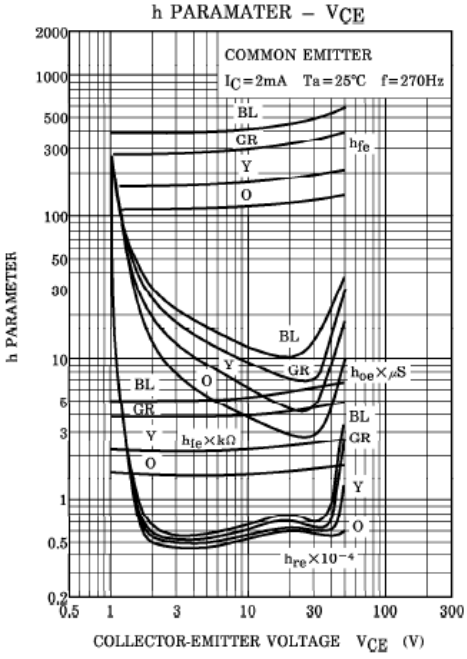
$f_T - I_C$



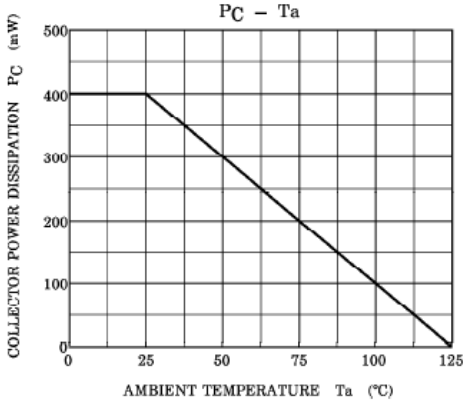
h PARAMATER – I_C



h PARAMATER – V_{CE}



P_C – Ta



International
IOR Rectifier

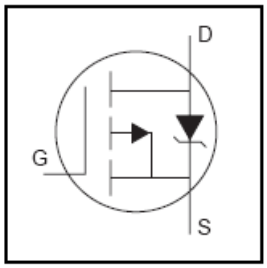
PD - 9.1492A

PRELIMINARY

IRFP9140N

HEXFET® Power MOSFET

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- P-Channel
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = -100V

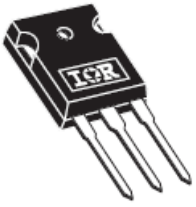
$R_{DS(on)}$ = 0.117Ω

I_D = -23A

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ -10V	-23	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ -10V	-16	
I_{DM}	Pulsed Drain Current ①⑤	-76	
P_D @T_C = 25°C	Power Dissipation	140	W
	Linear Derating Factor	0.91	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑤	430	mJ
I_{AR}	Avalanche Current①	-11	A
E_{AR}	Repetitive Avalanche Energy①	14	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	-5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-100	—	—	V	V_{GS} = 0V, I_D = -250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.11	—	V/°C	Reference to 25°C, I_D = -1mA⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.117	Ω	V_{GS} = -10V, I_D = -13A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250µA
g_{fs}	Forward Transconductance	5.3	—	—	S	V_{DS} = -50V, I_D = 11A⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	-25	µA	V_{DS} = -100V, V_{GS} = 0V
		—	—	-250		V_{DS} = -80V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	97	nC	I_D = -11A
Q_{gs}	Gate-to-Source Charge	—	—	15		V_{DS} = -80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	51		V_{GS} = -10V, See Fig. 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	V_{DD} = -50V
t_r	Rise Time	—	67	—		I_D = -11A
$t_{d(off)}$	Turn-Off Delay Time	—	51	—		R_G = 5.1Ω
t_f	Fall Time	—	51	—		R_D = 4.2Ω, See Fig. 10 ④⑤
L_D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	13	—		
C_{iss}	Input Capacitance	—	1300	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	400	—		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	—	240	—		f = 1.0MHz, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-23	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑤	—	—	-76		
V_{SD}	Diode Forward Voltage	—	—	-1.3	V	T_J = 25°C, I_S = -13A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	150	220	ns	T_J = 25°C, I_F = -11A
Q_{rr}	Reverse RecoveryCharge	—	830	1200	µC	di/dt = -100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 7.1mH R_G = 25Ω, I_{AS} = -11A. (See Figure 12)

③ I_{SD} ≤ -11A, di/dt ≤ -470A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ Uses IRF9540N data and test conditions

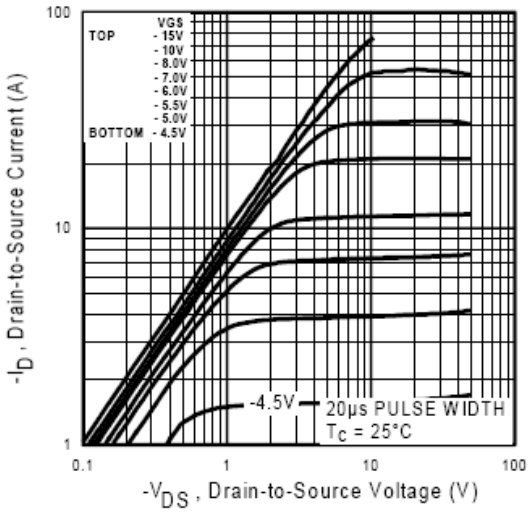


Fig 1. Typical Output Characteristics

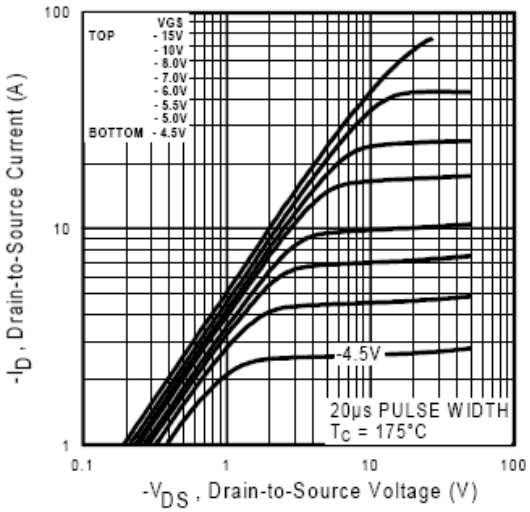


Fig 2. Typical Output Characteristics

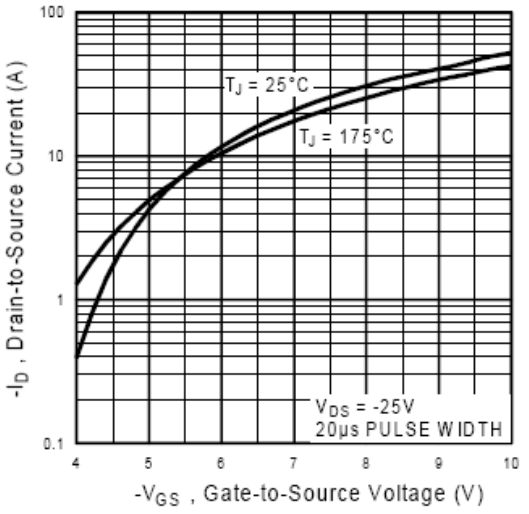


Fig 3. Typical Transfer Characteristics

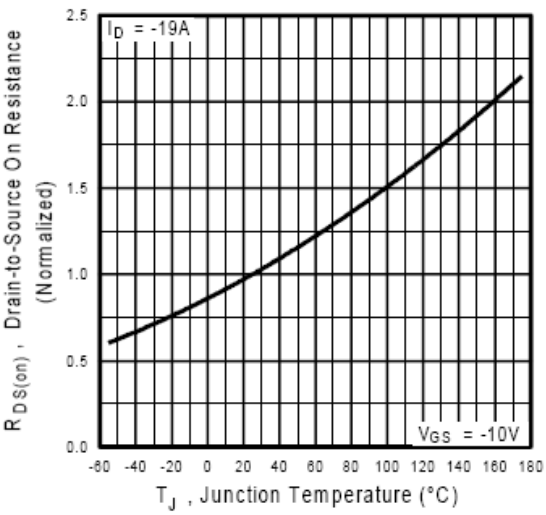


Fig 4. Normalized On-Resistance Vs. Temperature

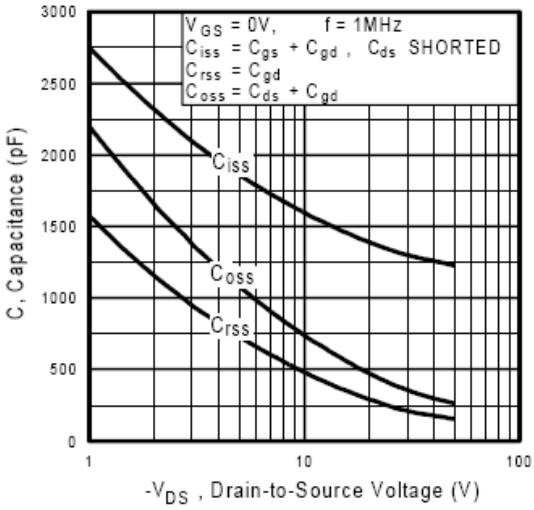


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

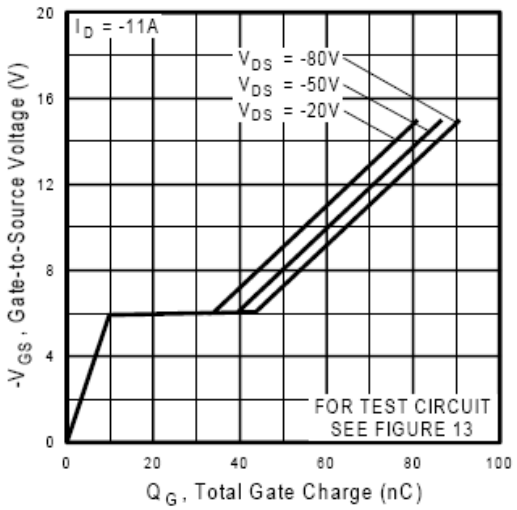


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

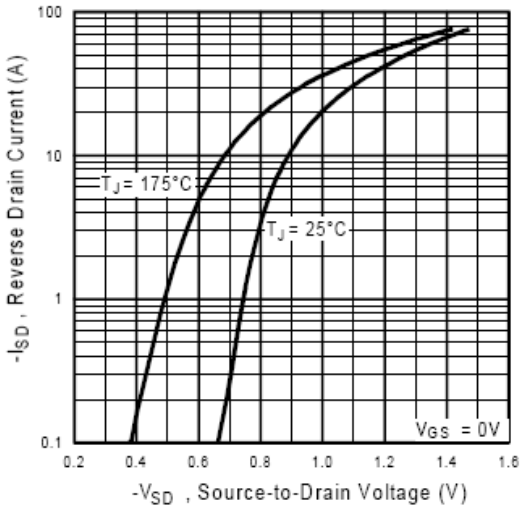


Fig 7. Typical Source-Drain Diode Forward Voltage

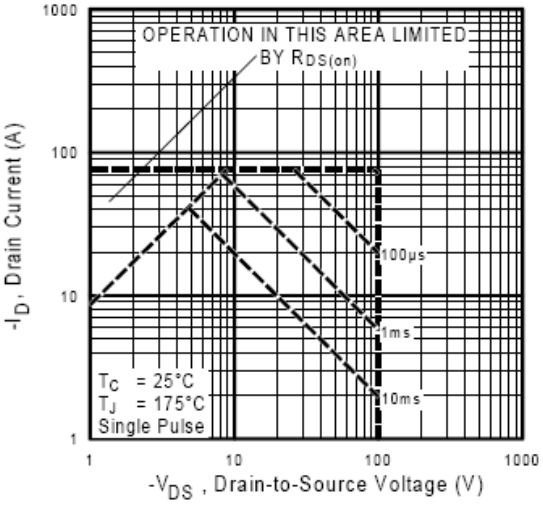


Fig 8. Maximum Safe Operating Area

International
IOR Rectifier

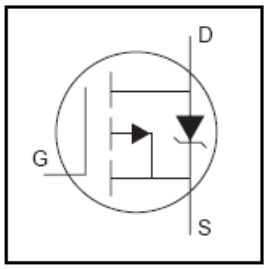
PD - 9.1492A

PRELIMINARY

IRFP9140N

HEXFET® Power MOSFET

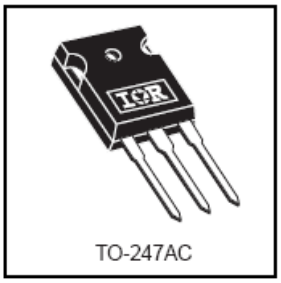
- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- P-Channel
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = -100V

$R_{DS(on)}$ = 0.117Ω

I_D = -23A



TO-247AC

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ -10V	-23	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ -10V	-16	
I_{DM}	Pulsed Drain Current ①⑤	-76	
P_D @T_C = 25°C	Power Dissipation	140	W
	Linear Derating Factor	0.91	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑤	430	mJ
I_{AR}	Avalanche Current①	-11	A
E_{AR}	Repetitive Avalanche Energy①	14	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	-5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-100	—	—	V	V_{GS} = 0V, I_D = -250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.11	—	V/°C	Reference to 25°C, I_D = -1mA⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.117	Ω	V_{GS} = -10V, I_D = -13A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
g_{fs}	Forward Transconductance	5.3	—	—	S	V_{DS} = -50V, I_D = 11A⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	V_{DS} = -100V, V_{GS} = 0V
		—	—	-250		V_{DS} = -80V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	97	nC	I_D = -11A
Q_{gs}	Gate-to-Source Charge	—	—	15		V_{DS} = -80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	51		V_{GS} = -10V, See Fig. 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	V_{DD} = -50V
t_r	Rise Time	—	67	—		I_D = -11A
$t_{d(off)}$	Turn-Off Delay Time	—	51	—		R_G = 5.1Ω
t_f	Fall Time	—	51	—		R_D = 4.2Ω, See Fig. 10 ④⑤
L_D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	13	—		
C_{iss}	Input Capacitance	—	1300	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	400	—		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	—	240	—		f = 1.0MHz, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-23	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑤	—	—	-76		
V_{SD}	Diode Forward Voltage	—	—	-1.3	V	T_J = 25°C, I_S = -13A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	150	220	ns	T_J = 25°C, I_F = -11A
Q_{rr}	Reverse RecoveryCharge	—	830	1200	μC	di/dt = -100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 7.1mH R_G = 25Ω, I_{AS} = -11A. (See Figure 12)

③ I_{SD} ≤ -11A, di/dt ≤ -470A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ Uses IRF9540N data and test conditions

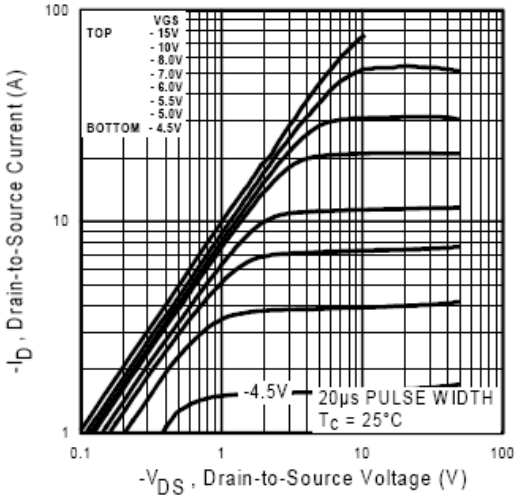


Fig 1. Typical Output Characteristics

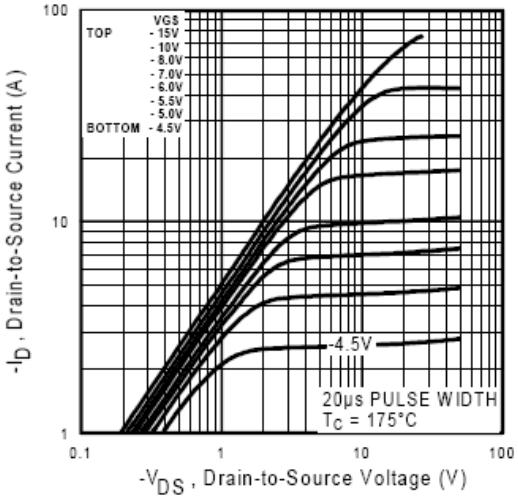


Fig 2. Typical Output Characteristics

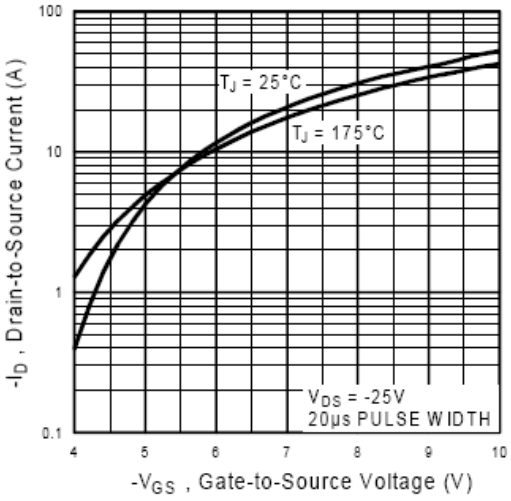


Fig 3. Typical Transfer Characteristics

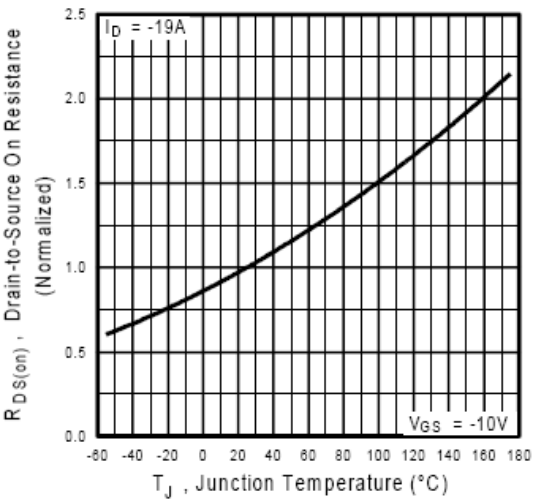


Fig 4. Normalized On-Resistance Vs. Temperature

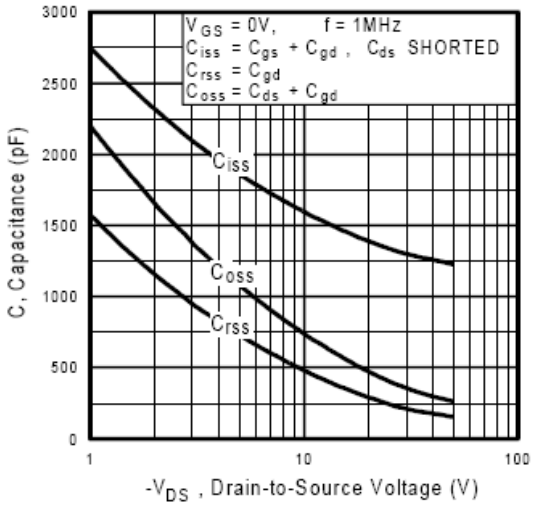


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

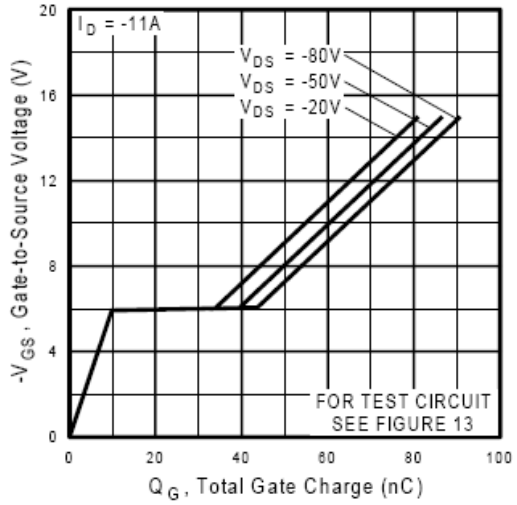


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

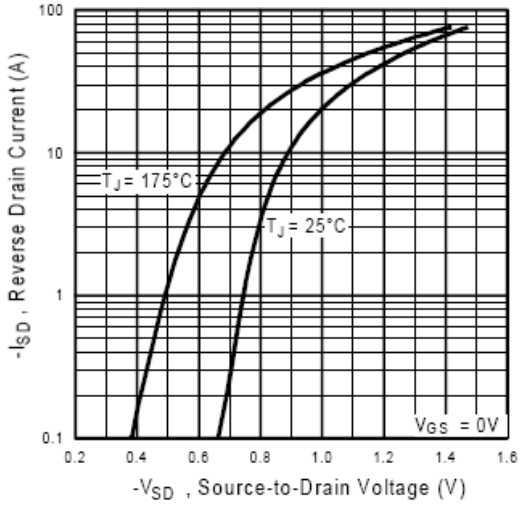


Fig 7. Typical Source-Drain Diode Forward Voltage

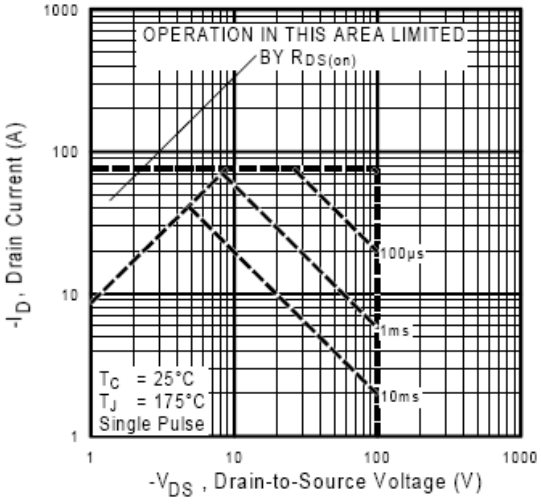


Fig 8. Maximum Safe Operating Area

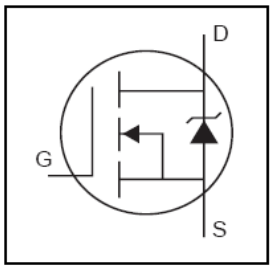
International
IOR Rectifier

PD - 91503D

IRFP150N

HEXFET® Power MOSFET

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 100V

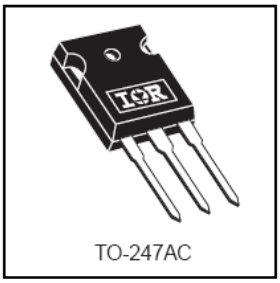
$R_{DS(on)}$ = 0.036Ω

I_D = 42A

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	42	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	30	
I_{DM}	Pulsed Drain Current ①⑤	140	
P_D @T_C = 25°C	Power Dissipation	160	W
	Linear Derating Factor	1.1	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑤	420	mJ
I_{AR}	Avalanche Current①⑤	22	A
E_{AR}	Repetitive Avalanche Energy①	16	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	----	0.95	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	----	
$R_{\theta JA}$	Junction-to-Ambient	----	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.11	——	V/°C	Reference to 25°C, I_D = 1mA⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.036	Ω	V_{GS} = 10V, I_D = 23A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	14	——	——	S	V_{DS} = 25V, I_D = 22A⑤
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	µA	V_{DS} = 100V, V_{GS} = 0V
		——	——	250		V_{DS} = 80V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
Q_g	Total Gate Charge	——	——	110	nC	I_D = 22A
Q_{gs}	Gate-to-Source Charge	——	——	15		V_{DS} = 80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	58		V_{GS} = 10V, See Fig. 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	——	11	——	ns	V_{DD} = 50V
t_r	Rise Time	——	56	——		I_D = 22A
$t_{d(off)}$	Turn-Off Delay Time	——	45	——		R_G = 3.6Ω
t_f	Fall Time	——	40	——		R_D = 2.9Ω See Fig. 10 ④⑤
L_D	Internal Drain Inductance	——	5.0	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	——	13	——		
C_{iss}	Input Capacitance	——	1900	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	450	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	230	——		f = 1.0MHz, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	42	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑤	——	——	140		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S =23A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	180	270	ns	T_J = 25°C, I_F = 22A
Q_{rr}	Reverse RecoveryCharge	——	1.2	1.8	µC	di/dt = 100A/µs ④ ⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 1.7mH R_G = 25Ω, I_{AS} = 22A. (See Figure 12)

③ I_{SD} ≤ 22A, di/dt ≤ 180A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ Uses IRF1310N data and test conditions.

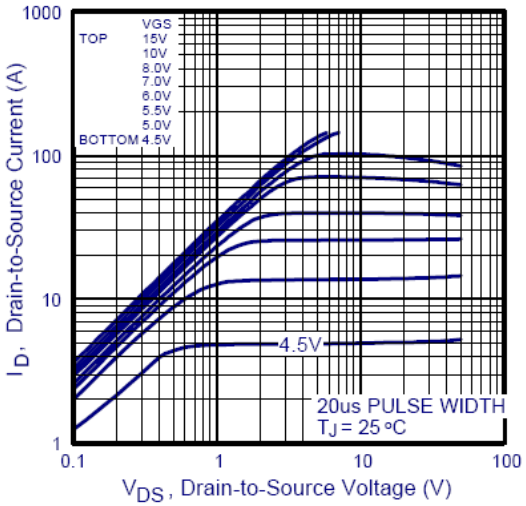


Fig 1. Typical Output Characteristics

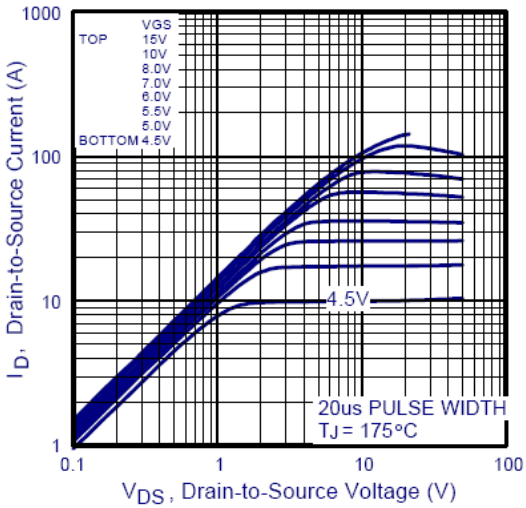


Fig 2. Typical Output Characteristics

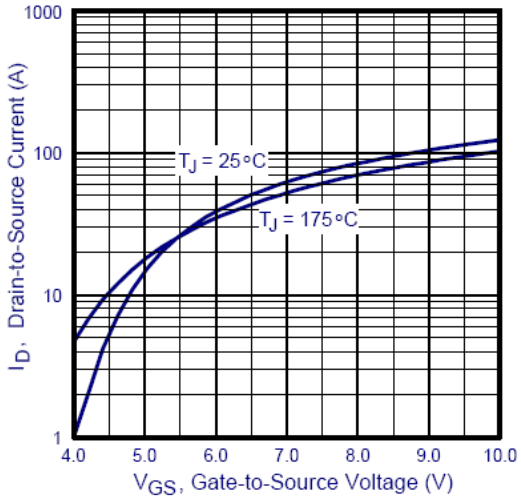


Fig 3. Typical Transfer Characteristics

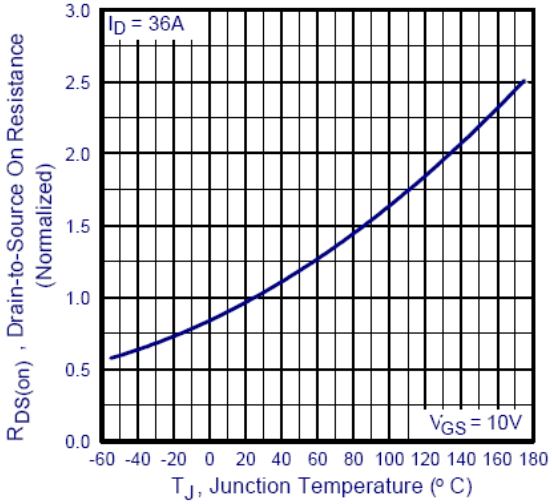


Fig 4. Normalized On-Resistance Vs. Temperature

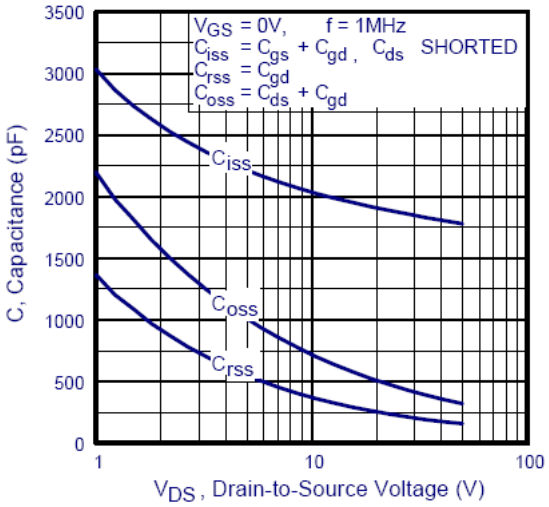


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

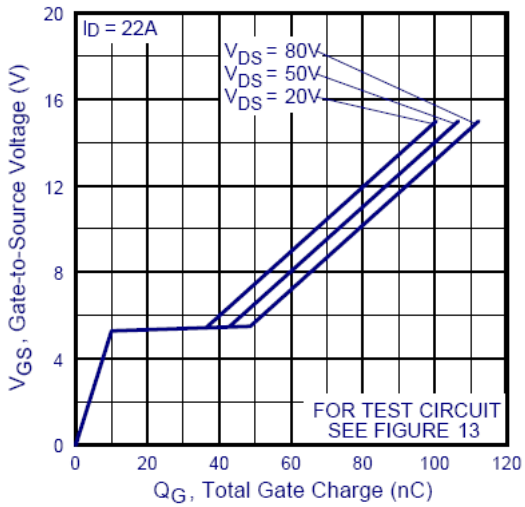


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

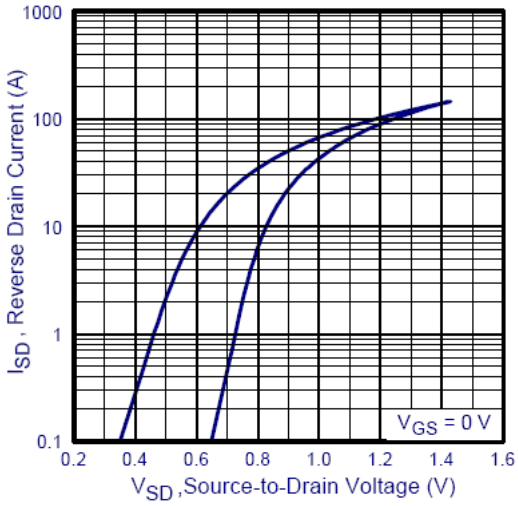


Fig 7. Typical Source-Drain Diode Forward Voltage

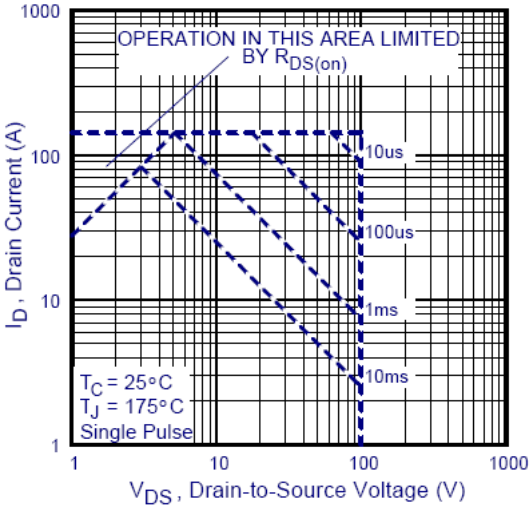


Fig 8. Maximum Safe Operating Area