

12 V – 5 V SWITCHED CAPACITOR DC-DC CONVERTER

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for the award of the degree of  
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JUNE 2012

“I hereby acknowledge that the scope and quality of this thesis is qualified for the award of the Bachelor Degree of Electrical Engineering (Power System)”

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## **DEDICATION**

**To my beloved mother and father:  
Azman Bin Sariban and Jeme Binti Jalil**

**My siblings:  
Saiful, Noorimah, Khairul, Ashrul, Norliza, Norzi, Noora, Norazima**

**and all my friends.**

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## **ABSTRACT**

The use of the DC-DC Converters has become more common in recent years. It also is one of the mostly used power electronic circuits and it has applications in various areas ranging from portable devices to aircraft power system. Various topologies of dc-dc converters are suitable for different applications. In this project, a prototype of the converter is constructed by using power switches, capacitors and inductorless components assures a small size, light weight and high power density of power supply. The selection of suitable switched capacitor is important to get the desired output. PSpice simulation and hardware implementation result will prove that the design circuit of “12 V – 5 V Switched Capacitor DC-DC Converter” can convert 12 V input power supply to the desired output 5 V.

## ABSTRAK

Penggunaan Penurunan DC-DC telah menjadi lebih kerap berlaku di tahun-tahun kebelakangan ini. Ia juga merupakan salah satu kebanyakan penggunaan kuasa litar elektronik dan ia mempunyai aplikasi dalam pelbagai bidang yang terdiri daripada peranti mudah alih kepada sistem kuasa pesawat. Pelbagai topologi penukar dc-dc yang sesuai untuk aplikasi yang berbeza. Dalam projek ini, prototaip penukar dibina dengan menggunakan suis kuasa, kapasitor dan tanpa komponen peraruh untuk memastikan saiz yang kecil, ringan dan ketumpatan kuasa tinggi daripada bekalan kuasa. Pemilihan kapasitor pengubah yang sesuai adalah penting untuk mendapatkan keluaran yang dikehendaki. Keputusan simulasi Pspice dan pelaksanaan perkakas akan membuktikan bahawa reka bentuk litar “12 V- 5 V Suis Kapasitor Pengubah DC-DC” boleh menukar bekalan kuasa kemasukan 12 V kepada 5 V keluaran yang dikehendaki.

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## **CHAPTER 1**

### **INTRODUCTION**

This chapter will explain the background of the project, objective of the project, scope of the project and problem statement. In this introduction section the review of Switched Capacitor DC-DC Converter will be discuss more detail.

#### **1.1 Background of the Project**

A dc-dc converter is an electronic circuit that allows for the conversion of direct current (dc) from one level of voltage to another level of voltage. Many consumer and industrial electronic products, such as LCD drivers, pocket computer systems etc, require more than one voltage sources. Hence, dc to dc converters are required for these applications.

A dc to dc converter has two main types of topologies, which are inductive converter and switched capacitor converter. Both of them according the components use to store and transfer energy. For many years, application of power supply in use is inductive converter. But in recent years, there is an increasing demand on the power converters with small size, light weight, high conversion efficiency, and high power density. All the features required are available on capacitor converter or inductorless converter. A switched capacitor is an integrated circuit element consisting of some switched and capacitor in which the capacitors are energy storage

components. Some switched refer to power switches. The power switches can be categorized into three groups. There are uncontrolled, semi-controlled and fully controlled.

## **1.2 Objective of the Project**

The objectives of this project are:

- i) To simulate the circuit by using PSPICE.
- ii) To design 12 V – 5 V switched capacitor dc – dc converter.
- iii) To select a suitable switched capacitor for dc – dc converter.

## **1.3 Scope of the Project**

The scopes of project are:

- i) Using MOSFET as a switched capacitor.
- ii) The converter is an inductorless.

## **1.4 Problem Statement**

For this project, 12 V<sub>dc</sub> from power supply need to convert to 5 V<sub>dc</sub> by using switched capacitor. The application device by using 5 V<sub>dc</sub> cannot get direct input voltage from power supply. The device can damage due to overvoltage. So, the dc to dc converter is a solution for this problem.



## **CHAPTER 2**

### **LITERATURE REVIEW**

This chapter discusses a basic concept of Switched Capacitor DC-DC Converter. This chapter also explains a detail about selection suitable switched capacitor for dc-dc converter.

#### **2.1 Introduction**

##### **2.1.1 DC-DC Converters**

Dc-dc converters are power electronics circuits that convert a dc voltage to a different dc voltage level. The isolator converter topologies are divided to three main types. There are buck converter, boost converter and buck-boost converter. A buck converter is a lowering the output voltage, step down application. A boost converter is a rising the output voltage, step up application. A buck-boost converter is a lowing or raising the output voltage. It can become to buck or boost converter [1].

### 2.1.2 The functions of dc-dc converter are:

- a) Convert a dc input voltage,  $V_s$  into a dc output voltage,  $V_o$ .
- b) Regulate the dc output voltage against load and line variation.
- c) Protect the supplied system and the input source from electromagnetic interference (EMI).
- d) Provide isolation between the input source and the load.
- e) To simplify power supply systems.
- f) To match the load to the power supply [1][2].

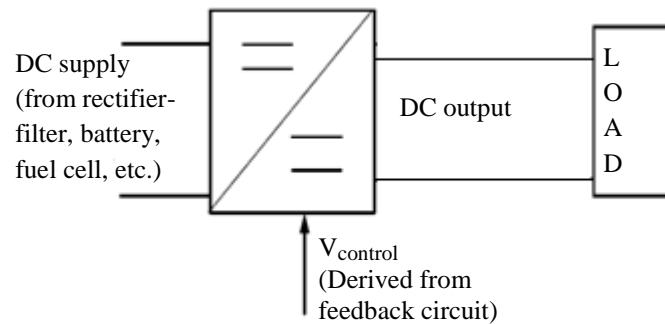


Figure 2.1 Basic block diagram dc-dc converter

## 2.2 Power Switches

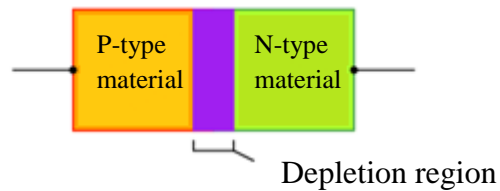
The power switches can be categorized into three groups.

- 1) Uncontrolled: diode
- 2) Semi-controlled: thyristor (SCR)
- 3) Fully controlled: power transistor (BJT, MOSFET, IGBT, GTO)

### 2.2.1 Uncontrolled: diode

Diode is suitable as an internally controlled switch where it just allow the current flow in one direction only [1].

a)



b)



c)

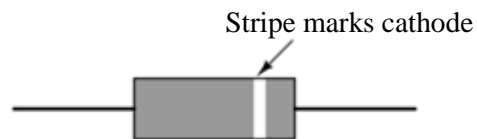


Figure 2.2 a) P-N junction representation, b) diode schematic symbol, c) real component appearance

### 2.2.2 Semi-controlled: thyristor (SCR)

A normal thyristors is not fully controllable switches. A "fully controllable switch" can be turned on and off at will. Thyristors can only be turned ON and cannot be

turned OFF. Thyristor is a family of three terminal devices. It has three terminals are the anode, cathode and gate. Thyristors are switched ON by a gate signal, but even after the gate signal is removed, it remains in the ON-state until any turn-off condition occurs. Which can be application of a reverse voltage to the terminals, or when the current flowing through (forward current) falls below a certain threshold value known as the "holding current". Thus, a thyristor behaves like a normal semiconductor diode after it is turned on or "fired". The thyristor also be able to conduct of large current and large voltage blocking for use in high power applications but limited switching frequencies between 10 to 20k Hz [1].

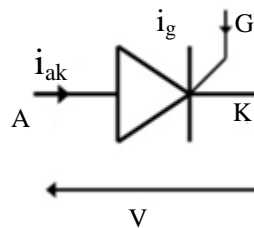


Figure 2.3 SCR schematic symbol

### 2.2.3 Fully Controlled: Power Transistor (BJT, MOSFET, IGBT, GTO)

In power electronics circuit a transistors are operated as switches. It is calling power transistor because it is controllable switches where as can be turned on and turned off by relatively very small control signal. It operated in saturation and cutoff modes only. No linear region operation is allowed due to excessive power losses.

### 2.2.3.1 Bipolar Junction Transistor (BJT)

The BJT is a current-controlled device. By design, most of the BJT collector current is due to the flow of charges injected from a high-concentration emitter into the base where there are minority carriers that diffuse toward the collector. So, BJTs are classified as minority-carrier devices. The voltage rating  $V_{CE}$  is less than 1000 V and current rating  $I_C$  is less than 400 A. The switching frequency up to 5k Hz and has low on-state voltage  $V_{CE(sat)}$  in range 2 and 3 V. In current driven, to obtain a reasonable  $I_C$  the  $I_B$  is required high current. The market value is high and complex base drive circuit. This device is not popular in new products [1].

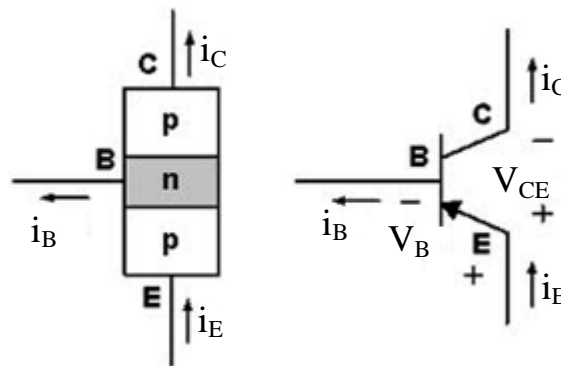
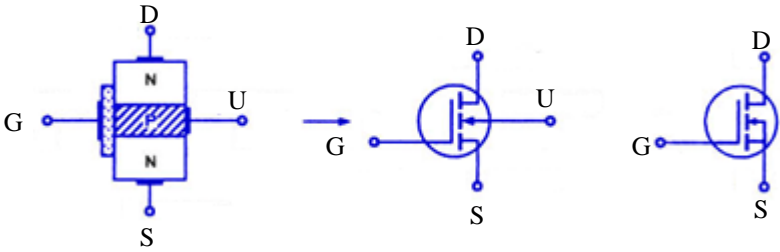


Figure 2.4 BJT schematic symbol

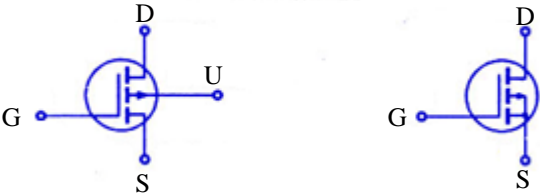
### 2.2.3.2 Metal Oxide Silicon Field Transistor (MOSFET)

Metal Oxide Silicon Field Transistor (MOSFET) is a voltage-controlled device. MOSFET have two modes of operation, depletion and enhancement. Hence, there are differences in the characteristics and operation of different types of MOSFET. The construction of an enhancement- type MOSFET is quite similar to that of the

depletion-type MOSFET. In enhancement mode operation, MOSFET have two type channel, channel and n-channel. The characteristic of p-channel is act as a reverse characteristic of n-channel. Turning on and off is very simple is a feature of MOSFET. That only need to provide  $V_{GS} = +15V$  to turn on and 0 V to turn off. Gate drive circuit is simple. Basically, MOSFET is a low voltage device. It is also dominant in high frequency application. Since frequency is largest that 100k Hz [1].



N – Channel E-MOSFET



P – Channel E-MOSFET

D: Drain      S: Source      G: Gate      U: Substrate

Figure 2.5 E-MOSFET schematic symbols

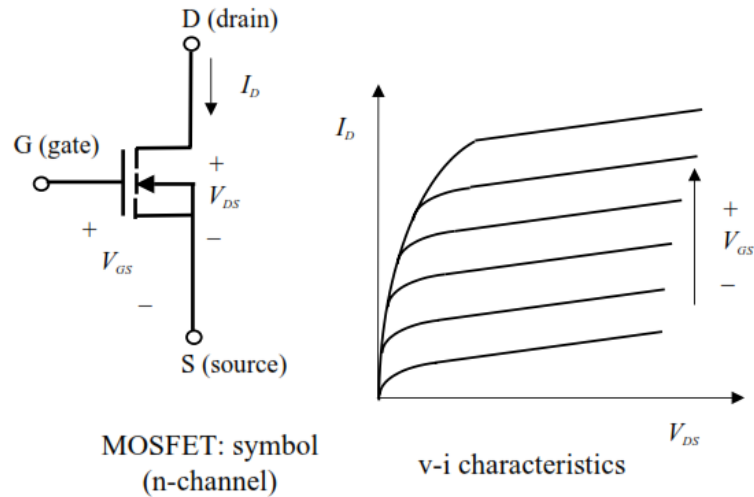


Figure 2.6 Symbol n-channel MOSFET and V-I characteristics

### 2.2.3.3 Insulated Gate Bipolar Transistor (IGBT)

Insulated Gate Bipolar Transistor (IGBT) is a combination of BJT and MOSFET characteristics. The device is easy to turn on and turn off. IGBT is turned on by applying a positive voltage between the gate and emitter and is turned off by making the gate signal zero or slightly negative. The gate behavior is similar to MOSFET. It has low losses like BJT due to low on-state Collector-Emitter. Hence, it has excellent switching characteristics, simple gate-drive circuit, peak current capability, high input impedance and snubberless. IGBTs are available in current and voltage ratings. Voltage rating,  $V_{CE} < 3.3\text{k V}$  and current rating,  $I_C < 1.2\text{k A}$  [1].

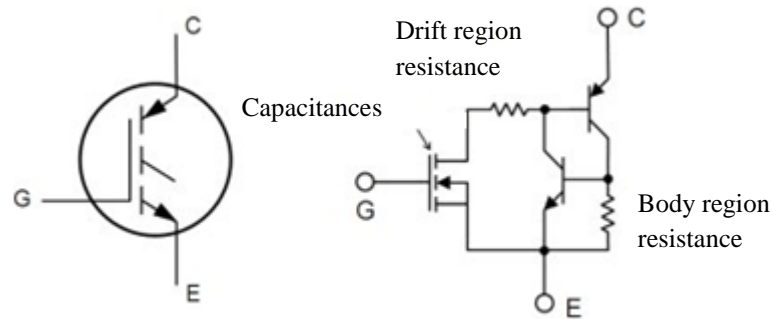


Figure 2.7 IGBT schematic symbol and equivalent circuit

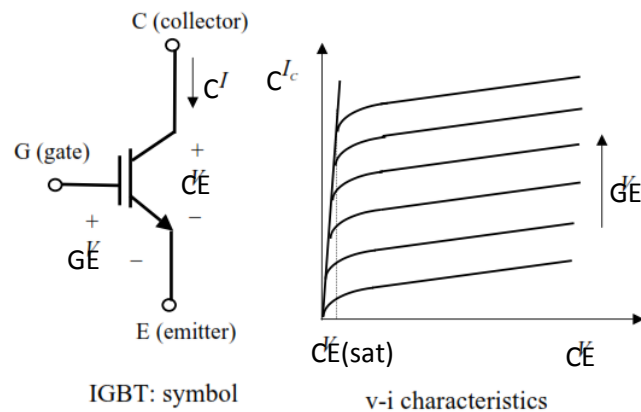


Figure 2.8 IGBT symbol and V-I characteristics

#### 2.2.3.4 Gate Turn-Off Thyristor (GTO)

Gate Turn-Off Thyristor (GTO) behaves like normal thyristor, but can be turned off using gate signal. However turning off is difficult. Need very large reverse gate current and normally  $1/5$  of anode current. GTO is a current driven device. It has voltage rating,  $V_{ak} < 5k$  V and current rating,  $I_a < 5k$  A. Hence, highest power ratings switch, frequency  $< 5k$  Hz. GTO normally required snubbers and high power snubbers are expensive[1].



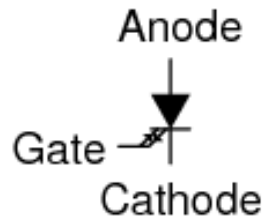


Figure 2.9 GTO schematic symbols

### 2.3 Comparison of Power Switches

Table 2.1 Comparison of power switches

Features	BJT	MOSFET	IGBT	GTO
Drive method	Current	Voltage	Voltage	Current
Drive circuit	Complex	Simple	Simple	Complex
Input impedance	Low	High	High	Low
Drive power	High	Low	Low	High
Switching speed	Slow ( $\mu\text{s}$ )	Fast (ns)	Medium	Medium
Operating frequency	Low (< 100 kHz)	Fast (<1 MHz)	Medium	Medium
SOA	Narrow	Wide	Wide	Wide
Saturation voltage	Low	High	Low	Low

\*SOA = safe operating area

By refer to the Table 1; MOSFET is a suitable switch compares the other power switches. MOSFET have more interesting characteristics. Easy to turn on and turn off. Gate drive circuit is simple and faster in switching speed than others power switches. It has a wide in safe operating area and high saturation voltage than else. MOSFET also is a biggest application in switched mode power supplies (SMPS) [2][3].

## 2.4 Capacitor

A capacitor is a passive element designed to store energy in electric field. It consists of two conducting plates separated by an insulator. A capacitor also acts as a filter. A set of capacitors in series-parallel connection may improve the efficiency of some step down switched capacitor converters. The capacitors in series parallel connections have the characteristic of charging in series and discharging in parallel [4].

At certain switching instants, some of the capacitors are switched to an input energy source so that energy is stored in these capacitors. At the same time, another set of capacitors are switched to the output load and deliver energy. When the switches turn on and turn off alternatively, those capacitors which have released energy before, are now switched to the input energy source and charged up while those capacitors which have stored energy before are now switched to the output load and deliver energy. Because of this operating principle, ripples usually occur at the output load voltage, while the ripple magnitude of the output load voltage is dependent on the capacitances of the capacitors, the resistance of the load, and the switching instants. Since almost all the applications require a steady voltage for their operations and the output ripple magnitude should be minimized [5][6].

## 2.5 555 Timer

The 555 timer has two basic operational modes: monostable and astable. In the monostable mode, the 555 Timer is function as a one-shot. It is said to have a single stable state that is the off state. Whenever it is triggered by an input pulse, the monostable switches to its temporary state. It remains in that state for a period of time determined by an RC network. It then returns to its stable state. In other words, the monostable circuit generates a single pulse of fixed time duration each time it receives an input trigger pulse. Thus the name is one-shot. One-shot multivibrators are used for turning some circuit or external component on or off for a specific length of time. It is also used to generate delays. When multiple one-shots are cascaded, a variety of sequential timing pulses can be generated. Those pulses will allow you to time and sequence a number of related operations.

The other basic operational mode of the 555 is as astable mode. An astable mode is simply and the 555 Timer is function as an oscillator. It generates a continuous stream of rectangular off on pulses that switch between two voltage levels. The frequency of the pulses and their duty cycle are dependent upon the RC network values [7].

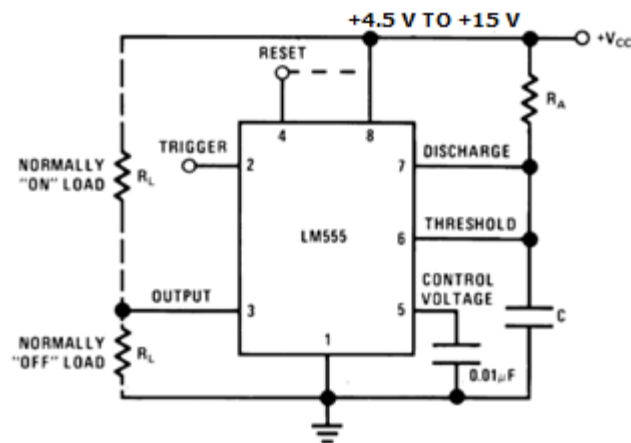


Figure 2.10 Monostable circuit

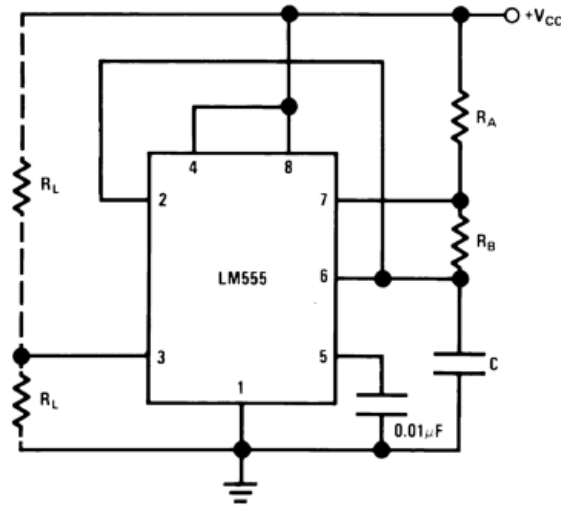


Figure 2.11 Astable circuit

### 2.5.1 Definition of Pin Functions

a) Pin 1 (Ground):

The ground (or common) pin is the most-negative supply potential of the device, which is normally connected to circuit common (ground) when operated from positive supply voltages.

b) Pin 2 (Trigger):

This pin is the input which causes the output to go high and begin the timing cycle. Triggering occurs when the trigger input moves from a voltage above  $2/3$  of the supply voltage to a voltage below  $1/3$  of the supply. For example using a 12 volt supply, the trigger input voltage must start from above 8 volts and move down to a voltage below 4 volts to begin the timing cycle. The action is level sensitive and the trigger voltage may move very slowly.

c) Pin 3 (Output)

Pin 3 is the digital output of the 555. It can be connected directly to the inputs of other digital ICs, or it can control other devices with the help of a few extra components.

d) Pin 4 (Reset)

Pin 4 is called the Reset input as it is this input that resets the output to the low state. This pin may be connected to push buttons to control the operation of the 555. Sometimes the Reset input is not used in a circuit, in which case it is connected directly to  $V_s$ . So that unwanted resetting cannot occur.

e) Pin 5 (Control Voltage)

A voltage applied to this pin will vary the timing of the RC network (quite considerably). The control voltage may be varied from 45 to 90% of the  $V_{cc}$  in the monostable mode, making it possible to control the width of the output pulse independently of RC. When it is used in the astable mode, the control voltage can be varied from 1.7V to the full  $V_{cc}$ . Varying the voltage in the astable mode will produce a frequency modulated (FM) output. In the event the control-voltage pin is not used, it is recommended that it be bypassed to ground. But if connects with a capacitor of about 0.01 $\mu$ F (10nF) for immunity to noise. This capacitor acts as decoupling capacitor. It can help stabilize the threshold and trigger reference voltage internal to the 555 Timer.

f) Pin 6 (Threshold)

Pin 6 is used to reset the latch and cause the output to go low. Reset occurs when the voltage on this pin moves from a voltage below  $1/3$  of the supply to a voltage above  $2/3$  of the supply. The action is level sensitive and can move slowly similar to the trigger voltage.

g) Pin 7 (Discharge)

This pin is an open collector output which is in phase with the main output on pin 3 and has similar current sinking capability.

h) Pin 8 ( $V_+$  /  $V_{cc}$ )

Pin 8 is where you connect the positive power supply ( $V_s$ ) to the 555. This can be any voltage between 4.5 V and 15 V DC, but is commonly 5V DC when working with digital ICs.

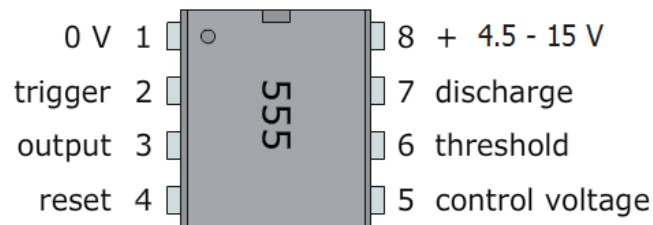


Figure 2.12 Pin out diagram of the 555 Timer

### 2.5.2 Operation of Astable Mode

Astable circuit is shown in figure 2.11. Both the trigger and threshold inputs (pins 2 and 6) to the two comparators are connected together and to the external capacitor. The capacitor charges toward the supply voltage through the two resistors,  $R_1$  and  $R_2$ . The discharge pin (7) connected to the internal transistor is connected to the junction of those two resistors. When power is first applied to the circuit, the capacitor will be uncharged. Therefore, both the trigger and threshold inputs will be near zero volts (see Figure 2.13). The lower comparator sets the control flip-flop causing the output to switch high. That also turns off transistor  $T_1$ . That allows the capacitor to

begin charging through R1 and R2. As soon as the charge on the capacitor reaches 2/3 of the supply voltage, the upper comparator will trigger causing the flip-flop to reset. That causes the output to switch low. Transistor T1 also conducts. The effect of T1 conducting causes resistor R2 to be connected across the external capacitor. Resistor R2 is effectively connected to ground through internal transistor T1. The result of that is that the capacitor now begins to discharge through R2 [7].

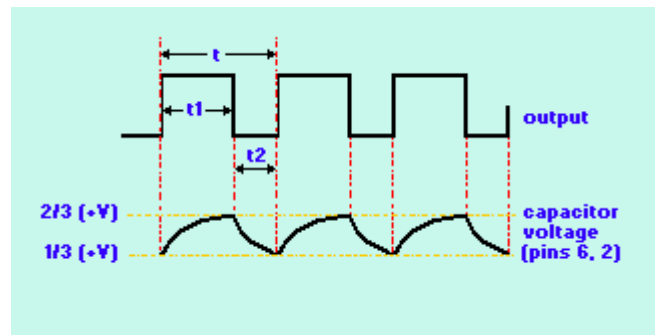


Figure 2.13 Pulse form signal

At the point where the voltage across the capacitor reaches 1/3 of the supply voltage, the lower comparator is triggered. That again causes the control flip-flop to set and the output to go high. Transistor T1 cuts off and again the capacitor begins to charge. That cycle continues to repeat with the capacitor alternately charging and discharging, as the comparators cause the flip-flop to be repeatedly set and reset. The resulting output is a continuous stream of rectangular pulses [7].

An output pulse is determined by the values of two resistors,  $R_A$  and  $R_B$  and by the timing capacitor,  $C$ . The design formula for the frequency,  $f$  of the pulses is [7]:

$$f = \frac{1}{0.693 \times C (R_A + 2R_B)} \quad (2.5.2.1)$$

The period,  $T$  of the pulses is given by:

$$T = \frac{1}{f} = 0.693 \times C (RA + 2RB) \quad (2.5.2.2)$$

The HIGH,  $t_1$  and LOW,  $t_2$  each pulse can be calculated from:

$$\text{HIGH, } t_1 = \text{charge time} = 0.693 \times C (RA + RB) \quad (2.5.2.3)$$

$$\text{LOW, } t_2 = \text{discharge time} = 0.693 \times C (RB) \quad (2.5.2.4)$$

The duty cycle,  $D$  of the waveform is:

$$D = \frac{T_{\text{on}}}{T} = \frac{RA + RB}{RA + 2RB} \quad (2.5.2.5)$$



## CHAPTER 3

### METHODOLOGY

This chapter will explain detail about stage development of Switched Capacitor DC-DC Converter

#### 3.1 Block Diagram of Switched Capacitor Dc-Dc Converter

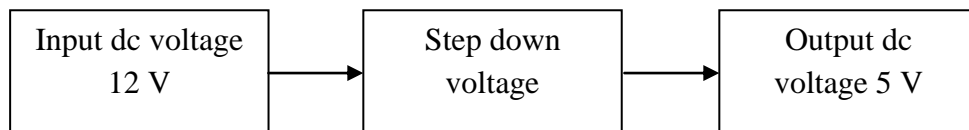


Figure 3.1 The block diagram of Switched Capacitor DC-DC Converter

Based on the block diagram of Switched Capacitor DC-DC Converter is shown in Figure 3.1, the  $12\text{ V}_{\text{dc}}$  input voltage is convert to  $5\text{ V}_{\text{dc}}$  by using stepdown voltage that derived from the circuit used in this project.

### 3.2 Gate Drive Circuit

Gate drive circuit is important to MOSFET to make it function and at the same time as switches. A 555 Timer is used to produce a pulse form signal. This timer use astable mode as operational mode. Switching frequency of MOSFET is use at range 20 kHz - 25 kHz. An output pulse is determined by the values of two resistors,  $R_A$  and  $R_B$  and by the timing capacitor,  $C$ . The below is shown calculation for value of frequency, period, duty cycle, high and low times that produce by 555 Timer.

$$R_A = 3 \text{ k}\Omega \quad R_B = 1.5 \text{ k}\Omega \quad C = 0.01 \text{ }\mu\text{F}$$

#### Frequency, f:

From equation (2.5.2.1)

$$\begin{aligned} f &= \frac{1}{0.693 \times C (R_A + 2R_B)} \\ &= \frac{1}{0.693 \times 0.01\mu \times (3\text{k} + 2(1.5\text{k}))} \\ &= 24.0 \text{ kHz} \end{aligned}$$

#### Period, T:

From equation (2.5.2.2)

$$\begin{aligned} T &= \frac{1}{f} = 0.693 \times C (R_A + 2R_B) \\ &= 0.693 \times 0.01\mu \times (3\text{k} + 2(1.5\text{k})) \\ &= 41.58 \text{ }\mu\text{s} \end{aligned}$$

**HIGH time, t1:**

From equation (2.5.2.3)

$$\text{HIGH, } t_1 = \text{charge time} = 0.693 \times C (R_A + R_B)$$

$$= 0.693 \times 0.01\mu \times (3\text{k} + 1.5\text{k})$$

$$= 31.189 \mu\text{s}$$

**LOW time, t2:**

From equation (2.5.2.4)

$$\text{LOW, } t_2 = \text{discharge time} = 0.693 \times C (R_B)$$

$$= 0.693 \times 0.01\mu \times 1.5 \text{ k}$$

$$= 10.395 \mu\text{s}$$

**Duty cycle, D:**

From equation (2.5.2.5)

$$D = \frac{T_{\text{on}}}{T} = \frac{R_A + R_B}{R_A + 2R_B}$$

$$= \frac{4.5\text{k}}{6\text{k}} = 0.75$$

By using PSpice software, the gate drive circuit is formed by 555 Timer (555D) is shown in Figure 3.2. The operational mode of timer is an astable mode. So, it has  $R_A$ ,  $R_B$  and  $C$ . The pin 5 is connected with  $0.01 \mu\text{F}$  and it acts as a decoupling capacitor. This chip uses 9 Vdc power supply.

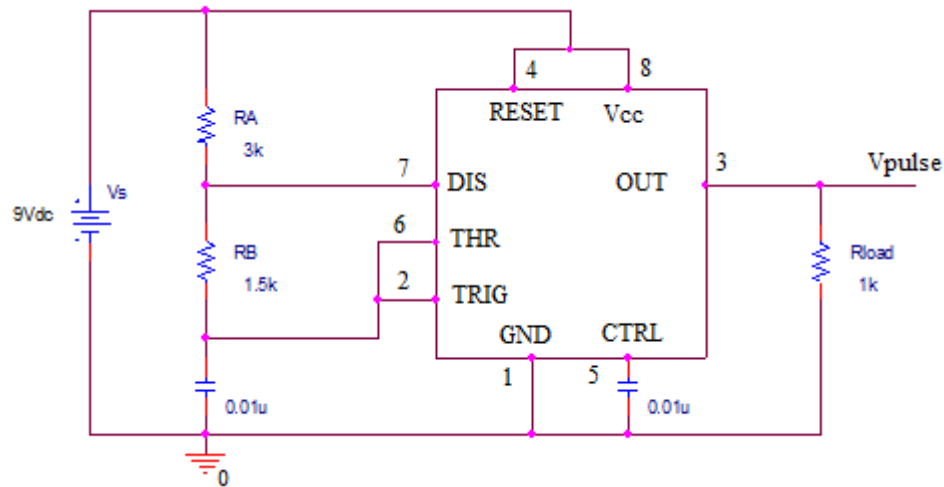


Figure 3.2 Gate driver circuit

### 3.3 12V-5V Switched Capacitor DC-DC Converter Circuit

By using PSpice software, the switched capacitor circuit is formed by two capacitors ( $C_1$  and  $C_2$ ), two externally-controlled switches ( $M_1$  and  $M_2$ ) and three internally-controlled switches ( $D_1 \sim D_3$ ). A capacitor,  $C_o$  is connected in parallel to the load. The illustration circuit is shown in Figure 3.3.

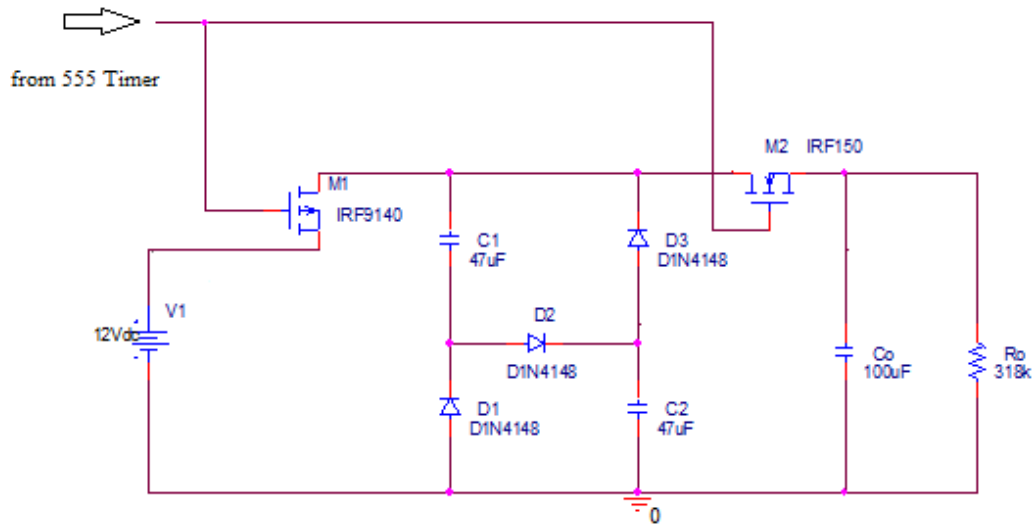


Figure 3.3 Structure of Switched Capacitor Converter Circuit

This circuit has two steady operation, state 1 and state 2. The operation is according to the timing diagram. Typically, a P-Mosfet is used as M1, while an N-Mosfet is used as M2. Thus, the timing diagram of the two switches is shown in Figure 3.4.

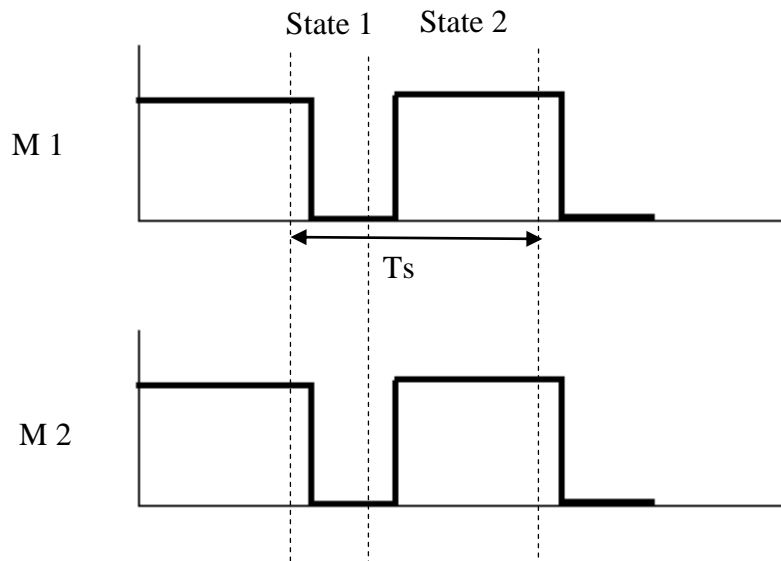


Figure 3.4 Timing diagram of the Switched Capacitor Converter

State 1: (M1 ON & M2 OFF)

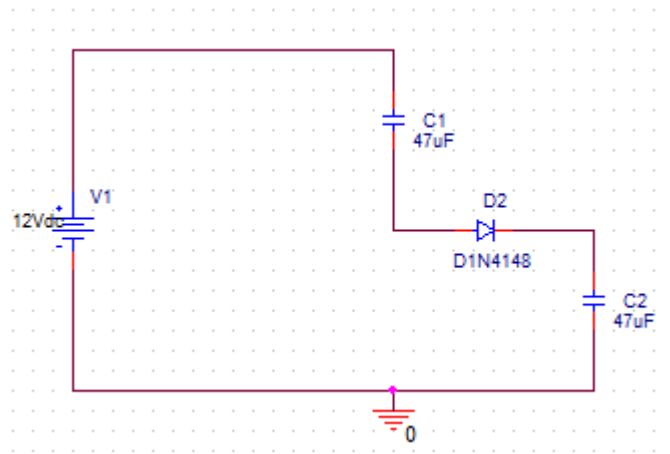


Figure 3.5 Equivalent circuit of Switched Capacitor Converter in state 1

In state 1, M1 is switched on and M2 is switched off. D2 is forward biased and D1, D3 is reverse biased. Consequently, C1 and C2 are connected in series to the input voltage. The capacitors being equal in value, C1 and C2 are charged at the same voltage

State 2: (M1 OFF & M2 ON)

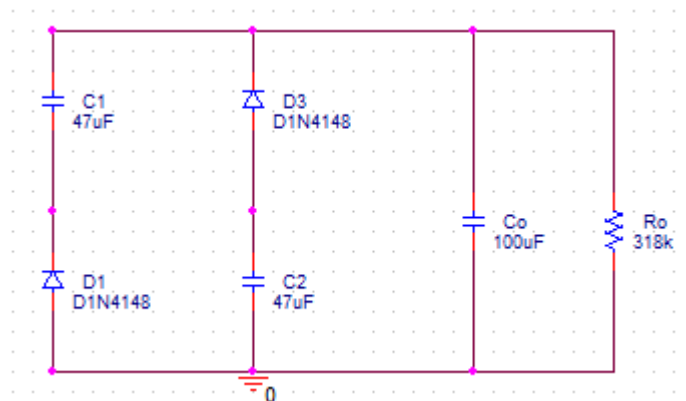


Figure 3.6 Equivalent circuit of Switched Capacitor Converter in state 2

In state 2, the switching timing is a vice versa where M2 is switched on and M1 is switched off. D2 is reverse biased and D1, D3 is forward biased. C1 and C2 continue their discharge on the load from the previous state. The output voltage is given by the voltage across capacitor C1, C2 in parallel. With the capacitor output,  $C_o$  the output voltage ripple can be reduced.

### 3.4 Testing Component

#### 3.4.1 555 Timer



Figure 3.7 555 Timer

The 555 Timer circuit is shown in Figure 3.7. The chip is supplied by 9 Vdc. LED as a load and light on when 555 Timer functioning. A Pulse form signal from 555 Timer is shown in Figure 3.8.

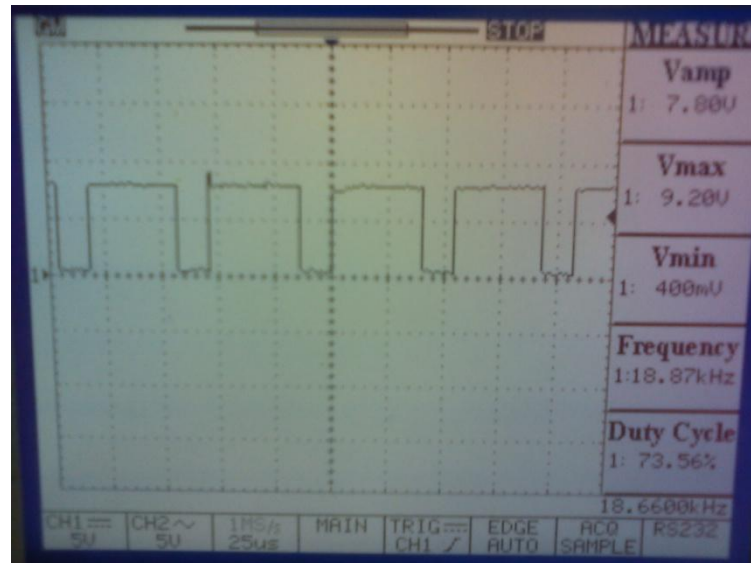


Figure 3.8 Pulse form signal from 555 Timer

### 3.4.2 P-MOSFET

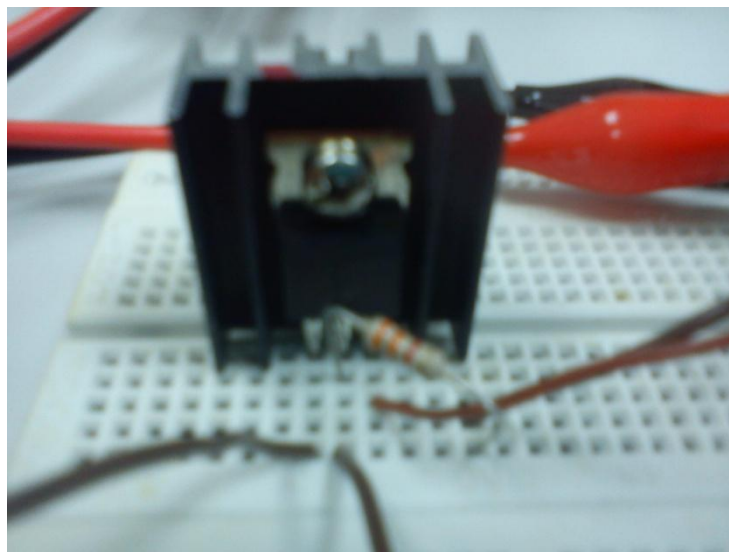


Figure 3.9 P-MOSFET testing



P-MOSFET testing is shown in Figure 3.9. P-MOSFET is use model IRF9640. The MOSFET testing is use oscilloscope to see the output. That component is supplied 6 Vdc. The resistor 220k  $\Omega$  is connect to pin Drain,D and output can see with tapped the probe at resister load. Pulse form signal of P-MOSFET is shown in Figure 3.10. Pulse of channel 1 is 555 Timer and pulse of channel 2 is P-MOSFET. Based on the pulse form signal, P-MOSFET is switched on when input is low and switched off when input is high.

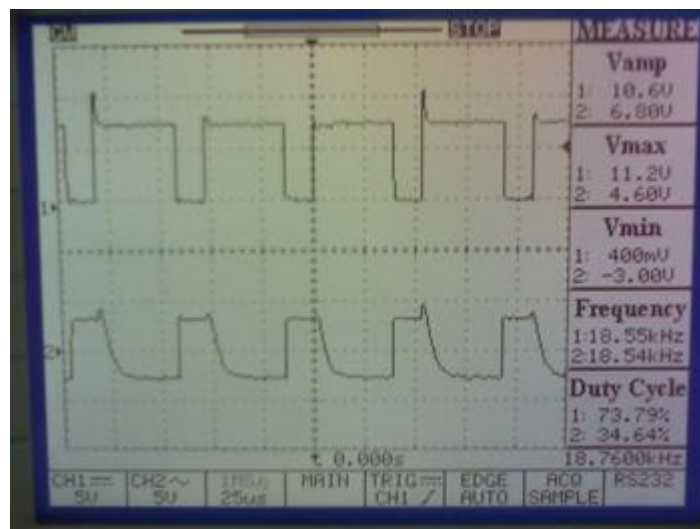


Figure 3.10 Pulse form signal of 555 Timer and P-MOSFET

### 3.4.3 N-MOSFET

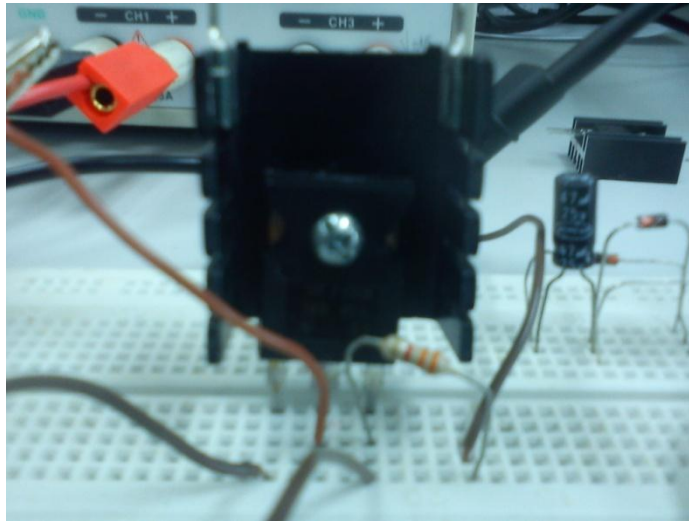


Figure 3.11 N-MOSFET Testing

N-MOSFET testing is shown in Figure 3.11. N-MOSFET is use model IRF150. The step to doing the N-MOSFET testing is same with P-MOSFET but different component connection. The resistor  $220k \Omega$  is connect to pin Source,S. Pulse form signal of N-MOSFET is shown in Figure 3.12. Pulse of channel 1 is 555 Timer and pulse of channel 2 is N-MOSFET. Based on the pulse form signal, N-MOSFET is switched on when input is high and switched off when input is low.

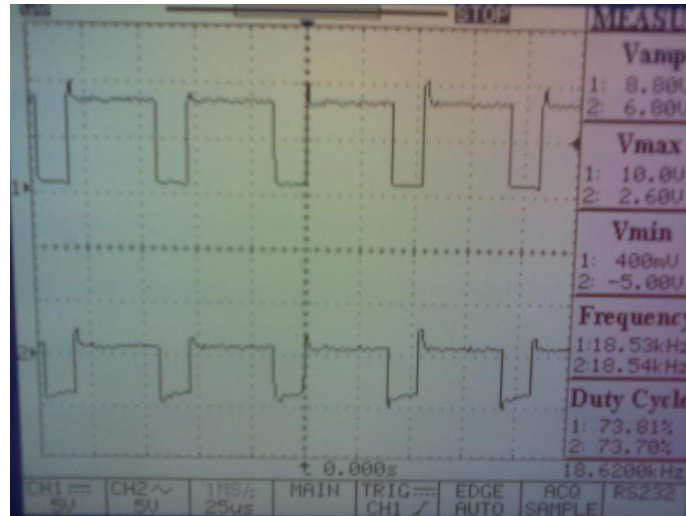


Figure 3.12 Pulse form signal of 555 Timer

## CHAPTER 4

### RESULT AND DISCUSSION

This chapter will explain the details of the results obtained from this project. This chapter included the software and hardware implementation results. The software results consist of simulation of fully design of Step down Switched Capacitor DC-DC Converter by using PSpice software.

#### 4.1 Operation of the Converter

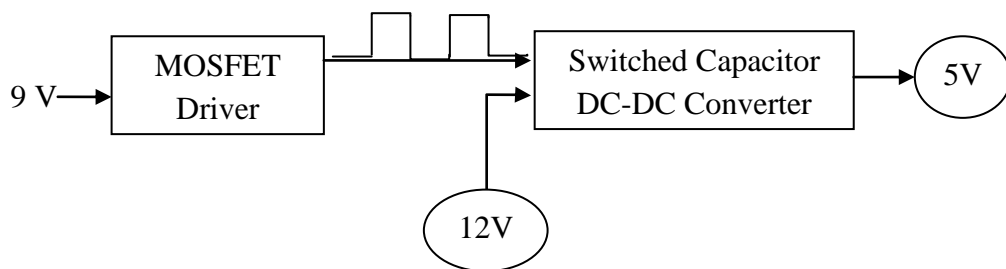


Figure 4.1 The operation of the Switched Capacitor Dc-Dc converter

The block diagram shows the actual operation of the circuit. Voltage constantly supplies 9 V to the MOSFET driver. This is to ensure that the driver chip can operate under optimal condition. The pulse form signal is an input to the driver and at the same time as a switch to turn on and turn off the MOSFET. The Switched Capacitor DC-DC Converter is a main circuit to convert 12 V to 5 V. The main circuit consists of two types of MOSFET, p-channel and n-channel MOSFET. The MOSFET alternated conduct based on the pulse form signal and the circuit only used one stage. This is the overall summary on the operation of the switched capacitor converter.

#### **4.1.1 Pulse Form Signal for MOSFET Driver**

This project is used two types of MOSFET. The Student version of PSpice Software that is used offers models for the p-channel (IRF9140) and n-channel (IRF150) power MOS switched. The MOSFET is required pulse form signal to inject at  $V_{gs}$  and make it function correctly. So, 555 Timer (555D) was used to produce that pulse. The operational mode of 555 Timer is astable mode. The schematic diagram is illustrated in Figure 4.2. The probe was tapped to measure the pulse form signal is shown in Figure 4.3.



Referring to Figure 4.2 and Figure 4.3, the result of simulation for value of pulse form signal voltage is 6.922 V. The value of period for one cycle is exactly 40  $\mu$ s and percentage of duty cycle is 75%.

#### 4.1.2 Voltage Output for Switched Capacitor DC-DC Converter

A 12V-5V Switched Capacitor DC-DC Converter has been simulated by using PSpice. The probe was tapped at  $V_{in}$  and  $V_{out}$  as shown in Figure 4.4. The result of  $V_{in}$  and  $V_{out}$  is shown in Figure 4.5.

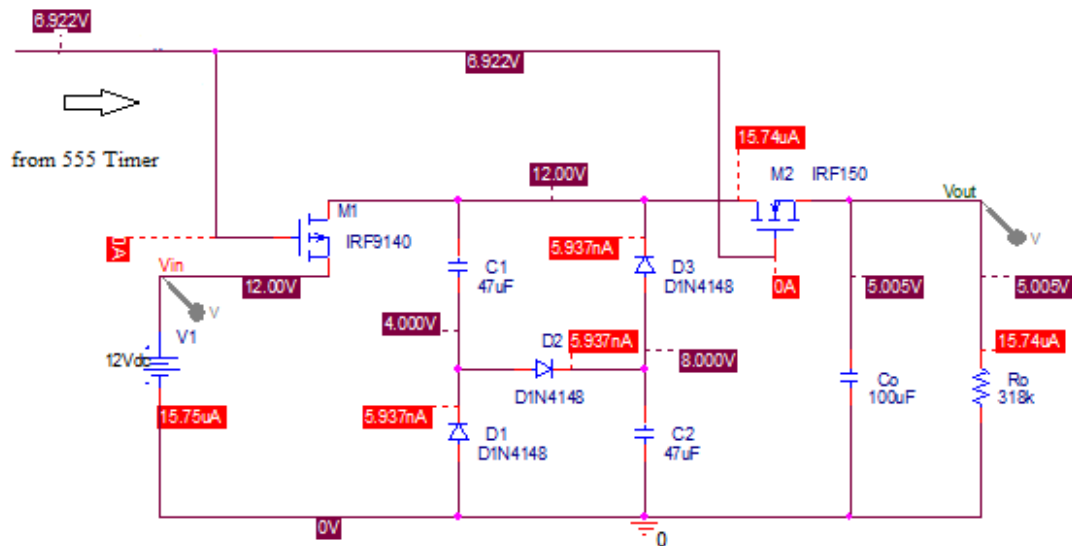


Figure 4.4 Probe tapped at input and output voltage

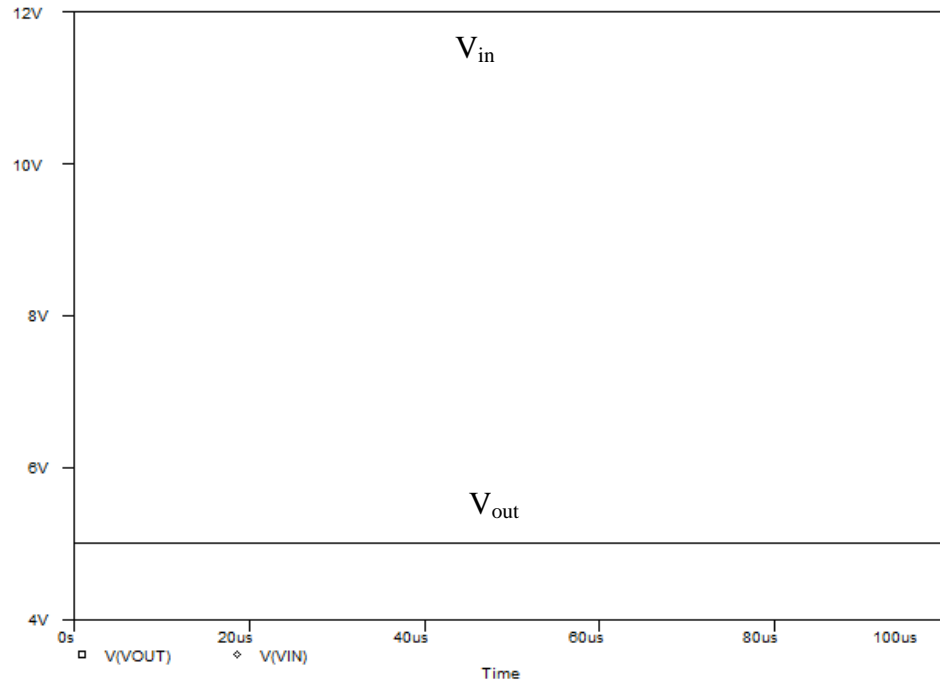


Figure 4.5 Graph for input and output voltage

## 4.2 Hardware Implementation

In hardware implementation the circuit divided by two parts, gate drive circuit and converter circuit.

### 4.2.1 Gate Drive Circuit

Gate driver circuit for driver MOSFET is used 555 Timer (NE555P). Voltage constantly supplies 9V dc to 555 Timer to energize that chip. The implementation of the gate drive circuit is shown in Figure 4.6.



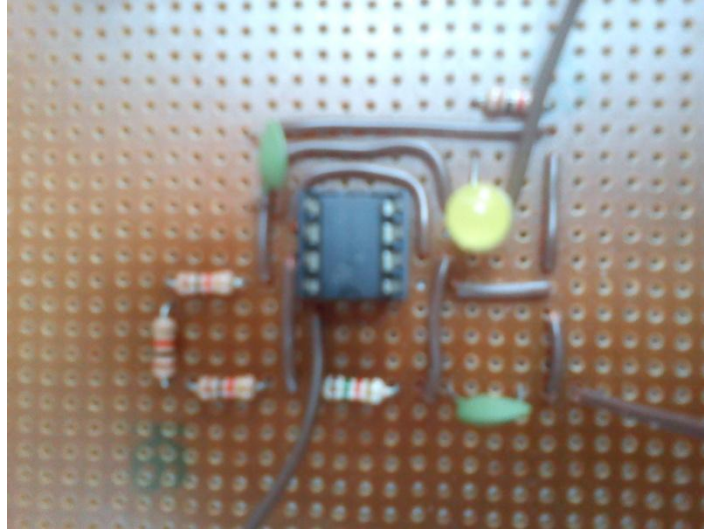


Figure 4.6 Implementation of gate drive circuit

#### 4.2.2 Switched Capacitor DC-DC Converter Circuit

The circuit of Switched Capacitor DC-DC Converter was implemented as shown in Figure 4.7. This circuit is using two type of MOSFET, p-channel (IRF9640) and n-channel (IRFP150N). In hardware implementation, p-channel MOSFET used is a different model. It is not same with simulation circuit. IRF9140 was used in simulation circuit for p-channel MOSFET. The characteristics of both MOSFET are not more different. IRF9640 can be use to replace IRF9140.

The result was obtained is shown in Figure 4.8. The probe is tapped at  $R_{load}$  to measure the output voltage. The output voltage is equal to 8.09 V. The result of simulation and hardware implementation is quite different. But  $R_{load}$  used is 1.5 k $\Omega$  the output voltage is 5.04 V. This problem is checked by using simulation by changing the value of  $R_{load}$  is equal to 1.5 k $\Omega$ , the reading of output voltage is 4 V. The value that obtained is not accurate compare with simulation result. The function of output capacitor is to reduce voltage ripple and give smooth reading.

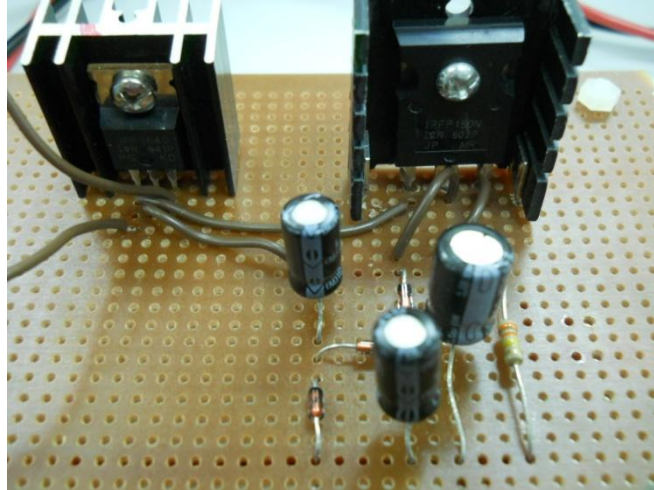


Figure 4.7 Switched Capacitor DC-DC Converter Circuit

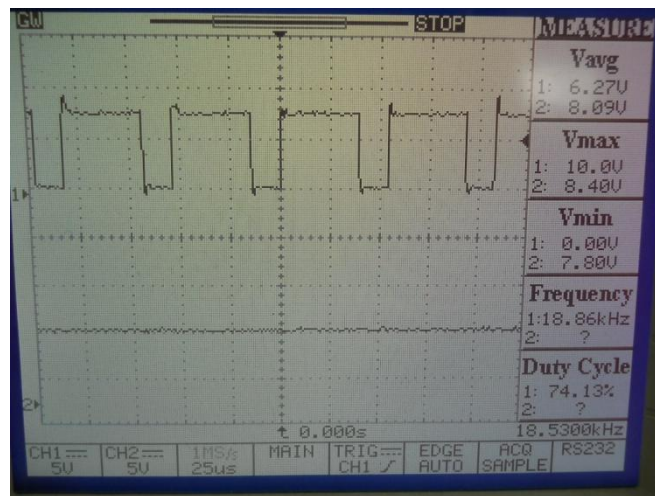


Figure 4.8 Pulse form signal and output voltage for  $R_{load} = 318 \text{ k}\Omega$

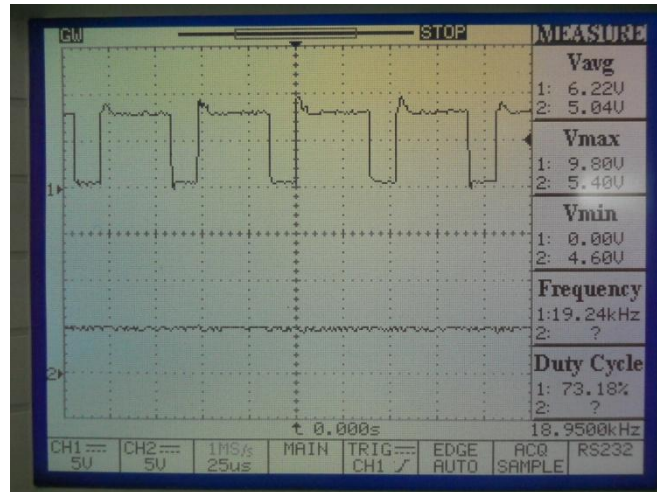


Figure 4.9 Pulse form signal and output voltage for  $R_{load} = 1.5 \text{ k}\Omega$

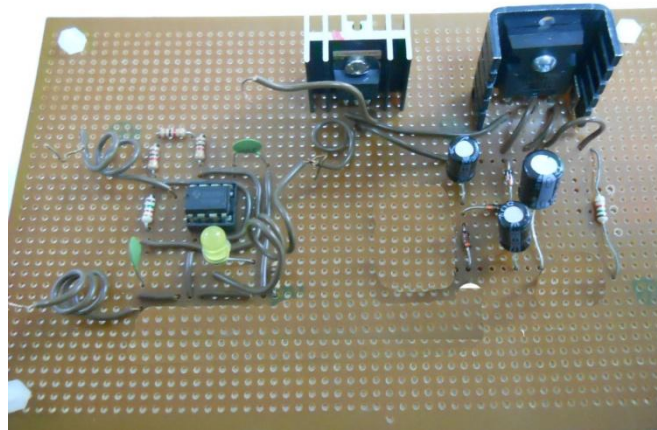


Figure 4.10 12 V – 5 V Switched Capacitor DC-DC Converter Circuit

## **CHAPTER 5**

### **CONCLUSION AND RECOMMENDATION**

#### **5.1 Conclusion**

A 12 V -5 V Switched Capacitor DC-DC Converter has been completed by using simulation PSpice software and hardware implementation. The selection of MOSFET as a suitable switched capacitor for this converter is refer to the feature of drive method, simple drive circuit, high input impedance, low drive power, fast in switching speed and operating frequency, wide of safe operating area and last it has high saturation voltage than the other power switches. This project constructed MOSFET power switches, capacitor and inductorless assures a small size, light weight and high power density of the power supply.

#### **5.2 Recommendations**

In this project, the value of output for simulation and hardware implementation is different. So, to overcome this problem, the feedback circuit can added to make a closed loop circuit and keep output voltage at a fixed value.

A next recommendation is make a multi-stage for Switched Capacitor DC-DC Converter. This project only uses one stage. The multi-stage can improved the value of step down voltage.

Lastly, for future projects on the ripple voltage analysis can be done to ensure the smooth output voltage.

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**APPENDICES**





February 2000

## LM555 Timer

### General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

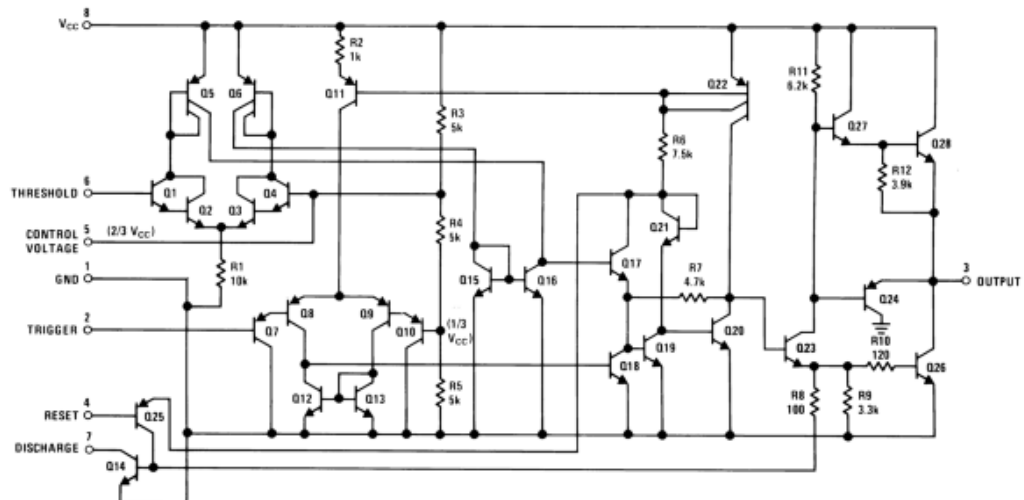
### Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output
- Available in 8-pin MSOP package

### Applications

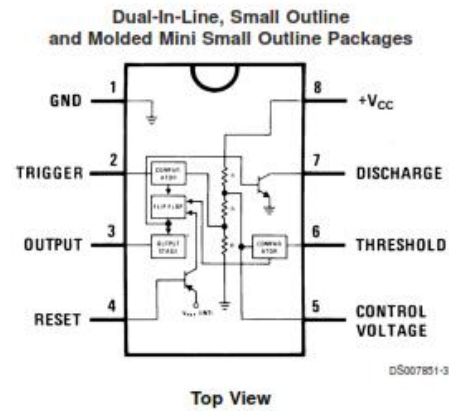
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

### Schematic Diagram



DS007851-1

## Connection Diagram



## Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
8-Pin SOIC	LM555CM	LM555CM	Rails	M08A
	LM555CMX	LM555CM	2.5k Units Tape and Reel	
8-Pin MSOP	LM555CMM	Z55	1k Units Tape and Reel	MUA08A
	LM555CMMX	Z55	3.5k Units Tape and Reel	
8-Pin MDIP	LM555CN	LM555CN	Rails	N08E

### Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	+18V
Power Dissipation (Note 3)	
LM555CM, LM555CN	1180 mW
LM555CMM	613 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C

### Soldering Information

Dual-In-Line Package	
Soldering (10 Seconds)	260°C
Small Outline Packages	
(SOIC and MSOP)	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

### Electrical Characteristics (Notes 1, 2)

( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = +5\text{V}$  to  $+15\text{V}$ , unless otherwise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Supply Voltage		4.5		16	V
Supply Current	$V_{CC} = 5\text{V}$ , $R_L = \infty$ $V_{CC} = 15\text{V}$ , $R_L = \infty$ (Low State) (Note 4)		3 10	6 15	mA
Timing Error, Monostable					
Initial Accuracy			1		%
Drift with Temperature	$R_A = 1\text{k}$ to $100\text{k}\Omega$ , $C = 0.1\mu\text{F}$ , (Note 5)		50		ppm/°C
Accuracy over Temperature			1.5		%
Drift with Supply			0.1		%/V
Timing Error, Astable					
Initial Accuracy			2.25		%
Drift with Temperature	$R_A, R_B = 1\text{k}$ to $100\text{k}\Omega$ , $C = 0.1\mu\text{F}$ , (Note 5)		150		ppm/°C
Accuracy over Temperature			3.0		%
Drift with Supply			0.30		%/V
Threshold Voltage			0.667		$\times V_{CC}$
Trigger Voltage	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$		5 1.67		V V
Trigger Current			0.5	0.9	$\mu\text{A}$
Reset Voltage		0.4	0.5	1	V
Reset Current			0.1	0.4	mA
Threshold Current	(Note 6)		0.1	0.25	$\mu\text{A}$
Control Voltage Level	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	9 2.6	10 3.33	11 4	V V
Pin 7 Leakage Output High			1	100	nA
Pin 7 Sat (Note 7)					
Output Low	$V_{CC} = 15\text{V}$ , $I_7 = 15\text{mA}$		180		mV
Output Low	$V_{CC} = 4.5\text{V}$ , $I_7 = 4.5\text{mA}$		80	200	mV

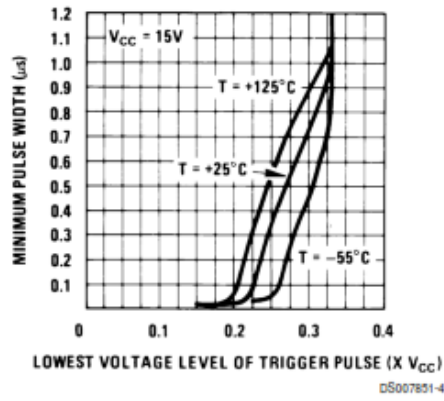
**Electrical Characteristics** (Notes 1, 2) (Continued)(T<sub>A</sub> = 25°C, V<sub>CC</sub> = +5V to +15V, unless otherwise specified)

Parameter	Conditions	Limits			Units
		LM555C			
		Min	Typ	Max	
Output Voltage Drop (Low)	V <sub>CC</sub> = 15V				
	I <sub>SINK</sub> = 10mA		0.1	0.25	V
	I <sub>SINK</sub> = 50mA		0.4	0.75	V
	I <sub>SINK</sub> = 100mA		2	2.5	V
	I <sub>SINK</sub> = 200mA		2.5		V
	V <sub>CC</sub> = 5V				
Output Voltage Drop (High)	I <sub>SOURCE</sub> = 200mA, V <sub>CC</sub> = 15V		12.5		V
	I <sub>SOURCE</sub> = 100mA, V <sub>CC</sub> = 15V	12.75	13.3		V
	V <sub>CC</sub> = 5V	2.75	3.3		V
Rise Time of Output			100		ns
Fall Time of Output			100		ns

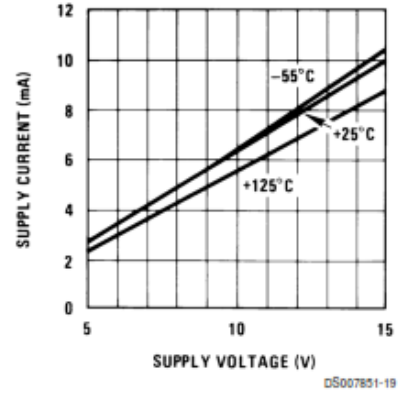
**Note 1:** All voltages are measured with respect to the ground pin, unless otherwise specified.**Note 2:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.**Note 3:** For operating at elevated temperatures the device must be derated above 25°C based on a +150°C maximum junction temperature and a thermal resistance of 106°C/W (DIP), 170°C/W (SO-8), and 204°C/W (MSOP) junction to ambient.**Note 4:** Supply current when output high typically 1 mA less at V<sub>CC</sub> = 5V.**Note 5:** Tested at V<sub>CC</sub> = 5V and V<sub>CC</sub> = 15V.**Note 6:** This will determine the maximum value of R<sub>A</sub> + R<sub>B</sub> for 15V operation. The maximum total (R<sub>A</sub> + R<sub>B</sub>) is 20MΩ.**Note 7:** No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.**Note 8:** Refer to RETS555X drawing of military LM555H and LM555J versions for specifications.

## Typical Performance Characteristics

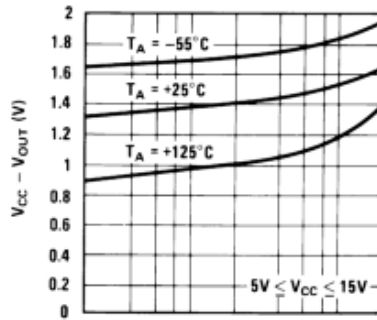
Minimum Pulse Width Required for Triggering



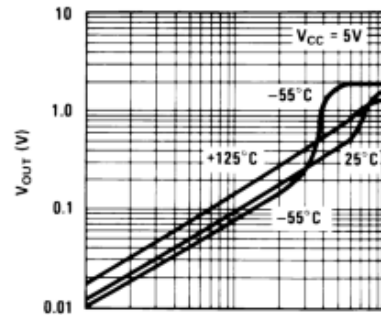
Supply Current vs. Supply Voltage



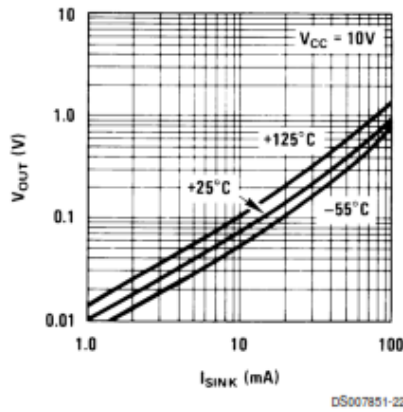
High Output Voltage vs. Output Source Current



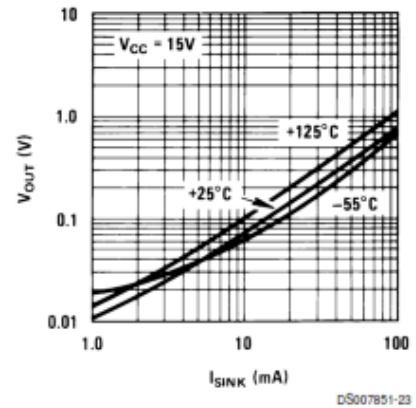
Low Output Voltage vs. Output Sink Current



Low Output Voltage vs. Output Sink Current

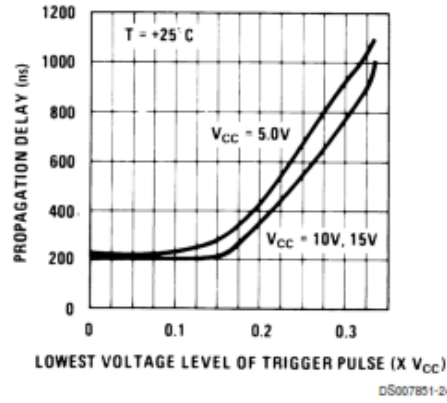


Low Output Voltage vs. Output Sink Current

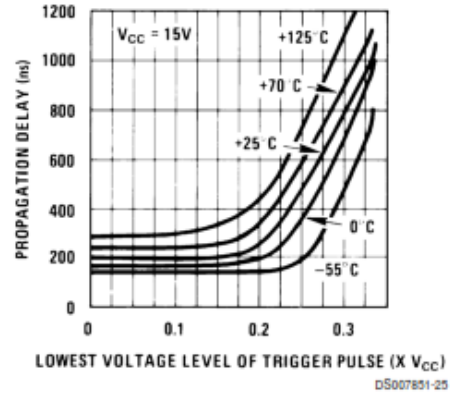


## Typical Performance Characteristics (Continued)

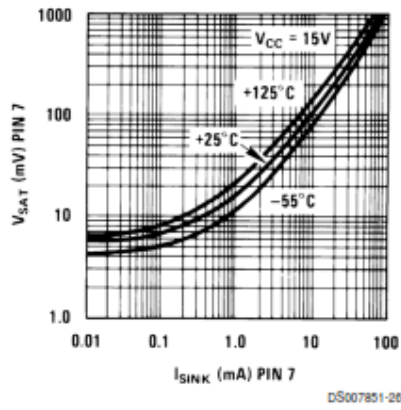
Output Propagation Delay vs. Voltage Level of Trigger Pulse



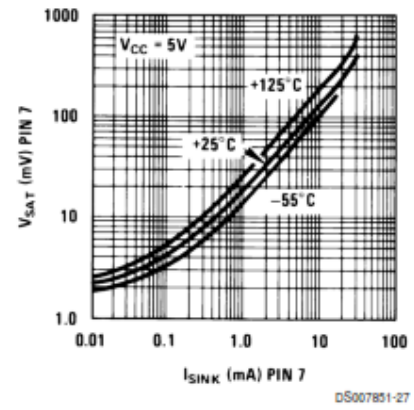
Output Propagation Delay vs. Voltage Level of Trigger Pulse



Discharge Transistor (Pin 7) Voltage vs. Sink Current



Discharge Transistor (Pin 7) Voltage vs. Sink Current



## Applications Information

### MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (Figure 1). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than  $1/3 V_{CC}$  to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

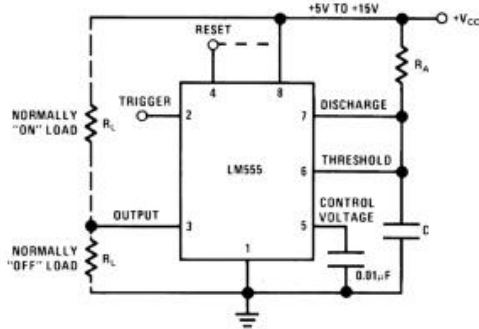
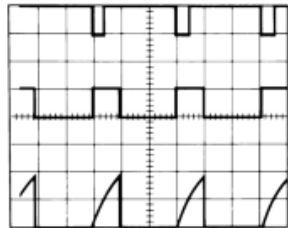


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of  $t = 1.1 R_A C$ , at the end of which time the voltage equals  $2/3 V_{CC}$ . The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. Figure 2 shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



$V_{CC} = 5V$   
 TIME = 0.1 ms/DIV.  
 $R_A = 9.1k\Omega$   
 $C = 0.01\mu F$

Top Trace: Input 5V/Div.  
 Middle Trace: Output 5V/Div.  
 Bottom Trace: Capacitor Voltage 2V/Div.

FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit so long as the trigger input is returned high at least  $10\mu s$  before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to  $V_{CC}$  to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

**NOTE:** In monostable operation, the trigger should be driven high before the end of timing cycle.

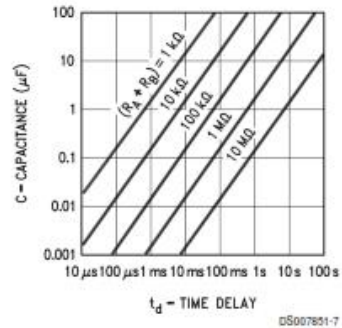


FIGURE 3. Time Delay

### ASTABLE OPERATION

If the circuit is connected as shown in Figure 4 (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through  $R_A + R_B$  and discharges through  $R_B$ . Thus the duty cycle may be precisely set by the ratio of these two resistors.

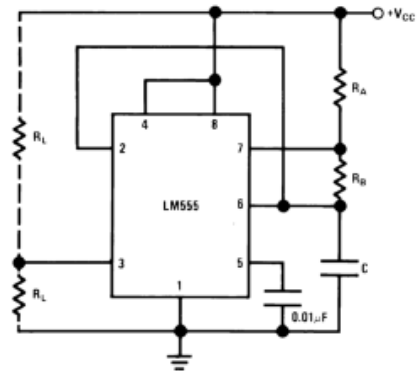
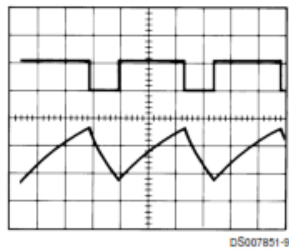


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between  $1/3 V_{CC}$  and  $2/3 V_{CC}$ . As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

### Applications Information (Continued)

Figure 5 shows the waveforms generated in this mode of operation.



DS007851-9  
 $V_{CC} = 5V$  Top Trace: Output 5V/Div.  
 TIME = 20 $\mu$ s/DIV. Bottom Trace: Capacitor Voltage 1V/Div.  
 $R_A = 3.9k\Omega$   
 $R_B = 3k\Omega$   
 $C = 0.01\mu F$

**FIGURE 5. Astable Waveforms**

The charge time (output high) is given by:  
 $t_1 = 0.693 (R_A + R_B) C$

And the discharge time (output low) by:  
 $t_2 = 0.693 (R_B) C$

Thus the total period is:  
 $T = t_1 + t_2 = 0.693 (R_A + 2R_B) C$

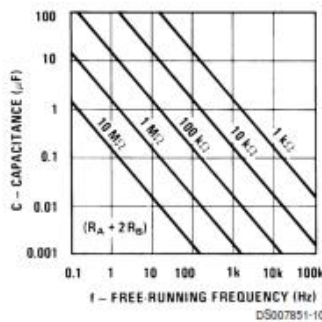
The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B) C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

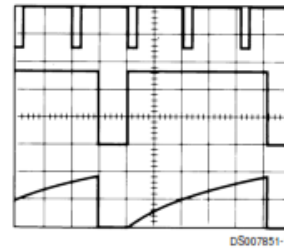
$$D = \frac{R_B}{R_A + 2R_B}$$



DS007851-10  
**FIGURE 6. Free Running Frequency**

#### FREQUENCY DIVIDER

The monostable circuit of Figure 1 can be used as a frequency divider by adjusting the length of the timing cycle. Figure 7 shows the waveforms generated in a divide by three circuit.

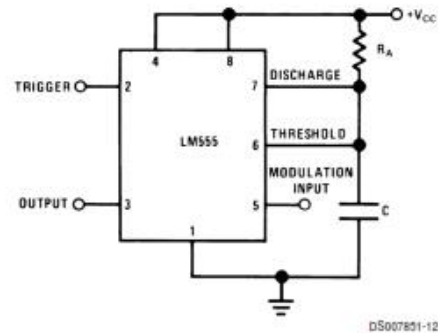


DS007851-11  
 $V_{CC} = 5V$  Top Trace: Input 4V/Div.  
 TIME = 20 $\mu$ s/DIV. Middle Trace: Output 2V/Div.  
 $R_A = 9.1k\Omega$  Bottom Trace: Capacitor 2V/Div.  
 $C = 0.01\mu F$

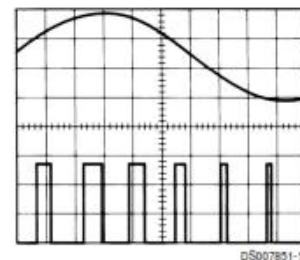
**FIGURE 7. Frequency Divider**

#### PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. Figure 8 shows the circuit, and in Figure 9 are some waveform examples.



DS007851-12  
**FIGURE 8. Pulse Width Modulator**



DS007851-13  
 $V_{CC} = 5V$  Top Trace: Modulation 1V/Div.  
 TIME = 0.2 ms/DIV. Bottom Trace: Output Voltage 2V/Div.  
 $R_A = 9.1k\Omega$   
 $C = 0.01\mu F$

**FIGURE 9. Pulse Width Modulator**



## Applications Information (Continued)

### PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

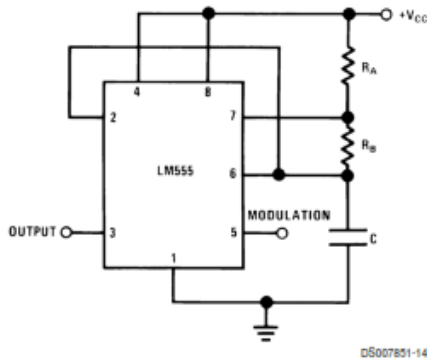
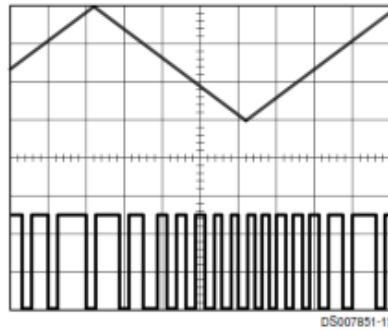


FIGURE 10. Pulse Position Modulator



$V_{CC} = 5V$   
 TIME = 0.1 ms/DIV.  
 $R_A = 3.9k\Omega$   
 $R_B = 3k\Omega$   
 $C = 0.01\mu F$

FIGURE 11. Pulse Position Modulator

### LINEAR RAMP

When the pullup resistor,  $R_A$ , in the monostable circuit is replaced by a constant current source, a linear ramp is generated. *Figure 12* shows a circuit configuration that will perform this function.

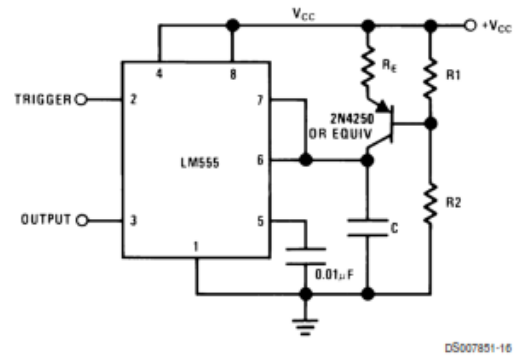
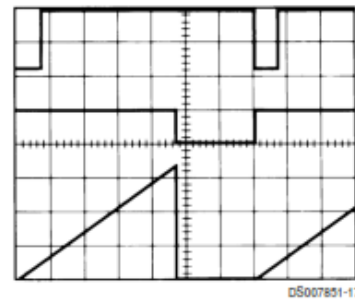


FIGURE 12.

*Figure 13* shows waveforms generated by the linear ramp. The time interval is given by:

$$T = \frac{2/3 V_{CC} R_E (R_1 + R_2) C}{R_1 V_{CC} - V_{BE} (R_1 + R_2)}$$

$V_{BE} \approx 0.6V$   
 $V_{BE} \approx 0.6V$



$V_{CC} = 5V$   
 TIME = 20µs/DIV.  
 $R_1 = 47k\Omega$   
 $R_2 = 100k\Omega$   
 $R_E = 2.7 k\Omega$   
 $C = 0.01 \mu F$

FIGURE 13. Linear Ramp

## Applications Information (Continued)

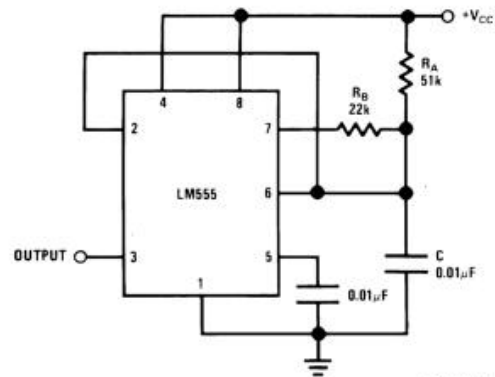
### 50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors  $R_A$  and  $R_B$  may be connected as in *Figure 14*. The time period for the output high is the same as previous,  $t_1 = 0.693 R_A C$ . For the output low it is  $t_2 =$

$$\left[ \frac{R_A R_B}{R_A + R_B} \right] C \ln \left[ \frac{R_B - 2R_A}{2R_B - R_A} \right]$$

Thus the frequency of oscillation is

$$f = \frac{1}{t_1 + t_2}$$



DS007851-18

**FIGURE 14. 50% Duty Cycle Oscillator**

Note that this circuit will not oscillate if  $R_B$  is greater than  $1/2 R_A$  because the junction of  $R_A$  and  $R_B$  cannot bring pin 2 down to  $1/3 V_{CC}$  and trigger the lower comparator.

### ADDITIONAL INFORMATION

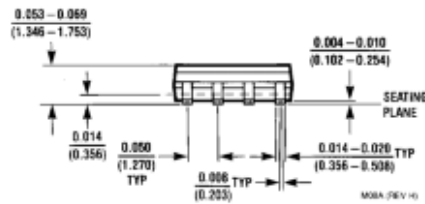
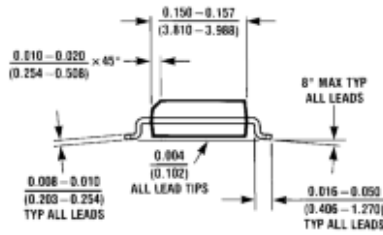
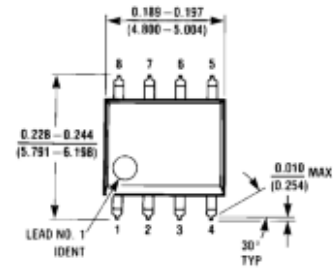
Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is  $0.1\mu\text{F}$  in parallel with  $1\mu\text{F}$  electrolytic.

Lower comparator storage time can be as long as  $10\mu\text{s}$  when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to  $10\mu\text{s}$  minimum.

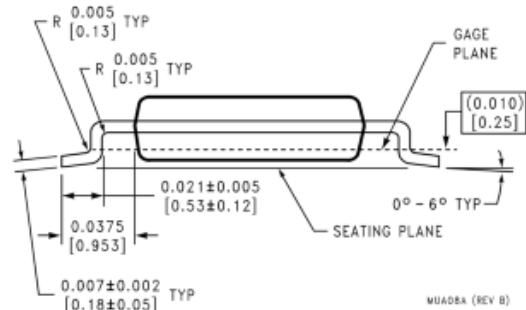
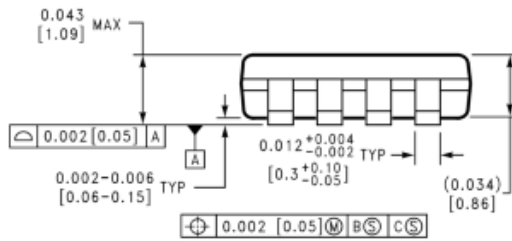
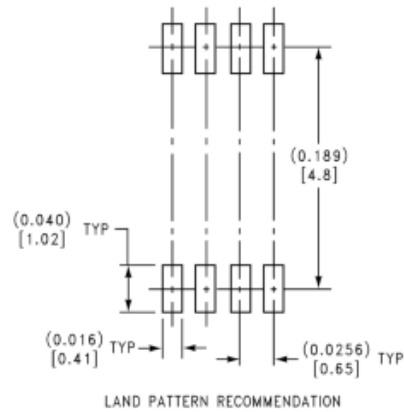
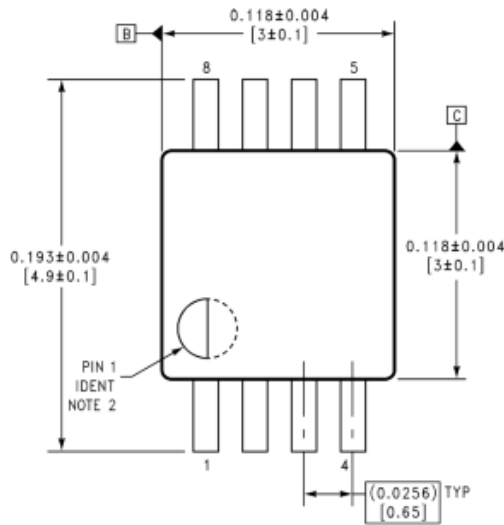
Delay time reset to output is  $0.47\mu\text{s}$  typical. Minimum reset pulse width must be  $0.3\mu\text{s}$ , typical.

Pin 7 current switches within 30ns of the output (pin 3) voltage.

**Physical Dimensions** inches (millimeters) unless otherwise noted

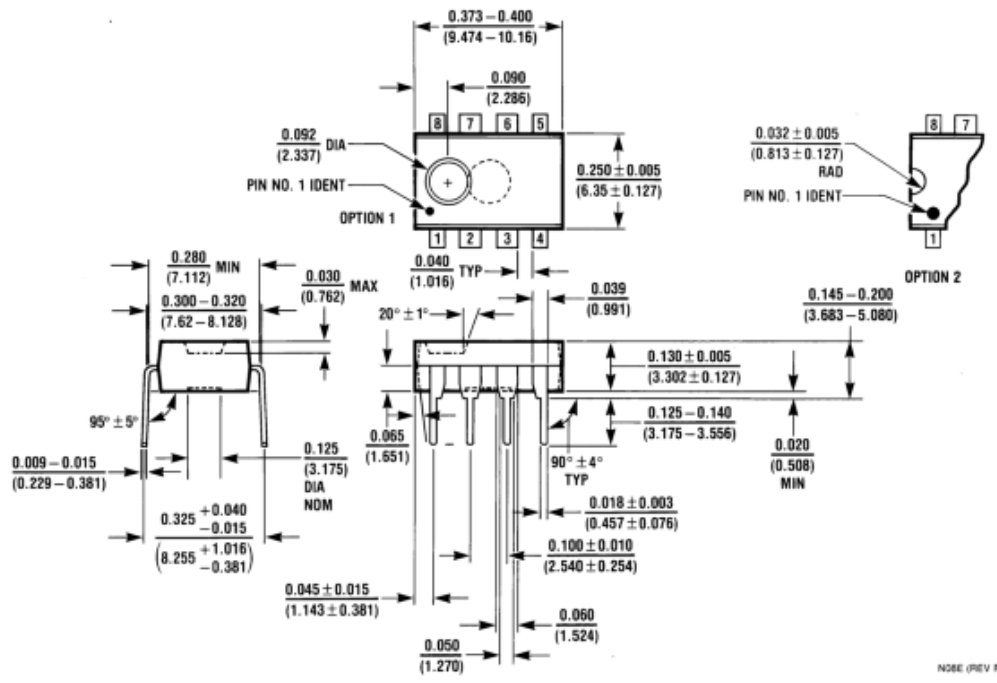


**Small Outline Package (M)**  
**NS Package Number M08A**



**8-Lead (0.118" Wide) Molded Mini Small Outline Package**  
**NS Package Number MUA08A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**Molded Dual-In-Line Package (N)**  
NS Package Number N08E

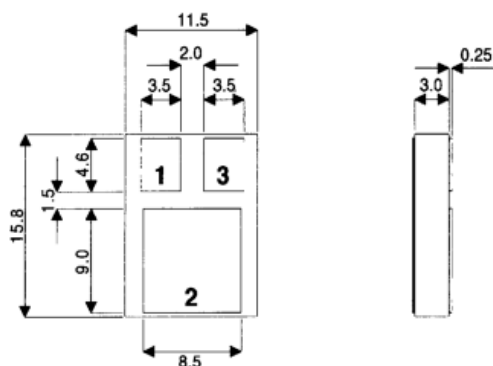
NO8E (REV F)



IRF9140SM

**MECHANICAL DATA**

Dimensions in mm (inches)

**P-CHANNEL  
POWER MOSFET**

$V_{DSS}$	-100V
$I_{D(cont)}$	-14A
$R_{DS(on)}$	0.020 $\Omega$

**FEATURES**

- HERMETICALLY SEALED SURFACE MOUNT PACKAGE
- SMALL FOOTPRINT – EFFICIENT USE OF PCB SPACE.
- SIMPLE DRIVE REQUIREMENTS
- LIGHTWEIGHT
- HIGH PACKING DENSITIES

**TO-220SM – Surface Mount Package**

Pad 1 – Gate

Pad 2 – Drain

Pad 3 – Source

**Note:** IRFNxxx also available with pins 1 and 3 reversed.

**ABSOLUTE MAXIMUM RATINGS** ( $T_{case} = 25^{\circ}C$  unless otherwise stated)

$V_{GS}$	Gate – Source Voltage	$\pm 20V$
$I_D$	Continuous Drain Current ( $V_{GS} = 0$ , $T_{case} = 25^{\circ}C$ )	-14A
$I_D$	Continuous Drain Current ( $V_{GS} = 0$ , $T_{case} = 100^{\circ}C$ )	-9.0A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	-56A
$P_D$	Power Dissipation @ $T_{case} = 25^{\circ}C$	75W
	Linear Derating Factor	0.6W/ $^{\circ}C$
$E_{AS}$	Single Pulse Avalanche Energy <sup>2</sup>	500mJ
$dv/dt$	Peak Diode Recovery <sup>3</sup>	-5.0V/ns
$T_J, T_{stg}$	Operating and Storage Temperature Range	-55 to 150 $^{\circ}C$
$T_L$	Package Mounting Surface Temperature (for 5 sec)	300 $^{\circ}C$
$R_{\theta JC}$	Thermal Resistance Junction to Case	1.67 $^{\circ}C/W$
$R_{\theta J-PCB}$	Thermal Resistance Junction to PCB (Typical)	4 $^{\circ}C/W$

**Notes**

- 1) Pulse Test: Pulse Width  $\leq 300ms$ ,  $\delta \leq 2\%$
- 2) @  $V_{DD} = -25V$ ,  $L \geq 3.8mH$ ,  $R_G = 25\Omega$ , Peak  $I_L = -14A$ , Starting  $T_J = 25^{\circ}C$
- 3) @  $I_{SD} \leq -14A$ ,  $di/dt \leq -100A/\mu s$ ,  $V_{DD} \leq BV_{DSS}$ ,  $T_J \leq 150^{\circ}C$ , SUGGESTED  $R_G = 9.1\Omega$

**ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ}\text{C}$  unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>STATIC ELECTRICAL RATINGS</b>					
$BV_{DSS}$	Drain – Source Breakdown Voltage	$V_{GS} = 0$ $I_D = -1\text{mA}$	-100		V
$\Delta BV_{DSS}$	Temperature Coefficient of Breakdown Voltage	Reference to $25^{\circ}\text{C}$ $I_D = -1\text{mA}$		-0.087	$\text{V}/^{\circ}\text{C}$
$R_{DS(on)}$	Static Drain – Source On-State Resistance <sup>1</sup>	$V_{GS} = -10\text{V}$ $I_D = -9\text{A}$		0.20	$\Omega$
		$V_{GS} = -10\text{V}$ $I_D = -14\text{A}$		0.22	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = -250\mu\text{A}$	-2	-4	V
$g_{fs}$	Forward Transconductance <sup>1</sup>	$V_{DS} \geq -15\text{V}$ $I_{DS} = -9\text{A}$	6.2		$\text{S}(\Omega)$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{GS} = 0$ $V_{DS} = 0.8BV_{DSS}$ $T_J = 125^{\circ}\text{C}$		-25	$\mu\text{A}$
				-250	
$I_{GSS}$	Forward Gate – Source Leakage	$V_{GS} = -20\text{V}$		-100	nA
$I_{GSS}$	Reverse Gate – Source Leakage	$V_{GS} = 20\text{V}$		100	

<b>DYNAMIC CHARACTERISTICS</b>					
$C_{iss}$	Input Capacitance	$V_{GS} = 0$		1400	pF
$C_{oss}$	Output Capacitance	$V_{DS} = -25\text{V}$		600	
$C_{riss}$	Reverse Transfer Capacitance	$f = 1\text{MHz}$		200	
$Q_g$	Total Gate Charge <sup>1</sup>	$V_{GS} = -10\text{V}$ $I_D = -14\text{A}$ $V_{DS} = 0.5BV_{DSS}$	31	60	nC
$Q_{gs}$	Gate – Source Charge <sup>1</sup>	$I_D = -14\text{A}$	3.7	13	nC
$Q_{gd}$	Gate – Drain ("Miller") Charge <sup>1</sup>	$V_{DS} = 0.5BV_{DSS}$	7	35.2	
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -50\text{V}$ $I_D = -14\text{A}$ $R_G = 9.1\Omega$		35	ns
$t_r$	Rise Time			85	
$t_{d(off)}$	Turn-Off Delay Time			85	
$t_f$	Fall Time			65	
<b>SOURCE – DRAIN DIODE CHARACTERISTICS</b>					
$I_S$	Continuous Source Current			-14	A
$I_{SM}$	Pulse Source Current <sup>2</sup>			-56	
$V_{SD}$	Diode Forward Voltage	$I_S = -14\text{A}$ $T_J = 25^{\circ}\text{C}$ $V_{GS} = 0$		-4.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = -14\text{A}$ $T_J = 25^{\circ}\text{C}$		280	ns
$Q_{rr}$	Reverse Recovery Charge	$d_f / d_t \leq -100\text{A}/\mu\text{s}$ $V_{DD} \leq -50\text{V}$		3.6	$\mu\text{C}$
$t_{on}$	Forward Turn-On Time		negligible		

<b>PACKAGE CHARACTERISTICS</b>					
$L_D$	Internal Drain Inductance (from centre of drain pad to die)		0.8		nH
$L_S$	Internal Source Inductance (from centre of source pad to end of source bond wire)		2.8		

**Notes**

- 1) Pulse Test: Pulse Width  $\leq 300\text{ms}$ ,  $\delta \leq 2\%$
- 2) Repetitive Rating – Pulse width limited by maximum junction temperature.

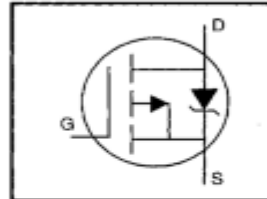
# International Rectifier

PD-9.422B

## IRF9640

HEXFET<sup>®</sup> Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- P-Channel
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements



$$V_{DSS} = -200V$$

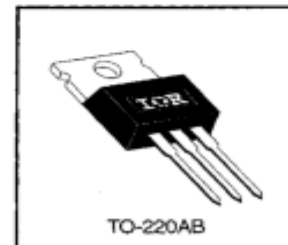
$$R_{DS(on)} = 0.50\Omega$$

$$I_D = -11A$$

### Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



### Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -10\text{ V}$	-11	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ -10\text{ V}$	-6.8	
$I_{DM}$	Pulsed Drain Current ①	-44	
$P_D$ @ $T_C = 25^\circ\text{C}$	Power Dissipation	125	W
	Linear Derating Factor	1.0	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy ②	700	mJ
$I_{AR}$	Avalanche Current ①	-11	A
$E_{AR}$	Repetitive Avalanche Energy ①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
$T_J$	Operating Junction and	-55 to +150	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf·in (1.1 N·m)	


### Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.0	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

**Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-200	—	—	V	$V_{GS}=0V$ , $I_D=-250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.20	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D=-1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.50	$\Omega$	$V_{GS}=-10V$ , $I_D=-6.6A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS}=V_{GS}$ , $I_D=-250\mu A$
$g_{fs}$	Forward Transconductance	4.1	—	—	S	$V_{DS}=-50V$ , $I_D=-6.6A$ ④
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	-100	$\mu A$	$V_{DS}=200V$ , $V_{GS}=0V$
		—	—	-500		$V_{DS}=-160V$ , $V_{GS}=0V$ , $T_J=125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{DS}=-20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS}=20V$
$Q_g$	Total Gate Charge	—	—	44	nC	$I_D=-11A$
$Q_{gs}$	Gate-to-Source Charge	—	—	7.1		$V_{DS}=-160V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	27		$V_{GS}=-10V$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	$V_{DD}=-100V$
$t_r$	Rise Time	—	43	—		$I_D=-11A$
$t_{d(off)}$	Turn-Off Delay Time	—	39	—		$R_G=9.1\Omega$
$t_f$	Fall Time	—	38	—		$R_D=8.6\Omega$ See Figure 10 ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	1200	—	pF	$V_{DS}=0V$
$C_{oss}$	Output Capacitance	—	370	—		$V_{GS}=-25V$
$C_{rss}$	Reverse Transfer Capacitance	—	81	—		$f=1.0\text{MHz}$ See Figure 5

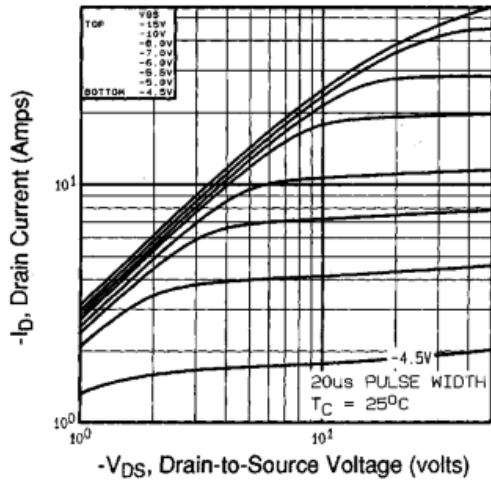
**Source-Drain Ratings and Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	-11	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	-44		
$V_{SD}$	Diode Forward Voltage	—	—	-5.0	V	$T_J=25^\circ\text{C}$ , $I_S=-11A$ , $V_{GS}=0V$ ④
$t_{rr}$	Reverse Recovery Time	—	250	300	ns	$T_J=25^\circ\text{C}$ , $I_F=-11A$
$Q_{rr}$	Reverse Recovery Charge	—	2.9	3.6	$\mu C$	$di/dt=100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

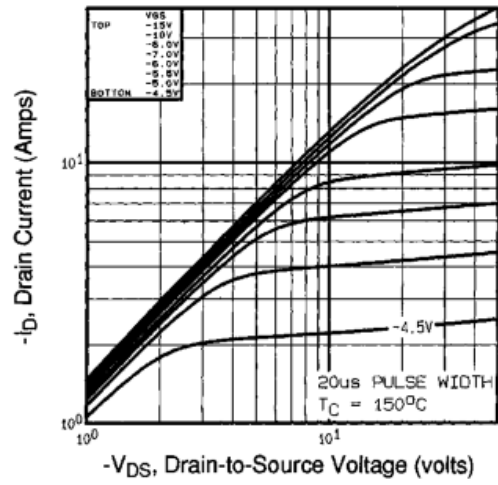
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ②  $V_{DD}=-50V$ , starting  $T_J=25^\circ\text{C}$ ,  $L=8.7\text{mH}$ ,  $R_G=25\Omega$ ,  $I_{AS}=-11A$  (See Figure 12)
- ③  $I_{SD}\leq 11A$ ,  $di/dt\leq 150A/\mu s$ ,  $V_{DD}\leq V_{(BR)DSS}$ ,  $T_J\leq 150^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .

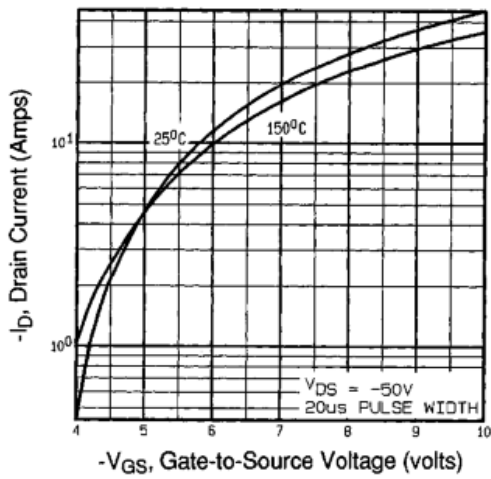




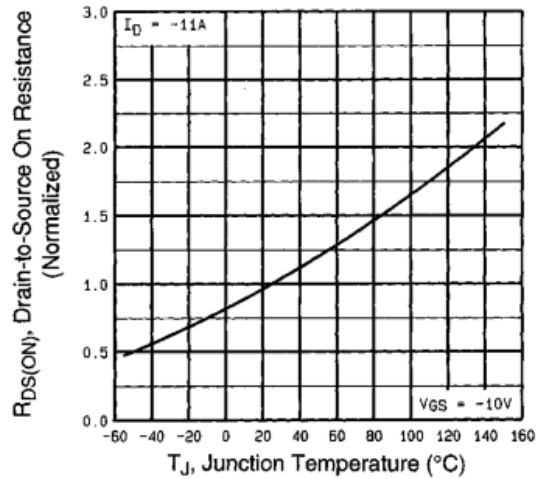
**Fig 1.** Typical Output Characteristics,  $T_C=25^\circ\text{C}$



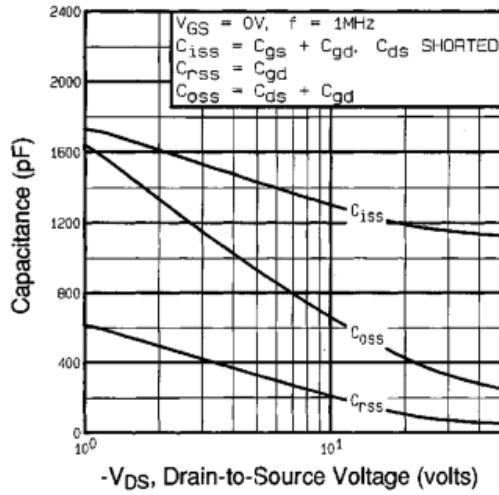
**Fig 2.** Typical Output Characteristics,  $T_C=150^\circ\text{C}$



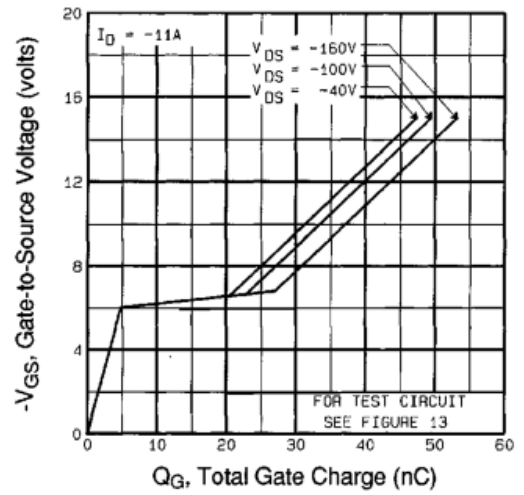
**Fig 3.** Typical Transfer Characteristics



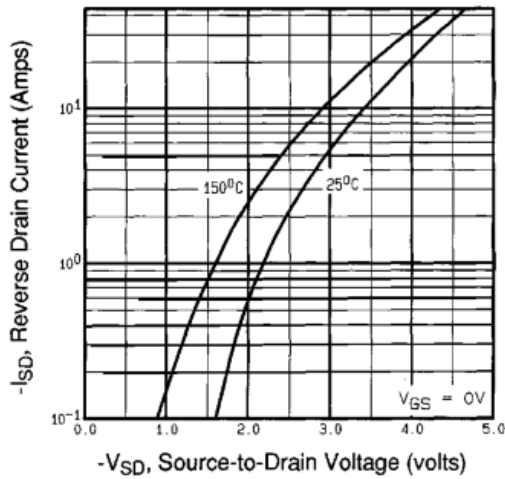
**Fig 4.** Normalized On-Resistance Vs. Temperature



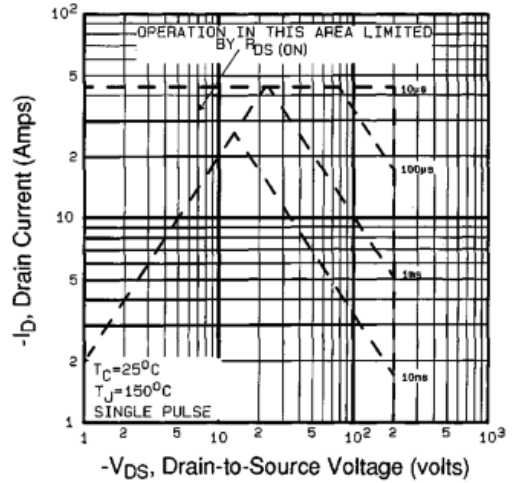
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

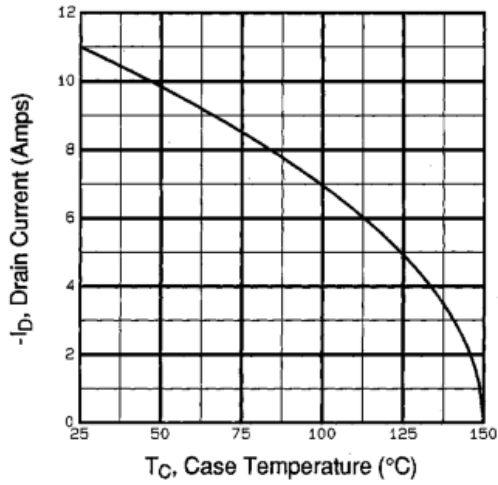


Fig 9. Maximum Drain Current Vs. Case Temperature

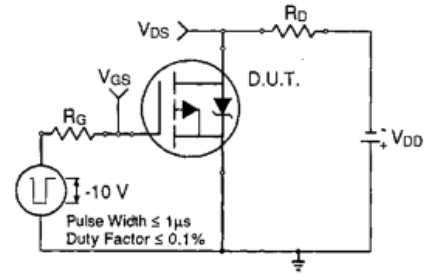


Fig 10a. Switching Time Test Circuit

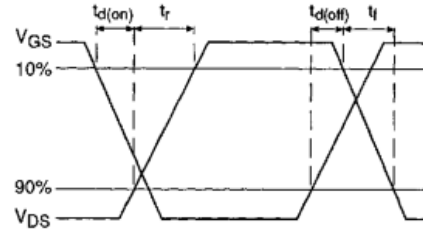


Fig 10b. Switching Time Waveforms

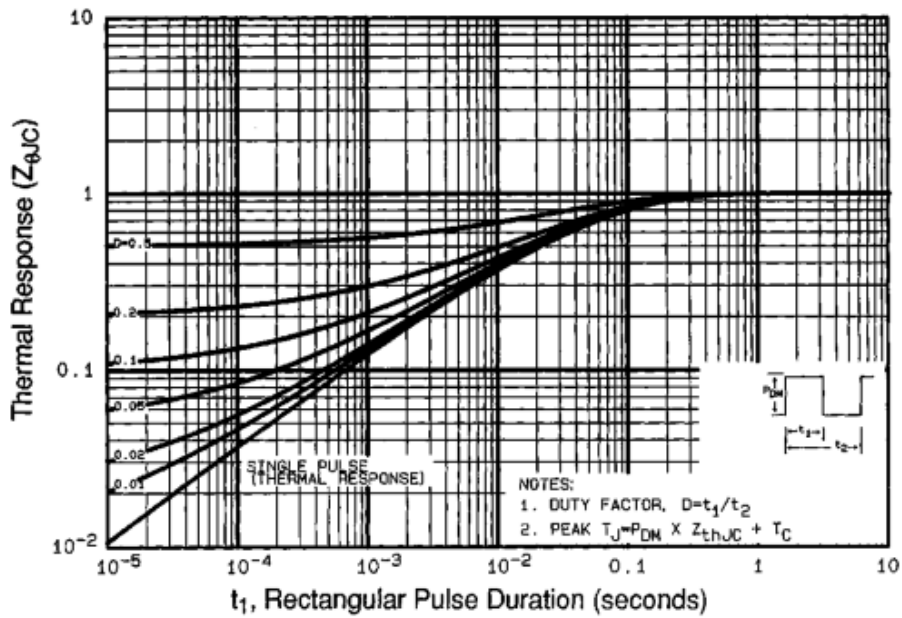


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

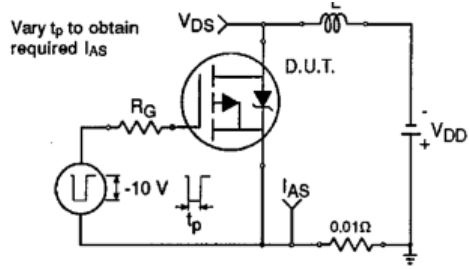


Fig 12a. Unclamped Inductive Test Circuit

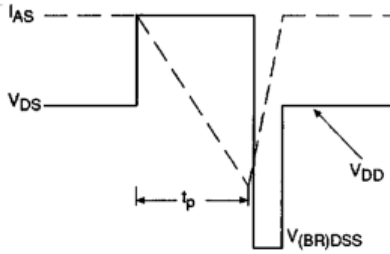


Fig 12b. Unclamped Inductive Waveforms

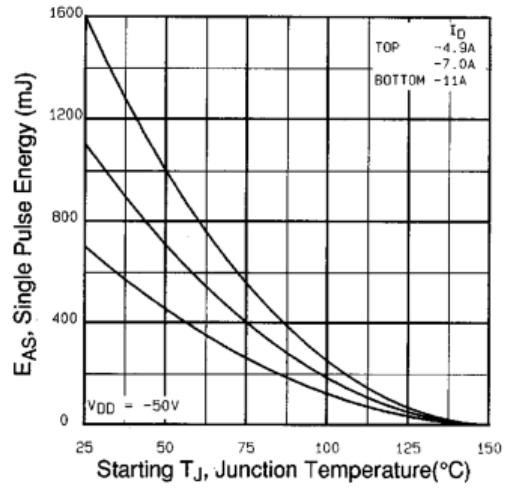


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

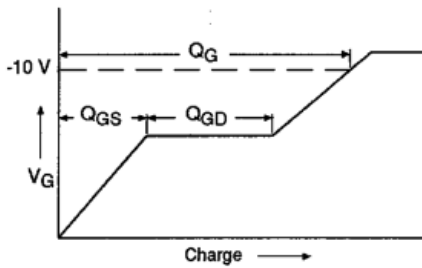


Fig 13a. Basic Gate Charge Waveform

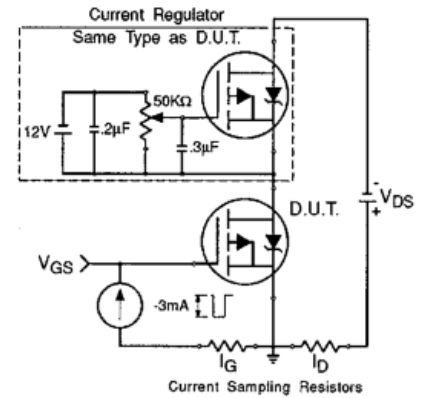


Fig 13b. Gate Charge Test Circuit

International  
**IR** Rectifier

PD-94526A

AUTOMOTIVE MOSFET

**IRF1503****Typical Applications**

- 14V Automotive Electrical Systems
- 14V Electronic Power Steering

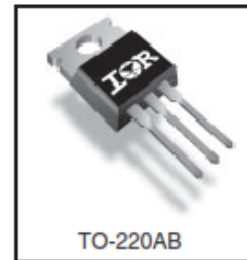
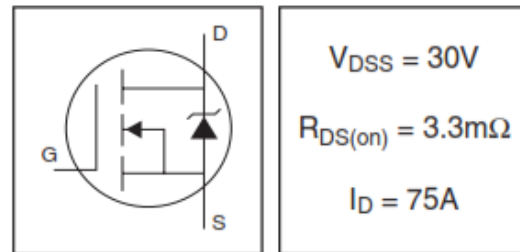
**Features**

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

**Description**

Specifically designed for Automotive applications, this design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this HEXFET power MOSFET are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

## HEXFET® Power MOSFET



TO-220AB

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V (Silicon limited)	240	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V (See Fig.9)	170	
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V (Package limited)	75	
$I_{DM}$	Pulsed Drain Current ①	960	
$P_D$ @ $T_C = 25^\circ\text{C}$	Power Dissipation	330	W
	Linear Derating Factor	2.2	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$E_{AS}$	Single Pulse Avalanche Energy ②	510	mJ
$E_{AS}$ (tested)	Single Pulse Avalanche Energy Tested Value ②	980	
$I_{AR}$	Avalanche Current ①	See Fig.12a, 12b, 15, 16	A
$E_{AR}$	Repetitive Avalanche Energy ③		mJ
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

**Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

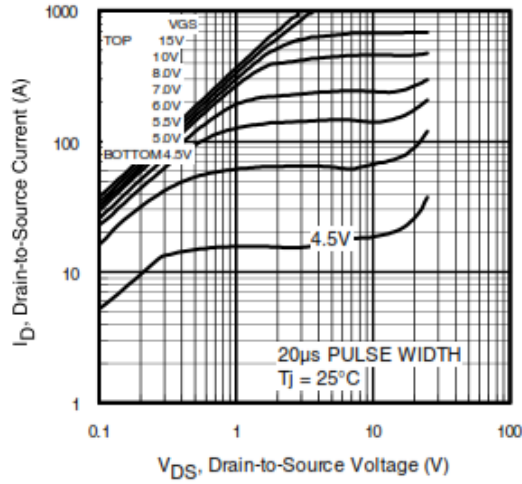
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.028	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.6	3.3	m $\Omega$	$V_{GS} = 10V, I_D = 140A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = 10V, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	75	—	—	S	$V_{DS} = 25V, I_D = 140A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 30V, V_{GS} = 0V$ $V_{DS} = 30V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200	nA	$V_{GS} = -20V$
$Q_g$	Total Gate Charge	—	130	200	nC	$I_D = 140A$
$Q_{gs}$	Gate-to-Source Charge	—	36	54	nC	$V_{DS} = 24V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	41	62	nC	$V_{GS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	$V_{DD} = 15V$ $I_D = 140A$ $R_G = 2.5\Omega$ $V_{GS} = 10V$ ③
$t_r$	Rise Time	—	130	—		
$t_{d(off)}$	Turn-Off Delay Time	—	59	—		
$t_f$	Fall Time	—	48	—		
$L_D$	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	13	—		
$C_{ISS}$	Input Capacitance	—	5730	—	pF	$V_{GS} = 0V$
$C_{OSS}$	Output Capacitance	—	2250	—		$V_{DS} = 25V$
$C_{RSS}$	Reverse Transfer Capacitance	—	290	—		$f = 1.0MHz$ , See Fig. 5
$C_{OSS}$	Output Capacitance	—	7580	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
$C_{OSS}$	Output Capacitance	—	2290	—		$V_{GS} = 0V, V_{DS} = 24V, f = 1.0MHz$
$C_{OSS\ eff.}$	Effective Output Capacitance ④	—	3420	—		$V_{GS} = 0V, V_{DS} = 0V$ to $24V$

**Source-Drain Ratings and Characteristics**

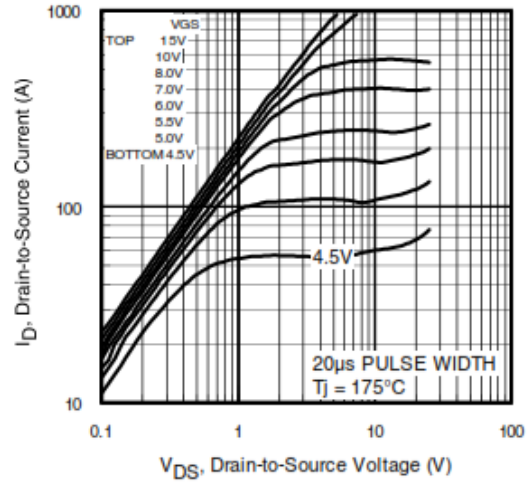
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	240	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	960		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 140A, V_{GS} = 0V$ ②
$t_{rr}$	Reverse Recovery Time	—	71	110	ns	$T_J = 25^\circ\text{C}, I_F = 140A, V_{DD} = 15V$
$Q_{rr}$	Reverse Recovery Charge	—	110	170	nC	$di/dt = 100A/\mu s$ ③
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

**Notes:**

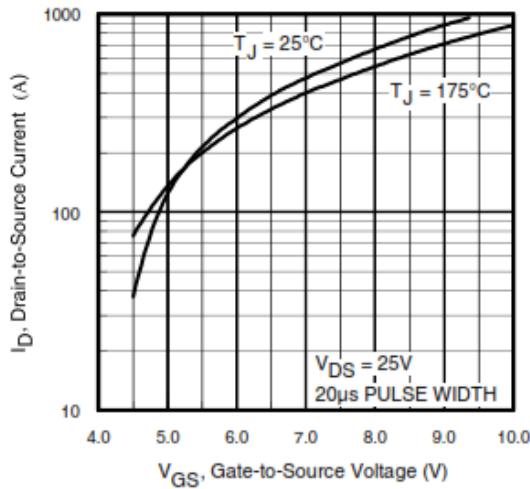
- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.049mH$   
 $R_G = 25\Omega, I_{AS} = 140A$ . (See Figure 12).
- ③ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .
- ④  $C_{OSS\ eff.}$  is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑤ Limited by  $T_{Jmax}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.



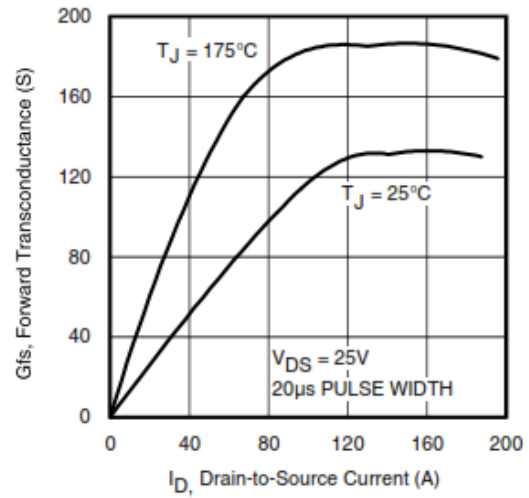
**Fig 1.** Typical Output Characteristics



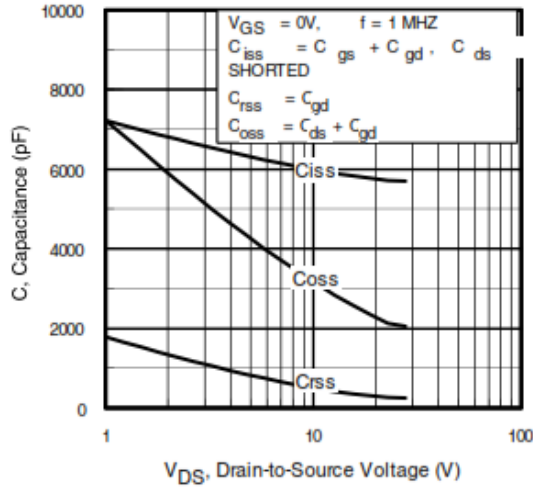
**Fig 2.** Typical Output Characteristics



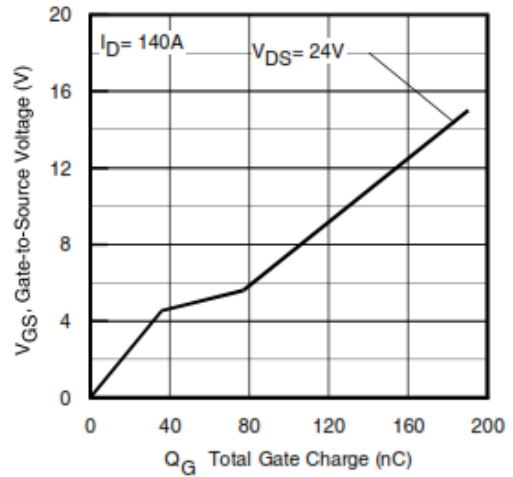
**Fig 3.** Typical Transfer Characteristics



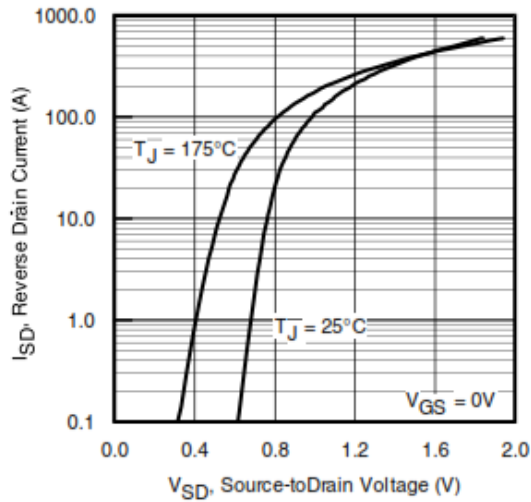
**Fig 4.** Typical Forward Transconductance Vs. Drain Current



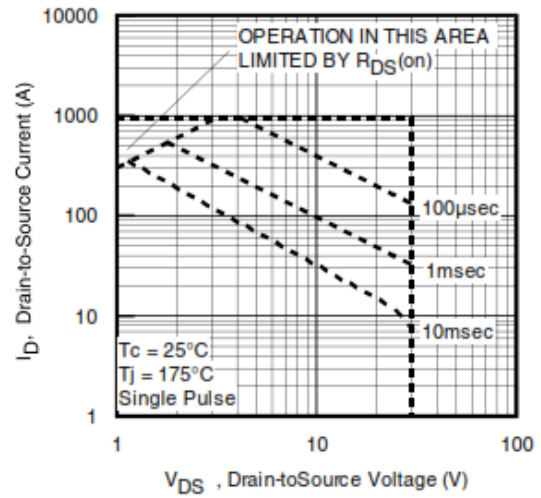
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

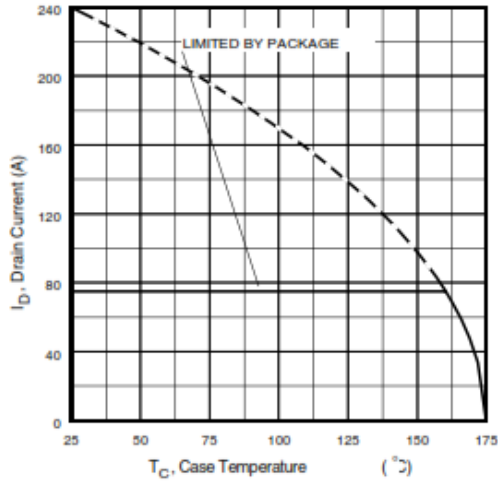


**Fig 7.** Typical Source-Drain Diode Forward Voltage

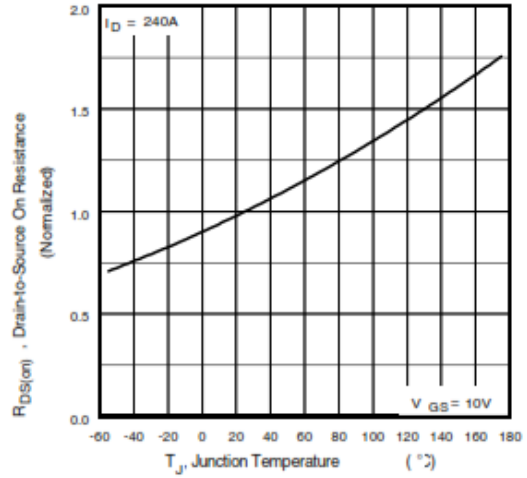


**Fig 8.** Maximum Safe Operating Area

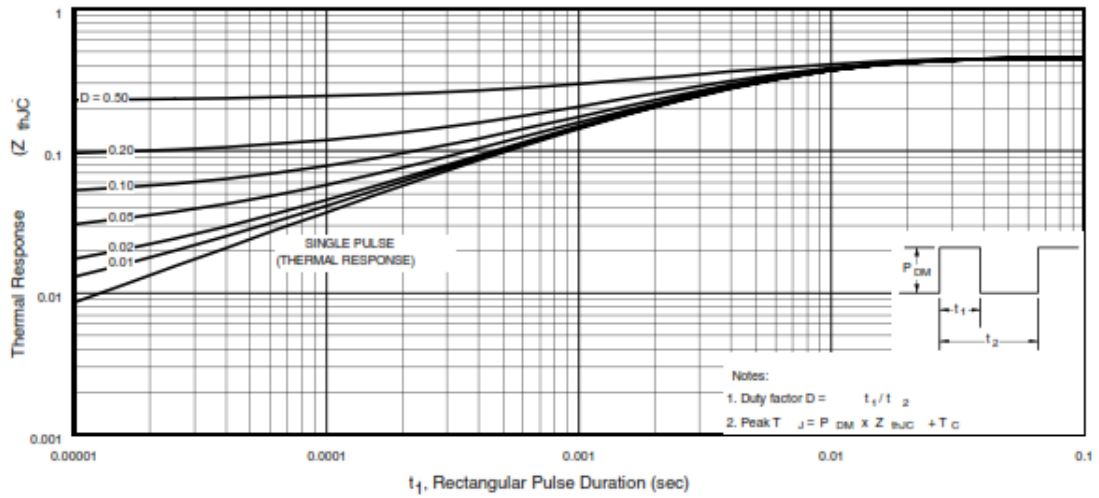




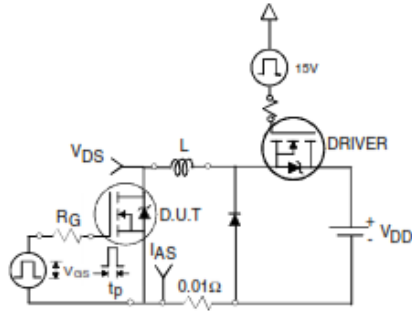
**Fig 9.** Maximum Drain Current Vs. Case Temperature



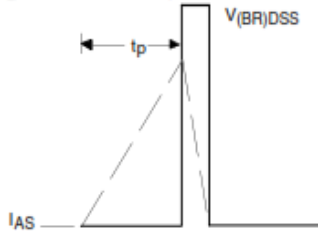
**Fig 10.** Normalized On-Resistance Vs. Temperature



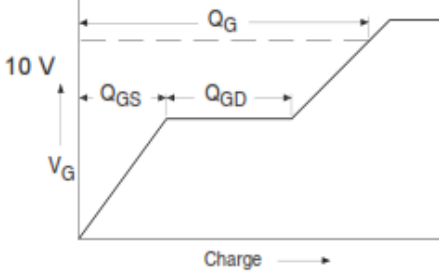
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



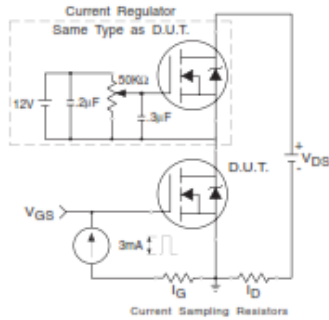
**Fig 12a.** Unclamped Inductive Test Circuit



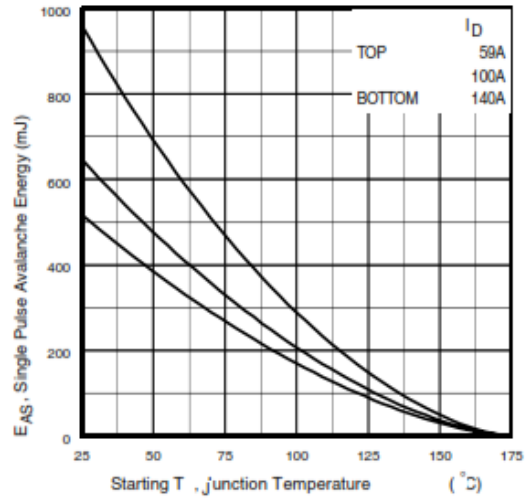
**Fig 12b.** Unclamped Inductive Waveforms



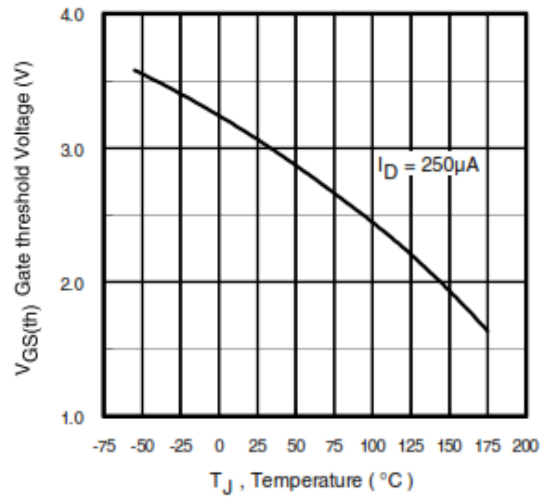
**Fig 13a.** Basic Gate Charge Waveform



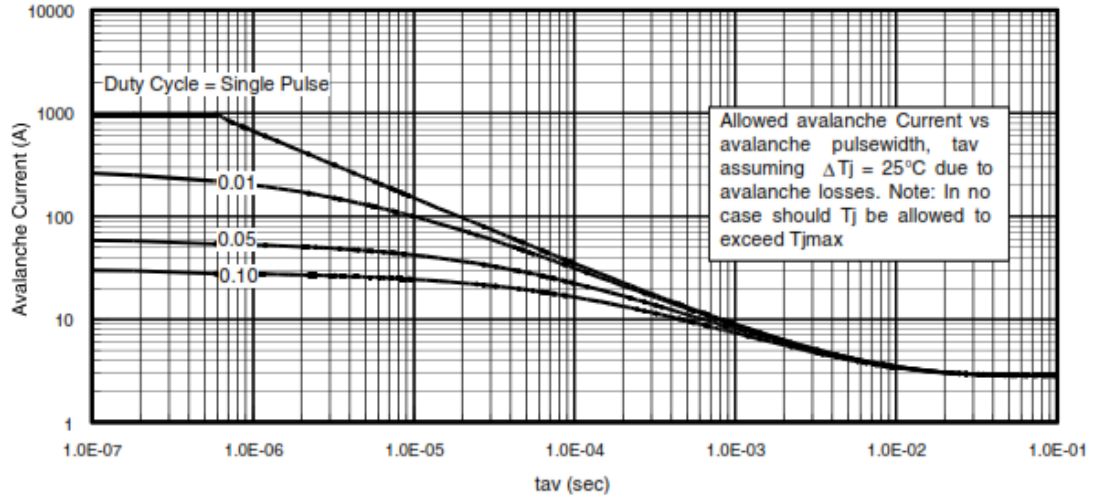
**Fig 13b.** Gate Charge Test Circuit



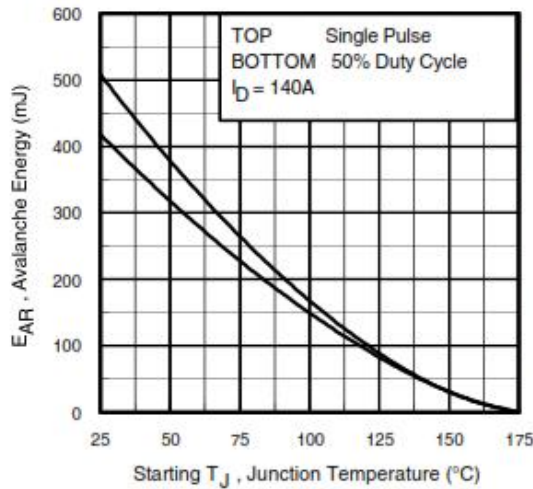
**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 14.** Threshold Voltage Vs. Temperature



**Fig 15. Typical Avalanche Current Vs.Pulsewidth**



**Fig 16. Maximum Avalanche Energy Vs. Temperature**

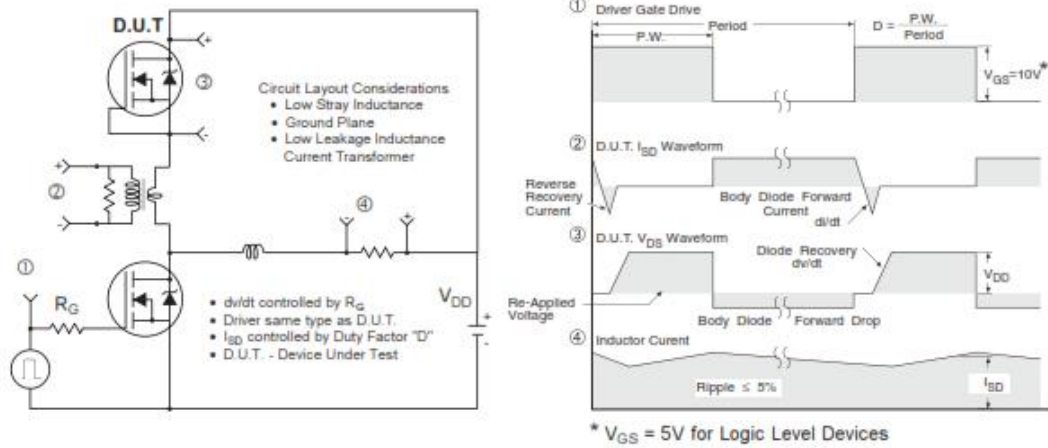
**Notes on Repetitive Avalanche Curves , Figures 15, 16:**  
 (For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
 Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

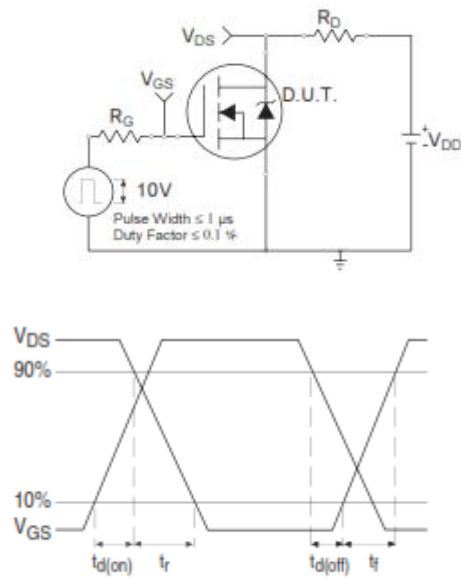
$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2 \Delta T / [ 1.3 \cdot BV \cdot Z_{thJC} ]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



**Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**

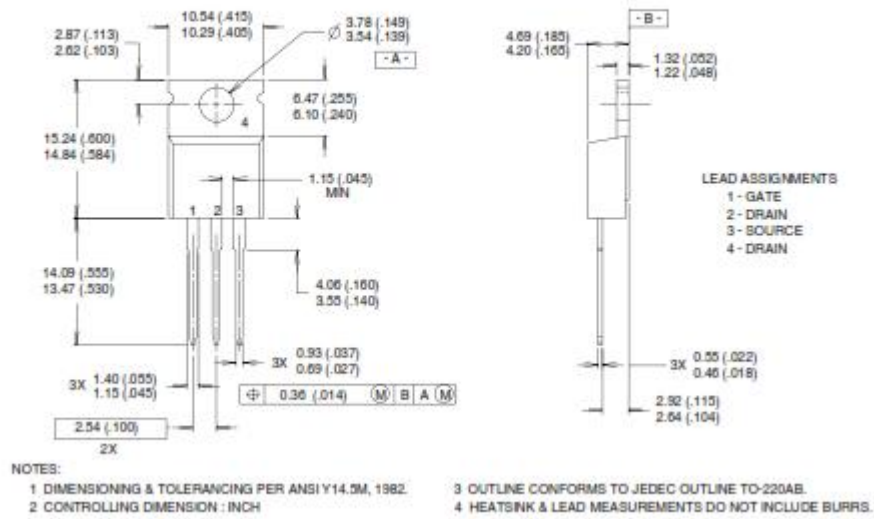


**Fig 18b. Switching Time Waveforms**

## Package Outline

### TO-220AB

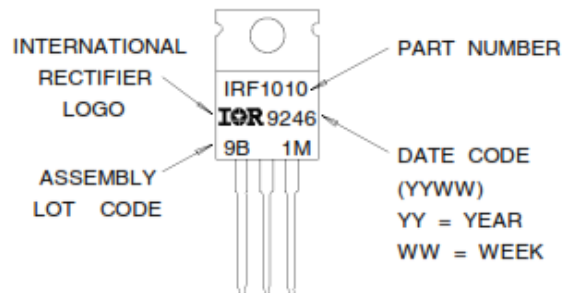
Dimensions are shown in millimeters (inches)



## Part Marking Information

### TO-220AB

EXAMPLE : THIS IS AN IRF1010  
 WITH ASSEMBLY  
 LOT CODE 9B1M



**TO-220AB package is not recommended for Surface Mount Application.**

Data and specifications subject to change without notice.  
 This product has been designed and qualified for Automotive [Q101] market.  
 Qualification Standards can be found on IR's Web site.

**1N4148**

Vishay Semiconductors

## Small Signal Fast Switching Diodes

### Features

- Silicon epitaxial planar diodes
- Electrically equivalent diodes:  
1N4148 - 1N914
- Compliant to RoHS Directive 2002/95/EC and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21 definition



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



94 9367

### Applications

- Extreme fast switches

### Mechanical Data

**Case:** DO-35

**Weight:** approx. 105 mg

**Cathode band color:** black

**Packaging codes/options:**

TR/10K per 13" reel (52 mm tape), 50K/box

TAP/10K per ammpack (52 mm tape), 50K/box

### Parts Table

Part	Ordering code	Type marking	Remarks
1N4148	1N4148-TAP or 1N4148-TR	V4148	Ampmpack/tape and reel

### Absolute Maximum Ratings

$T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified

Parameter	Test condition	Symbol	Value	Unit
Repetitive peak reverse voltage		$V_{RRM}$	100	V
Reverse voltage		$V_R$	75	V
Peak forward surge current	$t_p = 1\text{ }\mu\text{s}$	$I_{FSM}$	2	A
Repetitive peak forward current		$I_{FRM}$	500	mA
Forward continuous current		$I_F$	300	mA
Average forward current	$V_R = 0$	$I_{FAV}$	150	mA
Power dissipation	$l = 4\text{ mm}, T_L = 45\text{ }^{\circ}\text{C}$	$P_{tot}$	440	mW
	$l = 4\text{ mm}, T_L \leq 25\text{ }^{\circ}\text{C}$	$P_{tot}$	500	mW

### Thermal Characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified

Parameter	Test condition	Symbol	Value	Unit
Thermal resistance junction to ambient air	$l = 4\text{ mm}, T_L = \text{constant}$	$R_{thJA}$	350	K/W
Junction temperature		$T_j$	175	$^{\circ}\text{C}$
Storage temperature range		$T_{slg}$	- 65 to + 150	$^{\circ}\text{C}$

**Electrical Characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified

Parameter	Test condition	Symbol	Min.	Typ.	Max.	Unit
Forward voltage	$I_F = 10\text{ mA}$	$V_F$			1000	mV
Reverse current	$V_R = 20\text{ V}$	$I_R$			25	nA
	$V_R = 20\text{ V}, T_j = 150\text{ }^{\circ}\text{C}$	$I_R$			50	$\mu\text{A}$
Reverse current	$V_R = 75\text{ V}$	$I_R$			5	$\mu\text{A}$
	$I_R = 100\text{ }\mu\text{A}, t_p/T = 0.01, t_p = 0.3\text{ ms}$	$V_{(BR)}$	100			V
Diode capacitance	$V_R = 0, f = 1\text{ MHz}, V_{HF} = 50\text{ mV}$	$C_D$			4	pF
Rectification efficiency	$V_{HF} = 2\text{ V}, f = 100\text{ MHz}$	$\eta_r$	45			%
Reverse recovery time	$I_F = I_R = 10\text{ mA}, i_R = 1\text{ mA}$	$t_{rr}$			8	ns
	$I_F = 10\text{ mA}, V_R = 6\text{ V}, i_R = 0.1 \times I_R, R_L = 100\text{ }\Omega$	$t_{rr}$			4	ns

**Typical Characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified

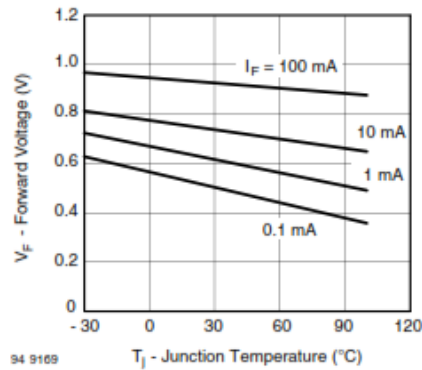


Figure 1. Forward Voltage vs. Junction Temperature

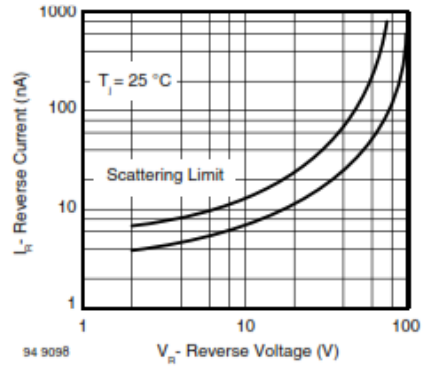


Figure 3. Reverse Current vs. Reverse Voltage

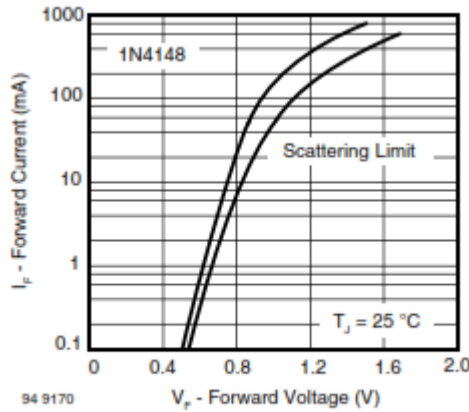
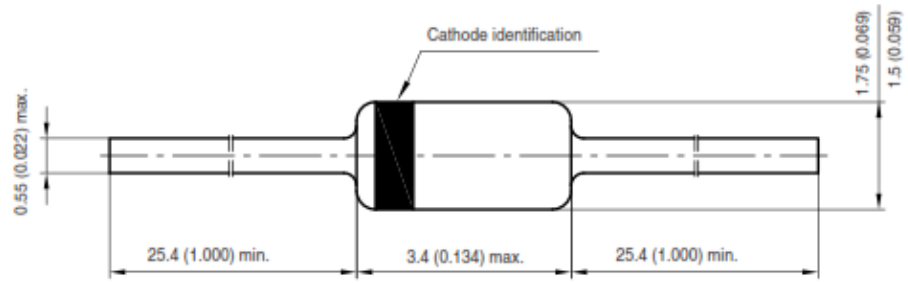


Figure 2. Forward Current vs. Forward Voltage

**Package Dimensions** in millimeters (inches): **DO-35\_02**

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