PI CONTROLLER FOR BATTERY CHARGER SYSTEMS

MOHD AZHAR BIN AZMI

UNIVERSITI MALAYSIA PAHANG

# UNIVERSITI MALAYSIA PAHANG

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JUDUL: <u>PI CONTROLLE</u>	JUDUL: <u>PI CONTROLLER FOR BATTERY CHARGER SYSTEM</u>		
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"I hereby acknowledge that the scope and quality of this thesis is qualified for the award of the Bachelor Degree of Electrical Engineering (Electronics)"

Signature	:		
Name	: <u>RAJA MOHD TAUFIKA BIN RAJA ISMAIL</u>		
Date	: 17 NOVEMBER 2008		

## PI CONTROLLER FOR BATTERY CHARGER SYSTEM

MOHD AZHAR BIN AZMI

This thesis is submitted as partial fulfillment of the requirements for the award of Bachelor of Electrical Engineering (Hons.) (Electronics)

Faculty of Electrical & Electronics Engineering Universiti Malayasia Pahang

NOVEMBER 2008

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Author	: MOHD AZHAR BIN AZMI
Date	: <u>17 NOVEMBER 2008</u>

To my beloved mother and father, Faridah Bt Che Hamat, Azmi Bin Ibrahim.

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#### ABSTRACT

There are many type of battery charger that had been developed for century. However there are also many charger that not suitable to use due to the method of charging and the safety during the charging process. Normally the charger will automatically charge the battery pack when it is connected to the charger, but it keeps charging even though the battery is fully charged. This situation can damage the battery itself or the user if explosion occur during the process. Beside that, the lifetime of the battery is also important. A good charging method can increase the lifetime of the battery. PI controller can control the output voltage from the charger to meet a desire value by controlling the rise time of the current, overshoot and error that occur during charging process. The Proportional (P) action will decrease the rise time and decrease error while Integral (I) action will eliminate the error occur. This project is developed to investigate the action of PI controller to the output from battery charger.

#### ABSTRAK

Sejak dulu lagi terdapat banyak pengecas bateri yang telah dicipta. Walaubagaimanapun, masih terdapat banyak pengecas yang tidak sesuai digunakan berdasarkan kaedah mengecas dan keselamatan semasa proces mengecas berlangsung. Kebiasaannya pengecas ini akan mengecas bateri secara automatik apabila bateri disambaungkan pada pengecas, tetapi ia tetap mengecas bateri tersebut walaupun ia telah dicas sepenuhnya. Keadaan ini akan menyebabkan kerosakan pada bateri tersebut dan juga membahayakan pengguna sekiranya berlaku letupan akibat terlebih cas. Selain itu, jangka hayat bateri tersebut juga amat penting. Kaedah mengecas yang baik boleh meningkatkan lagi jangka hayat bateri. PI controller boleh mengawal keluaran dari pengecas dengan mengawal "rise time", "overshoot" dan juga kesilapan yang berlaku semasa proces mengecas dijalankan. Proportional (P) akan memberi kesan dengan mengurangkan "rise time" manakala Integral (I) akan menghapuskan sebarang ketidakstabilan yang berlaku. Projek ini amat berguna untuk tujuan sistem kawalan.

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## LIST OF SYMBOLS

С	-	Capacitor
D	-	Duty cycle
DC	-	Direct Current
$D_m$	-	Freewheeling diode
f	-	Frequency
G(s)	-	Transfer function
$i_o, I_a$	-	Output current
$i_c, I_c$	-	Capacitor current
$i_L, I_L$	-	Inductor current
$i_s, I_s$	-	Input current
IC	-	Integrated Circuit
$K_d$	-	Derivative gain
kHz	-	kilo Hertz
$K_i$	-	Integral gain
$K_p$	-	Proportional gain
L	-	Inductor
mH	-	mili Henry
MHz	-	mega Hertz
MOSFET	-	metal-oxide-semiconductor field-effect transistor
ms	-	mili second
Q, M	-	Transistor
R	-	Resistor
rad/s		radians per second
<i>t</i> , <i>T</i>	-	time
V	-	Volt
$V_{o,} V_a$	-	Output voltage

$V_c$	-	Capacitor voltage
VLSI	-	Very-large-scale-integration
$V_s$	-	Input voltage
μF	-	micro Farad
μs	-	micro second
Ω	-	Ohm

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### **CHAPTER 1**

#### **INTRODUCTION**

#### 1.1 Introduction

This chapter will explain about the overview of battery charger, Proportional-Integral (PI) controller, objective of the project, project scope and the thesis outlines. This project is useful for control purpose.

### **1.2** Objective of the Project

The main objective of this project is to develop a PI controller for a battery charger to control the transient response of the system. Beside, this project is about to investigate the action of the PI controller to the output response of the battery charger.

## **1.3** Scope of the Project

This project is focus on the PI controller from developing to attaching it to a battery charger. Although the scope is to focus on PI controller, but a battery charger designing is required whether a simple battery charger or advance. So a DC-DC buck converter is developed as the battery charger.

#### **1.4 Problem Statement**

Today's technologies had shown a drastic changing in all section due to its developments. Many systems had been created for this purpose. In the battery industries, there are lot of battery charger that been developed to drive a good charging process. However there are still many chargers that are not suitable to use that may damage the battery itself or the user. A bad charging process may shorten the lifetime of the battery and more dangerous is the battery may explode. A control system should be developed to overcome this problem.

### 1.5 Project Background

This section describe about an overview of battery charger system and PID controller.

#### **1.5.1** Overview of Battery Charger

A battery charger is a device used to recharge the rechargeable battery. There are many types of battery charger that have been developed based on the global usage of battery source. A battery charger consists of simple battery charger, trickle, timer-based, intelligent and fast battery charger. A simple battery charger works by connecting the DC power source to the cell or battery that being charge and normally takes a long time to finish the charging process.

In this situation, an over charging might occur due to unmonitored process. Trickle battery charger used a simple battery charger that charges the battery slowly at the self-discharge rate. By leaving a battery in a trickle charger will keep the battery top-up without over charging occur. A timer-based battery charger will operate due to the pre-determine time. Usually this charger has been set to operate with a specific battery type according to a charging time. An intelligent battery charger can monitor the charging process by monitoring the battery voltage, temperature, and time under charge to determine the optimum current at that instant. When the combination of voltage, temperature, and time indicate that the battery had been fully charged then the charging process will stop.

Nowadays, a lot of equipment are using the battery source and there many issue occur related to charging process and the normal issue is over charging and the battery life is shorten that it suppose to be. Beside the monitoring the charging process, we should aware about charging technique. A bad charging technique may cause over charging and also shorten the lifetime of the battery. There are three step that drive to a good charging process which is getting the charge into the battery (charging), optimizing the charging rate (stabilizing), and know when to stop the charging process (terminating).

#### 1.5.2 Overview of Proportional-Integral-Derivative (PID) Controller

The term Proportional-Integral-Derivative (PID) and Fuzzy-Logic is very popular and always being used in control system. PID controller consists of three control action which is Proportional action, Integral action, and Derivative action. The proportional action will have the effect of reducing the rise time and steady-state error but never eliminate this error. The Integral action will eliminate the steady-state error but it may make the transient response become worse. The Derivative action will increase the stability of the system, reducing the overshoot, and improving the transient response.

#### 1.5.3 Basic Form of PI controlled Battery Charger

Basically the form of battery charger consists of rectifier and regulator however for this PI controlled battery charger it's consist of rectifier, DC-DC converter (regulator), and PI controller. The Figure 1.1 shows the form of this battery charger.

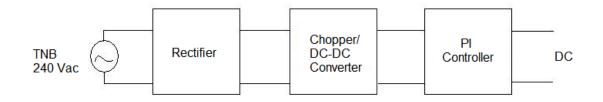


Figure 1.1: Basic Form of PI controlled Battery Charger

#### 1.6 Thesis outline

This thesis consists of five chapters. Chapter 1 illustrate about the objective and the scope of the project, problem statement, and the background of the project.

Chapter 2 will review about the DC-DC buck converter and its operation and further explanation about PID controller.

Chapter 3 will explain about the methodology of the project including modeling and designing the DC-DC Buck Converter, PI controller, and the complete circuitry.

Chapter 4 will discuss about all the result from simulation and hardware result.

Chapter 5 will discuss about the conclusion from this project and also the recommendation for future development and modification.

#### **CHAPTER 2**

#### LITERATURE REVIEW

## 2.1 Introduction

This chapter will review in detail about the element that had been used in this project such as DC-DC power converter and PID controller.

## 2.2 DC-DC Buck Converter

The most common power converter and always been used by power supply designer is buck converter also known as step-down converter. It is normally used because the output voltage  $V_o$  is always less than the input voltage  $V_s$  in the same polarity and it is not isolated from the input.

The buck converter circuit is a one of switch mode regulator. It uses a power transistor such as MOSFET, IGBT, and others as the switching element and commonly controlled by pulse-width-modulation (PWM). This converter also uses an inductor and a capacitor as energy storage elements so that energy can be transferred from the input to the output in discrete packets. The advantage of using switching regulators is that they offer higher efficiency than linear regulators. The one disadvantage is noise or ripple; the ripple will need to be minimized through careful component selection. The basic circuit for buck converter is shown by Figure 2.1.

To reduce output voltage ripple, the switching frequency should be increased but this lowers efficiency. This means that the selection of the switching devices will be an important issue. The output voltage ripple can also be reduced by increasing the output capacitance; this means a large capacitor in practical design. It also can be reduce by adding some device that function as filter. Normally some designers add some control system which the output voltage can be controlled such control the ripple voltage.

The state of the converter in which the inductor is never zero for any period of time is called the continuous conduction mode (CCM). The DC-DC converters can operate in two distinct modes with respect to the inductor current  $i_L$ . Figure 2.2 describe the CCM where the inductor current is always greater than zero. When the average value of output current is low and/or the switching frequency f is low, the converter may enter the discontinuous conduction mode (DCM). In the DCM, the inductor current is zero during a portion of the switching period. The CCM is preferred in high efficiency and good utilization of semiconductor switches and passive components. The DCM may be used in applications with special control requirement because the dynamic order of the converter is reduced where the energy stored in the inductor is zero at the beginning and at the end of each switching period [1].

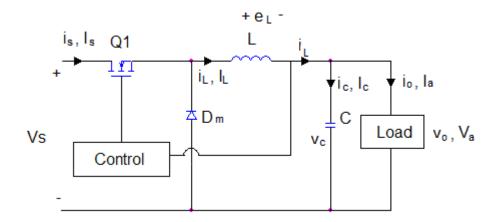


Figure 2.1: Buck Converter

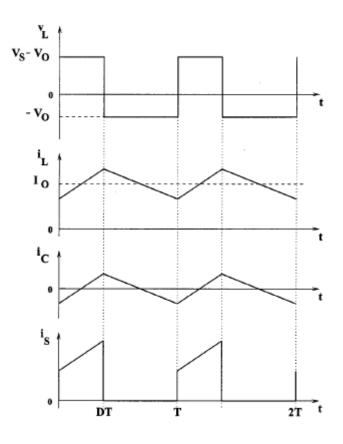


Figure 2.2: Waveforms of Buck Converter

#### 2.2.1 Buck Converter Operation

DC-DC buck converter is the basic power converter that normally been used. This converter operates in two modes which are mode 1 and mode 2.

#### 2.2.1.1 Mode 1 operation

Mode 1 begins when the MOSFET Q1 of Figure 2.1 is switch on at t = 0. In this state, the current will rise through the inductor and the energy stored in it increase [2]. During this state the inductor acquires the energy. When the MOSFET is turn ON, the diode will be in OFF state. Since the diode is there, there will always a current source for the inductor. The equivalent circuit for Mode 1 is shown by Figure 2.3.

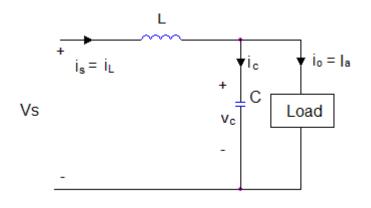


Figure 2.3: Equivalent circuit for Mode 1

#### 2.2.1.2 Mode 2 operation

Mode 2 begins when the MOSFET Q1 of Figure 2.1 is turn switch off at  $t = t_1$ . The freewheeling diode  $D_m$  conducts due to energy stored in the inductor and the inductor current continues to flow through *L*, *C*, load, and diode  $D_m$ . The inductor current fall until MOSFET Q1 is switched ON again in the next cycle [2]. Figure 2.4 show the equivalent circuit for Mode 2 operation.

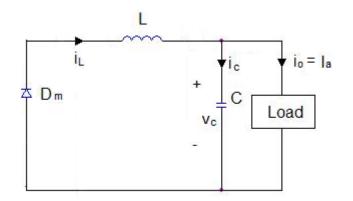


Figure 2.4: Equivalent circuit for Mode 2

#### 2.2.1.3 Pulse-Width-Modulator (PWM)

PWM is one of the method uses to switch ON and OFF the power transistor. There are many way to generate this PWM although by using a timer or microcontroller. The simplest way to generate a PWM signal is the intersective method, which requires only a sawtooth or a triangle waveform and a comparator. When the value of the reference signal, the sine wave is more than the modulation waveform, the PWM signal is in the high state, otherwise it is in the low state. Figure 2.5 illustrates the waveform of the PWM generated trough this method [3].

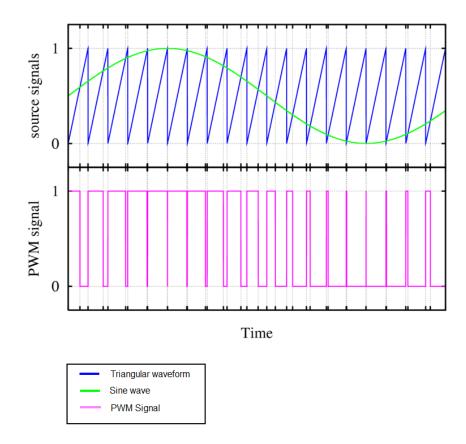


Figure 2.5: PWM Waveform

## 2.2.2 Buck Converter basic formula

In Figure 2.1, assuming that the inductor current rises linearly from  $I_1$  to  $I_2$  in time  $t_1$ 

$$V_s - V_a = L \frac{I_2 - I_1}{t_1} = L \frac{\Delta I}{t_1}$$
$$t_1 = \frac{\Delta I L}{V_a}$$

Substituting  $t_1 = DT$ , hence the output average output voltage is

$$V_a = V_a \frac{t_1}{T} = DV_a$$

Condition for CCM the value of inductor and capacitor is

$$L = V_a \frac{(1-D)R}{2f}$$
$$C = \frac{1-D}{16Lf^2}$$

where D is duty cycle and f is switching frequency.

### 2.3 PID Controller

PID controller is the most popular control system that had been use in worldwide due to their control action which is quite easier to develop. This controller consist of three control action element which is Proportional (P), Integral (I), and Derivative (D). Combinations of this three control action produce Proportional-Integral-Derivative (PID) control action.

#### 2.3.1 Proportional Control Action

For a controller with proportional control action, the relationship between the output of the controller u(t) and the actuating error signal e(t) is

$$u(t) = K_p e(t)$$

In Laplace transform quantities,

$$\frac{U(s)}{E(s)} = K_p$$

where  $K_p$  is term of the proportional gain [4]. A Proportional controller reduces the error but not eliminate it unless the process has naturally integrating properties.

## 2.3.2 Integral Control Action

In controller with integral control action, the value of the controller output u(t) is changed at a rate proportional to the actuating error signal e(t). That is

$$\frac{du(t)}{dt} = K_i e(t)$$

or

$$u(t) = K_i \int_0^t e(t) dt$$

 $K_i$  is an adjustable constant. The transfer function of the integral controller is

$$\frac{U(s)}{E(s)} = \frac{K_i}{s}$$

## 2.3.3 Proportional-Integral Control Action

The Proportional-Integral control action is defined by

$$u(t) = K_p e(t) + \frac{K_p}{T_i} \int_0^t e(t) dt$$

The transfer function for the controller is

$$\frac{U(s)}{E(s)} = K_p \left( 1 + \frac{1}{T_i s} \right)$$

where  $T_i$  is the integral time.

### 2.3.4 Proportional-Derivative Control Action

For Proportional-Derivative control action the controller is defined by

$$u(t) = K_p e(t) + K_p T_d \frac{de(t)}{dt}$$

and the transfer function for the controller is

$$\frac{U(s)}{E(s)} = K_p \left( 1 + T_d s \right)$$

where  $T_d$  is called the derivative time [4].

## 2.3.5 Proportional-Integral-Derivative Control Action

The combination of proportional control action, integral control action, and derivative control action is termed proportional-integral-derivative control action [4].

The equation for the controller is defined by

$$u(t) = K_p e(t) + \frac{K_p}{T_i} \int_0^t e(t) dt + K_p T_d \frac{de(t)}{dt}$$

The transfer function is

$$\frac{U(s)}{E(s)} = K_p \left( 1 + \frac{1}{T_i s} + T_d s \right)$$

# 2.4 Implementation of Digital PID Controllers for DC-DC Converters Using Digital Signal Processor

Traditionally, the control methodology for DC-DC converter has been analog control. Analog-based control systems have two main advantages which is low cost and wide control bandwidth. Nowadays, the advance technologies in very-large-scale integration (VLSI) have made a digital control of DC-DC converters by using microcontroller and digital signal processor. Digital control of DC-DC converters offer a several advantages over analog control which is more advance algorithms such as adaptive control and nonlinear control can be implemented using digital control, more flexible by changing the software, and the power efficiency optimization can be achieved. Digital control can be implemented using digital signal processors, microcontrollers, and digital integrated circuit (IC). Generally DSP have more computational than microcontrollers. Therefore more advanced control algorithms can be implemented on a DSP. Although microcontroller is less expensive compare to DSP but it provide digital control solution at lower cost [5]. In DC-DC converters as shown in Figure 2.6 the output voltage is a function of the input line voltage, the duty cycle and load current. It is desirable to have a constant output voltage in the event of disturbances such a sudden change of input voltage or load current. Negative feedback is applied to DC-DC converters to automatically adjust the duty cycle to obtain the desired output voltage with high accuracy in spite of disturbance [5]. The frequency response technique is used to design digital control for buck converter.

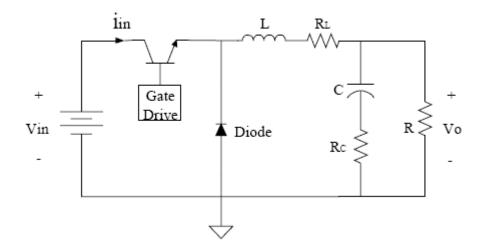


Figure 2.6: Basic Buck Converter

For a buck converter the output-to-control small signal transfer function of buck converter that obtain by using standard state-space averaging technique is

$$\frac{\hat{v}_o(s)}{\hat{d}_o(s)} = \frac{Vo}{D} \left[ \frac{1 + sR_cC}{1 + s\left(R_cC + \left[R / / R_L\right]C + \frac{L}{R + R_L}\right) + s^2LC\left(\frac{R + RC}{R + R_L}\right)} \right]$$

In this transfer function,  $\hat{v}_o(s)$  and  $\hat{d}(s)$  are the small variations of the output voltage and duty cycle respectively. *D* is the duty cycle of the PWM signal. It is a common two-pole low pass filter, with a left half plane zero introduce by the ESR of the filter capacitance [5].

A PID is designed for buck converter to improve the loop gain, cross-over frequency and phase margin [5]. The example of Bode plot for the PID compensated system is shown in Figure 2.7. The transfer function of the PID controller is given by

$$G_c(s) = K_p + \frac{K_i}{s} + K_d s$$

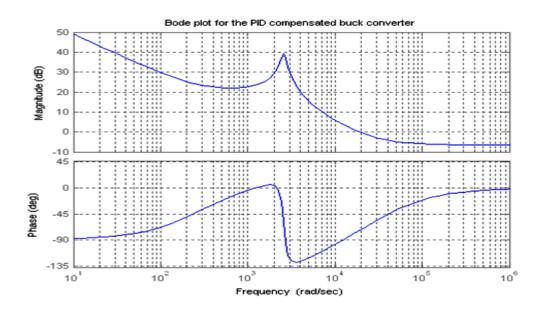


Figure 2.7: Example of Bode plot for PID controller compensated buck converter

A PI controller was also designed for the control of the buck converter at steady state to reduce steady-state oscillation. The DC gain of the controller was adjusted to obtain sufficient phase margin and high cross-over frequency [5]. The transfer function of the PI controller is given by

$$G_c(s) = K_p + \frac{K_i}{s}$$

The example Bode plot for the PI compensated system is shown in Figure 2.8. The phase margin of PID controller supposes to be better than PI controller and both better then the system alone.

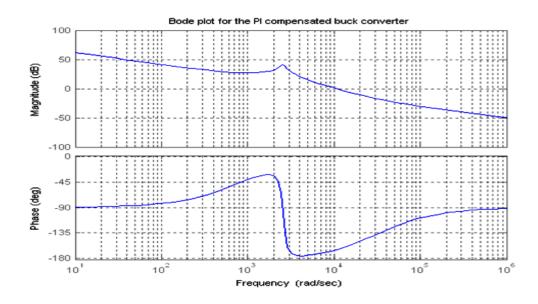


Figure 2.8: Example of Bode plot for PI controller compensated buck converter

### CHAPTER 3

### METHODOLOGY

### 3.1 Introduction

This chapter will illustrate the overall process in building the PI controller for buck converter from designing the buck converter and analog PI controller until to the developing of the hardware.

### **3.2** Designing of Buck converter

For the buck converter, the input voltage is set to 24 V and the output voltage is 16 V. The switching frequency is set to 30 kHz and load resistor is 33  $\Omega$ . The basic step to design a CCM buck converter is to set the switching frequency higher than 20 kHz, the inductor greater ten times the calculated value and also same for the capacitor value.

The value of the inductor is 2 mH and the value for capacitance is 1  $\mu$ F. For duty cycle equal to 67% the period is 33.333  $\mu$ s. T<sub>ON</sub> is the time for the switch is ON where the value is equal to 22.33  $\mu$ s. T<sub>OFF</sub> is the time for the switch is OFF where the value is equal to 11  $\mu$ s. The MOSFET which is IRF510 is been choose since it is able to handle a high frequency switching period. The circuit design for buck converter is shown as Figure 3.1.

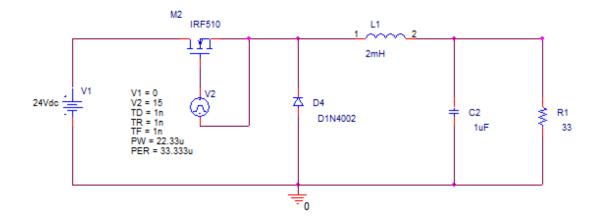


Figure 3.1: Circuit of Buck Converter

The transfer function for buck converter is

$$G_{b}(s) = \frac{V_{o}}{D} \left( \frac{1}{1 + \frac{L}{sR} + s^{2}LC} \right)$$
(3.1)

#### 3.2.1 Pulse-Width-Modulation (PWM) Generation

Since buck converter using a PWM as switching element then another circuit to generate PWM is being setup by using 16F877A PIC microcontroller. This 16F877A microcontroller have a built in PWM generator that easily can be used by program the instruction into the microcontroller. Figure 3.2 show the basic setup for 16F877A microcontroller.

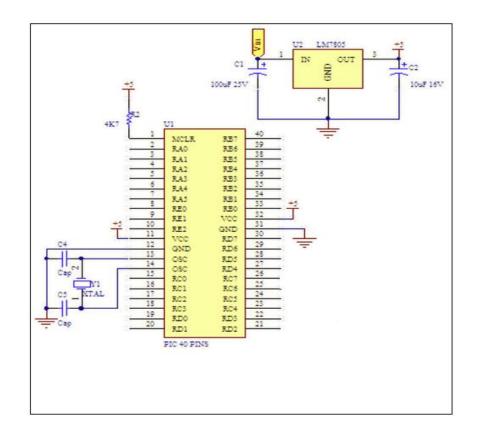


Figure 3.2: Basic PIC 40 Pins Setup

After the circuit is assemble, the program can be write to the microcontroller by using Microcode Studio software and a special microcontroller burner device. The program to generate 30 kHz PWM with duty cycle 67% by using 16F877A microcontroller is shown in next page.

DEFINE OSC 4 DEFINE CCP1\_REG PORTC 'Hpwm 1 pin port DEFINE CCP1\_BIT 2 'Hpwm 1 pin bit DEFINE CCP2\_REG PORTC 'Hpwm 2 pin port DEFINE CCP2\_BIT 1 'Hpwm 2 pin bit

TRISB.7 = 0TRISC.1 = 0TRISC.2 = 0

hpwmsub:

HPWM 1,171,30000 ' Send a 67% duty cycle PWM signal at 30kHz

led\_blink:

HIGH PORTB.7 PAUSE 500 ; delay 500 LOW PORTB.7 PAUSE 500 HIGH PORTB.7 PAUSE 500 ; delay 500 LOW PORTB.7 PAUSE 500 HIGH PORTB.7 PAUSE 500 ; delay 500 LOW PORTB.7 PAUSE 500 HIGH PORTB.7 ; delay 500 PAUSE 500

goto led\_blink

The program is start with definition of the system crystal and the hardware pulse-width-modulation (HPWM) register port. The hpwmsub is the subroutine of HPWM which is set to port 1 with 67% of duty cycle at 30 kHz while the led\_blink subroutine is a program to make sure the hardware is functioning.

### 3.2.2 MOSFET Driver Circuit

In order to use the MOSFET or to turn it ON and OFF, a driver circuit need to be use since the voltage from 16F877A PIC is very low to operate the MOSFET. By referring to Appendix A the datasheet of IRF510, a 15 V is needed to operate this IRF150. The driver circuit for IRF510 is shown in Figure 3.3.

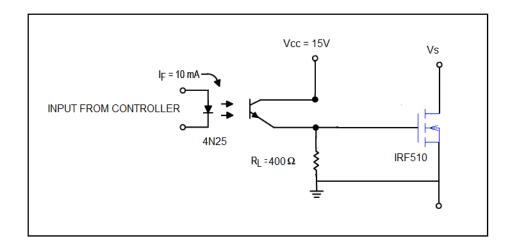


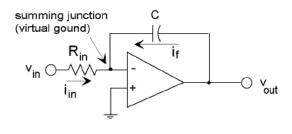
Figure 3.3: Driver Circuit for IRF510

Isolation is required to prevent damages on the high power switch to propagate back to low power electronics. Normally opto-coupler or high frequency magnetic materials are used. In this project, the 4N25 opto-coupler is being used because it can handle high frequency and high voltage break-down. The characteristic for 4N25 opto-coupler is shown in Appendix B.

## 3.3 Designing of Analog PI controller

For designing an analog PI controller a basic op-amp LM741 is being used. There are three steps to build a PI control. First step is to build an integrator illustrate in Figure 3.4 (a) and 3.4(b). The integrator obey the equation,

$$v_{out} = -\frac{1}{R_n C} \int_0^t v_{in}(t) dt + v_o ut(0)$$



(a)

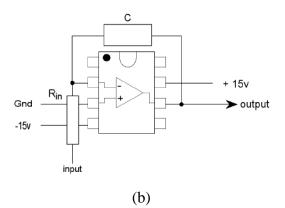


Figure 3.4: (a) Integrator diagram (b) Integrator IC layout.

The value of  $R_{in} = 10 \text{ k}\Omega$  and the value of capacitor  $C = 10 \mu F$ .

The second step of building a PI controller is to build the unity gain inverting amplifier. This unity gain is function as Proportional (P) control action. The diagram and layout for this unity gain inverting amplifier is shown as Figure 3.5(a) and 3.5(b). The value of  $R_{in}$  and  $R_f$  is 10 k $\Omega$ .

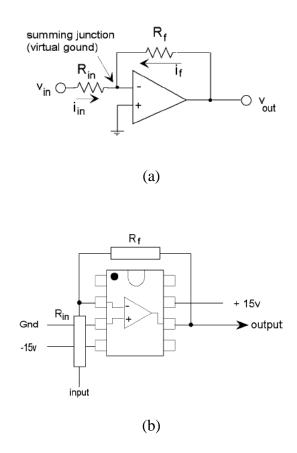
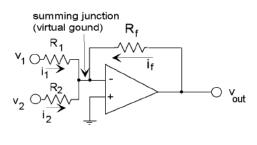


Figure 3.5: (a) Unity gain diagram (b) Unity gain IC layout

The last step is to build a summer for Proportional and Integrator control action. This summer is use to combine the action from both control action. The Figure 3.6 (a) and (b) illustrates the diagram and layout for this summer and Figure 3.7 shown the complete diagram for analog PI controller. The value of  $R_1$  and  $R_2$  is set to 10 k $\Omega$ .



(a)

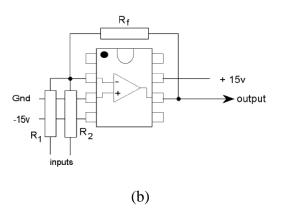


Figure 3.6: (a) Summer diagram (b) Summer IC layout

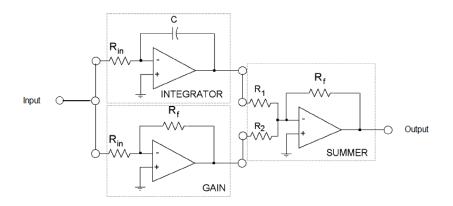


Figure 3.7: The complete analog PI controller circuit diagram

### **3.4** Development of the Project

The development of this project consists of two stage which is simulation stage and hardware development stage. After the simulation stage is done, the next process is developing the hardware as well as simulation.

### 3.4.1 Simulation Stage

The simulation for this project is done by using Orcad Pspice software. The full circuit is shown in Figure 3.8. The simulation time is set to 1 ms.

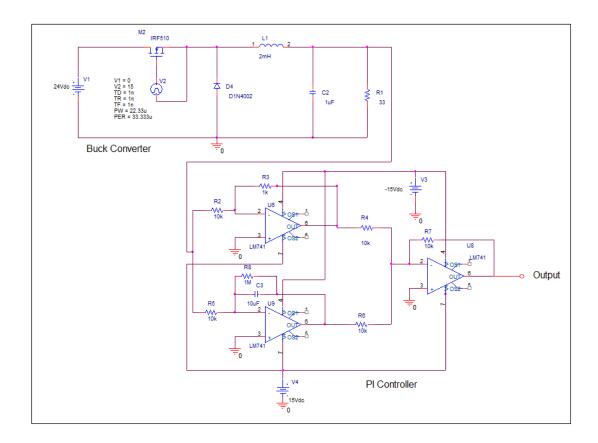


Figure 3.8: Complete PI controller for battery charger circuit diagram

### 3.4.2 Hardware Development Stage

After the simulation stage is done, the hardware for this project is been assembles on the strip board. The hardware is built by referring to the circuit diagram in Figure 3.8. The hardware for buck converter and PI controller is shown in Figure 3.9.

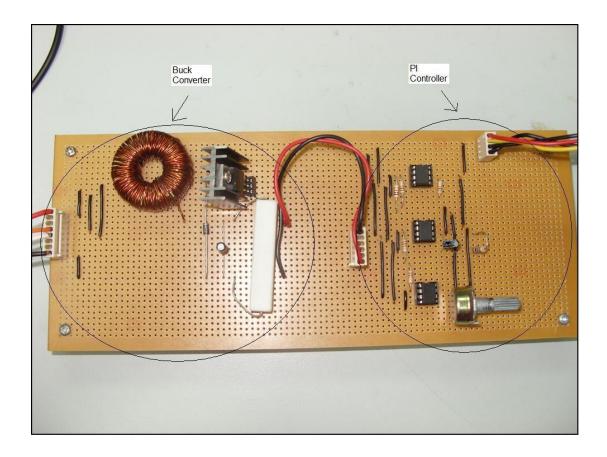


Figure 3.9: Complete Hardware of Buck Converter with PI Controller

Referring to Figure 3.9, the left side is a buck converter while the right side is PI controller. The output from buck converter is connected to PI controller input by the jumper at the middle of the hardware. The integral control action is fixed to  $K_i = 1/s$  and the proportional control action,  $K_p$  is variable by using the potential meter.

Figure 3.10 show the hardware for PWM generator and MOSFET driver circuit. For PWM generator, the 4 MHz crystal is being used and the circuit is assembled as the basic circuit. The MOSFET driver circuit is assembled according to circuit in Figure 3.3.

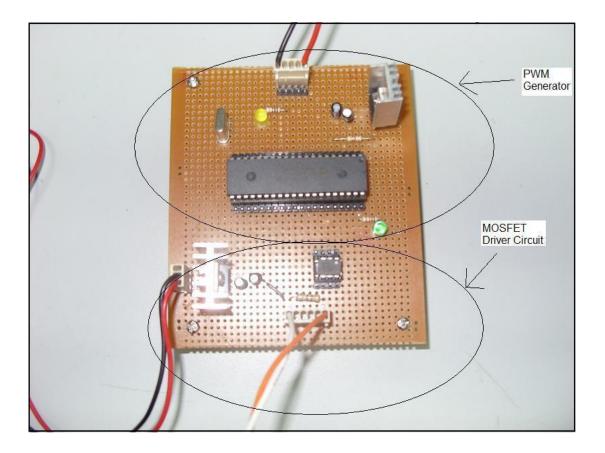


Figure 3.10: Hardware for PWM Generator and MOSFET Driver Circuit

### **CHAPTER 4**

### **RESULT AND DISCUSSION**

### 4.1 Introduction

This chapter discussed about the result obtains from simulation and hardware. All discussion is focus on the effect of PI controller control action to the output from DC-DC buck converter.

### 4.2 Simulation Result

Since the Integral (I) control action is fixed, then only the Proportional (P) can be adjusted during the test.

### 4.2.1 Output from Buck Converter

Figure 4.1 shows the output result from buck converter. From this graph, the output voltage is 15.5 V closed to the desired voltage which is 16 V. The rise time is about 0.11 ms and the ripple voltage is quite high.

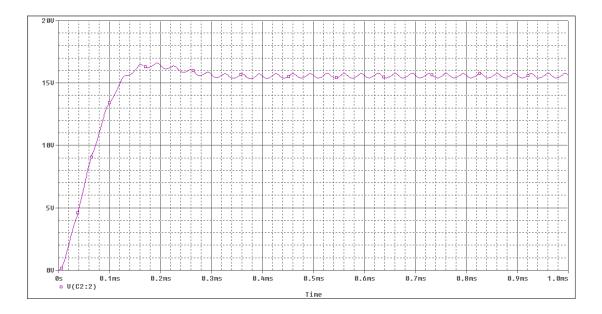
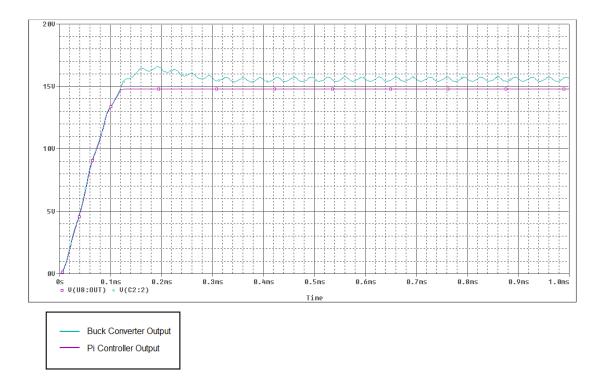


Figure 4.1: Buck Converter Output

# **4.2.2** Output from PI Controller with $K_p = 1$

Figure 4.2 show the result obtains from PI controller output point with  $K_p = 1$  and buck converter output point. As the graph plotted in Figure 4.2, the ripple voltage from PI controller output is being eliminated by Integral (I) action control while the rise time is remain the same as buck converter.



**Figure 4.2:** Buck Converter and PI Controller output with  $K_p = 1$ 

# **4.2.3** Output from PI Controller with $K_p = 5$

Figure 4.3 show the output from buck converter and PI controller with  $K_p = 5$ . The ripple voltage from PI controller output is being eliminated by Integral (I) control action and the rise time is change to 0.02 ms due to Proportional (P) control action.

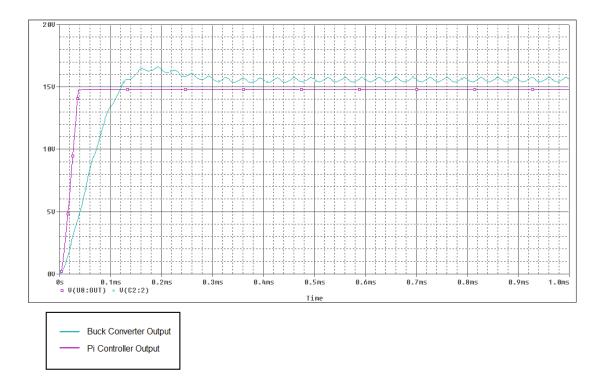


Figure 4.3: Buck Converter Output and PI controller output with  $K_p = 5$ 

# 4.2.4 Output from PI Controller with $K_p = 0.9$

Figure 4.4 show the output from buck converter and PI controller with  $K_p = 0.9$ . There is a low ripple voltage appeared, that's mean the value of  $K_i$  need to be change to eliminate the ripple voltage. The rise time for the output from PI controller is change to 0.13 ms.

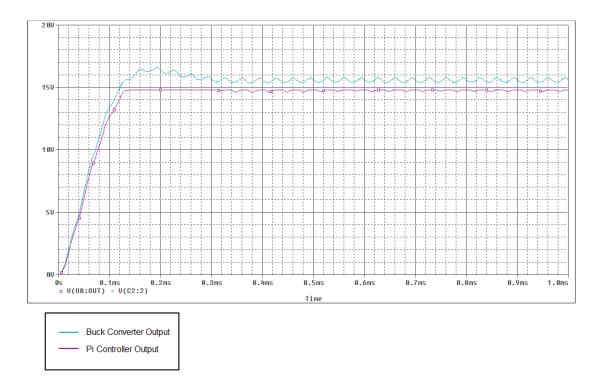


Figure 4.4: Buck Converter Output and PI Controller Output with  $K_p = 0.9$ 

## 4.3 Hardware Result

The output result from hardware is determined by several points such as point at buck converter output point and PI controller output point. Figure 4.5 show the buck converter output point while Figure 4.6 show the PI controller output point.

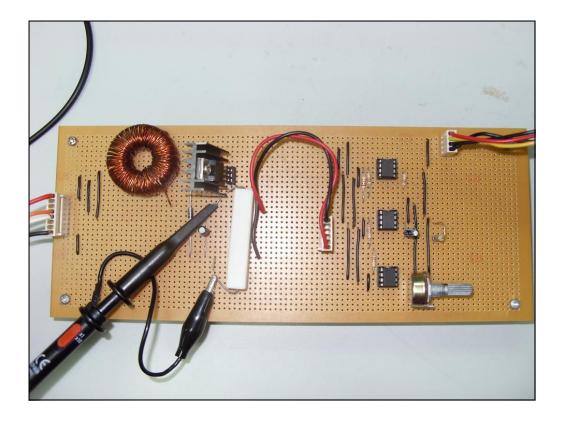


Figure 4.5: Buck Converter Output Point

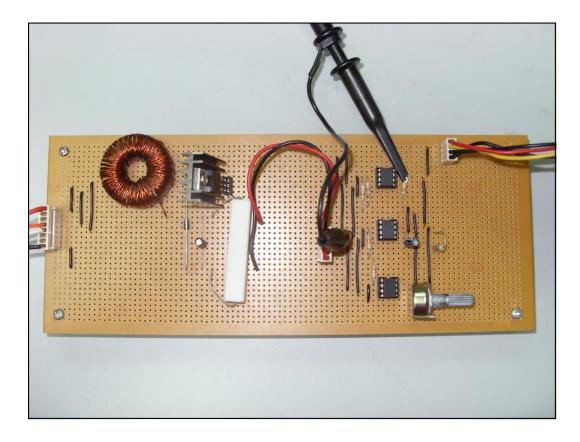


Figure 4.6: PI Controller Output Point

### 4.3.1 Buck Converter Output Result

The output for buck converter is measured at the point shown in Figure 4.5 give the result shown in Figure 4.7. The Oscilloscope is set to 5 V per division and 1 ms per division. The output before using the PI controller has a high ripple voltage.

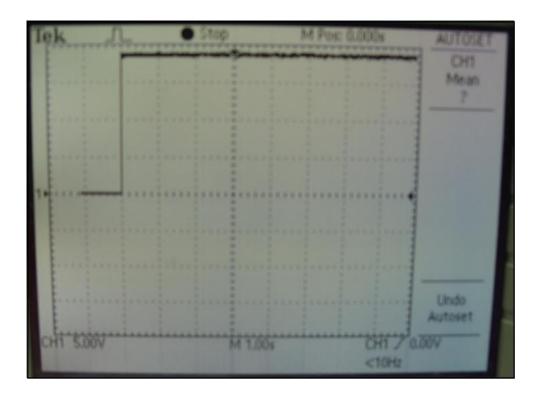


Figure 4.7: Output from Buck Converter

### 4.3.2 PI Controller Output Result

Figure 4.8 show the output from PI controller. The output ripple voltage is low compare to the ripple voltage before using PI controller. The rise time is remaining the same since the value of proportional gain  $K_p$  is 1. The Oscilloscope is set to 5 V per division and 1 ms per division.

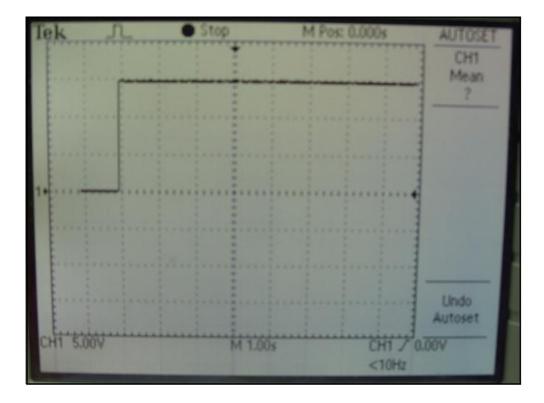
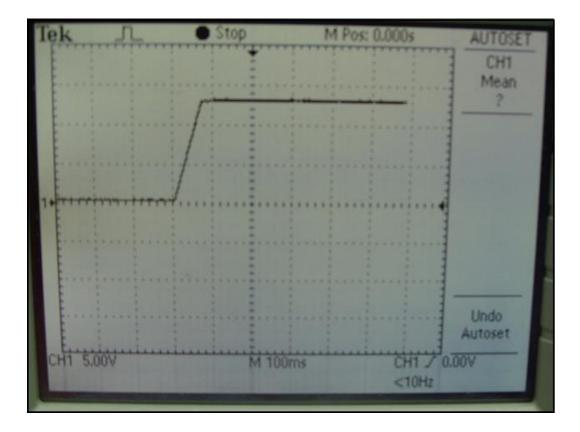


Figure 4.8: Output from PI Controller

# 4.3.3 PI Controller Output with $K_p = 0.5, K_p < 1$

Figure 4.9 shows the output waveform from PI controller when the proportional gain  $K_p$  is decrease to 0.5. The Integral (I) control action reduce the ripple voltage while the rise time is decrease due to the Proportional (P) control action. The Oscilloscope is set to 5 V per division and 100 ms per division.



**Figure 4.9:** PI Controller Output with  $K_p = 0.5$ 

## 4.4 System Comparison

This section shows the output response for buck converter without PI controller and output response with PI controller. The comparison for both systems is discussed. The output response for the system can be determined by using MATLAB software

# 4.4.1 Output Response of Buck Converter without PI Controller

Figure 4.10 show the Bode plot of buck converter without using the PI controller. By using equation 3.1 the system transfer function is

$$G_b(s) = \frac{23.88}{s^2 + 3000s + 5 \times 10^8}$$

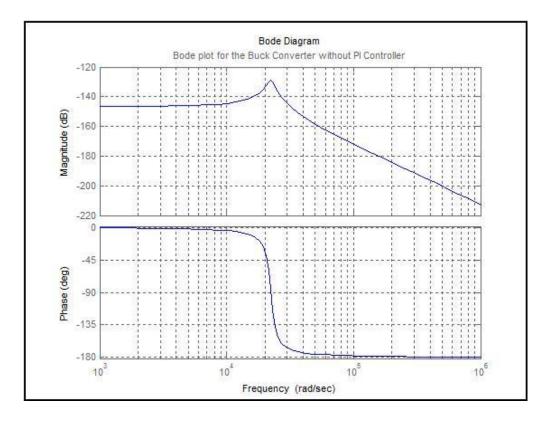


Figure 4.10: Bode plot of the Buck Converter without PI Controller

## 4.4.2 Output Response of Buck Converter with PI Controller

Figure 4.11 show the Bode plot of the buck converter with PI controller. The transfer function for this system is

$$G_{bc}(s) = \frac{23.88s + 23.88}{s^3 + 3000s^2 + 5 \times 10^8 s}$$

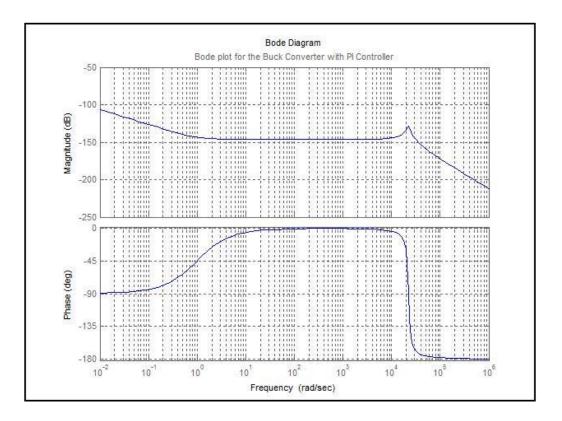


Figure 4.11: Bode plot of the Buck Converter with PI Controller

Figure 4.10 and Figure 4.11 illustrate the comparison between the system alone and the system with PI controller. There is a difference on phase margin and crossover frequency value due to the action of PI controller.

### 4.5 Discussion

By referring to the result from simulation and hardware, the effect of the control action from PI controller to the buck converter output is clearly can be seen. Since the Integral (I) control action is fixed so the action from this control action can't be observe. However the Proportional (P) control action can be investigate by adjusting the potential meter use in the circuit. When the proportional gain  $K_p$  larger than 1 the rise time is increase and when  $K_p$  less than 1 the rise time is decrease.

### **CHAPTER 5**

### CONCLUSION

### 5.1 Introduction

This chapter will explain about the overall conclusion for this project, future recommendation, and costing and commercializing.

## 5.2 Conclusion

The PI controller for battery charger system is one of control system that had been used in industry whether for control purpose or education purpose. This controller can be developing by using analog system or digital system. In this project the controller is built in analog system since the LM741 op-amp is being used. By finishing his project, the control action from each element can be investigated.

### 5.3 Future Recommendation

Since this project is only for investigate the action of PI controller, there are many changes had to be done in order to complete the battery charger controlled by PI controller. Auto ON/OFF system or trickle mode system needs to be added in this system to avoid overcharging occur. To get a proper control action, the complete PID controller is recommended since the control action is better than PI controller.

### 5.4 Costing and Commercialization

In this section describe all about the costing involve in completing this project and also the explanation about commercialization issue.

### 5.4.1 Costing

The overall of the whole project is based on the hardware development. All the cost especially for the component used in this project is shown in Table 5.1. The total cost for this project is RM 80.12.

No	Part	Cost	Quantity	Total
1	Inductor (2mH)	RM 8.00	1	RM 8.00
2	16F877A PIC	RM 22.00	1	RM 22.00
3	Strip Board	RM 5.50	2	RM 11.00
4	Resistor (33 $\Omega$ 10 W)	RM 1.00	1	RM 1.00
5	Potential Meter (100 kΩ)	RM 0.50	1	RM 0.50
6	Board Stand	RM 0.70	8	RM 5.60
7	MOSFET (IRF 510)	RM 4.80	1	RM 4.80
8	Capacitor (1µF)	RM 0.12	4	RM 0.48
9	Diode (D1N4002)	RM 0.50	1	RM 0.50
10	Resistor (10 kΩ)	RM 0.02	5	RM 0.10
11	Capacitor (10µF)	RM 0.12	1	RM 0.12
12	Heatsink	RM 0.70	3	RM 2.10
13	LM741	RM 2.00	3	RM 6.00
14	Opto-coupler (4N25)	RM 3.00	1	RM 3.00
15	Voltage Regulator (LM7805)	RM 2.00	1	RM 2.00
16	Voltage Regulator (LM 7815)	RM 2.00	1	RM 2.00
17	Resistor (4.7 kΩ)	RM 0.12	1	RM 0.12
18	Resistor (100 Ω)	RM 0.12	2	RM 0.24
19	Resistor (400 Ω)	RM 0.12	1	RM 0.12
20	Resistor (1 MΩ)	RM 0.12	1	RM 0.12
21	Crystal	RM 0.80	1	RM 0.80
22	IC base	RM 0.60	5	RM 3.00
23	LED	RM 0.50	2	RM 1.00
24	Pin Connector 7 pin	RM 2.00	3	RM 6.00
	1	<b>I</b>	Total	RM 80.12

 Table 5.1: Cost of the Component

### 5.4.2 Commercialization

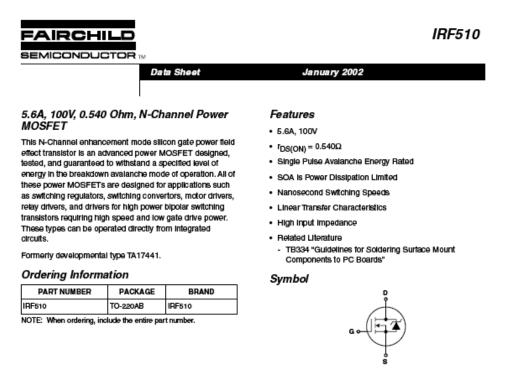
Since this project is base on investigation on PI controller, this hardware is not suitable to commercialize unless some modification is made to improve the system. Although the PI control system is commonly used in industry, but digital PI controller is better than analog PI controller since it is controlled by digital signal processor which is more reliable and low cost.

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- [6] Battery Charger, Citing Internet sources URL http://en.wikipedia.org/wiki/Battery\_charger

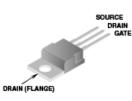
# APPENDIX A

#### **IRF510** datasheet



Packaging

JEDEC TO-220AB



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IRF510 Rev. B

#### IRF510

Absolute Maximum Ratings T<sub>C</sub> = 25°C, Unless Otherwise Specified

raborate maannan naange 10-25 of enece openies		
- • · · · ·	IRF510	UNITS
Drain to Source Voltage (Note 1)VDS	100	v
Drain to Gate Voltage (R <sub>GS</sub> = 20kΩ) (Note 1) V <sub>DGR</sub>	100	v
Continuous Drain Current	5.6	A
T <sub>C</sub> = 100 <sup>6</sup> C I <sub>D</sub>	4	А
Pulsed Drain Current (Note 3)	20	A
Gate to Source Voltage	±20	v
Maximum Power Dissipation	43	w
Linear Derating Factor	0.29	M/oC
Single Pulse Avalanche Energy Rating (Note 4) EAS	19	mJ
Operating and Storage Temperature Range	-55 to 175	°c
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	300	°C
Package Body for 10s, See Techbrief 334 T <sub>pkg</sub>	260	°c
CAUTION: Stresses above those listed in "Aboulute Maximum Batings" may gauge permanent damage to the device. This is	a stress only ratio a	nd operation of the

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those in dicated in the operational sections of this specification is not implied.

NOTE:

1.  $T_J = 25^{\circ}$ C to  $150^{\circ}$ C.

Electrical Specifications  $T_C = 25^{\circ}C$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BVDSS	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250µA, (Figure 10)		-	-	v
Gate to Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250µA		-	4.0	v
Zero-Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 95V, V <sub>GS</sub> = 0V	-	-	25	μA
		$V_{DS} = 0.8 \text{ x}$ Rated $BV_{DSS}$ , $V_{GS} = 0V$ , $T_J = 150^{\circ}C$	-	-	250	μA
On-State Drain Current (Note 2)	ID(ON)	V <sub>DS</sub> > I <sub>D(ON) x</sub> r <sub>DS(ON)MAX</sub> , V <sub>GS</sub> = 10V (Figure 7)		-	-	A
Gate to Source Leakage Current	IGSS	V <sub>GS</sub> = ±20V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	FDS(ON)	V <sub>GS</sub> = 10V, I <sub>D</sub> = 3.4A (Figures 8, 9)	-	0.4	0.54	Ω
Forward Transconductance (Note 2)	9rs	V <sub>GS</sub> = 50V, I <sub>D</sub> = 3.4A (Figure 12)	1.3	2.0	-	S
Turn-On Delay Time	ta(ON)	$\begin{array}{l} I_D \simeq 5.6A, \ R_{GS} = 24\Omega, \ V_{DD} = 50V, \ R_L = 9\Omega, \\ V_{DD} = 50V, \ V_{GS} = 10V \\ MOSFET switching times are essentially independent \\ of operating temperature \end{array}$		8	12	ns
Rise Time	ţ.			25	63	ns
Turn-Off Delay Time	ta(OFF)			15	7	ns
Fall Time	tf			12	59	ns
Total Gate Charge (Gate to Source + Gate to Drain)	Q <sub>g(TOT)</sub>	$\label{eq:VGS} \begin{split} &V_{GS} = 10V,  I_D = 5.6A,  V_{DS} = 0.8  \times \text{Rated BV}_{DSS}, \\ &I_{CJ(EE)} = 1.5mA (Figure 14) \\ &\text{Gate charge is essentially independent of operating temperature.} \\ &V_{GS} = 0V,  V_{DS} = 25V,  f = 1.0MHz  (Figure 11) \end{split}$		5.0	30	nC
Gate to Source Charge	Qgs			2.0	-	nC
Gate to Drain "Miller" Charge	Qgd			3.0	-	nC
Input Capacitance	CISS			135	-	pF
Output Capacitance	Coss			80	-	pF
Reverse-Transfer Capacitance	CRSS			20	-	pF
Internal Drain Inductance	LD	Measured From the Contact Screw On Tab To Center of Die Most Symbol Showing the Internal Devices	-	3.5	-	nH
		Measured From the Drain Lead, 6mm (0.25in) From Package to Center of Die	-	4.5	-	nH
Internal Source Inductance	LS	Measured From The Source Lead, 6mm (0.25in) From Header to Source Bonding Pad	-	7.5	-	nH
Junction to Case	Reac		-	-	3.5	°C/W
Junction to Ambient	R <sub>BJA</sub>	Free air operation	-	-	80	°C/W

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IRF510 Rev. B

### IRF510

#### Source to Drain Diode Specifications

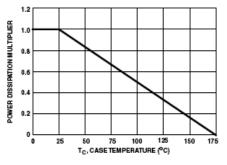
PARAMETER	SYMBOL	Test Conditions		MIN	түр	MAX	UNITS
Continuous Source to Drain Current	I <sub>SD</sub>	Modified MOSFET	٩D	-	-	5.6	Α
Pulse Source to Drain Current (Note 3)	<sup>I</sup> SDM	Symbol Showing the Integral Reverse P-N Junction Diode		-	-	20	A
Source to Drain Diode Voltage (Note 2)	V <sub>SD</sub>	T <sub>J</sub> = 25 <sup>0</sup> C, I <sub>SD</sub> = 5.6A, V <sub>GS</sub> = 0V (Figure 13)		-	•	2.5	v
Reverse Recovery Time	tп	$T_J = 25^{0}$ C, $I_{SD} = 5.6$ A, $dI_{SD}/d_t = 100$ A/µs		4.6	96	200	ns
Reverse Recovered Charge	QRR	$T_J = 25^{\circ}C$ , $I_{SD} = 5.6A$ , $dI_{SD}/d_t = 100A/\mu s$		0.17	0.4	0.83	μC

NOTES:

2. Pulse test: pulse width  $\leq$  300 $\mu$ s, duty cycle  $\leq$  2%.

3. Repetitive rating: pulse width limited by max junction temperature. See Transient Thermal Impedance curve (Figure 3). 4. V\_DD = 25 V, start T\_J = 25 °C, L = 910  $\mu$ H, R\_G = 25  $\Omega$ , peak I\_{AS} = 5.6 A.

Typical Performance Curves Unless Otherwise Specified



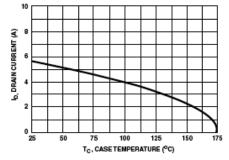
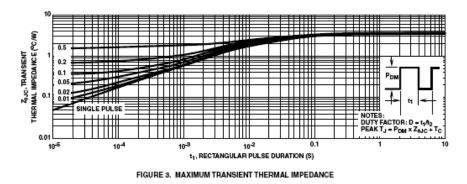


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE



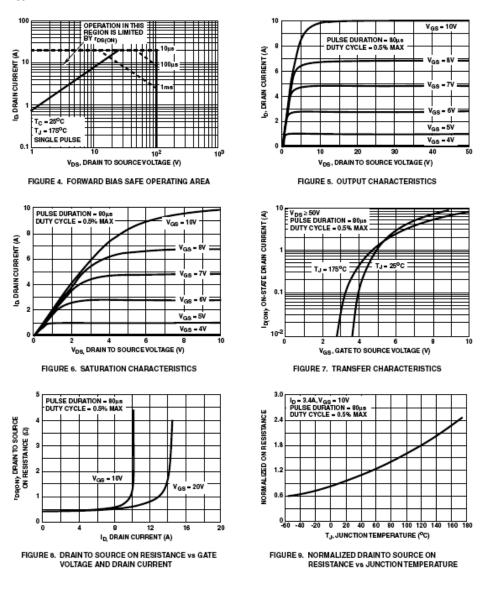


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IRF510 Rev. B



Typical Performance Curves Unless Otherwise Specified (Continued)



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RF510 Rev. B



Typical Performance Curves Unless Otherwise Specified (Continued)

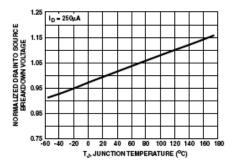
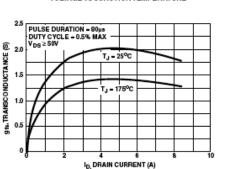


FIGURE 10. NORMALIZED DRAINTO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE



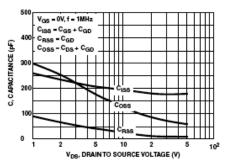


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

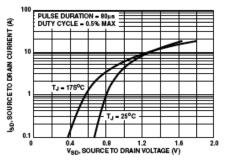


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

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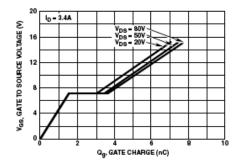


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

RF510 Rev. B

#### IRF510

#### Test Circuits and Waveforms

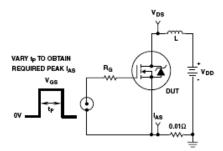


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

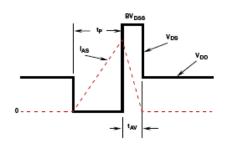


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

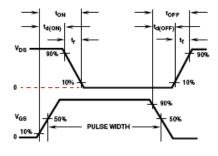


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

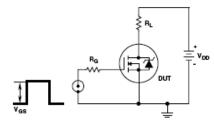


FIGURE 17. SWITCHING TIME TEST CIRCUIT

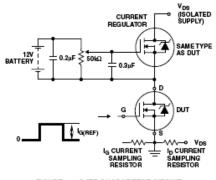


FIGURE 19. GATE CHARGE TEST CIRCUIT

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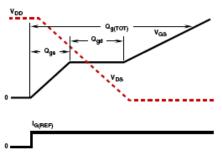


FIGURE 20. GATE CHARGE WAVEFORM

RF510 Rev. B

he following are realized					
ot intended to be an exhau			owns or is authorized to use and I		
Bottomless™ CoolFET™ CROSSVOLT™ DenseTrench™ DOME™ EcoSPARK™ EcoSPARK™ EroSgna™	FAST <sup>®</sup> FASTr <sup>™</sup> FRFET <sup>™</sup> GlobalOptoisolator <sup>™</sup> GTO <sup>™</sup> HISeC <sup>™</sup> HISeC <sup>™</sup> ISOPLANAR <sup>™</sup> LittleFET <sup>™</sup> MicroPak <sup>™</sup>	OPTOLOGIC <sup>™</sup> OPTOPLANAR <sup>™</sup> PACMAN <sup>™</sup> POWE <sup>1</sup> 247 <sup>™</sup> PowerTrench <sup>®</sup> QFET <sup>™</sup> QS <sup>™</sup> QT Optoelectronics <sup>™</sup> Quiet Series <sup>™</sup>	SMART START <sup>™</sup> VCX STAR*POWER <sup>™</sup> SuperSOT <sup>™</sup> -3 SuperSOT <sup>™</sup> -6 SuperSOT <sup>™</sup> -8 SyncFET <sup>™</sup> TinyLogic <sup>™</sup> TruTranslation <sup>™</sup> UHC <sup>™</sup>		
FACT Quiet Series™	MICROWIRE™	SILENT SWITCHER®	UltraFET®		
TAR"POWER is used unde	r license				
DISCLAIMER					
DOES NOT ASSUME AN DR CIRCUIT DESCRIBE RIGHTS, NOR THE RIGH	Y LIABILITY ARISING O D HEREIN; NEITHER D	UT OF THE APPLICATION	10N OR DESIGN. FAIRCHILD OR USE OF ANY PRODUCT ENSE UNDER ITS PATENT		
IFE SUPPORT POLICY					
	HOUT THE EXPRESS WRIT ystems are devices or ided for surgical implant int sustain life, or (c) whose perly used in accordance vided in the labeling, can i	TEN APPROVAL OF FAIRCHILI 2. A critical componer support device or sysi be reasonably expect support device or sys e effectiveness.	PONENTS IN LIFE SUPPORT DSEMICONDUCTOR CORPORATIO the same component of a life term whose failure to perform can the cause the failure of the life to cause the failure of the life term, or to affect its safety or		
RODUCT STATUS DEFINIT	TIONS				
efinition of Terms					
Datasheet Identificatio	n Product Status	Definition			
Advance information	Formative or In Design		ains the design specifications for L. Specifications may change in notice.		
Preliminary	First Production	supplementary data Fairchild Semicondu	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.		
	Full Production	Semiconductor reser	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes a any time without notice in order to improve design.		
No Identification Needed		any time without not			

# **APPENDIX B**

### **4N25 Datasheet**



SEMICONDUCTOR



# 6-Pin DIP Optoisolators **Transistor Output**

The 4N25, 4N26, 4N27 and 4N28 devices consist of a gallium arsenide infrared emitting diode optically coupled to a monolithic silicon phototransistor detector.

- · Most Economical Optoisolator Choice for Medium Speed, Switching Applications
- · Meets or Exceeds All JEDEC Registered Specifications
- To order devices that are tested and marked per VDE 0884 requirements, the suffix "V" must be included at end of part number. VDE 0884 is a test option.

### Applications

- General Purpose Switching Circuits
- · Interfacing and coupling systems of different potentials and impedances
- I/O Interfacing
- Solid State Relays

Storage Temperature Range

Soldering Temperature (10 sec, 1/10" from case)

#### MAXIMUM RATINGS (TA = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit	
INPUT LED				
Reverse Voltage	VR	3	Volts	
Forward Current — Continuous	١F	60	mA	
LED Power Dissipation @ T <sub>A</sub> = 25°C with Negligible Power in Output Detector Derate above 25°C	PD	120 1.41	mW mW/∘C	
OUTPUT TRANSISTOR				
Collector-Emitter Voltage	VCEO	30	Volts	
Emitter–Collector Voltage	VECO	7	Volts	
Collector-Base Voltage	VCBO	70	Volts	
Collector Current — Continuous	IC	150	mA	
Detector Power Dissipation @ T <sub>A</sub> = 25°C with Negligible Power in Input LED Derate above 25°C	PD	150 1.76	mW mW/∘C	
TOTAL DEVICE	•			
Isolation Surge Voltage <sup>(1)</sup> (Peak ac Voltage, 60 Hz, 1 sec Duration)	VISO	7500	Vac(pk)	
Total Device Power Dissipation @ TA = 25°C Derate above 25°C	PD	250 2.94	mW mW/∘C	
Ambient Operating Temperature Range	TA	-55 to +100	°C	

-55 to +150

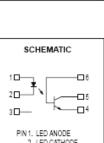
260

۰С

∘С

T<sub>stg</sub>

Ti



STANDARD THRU HOLE

4N25 4N26

4N27

4N28



Isolation surge voltage is an internal device dielectric breakdown rating. For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.

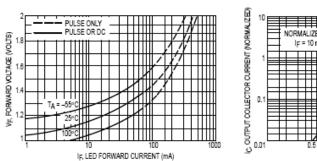


ELECTRICAL CHARACTERISTICS (T	A = 25°C unless otherwise	noted)(1)	_			
Characteristic	)	Symbol	Min	Тур <sup>(1)</sup>	Max	Unit
INPUT LED						
Forward Voltage (I <sub>F</sub> = 10 mA)	TA = 25°C TA = −55°C TA = 100°C	VF		1.15 1.3 1.05	1.5 —	Volts
Reverse Leakage Current (VR = 3 V)		IR	_	-	100	μA
Capacitance (V = 0 V, f = 1 MHz)		CJ	—	18	_	pF
OUTPUT TRANSISTOR						
Collector-Emitter Dark Current (V <sub>CE</sub> = 10 V, T <sub>A</sub> = 25°C	4N25,26,27 4N28	ICEO	Ξ	1 1	50 100	nA
(V <sub>CE</sub> = 10 V, T <sub>A</sub> = 100°C)	All Devices	ICEO	_	1	_	μA
Collector-Base Dark Current (VCB = 10 V	)	ICBO	_	0.2	_	nA
Collector-Emitter Breakdown Voltage (IC =	= 1 mA)	V(BR)CEO	30	45	_	Volts
Collector-Base Breakdown Voltage (IC =	100 μA)	V(BR)CBO	70	100	_	Volts
Emitter-Collector Breakdown Voltage (IE =	= 100 μA)	V(BR)ECO	7	7.8	_	Volts
DC Current Gain (I <sub>C</sub> = 2 mA, V <sub>CE</sub> = 5 V)		hFE	-	500	-	-
Collector-Emitter Capacitance (f = 1 MHz,	V <sub>CE</sub> = 0)	CCE	-	7	_	pF
Collector-Base Capacitance (f = 1 MHz, V	(CB = 0)	CCB	-	19	-	pF
Emitter-Base Capacitance (f = 1 MHz, VE	B = 0)	CEB	-	9	_	pF
COUPLED						
Output Collector Current (IF = 10 mA, VCE	= 10 V) 4N25,26 4N27,28	IC (CTR)(2)	2 (20) 1 (10)	7 (70) 5 (50)	=	mA (%)
Collector-Emitter Saturation Voltage (IC =	2 mA, IF = 50 mA)	V <sub>CE(sat)</sub>	-	0.15	0.5	Volts
Tum-On Time (IF = 10 mA, V <sub>CC</sub> = 10 V, F	RL = 100 Ω)(3)	ton	-	2.8	-	μs
Turn-Off Time (IF = 10 mA, V <sub>CC</sub> = 10 V, F	RL = 100 Ω) <sup>(3)</sup>	toff	_	4.5	-	μs
Rise Time (IF = 10 mA, V <sub>CC</sub> = 10 V, R <sub>L</sub> =	100 Ω) <sup>(3)</sup>	۲r	-	1.2	_	μs
Fall Time (IF = 10 mA, $V_{CC}$ = 10 V, RL = 1	100 Ω) <sup>(3)</sup>	ŧ	-	1.3	_	μs
Isolation Voltage (f = 60 Hz, t = 1 sec)(4)		VISO	7500	-	_	Vac(pk)
Isolation Resistance (V = 500 V)(4)		RISO	1011	-	_	Ω
Isolation Capacitance (V = 0 V, f = 1 MHz)	(4)	CISO	-	0.2	_	pF

ELECTRICAL CHARACTERISTICS (TA = 25°C unless otherwise noted)(1)

Always design to the specified minimum/maximum electrical limits (where applicable).
 Current Transfer Ratio (CTR) = I/J = x 100%.
 For test circuit setup and waveforms, refer to Figure 11.
 For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.





TYPICAL CHARACTERISTICS

10

2

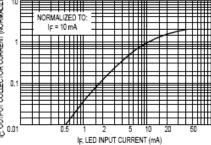
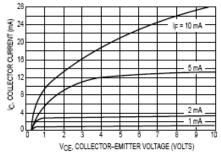
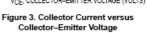


Figure 1. LED Forward Voltage versus Forward Current



NORMALIZED TO TA = 25°C





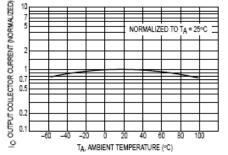


Figure 4. Output Current versus Ambient Temperature

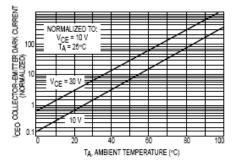


Figure 5. Dark Current versus Ambient Temperature

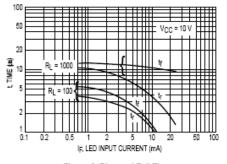


Figure 6. Rise and Fall Times (Typical Values)



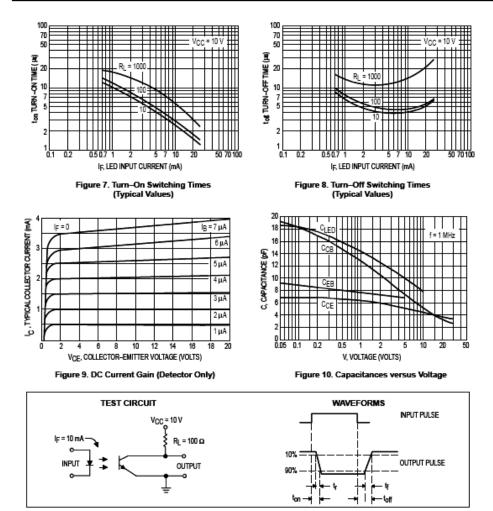
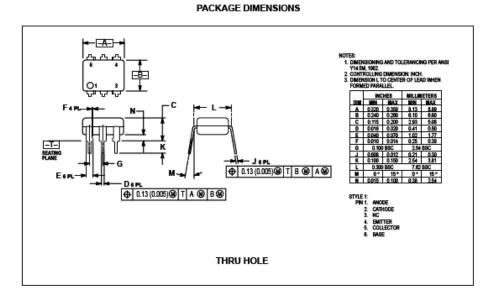
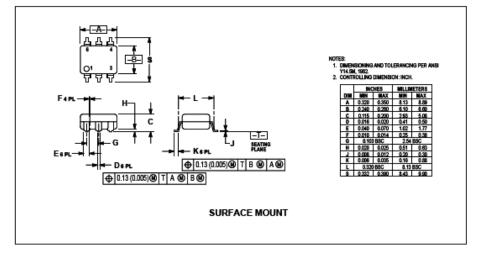


Figure 11. Switching Time Test Circuit and Waveforms

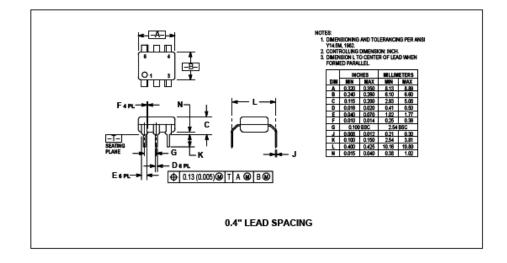






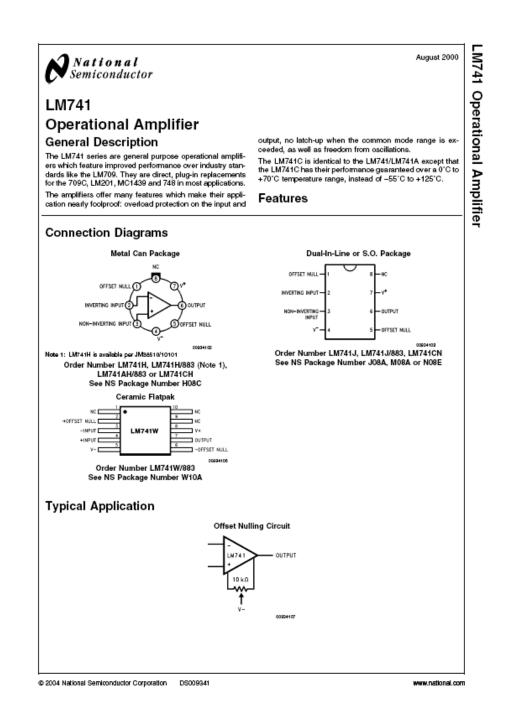
# 59





### **APPENDIX C**

### LM741 Datasheet



LM741

# Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

		LM741A		L	M741		L	.M741(	С		
Supply Voltag	je	±22V		3	22V			± 18V			
Power Dissip	ation (Note 3)	500 mW	1	50	0 mW		5	500 mV	v		
Differential In	put Voltage	±30V		-	-30V			±30V			
Input Voltage	(Note 4)	±15V		±15V				±15V			
Output Short	Circuit Duration	Continuo	us	Continuous			Co	ontinuo	us		
Operating Ter	mperature Range	-55°C to +1	-55°C	to +12	5°C	0.0	to +7	0°C			
Storage Tem	perature Range	-65°C to +1	50°C	-65°C	to +15	0°C	-65'	C to +1	50°C		
Junction Tem	perature	150°C		1	50°C			100°C			
Soldering Info	ormation										
N-Package	(10 seconds)	260°C		2	60°C			260°C			
J- or H-Pa	kage (10 seconds)	300.C		3	00°C			300°C			
M-Package											
Vapor Pt	nase (60 seconds)	215°C		2	15°C			215°C			
Infrared	(15 seconds)	215°C		2	15°C			215°C			
See AN-450	Surface Mounting Metho	ds and Their	Effect o	n Produc	t Relia	ibility" f	for othe	er meth	ods of		
soldering	-										
surface mour	it devices.										
ESD Tolerand	≫ (Note 8)	400V		4	.00V			400V			
Electrical Chara	acteristics (Note 5	)									
Parameter	Conditions		LM741	A LM74			1 LM7410			С	Units
											ł
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Input Offset Voltage	T <sub>A</sub> = 25°C	Min	Тур	Max	Min	Тур	Max	Min	Тур	мах	
Input Offset Voltage	T <sub>A</sub> = 25°C R <sub>S</sub> ≤ 10 kΩ	Min	Тур	Max	Min	Тур 1.0	Max 5.0	Min	Тур 2.0	мах 6.0	mV
Input Offset Voltage		Min	Тур 0.8	Max 3.0	Min			Min			mV mV
Input Offset Voltage	R <sub>S</sub> ≤ 10 kΩ	Min			Min			Min			
Input Offset Voltage	R <sub>S</sub> ≤ 10 kΩ R <sub>S</sub> ≤ 50Ω	Min			Min			Min			
Input Offset Voltage	R <sub>5</sub> ≤ 10 kΩ R <sub>5</sub> ≤ 50Ω T <sub>AMIN</sub> ≤ T <sub>A</sub> ≤ T <sub>AMAX</sub>	Min		3.0	Min			Min			mV
	$\label{eq:result} \begin{split} & \overrightarrow{R}_{S} \leq 10 \; \mathrm{k}\Omega \\ & \overrightarrow{R}_{S} \leq 50\Omega \\ & \overrightarrow{T}_{AMIN} \leq \overrightarrow{T}_{A} \leq \overrightarrow{T}_{AMAX} \\ & \overrightarrow{R}_{S} \leq 50\Omega \end{split}$	Min		3.0	Min		5.0	Min		6.0	mV mV mV
Average Input Offset	$\label{eq:result} \begin{split} & \overrightarrow{R}_{S} \leq 10 \; \mathrm{k}\Omega \\ & \overrightarrow{R}_{S} \leq 50\Omega \\ & \overrightarrow{T}_{AMIN} \leq \overrightarrow{T}_{A} \leq \overrightarrow{T}_{AMAX} \\ & \overrightarrow{R}_{S} \leq 50\Omega \end{split}$	Min		3.0 4.0	Min		5.0	Min		6.0	mV mV mV
Average Input Offset Voltage Drift	$\label{eq:result} \begin{split} & \overrightarrow{R}_{S} \leq 10 \; \mathrm{k}\Omega \\ & \overrightarrow{R}_{S} \leq 50\Omega \\ & \overrightarrow{T}_{AMIN} \leq \overrightarrow{T}_{A} \leq \overrightarrow{T}_{AMAX} \\ & \overrightarrow{R}_{S} \leq 50\Omega \end{split}$			3.0 4.0	Min		5.0	Min		6.0	mV mV mV
Average Input Offset Voltage Drift Input Offset Voltage	$\label{eq:rescaled_response} \begin{split} & \overrightarrow{R}_{S} \leq 10 \ k\Omega \\ & \overrightarrow{R}_{S} \leq 50\Omega \\ & \overrightarrow{T_{AMIN}} \leq \overrightarrow{T}_{A} \leq \overrightarrow{T}_{AMAX} \\ & \overrightarrow{R}_{S} \leq 50\Omega \\ & \overrightarrow{R}_{S} \leq 10 \ k\Omega \end{split}$			3.0 4.0	Min	1.0	5.0	Min	2.0	6.0	mV mV mV μV/°C
Average Input Offset Voltage Drift Input Offset Voltage Adjustment Range	$\label{eq:rescaled_response} \begin{split} & \overrightarrow{R}_{S} \leq 10 \ k\Omega \\ & \overrightarrow{R}_{S} \leq 50\Omega \\ & \overrightarrow{T_{AMIN}} \leq \overrightarrow{T}_{A} \leq \overrightarrow{T}_{AMAX} \\ & \overrightarrow{R}_{S} \leq 50\Omega \\ & \overrightarrow{R}_{S} \leq 10 \ k\Omega \end{split}$			3.0 4.0	Min	1.0	5.0	Min	2.0	6.0	mV mV mV
Average Input Offset Voltage Drift Input Offset Voltage Adjustment Range	$eq:rescaled_$		0.8	3.0 4.0 15	Min	1.0 ±15	5.0 6.0	Min	2.0 ±15	6.0	mV mV mV µV/°C mV
Average Input Offset Voltage Drift Input Offset Voltage Adjustment Range Input Offset Current	$eq:rescaled_$		0.8	3.0 4.0 15 30	Min	1.0 ±15 20	5.0 6.0 200	Min	2.0 ±15	6.0 7.5 200	mV mV μV/*C mV nA
Input Offset Voltage Average Input Offset Voltage Drift Input Offset Voltage Adjustment Range Input Offset Current Average Input Offset Current Drift	$eq:rescaled_$		0.8	3.0 4.0 15 30 70	Min	1.0 ±15 20	5.0 6.0 200	Min	2.0 ±15	6.0 7.5 200	mV mV μV/°C mV nA
Average Input Offset Voltage Drift Input Offset Voltage Adjustment Range Input Offset Current Average Input Offset	$eq:rescaled_$		0.8	3.0 4.0 15 30 70	Min	1.0 ±15 20	5.0 6.0 200	Min	2.0 ±15	6.0 7.5 200	mV mV μV/°C mV nA
Average Input Offset Voltage Drift Input Offset Voltage Adjustment Range Input Offset Current Average Input Offset Current Drift	$\begin{array}{c} \overline{P_{B}} \leq 10 \ k\Omega \\ \overline{P_{B}} \leq 50\Omega \\ \overline{T_{AMIN}} \leq \overline{T_{A}} \leq \overline{T_{AMAX}} \\ \overline{P_{B}} \leq 50\Omega \\ \overline{P_{B}} \leq 10 \ k\Omega \\ \end{array}$ $\overline{T_{A}} = 25^{\circ}C, \ V_{B} = \pm 20V \\ \overline{T_{A}} = 25^{\circ}C \\ \overline{T_{AMIN}} \leq \overline{T_{A}} \leq \overline{T_{AMAX}} \\ \overline{T_{A}} = 25^{\circ}C \\ \overline{T_{A}} = 25^{\circ}C \\ \end{array}$		0.8	3.0 4.0 15 30 70 0.5		1.0 ±15 20 85	5.0 6.0 200 500		2.0 ±15 20	6.0 7.5 200 300	mV mV mV mV mV mV πA
Average Input Offset Voltage Drift Input Offset Voltage Adjustment Range Input Offset Current Average Input Offset Current Drift Input Bias Current	$ \begin{array}{c} \overrightarrow{R}_{B} \leq 10 \ \text{k}\Omega \\ \overrightarrow{R}_{B} \leq 50\Omega \\ \hline \overrightarrow{T_{AMIN}} \leq \overrightarrow{T}_{A} \leq \overrightarrow{T}_{AMAX} \\ \overrightarrow{R}_{B} \leq 50\Omega \\ \overrightarrow{R}_{B} \leq 10 \ \text{k}\Omega \\ \hline \hline \overrightarrow{T}_{A} = 25^{\circ}\text{C}, \ \overrightarrow{V}_{B} = \pm 20\text{V} \\ \hline \overrightarrow{T}_{A} = 25^{\circ}\text{C} \\ \hline \overrightarrow{T_{AMIN}} \leq \overrightarrow{T}_{A} \leq \overrightarrow{T}_{AMAX} \\ \hline \end{array} $	/ ±10	0.8	3.0 4.0 15 30 70 0.5 80	0.3	1.0 ±15 20 85	5.0 6.0 200 500	0.3	2.0 ±15 20	6.0 7.5 200 300 500	mV mV mV/*C mV nA nA nA
Average Input Offset Voltage Drift Input Offset Voltage Adjustment Range Input Offset Current Average Input Offset Current Drift Input Bias Current		/ ±10	0.8	3.0 4.0 15 30 70 0.5 80		1.0 ±15 20 85 80	5.0 6.0 200 500		2.0 ±15 20 80	6.0 7.5 200 300 500	mV mV μV/°C mV nA nA/°C nA
Average Input Offset Voltage Drift Input Offset Voltage Adjustment Range Input Offset Current Average Input Offset Current Drift		7 ±10	0.8	3.0 4.0 15 30 70 0.5 80		1.0 ±15 20 85 80	5.0 6.0 200 500		2.0 ±15 20 80	6.0 7.5 200 300 500	mV mV μV/°C mV nA nA nA °C nA μA μΩ
Average Input Offset Voltage Drift Input Offset Voltage Adjustment Range Input Offset Current Average Input Offset Current Drift Input Bias Current	$eq:rescaled_$	7 ±10	0.8	3.0 4.0 15 30 70 0.5 80		1.0 ±15 20 85 80	5.0 6.0 200 500		2.0 ±15 20 80	6.0 7.5 200 300 500	mV mV μV/*C mV nA nA *C nA Ω ΩΩ
Average Input Offset Voltage Drift Input Offset Voltage Adjustment Range Input Offset Current Average Input Offset Current Drift Input Bias Current Input Resistance		7 ±10	0.8	3.0 4.0 15 30 70 0.5 80		1.0 ±15 20 85 80	5.0 6.0 200 500	0.3	2.0 ±15 20 2.0	6.0 7.5 200 300 500	mV mV mV mV mV mV mV nA nA'°C nA μA MΩ MΩ

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2

Parameter	Conditions		LM741	A		LM741		L	M741	C	Units
		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Large Signal Voltage Gain	$T_A = 25^{\circ}C, R_L \ge 2 k\Omega$										
	$V_8 = \pm 20V, V_0 = \pm 15V$	50									V/mV
	$V_{S} = \pm 15V, V_{O} = \pm 10V$				50	200		20	200		V/mV
	$T_{AMN} \le T_A \le T_{AMAX}$										
	$R_L \ge 2 k\Omega$ ,										
	$V_S = \pm 20V, V_O = \pm 15V$	32									V/mV
	$V_{S} = \pm 15V, V_{O} = \pm 10V$				25			15			V/mV
	$V_{S} = \pm 5V, V_{O} = \pm 2V$	10									V/mV
Output Voltage Swing	$V_8 = \pm 20V$										
	$R_L \ge 10 k\Omega$	±16									v
	$R_L \ge 2 k\Omega$	±15									v
	V <sub>S</sub> = ±15V										
	$R_L \ge 10 k\Omega$				±12	±14		±12	±14		v
	R <sub>L</sub> ≥2kΩ	10	25	35	±10	±13 25		±10	±13 25		v
Output Short Circuit Current	T <sub>A</sub> = 25'C	10	25	35 40		25			25		mA
Common-Mode	$T_{AMIN} \le T_A \le T_{AMAX}$	10		40							mA
	$T_{AMIN} \le T_A \le T_{AMAX}$				70	90		70	90		dB
Rejection Ratio	R <sub>S</sub> ≤ 10 kΩ, V <sub>CM</sub> = ±12V R <sub>S</sub> ≤ 50Ω, V <sub>CM</sub> = ±12V	80	95		10	90		70	90		dВ
Supply Voltage Rejection	$T_{aMIN} \le T_A \le T_{aMAX}$	~~~	95								uр
Ratio	$V_s = \pm 20V$ to $V_s = \pm 5V$										
- Kabo	R <sub>s</sub> ≤ 50Ω	86	96								dB
	R <sub>s</sub> ≤ 10 kΩ				77	96		77	96		dB
Transient Response	T <sub>A</sub> = 25°C, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		μs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 6)	T <sub>A</sub> = 25°C	0.437	1.5								MHz
Slew Rate	T <sub>A</sub> = 25°C, Unity Gain	0.3	0.7			0.5			0.5		V/µs
Supply Current	T <sub>A</sub> = 25°C					1.7	2.8		1.7	2.8	mA
Power Consumption	T <sub>A</sub> = 25°C										
	$V_8 = \pm 20V$		80	150							mW
	V <sub>S</sub> = ±15V					50	85		50	85	mW
LM741A	$V_{S} = \pm 20V$										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741	$V_{S} = \pm 15V$										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

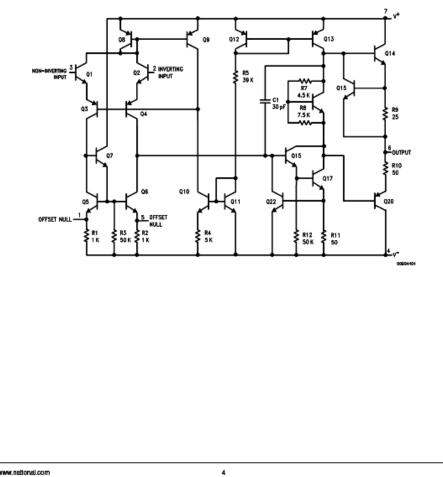
LM741

Electrical Characteristics (Note 5) (Continued) Note 3: For operation at elevated temperatures, these devices must be denated based on thermal resistance, and T<sub>i</sub> max. (listed under "Absolute Maxim Note 3: For operation at elevated temperatures, the Ratings"),  $T_j=T_A+(e_{jA},P_D).$ 

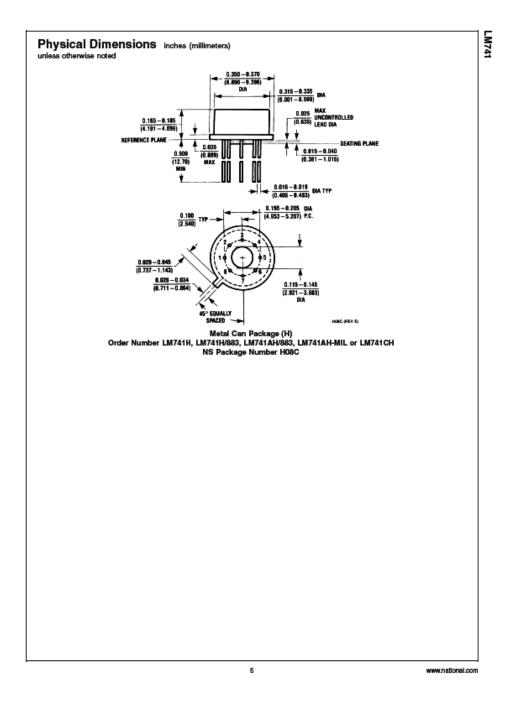
Thermal Resistance	Cerdip (J)	DIP (N)	HO8 (H)	SO-8 (M)
θ <sub>jA</sub> (Junction to Ambient)	100°C/W	100°C/W	170°C/W	195°C/W
θ <sub>jC</sub> (Junction to Case)	N/A	N/A	25°C/W	N/A

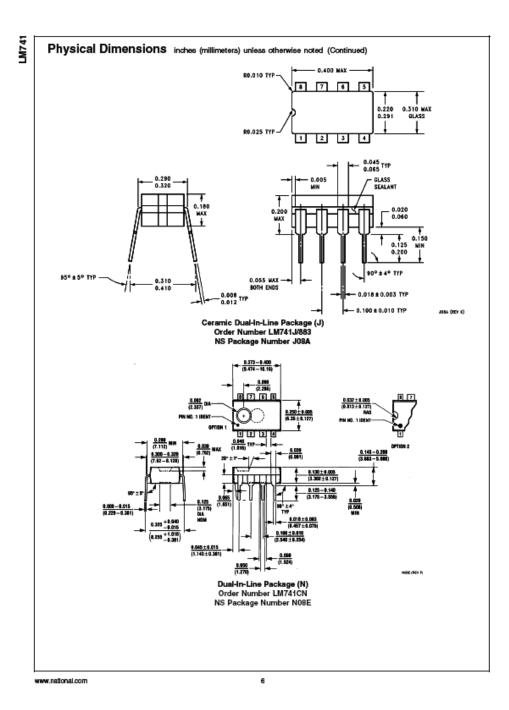
Note 4: For supply voltages loss frant ±15V, the absolute maximum input voltage is equal to the supply voltage. Note 5: Unless otherwise specified, these specifications apply for Vs = ±15V, -55°C  $\leq$  T<sub>A</sub>  $\leq$  +125°C (UM741/LM741A). For the LM741C/LM741E, these specifications are limited to 0°C  $\leq$  T<sub>A</sub>  $\leq$  +70°C. Note 5: Calculated value from: BW (MHz) = 0.35675550 Time(jus). Note 7: For mitiary specifications are PETS71X for UM741 and RETS741AX for LM741A. Note 8: Human body model 1.5 KQ in series with 100 pF:

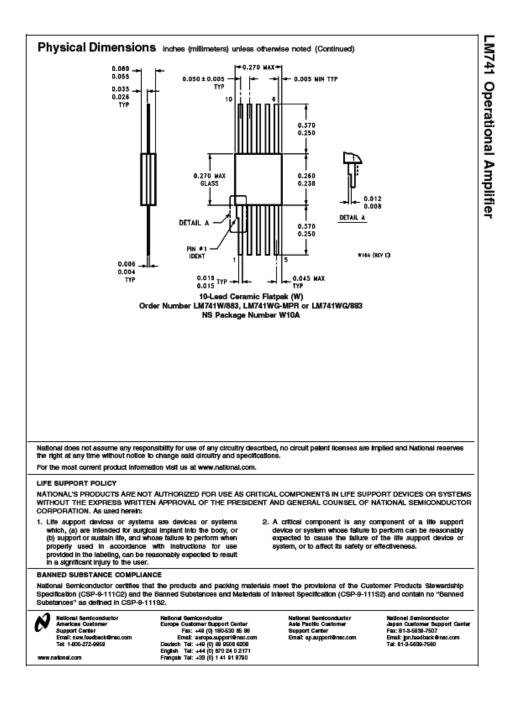
### Schematic Diagram



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# APPENDIX D 16F877A Datasheet



# PIC16F87XA

### 28/40/44-Pin Enhanced Flash Microcontrollers

#### Devices Included in this Data Sheet:

- PIC16F873A
   PIC16F876A
   PIC16F876A
   PIC16F877A
- FIC10F6/4A

#### High-Performance RISC CPU:

- Only 35 single-word instructions to learn
- · All single-cycle instructions except for program
- branches, which are two-cycle • Operating speed: DC – 20 MHz clock input
- DC 200 ns instruction cycle • Up to 8K x 14 words of Flash Program Memory, Up to 368 x 8 bytes of Data Memory (BAM)
- Up to 388 × 8 bytes of Data Memory (RAM), Up to 256 × 8 bytes of EEPROM Data Memory Pinout compatible to other 28-pin or 40/44-pin
- PIC16CXXX and PIC16FXXX microcontrollers

#### Peripheral Features:

Timer0: 8-bit timer/counter with 8-bit prescaler

- Timer1: 16-bit timer/counter with prescaler, can be incremented during Sleep via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period
  register, prescaler and postscaler
- Two Capture, Compare, PWM modules
- Capture is 16-bit, max. resolution is 12.5 ns
   Compare is 16-bit, max. resolution is 200 ns
   PWM max. resolution is 10-bit
- Synchronous Serial Port (SSP) with SPI™ (Master mode) and I<sup>2</sup>C™ (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
- Parallel Slave Port (PSP) 8 bits wide with external RD, WR and CS controls (40/44-pin only)
- Brown-out detection circuitry for Brown-out Reset (BOR)

#### Analog Features:

- 10-bit, up to 8-channel Analog-to-Digital Converter (A/D)
- Brown-out Reset (BOR)
- Analog Comparator module with:
   Two analog comparators
- Programmable on-chip voltage reference (VREF) module
- Programmable input multiplexing from device inputs and internal voltage reference
- Comparator outputs are externally accessible

#### Special Microcontroller Features:

- · 100,000 erase/write cycle Enhanced Flash
- program memory typical
- 1,000,000 erase/write cycle Data EEPROM memory typical
- Data EEPROM Retention > 40 years
- Self-reprogrammable under software control
- In-Circuit Serial Programming<sup>™</sup> (ICSP<sup>™</sup>) via two pins
- Single-supply 5V In-Circuit Serial Programming
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- · Programmable code protection
- Power saving Sleep mode
- Selectable oscillator options
- · In-Circuit Debug (ICD) via two pins

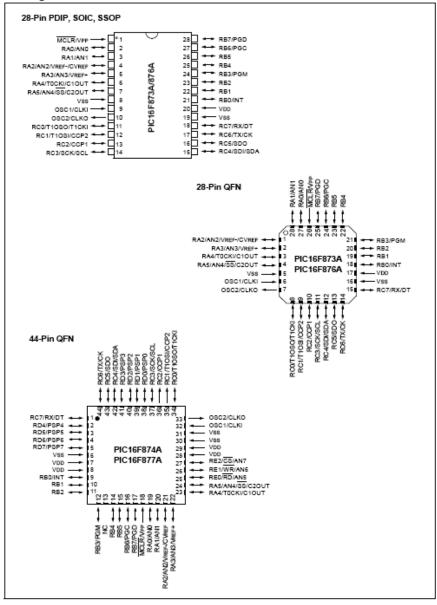
#### CMOS Technology:

- Low-power, high-speed Flash/EEPROM
- technology
- Fully static design
- Wide operating voltage range (2.0V to 5.5V)
- Commercial and Industrial temperature ranges
- Low-power consumption

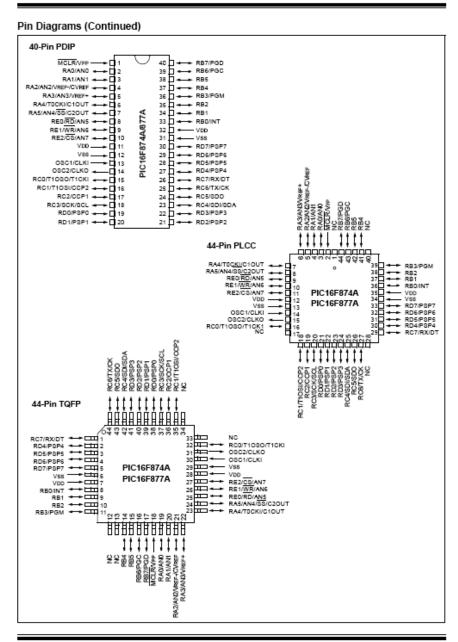
	Program Memory		Data EEPROM 10-bit CCP		ISSP		Timers					
Device	Bytes	# Single Word Instructions	SRAM (Bytes)	(Bytes)	I/O	A/D (ch)		SPI	Master I <sup>2</sup> C	USART	8/16-bit	Comparators
PIC16F873A	7.2K	4096	192	128	22	5	2	Yes	Yes	Yes	2/1	2
PIC16F874A	7.2K	4096	192	128	33	8	2	Yes	Yes	Yes	2/1	2
PIC16F876A	14.3K	8192	368	256	22	5	2	Yes	Yes	Yes	2/1	2
PIC16F877A	14.3K	8192	368	256	33	8	2	Yes	Yes	Yes	2/1	2

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### Pin Diagrams



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#### DEVICE OVERVIEW 1.0

This document contains device specific information about the following devices:

- PIC16F873A
- PIC16F874A PIC16F876A
- PIC16F877A

PIC16F873A/876A devices are available only in 28-pin packages, while PIC16F874A/877A devices are available in 40-pin and 44-pin packages. All devices in the PIC16F87XA family share common architecture with the following differences:

- The PIC16F873A and PIC16F874A have one-half of the total on-chip memory of the PIC16F878A and PIC16F877A
- · The 28-pin devices have three I/O ports, while the 40/44-pin devices have five
- · The 28-pin devices have fourteen interrupts, while the 40/44-pin devices have fifteen
- The 28-pin devices have five A/D input channels, while the 40/44-pin devices have eight
- The Parallel Slave Port is implemented only on
- the 40/44-pin devices

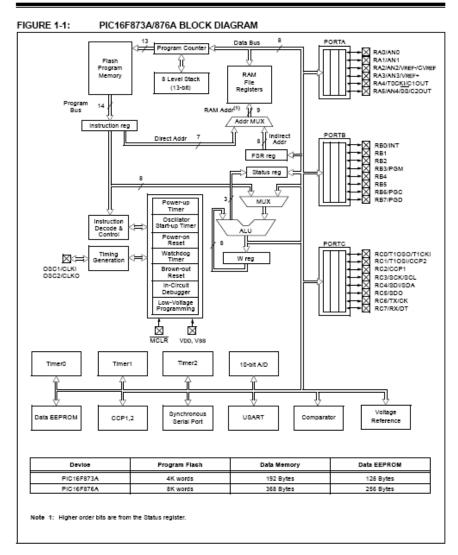
TABLE 1-1:	PIC16F87XA	DEVICE FEATURES

The available features are summarized in Table 1-1. Block diagrams of the PIC16F873A/876A and PIC167874/4877A devices are provided in Figure 1-1 and Figure 1-2, respectively. The pinouts for these device families are listed in Table 1-2 and Table 1-3.

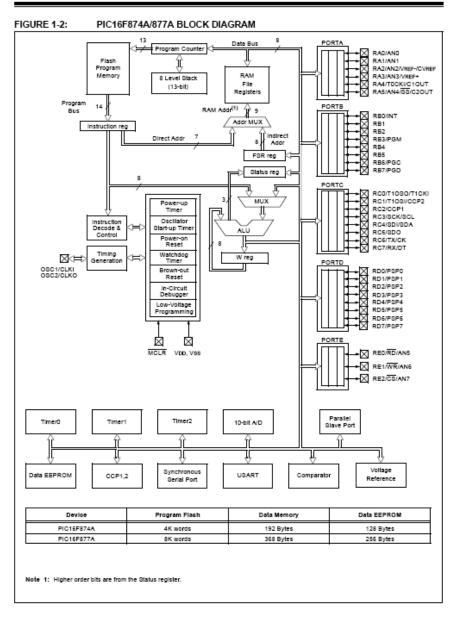
Additional information may be found in the PICmicro<sup>®</sup> Mid-Range Reference Manual (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip web site. The Reference Manual should be considered a complementary document to this data sheet and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

Key Features	PIC16F873A	PIC16F874A	PIC16F876A	PIC16F877A
Operating Frequency	DC – 20 MHz			
Resets (and Delays)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)
Flash Program Memory (14-bit words)	4K	4K	8K	8K
Data Memory (bytes)	192	192	368	368
EEPROM Data Memory (bytes)	128	128	256	256
Interrupts	14	15	14	15
I/O Ports	Ports A, B, C	Ports A, B, C, D, E	Ports A, B, C	Ports A, B, C, D, E
Timers	3	3	3	3
Capture/Compare/PWM modules	2	2	2	2
Serial Communications	MSSP, USART	MSSP, USART	MSSP, USART	MSSP, USART
Parallel Communications	-	PSP	_	PSP
10-bit Analog-to-Digital Module	5 input channels	8 input channels	5 input channels	8 input channels
Analog Comparators	2	2	2	2
Instruction Set	35 Instructions	35 Instructions	35 Instructions	35 Instructions
Packages	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 44-pin PLCC 44-pin TQFP 44-pin QFN	28-pin PDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 44-pin PLCC 44-pin TQFP 44-pin QFN

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	PDIP, SOIC, SSOP Pin#	QFN Pin#	І/О/Р Туре	Buffer Type	Description
OSC1/CLKI OSC1	9	6	-	ST/CMOS <sup>(3)</sup>	Osciliator crystal or external clock input. Osciliator crystal input or external clock source input. ST buffer when configured in RC mode; otherwise CMOS.
CLKI			I		External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
OSC2/CLKO OSC2	10	7	0	-	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO			0		In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate
MCLR/VPP MCLR	1	26	I	ST	Master Clear (input) or programming voitage (output). Master Clear (Reset) input. This pin is an active low Reset to the device.
VPP			Р		Programming voltage input.
					PORTA is a bidirectional I/O port.
RAO/ANO RAO ANO	2	27	1/0	TTL	Digital I/O. Analog Input 0.
RA1/AN1 RA1 AN1	3	28	1/0	TTL	Digital I/O. Analog Input 1.
RA2/AN2/VREF-/	4	1		TTL	Digital I/O.
RA2			1		Analog Input 2.
AN2 VREF- CVREF			0		A/D reference voltage (Low) Input. Comparator VREF output.
RA3/AN3/VREF+	5	2		TTL	
RA3			1/0		Digital I/O.
AN3 VREF+					Analog Input 3. A/D reference voltage (High) Input.
RA4/TOCKI/C1OUT	6	3		ST	
RA4 TOCKI C1OUT			1/0		Digital I/O – Open-drain when configured as output. Timer0 external clock input. Comparator 1 output.
RA5/AN4/SS/C2OUT	7	4		TTL	
RA5			I/O		Digital I/O.
AN4 SS					Analog Input 4. SPI slave select input
C2OUT			6		SPI slave select input. Comparator 2 output.
.egend: I - Input	0 <b>-</b> ou	tput	VC	) – input/outpu	
— - Not u		TTL Inpu		r = Schmitt Trig	
					s the external interrupt. Il Programming mode.

Pin Name	PDIP, SOIC, SSOP Pin#	QFN Pin#	І/О/Р Туре	Buffer Type	Description
					PORTB is a bidirectional I/O port. PORTB can be software
				(1)	programmed for internal weak pull-ups on all inputs.
RB0/INT	21	18	1/0	TTL/ST <sup>(1)</sup>	B1-11-1 1/B
RB0 INT			1		Digital I/O. External Interrupt.
RB1	22	19	1/0	TTL	Digital I/O.
RB2	23	20	1/0	TTL	Digital I/O.
RB3/PGM	24	21		TTL	District VD
RB3 PGM			1/0		Digital I/O. Low-voltage (single-supply) ICSP programming enable pir
	25	22	1/0	TTL	
RB4					Digital I/O.
RB5	26	23	1/0	TTL	Digital I/O.
RB6/PGC	27	24		TTL/ST(2)	
RB6			1/0		Digital I/O.
PGC			'		in-circuit debugger and ICSP programming clock.
RB7/PGD RB7	28	25	1/0	TTL/ST(2)	Distant NO
PGD			10		Digital I/O. In-circuit debugger and ICSP programming data.
FGD					PORTC is a bidirectional I/O port.
					PORTC is a bidirectional I/O port.
RCD/T1OSO/T1CKI RCD	11	8	1/0	ST	Digital I/O.
T1050			0		Timer1 oscillator output.
TICKI			ĭ		Timer1 external clock input.
RC1/T1OSI/CCP2	12	9		ST	
RC1		-	1/0		Digital I/O.
T10SI			1		Timer1 oscillator input.
CCP2			1/0		Capture2 Input, Compare2 output, PWM2 output.
RC2/CCP1	13	10		ST	
RC2			1/0		Digital I/O.
CCP1			1/0		Capture1 Input, Compare1 output, PWM1 output.
RC3/SCK/SCL	14	11		ST	
RC3 SCK			1/0		Digital I/O. Synchronous serial clock input/output for SPI mode.
SCL			1/0		Synchronous serial clock input/output for SP1 mode. Synchronous serial clock input/output for I <sup>2</sup> C mode.
RC4/SDI/SDA	15	12		ST	Synonionous senarolosis inputoupation rio mode.
RC4	15	12	1/0	31	Digital I/O.
SDI					SPI data In.
SDA			1/0		I <sup>2</sup> C data I/O.
RC5/SDO	16	13		ST	
RC5			1/0		Digital I/O.
SDO			0		SPI data out.
RC6/TX/CK	17	14		ST	
RC6			1/0		Digital I/O.
тх ск			0		USART asynchronous transmit.
			1/0		USART1 synchronous clock.
RC7/RX/DT RC7	18	15	1/0	ST	Diata NO
RC7			10		Digital I/O. USART asynchronous receive.
DT			10		USART synchronous data.
Vas	8, 19	5.6	P	_	Ground reference for logic and I/O pins.
VDD	20	17	P		Positive supply for logic and I/O pins.
				_	
Legend: I - Input	0 - 0U			) – input/outpu 5 – Sobmitt Tri	
— = Notu Note 1: This buffe		TTL Inpu		r = Schmitt Tri	gger input s the external interrupt.

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Pin Name	PDIP Pin#	PLCC Pin#	TQFP Pin#	QFN Pin#	I/O/P Typə	Buffer Type	Description
OSC1/CLKI OSC1	13	14	30	32	I	ST/CMOS <sup>(4)</sup>	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode;
							otherwise CMOS.
CLKI					1		External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
OSC2/CLKO	14	15	31	33		-	Oscillator crystal or clock output.
OSC2					0		Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO					0		In RC mode, OSC2 pin outputs CLKO, which
							has 1/4 the frequency of OSC1 and denotes th Instruction cycle rate.
MCLR/VPP MCLR	1	2	18	18	Т	ST	Master Clear (input) or programming voltage (output Master Clear (Reset) input. This pin is an activity
VPP					Р		low Reset to the device. Programming voltage input.
							PORTA is a bidirectional I/O port.
RA0/AN0	2	3	19	19		TTL	
RAD AND					1/0		Digital I/O. Analog Input 0.
RA1/AN1	3	4	20	20		TTL	rine g input e.
RA1	-				I/O		Digital I/O.
AN1					1		Analog Input 1.
RA2/AN2/VREF-/CVREF RA2	4	5	21	21	1/0	TTL	Digital I/O.
AN2					10		Analog Input 2.
VREF-					1		A/D reference voltage (Low) Input.
CVREF	_				0		Comparator VREF output.
RA3/AN3/VREF+ RA3	5	6	22	22	1/0	TTL	Digital I/O.
AN3					10		Analog Input 3.
VREF+					1		A/D reference voltage (High) input.
RA4/TECKI/C1OUT	6	7	23	23		ST	
RA4					1/0		Digital I/O – Open-drain when configured as output.
тоскі					1		TimerD external clock input.
C1OUT					0		Comparator 1 output.
RA5/AN4/SS/C2OUT	7	8	24	24		TTL	
RA5 AN4					1/0		Digital I/O.
AN4 SS							Analog Input 4. SPI slave select Input.
C2OUT					ō		Comparator 2 output.
Legend: I - Input — - Not use		- outpu			input/out Schmitt 1	, put P Trigger input	- power
						as the extern	al interrupt.
2: This buffer l							

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Pin Name	PDIP Pin#	PLCC Pin#	TQFP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
							PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-up on al inputs.
RB0/INT RB0 INT	33	36	8	9	1/0 1	TTL/ST <sup>(1)</sup>	Digital I/O. External interrupt.
RB1	34	37	9	10	1/O	TTL	Digital I/O.
RB2	35	38	10	11	1/0	TTL	Digital I/O.
RB3/PGM RB3 PGM	36	39	11	12	1/0 1	TTL	Digital I/O. Low-voltage ICSP programming enable pin.
R84	37	41	14	14	1/O	TTL	Digital I/O.
RB5	38	42	15	15	1/0	TTL	Digital I/O.
RB6/PGC RB6 PGC	39	43	16	16	1/0 1	TTL/ST <sup>(2)</sup>	Digital I/O. In-circuit debugger and ICSP programming clock
RB7/PGD RB7 PGD	40	44	17	17	1/0 1/0	TTL/ST <sup>(2)</sup>	Digital I/O. In-circuit debugger and ICSP programming data

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Pin Name	PDIP Pln#	PLCC Pin#	TQFP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
	+						PORTC is a bidirectional I/O port.
RCD/T10SO/T1CKI RCD T10SO T1CKI	15	16	32	34	1/0 0 1	ST	Digital I/O. Timeri oscillator output. Timeri external clock input.
RC1/T1OSI/CCP2 RC1 T1OSI CCP2	16	18	35	35	1/0   1/0	ST	Digital I/O. Timer1 oscillator input. Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1 RC2 CCP1	17	19	36	36	1/0 1/0	ST	Digital I/O. Capture1 Input, Compare1 output, PWM1 output.
RC3/SCK/SCL RC3 SCK SCL	18	20	37	37	1/0 1/0 1/0	ST	Digital I/O. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I <sup>2</sup> C mode.
RC4/SDI/SDA RC4 SDI SDA	23	25	42	42	1/0 1 1/0	ST	Digital I/O. SPI data In. I <sup>2</sup> C data I/O.
RC5/SDO RC5 SDO	24	26	43	43	1/0 0	ST	Digitai I/O. SPI data out.
RC6/TX/CK RC6 TX CK	25	27	44	44	1/0 0 1/0	ST	Digital I/O. USART asynchronous transmit. USART1 synchronous clock.
RC7/RX/DT RC7 RX DT	26	29	1	1	1/0 1 1/0	ST	Digital I/O. USART asynchronous receive. USART synchronous data.

Note 1: This buffer is a Schmitt Trigger input ST - Schmitt Trigger input
 This buffer is a Schmitt Trigger input when configured as the external interrupt.
 This buffer is a Schmitt Trigger input when configured in Serial Programming mode.
 This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

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Pin Name	PDIP Pln#	PLCC Pin#	TQFP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
							PORTD is a bidirectional I/O port or Parallel Slave
							Port when interfacing to a microprocessor bus.
RD0/PSP0	19	21	38	38		ST/TTL <sup>(3)</sup>	
RD0					I/O		Digital I/O.
PSPD					1/0		Parallel Slave Port data.
RD1/PSP1	20	22	39	39		ST/TTL <sup>(3)</sup>	
RD1					I/O		Digital I/O.
PSP1					1/0		Parallel Slave Port data.
RD2/PSP2	21	23	40	40		ST/TTL <sup>(3)</sup>	
RD2					1/0		Digital I/O.
PSP2					1/0		Parallel Slave Port data.
RD3/PSP3	22	24	41	41		ST/TTL <sup>(3)</sup>	
RD3					1/0		Digital I/O.
PSP3					1/0		Parallel Slave Port data.
RD4/PSP4	27	30	2	2		ST/TTL <sup>(3)</sup>	
RD4 PSP4					1/0		Digital I/O. Parallel Slave Port data.
					10		Paraller Slave Port data.
RD5/PSP5	28	31	3	3		ST/TTL <sup>(3)</sup>	
RD5 PSP5					1/0		Digital I/O. Parailei Slave Port data.
					10	ST/TTL <sup>(3)</sup>	Parallel Slave Port data.
RD6/PSP6 RD6	29	32	4	4	1/0	SI/TIL	DI-16-11/D
PSP6					1/0		Digital I/O. Parallel Slave Port data.
RD7/PSP7	30	33	5	5		ST/TTL <sup>(3)</sup>	Parallel olare Port data.
RD7	30	33	5	5	1/0	SI/TIL	Digital I/O.
PSP7					1/0		Parallel Slave Port data.
1017							PORTE is a bidirectional I/O port.
RE0/RD/AN5		9				ST/TTL <sup>(3)</sup>	PORTE is a bidirectional ito port.
RED/RD/ANS RED	8	9	25	25	1/0	SI/TILW	Diata IVO
RD					10		Digital I/O. Read control for Parallel Slave Port.
AN5					l i		Analog Input 5.
RE1/WR/AN6	9	10	26	26	-	ST/TTL <sup>(3)</sup>	
RE1	1	10	20	20	1/0	31/112	Digital I/O.
WR					1		Write control for Parallel Slave Port.
AN6					1		Analog Input 6.
RE2/CS/AN7	10	11	27	27		ST/TTL <sup>(3)</sup>	
RE2					1/O		Digital I/O.
CS					1		Chip select control for Parallel Slave Port.
AN7					1		Analog Input 7.
Vss	12, 31	13, 34	6, 29	6, 30, 31	P	-	Ground reference for logic and I/O pins.
Voo	11, 32	12, 35	7,28	7, 8, 28, 29	Р	-	Positive supply for logic and I/O pins.
NC	+	1, 17,	12.13.	13			These pins are not internally connected. These pins
	-	1, 17, 28, 40	12,13, 33, 34	15	-	-	should be left unconnected.

Legend: I = Input O = output I/O = input/output P = power — Not used TTL = TTL Input ST = Schmitt Trigger Input Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt. 2: This buffer is a Schmitt Trigger input when used in Serial Programming mode. 3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

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