DESIGN AND DEVELOP CURRENT LIMITER FOR MOSFET DURING OVERVOLTAGE OPERATION.

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This thesis is submitted as partial fulfillment of the requirements for the award of the Bachelor of Electrical Engineering (Power Systems)

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JUNE, 2012

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Date : 21TH JUNE 2012.

Specially dedicated, in thankful appreciation, encouragement and understandings to my beloved family and those who contributed for this project.

ACKNOWLEDGEMENT

In the name of God, Most Beneficent, Most Merciful. Alhamdulillah, all the praise and thanks are to Him, the Lord of the universe and peace upon His Messenger Muhammad S.A.W., the last prophets and the righteous followers, his family and companions, and those follow the guidance until the Day of Judgment.

First and foremost, a special gratitude and thank to my supervisor Mr. Ramdan bin Razali, who helped me a lot for the project research, for all the support, continuous patience, and supervision given throughout the project.

I would like to give my appreciation to Dr. Hamdan bin Daniyal and Mr. Azri for their valuable time spent on guiding me during the completion of this project. Their guidance and help are indeed very much appreciated.

Apart from that, I would like to my beloved parents, Mamat bin Jusoh and Haliyah binti Md. Zain, for their support and motivation during done final year project.

I am also thankful to my housemates, lecture mates and friends especially Fatinah binti Abdul Ghani and Ayu Annur Fetrah binti Yusoff for their helping hand, encouragement and knowledge sharing. Throughout the period of accomplishing this project, those persons are very helpful on providing me lot of brilliant ideas.

ABSTRACT

Gate drive circuit is important for the purpose of controlling signal to the gate of power switch. Currently, most gate drive circuit is designed without current control; as such the overload, short circuit or overvoltage will cause permanent damage to the power switch. Protecting the power switch from being damage from the overload, short circuit and overvoltage must be considered seriously. In this project, the new design of gate drive circuit with current limiter to controls the gate voltage signal to the MOSFET and limits the current flow through the Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) during overvoltage. It will use the current limiter circuit to control voltage supplied to the gate of power switch and thus limit the amount of current flow to the MOSFET during overvoltage operation. Hence the gate drive circuit with current limiter is very important to protect the power switch from over current.

ABSTRAK

Litar pemacu adalah penting bagi tujuan mengawal isyarat pintu suis kuasa. Pada masa ini, litar pemacu direka tanpa kawalan arus; beban yang berlebihan, litar pintas atau voltan yang berlebihan akan menyebabkan kerosakan kekal kepada suis kuasa. Melindungi suis kuasa daripada kerosakan akibat arus berlebihan, litar pintas dan voltan yang berlebihan perlu dipertimbangkan secara serius. Dalam projek ini, reka bentuk baru litar pemacu pintu dengan pengehad arus untuk mengawal isyarat voltan pintu MOSFET dan menghadkan pengaliran arus melalui MOSFET semasa voltan berlebihan. Ia akan menggunakan litar arus penghad untuk mengawal voltan yang dibekalkan kepada pintu suis kuasa dan dengan itu menghadkan jumlah aliran arus MOSFET semasa operasi voltan berlebihan. Oleh itu litar litar pemacu dengan pengehad arus adalah sangat penting untuk melindungi suis kuasa dari lebih arus melaluinya.

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LIST OF SYMBOLS

BJT	Bipolar Junction Transistor
FKEE	Faculty of Electrical and Electronics
FYP	Final Year Project
Id	Drain Current
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
PWM	Pulse Width Modulation
VDS	Drain to Source Voltage
VGS	Gate to Source Voltage

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1. General

Gate driver is an important circuit for electronic switches such as Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET), insulated gate bipolar transistor (IGBT), Bipolar Junction Transistor (BJT) and others. It functions to control switching output. The gate drive circuit produces control signal fed to the power switch. Currently, most base drive circuit is designed without current control; as such the overload, short circuit or overvoltage will cause permanent damage to the power switch. Protecting the power switch from being damage from the overload, short circuit or overvoltage must be considered seriously. Gate drive circuit with current limiter is needed to design to limit current to the power switch whenever overvoltage occurs. Many researchers continue to work on this problem.

1.2. Project Objective

There are several objectives of this project. The objectives of this project are as below:

1) To design and implement the gate drive circuit that controls the gate voltage signal to the MOSFET.
2) To incorporate the current limiter to the gate drive circuit which limits the current flow through the MOSFET during overvoltage operation.

1.3. Scopes of the project

The scope of the thesis is used as the guideline of the project. In this project, a complete hardware of a gate drive circuit had been implemented and constructed. In order to achieve the objective, there are several scope had been outlined.

Firstly, the concept of driver circuit is being studied in order to know its function as well as its major field of application. A number of articles regarding the driver circuit are read to obtain the basic ideal of the driver circuit and improvement that have been done in driver circuit. Gate drive circuit is design:

1) R2,C= On time
2) R3 = Off-time
3) R5 =To control pulse length (switching frequency)

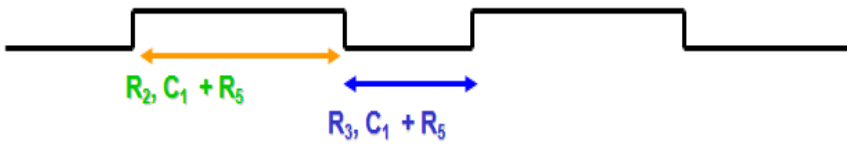


Figure 1.1: Signal of gate driver

Secondly, current limiter circuit is design to limit drain current of IRF520 n-channel MOSFET by limiting gate to threshold voltage (Vgs).

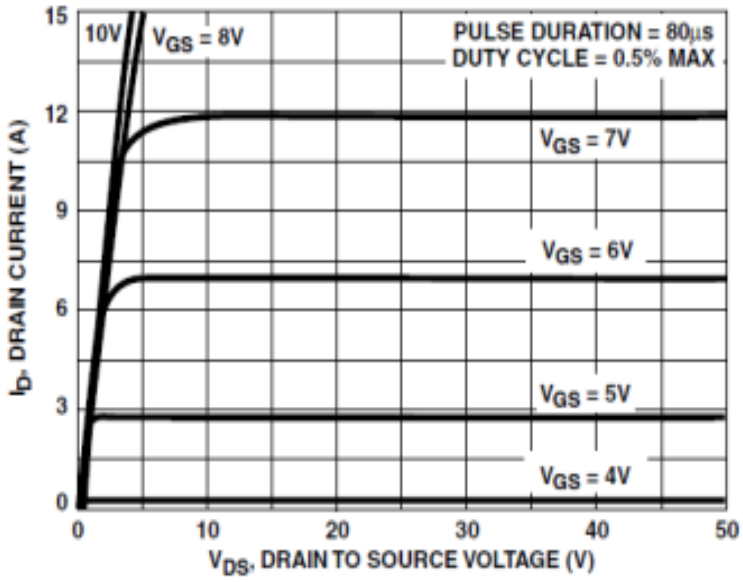


Figure 1.2: Output Characteristic of IRF520 n-channel MOSFET

Then, design the simulation circuit of gate drive and current limiter circuit by using PROTEUS software. The power MOSFET IRF520 n-channel enhancement mode with current drain rating at 9.2A is used as power witch. Then do the analysis on the output waveform.

Next, construct the gate drive and current limiter circuit on breadboard based on collector data from simulation part and literature review.

Finally, the complete hardware implementation of gate drive circuit will be carried out in order to confirm that the meets the objectives of this project.

1.4. Main Contributions of the Project

The main contributions of the project is design and develop new current limiter gate drive circuit which can limit current flow through the inverter with to prevent high current flow that can cause damage the power switch.

1.5 Report Organization

This thesis consists of five chapters. **Chapter 1** of the report introduces the subject matter with a brief review of the project. The objective, scopes, main contribution, thesis outline and Gantt chart of the report are presented.

Chapter 2 deals with literature review, where, the previous works related to the subject are discussed. This includes the gate drive circuit design and technique to prevent the overload and short circuit of load by limiting the current.

Chapter 3 describes the methodology which explains in flow chart on how to do this project step by step. Besides that, this chapter also discusses the circuit design and its operation. Then, the simulation of the circuit using Pspice software is designed. Besides that, describes hardware development of experimental setup for gate drive circuit and current limiting circuit in the laboratory for the implementation and verification of the proposed method.

Chapter 4 describes the expected result obtained from the simulation and the data from simulation is analyzed. Comparison between the simulation and experimental results are made in order to achieve the objective of project. The experimental validation and results are presented and discussed.

Finally, **chapter 5** summarizes the achievements of this research and the recommendations for future work.

1.6 Gantt Chart

Table 1 Schedule for FYP 1

NO.	ACTIVITIES	W1	W2	W3	W4	W5	W6	W7	W8	W9	W10	W11	W12	W13	W14	W15
1	PSM 1 briefing session	■														
2	Find supervisor and project title		■	■												
3	Meet supervisor to discuss the project		■	■	■	■	■	■	■	■	■	■	■	■	■	■
4	Register title and submit abstrack			■												
5	Literature review				■	■	■	■	■	■						
6	Submit proposal and slide presentation										■					
7	PSM 1 seminar presentation											■				
8	Design the simulation												■	■	■	
9	Submit report and log book															■

Table 2 Schedule for FYP 2

NO.	ACTIVITIES	W 1	W 2	W 3	W 4	W 5	W 6	W 7	W 8	W 9	W 10	W 11	W 12	W 13	W 14	W 15
1	PSM 2 briefing session															
2	Meet supervisor to disscuss the project															
3	Order the components															
4	Implement gate drive circuit															
5	Data analysis															
6	Submit draft 1															
7	Submit draft 2															
8	Submit final draf and logbook															
9	Submit slide presentation															
10	PSM 2 seminar presentation															
11	Submit report															

1.7 Conclusion

As a conclusion, this chapter is discuss about general of this project, the objectives of this project, scope and main contribution of the project, report organization and gantt chart as schedule of project progress. For next chapter, some literature review is discussed with study the previous research about this project to get idea to do.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Some research has been done to obtain and gain some information about the project. It is to compare the previous with this project to make some improvement or to try the method that has been used for the previous project.

2.2 Gate Driver Design

Many researchers find the solution of protection against overload and short circuit. Some researchers allow the fault current to reach the limit and then initiated to shut off the system. This method cause the fault current increased thus several devices damage although it takes a temporary time. (Werner, Mario and Martin,1989) [1]

Another researcher designs a MOSFET gate driver as Figure 2.1 below. To turn on the driver, MOSFET need V_{GS}=+15V and 0V to turn off. In this circuit, PWM signal from control circuit is flow to the LM311 amplifier. This amplifier served with open collector output Q1. This Q1 turn on when B1 is high that will cause V_{GS} is pulled to ground and turn off when B1 is low that will cause V_{GS} is pulled to V_{GG}. If V_{GG} is set to +15V, the MOSFET will turns on. However, this circuit cannot control the current flow. (Dr Zainal Salam, 2003) [2]

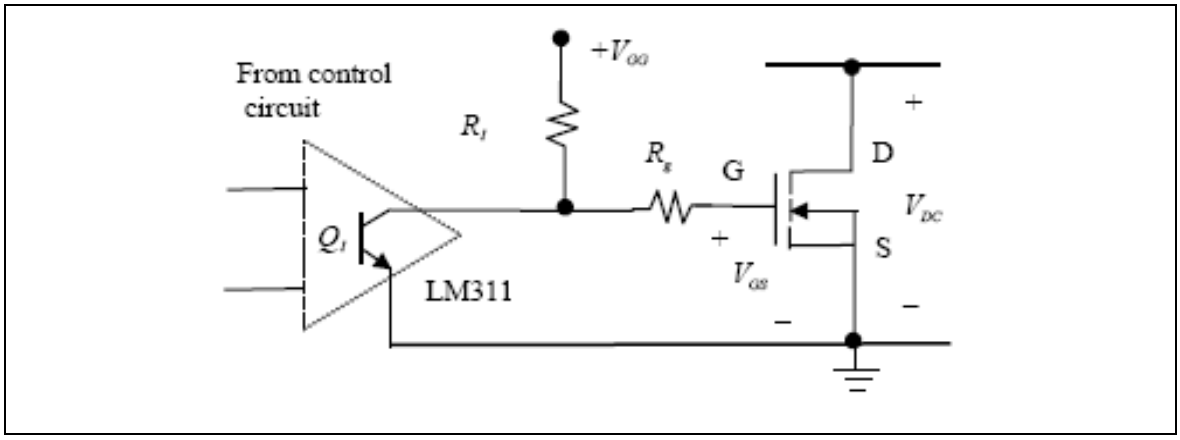


Figure 2.1: MOSFET gate driver

Another design of driver circuit is as Figure 2.2 below. It shows an optically isolated drive circuit using N-channel MOSFET on side of load. It supplied from drain of MOSFET. This circuit used 4N25 opto-coupler as isolation for driver. An opto-isolator is used to provide significant protection from serious overvoltage conditions in one circuit affecting the other for safety reason. It is a device that uses a short optical transmission path to transfer a signal between elements of the circuit. Zener diode 15V is used as voltage regulator to stable the output voltage. So, this circuit also cannot control current because when using zener diode, the voltage output is constant 15V. So, the current is remaining with the voltage. (Jamie Catt, 1993) [3]

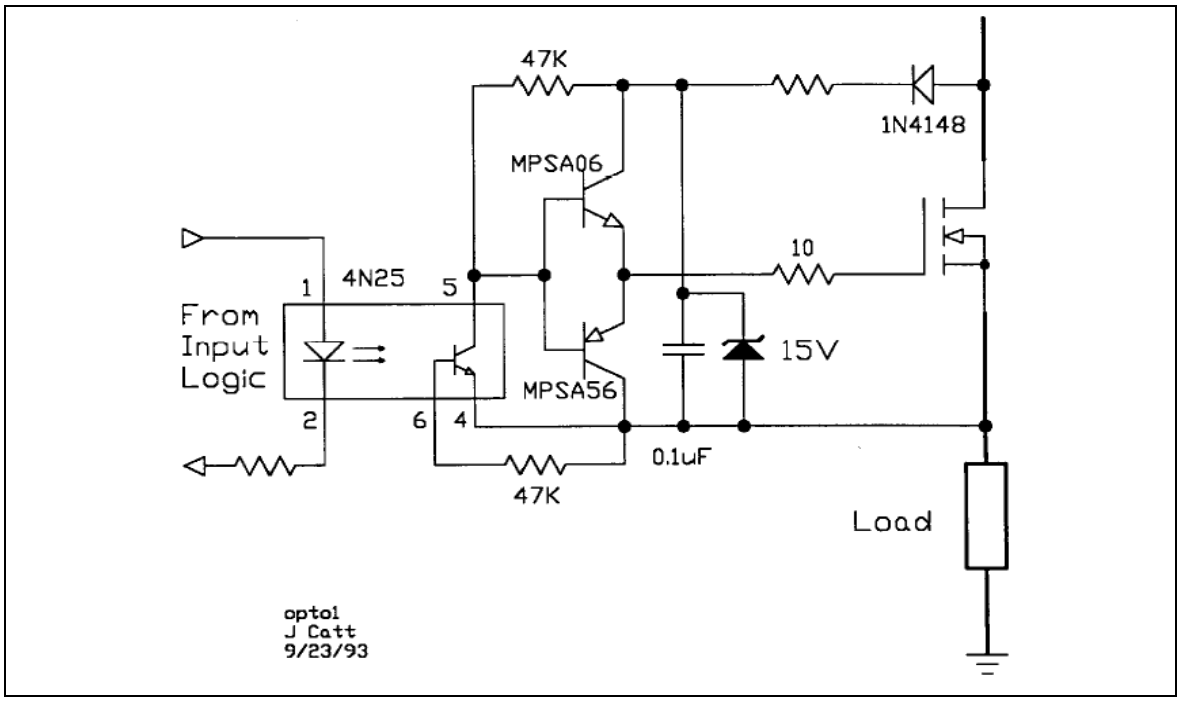


Figure 2.2: Optically isolated gate drive circuit.

Besides that, another way to limit current is using the inductor with protection choke technique design to limit the rate of rise of fault current with a secondary winding to trigger the thyristor crowbar circuit to divert the current from the power transistor to the thyristor. The protection choke allows transformer coupling into the power transistor circuit. So, when fault occur, the current will be diverted from the power transistors to the thyristor which has large current load capacity. The disadvantages of this method are expensive thyristor device the design of the protection choke with secondary windings leads to the bulkiness of the equipment. (P.D. Evans and B.M. Saied, 1982) [4]

The another literature presents a technique where in the slope or rate of rise of the fault current is sensed and protective action is initiated well before the fault current reaches the set value. This method also needs to be added extra sensor, cost and complex circuit as Figure 2.3 below. (Sujit Biswaruk, and Joseph, 1988) [5]

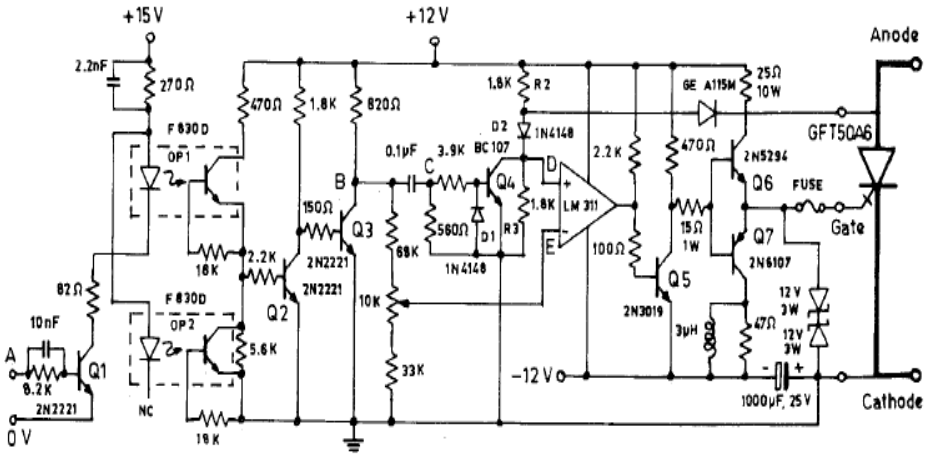


Figure 2.3: Complete auto-protecting gate drive circuit for GTO thyristors.

Besides that, circuit in Figure 2.4 below is a high voltage MOSFET driver. The weakness of this circuit is the resistors still have current flowing through them although the circuit is not being driven with pulses. (Engineering services, 2004) [6]

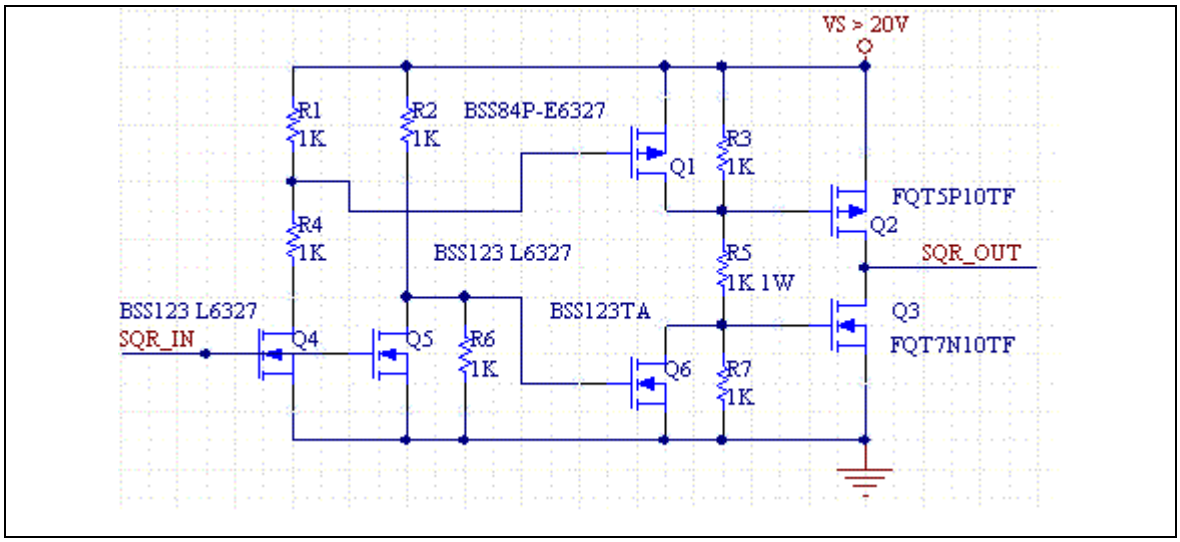


Figure 2.4: High voltage MOSFET driver with minimized cross-over current.

Figure 2.5 shows drive circuit current limitation using multiple drive voltages. In normal operation, 15V is applied to drive the gate fully on which also causes the diode D to be forward biased through resistor R1. In normal operation the VDS voltage drop will typically be around 2 - 3V, but this increases with increasing drain current. The voltage at point P is thus equal to the VDS voltage drop across the MOSFET, plus the voltage drop across D. However, if an over current is detected by monitoring the drain source voltage of the MOSFET, causes the VDS of the MOSFET to increase. When the voltage at point Preaches the rating of the Zener Z1, Z1 begins to conduct, turning on T2, and clamping the voltage at point P, causing D to become reverse biased. Turning on T2 causes Zener Z2 to clamp the MOSFET gate voltage at 6V, limiting the collector current to a lower level. (B.Maurice and L. Wuidart, 1999) [7]

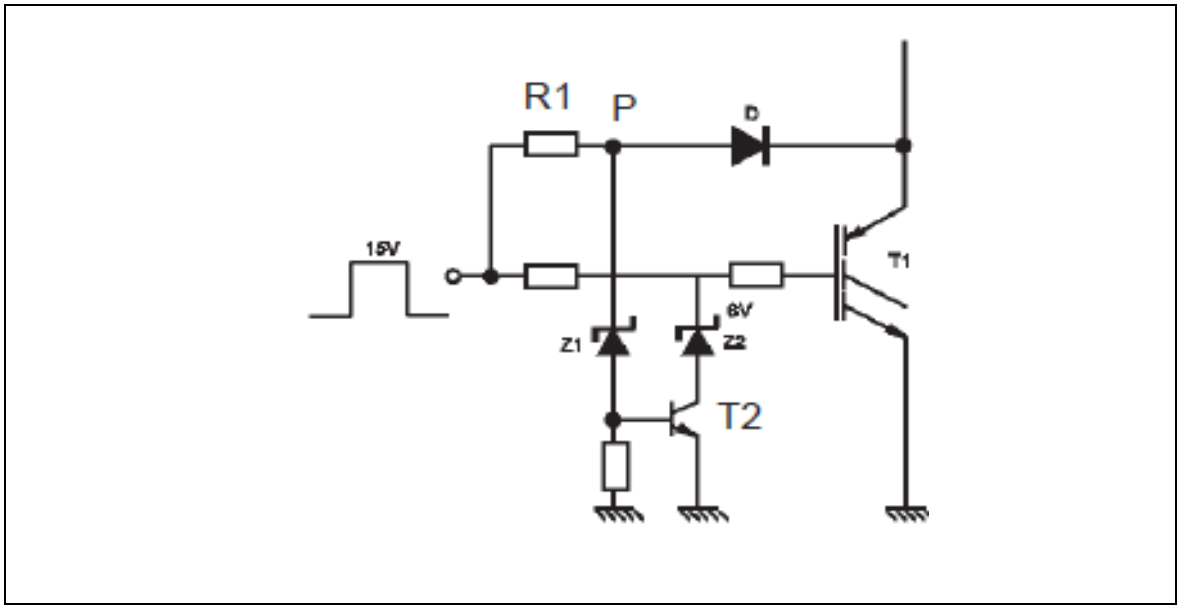


Figure 2.5: Current limitation using multiple drive voltages.

Besides than that, the gate drive circuit is used to amplify the low signal input from control circuit to a higher voltage signal. The higher gate signal voltage is needed for the functioning of the inverter circuit. Left side of the driver circuit is part where to control switching output. Gate Drive Circuit in Figure 2.6 below used 555 timer IC in a variety of timer, pulse generation, and oscillator applications. The 555 can be used to provide time delays, as an oscillator, and as a flip-flop element. Each component has its own function. Resistor 1 and capacitor 1 is function as control on time, resistor 3 to control off-time, resistor 5 to control pulse length (switching frequency), diode 1 is to make sure ON/OFF independently, while potentiometer is used in this circuit to change the width of PWM. [2]

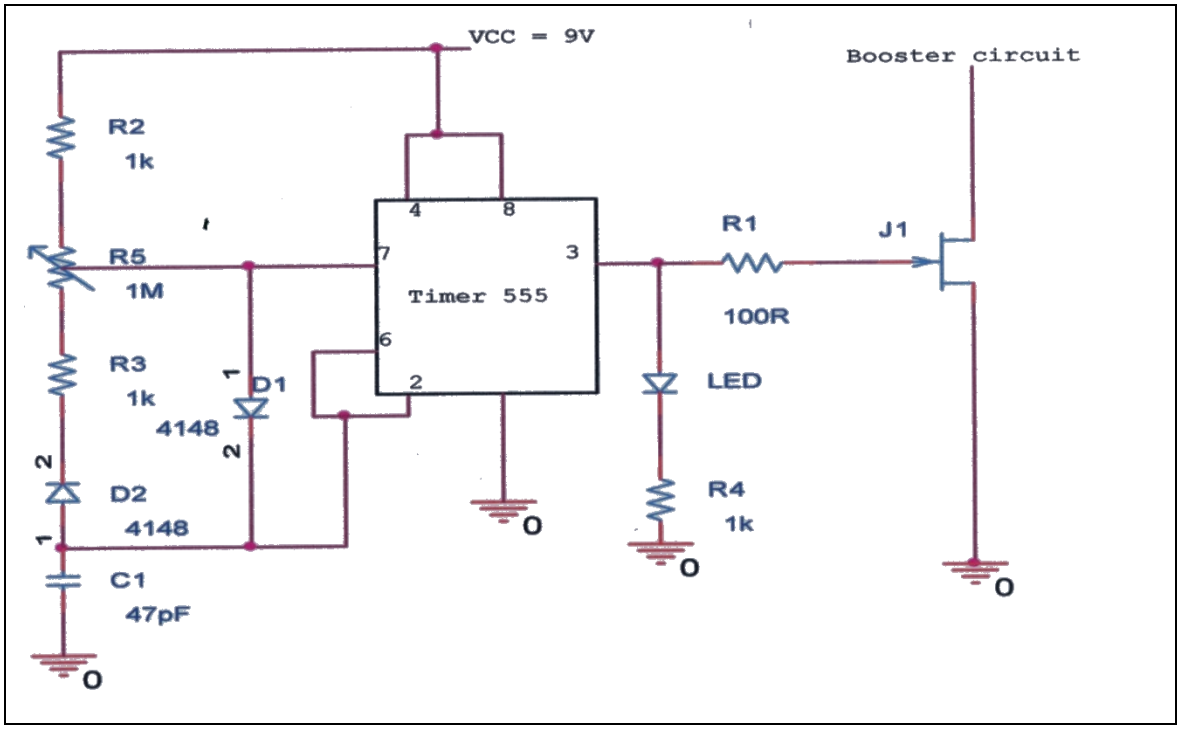


Figure 2.6: Gate drive circuit

Another design for current limiting circuit is as in Figure 2.7 below. With a resistor, the voltage drop is varied depending on the consumed current by the load. The higher current is drawn by the load, the higher voltage drop on that resistor. In this active circuit, the current limiting circuit tries not to drop the voltage if the current drawn by the load is below the allowable range. In normal condition, the limiter circuit tries not to dissipate the power, so almost all power is delivered to the load. If the load tries to draw more than allowed, the current limiting circuit will now act as resistor, controlling it is resistant value to limit the current to a predetermined level. This circuit works with output voltage at Q1 emitter act as a voltage follower, means that the voltage will follow its base voltage. Because the R sense value is chosen to be a low resistance, the voltage will be appearing at load as a full voltage delivered from voltage source. If the load now draws more current, at some level, the voltage drop across R sense will reach the level at a point where the transistor Q2 begin to conduct and the current will flow from its collector to its emitter, decreasing the base voltage of Q2. Because now the

Q1 base voltage decrease, the voltage output of the Q2 emitter will also decrease as it works as a voltage follower circuit. When this output voltage decrease, the current to the load will also decrease. After this point of allowed maximum current, the more the load try to draw more current (by lowering its internal resistance equivalence), the lower the output will be delivered to maintain a constant current. (Vidisonic)[8]

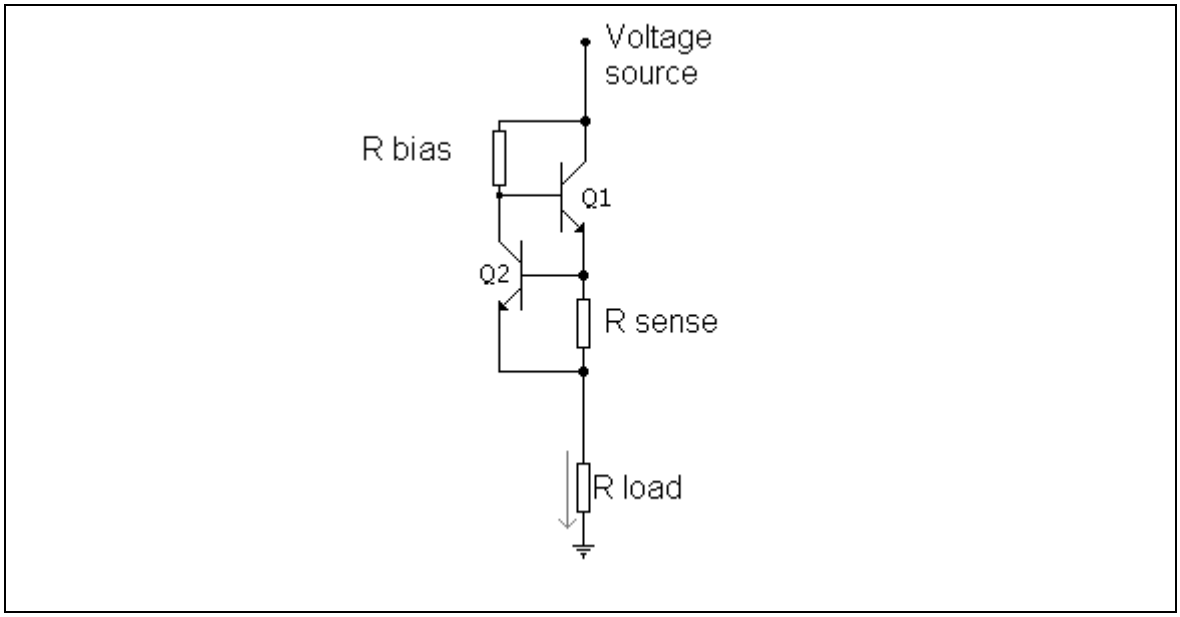


Figure 2.7: Current Limiting Circuits

The MOSFET is a voltage-controlled device and is relatively simple to turn on and off and therefore required an appropriate gate voltage or base current signal to drive the MOSFET into saturation mode for low on-state voltage in order to switch it on. It has a positive temperature coefficient, stopping thermal runaway. Besides that, MOSFET has good performance in high frequency (>100 kHz) and has simpler gate drive circuit. The MOSFET also has a body-drain diode, which is particularly useful in dealing with limited freewheeling currents. MOSFET also has cheaper price and compatible with the highest frequency application in PWM inverter circuit. P-channel of MOSFET required a complex driver circuit and the drain-source on resistor, RDS (on)

for the p-channel is higher than N-channel which will lead to an increase in switching power losses. Using the Enhancement-mode MOSFET as a Switch as these transistors require a positive gate voltage to turn "ON" and a zero voltage to turn "OFF" making them easily understood as switches and also easy to interface with logic gates. (Dr. Zainal Salam, 2003)[2]

2.3 Conclusion

As a conclusion, to protect the power switch, the design outlines from literature reviews should be followed. To protect the power switch, the current flow to the transistor is limited according to the load demand by controlling the gate voltage signal. To design the driver circuit of MOSFET, the circuit must able to limit the current flow to the power switch. MOSFET offers cheaper price and compatible with the highest frequency application in PWM inverter circuit. Therefore in this project, the n-channel enhancement MOSFET is chosen in this project because the Enhancement-mode MOSFET usually used as a switch as these transistors require a positive gate voltage to turn "ON" and a zero voltage to turn "OFF" making them easily understood as switches and also easy to interface with logic gates. Besides that, MOSFET also is used to avoid the losses and to get the simpler gate drive circuit.

For the next chapter is methodology which is discuss about the project work flow diagram, the design of gate drive circuit and current limiter, the simulation and experimental process.

CHAPTER 3

METHODOLOGY

3.1 Introduction

It has been mentioned in previous chapter that in this project n-channel MOSFET is used. The developing process of gate drive circuit involves in designing of control signal and the driver includes hardware and simulation. This chapter describes the methods in design and implementation further step by step about how to conduct this project. This project is divided into two parts which are simulation and experimental implementation of the project part.

3.2 Project Work Flow Diagram.

To simply understand the related works of this project, the work flow chart is presents in Figure 3.1.

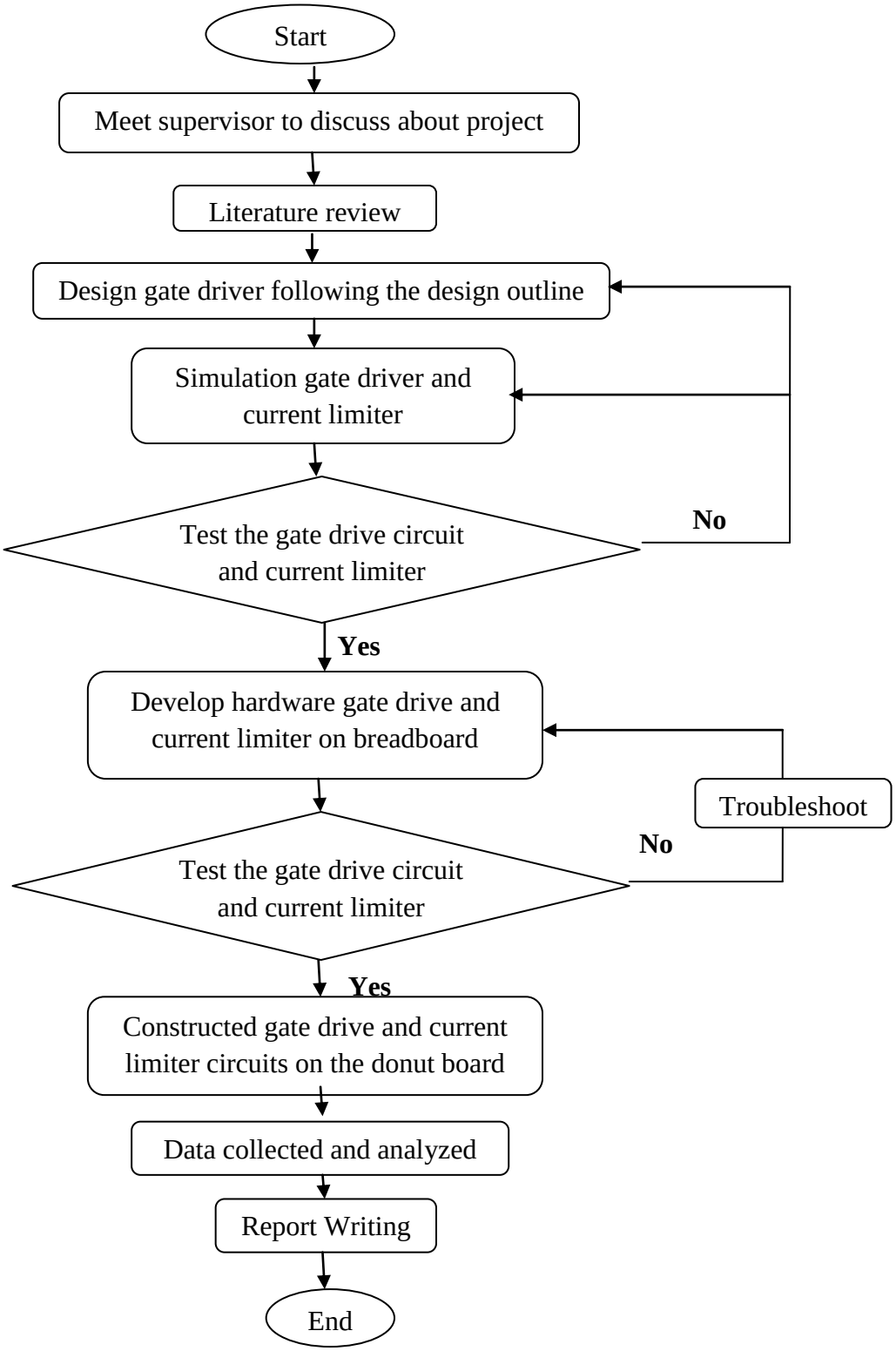


Figure 3.1: Project Work Flow.

3.3 The Design of Gate Drive Circuit with Current Limiter.

From literature review, gate drive circuit's concept in Figure 2.6 is used. The gate drive circuit is used to control switching output to power switch. Left side of the driver circuit is part where to control switching output. Gate Drive Circuit in Figure 3.2 below used 555 timer IC in a variety of timer, pulse generation, and oscillator applications. The 555 can be used to provide time delays, as an oscillator, and as a flip-flop element. This gate driver is an astable multivibrator.

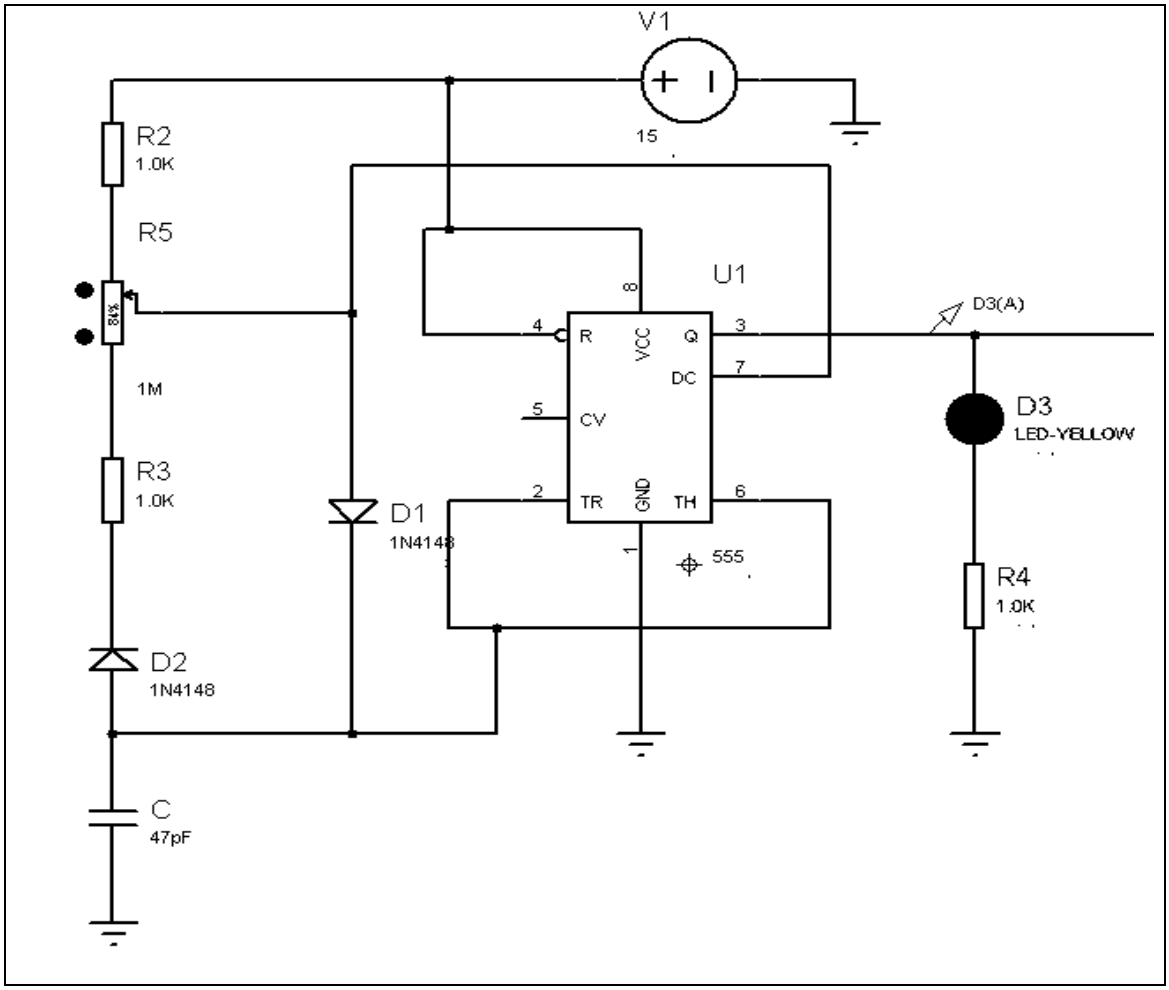


Figure 3.2: Gate drive circuit

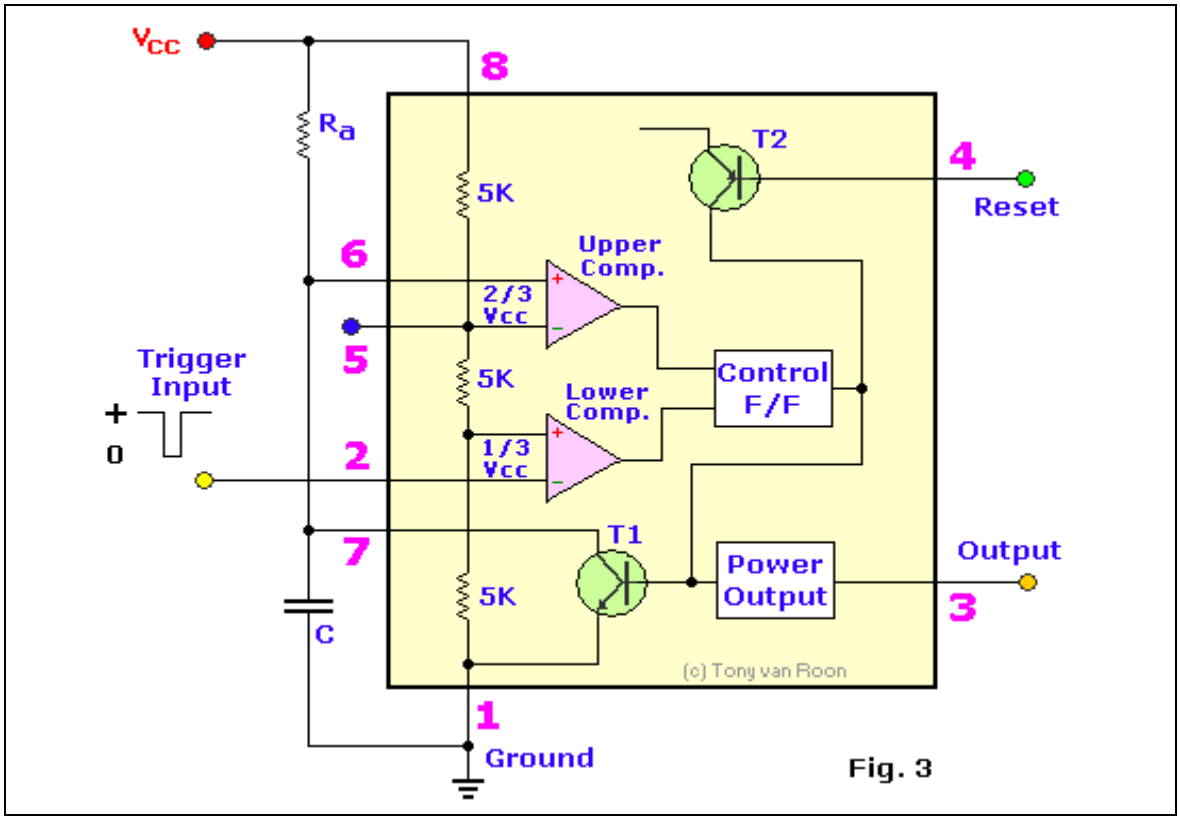


Figure 3.3: Inside the 555 Timer.

Inside the 555 timer as in Figure 3.3 above are the equivalent of over 20 transistors, 15 resistors, and 2 diodes, depending of the manufacturer. The equivalent circuit providing the functions of control, triggering, level sensing or comparison, discharge and power output. The 555 timer can supply voltage between 4.5 and 18 volt, supply current 3 to 6 mA, and a Rise/Fall time of 100 nSec. It can also withstand quite a bit of abuse.

An astable multivibrator is simply and oscillator. The astable multivibrator generates a continuous stream of rectangular off on pulses that switch between two voltage levels. The frequency of the pulses and their duty cycle are dependent upon the RC network values. Both the trigger and threshold bin puts (pins 2 and 6) to the two comparators are connected together and to the external capacitor. The capacitor charges

toward the supply voltage through the two resistors, R1 and R2. The discharge pin (7) connected to the internal transistor is connected to the junction of those two resistors. When power is first applied to the circuit, the capacitor will be uncharged; therefore, both the trigger and threshold inputs will be near zero volts. The lower comparator sets the control flip-flop causing the output to switch high. That also turns off transistor T1. That allows the capacitor to begin charging through R1 and R2. As soon as the charge on the capacitor reaches 2/3 of the supply voltage, the upper comparator will trigger causing the flip-flop to reset. That causes the output to switch low. Transistor T1 also conducts. The effect of T1 conducting causes resistor R2 to be connected across the external capacitor. Resistor R2 is effectively connected to ground through internal transistor T1. The result of that is that the capacitor now begins to discharge through R2. The only difference between the single 555, dual 556, and quad 558 (both 14-pin types), is the common power rail. For the rest everything remains the same as the single version, 8-pin 555. As soon as the voltage across the capacitor reaches 1/3 of the supply voltage, the lower comparator is triggered. That again causes the control flip-flop to set and the output to go high. Transistor T1 cuts off and again the capacitor begins to charge. That cycle continues to repeat with the capacitor alternately charging and discharging, as the comparators cause the flip-flop to be repeatedly set and reset. The resulting output is a continuous stream of rectangular pulses. (Tony van Roon, 2003) [9].

From literature review, current limiter's concept in Figure 2.5 is used. Figure 2.5 is drive circuit current limitation using multiple drive voltages. This concept is used and some improvement is done to make sure my project's objectives are success.

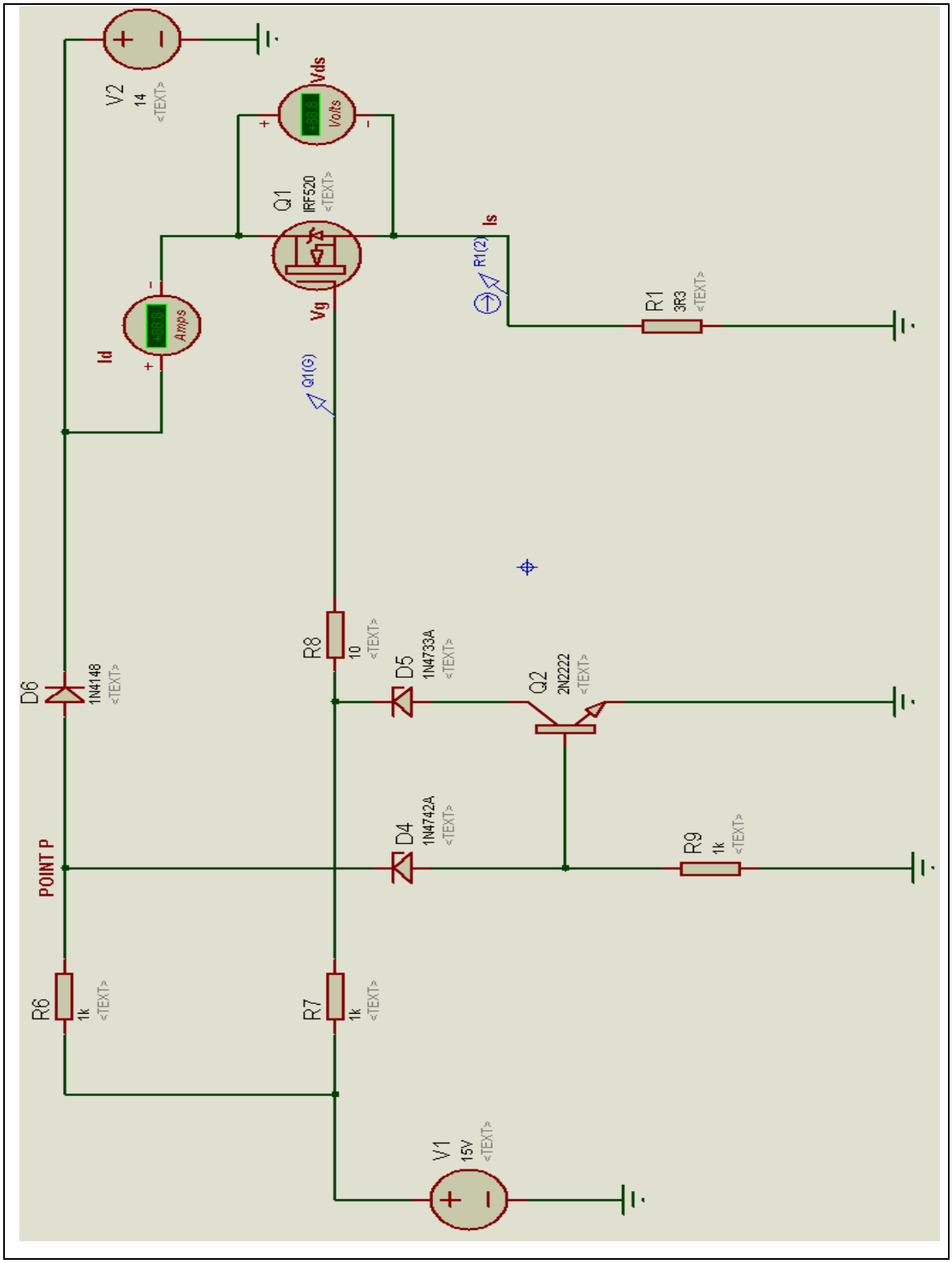


Figure 3.4: Current Limiter circuit.

Figure 3.4 shows current limiter circuit. In normal operation, 15V is applied to drive the gate fully on which also causes the D6 to be forward biased through resistor R6. In normal operation the VDS of MOSFET voltage drop will typically be around 2 - 3V, but this increases with increasing drain current. The voltage at point P is thus equal to the VDS voltage drop across the MOSFET, plus the voltage drop across D6. However, if an overvoltage is detected by monitoring the drain source voltage of the MOSFET, causes the VDS of the MOSFET to increase. When the voltage at point Preaches the rating of the Zener D4, D4 begins to conduct, turning on Q2, and clamping the voltage at point P, causing D6 to become reverse biased. Turning on Q2 causes Zener D5 to clamp the MOSFET gate voltage at 5.40V, limiting the collector current to a lower level.

VP=VD+VDS

Normal operation: VP<VZ1

Overvoltage : VP>VZ1

One of the main limitations of a MOSFET is the maximum current it can handle. So the $R_{DS(on)}$ parameter is an important guide to the switching efficiency of the MOSFET and is simply the ratio of V_{DS} / I_D when the transistor is turned ON. When using a MOSFET or any type of field effect transistor for that matter as a solid-state switching device it is need to select ones that have a very low $R_{DS(on)}$ value or at least mount them onto a suitable heat sink to help reduce any thermal runaway and damage. Power MOSFETs used as a switch generally have surge-current protection built into design as in this project.

From literature review, a design outline should be follow to design the driver circuit. It seems that IRF520 n-channel enhancement MOSFET is chosen as power switch. The ratings of this device as in Table 3.1 below:

Table 3.1 IRF520 Characteristics.

Parameter	Value
Continuous drain rating (Id)	9.2A
Drain source voltage (Vds)	100V
On resistance Rds(on)	0. 3Ω
Voltage Vgs maximum	20V

In this circuit, 1N4148 diode for D1 which is made from silicon is used. It allows electricity to flow in one direction only. Electricity uses up a little energy pushing its way through the diode. There is a small voltage across a conducting diode called the forward voltage drop and this diode has 0.7V forward voltage drop. The forward voltage drop of a diode is almost constant whatever the current passing through the diode so they have a very steep characteristic. When a reverse voltage is applied a perfect diode does not conduct, but all real diodes leak a very tiny current of a few μA or less. This can be ignored in most circuits because it will be very much smaller than the current flowing in the forward direction. However, this diode has a 75V maximum reverse voltage and if this is exceeded the diode will fail and pass a large current in the reverse direction, this is called breakdown. Signal diodes are used to process information (electrical signals) in circuits, so they are only required to pass small currents of up to 100mA. For general use, silicon diodes are better because they are less easily damaged by heat when soldering, they have a lower resistance when conducting, and they have very low leakage currents when a reverse voltage is applied. (Wikipedia, Diode) [10].

Zener diodes D2 and D3 in circuit are used to maintain a fixed voltage. They are designed to 'breakdown' in a reliable and non-destructive way so that they can be used in reverse to maintain a fixed voltage across their terminals. Zener diodes are rated by their breakdown voltage and maximum power.

The 2N2222 is a common NPN bipolar junction transistor used for general purpose low-power amplifying or switching applications. It is designed for low to medium current, low power, medium voltage, and can operate at moderately high speeds. It is frequently used as a small-signal transistor; it is a small general purpose transistor of enduring popularity. It is used for both analog signal amplification and switching applications. When an electronic signal is present at the transistor's collector, applying a signal to the transistor's base will cause a signal to emit from the device's emitter. In this way, the 2N2222 is often used to switch signals on and off. The switching abilities of the 2N2222 transistor also make it useful as a simple "and" gate. When used in this capacity, the transistor will only send a signal when two separate signals are present: one at its collector *and* one at its base. This allows the 2N2222 to be used to automatically control signal flow in a circuit depending on what signals are, or are not, present. In amplification applications, the 2N2222 receives an analog signal, such as an audio signal, through its collector and a separate signal is applied to its base. The output at the transistor's emitter will then be identical to the collector signal with the exception that it increases in power by an amount proportional to the signal applied to its base. (Wikipedia, 2N2222) [11].

3.4 The Simulation.

In this part, gate drive circuit and current limiter are developed using Proteus. The simulation is simulated until get the expected result of gate drive circuit that can control current flow to the inverter. If the expected waveform is not generated, the simulation circuit is modified and simulated again until the wanted output waveform is produced. The simulation is to compare the experimental result with simulation result and to design the gate drive with current limiter circuit.

The design of gate drive circuit is done as Figure 3.5 below. 15V supply voltage is supplied to gate drive circuit.

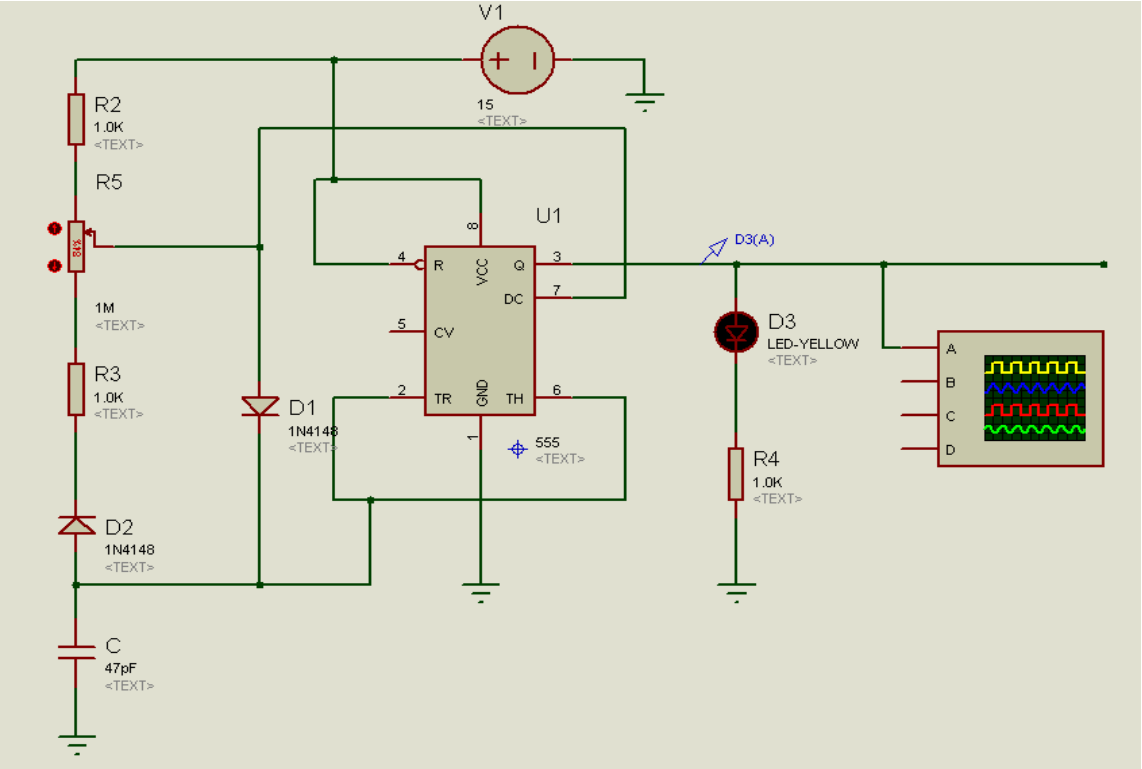


Figure 3.5: Simulation of Gate Drive Circuit

Current limiter circuit is success, the simulation as Figure 3.6 is done. To simulate current limiter circuit in overvoltage operation, 14V drain voltage is given while for normal operation is11Vdc. Firstly, 11Vdc of V2 is supplied to circuit to put the circuit in normal condition. Then, 11Vdc is up to 14Vdc to see the circuit works in overvoltage operation. In this simulation, zener diode D4 is set to 12V. For D5, 5.1V zener diode is used. The results obtained are shown in result part.

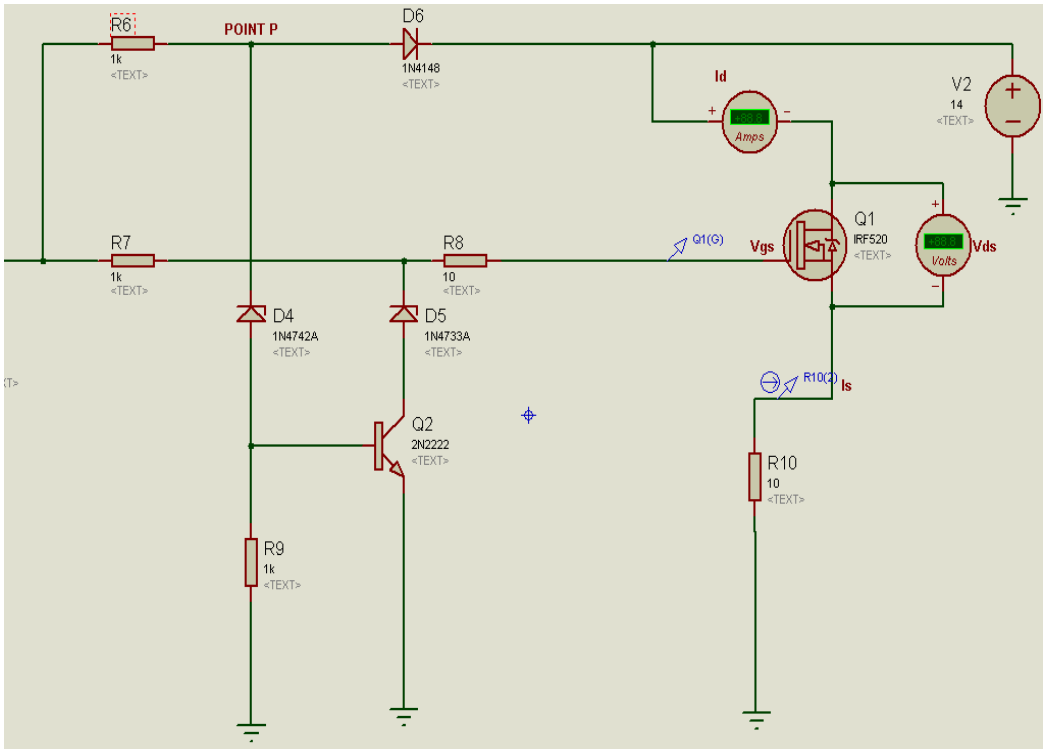


Figure 3.6: Simulation of Current Limiter Circuit.

3.5 Hardware implementation part

Firstly, a gate driver and current limiter circuits are build temporarily on the breadboard after successful in simulation. The results of square wave waveform are shown in the oscilloscope and measured the value of voltage and current using multimeter. After that, the circuit is tested to make sure it operates well. If the testing fails, the circuit is troubleshoot to repair the error. The gate driver with current limiter circuit is built on breadboard as Figure 3.7 and Figure 3.8.

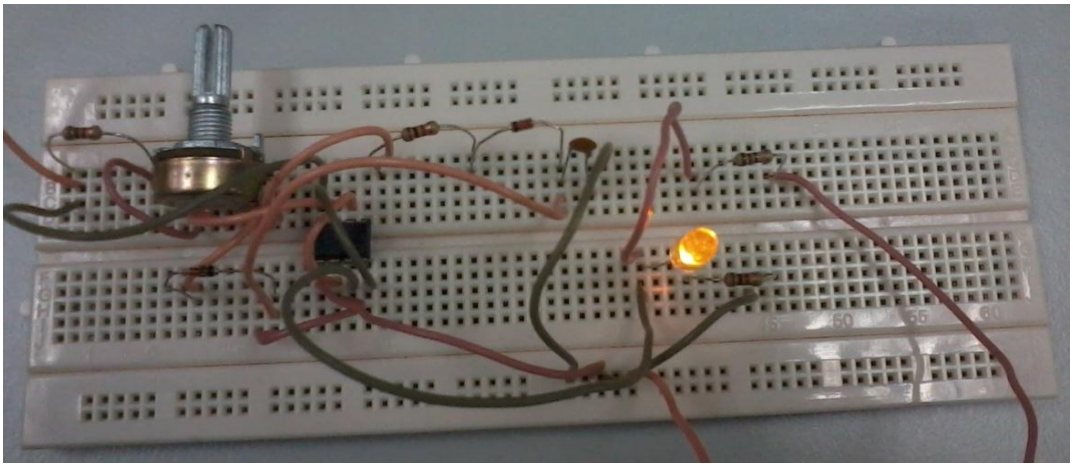


Figure 3.7: Gate Drive Circuit Testing on Breadboard

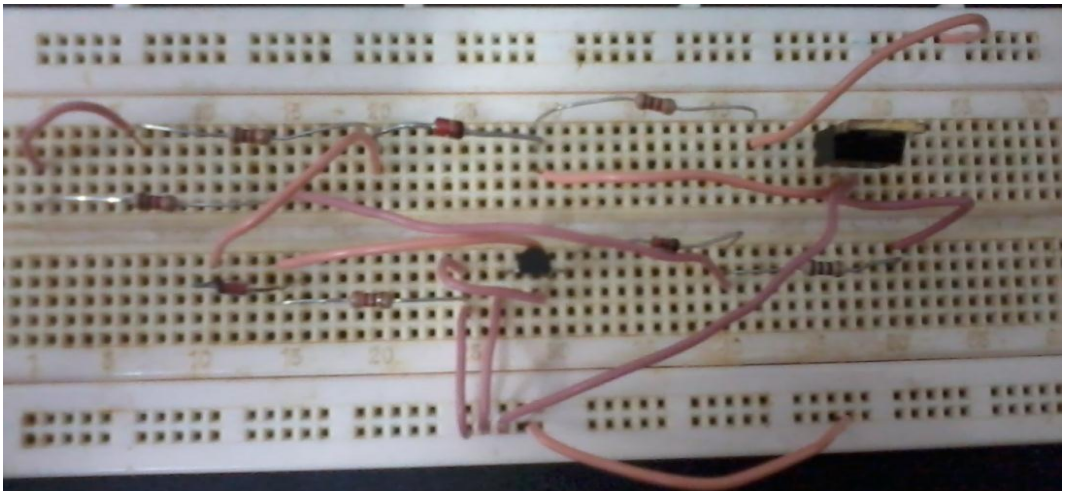


Figure 3.8: Current Limiter Testing Circuit on Breadboard.

After the expected results is got and achieve the objective, the gate drive circuit is constructed on a donut board. Wrapping process is done using wrapping tool to connect the circuit as circuit design before this in Figure 3.2. Figure 3.9 shows the gate drive circuit while Figure 3.10 shows the current limiter circuit. The results obtained are discussed in results and analysis part.

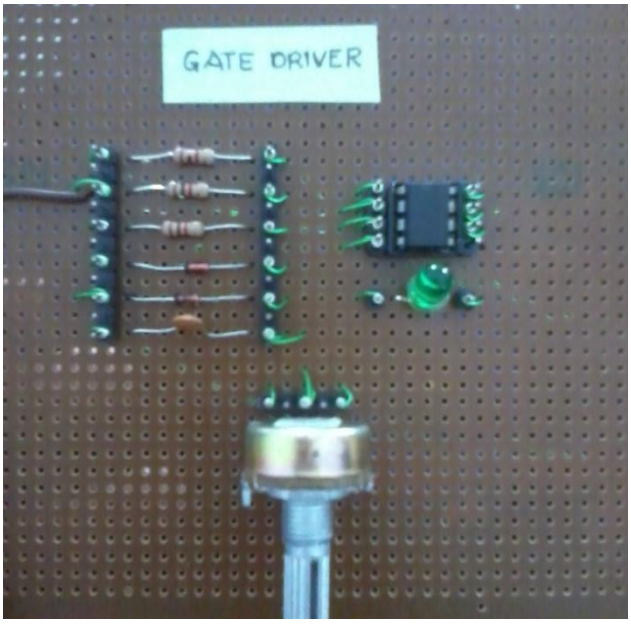


Figure 3.9: Gate driver circuit.

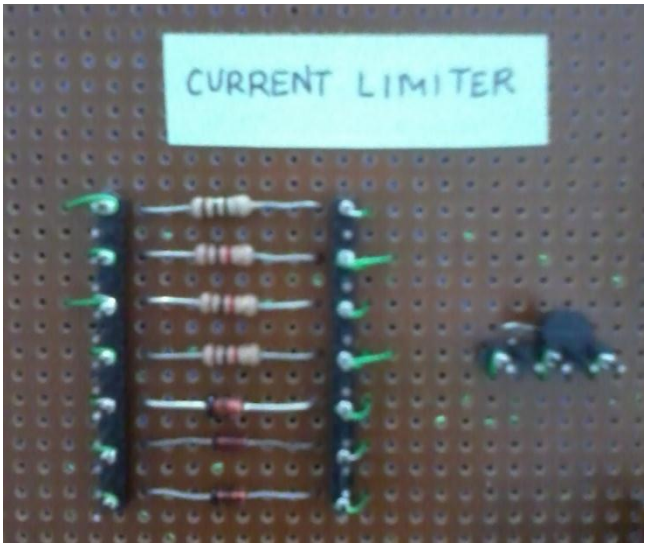


Figure 3.10: Current limiter circuit.

For MOSFET, a heat sink is used to cool MOSFET. Heat sink is a passive component that cools a device by dissipating heat into the surrounding air. Heat sinks are used to cool electronic components such as high-power semiconductor devices, and optoelectronic devices. Waste heat is produced in transistors due to the current flowing through them. The heat sink helps to dissipate the heat by transferring it to the surrounding air. Besides that, the heat silicon also is used between MOSFET and heat sink. It is used for better heat transfer.

Figure 3.11 below shows the complete circuit of gate driver and current limiter after constructed on donut board. Then, the circuit is tested as overall experimental setup of Figure 3.12 to ensure it is works and the connection is right.

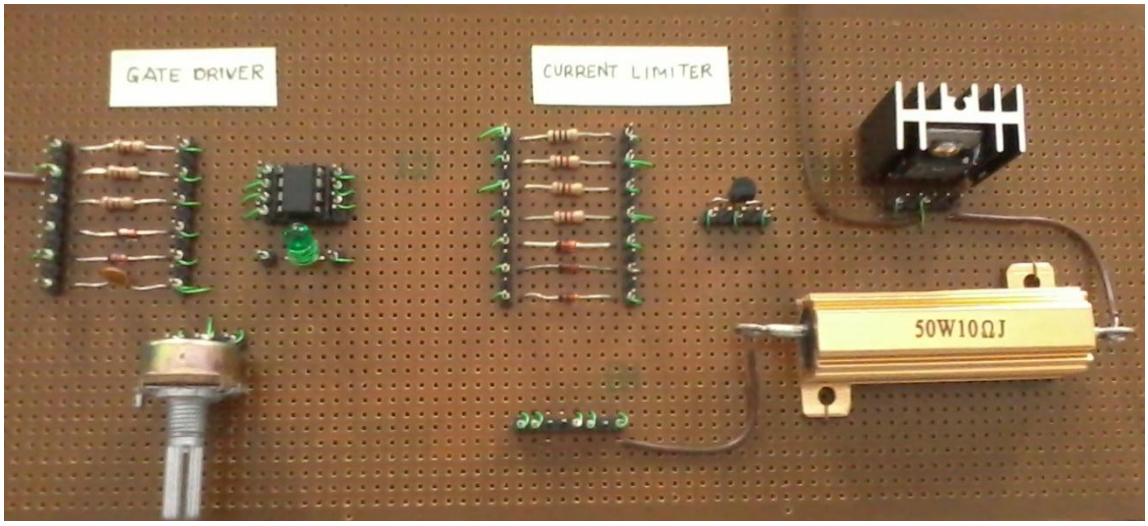


Figure 3.11: Complete circuit

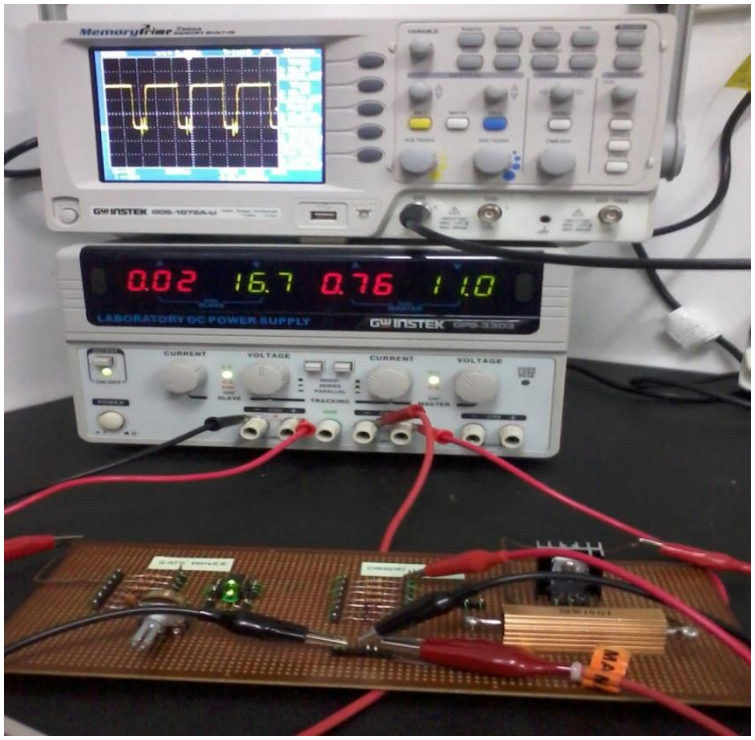


Figure 3.11: Overall experimental setup

3.6 Conclusion

As a conclusion, this chapter is discussed about the project work flow diagram, the design of gate drive circuit and current limiter, the simulation and experimental process. Next chapter is results which is the show the result obtained in simulation and experimental part and the results are discussed and analyzed.

CHAPTER 4

RESULTS AND ANALYSIS

4.1 Introduction

In results and analysis part, it is consists of two results. There are simulation results and the experimental results. All the results are discussed and analyzed. The experimental result is compare with the simulation result to ensure the experimental result is correct.

4.2 Simulation result

After simulate the gate drive circuit, 15V signal is produce as in Figure 4.1. The gate driver signal above is obtained with different pulse length when adjusted R5 to

control the pulse length as Figure 4.2. So, for the first objective which is to control the gate voltage signal to the MOSFET is achieved.

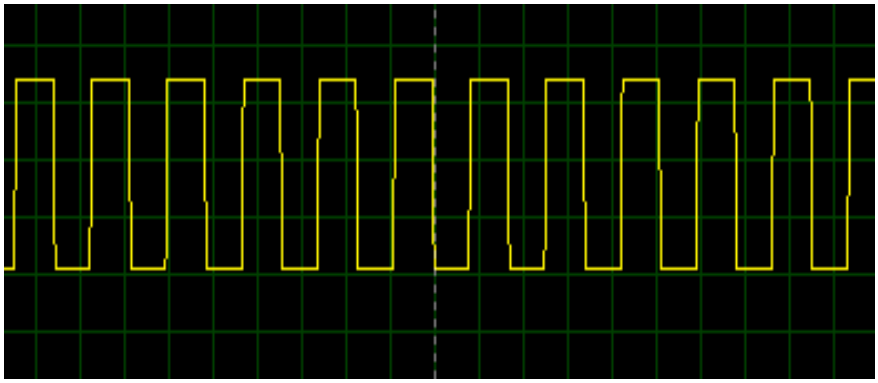


Figure 4.1: Gate Driver Signal

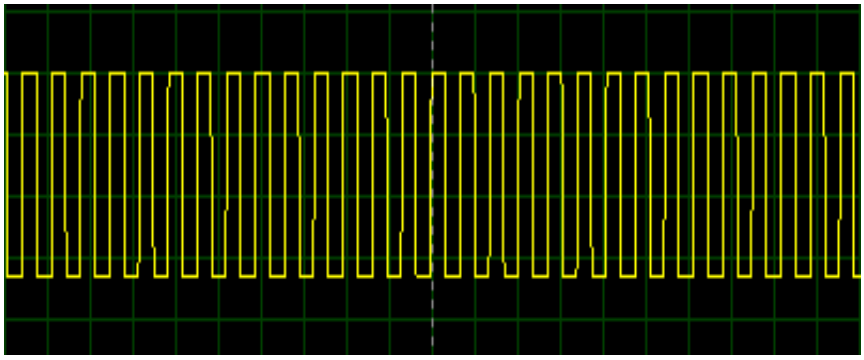


Figure 4.2: Gate driver signal when controlling the potentiometer

The simulation result of current limiter circuit is done. In normal operation (11Vds) is supplied while 14V for overvoltage operation. Table 4.1 below shows the simulation values of gate to source voltage (Vgs), drain to source voltage (Vds) and drain current (Id) in normal and overvoltage operation after simulating the circuit as in Figure 4.3 and 4.4.

Table 4.1 Simulation Results

CONDITION	PARAMETER	VALUE
Normal operation (11V)	Gate to source voltage(Vgs)	15V
	Drain Current(Id)	1.04A
	Drain to source voltage (Vds)	0.62V
Overvoltage operation (14V)	Gate to source voltage(Vgs)	5.43V
	Drain Current(Id)	0.15A
	Drain to source voltage (Vds)	12.5V

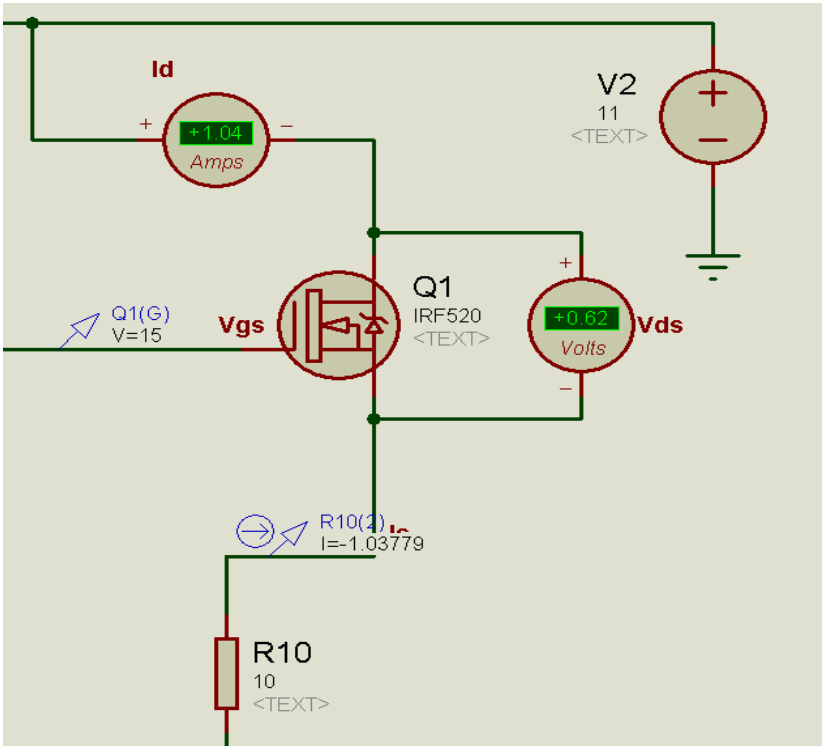


Figure 4.3: The simulation in normal condition.

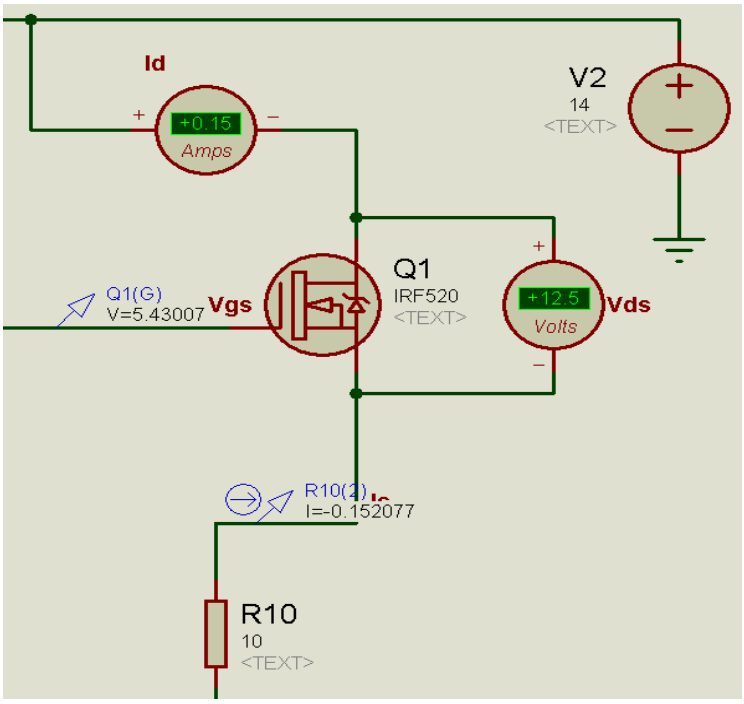


Figure 4.4: The simulation in overvoltage condition.

Below is the calculation based on result of simulation for both conditions to ensure the results obtained are correct.

Normal operation: VP<VD4

VP=VD+VDS

=0.7+0.62V

=2.18V

VP<VD4

2.18V<15V

So, the result of simulation is successful because as theory, when VP<VD4, it is in the normal operation and the result must be obtained is 15V gate voltage because the

voltage at point P is not reached the rating of the Zener D4, so D4 and current limiter circuit will not conduct. So, in normal operation, 15V is applied to drive the gate of MOSFET fully on.

Overvoltage: VP>VD4

VP=VD+VDS

=0.7+18.7V

=19.4V

VP>VD4

19.4V>15V

So, the result of simulation is successful because as theory, when VP>VD4, it is in the overvoltage operation and the result must be obtained is 5.43V PWM signal because the zener diode of Q2 is clamped at 5.43V gate voltage. When the voltage at point Preaches the rating of the Zener D4, D4 begins to conduct, turning on Q2, and clamping the voltage at point P, causing D6 to become reverse biased. Turning on Q2 causes Zener D5 to clamp the MOSFET gate voltage at 5.43V, limiting the collector current to a lower level.

Figure 4.5 and 4.6 shows the signal of the gate driver and Vgs when the circuit in normal and overvoltage operation.

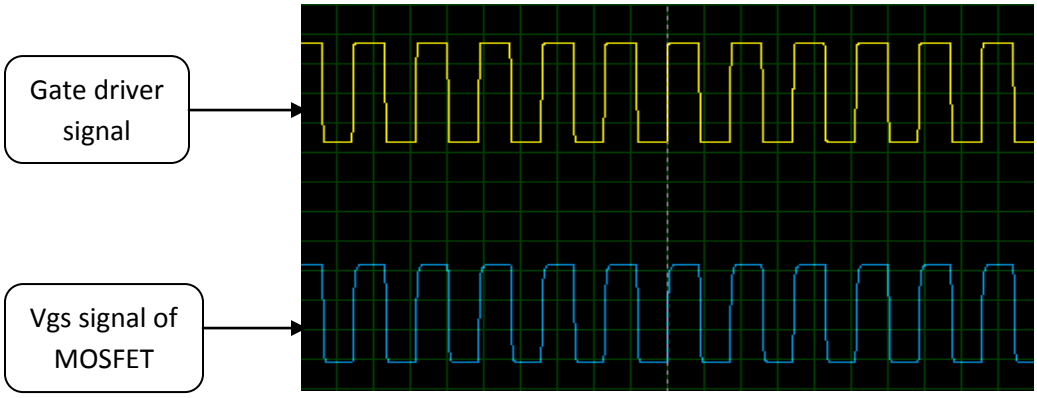


Figure 4.5: Simulation of gate driver and current limiter circuit during normal operation.

When supplied 15V gate driver signal and 11V Vd to the MOSFET, 15V Vgs signal of MOSFET is obtained. For current limiter during normal operation, 15V is applied to drive the gate fully on with 1.04A Id.

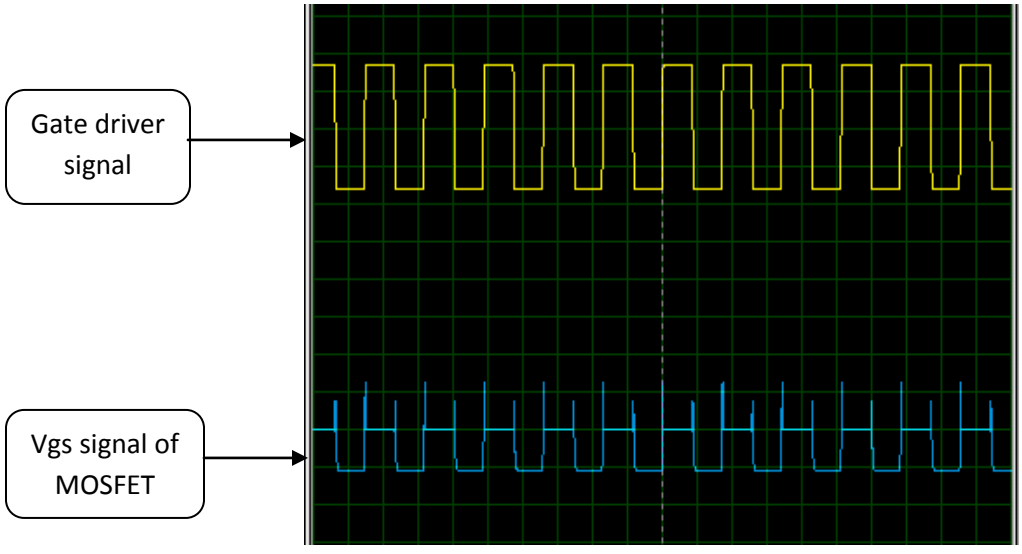


Figure 4.6: Simulation of gate driver and current limiter circuit during overvoltage operation.

When supplied 15V Vgs signal and 14V Vd of MOSFET, 5.43V Vgs signal of MOSFET is obtained because voltage at point P reaches the rating of the 12V D4 cause 5.1V D5 is clamped the MOSFET gate voltage at 5.43V, limiting Id to 0.15A. So, the second objective to limit the current flow through the MOSFET during overvoltage operation is achieved.

4.3 Experimental Results.

After doing hardware implementation of gate drive circuit in Figure 3.10 to produce 15V square wave signal, the square wave waveform result is obtained on oscilloscope was recorded. The input of gate driver is given is16.5V to get 15V signal. The input cannot give 15V because a small voltage will drop in circuit to obtain the output. So, to get 15V output signal, the input voltage is need to give a little high voltage than the wanted output. In this circuit, it seems that this circuit has 1.6V voltage drop. The gate drive signal is shown in Figure 4.3 as below:

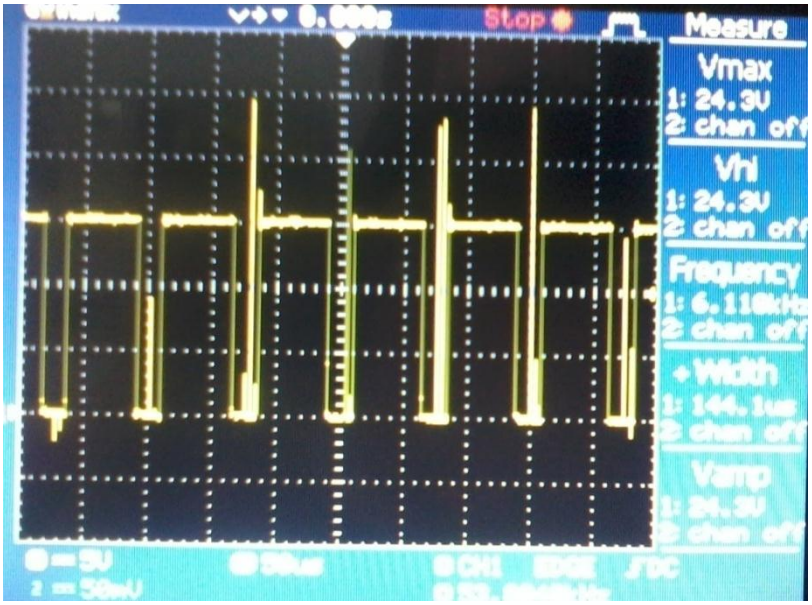


Figure 4.7: Gate Driver Signal.

The gate driver signal in Figure 4.8 is obtained with different pulse length when adjusted R5 to control the pulse length. So, for the first objective which is to control the gate voltage signal to the MOSFET is achieved.

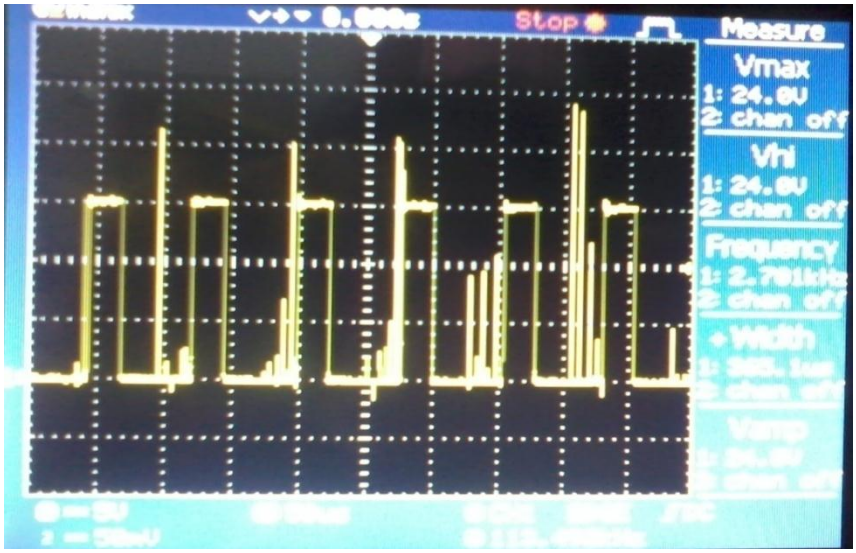


Figure 4.8: Gate driver signal when adjust the potentiometer.

After that, the current limiter circuit is connected to the gate drive circuit. To test the normal condition, 11V drain voltage (Vd) is supplied to the circuit. Then, the gate voltage waveform obtain in oscilloscope is recorded as Figure 4.9. The waveform obtained is 15V square wave signal. For current limiter during normal operation, 15V is applied to drive the gate fully on with 1.04A Id.

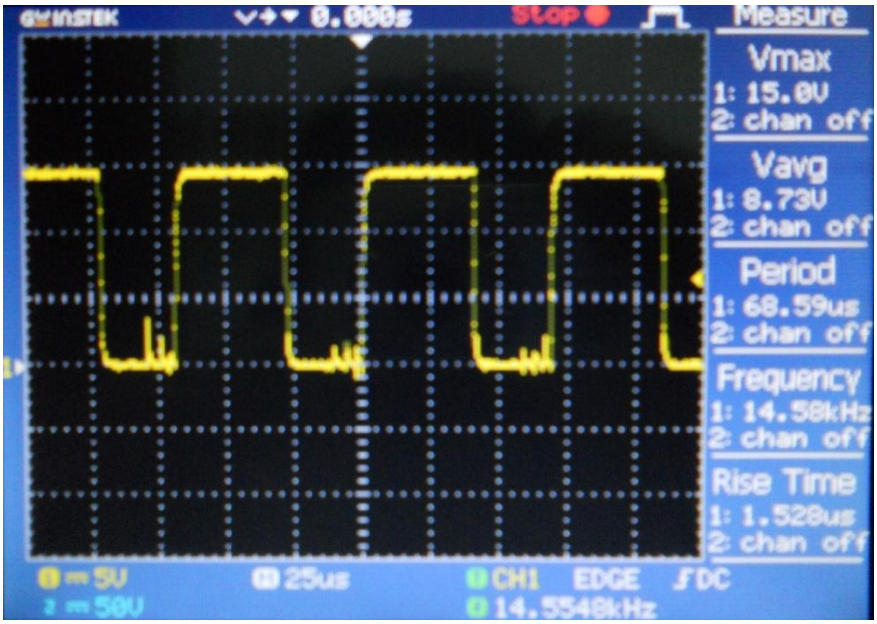


Figure 4.9: Normal Condition Square Wave Signal.

Then, to test the overvoltage condition, 14V drain voltage (Vd) is supplied to the circuit. Then, the gate voltage waveform obtain in oscilloscope is recorded as Figure 4.10. The waveform obtained is 5.40V signal. The signal is clamp to 5.40V because voltage at point P reaches the rating of the 12V D2 cause D1 is clamped the MOSFET Vgs to 5.40V, limiting Id to 0.14A. So, the second objective to limits the current flow through the MOSFET during overvoltage operation is achieved.

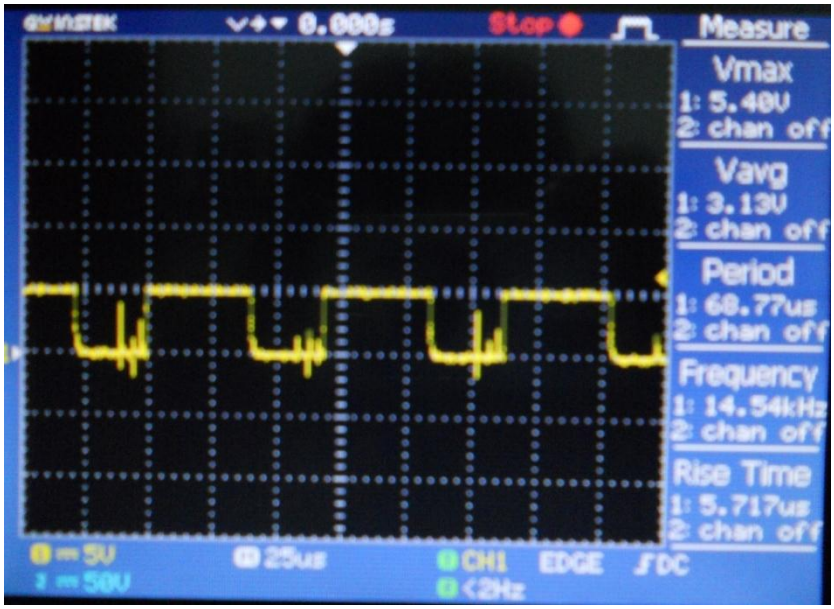


Figure 4.10: Overvoltage Signal

In normal condition, the chosen zener diode is 12V. So, high of 12V is the overvoltage will occur. So, 11V is set as the normal condition while 20V is set as overvoltage condition. The results obtained in experiment are constructed in Table below:

Table 4.3 The experimental values.

Condition	**Parameter**	**Value**
Normal (11V)	Gate to source voltage(Vgs)	15V
	Drain current (Id) for 3W resistor	1.04A
	Drain to source voltage (Vds)	0.60V
Overvoltage (14V)	Gate to source voltage(Vgs)	5.40V
	Drain current (Id) for 3W resistor	0.14A
	Drain to source voltage (Vds)	12.30V

So, from the result obtained in Table 4.3, the calculation is done to ensure the measured value is correct.

For normal operation: VP<VD4

VP=VD+VDS

=0.7+1.30V

=2V

VP<VD4

2V<15V

So, the result of experimental is successful because as theory, when VP<VD4, it is in the normal operation and the result must be obtained is 15V gate voltage because the voltage at point P is not reached the rating of the Zener D4, so D4 and current limiter circuit will not conduct. So, in normal operation, 15V is applied to drive the gate of MOSFET fully on.

For overvoltage: VP>VD4

VP=VD+VDS

=0.7+18.5V

=19.2V

VP>VD4

19.2V>15V

So, the result of simulation is successful because as theory, when VP>VD4, it is in the overvoltage operation and the result must be obtained is 5V PWM signal because the zener diode of Q2 is clamped at 5V gate voltage. When the voltage at point Preaches the rating of the Zener D4, D4 begins to conduct, turning on Q2, and clamping the voltage at point P, causing D6 to become reverse biased. Turning on Q2 causes Zener D5 to clamp the MOSFET gate voltage at 5V, limiting the collector current to a lower level.

It seems that in normal condition, the drain current is 1.55A. When the overvoltage is occurred, the current is decrease to 0.28A because the current is limited. So, the concept of second objective of this project which is to limit current flow through the power MOSFET during overvoltage operation is achieved.

From the results obtained, the experimental results are same with the simulation result after comparing both results. So, this project is successfully done.

For IRF520 MOSFET, the forward biased safe operating area is needed to consider preventing MOSFET from damage. If not consider, the MOSFET will permanently damage. From the Figure 4.11, the peak current limitation is 30A while drain to source voltage is limit to 100V. So, to prevent the MOSFET from damage, the values of peak current and drain to source voltage are need to ensure that not over the limitation values.

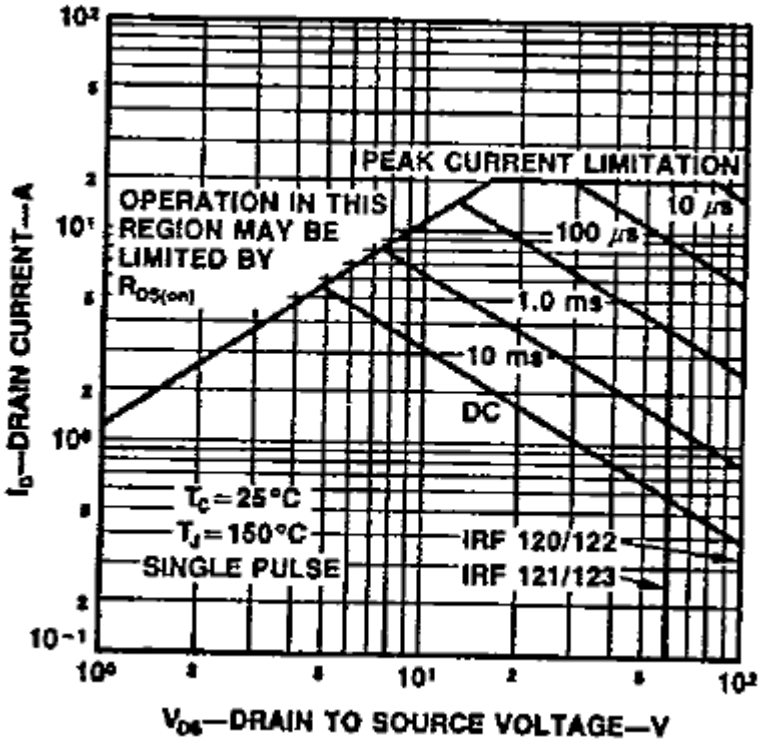


Figure 4.11: The Forward Biased Safe Operating Area.

4.4 Conclusion

As a conclusion, this chapter is discussed about results which is the obtain result in simulation and experimental part and the results are discussed and analyzed. Next chapter is about conclusion of the project. It is consist of summary and recommendation for the future research.

CHAPTER 5

CONCLUSION

5.1 Summary of the Project

As a conclusion, to ensure the objectives of the project is achieve or not, below are the objectives of this project. There are two objectives of this project. The objectives of this project are as below:

1) To design and implement the gate drive circuit those amplify and control the voltage signal to the power MOSFET.
2) To incorporate the current limiter to the gate drive circuit which limits the current flow through the power MOSFET during overvoltage operation.

All the objectives of this project are achieved and successful. The result from both simulation and experiment are achieved the objectives. For the first objective, the design and implement the gate drive circuit in Figure 3.4 is successful to amplify and control the voltage signal to the power MOSFET. This circuit is generated 15V square wave signal. Then, for the second objective, the current limiter circuit is successful to limit the current flow through the power MOSFET during overvoltage operation. When the overvoltage condition occurs, the current is limited to the current set value.

5.2 Recommendation

There are a few recommendations for future researches based on this project are as follows:

1) Design the gate drive circuit that can amplify and control the gate voltage signal to the MOSFET.

2) Design the current limiter to the gate drive circuit which limits the current flow through the MOSFET during overvoltage and over current operation.

REFERENCES

[1] Werner Bosterling,Mario Campello, and Martin Tscharn, "Base drive and protection for bipolar transistor modules," PCIM *Europe,* pp. 27-30, Feb. /Mar. 1989.

[2] Dr. Zainal Salam, ''*Power Electronics and Drives*,'' UTM, Johor, version 3,2003.

[3] Jamie Catt, ''Optically Isolated Gate Drive Circuit;'' international rectifier design tips, Sept 1993.

[4] P. D. Evans and B. M. Saied, "Protection methods for power-transistor circuits," ***IEE*** Proc., Vol. 129, R.B, No. 6, pp. 359-363, Nov. 1982.

[5] Sujit K. Biswas, Biswaruk Basak and Joseph Vithayathil, "An Autoprotecting Gate Drive Circuit for GTO Thyristors,''IEEE Transactions of Industry AApplications, Vol 24, No. 1, January/ February 1988.

[6] Engineering services, "High voltage MOSFET driver,'' Daycounter Inc, [Online]. Available: http://www.daycounter.com/Circuits/HV-MOSFET-Driver/HV-MOSFET-Driver.phtml [Accessed: 2004].

[7] B. Maurice and L. Wuidart, "Drive circuit for power MOSFETs and IGBTs,'' st application note, 1999.

[8] Vidisonic, "Current Limiting Circuit,'' [Online]. http://www.vidisonic.com/2008/07/10/current-limiting-circuit

[9] Tony van Roon, "555 Timer Tutorial,'' 2003.

[10] Wikipedia, "Diode," [Online] http://en.wikipedia.org/wiki/Diode

[11] Wikipedia, "2N2222," [Online] http://en.wikipedia.org/wiki/2N2222

APPENDIX A

FAIRCHILD SEMICONDUCTOR®

IRF520

Data Sheet **January 2002**

9.2A, 100V, 0.270 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA09594.

Ordering Information

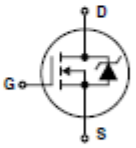
PART NUMBER	PACKAGE	BRAND
IRF520	TO-220AB	IRF520

NOTE: When ordering, use the entire part number.

Features

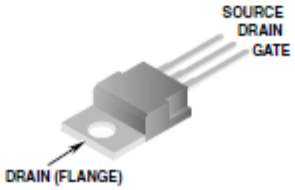
- 9.2A, 100V
- $r_{DS(ON)} = 0.270\Omega$
- SOA is Power Dissipation Limited
- Single Pulse Avalanche Energy Rated
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC TO-220AB



IRF520

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

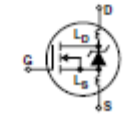
		IRF520	UNITS
Drain to Source Breakdown Voltage (Note 1)	V_{DS}	100	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	100	V
Continuous Drain Current	I_D	9.2	A
$T_C = 100^oC$	I_D	6.5	A
Pulsed Drain Current (Note 3)	I_{DM}	37	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	60	W
Dissipation Derating Factor		0.4	W/^oC
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS}	36	mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

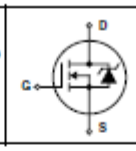
NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V (Figure 10)		100	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250µA		2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 95V, V_{GS} = 0V		-	-	250	µA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_J = 150^oC$		-	-	1000	µA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = 10V (Figure 7)		9.2	-	-	A
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 5.6A, V_{GS} = 10V (Figure 8, 9)		-	0.25	0.27	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 50V$, I_D = 5.6A (Figure 12)		2.7	4.1	-	S
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 50V, I_D = 9.2A, R_G = 18Ω, R_L = 5.5Ω MOSFET Switching Times are Essentially Independent of Operating Temperature		-	9	13	ns
Rise Time	t_r			-	30	63	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	18	70	ns
Fall Time	t_f			-	20	59	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = 10V, I_D = 9.2A, V_{DS} = 0.8 x Rated BV_{DSS}, $I_{g(REF)}$ = 1.5mA (Figure 14) Gate Charge is Essentially Independent of Operating Temperature		-	10	30	nC
Gate to Source Charge	Q_{gs}			-	2.5	-	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	2.5	-	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 11)		-	350	-	pF
Output Capacitance	C_{OSS}			-	130	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	25	-	pF
Internal Drain Inductance	L_D	Measured From the Contact Screw On Tab To Center of Die	Modified MOSFET Symbol Showing the Internal Devices Inductances	-	3.5	-	nH
		Measured From the Drain Lead, 6mm (0.25in) From Package to Center of Die		-	4.5	-	nH
Internal Source Inductance	L_S	Measured From the Source Lead, 6mm (0.25in) From Header to Source Bonding Pad		-	7.5	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	2.5	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	80	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode 	-	-	9.2	A
Pulse Source to Drain Current (Note 3)	I_{SDM}		-	-	37	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^oC$, $I_{SD} = 9.2A$, $V_{GS} = 0V$ (Figure 13)	-	-	2.5	V
Reverse Recovery Time	t_{rr}	$T_J = 25^oC$, $I_{SD} = 9.2A$, $dI_{SD}/dt = 100A/\mu s$	5.5	100	240	ns
Reverse Recovered Charge	Q_{RR}	$T_J = 25^oC$, $I_{SD} = 9.2A$, $dI_{SD}/dt = 100A/\mu s$	0.17	0.5	1.1	µC

NOTES:

2. Pulse test: pulse width ≤ 300µs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. $V_{DD} = 25V$, starting $T_J = 25^oC$, L = 640mH, $R_G = 25\Omega$, peak $I_{AS} = 9.2A$.

Typical Performance Curves Unless Otherwise Specified

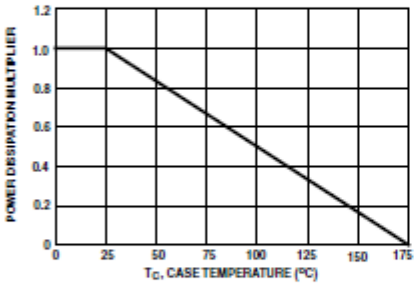


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

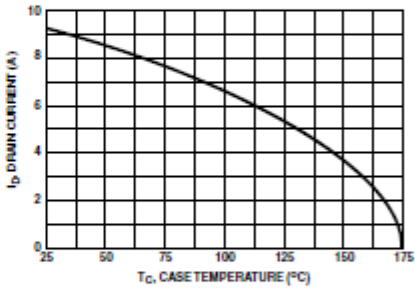


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

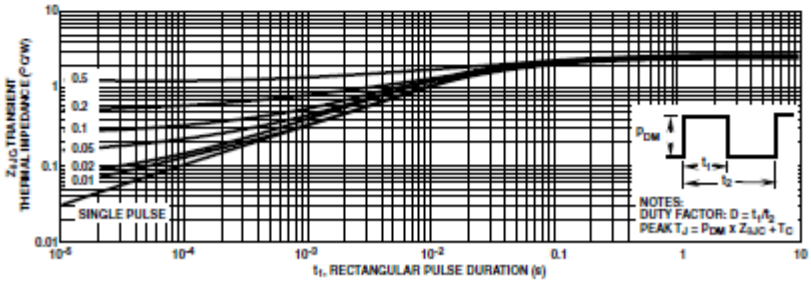


FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves Unless Otherwise Specified (Continued)

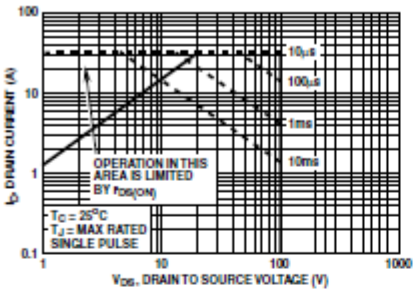


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

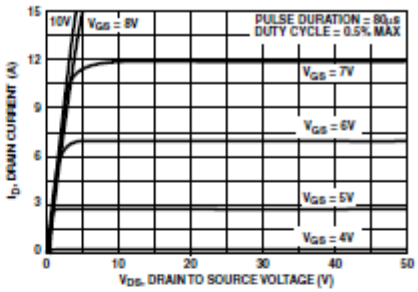


FIGURE 5. OUTPUT CHARACTERISTICS

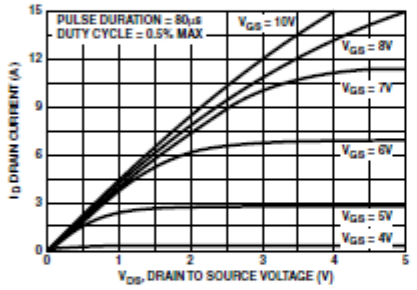


FIGURE 6. SATURATION CHARACTERISTICS

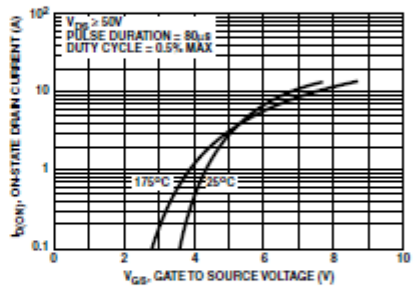


FIGURE 7. TRANSFER CHARACTERISTICS

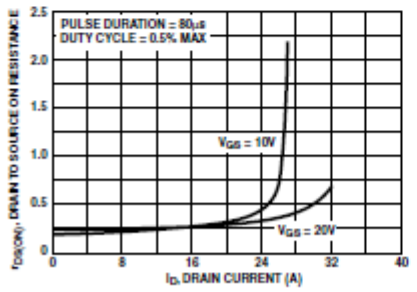


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

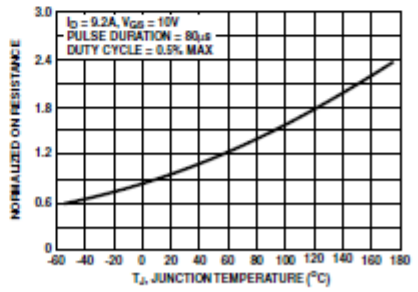


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

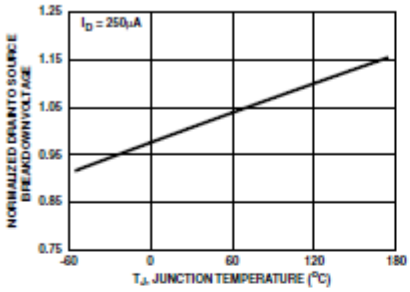


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

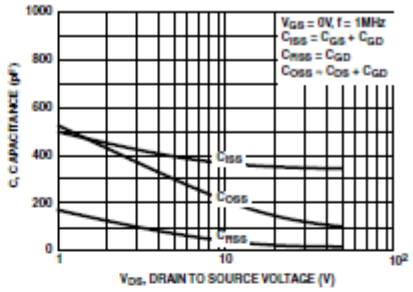


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

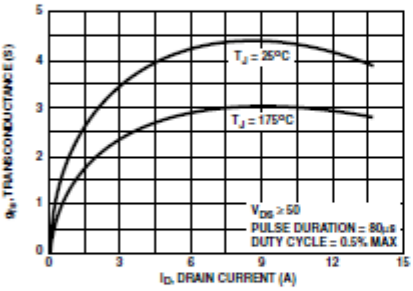


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

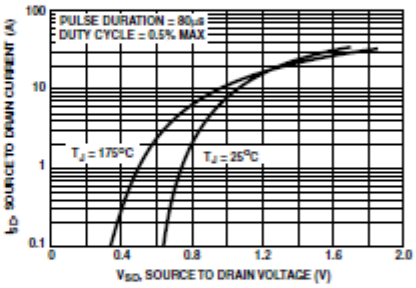


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

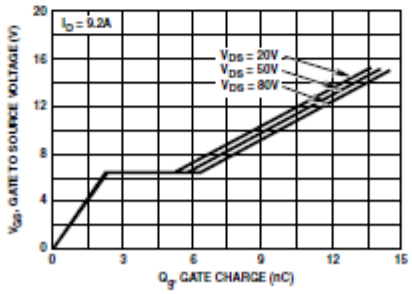


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

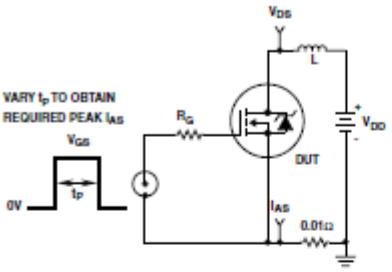


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

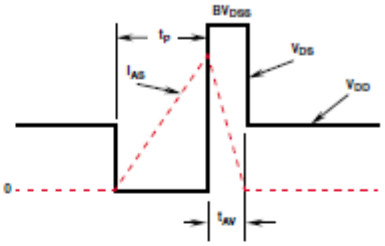


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

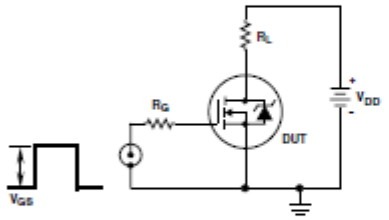


FIGURE 17. SWITCHING TIME TEST CIRCUIT

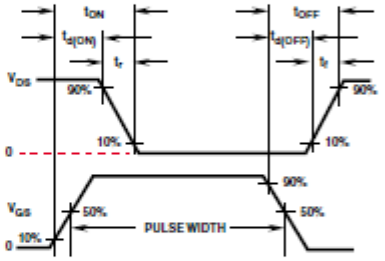


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

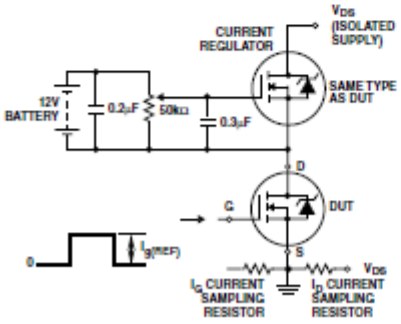


FIGURE 19. GATE CHARGE TEST CIRCUIT

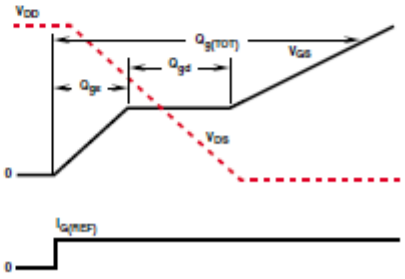


FIGURE 20. GATE CHARGE WAVEFORMS

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CROSSVOLT™	GlobalOptoisolator™	POP™	SuperSOT™-3	
DenseTrench™	GTO™	Power247™	SuperSOT™-6	
DOME™	HiSeC™	PowerTrench®	SuperSOT™-8	
EcoSPARK™	ISOPLANAR™	QFET™	SyncFET™	
E²CMOS™	LittleFET™	QS™	TinyLogic™	
EnSigna™	MicroFET™	QT Optoelectronics™	TruTranslation™	
FACT™	MicroPak™	Quiet Series™	UHC™	
FACT Quiet Series™	MICROWIRE™	SILENT SWITCHER®	UltraFET®	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Definition of Terms

Datasheet Identification	Product Status	Definition
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Rev. H4

APPENDIX B

FAIRCHILD
SEMICONDUCTOR®

KSP2222A

KSP2222A

General Purpose Transistor

- Collector-Emitter Voltage: V_{CEO}= 40V
- Collector Power Dissipation: P_C (max)=625mW
- Refer KSP2222 for graphs

TO-92
1. Emitter 2. Base 3. Collector

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_a=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage	75	V
V_{CEO}	Collector-Emitter Voltage	40	V
V_{EBO}	Emitter-Base Voltage	6	V
I_C	Collector Current	600	mA
P_C	Collector Power Dissipation	625	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C

Electrical Characteristics T_a=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
BV_{CBO}	Collector-Base Breakdown Voltage	I_C=10μA, I_E=0	75			V
BV_{CEO}	Collector Emitter Breakdown Voltage	I_C=10mA, I_B=0	40			V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E=10μA, I_C=0	6			V
I_{CBO}	Collector Cut-off Current	V_{CB}=60V, I_E=0			0.01	μA
I_{EBO}	Emitter Cut-off Current	V_{EB}=3V, I_C=0			10	nA
h_{FE}	DC Current Gain	I_C=0.1mA, V_{CE}=10V V_{CE}=10V, I_C=1mA V_{CE}=10V, I_C=10mA V_{CE}=10V, *I_C=150mA V_{CE}=10V, *I_C=500mA	35 50 75 100 40		 300 	
V_{CE} (sat)	* Collector-Emitter Saturation Voltage	I_C=150mA, I_B=15mA I_C=500mA, I_B=50mA			0.3 1	V V
V_{BE} (sat)	* Base-Emitter Saturation Voltage	I_C=150mA, I_B=15mA I_C=500mA, I_B=50mA		0.6	1.2 2	V V
f_T	Current Gain Bandwidth Product	V_{CE}=20V, I_C=20mA f=100MHz	300			MHz
C_{ob}	Output Capacitance	V_{CB}=10V, I_E=0, f=1MHz			8	pF
t_{ON}	Turn On Time	V_{CC}=30V, I_C=150mA I_{B1}=15mA, V_{BE}(off)=0.5V			35	ns
t_{OFF}	Turn Off Time	V_{CC}=30V, I_C=150mA I_{B1}=I_{B2}=15mA			285	ns
NF	Noise Figure	I_C=100μA, V_{CE}=10V R_S=1KΩ, f=1KHz			4	dB

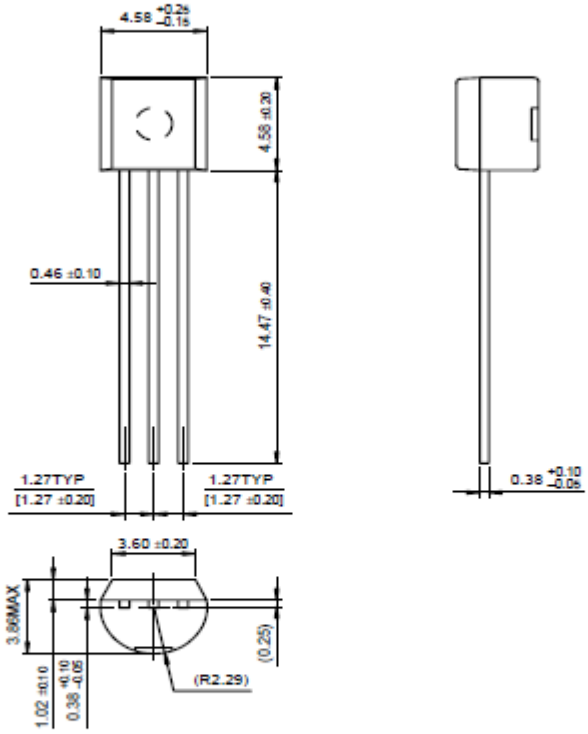
* Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%
* Also available as and PN2222A

Rev. A1, June 2001

KSP2222A

Package Demensions

TO-92



Dimensions in Millimeters

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DenseTrench™	GTO™	PowerTrench®	SuperSOT™-8
DOME™	HiSeC™	QFET™	SyncFET™
EcoSPARK™	ISOPLANAR™	QS™	TruTranslation™
E^2CMOS™	LittleFET™	QT Optoelectronics™	TinyLogic™
EnSigna™	MicroFET™	Quiet Series™	UHC™
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APPENDIX C

SHANGHAI SUNRISE ELECTRONICS CO., LTD.

IN4148

SILICON EPITAXIAL PLANAR SWITCHING DIODE

REVERSE VOLTAGE: 75V

FORWARD CURRENT: 150mA

TECHNICAL SPECIFICATION

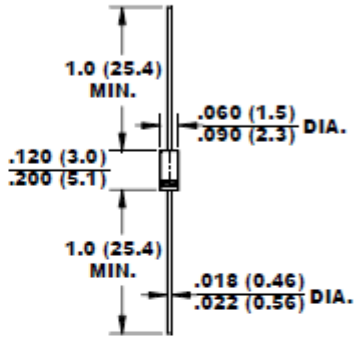
FEATURES

- Small glass structure ensures high reliability
- Fast switching
- Low leakage
- High temperature soldering guaranteed: 250°C/10S/9.5mm lead length at 5 lbs tension

MECHANICAL DATA

- Terminal: Plated axial leads solderable per MIL-STD 202E, method 208C
- Case: Glass,hermetically sealed
- Polarity: Color band denotes cathode
- Mounting position: Any

DO - 35



Dimensions in inches and (millimeters)

MAXIMUM RATINGS AND CHARACTERISTICS

(Ratings at 25°C ambient temperature unless otherwise specified)

RATINGS		SYMBOL	VALUE	UNITS
Reverse Voltage		V_R	75	V
Peak Reverse Voltage		V_{RM}	100	V
Forward Current (average)		I_O	150	mA
Repetitive Forward Peak Current		I_{FRM}	300	mA
Forward Voltage (I_F=10mA)		V_F	1	V
Reverse Current (V_R=20V)		I_{R1}	25	nA
Reverse Current (V_R=75V)			5	μA
Reverse Current (V_R=20V,T_J=100°C)		I_{R2}	50	μ A
Capacitance	(note 1)	Ct	4	pF
Reverse Recovery Time	(note 2)	I_F	4	nS
Thermal Resistance (junction to ambient)	(note 3)	R_θ(ja)	0.35	°C/mW
Operating Junction and Storage Temperature Range		T_{STG},T_J	-55 ~+175	°C

Notes:

1: V_R=0V, f=1 MHz

2: I_F=10mA to I_R=1mA, V_R=6V, R_L=100Ω

3: Valid provided that leads are kept at ambient temperature at a distance of 8mm from case.

http://www.sse-diode.com

APPENDIX D

WEITRON

1N4728A Thru 1N4761A

Axial Lead Zener Diodes

Pb Lead(Pb)-Free

SMALL SIGNAL ZENER DIODES 1.0 WATTS

Features:

* High reliability
* Very sharp reverse characteristic
* Low reverse current level
* VZ-tolerance ±5%

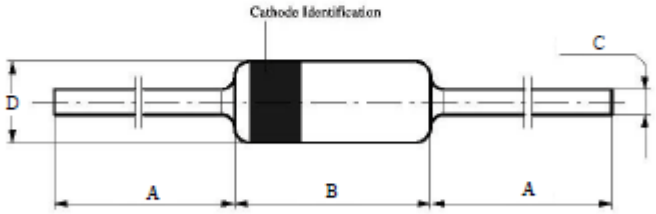
DO-41

Mechanical Data:

* Voltage stabilization
* Case : DO-41 Glass Case
* Weight : Approx 0.33 gram

DO-41 Outline Dimensions

Unit:mm



	A		B		C		D	
DIM	Min	Max	Min	Max	Min	Max	Min	Max
DO-41	26.0	-	-	4.50	-	0.85	-	2.7

Maximum Ratings and Electrical Characteristics (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	Value	Unit
Power dissipation $T_A \leq 50°C$	P_V	1.0	W
Z-current	I_Z	P_V/V_Z	mA
Junction ambient l=9.5mm(3/8") T_L=constant	$R_{\theta JA}$	100	K/W
Junction temperature	T_J	200	°C
Storage temperature range	T_{stg}	-65~+175	°C

Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Forward voltage I_F=200mA	V_F	-	-	1.2	V

Type	V_{Znom} [1]	I_{ZT} for	r_{ZT}	r_{ZK} at	I_{ZK}	I_R at	V_R
	V	mA	Ω	Ω	mA	μA	V
1N4728A	3.3	76	<10	<400	1	<100	1
1N4729A	3.6	69	<10	<400	1	<100	1
1N4730A	3.9	64	<9	<400	1	<50	1
1N4731A	4.3	58	<9	<400	1	<10	1
1N4732A	4.7	53	<8	<500	1	<10	1
1N4733A	5.1	49	<7	<550	1	<10	1
1N4734A	5.6	45	<5	<600	1	<10	2
1N4735A	6.2	41	<2	<700	1	<10	3
1N4736A	6.8	37	<3.5	<700	1	<10	4
1N4737A	7.5	34	<4.0	<700	0. 5	<10	5
1N4738A	8.2	31	<4.5	<700	0. 5	<10	6
1N4739A	9.1	28	<5.0	<700	0. 5	<10	7
1N4740A	10	25	<7	<700	0.25	<10	7.6
1N4741A	11	23	<8	<700	0.25	<5	8.4
1N4742A	12	21	<9	<700	0.25	<5	9.1
1N4743A	13	19	<10	<700	0.25	<5	9.9
1N4744A	15	17	<14	<700	0.25	<5	11.4
1N4745A	16	15.5	<16	<700	0.25	<5	12.2
1N4746A	18	14	<20	<750	0.25	<5	13.7
1N4747A	20	12.5	<22	<750	0.25	<5	15.2
1N4748A	22	11.5	<23	<750	0.25	<5	16.7
1N4749A	24	10.5	<25	<750	0.25	<5	18.2
1N4750A	27	9.5	<35	<750	0.25	<5	20.6
1N4751A	30	8.5	<40	<1000	0.25	<5	22.8
1N4752A	33	7.5	<45	<1000	0.25	<5	25.1
1N4753A	36	7.0	<50	<1000	0.25	<5	27.4
1N4754A	39	6.5	<60	<1000	0.25	<5	29.7
1N4755A	43	6.0	<70	<1500	0.25	<5	32.7
1N4756A	47	5.5	<80	<1500	0.25	<5	35.8
1N4757A	51	5.0	<95	<1500	0.25	<5	38.8
1N4758A	56	4.5	<110	<2000	0.25	<5	42.6
1N4759A	62	4.0	<125	<2000	0.25	<5	47.1
1N4760A	68	3.7	<150	<2000	0.25	<5	51.7
1N4761A	75	3.3	<175	<2000	0.25	<5	56

1) Based on DC-measurement at thermal equilibrium while maintaining the lead temperature(T_L)at 30℃, 9.5mm(3/8") from the diode body.