MODELING AND IMPLEMENTATION OF SPACE VECTOR MODULATION FOR THREE-PHASE DIRECT TORQUE CONTROL MATRIX CONVERTER

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Thesis submitted in fulfilment of the requirements
for the award of the degree of
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SUPERVISOR'S DECLARATION

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Specially dedicated to

my lovely parents Rekiah Ismail and Ghoni Isa,

Husband Mohd Nuhairi,

Sons and daughter Aiman Asyraf, Alisa Sofia and Adam Haris

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ABSTRACT

Matrix converter (MC) as induction motor drivers have received considerable attention because of its high integration capability and the higher reliability direct AC-AC power converter without any bulky DC link component. It can provide sinusoidal output current and input current, adjustable input power factor, and regeneration capability; and very attractive in areas where volume, efficiency and reliability are important. Widespread, systematic, and in-depth studies have been focused on the modulation algorithm and the commutation strategy of the MC, and the key technologies for its application in induction motor drive system. In this thesis, the main aim is to improve the performance of the induction motor drive based on the space vector modulation (SVM) method. In addition, some improvement is performed which are by using close-loop induction motor drive controller based on the relations of the efficiency and power factor with the rotor frequency and slip frequency in a steady state mathematical model and second, enhancing this controller by replacing the PI controller with the combination of Direct Torque Control (DTC) and Particle Swarm Optimization (PSO). The combination of DTC-PSO technique generates the required voltage vectors under 0.86 input power factor operations and it also gains the change regularity between efficiency and power factor. The duty cycles of the switches are modeled using SVM for 0.65 voltage transfer ratios. The mathematical models for the proposed systems are implemented by using *Matlab/Simulink* for different speed and load. Finally, the whole system has been verified from the experiments and the output voltage, and the input current generated by the model of the converter. The results demonstrate the good quality and robustness in the system dynamic response and a reduction in the steady-state and transient motor ripple torque.

ABSTRAK

Kebelakangan ini, matrik penukar (MC) sebagai pemandu motor induksi telah menerima perhatian kerana keupayaan integrasi yang tinggi dan kebolehpercayaan yang lebih tinggi sebagai penukar kuasa langsung AC-AC tanpa meggunakan sebarang komponen sambungan DC yang sangat besar. Ia boleh menyediakan arus keluaran dan arus masukan yang sinusoidal, faktor kuasa masukan boleh laras, dan keupayaan penjanaan semula; dan ia sangat menarik digunakan pada keadaan kecekapan isipadu dan kebolehpercayaan adalah penting. Fokus kajian yang meluas, sistematik, dan mendalam telah dilakukan kepada modulasi algoritma dan strategi peringanan MC, dan juga teknologi utama bagi kegunaan dalam sistem pemacu motor aruhan. Tujuan utama tesis ini adalah untuk meningkatkan prestasi pemacu motor aruhan yang berdasarkan ruang vektor kaedah modulasi (SVM). Di samping itu, beberapa pembaikan dilakukan yang dengan menggunakan pemacu motor aruhan litar-tutup berasaskan hubungan kecekapan dan faktor kuasa dengan frekuensi pemutar dan frekuensi gelinciran di dalam keadaan mantap dan kedua meningkatkan pengawal ini dengan menggantikan pengawal PI dengan gabungan Kawalan Langsung Daya Kilasan (DTC) dan Particle Swarm Optimization (PSO). Gabungan teknik DTC-PSO menjana vektor voltan yang diperlukan di bawah 0.86 operasi input faktor kuasa dan ia juga mendapat kekerapan menukar antara kecekapan dan faktor kuasa. Kitaran bekerja suis dimodelkan menggunakan SVM bagi nisbah pemindahan voltan 0.65 Model matematik untuk kawalan langsung MC berasaskan SVM dilaksanakan dengan menggunakan *Matlab/Simulink* untuk kelajuan dan beban yang berbeza. Akhir sekali, seluruh sistem telah disahkan dari eksperimen dan voltan keluaran, dan arus masukan yang dihasilkan oleh model pengubah. Keputusan menunjukkan kualiti yang baik dan kekukuhan dalam sistem gerak balas dinamik dan pengurangan dalam riak daya kilasan motor keadaan mantap dan fana.

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LIST OF SYMBOLS

m	Modulation index
V_{pn}	DC-link voltage
T_s	Sampling period
η	Efficiency
$f_1,\ f_2$	Stator and rotor frequency
Γ_r	Rotor time constant
$\psi_{rd},\ \psi_{rq}$	*dq* rotor flux.
$\psi_{sd,}\ \psi_{sq},$	*dq* stator flux
$\vec{\lambda}_r$	Rotor flux linkage space vector
$\vec{\lambda}_s$	Stator flux linkage space vector
$\vec{\mathrm{i}}_{\mathrm{p}}$	VSI averaged input current
$\sin(\emptyset_i)_Q$	output power factor regulator
$\sin(\emptyset_i)_f$	observed value of power factor regulator
$\sin(\emptyset_i)_g$	given value of power factor regulator
$\vec{\mathrm{T}}_{\mathrm{ph}}$	Transfer matrix
$\vec{\mathrm{T}}_{\mathrm{VSI}}$	Space vector representation of transfer matrix of VSI
$\vec{\mathrm{T}}_{\mathrm{VSR}}$	Space vector representation of transfer matrix of VSR
$\vec{\mathrm{V}}_s,\ \vec{\mathrm{V}}_r$	Stator and rotor voltage space vector
$\vec{I}_{i_{ref}}$	Reference current vector
$\vec{I}_a, \vec{I}_b, \vec{I}_c$	Space vector representation of input current *a*, *b* and *c*
$\vec{I}_i, \vec{I}_o$	Space vector representation of input and output current
$\vec{V}_{o_{ref}}$	Reference voltage vector $\vec{V}_o$
$\vec{V}_i, \vec{V}_o$	Space vector representation of input and output voltage

$\vec{V}_{pn}$	Space vector representation of DC-link voltage
$\emptyset_L$	Phase angle between the load current and the load voltage
$\emptyset_i$	Phase angle between the input current and the input voltage
$\emptyset_o$	Phase angle between the output current and the output voltage
$\cos\varphi$	Power factor
$C_{3/2}$	$^{3}/_{2}$ transformation matrix of the *abc* frame to dq frame
I_j	The switch stage of the inversion stage
I_{om}	Maximum output current
L_{lr}	Rotor leakage inductance
L_s, L_r, L_m	Stator, rotor and the magnetizing inductance
R_i	The switch stage of the rectification stage
R_s	Stator resistance
T_L	load torque
T_e	Electromagnetic torque
V_0	Zero voltage vector
V_a, V_b, V_c	Input voltage *a*, *b* and *c*
V_{ab},V_{ac}	Inputs line-to-line voltages
V_{im}	Maximum input voltage
V_{iph}	Input phase voltage
V_{sd}, V_{sq}	Stator voltage at *d* and *q* frame
V_u, V_v, V_w	Output voltage *u*, *v* and *w*
$V_u(t), V_v(t), V_w(t)$	Instantaneous output voltage *u*, *v* and *w*
V_x	Flux controller loop to SVM
V_y	Output torque controller loop to SVM
d_{α_vi},$d_{\beta\alpha\_vi}$	Switching vector duty cycles

$e_{\psi s}$	Error for stator flux
i_{sd}	Stator current at *d* frame
$k_{p\psi}$.	Proportional gain for flux
m_i	VSR modulation index
m_v	Input voltage modulation index
p_n	Number of poles
ε_{ϕ_i}	Tolerance
θ_v, θ_i	Input and output arbitrary angle
ω_0	Output angular velocity
ω_i	Input angular velocity
$\Delta\omega^B$	Rotor angular frequency corresponding to the maximum point of the slip frequency
$\Delta\omega$	Slip frequency
c_1 , c_2	Acceleration coefficients
gbest	Best particle among the entire population
I	Inversion stage
i_{ar}, i_{br}, i_{cr}	Rotor current
i_{as}, i_{bs}, i_{cs}	Stator current
I_{dc}	DC current generator
J	Moment of inertia
M	Modulation matrix
P	Active power
$pbest_i$	Best previous position of x_i
Q	Reactive power
R	Rectification stage

$rand_1$, $rand_2$	Random functions
T	Converter transfer matrix
v_i	rate of the velocity for particle x_i
w	Inertia weight factor
x_i	*ith* particle
J	Moment of inertia
ω	Angular velocity

LIST OF ABBREVIATION

ANN	Artificial Neural Network
ASVM	Asymmetrical SVM
DMC	Direct Matrix Converter
DSP	Digital Signal Processing
DTC	Direct Torque Control
IDP	Isolated Driver Potentials
IGBT	Insulated Gate Bipolar Transistor
IM	Induction Motor
IMC	Indirect Matrix Converter
IPID	Intelligent PID
ITF	Indirect Transfer Function
MC	Matrix Converter
PWM	Pulse Width Modulation
SMC	Sparse Matrix Converter
SSVM	Symmetrical SVM
SVM	Space Vector Modulation
THD	Total Harmonic Distortion
USMC	Ultra Sparse Matrix Converter
VSI	Voltage Source Inverter
VSMC	Very Sparse Matrix Converter
VSR	Voltage Source Rectifier
VVVF	Variable Voltage Variable Frequency

CHAPTER 1

INTRODUCTION

1.1 OVERVIEW OF MATRIX CONVERTER

Matrix converter (MC) has recently received considerable interests, because it possesses the topological and operational features to fulfill these current trends for the drives (Venturini 1980; Huber and Borojevic 2002; Kazmierkowski et al. 2002; Kwak 2007). The converter has also attracted the industry application, and the technical development has been further accelerated because of a strong demand in power quality, energy efficiency and downsizing of the converters (Deblon 2007). The induction motor drive fed by MC is superior to the conventional inverter because of the lack of the bulky DC-link capacitors with limited lifetime and high cost, the bidirectional power flow capability, the sinusoidal input and output currents, no harmonic problems and adjustable input power factor. Furthermore, because of the high integration capability and the higher reliability of the semiconductor structures, the MC topology is recommended for extreme temperatures and critical volume or weight applications.

1.2 PROBLEM STATEMENT

With the development of power electronics, frequency control has been in the communication speed to occupy a dominant position. The key drive for industrial automation technology is an important means of energy efficiency. Motor control theories, especially the Direct Torque Control (DTC) development and improvement of the theory, making the effect of AC variable frequency drive and DC speed comparable, especially in the DTC system superior in terms of fast torque response. Coupled with the inherent advantages of AC motors, making the exchange adjustment speed occupied

more than 80%. Direct torque control of induction motor is a response to these needs arising from the new motor control theory, which uses space vector analysis, the direct calculation of the stator coordinates system and the torque control of AC motor, with stator flux orientation, by PWM signal directly to the inverter switching state of optimal control to obtain high dynamic performance of torque. The torque responsive control system, limited to within a shot, and no overshoot, is a high dynamic performance speed control method of communication. Therefore, this research has important practical significance in asynchronous motor DTC.

Matrix converter is an excellent input and output characteristics of the AC direct power converter, which allows the frequency unipolar conversion, no large-capacity storage device such as a large capacitance, sinusoidal input current, input power factor more than 0.99 and can be freely adjusted, and has nothing to do with the load power factor. The output voltage sinusoidal, the output frequency; voltage adjustable output frequency may be higher, below the input frequency. In particular, its power can flow in both directions, with a four quadrant operation capability, combined with small size; high efficiency, modular development in line with MC in the AC drive system can generate significant cost saving, but also avoid pollution caused by power system harmonic's environmental issues. MC and DTC system architecture of the AC drive system is a non negative effect, precision of the sustainable development control system, and thus of far reaching.

1.3 RESEARCH OBJECTIVES

The main research objectives are set as follows:

- To study the induction motor MC drive based on the space vector modulation (SVM) method.
- To improve the design of the IM based MC-SVM drive based on the power factor method.
- To enhance the proposed MC induction motor controller using a combination of DTC-PSO technique along with the existing power factor method.
- To validate the performance of MC-DTC-PSO experimentally based on the output voltage, and the input current generated by the model of the converter.

1.4 RESEARCH SCOPES

The research scopes are:

- The research apply on the Indirect Transfer Function algorithm of the MC
- The proposed system is implemented on the three-phase 1 hp Induction Motor.

1.5 MAIN CONTRIBUTION OF THE THESIS

The main contributions of this thesis are summarized as follows:

- Improvement of the induction motor drive performance based on the space vector modulation (SVM) method.
- Designing a new induction motor MC drive based on the SVM by using the close-loop induction motor drive controller based on the relations of the efficiency and power factor with the rotor frequency and slip frequency.
- Enhancing the controller by using the combination of Direct Torque Control – Particle Swarm Optimization (DTC-PSO) technique.

1.6 THESIS ORGANIZATION

The thesis consists of five chapters with the content of each chapter is outlined as follows:

Chapter 1 of the thesis discusses on the brief overview of MC development and its application in the industry. The objectives and contributions of the thesis are also presented.

Chapter 2 reviews the basic MC technology and its protection issues as a background for the research. The bidirectional switch configurations and MC topologies are presented. The fundamental of the SVM and switching principle as well as the basic of Direct Torque Control are also presented.

Chapter 3 discusses the proposed control method in getting the optimum efficiency for the IM with the first analysis done on the relations of the IM efficiency and power factor. Next, the combination of the power factor control with the DTC and PSO are also discussed. This chapter also presents the laboratory setup of the MC.

Chapter 4 analyzes the simulation results of the proposed control algorithm and verified with the actual performance. The operating performance and other aspects of the research as well as the designs of the actual reference are also discussed.

Chapter 5 summarizes the achievements of the research and the recommendations for future work.

CHAPTER 2

LITERATURE REVIEW

2.1 RESEARCH AND APPLICATION OF MATRIX CONVERTER

Over the years, the discussion on matrix transformation technology have been discussed that will drive the next generation of the inverter. The MC eliminates the need to pay an AC inverter DC-link, absorbs any current clutter and also provides a clean output voltage, which can be effective for input regulator output voltage and current control. Furthermore, it can achieve the power factor of 1, sinusoidal input current and capable of operating in four quadrants. Another attraction is the ability to remove the DC capacitor and thus, increase its reliability. Although the MC has a very attractive prospect, but because of its high cost had limited the existence in the current commercial applications.

Form of MC topology was first proposed by Gyugyi and Pelly (1976). Venturini (1979) proposed the nine components of the power switch to pay a delivery transformation matrix device structure, and that its input power factor angle can be adjusted. Later, the finding showed that this converter has inherent limits, which the maximum voltage gain is 0.866, and has nothing to do with the control algorithm. The concepts of the MC were first to give a low-frequency characteristic and proposed frequency modulation and its algorithms, known as direct transfer recursive function method (Venturini 1979).

The MC is theoretically equivalent to a rectifier and inverter virtual connection. The traditional pulse width modulation (PWM) techniques were applied to the rectifier

and inverter as a two way modulation switch in order to achieve energy transfer and feedback. This method is also called indirect transfer function (Rodriguez 1983).

With the power electronics and computer control technology continues to evolve, research on MC increasingly valued by the people and solving Venturini and Alesina control programs in less than proposed by (Venturini and Alesina 1980). A series of MC research from various angles with different control schemes suggested an indirect PWM control method (Ziogas et al. 1985). The overall idea was to first input voltage or rectifier, resulting in a virtual DC circuit, then presses the desired frequency inverter, resulting in a similar typical PWM inverter output voltage waveform. The studies of the basic control scheme to overcome the shortcoming of *Venturini*, output voltage ratio, power factor and input current quality had made good improvements. However, there was a limitation on the output frequency which is up to only 300Hz.

Huber et al. (1989) proposed a technique based on SVM-PWM technology. First, the PWM-MC according to the switching states defines the hexagonal switch state vector. Then, the output vector of the adjacent switching state vector was synthesized to be the switch of each sampling duty period. The continuous synthesis of a certain angular rotation of the output voltage vector will obtain the required frequency and sinusoidal output voltage. The use of space vector transfer MC is proving to be consistent with the theoretical analysis; that is with input power factor close to 1, and good input current waveform. Braun and Rodriguez (Braun and Hasse 1983; Kastner and Rodriguez 1985) proposed space vector amount of pulse width modulation (SVPWM) used the method of MC control. Huber et. al. (Huber and Borojevic 1989; Huber et al. 1989; Huber et al. 1992; Huber et al. 1993; Huber and Borojevic 1995) analyzed and designed the space vector modulated three-phase to three-phase MC with input power factor correction. The simultaneous output-voltage and input-current space vector modulation, was systematically reviewed. The modulation algorithm is theoretically derived from the desired average transfer functions, using the indirect transfer function (ITF) approach. The input power factor is above 0.99 in the whole operating range

Ishiguro et al. (1991) proposed the dual voltage instantaneous value method which presented a novel control method for forced commutated PWM. Using this control method the sinusoidal input and output current waveforms and the unity input displacement factor can be obtained. Moreover, the compensation of the asymmetry and harmonic contaminated input source voltages was easily realized. This control method allows the input displacement factor not to be controllable, but to be fixed at approximately unity. Since a unity input displacement factor is desirable for motor drive use for the PWM cycloconverters, this constraint is not a new obstacle. The technology improved the converter switching frequency limit and increase the output voltage ratio. Moreover, the compensation of the asymmetry and harmonic contaminated input source voltages is easily realized with real time control. However, the control scheme allows control of the input power factor not to be controllable, but to be fixed at approximately unity. However, the switch state of the conversion process and the input current synthesis required more complex rules and software. Rossiter Corrêa et al. (2006) presented a PWM method for control of four-switch three-phase inverters. The proposed vector PWM offers a simple method to select three or four vectors that effectively synthesize the desired output voltage, even in presence of voltage oscillations across the two dc-link capacitors. The method utilizes the SVM, and includes its scalar version. The effect of Wye and delta motor winding connections over the pulse width modulator was also considered. The common mode voltage generated by the four-switch three-phase converter is evaluated and compared to that provided by the standard six-switch three-phase inverter. The result showed that the PWM pattern based on three vectors, in which two are small, presents the lowest harmonic distortion. However, the common-mode voltage analysis points out that use of the two greatest vectors are more adequate for common-mode voltage reduction. Kwon and Cha (1993) proposed the MC by non-ideal current source and voltage source composed of *dq* circuit transformation technique using practical step up nine dynamic switching MC.

Burany (1989) proposed a four-step commutation strategy, which can be realized with soft-switching semi-converter. The bidirectional switch commutation process between the relative size of the voltage and current direction of the signal is divided into four steps, which effectively avoid the commutation process of the short circuit and open circuit failure, to achieve a real sense of flow security. Since then,

Ziegler and Hoffman (2002) proposed a two-step flow method of MC further reducing the time flow for two-way switch. Meanwhile, Empringham et al. (2002) proposed a smart way converter using a programmable logic device (PLD) technique which used according to the current direction of the signal detection and switching-off state for the use of temporal logic to determine the steps flow. Mahlein et al. (2002) proposed an improved multi-step strategy for flow control, eliminating the need for a special direction of the input voltage or output current detection circuit. Wei et al. (2003) also proposed an MC voltage converter mode. The current strategy for the application was basically to achieve the safe operation of a bidirectional switch for the MC application in the actual industry.

Matrix converter is made from 1976 and has been present for 30 years; researchers have made many experimental prototypes of MC, but not really into the practical reports. Xinyi (1994) using SVM analysis of DC- AC and AC-DC converter and obtained AC-AC converter modulation method after synthesized, and used a digital signal processor TMS32014 as the controller, designed and fabricated the prototype experiment. Nielsen et al. (2002) developed the controller using SIEMENSC166 as the peripheral circuit of MC.

2.2 THEORETICAL BACKGROUND

2.2.1 Bidirectional Switches

A matrix converter consists of nine bidirectional switches, arranged in three groups of three, each group being associated with an output line. This arrangement connects any of the input line *a*, *b*, or *c* to any of the output line *u*, *v* or *w*, as shown in Figure 2.1. A bidirectional switch can control the current and to block the voltage in both directions.

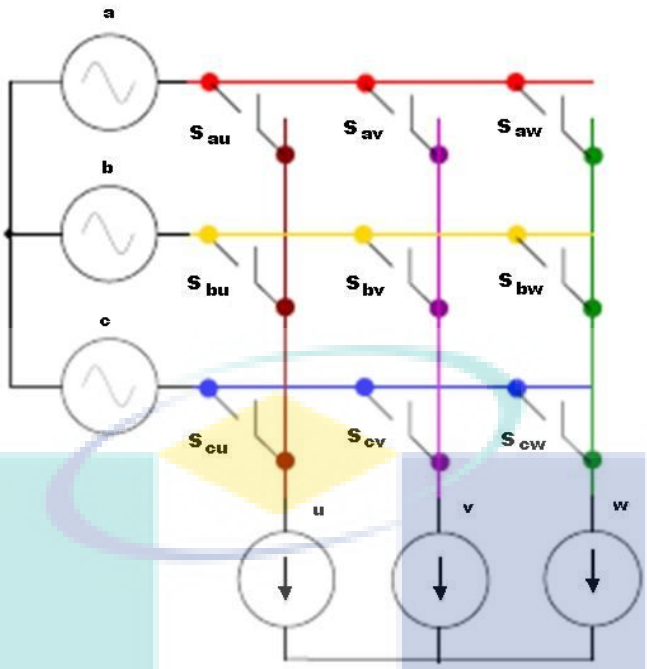


Figure 2.1: Matrix converter principle

The arrangement of bidirectional switches is such that any of the input phases *a*, *b*, *c* is connected to any output phases *u*, *v*, *w*. The switches are controlled in such a way that the average output voltage is a sinusoid of desired frequency with desired amplitude. The three by three switches give 512 combinations of switching states. Compared with other AC to AC converters, the MC has the following advantages:

- Inherent four quadrant operation and regeneration capability due to the use of the bidirectional switch and hence it can be used as an alternative to PWM inverter drive for three-phase frequency control.
- Pure sine in and pure sine out waveforms are the unique features of the MC.
- Displacement factor is unity
- High drive performance and long life due to the absence of intermediate DC- link circuit.

The practical realization of the MC requires bidirectional switches capable of blocking voltage and conducting current in both directions, but there is no such device available currently. All switching actions involve power dissipation because the

switches contain on-state resistance during continuous conduction. Various options of single phase bidirectional switches are shown in Figure 2.2.

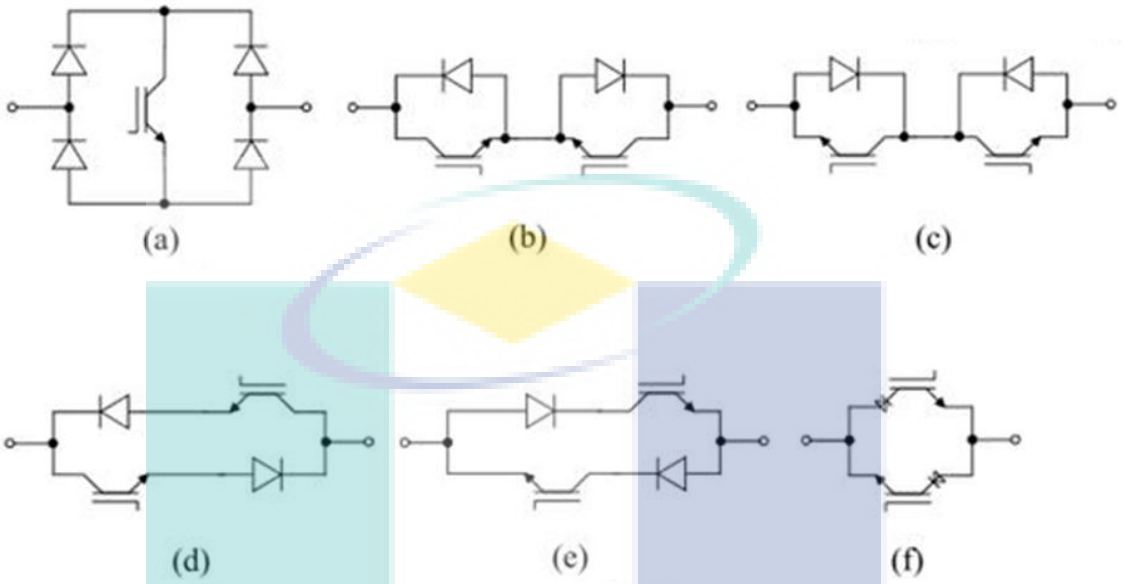


Figure 2.2: Bidirectional switches (a) IGBT and diode bridge, (b) Common-emitter (c) common-collector (d) Common cathode diode and switch in series (e) Common anode diode and switch in series (f) anti-parallel IGBT configuration

The configuration in Figure 2.2 (a) contains only one active switch and is the simplest choice. However, it cannot be used in MCs with most safe commutation methods. In addition, it has more conducting components in a supply-to-load current path than the configurations in Figure 2.2 (b) to (f). Conventionally, the most popular MC switches have been common-emitter and common-collector configurations (Nielsen et al. 2002; Wheeler et al. 2002; Wheeler et al. 2002) due to the single active switch and diode conducting per output phase. In practice, the only difference is the number of required isolated emitter potentials i.e. A common-collector switch requires only six isolated gate control units, whereas the common-emitter requires nine. The common-collector based IGBT modules containing all switches of the MC have been available for a low power range (Wei and Lipo 2004; Jussila and Tuusa 2007) and IGBT modules with a common-emitter bidirectional switches are also available (Bruckmann et al. 2001; Motto et al. 2004; Casadei et al. 2005; Itoh and Nagayoshi 2007).

The separated serial combinations Figure 2.2 (d) to (e), are not as commonly used as the previous two, and they have similarities with the switches required in the current source converter. However, differences arise from the number of isolated gate drivers: with the MC, the configuration in Figure 2.2 (d) requires eighteen isolated gate drivers, whereas the configuration in Figure 2.2 (e) requires only six, as in the common-collector configuration. A fast switching pair such as Figure 2.2 (c) can be employed if the devices have reverse blocking capabilities, such as the MCT or the non-punch-through IGBT. Figure 2.3 shows a fast-acting switch that has been reportedly used in matrix converter (Kang et al. 2002; Martin 2004; Takeshita and Andou 2010). Two IGBTs is connected using a common-collector configuration. Since an IGBT does not have reverse blocking capability, two fast recovery diodes are connected with the anti-series, each in inverse parallel across an IGBT, to sustain a voltage of either polarity when both IGBTs are switched off. Independent control of the positive and negative currents can be obtained that permits a safe commutation technique to be implemented.

Figure 2.3: Practical switch for matrix converter operation (a) heat sink mounting (b) equivalent circuit

The common-collector configuration has the practical advantage that the four switching devices, two diodes and two IGBTs, can be mounted, without isolation, onto the same heat sink. Natural air-cooled heat sinks are used in each phase to dissipate the estimated losses without exceeding the maximum allowable junction temperatures.

2.2.2 Topologies

A traditional MC configuration is based on a direct AC power conversion by directly connecting three-phase input voltages to three-phase output loads through bidirectional switches with no intermediate power conversion stage (Wheeler et al. 2002). The advantage of the direct matrix converter (DMC) is no limitation on the output frequency as compared to the cycloconverter. However, there is a limitation on the output amplitude and this can be solved using overmodulation technique. The second approaches to interconnection systems using MC are known as indirect matrix converters (IMC). Two energy stages in IMC (Jussila and Tuusa 2007) are the rectifier, which converts the three-phase input to DC output and the inverter which inverts the DC back to AC with different variables on the output. The two stages of energy conversion are decoupled and controlled independently, and average energy flow is equal. The difference between the instantaneous input and output power must be absorbed or delivered by an energy storage element within the converter which is a capacitor or an inductor.

Various MC topologies have been studied and are not only concerned on conventional DMC. The IMC has also been studied and can be considered an option for the DMC (Kolar et al. 2002; Minari et al. 2002; Jussila et al. 2005; Klumpner and Blaabjerg 2005; Klumpner 2006; Takeshita and Andou 2010). Jussila and Tuusa (2007) (2007) compared the space vector modulated DMC and IMC supplies induction motor. In an ideal case, DMC and IMC provide similar performance with an identical control system. However, in real motor drives some differences in output voltages, and power losses occur caused by different main circuits; whose effects are increased by different commutation methods needed to provide safe operation in both cases. Thus, the output voltages of the converters do not follow their references similarly, but the effects of non-ideals are more severe in the IMC than in the DMC. In addition, the efficiency of the IMC is smaller than DMC under most loading situations tested.

A. Direct Matrix Converter

In order to provide balance for the output voltages and for the input currents, it is necessary that the modulation strategy uses the input voltages equally when producing the output voltages. Direct control, also referred to as scalar modulation or *Venturini* modulation (Venturini 1980), establishes independent relations for each output, by sampling and distributing slides of input voltages in such a way that the average result follows the reference output phase voltage and the average input currents are sinusoidal.

B. Indirect Matrix Converter

The IMC model uses only active vectors. The main idea of the technique is to consider the MC as a two-stage transformation converter; a rectification stage to provide a constant virtual DC-link voltage V_{pn} during the switching period by mixing the line-to-line voltages in order to produce a sinusoidal distribution of the input currents, and an inverter stage to produce the three output voltages. Figure 2.4 shows the converter model when the indirect modulation technique is used.

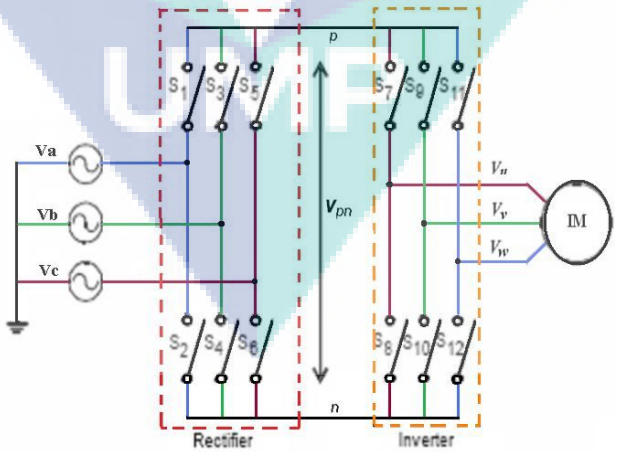


Figure 2.4: Indirect matrix converter topology

The indirect approach has mainly the merit of applying the well-established space vector modulation (SVM) for voltage source inverter (VSI) to MC, although

initially proposed only for the control of the output voltage (Kazmierkowski et al. 2002; Musallam and Johnson 2011). The SVM was successively developed in order to achieve the full control of the input power factor, to fully utilize the input voltages and to improve the modulation performance (Wheeler et al. 2002; Deblon 2007; Kwak 2007; Xiaohong et al. 2009). A comparison between different types of modulation strategies showing that the indirect approach for MCs, initially preferred for its simplicity, is now partially replaced by modern direct theories, that allow an immediate understanding of the modulation process, without the need for a fictitious DC-link (Kolar et al. 2002; Wheeler et al. 2002; Pena et al. 2009; You et al. 2011).

C. Sparse Matrix Converter

Other derivative topologies of MC are the sparse matrix converter (SMC) (Kolar et al. 2002; Park and Lee 2009; Park and Lee 2010). SMC offers a reduced number of components, a low complexity modulation scheme and realization effort (Kolar et al. 2002; Wei et al. 2002; Fang and Chen 2009; Zhang et al. 2009). Invented in 2001, SMC avoids the multi-step commutation procedure of the conventional MC, improving system reliability in industrial operations. Its principal application is in highly compact integrated AC drives. It provides identical functionality, but with a reduced number of power switches and the option of employing an improved zero DC-link current commutation scheme, which provides lower control complexity and higher safety and reliability compared to the DMC. The Very Sparse Matrix Converter (VSMC) topology is developed from 12 transistors, 30 diodes, and 10 IDP. There are no limitations in functionality compared to the DMC and SMC. However, it has fewer transistors and higher conduction losses due to the increased number of diodes in the conduction paths compared to the SMC. Meanwhile, the Ultra Sparse Matrix Converter (USMC) topology is nine transistors, 18 diodes, and seven IDP. The significant limitation of this converter topology compared to SMC is the restriction of its maximal phase displacement between input voltage and input current, which is restricted to ± 30°.

D. Z-source Matrix Converter

The other topology is Z-source MC, which comprises of two type structure; voltage-fed and current-fed. A type of three-phase AC-AC Z-Source converters, which are derived from MC theories were proposed which overcomes the voltage transfer limitation of MC and also exhibits the inherent benefits of MC. (Klumpner and Blaabjerg 2002; Liu et al. 2010). Only additional passive components are required without any increase in the number of power semiconductor switches, which can increase the complexity of control. A current-fed Z-source MC topology was proposed which combines the current-fed Z-source AC-AC converter with traditional current-fed MC. It has lower output voltage and higher reliability and able to overcome the conceptual and theoretical barriers and limitations of the MC (Klumpner et al. 2002; Fang et al. 2011; Ge et al. 2012).

2.3 FUNDAMENTAL OF SPACE VECTOR MODULATION

Space vector modulation refers to a special switching sequence which is based on the upper switches of a three-phase MC. Theoretically, SVM treats a sinusoidal voltage as a phasor or amplitude vector which rotates at a constant angular frequency, ω. This amplitude vector is represented in *dq* plane where it denotes the real and imaginary axes. As SVM treats all three modulating signals or voltages as a single unit, the vector summation of three modulating signals or voltages are known as the reference voltage, $V_{o_{ref}}$ which is related to the magnitude of output voltage of the switching topologies. The aim of SVM is to approximate the reference voltage vector, $V_{o_{ref}}$ from the switching topologies. For a three-phase MC, there are 27 valid switches combinations giving thus 27 voltage vectors as shown in Appendix A. The switching combinations can be classified into three groups, which are, synchronously rotating vectors, stationary vectors and zero vectors.

A *stationary vector* (Group I) is classified into three sets. Each of these has six switch combinations and has a common feature of connecting two output phases to the same input phase. The corresponding space vectors of these combinations have a constant phase angle, thus being named *stationary vector*.

A *zero vector* (Group II) is the final three combinations in the table form the last group. These have three output phases switched simultaneously onto the same input phase resulting in zero line-to-line voltages and are called zero *voltage vectors*. When a three-phase load is connected to the converter output terminals, a three-phase output current is drawn from the power source. The input currents are equivalent to the instantaneous output currents; thus, all input current vectors corresponding to the 27 output voltage vectors are listed in Appendix A.

A *synchronously rotating vector* (Group III) consists of six combinations having each of the three output phases connected to a different input phase. Each of them generates a three-phase output voltage having magnitude and frequency equivalent to those of the input voltages (V_i *and* ω_i) but with a phase sequence altered from that of the input voltages. As the input frequency is not related to the output frequency, the SVM method does not use the group III vectors to synthesize the reference voltage vector that rotates at a frequency, ω_o.

A complete cycle of a three phase sinusoidal voltage waveform can be divided into six sextants as shown in Figure 2.5. At each transition point from one sextant to another the magnitude of one phase voltage is zero while the other two have the same amplitude but an opposite polarity.

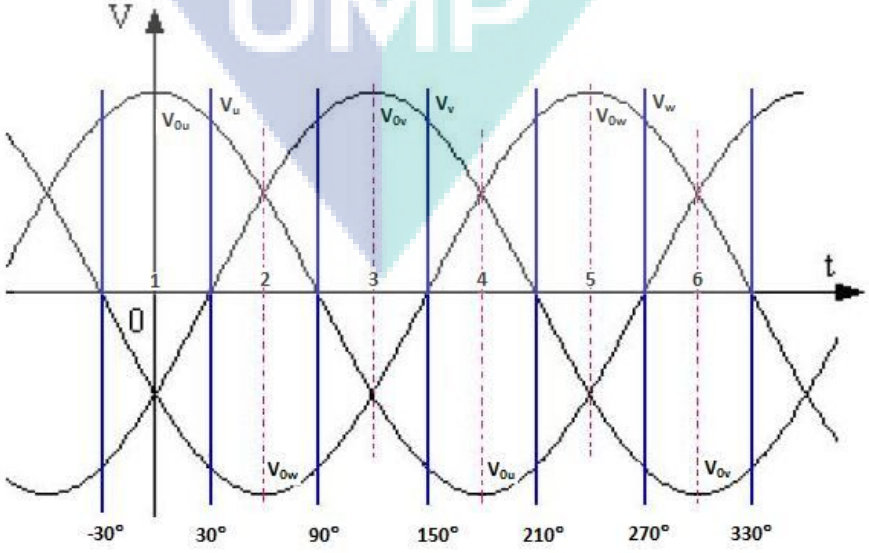


Figure 2.5: Six intervals of switching cycles

The phase angles of these points are fixed. Applying this rule to the 18 stationary voltage vectors in Appendix A, their phase angles are determined by the converter output voltages $V_u, V_v \; and \; V_w$. The first six all giving zeroes V_v, may locate either at the transition points between sextants 1 and 2 ($\omega_o t \; = 30°$) or that between sextants 4 and 5 ($\omega_o t \; = 210°$), depending upon the polarity of V_u and V_w. From the waveform diagram given in Figure 3.1 the three having positive V_u and negative V_w are at the end of sextant 1 ($\omega_o t \; = 30°$); conversely, the other three are at the end of sextant 4 ($\omega_o t \; = 210°$). The magnitudes of V_u and V_w are determined by the switch positions of the converter and can correspond to any of the input voltages, $V_a, V_b \; and \; V_c$. Similarly, vectors in the second set generating zero V_w and non-zero $V_u \; and \; V_v$ are at the end of either sextant 3 ($\omega_o t \; = 150°$) or 6 ($\omega_o t \; = 330°$). The three having positive V_v and negative V_u are for the former sextant, the other three are for the latter. The final set is for sextants 2 ($\omega_o t \; = 90°$) and 5 ($\omega_o t \; = 270°$).

Projecting the stationary voltage and current vectors onto the dq plane, the voltage hexagon obtained is shown in Figure 2.6. It should be noted that this voltage vector diagram can also be obtained by considering the magnitudes and phases of the output voltage vectors associated with the switch combinations given in Appendix A.

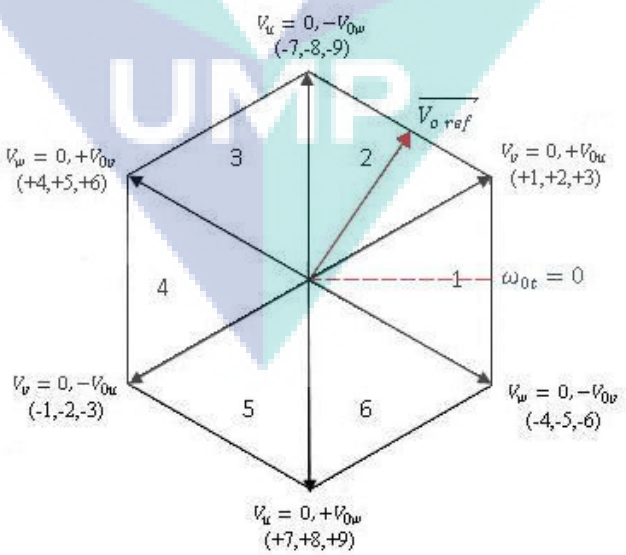


Figure 2.6: Output voltage vector diagram

The same principle can be applied to the corresponding 18 input current vectors, leading to the current hexagon depicted in Figure 2.7. Both the output voltage and input current vector diagrams are valid for a certain period of time since the actual magnitudes of these vectors depend on the instantaneous values of the input voltages and output currents.

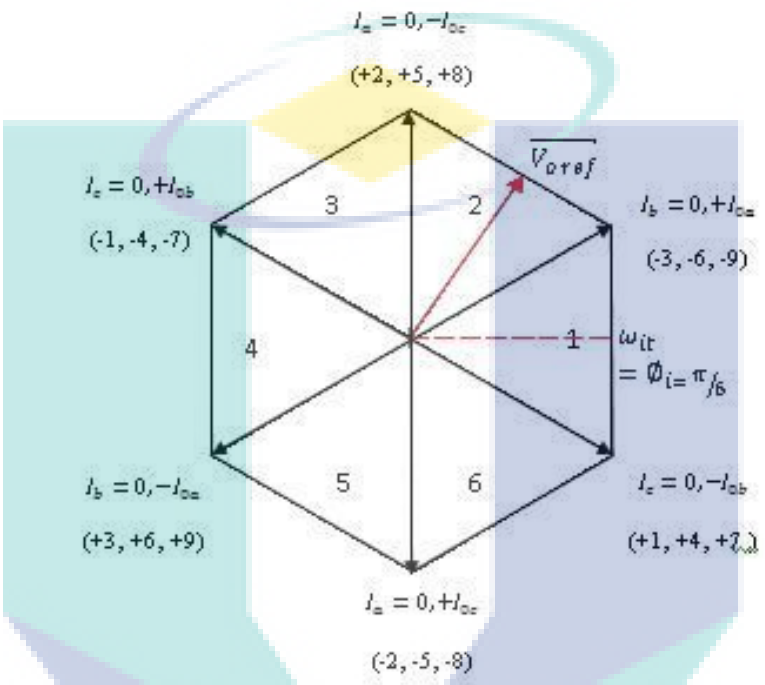


Figure 2.7: Input current vector diagram

2.3.1 Selection of Stationary Vectors and Duty Cycle

Implementation of the SVM method involves two main procedures; switching vector selection and vector on-time calculation. Having arranged the available switch combinations for matrix converter control, the SVM method is designed to choose appropriately four out of 18 switch combinations from the second group at any time instant. The selection process follows three distinct criteria, namely, that at the instant of sampling, the chosen switch combinations must simultaneously result in:

- The stationary output voltage vectors being adjacent to the reference voltage vector in order to enable the adequate output voltage synthesis.
- The input current vectors being adjacent to the reference current vector in order that the phase angle between the input line voltage and phase current, and hence the input power factor, being the desired value.
- The stationary voltage vectors having the magnitudes corresponding to the maximum available line input voltages.

To satisfy the first condition above, consider the reference voltage vector, $\vec{V}_{o_{ref}}$ that lies in one of the six sectors at any particular time instant. One of the line voltages in this corresponding sector is bound to be either most positive or most negative, hence being denoted as the peak line. The vectors selected to synthesis the reference voltage vector should be those that make the voltage on the peak line non-zero. This can be illustrated using the input line voltage waveform in Figure 2.8 (a) when the reference voltage vector, $\vec{V}_{o_{ref}}$ and reference current vector, $\vec{I}_{i_{ref}}$ lie in sector 1. The positive switch status is chosen to illustrate the actual use to select the negative when the switch state.

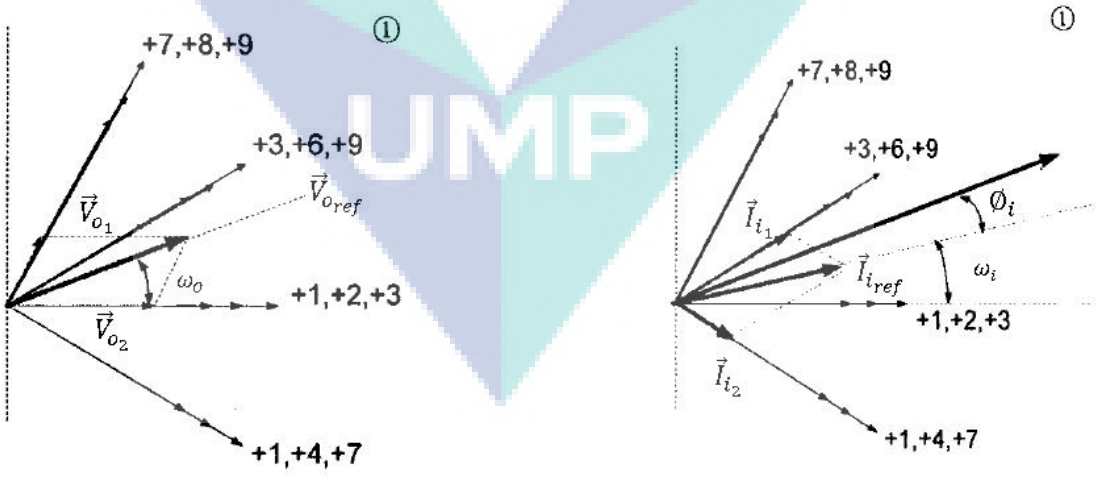


Figure 2.8: Vector diagrams: (a) output sector 1 and (b) input sector 1

$\vec{V}_{o_{ref}}$ can be decomposed into $\vec{V}_{o_1}$ and $\vec{V}_{o_2}$ and the synthesis of $\vec{V}_{o_1}$ lead to the selector switch state of +7, +9. Meanwhile, the synthesis of $\vec{V}_{o_2}$ resulting in the selector

switch state of +1, +3 corresponding to the voltage vector. The selected switch synthesis of $\vec{I}_{i_{ref}}$ is similar to the $\vec{V}_{o_{ref}}$. Extended to any sector, this method can be selected according to the four switch states. $\emptyset_i$ must be kept at 30° for unity input power factor, resulting in the zero phase shift angle between the input phase voltage and current.

The output voltage and input current sector switch combination table for the SVM is shown in Table 2.1. S_u is the output voltage sector and S_i is the input current sector. For the current in the first quadrant, the switch state of +l, +3 and +7, +9 of the voltage vector direction is inconsistent. The synthesis of the current direction will change, thus the new equation is developed to meet the requirements of uniformity, using the same directional vector, $A.jB = 0$.

Table 2 1: The output voltage and input current sector switch combination

			Voltage sector, S_u					
			1	**2**	**3**	**4**	**5**	**6**
Current sector, S_i	**1**	**A**	-3	+9	-6	+3	-9	+6
		B	+1	-7	+4	-1	+7	-4
		C	+9	-6	+3	-9	+6	-3
		D	-7	+4	-1	+7	-4	+1
	2	**A**	+2	-8	+5	-2	+8	-5
		B	-3	+9	-6	+3	-9	+6
		C	-8	+5	-2	+8	-5	+2
		D	+9	-6	+3	-9	+6	-3
	3	**A**	-1	+7	-4	+1	-7	+4
		B	+2	-8	+5	-2	+8	-5
		C	+7	-4	+1	-7	+4	-1
		D	-8	+5	-2	+8	-5	+2
	4	**A**	+3	-9	+6	-3	+9	-6
		B	-1	+7	-4	+1	-7	+4
		C	-9	+6	-3	+9	-6	+3
		D	+7	-4	+1	-7	+4	-1

	5	**A**	-2	+8	-5	+2	-8	+5
		B	+3	-9	+6	-3	+9	-6
		C	+8	-5	+2	-8	+5	-2
		D	-9	+6	-3	+9	-6	+3
	6	**A**	+1	-7	+4	-1	+7	-4
		B	-2	+8	-5	+2	-8	+5
		C	-7	+4	-1	+7	-4	+1
		D	+8	-5	+2	-8	+5	-2

The results lead to the differential equations of the duty cycle because the existence of the positive and negative selection switching state. Only the positive part is considered, thus some tuning should be done in the actual calculation. For example, in the first quadrant, d_A, d_D are negative and d_B, d_C are positive; the selected switching state of -3, + l, +9 and -7 should be adjusted. It should be noted that the four duty cycle must not be greater than 1. Because of this constraint, the existence of the zero vector, d_0 is considered in order to complete the entire cycle:

Various algorithms of SVM output signal or the waveform for the switches were proposed as shown in Figure 2.9. Several aspects need to be considered especially for ease of implementation and signal performance such as total harmonic distortion (THD) and switching losses. Therefore, different types of algorithms contribute the distinctive level of performance, and each algorithm is suitable for different operating condition. There are several switching rules need to be followed, which are:

- Trajectory of reference voltage vector, $\vec{V}_{o_{ref}}$ should be circular in shape
- Only one switching per state transition
- Not more than three switching in a sampling period, T_S
- The final state within a sampling period must be the initial state of the next sampling period

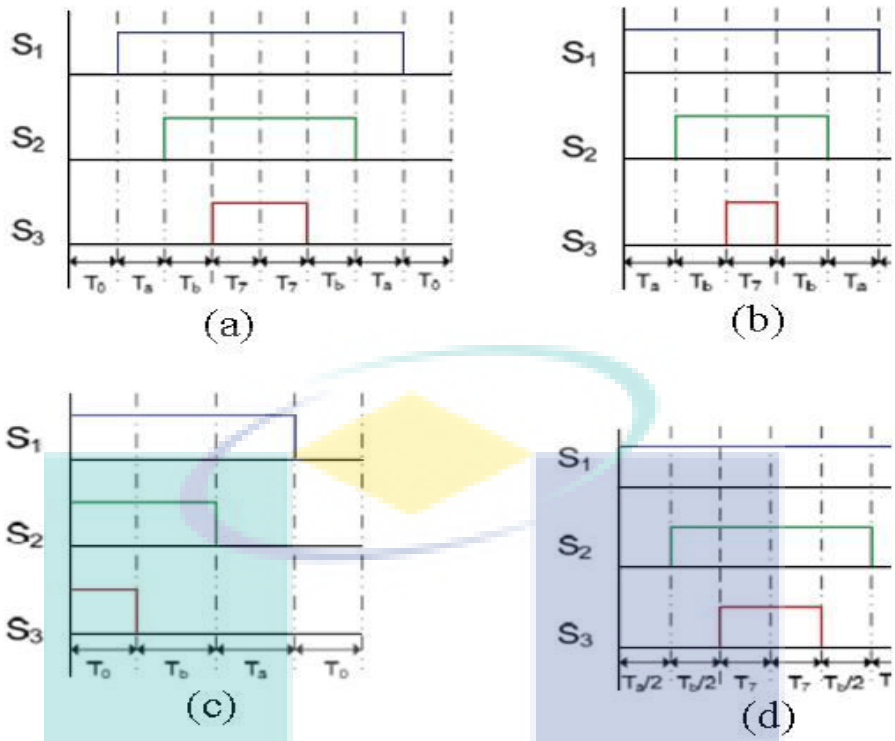


Figure 2.9: Algorithm of output signals based on sector; a) Symmetrical sequence b) Alternating sequence c) Left aligned sequence d) Bus clamped sequence

These rules aid in limiting the number of switching actions that would lead towards reduction in switching losses. Besides, symmetry property could be maintained in waveforms at a three-phase MC to achieve lower THD. The Symmetrical SVM has the lowest THD among the four types of the algorithm. SSVM utilizes all the three zero configurations in each cycle period with equal duty cycles. Concerning the particular case of the output voltage vector lying in sextant 1 and input current in sextant 1; the switching configurations selected are, in general 0_a, 0_b, 0_c, -7, +9, +1, -3 as shown in Figure 2.10. The use of three zero configurations leads to 12 switching commutations in each cycle period.

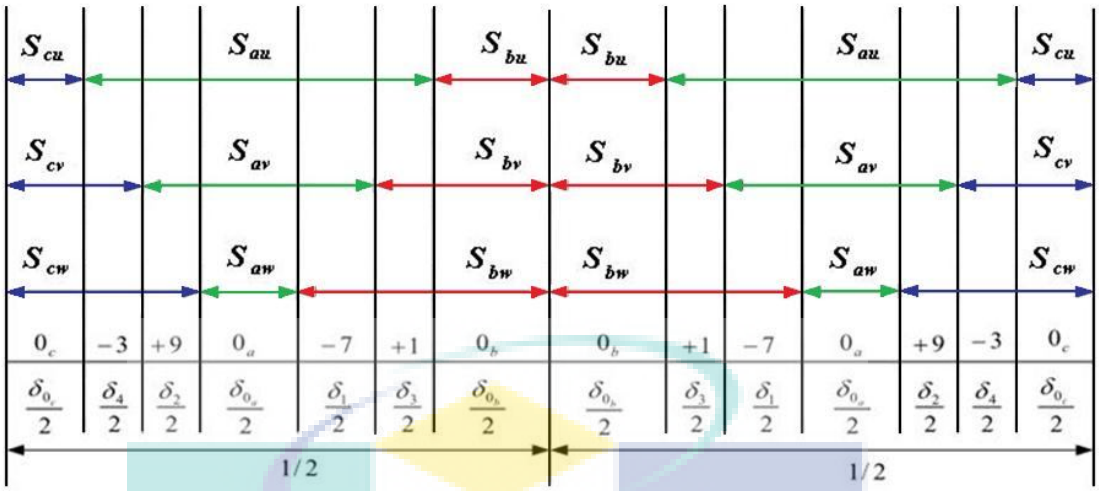


Figure 2.10: Double side switching pattern in a sampling period, T_s

2.4 MATRIX CONVERTER ISSUES

In all MC topologies, some basic operational limitations exist. Due to the voltage source type input i.e. supplies filter capacitor, load must be resistive or inductive. If the path of the inductive load current is cut abruptly, the high load voltage spike may arise. Thus, the load current path must always be ensured because purely resistive circuits do not exist in practice. On the other hand, input phases should never be short-circuited to avoid input current spikes. In the MC, every output phase must always be connected to a single input phase.

2.4.1 Overvoltage Protections

Likewise any other static converter, the MC needs to be protected against the over-voltages and the over-currents that might be destructive for its semiconductor devices. An effective and robust protection scheme plays an important role in the implementation of a stable and reliable power converter. The protection circuit which consists of input and output diode bridges, an electrolytic capacitor, and its charge and discharge circuit has been proposed which has a large volume. It also constrains the lifetime of the system, and the discharge circuit by a DC chopper increases the number of parts (Klumpner and Blaabjerg 2002; Klumpner et al. 2002).

On the other hand, a varistor protection and a suppressor diode protection were proposed which are very useful for a small capacity system, but unsuitable for a large-capacity system (Mahlein et al. 2002; You and Rahman 2009; Pfeifer and Schroder 2010). The strategy offers an additional possibility to remove the needed varistors.

The protection strategy with excellent overvoltage protection allows the removal of the large and expensive diode clamp. In addition, a varistor with unusual ratings is needed to be applied to the MC. Itoh et al. (2005) proposed a protection circuit which consists of a small capacitor in a dynamic clamp circuit using an IGBT and a resistor. The clamp circuit shown in Figure 2.11 does not need a drive and control circuit for the IGBT. Wang et al. (2005) proposed a shutdown strategy for MC under the normal or fault conditions. It provides a controlled freewheeling path for the load currents. Using the proposed strategy, the motor currents can be reduced to zero as soon as possible, while without causing over voltages.

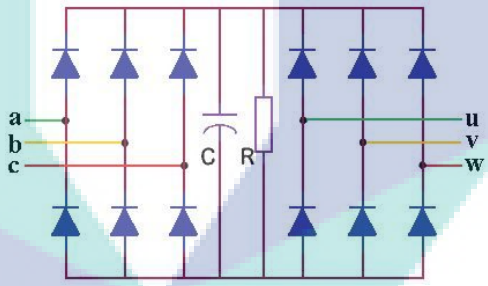


Figure 2.11: Clamping circuit

Even one of the switches is at fault and can't be used; the method is still useful. In order to avoid unexpected over-voltages under a switch open-circuit fault condition, a small-capacity clamping circuit is necessary. Different from the usual clamping circuit, a small capacitor is competent here, instead of a large one.

2.4.2 Switch Commutations

Overcoming the undeniable greater realization and control complexity, the anti-parallel arrangement of two unidirectional active devices with a series diode has been established in the 1990s as the most used bidirectional switch configurations

(Svensson and Alaküla 1991; Nielsen 1996; Klumpner et al. 2000.; Alesina and Venturini 2002; Beasant et al. 2002; Empringham et al. 2002; Kwon et al. 2002; Wheeler and Grant 2002; Ziegler and Hoffman 2002). This has been mainly due to the implementation of several commutation strategies using the bidirectional switch, which provides the capability to selectively enable the conduction of the negative and positive current polarity, allow to carry out safe load current commutation and eliminate the need of any snubber network. Hereinafter, the bidirectional switches will be considered in the anti-parallel arrangement of Figure 2.12.

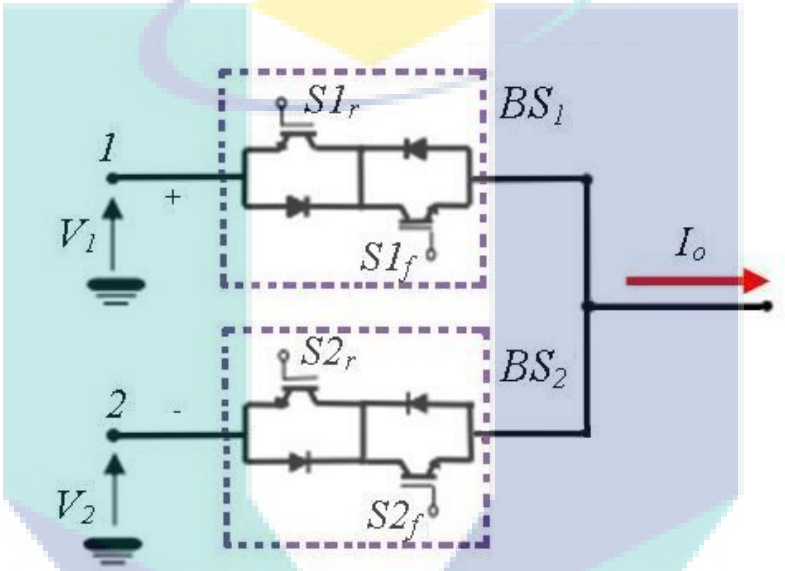


Figure 2.12: General commutation circuit of two bidirectional switches

Figure 2.13 shows the commutation steps in the three-phase to three-phase MC. The subscripts *f* and *r* in the IGBT stand for forward and reverse respectively, and it refers to the output current flow direction, which is assumed to be forward or positive when it is from the input to the output.

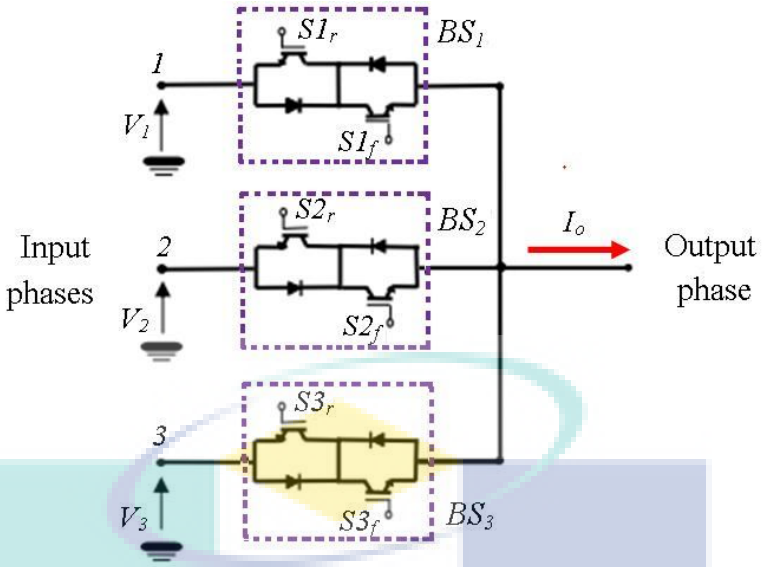


Figure 2.13: Three-phase input to single-phase output basic scheme

When the output phase has to be commutated from one input phase to another, two rules must be respected by any commutation strategy:

- The commutation does not have to cause a short circuit between the two input pulses, because the consequent high circulating current might destroy the switches.
- The commutation does not have to cause an interruption of the output current because the consequent overvoltage might likely destroy the switches.

To fulfil the requirements, some knowledge of the commutation conditions is mandatory. In order to carry out a safe commutation, the voltage between the involved bidirectional switches or the output current must be measured. The information is necessary in order to determine the proper sequence of the devices switching state combinations that do not lead to the hazard either of a short circuit or of an over voltage and provides the safe commutation of the output current. This is the common operating principle of all the commutation steps that have been proposed in the literature.

E. Output Current Sign Based Commutation

i) Four-step Commutation

This step was initially proposed in Burany (1989). It has a general validity, in a sense that it does not depend on the MC control algorithm employed. The simplified commutation circuit is shown in Figure 2.12. The step assumes that when the output phase is connected to an input phase, both the IGBTs of the bidirectional switch, BS_1 for instance, have to be turned on. Due to the finite turn-off and turn-on time of the IGBTs as well as the different propagation time delay of their gating signals, when the commutation of the output phase between the two input lines is required it is impossible to simultaneously switching off BS_1 and switching on BS_2.

For instance, assuming that $V_1 > V_2$, if the device $S2_r$, because of the aforementioned time delays, turn-on before the device $S1_f$ turn-off, a short circuit current starts to flow between the two input phases. In a dual way, assuming that $I_o > 0$, if the device $S1_f$ turns off before the device $S2_f$ turns on, the output current is interrupted, and a voltage spike is induced on the opened switches. Solving the problem consists in a careful control of the switching instants and in performing the commutation using only non-hazardous switch state combinations (Burany 2002). Table 2.2 shows a group of non-hazardous combinations, accordingly to the output current sign.

Table 2 2: Non-hazardous combinations of device state

State	$S1_f$	$S1_r$	$S2_f$	$S2_r$	Sign I_o
1	1	1	0	0	+ -
2	0	0	1	1	+ -
3	1	0	0	0	+
4	0	1	0	0	-
5	0	0	1	0	+
6	0	0	0	1	-
7	1	0	1	0	+
8	0	1	0	1	-

The ON state of a device is indicated by 1 and the OFF state by 0. It has to be noted that the switch states 1 and 2, are unconditional states, since it may exist independently of the current sign. However, switch states 3 to 8 are conditional states, since it is legal until the current sign is the one dictated by the most right hand-side column. Now, a commutation process always starts from and terminates with an unconditional state. This transition cannot be made directly in one step, but it has to be made through a sequence of several conditional states. In the case of 1 to 2, commutation is required and the output current I_o is positive. The switching state sequence to perform consists of the following four steps:

- Turning off $S1_r$;
- Turning on $S2_f$;
- Turning off $S1_f$;
- Turning on $S2_r$;

Accordingly, the sign of the output current that must be measured, in general:

- Turning off the IGBT which is not conducting the output current with the off-going bidirectional switch, BS_1 in the case;
- Turning on the IGBT which will conduct the output current within the on-coming bidirectional switch, BS_2 in the case;
- Turning off the IGBT which is conducting the output current within the off-going bidirectional switch;
- Turning on the IGBT which will not conduct the output current within the on-coming bidirectional switch.

In the same way, if the output current I_o is negative, the switching state sequence to follow is:

- Turning off $S1_f$;
- Turning on $S2_r$;
- Turning off $S1_r$;
- Turning on $S2_f$;

Symmetrical switching state sequences have to be used when the output current has to be commutated from BS_2 to BS_1. In order to ensure that the actual sequence of the IGBT gating signals, a short time delay should be inserted between consecutive steps. The time delay has to be set to a value higher than the maximum propagation time delay difference of the IGBT gating signals. Figure 2.14 shows the four-step switching diagram for two bidirectional switches and the output current commutation instant is highlighted. The numeration of the steps refers to a commutation from BS_1 to BS_2. It has to be noted that the output current commutation always takes place after step 2 or 3, depending on the polarity of the voltage across the two switches. In an unconditional state, whenever the output current is dictated to reverse by the source and the load, it can do it automatically.

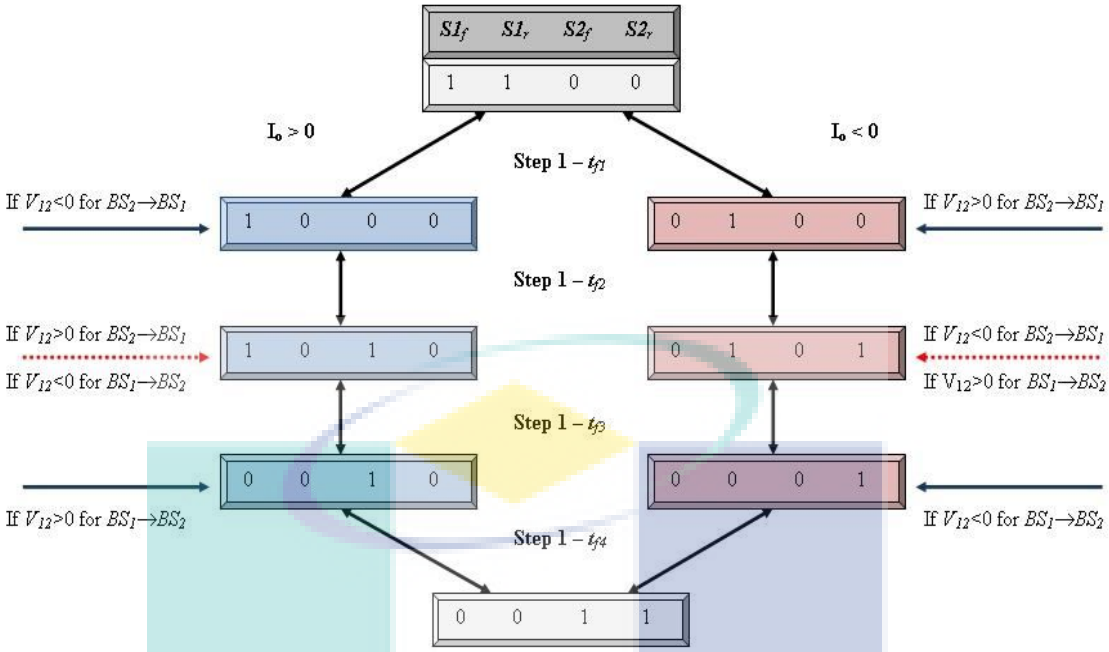


Figure 2.14: Four-step switching diagram for two bidirectional switches

From the switching diagram in Figure 2.14 and Figure 2.15, it can also be noted that during a commutation sequence, it is impossible for the output current to change the sign. This is the main potential drawback of the strategy. However, becomes a minor problem when an output current sensor with good resolution is used, since breaking a current, even an inductive one, at the zero crossing does not cause significant over voltages.

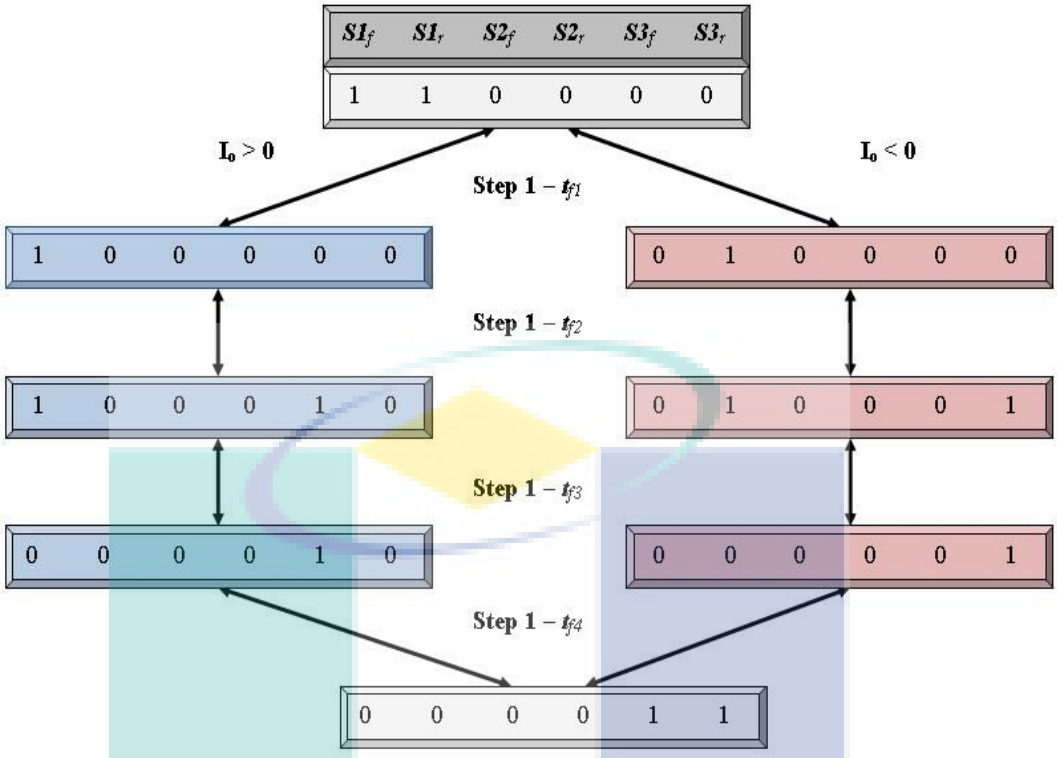


Figure 2.15: The bidirectional switches $BS_1 \leftrightarrow BS_3$ commutation

It is worth noting that the extension of this commutation step to a power converter with a higher number of input phases such as the MC, does not imply significant complications because the commutation always takes place between two bidirectional switches and the other are idle during the process. With reference to the topology shown in Figure 2.14 the switching diagram for the three bidirectional switches is given in Figure 2.15 and the list of the legal switch state combinations is shown in Table 2.3. The numeration of the steps refers to a commutation from BS_1 to BS_2.

Table 2 3: List of legal device state combinations for three inputs to one output direct AC-AC converter

State	$S1_f$	$S1_r$	$S2_f$	$S2_r$	$S3_f$	$S3_r$	Sign I_o
1	1	1	0	0	0	0	+ -
2	0	0	1	1	0	0	+ -
3	0	0	0	0	1	1	+ -
4	1	0	0	0	0	0	+
5	0	1	0	0	0	0	-
6	0	0	1	0	0	0	+
7	0	0	0	1	0	0	-
8	0	0	0	0	1	0	+
9	0	0	0	0	0	1	-
10	1	0	1	0	0	0	+
11	0	1	0	1	0	0	-
12	1	0	0	0	1	0	+
13	0	1	0	0	0	1	-
14	0	0	1	0	1	0	+
15	0	0	0	1	0	1	-

The four-step commutation strategy does not have significant hardware requirements apart from some sort of output current sign circuit measurement. It carries out the safe commutation of the output current and no snubber networks are needed. The time step delays can be set to the same constant value (Nielsen 1996; Klumpner et al. 2000.) or to different constant values (Schuster 2002; Nath et al. 2010) or variable values (Chang and Braun 2002).

As a matter of fact, it is important to point out that the sum of the time step delays settles the minimum duty cycle. The converter modulation control is able to apply to the output and hence it settles the width of the control discontinuity in the linear modulation region of the converter. In other words, the sum of the time step delays settles the theoretical minimum time for which an output phase can be connected to an input phase.

ii) Two-step Commutation

The commutation step was firstly proposed in Beasant et al. (2002) and Svensson and Alaküla (1991) and has been improved in (Empringham et al. 2000; Empringham et al. 2002). Concerning the commutation circuit of Figure 2.13, the key idea of this step is to keep the non-conducting IGBTs turned off during the commutation process to safely commutate the output current. In steady-state condition, the non-conducting IGBT switch is also turned off. When the output current is larger than a small predefined positive threshold value, $+I_{thres}$ only the positive current conducting IGBTs, $S1_f$ and $S2_f$ in this case, can be gated. When a commutation is required, the overlap method is used: the on-coming IGBT is gated before the off-going IGBT is turned off. Likewise, when the output current is lower than a predefined negative threshold value, $-I_{thres}$ only the negative current conducting IGBTs, $S1_r$ and $S2_r$, can be gated.

When the output current falls within the threshold band, $\pm I_{thres}$, which means that the current is close to zero and about to reverse, the non-conducting IGBT of the switched on the bidirectional switch is turned on in order to allow the current to reverse. As soon as the current has overcome the opposite signed threshold value, normal operations are resumed. Since during this commutation the output phase is connected to the same input phase and the current only commutates from one IGBT of the bidirectional switch to another, it is referred as "Inter-Switch Commutation" (Beasant et al. 2002).

With respect to the four-step, this strategy has the advantage of a reduced number of steps and consequently, a faster commutation process which improves the

output modulation control. However, the presence of the inter-switch commutation causes some drawbacks. First of all, if a phase commutation is required during an inter-switch commutation, a special procedure has to be followed, otherwise a short or open circuit may occur. A first possibility is to disable the phase commutation and hence the output modulation until the end of the inter-switch commutation (Svensson and Alaküla 1991). Obviously, the modulation of the output current and voltage are, to some extent, negatively affected by this solution, which might also give poor performance when the current measurement is not accurate, and the desired output current is small.

A second possibility is to use a dead time commutation if a phase commutation is required when the output current is within the threshold band(Wheeler 1993). The two devices on the off-going switch are turned off, and the devices in the on-coming switch are turned on a short time later. This is not an ideal solution because the output current is interrupted. Whether a snubber network may be needed or not depends on the output current threshold value. Figure 2.16 shows the switching diagram of the two-step commutation strategy related to the circuit of Figure 2.13. As for the four-step, the extension of the strategy to a three-phase MC is a straightforward task.

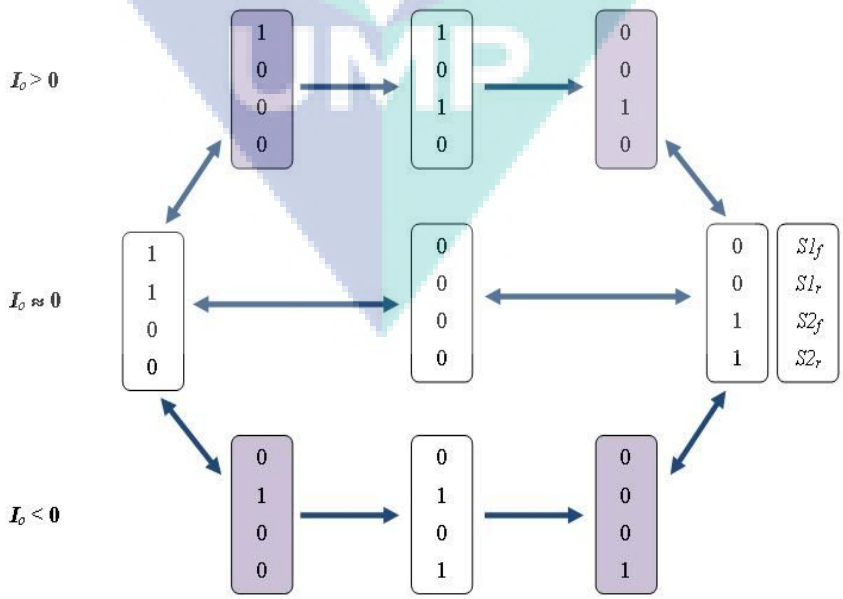


Figure 2.16: Two-step strategy for two bidirectional switches

The inter-switch commutation as defined before is eliminated in (Empringham et al. 2000; Empringham et al. 2002; Linhart et al. 2010). This is done by a significant improvement of the current sign detection and the implementation of an intelligent gate drive circuit. The current sign is detected monitoring the collector-emitter voltage of the IGBTs within the bidirectional switch, and this information is continuously provided to all the gate drivers of the IGBTs on the same output phase through a communication ring. In this way, the reliability of the current sign detection is increased, so when the output current has to reverse a simple dead time commutation is carried out. The dead time is short (≈ 250 ns) that it does not unduly distort the output current waveform (Empringham et al. 2000). The modified switching diagram with respect to Figure 2.16 is shown in Figure 2.17.

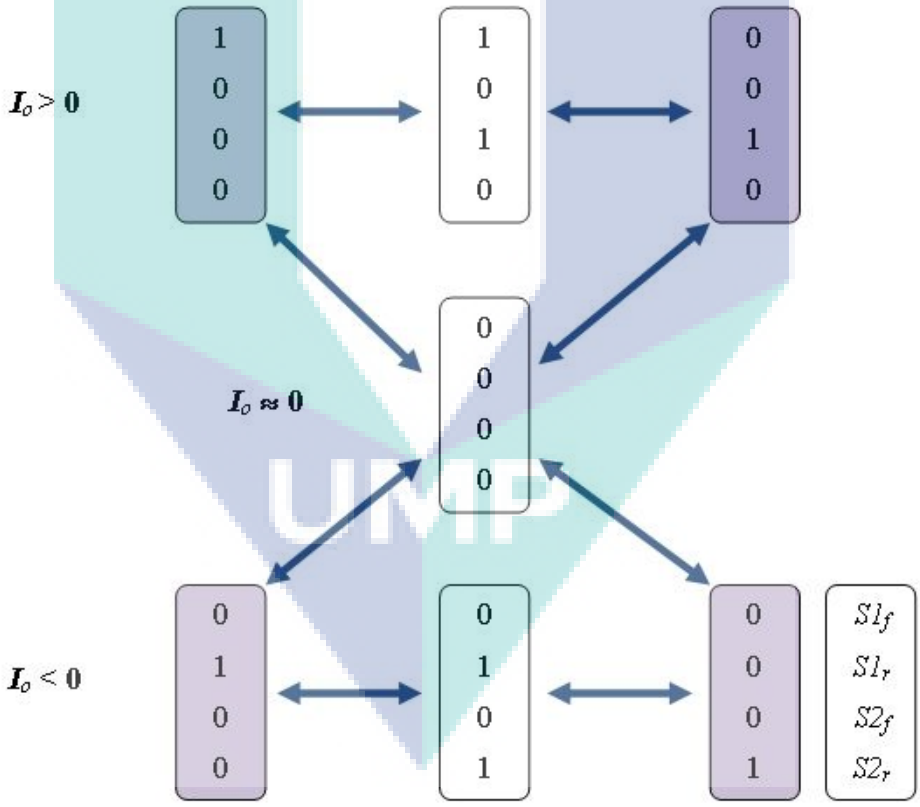


Figure 2.17: Two-step strategy without inter-switch commutation

The improved two-step commutation strategy performs fast and safe commutations, but it needs to monitor the collector-emitter voltages, which set some

constraints on the technological realization (i.e. the insulated power supplies are nine) and it is implemented on FPGA controllers.

F. Input Voltage Sign Based Commutation

i) Four-step Commutation

Burany (2002) proposed the commutation techniques relying on the input voltage measurement and effectively implemented in (Alesina and Venturini 2002; Mahlein et al. 2002; Ziegler and Hoffman 2002). Alesina and Venturini (2002) proposed the basic idea of the strategy referred as "staggered commutation" which is to reproduce the same operating conditions of a commutation process as in a traditional DC-link converter, where the dead time commutation method can be easily used because of the automatic timing action of the freewheeling diodes. To achieve, the input phase voltages have to be measured in order to detect the sign of the voltage across the two bidirectional switches involved in the commutation process. The strategy assumes that when the output phase has to stay connected to an input phase, both the active devices of the corresponding bidirectional switches are turned on. When a commutation of the output phase between two input lines is required it is firstly determined whether the switch turning off is at lower or higher voltage than that of the next switch turning on. This is needed to identify within the two commutating bidirectional switches the active devices which will operate as "freewheeling" devices.

In general, within the commutating bidirectional switches, the two freewheeling devices are those that allow the current to flow outward from the lower input phase voltage switch ($S2_f$ in Figure 2.18) and inward to the higher input phase voltage switch ($S1_r$).

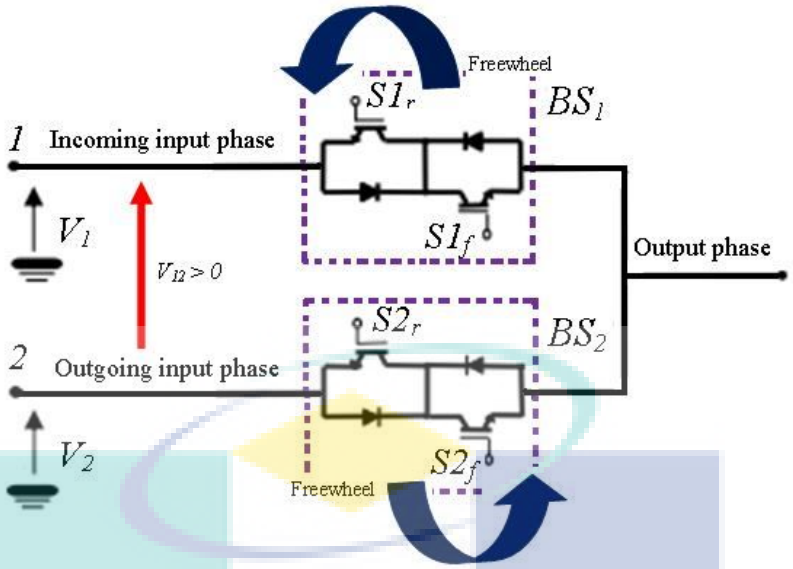


Figure 2.18: Staggered commutation

Once the freewheeling devices have been identified, the commutation strategy staggers in the following sequential steps:

- The freewheeling device of the incoming switch ($S1_r$ in Figure 2.18) is turned on;
- The non-freewheeling device of the outgoing switch ($S2_r$) is turned off;
- The non-freewheeling devices on the incoming switch ($S1_f$) are turned on;
- The freewheeling device of the outgoing switch ($S2_f$) is turned off.

In order to guarantee the above desired four-step switching sequence, a short time delay has to be inserted between the steps. With reference to the commutation circuit shown in Figure 2.18, the switching diagram of the strategy is shown in Figure 2.19.

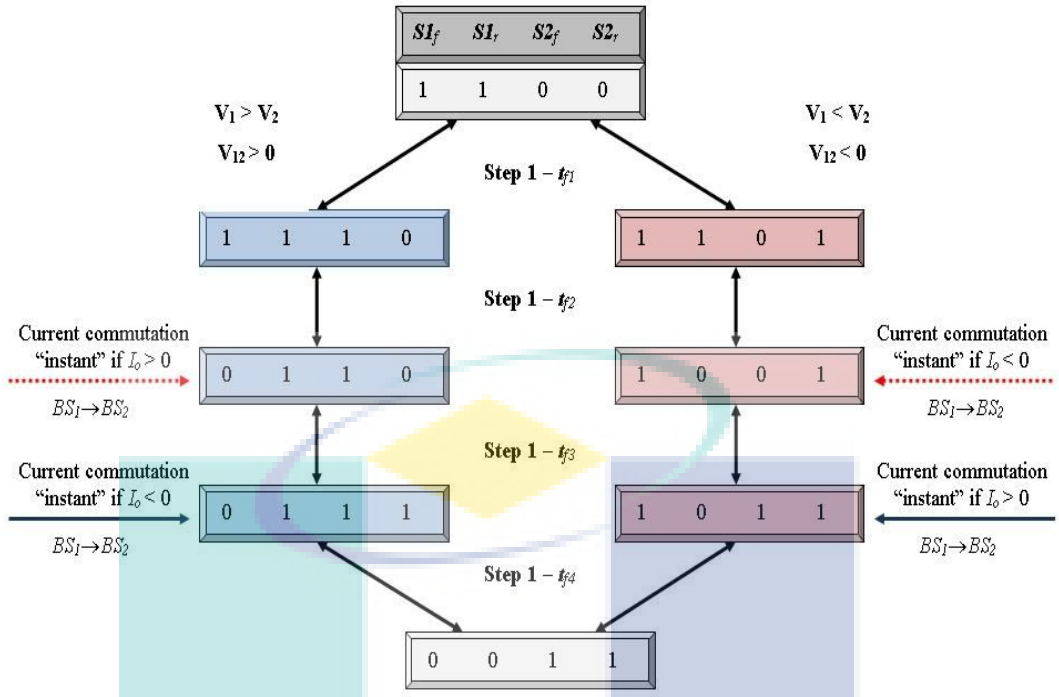


Figure 2.19: Four-step voltage-based commutation strategy

The relevant list of legal combinations of devices state is shown in Table 2.4. Using the commutation strategy it is possible to safely commutate the output current and additional snubber networks are not required.

Table 2 4: Legal combinations of devices state for the four step voltage based commutation strategy

State	$S1_f$	$S1_r$	$S2_f$	$S2_r$	Sign V_{12}
1	1	1	0	0	+ -
2	0	0	1	1	+ -
3	1	1	1	0	+
4	1	1	0	1	-
5	0	1	1	1	+
6	1	0	1	1	-

7	0	1	1	0	+
8	1	0	0	1	-

However, it has to be noted that the risk of a short circuit, is different from the open circuit, during a commutation process is not completely removed. As a matter of fact, if the measurement of the commutation voltage sign is incorrect, a short circuit path becomes available. Therefore, a reliable measurement of the input voltages is required by the commutation strategy to be effective. From a practical point of view, this constraint can affect either the MC output modulation strategy, by choosing a safe but non-optimal switching sequence, or the input filter parameter design, in order to reduce the ripple of the MC input voltages.

It has also to be pointed out that as for the current based four-step commutation strategy, the actual output current commutation instant during the switching sequence is varied depending on the output current sign. In this case, the current can commutate after the second or the third step. For an optimized modulation of the output quantities such variability has to be taken into account and compensated. As for the previous current based commutation strategies, the extension of this strategy to a power converter with a higher number of input phases does not imply significant problems because the commutation always takes place between two bidirectional switches, and the others are idle during the process.

ii) Two-step Commutation

Ziegler and Hoffman (2002) proposed a two-step commutation strategy known as the *METZI* commutation which is based on the input voltage measurement. It is based on the basic operating principle to provide a freewheeling path for both output current polarities at any time, either for steady or for transient device state combinations. It is specifically defined for a three-phase to three-phase MC and applies to the converter topology shown in Figure 2.19.

With respect to the four-step staggered commutation strategy, the number of steps required in the switching sequence is halved with a consequent positive effect on the modulation performance of the converter. Unfortunately, the reduction of the step's number is obtained at the expense of the commutation strategy simplicity. In fact, reducing the step's number will cause more devices to be switched on either in steady or transient states, from a minimum of two to a maximum of four. As a whole, the strategy consists of 30 different device state combinations (Ziegler and Hoffman 2000).

Since the switching sequence during a commutation process is defined accordingly to the commutation voltage sign, the reliability of the input line-to-line voltages zero-crossing point detection is an important issue even for the *METZI* strategy. The voltage sign detection circuit proposed in (Ziegler and Hoffman 2000) and patented in (Waltsgott et al. 1998) relies on the detection of the zero-crossing instant of the filtered and unfiltered line-to-line voltages. However, despite a very reliable voltage sign detection based commutation, the risk of a short circuit cannot be eliminated because the voltage difference can change sign during the commutation process. In order to completely remove the risk of a short circuit it is necessary to modify the switching sequence requested by the modulation algorithm.

In Figure 2.20, a fundamental period of the MC input line-to-neutral voltages are shown, and the regions where the detection of the line-to-line voltages sign becomes critical are highlighted. Assuming that the region marked as “uncritical” in Figure 2.20 is the switching sequence required by the main control algorithm to minimize the converter switching losses is $b \rightarrow c \rightarrow a$. In the region marked as “uncritical” this switching sequence can be carried out safely. A critical situation appears when the voltage V_b becomes nearly equal to V_c, if the sign detection of the line-to-line voltage V_{bc} is wrong or if the sign changes when the switching sequence is already in progress a freewheeling path becomes a short circuit path.

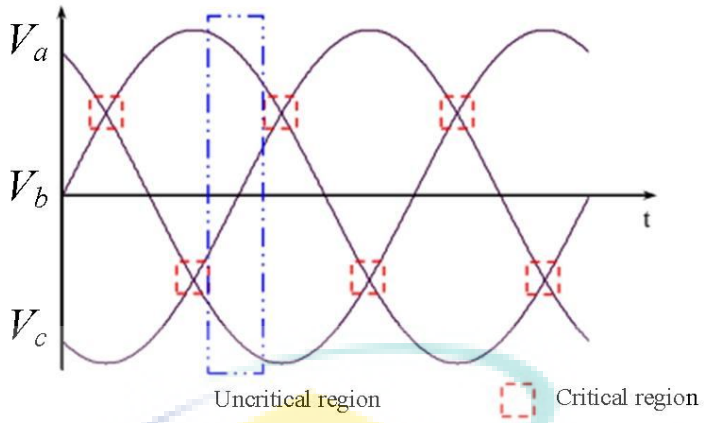


Figure 2.20: Critical commutation region strategies

There are several possibilities to manage commutations within a critical region (Waltsgott et al. 1998). The first solution is to interdict the critical phase commutation $b \rightarrow c$ till the voltages differ enough from each other. However, the connection time of the output phase with the input phases b and c would be unduly modified. Such variation may have little effect on the output voltage because the input voltages are nearly equal but would distort the input currents. The second solution proposed in (Ziegler and Hoffman 2000), is changing the switching sequence by adding the uncritical commutations. The critical phase commutation is carried out passing through the remaining third input line-to-neutral voltage. Concerning the previous example, the modified switching sequence would be $b \rightarrow a \rightarrow c \rightarrow a$. This solution is easy to be implemented in the commutation logic and requires only an information about the critical region, but it has the disadvantage of inserting additional commutations that increase the converter switching losses.

Mahlein et al. (2002) proposed a better solution with the basic idea is to reshuffle, within a critical region, the switching sequence in order to avoid any critical commutation. The solution still needs to detect the critical area, but no additional commutations are inserted. Concerning the previous example, the reshuffled safe switching sequence would be $b \rightarrow a \rightarrow c$. In this way the input-output modulation performances of the converter are not affected. The unique side effect of such a solution is an increase of the switching losses with respect to the optimized switching sequence. The amount of this extra loss depends on the width of the

critical region which depends on the disturbances existing on the AC mains, the power delivered to the load and the value of the input filter capacitance. It is worth noting that the previous proposed solutions for eliminating the short circuit risk inherent to commutation strategies based on the input voltage sign detection can be applied to the four-step staggered commutation strategy too.

It is also worth noting that in *METZI* commutation, as in the previous staggered commutation, the actual output current commutation instant during a two-step switching sequence is varied depending on the output current sign. As for the current based four-step commutation strategy, the time difference is equal to one-step delay.

2.5 DIRECT TORQUE CONTROL TEHNIQUE FOR MATRIX CONVERTER DRIVE INDUCTION MOTOR

The effects of torque ripple are particularly undesirable in some demanding motion control and machine tool applications. They lead to speed oscillations which cause deterioration in the performance. In addition, the torque ripple may excite resonances in the mechanical portion of the drive system, produce acoustic noise, and, in machine tool applications, leave visible patterns in high-precision machined surfaces.

Direct torque control is introduced during the mid-1980s, is another method of torque control, which was developed to achieve a high performance AC variable speed technology. It was first proposed in 1985 by Depenbrock, and then extended to a weak magnetic speed range in 1987 (Depenbrock 1987). Unlike vector control, DTC has its own characteristics; it is largely solved in the computational complexity of vector control, properties vulnerable to motor parameter changes and actual performance difficult to achieve the theoretical analysis of some major issues. The idea is that the motor and the inverter as a whole, the use of spatial analysis methods in the stator voltage vector coordinate system flux. The torque is calculated by tracking the magnetic chain of open-type PWM inverter off state. Therefore, there is no need to extract the curse of the stator current, simple control structure and facilitate the realization of all-

digital. The birth of DTC, take the new ideas of clear and concise control system architecture, excellent static and dynamic performance by the widespread concern and the rapid development.

First, in the use of a bang-bang control, the actual torque ripple within the upper and lower limits is not completely constant. Second, because of the flux calculated using the band integral part of the voltage model, initial points, accumulated error and the stator resistance changes are affected by the accuracy of the flux calculations. The impact of these two problems was obvious at low speeds, thus making the DTC speed range is limited.

Direct torque control method has becomes one of the high-performance control strategies for induction motor to provide a very fast torque and flux control (Lee et al. 2009). It is the direct control of torque and flux of an electrical motor by the selection through a look-up table, of the power converter voltage space vectors. The main advantage of DTC is its structure simplicity, since no coordinates transformations, current controllers and PWM are needed. Moreover, the controller does not depend on motor parameters. DTC is considered to be a simple and robust control scheme which achieves the quick and precise torque control response. For such advanced reasons, the combination of the advantages of the matrix converter with those of the DTC method is effectively possible (Chen et al. 2008).

However, some research is still being done to reduce the electromagnetic torque ripple, which is its main drawback that leads to the rising stator current distortion noise (Alesina and Venturini 2002). The following methods are applied to improve the effects of the ripple on the torque output: fuzzy logic controller, multilevel inverter, the modulation methods of the SVM (Casadei et al. 2000; Lascu et al. 2002; Buja and Kazmierkowski 2004).

Using the above methods always increases the complication of the system structure and burdens the workload of the DSP because of complicated calculations such as square root and trigonometric functions algorithm are involved. It is crucial to keep the short sampling period time in order to maintain the electromagnetic torque

ripple within an acceptable hysteresis band (Buja and Kazmierkowski 2004). It is difficult to implement DTC using common IC hardware. The DTC algorithm is usually implemented by serial calculations on a DSP board. However, as a predictive control scheme, the DTC has a steady-state control error produced by the time delay of the lengthy computations, which depends largely on the control algorithm and hardware performance. A typical DSP (TMS32010) execution time of the DTC algorithm for a VSI-fed induction motor is more than 250μs (Habetler et al. 2002).

Artificial Neural Network (ANN) has faster parallel calculation and simpler circuit structure, so it is superior to a DSP board in execution time and hardware structure. The execution time of neural devices is less than 0.5μs (analogue) or 0.8μs (digital) per neuron (Zaghloul et al. 1994). So, DTC of VSI fed induction motor based on ANN had been pointed out (Shi et al. 2002; Dung and Thuong 2004). Moreover, the designers must possess plentiful experiences on related theories. DTC based system of the electromagnetic torque regulator for the three-point hysteresis comparator is shown in Figure 2.21.

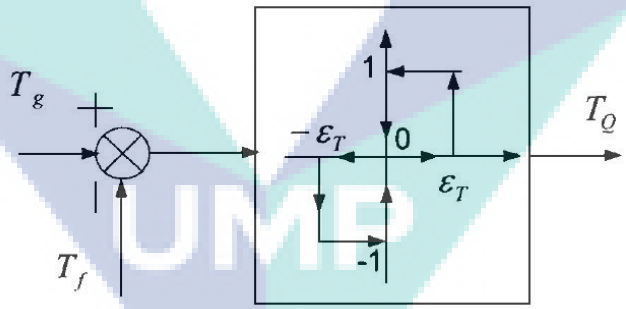


Figure 2.21: Schematic diagram of the three-torque regulator

In the detailed analysis of the MC fed induction motor DTC; it is necessary to review the VSI power induction motor DTC principles and methods. Voltage source inverter power asynchronous motor DTC calculation is estimated according to the stator flux and torque hysteresis and the stator flux sector. DTC control requires the preparation of a look-up table which selects the appropriate switch inverter switching state that the inverter output voltage space vector to the stator flux and torque regulation

(Tao 2007). DTC system of the stator flux regulator for the two-point hysteresis comparator is shown in Figure 2.22.

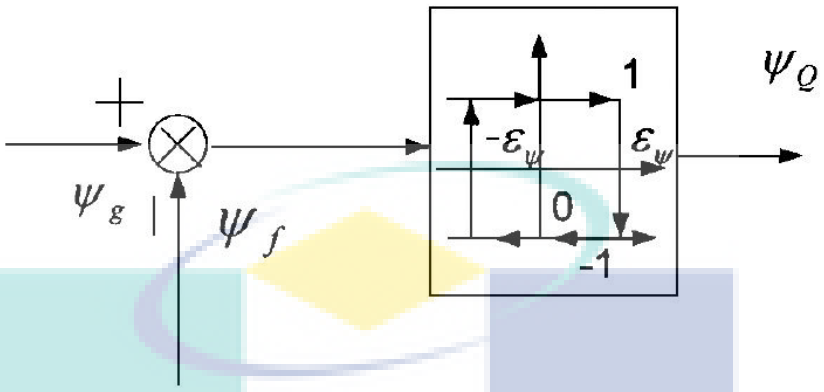


Figure 2.22: Flux regulator

Where ψ_g the desired value of the stator flux is, ψ_f is the observed value, ε_ψ is the tolerance, ψ_Q the flux regulator output. Electromagnetic torque for a given value of T_g, observed value of T_f, tolerance ε_T, the output of the torque regulator T_Q. Generally, by considering the flux and torque comparator's output and the stator flux sector the selection of the six non-zero inverter output vectors and two zero vectors were done in order to achieve the linkage and torque regulation (Jing and Fahai 2005).

2.6 PARTICLE SWARM OPTIMIZATION TECHNIQUE

Particle swarm optimization (PSO) is a population based stochastic optimization technique developed by Dr. Eberhart and Dr. Kennedy in 1995, inspired by social behavior of bird flocking or fish schooling. PSO shares many similarities with evolutionary computation techniques such as Genetic Algorithms (GA). The system is initialized with a population of random solutions and searches for optima by updating generations. However, unlike GA, PSO has no evolution operators such as crossover and mutation. In PSO, the potential solutions, called particles, fly through the problem space by following the current optimum particles.

Each particle keeps track of its coordinates in the problem space which are associated with the best solution (fitness) it has achieved so far. (The fitness value is

also stored.) This value is called *pbest*. Another "best" value that is tracked by the particle swarm optimizer is the best value, obtained so far by any particle in the neighbors of the particle. This location is called *lbest*. when a particle takes all the population as its topological neighbors, the best value is a global best and is called *gbest*.

The particle swarm optimization concept consists of, at each time step, changing the velocity of (accelerating) each particle toward its *pbest* and *lbest* locations (local version of PSO). Acceleration is weighted by a random term, with separate random numbers being generated for acceleration toward *pbest* and *lbest* locations.

In past several years, PSO has been successfully applied in many research and application areas. It is demonstrated that PSO gets better results in a faster, cheaper way compared with other methods. Another reason that PSO is attractive is that there are few parameters to adjust. One version, with slight variations, works well in a wide variety of applications. Particle swarm optimization has been used for approaches that can be used across a wide range of applications, as well as for specific applications focused on a specific requirement.

Thus, PSO has gained popularity in recent years. PSO development and its applications for power systems are presented in (Yoshida et al. 2001; Alves da Silva and Abrao 2002; Liu et al. 2007). Compared to other computational intelligence techniques, PSO has fewer parameters to tune. Since 1995, many researchers from different fields have attempted to improve the performance of the original PSO. Newer versions and the choices of proper values of the parameters to improve the performances of PSO are discussed in (Clerc and Kennedy 2002; Zhang et al. 2003; Kennedy 2006; Kennedy and Mendes 2006). The modifications of the PSO mainly consider the swarm size, the number of iterations, and the velocity to update the search direction and the steps. Both the performance and the execution time of PSO are improved in the modifications. In (Kwok et al. 2006), the authors presented a study on applying PSO to parameter identification of a physical system, where a comparison between PSO and GA was made to justify the choice of PSO.

CHAPTER 3

METHODOLOGY

The block diagram of the proposed system is shown in Figure 3.1. It consists of the RLC filter circuit, MC circuit, clamp circuit and control system. The MC circuit is built using the IGBT switching module. The SVM algorithm will be performed in the MC circuit that will trigger the IGBT switching. The DTC, the power factor calculation and the intelligent control will be done in the control circuit, and will be explained in the next section. The expressions relating the input and output of the three-phase MC were implemented by using *Matlab/Simulink*.

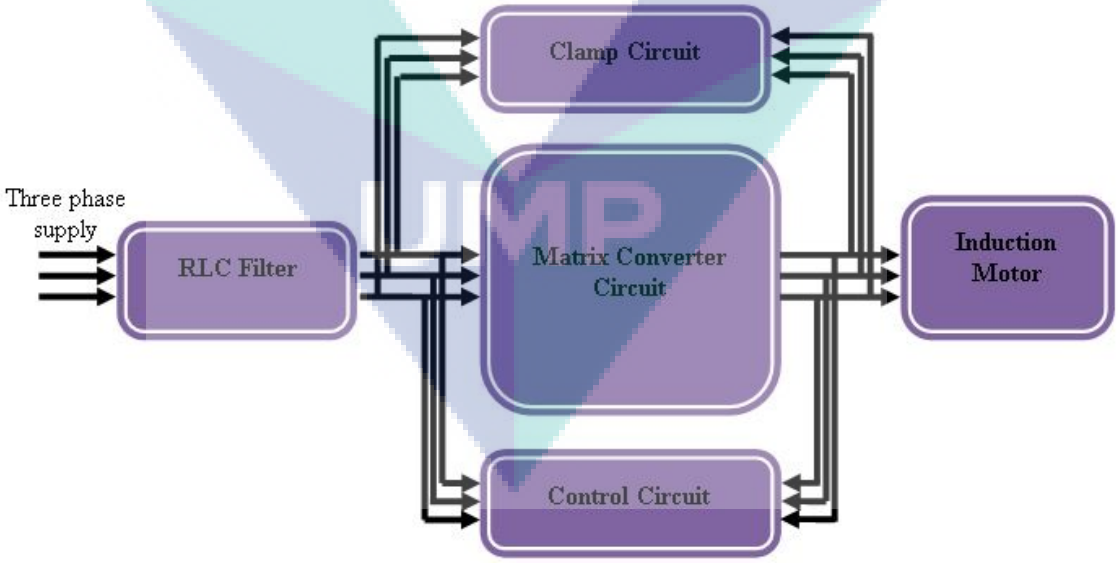


Figure 3.1: Block diagram of the proposed system

The main circuit construction of the three-phase MC is shown in Figure 3.2. It comprises of input *a*, *b* and *c*, connected to the output *u*, *v* and *w*.

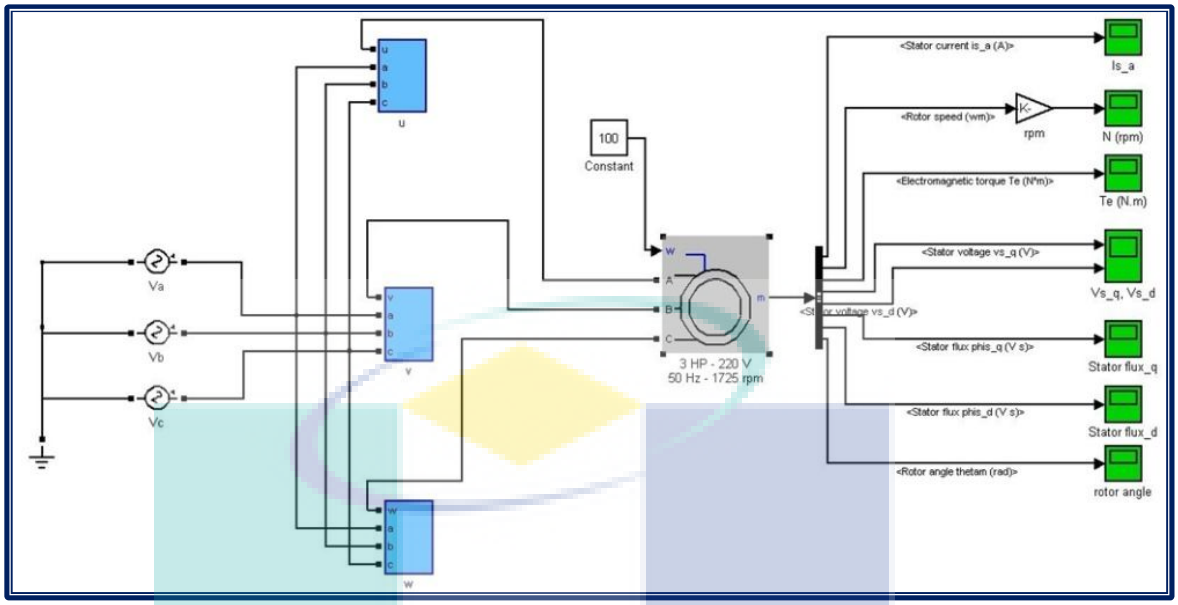


Figure 3.2: MC Circuit

The IGBTs circuit for each input-output phase is shown in Figure 3.3. The connection is made in common-collector. The gate terminal will be triggered by the IGBT driver.

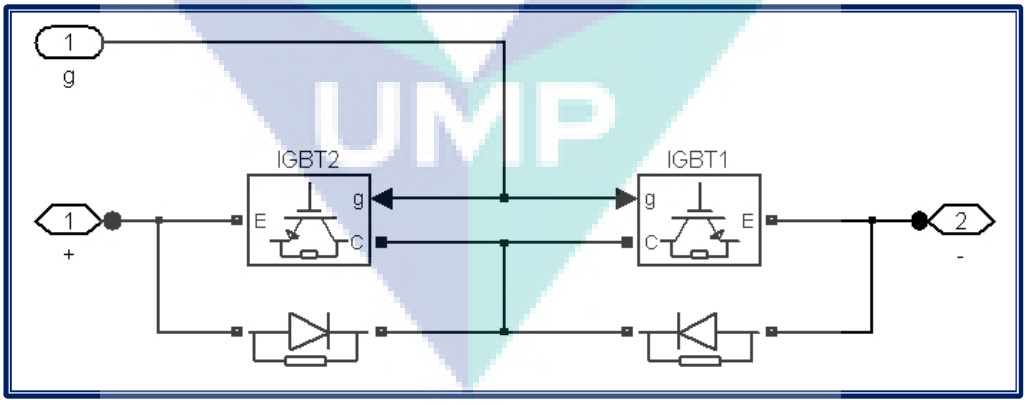


Figure 3.3: IGBT Circuit

The switch control signals for MC are shown in Figure 3.4 and the switching vector combinations are summarized in Appendix A.

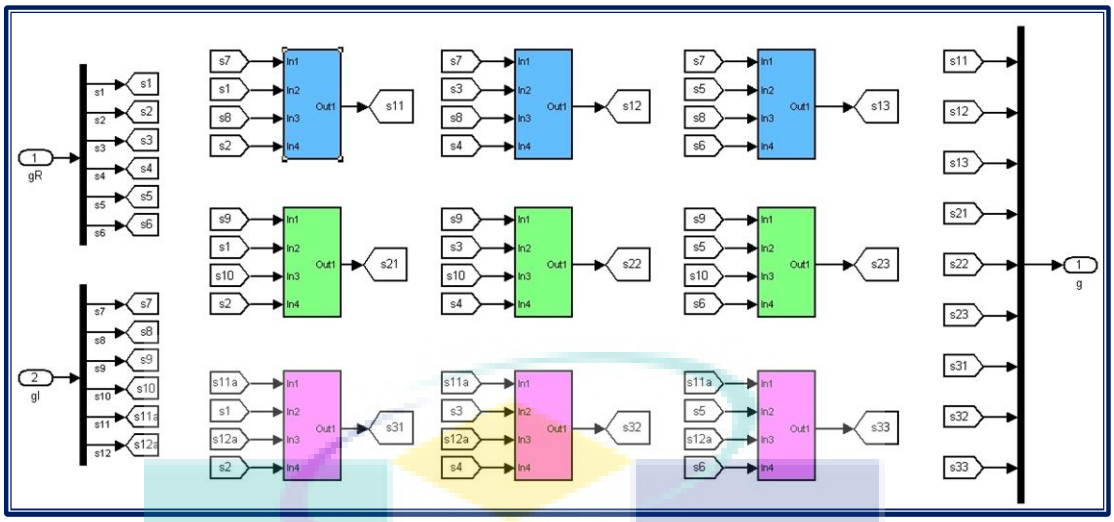


Figure 3.4: Matrix converter switching

The switching subsystem for MC in Figure 3.4 is shown in Figure 3.5.

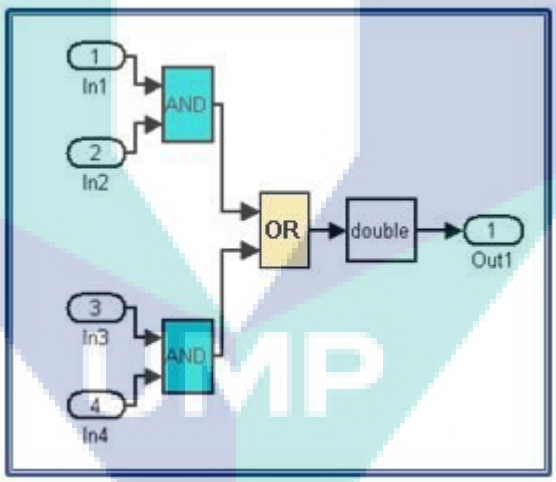


Figure 3.5: Matrix converter switching subsystem

3.1 MODELLING OF MATRIX CONVERTER SPACE VECTOR MODULATION CONTROL ALGORITHM

The indirect transfer function (ITF) approach is employed in the three-phase control MC. The transfer matrix is equal to the product of two matrices. This is equivalent to the operation of a voltage source rectifier (VSR) multiplying with the

operation of the voltage source inverter (VSI). Consider the VSR part of the circuit in Figure 3.6 as a standalone VSR loaded by a DC current generator, I_{dc}.

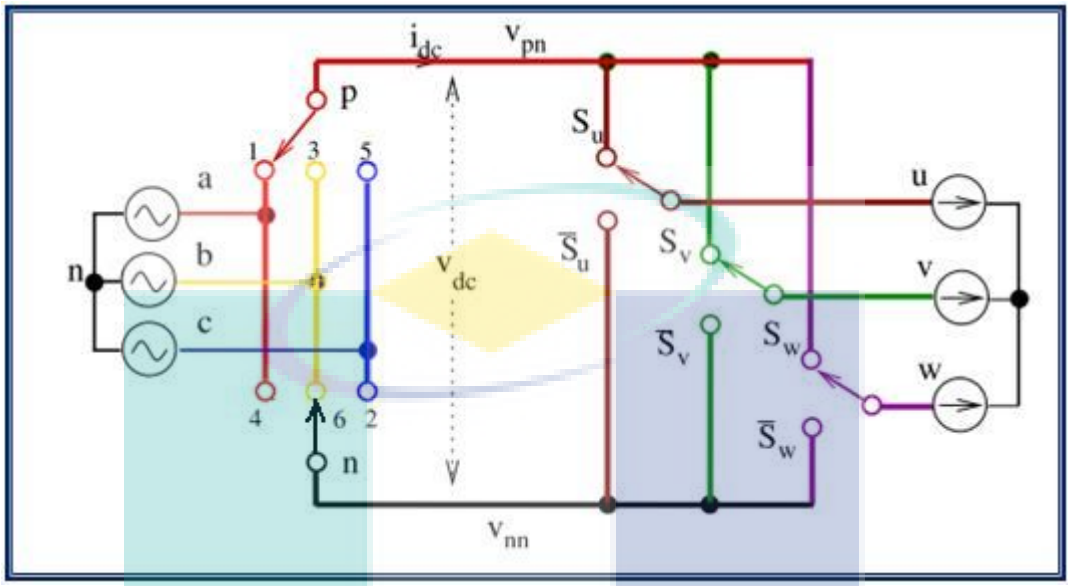


Figure 3.6: Emulation of VSR-VSI conversion

The construction of a physical model for the SVM controlled MC is shown in Figure 3.7. It comprises input modulator, output modulator, MC modulator and MC IGBTs switches. The input modulator is the modeling of rectification part, and the output modulator is the inversion part. The maximum VSI voltage gain is equal to unity; is shown in the output modulation index.

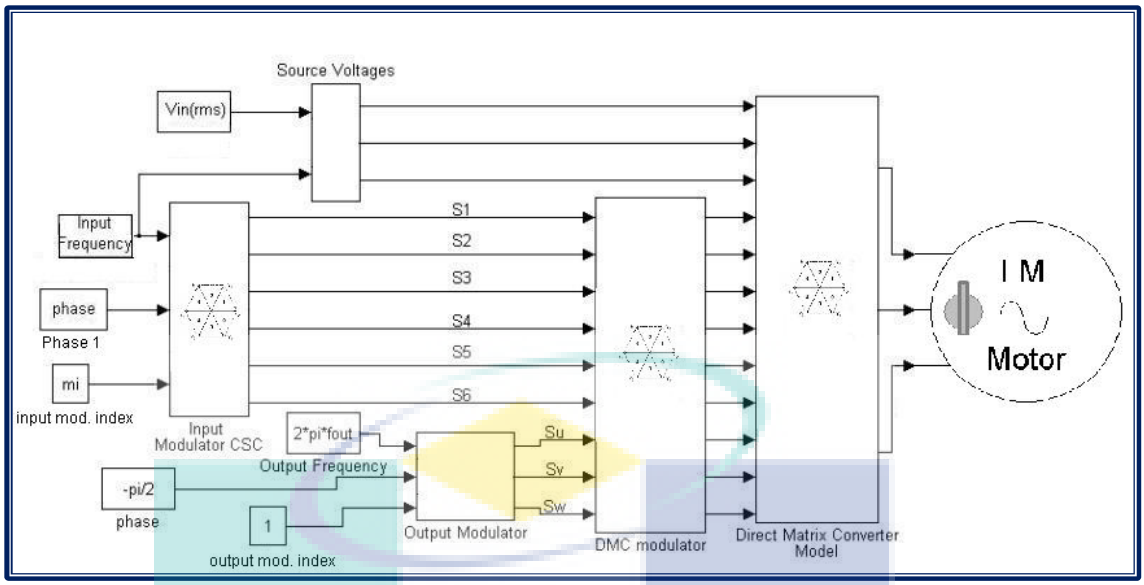


Figure 3.7: Block diagram of the mathematical model for the SVM-MC

3.1.1 Voltage Source Rectifier Space Vector Modulation

The Voltage Source Rectifier (VSR) input current vector diagram is shown in Figure 2.7 in the previous chapter. The duty cycles for VSR are calculated as

$$d_{\alpha i} = m_i \cdot \sin\left(\frac{\pi}{3} - \theta_i\right) \quad (3.1)$$

$$d_{\beta i} = m_i \cdot \sin\theta_i \quad (3.2)$$

$$d_{0i} = 1 - d_{\alpha i} - d_{\beta i} \quad (3.3)$$

Where m_i is given as

$$0 \leq m_i \leq 1 \quad (3.4)$$

For a switching cycle within the first sector as

$$\begin{bmatrix} \vec{I}_a \\ \vec{I}_b \\ \vec{I}_c \end{bmatrix} = \begin{bmatrix} d_{\alpha i} + d_{\beta i} \\ -d_{\alpha i} \\ -d_{\beta i} \end{bmatrix} . I_{dc}$$

$$= m_i . \begin{bmatrix} \cos\left(\theta_i - \frac{\pi}{6}\right) \\ -\sin\left(\frac{\pi}{3} - \theta_i\right) \\ -\sin(\theta_i) \end{bmatrix} . I_{dc} \quad (3.5)$$

$$\theta_i = (\omega_i t - \emptyset_i) + \frac{\pi}{6}, \ \frac{\pi}{6} \leq \omega_i t - \emptyset_i \leq -\frac{\pi}{6} \quad (3.6)$$

Substitute θ_i from Eq. (3.6) to Eq. (3.7). Thus, the transfer matrix of the VSR, $\vec{T}_{VSR}$ is defined as

$$\begin{bmatrix} \vec{I}_a \\ \vec{I}_b \\ \vec{I}_c \end{bmatrix} = m_i . \begin{bmatrix} \cos(\omega_i t - \emptyset_i) \\ \cos\left(\omega_i t - \emptyset_i - \frac{2\pi}{3}\right) \\ \cos\left(\omega_i t - \emptyset_i + \frac{2\pi}{3}\right) \end{bmatrix} . I_{dc} = \vec{T}_{VSR} . I_{dc} \quad (3.7)$$

The modulation index from Eq. (3.4) is replaced to Eq. (3.7) resulting in the desired input current phase. The VSR output voltage is determined as

$$\vec{V}_{pn} = \vec{T}_{VSR}^{T} . V_{iph}$$

$$= \frac{3}{2} . m_i . V_{im} . \cos \emptyset_i = constant \quad (3.8)$$

The modeling of the rectification stage (gR) is generated from Figure 3.8.

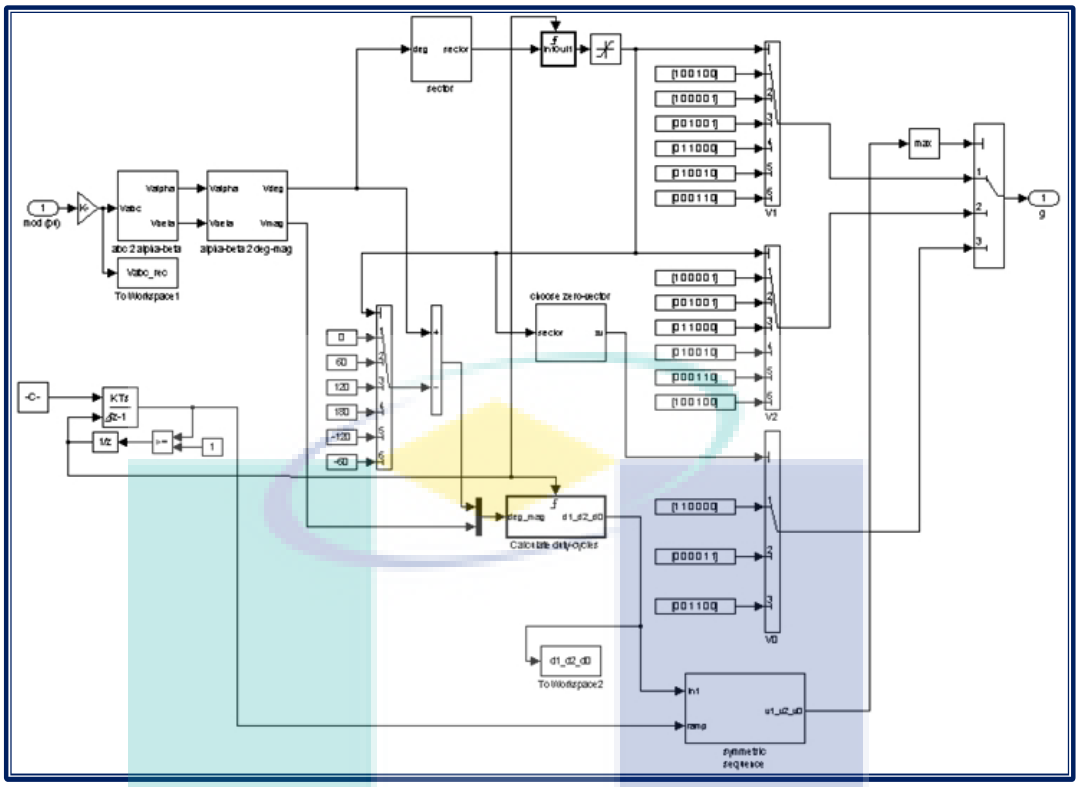


Figure 3.8: SVM rectification

The input phase voltages are changed to *dq* plane in the SVM rectification stage as shown in Figure 3.9.

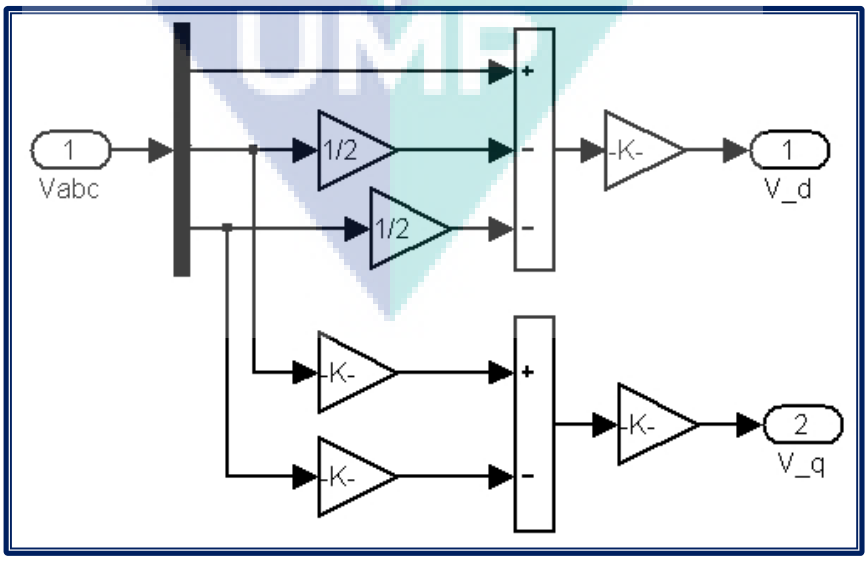


Figure 3.9: V_{abc} to V_{dq}

The value in *dq* plane is then changed to magnitude and angle as in Figure 3.10 and will be the input for sector identification shown in Figure 3.11.

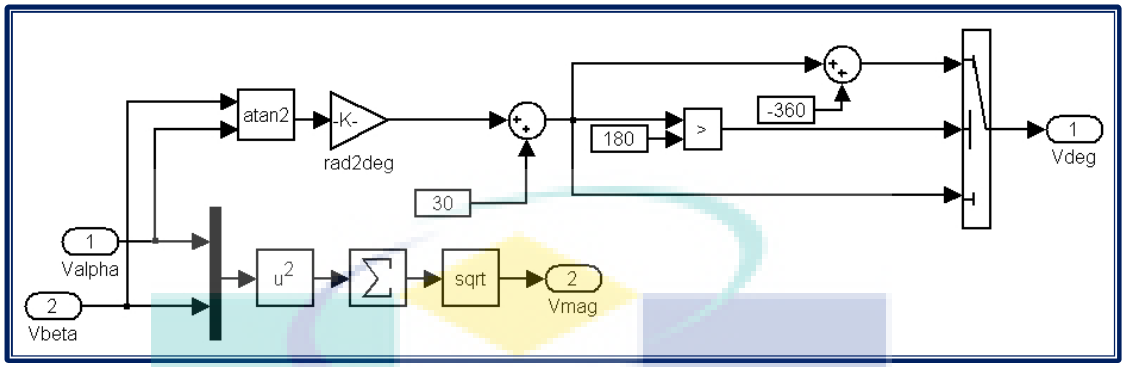


Figure 3.10: V_{dq} to degree-magnitude

Figure 3.11 is the sector identification and reference angle generation. The angle is generated from the reference output frequency by integrating it. Based on the angle (Figure 3.12), the sector can be identified.

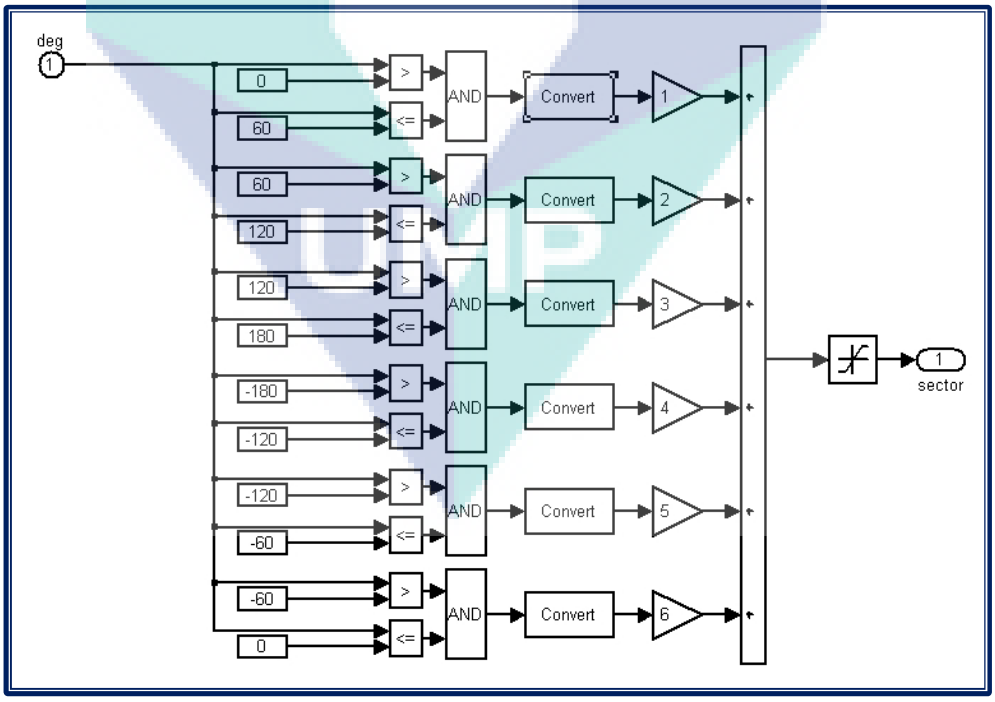


Figure 3.11: Sector Identification

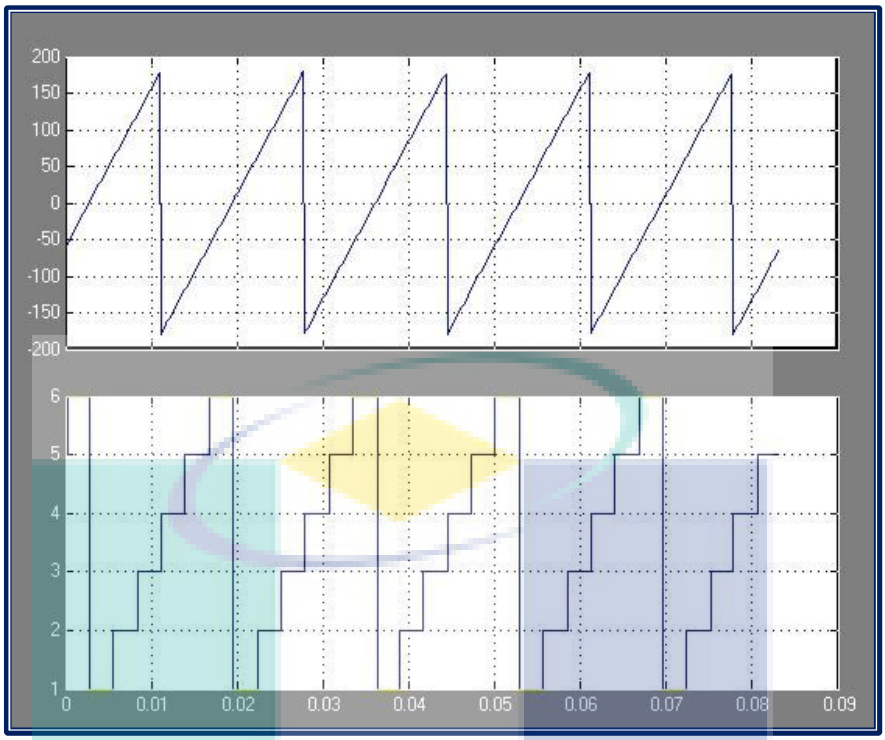


Figure 3.12: Result for sector identification

3.1.2 Voltage Space Inverter Space Vector Modulation

Consider the VSI part of the MC in Figure 3.6 as a standalone VSI supplied by a DC voltage source $V_{pn} = V_{dc}$. The VSI switches can assume only six allowed combinations that yield non-zero output voltages. The space vector of the desired output line voltages is given as

$$\overrightarrow{V_o} = \sqrt{3} \, . V_{oi} . e^{j(\omega_o t - \emptyset_i + 30^\circ)} \qquad (3.\ 9)$$

V_{oi} $; i \in \{u, v, w\}$ can be approximated by two adjacent state vectors V_d and V_q, and the zero voltage vector, V_0 using PWM as shown in Figure 2.6. The duty cycles of the switching state vectors are as

$$d_{av} = m_v \, . \sin\left(\frac{\pi}{3} - \theta_v\right) \qquad (3.\ 10)$$

$$d_{\beta v} = m_v \,.\sin\theta_v \tag{3. 11}$$

$$d_{0v} = 1 - d_{\alpha v} - d_{\beta v} \tag{3. 12}$$

where m_v is the VSI modulation index as

$$0 \le m_v = \frac{(\sqrt{3}.V_{oi})}{V_{dc}} \le 1 \tag{3. 13}$$

The averaged output line voltages are

$$\begin{bmatrix}\vec{V}_u\\ \vec{V}_v\\ \vec{V}_w\end{bmatrix} = \begin{bmatrix}d_{\alpha v} + d_{\beta v}\\ -d_{\alpha v}\\ -d_{\beta v}\end{bmatrix}.V_{dc}$$

$$= m_v \cdot \begin{bmatrix}\cos\left(\theta_v - \frac{\pi}{6}\right)\\ -\sin\left(\frac{\pi}{3} - \theta_v\right)\\ -\sin(\theta_v)\end{bmatrix}.V_{dc} \tag{3. 14}$$

For the first sector, $-30^\circ \le \omega_o t - \emptyset_o + 30^\circ \le +30^\circ$

$$\theta_v = (\omega_o t - \emptyset_o + 30^\circ) + 30^\circ \tag{3. 15}$$

By substituting Eq. (3.13) into Eq. (3.14)

$$\begin{bmatrix}\vec{V}_u\\ \vec{V}_v\\ \vec{V}_w\end{bmatrix} = m_v \,. \begin{bmatrix}\cos(\omega_o t - \emptyset_o + 30^\circ)\\ \cos(\omega_o t - \emptyset_o + 30^\circ - 120^\circ)\\ \cos(\omega_o t - \emptyset_o + 30^\circ + 120^\circ)\end{bmatrix}.V_{dc}$$

$$= \vec{T}_{\text{VSI}} \,.V_{dc} \tag{3. 16}$$

Substituting the modulation index from Eq. (3.13) into Eq. (3.16), the output line voltages are obtained as

$$V_{o=}\begin{bmatrix}\vec{V}_u\\ \vec{V}_v\\ \vec{V}_w\end{bmatrix} = \sqrt{3}\,.V_{oi}\,.\begin{bmatrix}\cos(\omega_o t - \emptyset_o + 30^\circ)\\ \cos(\omega_o t - \emptyset_o + 30^\circ - 120^\circ)\\ \cos(\omega_o t - \emptyset_o + 30^\circ + 120^\circ)\end{bmatrix} \quad (3.17)$$

The VSI averaged input current is determined as

$$\vec{\imath}_p = \vec{T}^{T}_{VSI}.\,i_o = \frac{\sqrt{3}}{2}\,.I_{om}\,.m_v.\cos(\emptyset_L) = constant \quad (3.18)$$

The ITF approaches enable application of well known standard VSI and VSR PWM techniques for MC control. In the case of output line voltage synthesis, the maximum VSI voltage gain is equal to unity and hence from Eq. (3.18) the maximum MC gain is $\sqrt{3}/_2$. When sinusoidal output voltages are synthesized, the maximum phase voltage amplitude is one-half of the DC-link, and from Eq. (3.18) the maximum MC gain is $3/_4$. In this case, the output neutral point voltage is equal to DC-link midpoint voltage, which varies as $V_{im}/_4 \cdot \cos 3\omega_i\, t$ with respect to the input neutral. The modeling of the inversion stage is shown in Figure 3.13.

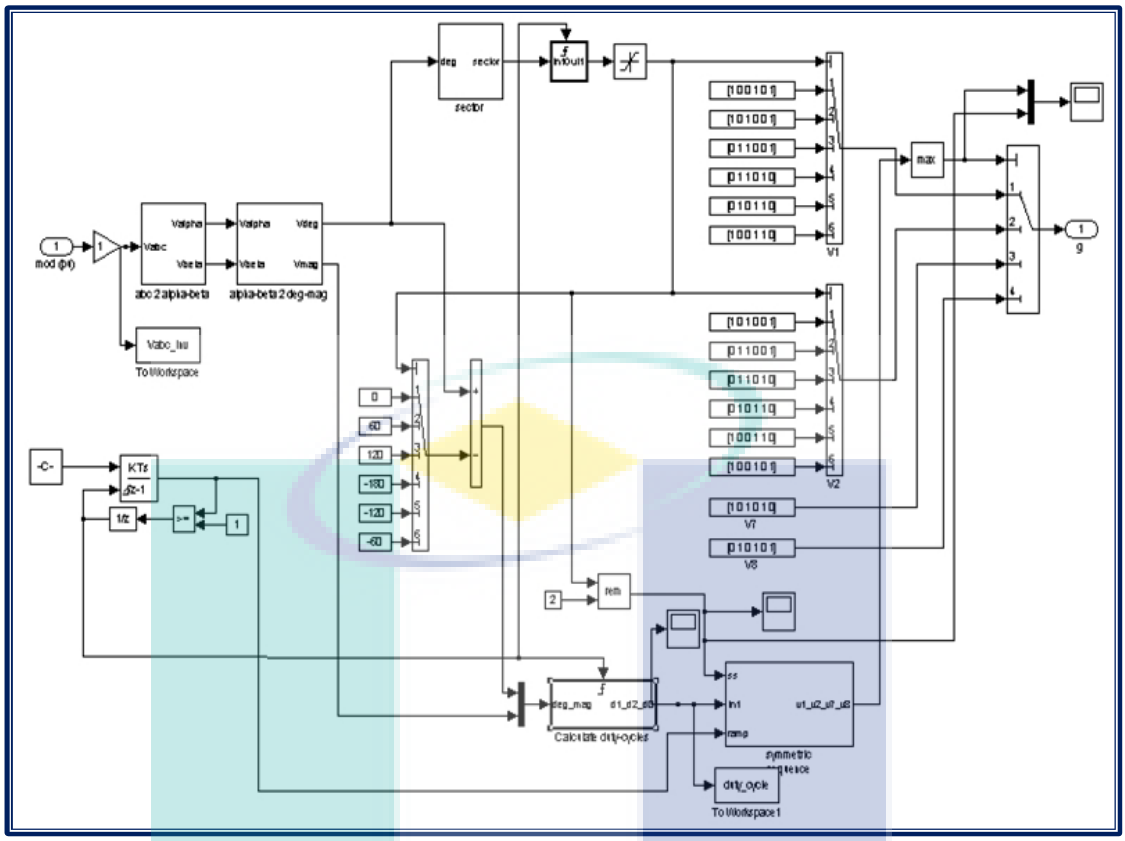


Figure 3.13: SVM inversion stage

3.1.3 Output Voltage and Input Current SVM

Direct converter modulation of an MC can be derived from the ITF. First modulation is carried out as if the converter is an indirect. The switch control signals for MC are then derived based on the relation between the VSR and VSI. The modulation index of the MC is given as

$$m = m_i . m_v \qquad (3.\ 19)$$

For simplicity, $m_v = 1$ and $m = m_i$.The modulation algorithm is derived similarly to VSR and VSI except in the opposite direction. Since, both the VSR and VSI hexagons contain six sextants; there are 36 combinations or operating modes. However, only 27 valid switch combinations giving thus 27 voltage vectors as shown

in Table 2.1. If the first output voltage and input current are active, the transfer matrix becomes

$$\vec{\mathrm{T}}_{\mathrm{ph}} = m \cdot \begin{bmatrix} \cos\left(\theta_v - \frac{\pi}{6}\right) \\ -\sin\left(\frac{\pi}{3} - \theta_v\right) \\ -\sin(\theta_v) \end{bmatrix} \cdot \begin{bmatrix} \cos\left(\theta_i - \frac{\pi}{6}\right) \\ -\sin\left(\frac{\pi}{3} - \theta_i\right) \\ -\sin(\theta_i) \end{bmatrix}^T \quad (3.\ 20)$$

The output line voltages are

$$V_o = \begin{bmatrix} \vec{V}_u \\ \vec{V}_v \\ \vec{V}_w \end{bmatrix} = \begin{bmatrix} d_{\alpha v} + d_{\beta v} \\ -d_{\alpha v} \\ -d_{\beta v} \end{bmatrix} \cdot \begin{bmatrix} d_{\alpha i} + d_{\beta i} \\ -d_{\alpha i} \\ -d_{\beta i} \end{bmatrix}^T \cdot \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (3.\ 21)$$

$$V_{ab} = V_{a0} - V_{b0} \ \ and \ \ V_{ac} = V_{a0} - V_{c0} \quad (3.\ 22)$$

which finally yields

$$\begin{bmatrix} \vec{V}_u \\ \vec{V}_v \\ \vec{V}_w \end{bmatrix} = \begin{bmatrix} d_{\alpha\_vi} + d_{\beta\alpha\_vi} \\ -d_{\alpha\_vi} \\ -d_{\beta\alpha\_vi} \end{bmatrix} . V_{ab} + \begin{bmatrix} d_{\alpha\beta\_vi} + d_{\beta\_vi} \\ -d_{\alpha\beta\_vi} \\ -d_{\beta\_vi} \end{bmatrix} . V_{ac} \quad (3.\ 23)$$

Where,

$$d_{\alpha\_vi} = d_{\alpha_v} . d_{\alpha_i} = m \cdot \sin\left(\frac{\pi}{3} - \theta_v\right) \cdot \sin\left(\frac{\pi}{3} - \theta_i\right) = \frac{T_{\alpha\_vi}}{T_s} \quad (3.\ 24)$$

$$d_{\beta\alpha\_vi} = d_{\beta_v} . d_{\alpha_i} = m \cdot \sin(\theta_v) \cdot \sin\left(\frac{\pi}{3} - \theta_i\right) = \frac{T_{\beta\alpha\_vi}}{T_s} \quad (3.\ 25)$$

$$d_{\alpha\beta\_vi} = d_{\alpha_v} . d_{\beta_i} = m \cdot \sin\left(\frac{\pi}{3} - \theta_v\right) \cdot \sin(\theta_i) = \frac{T_{\alpha\beta\_vi}}{T_s} \quad (3.\ 26)$$

$$d_{\beta\_vi} = d_{\beta_v} . d_{\beta_i} = m . \sin(\theta_v) . \sin(\theta_i) = \frac{T_{\beta\_vi}}{T_s} \quad (3.27)$$

As can be seen, the output line voltages are synthesized inside each switching cycle from samples of two inputs line-to-line voltages, V_{ab} and V_{ac}. By comparison of Eq. (3.23) – (3.27), it can be concluded that simultaneous output voltage and input current SVM can be obtained by employing the standard VSI SVM sequentially in two VSI sub topologies of the three-phase DMC.

When the standard VSI SVM is applied in the first VSI sub topology, where $V_{pn} = V_{ab}$, the duty cycles of the two adjacent voltage switching state vectors are d_{α_vi} and $d_{\beta\alpha\_vi}$ as defined in Eq. (3.25) and Eq. (3.26). The standard VSI-SVM in the second sub topology, with $V_{pn} = V_{ac}$, results in the state switching vector duty cycles $d_{\alpha\beta\_vi}$ and d_{β_vi} , also defined as Eq. (3.26) and (3.27). The remaining part of the switching cycle is given as

$$d_0 = 1 - d_{\alpha\_vi} - d_{\beta\alpha\_vi} - d_{\alpha\beta\_vi} - d_{\beta\_vi} \quad (3.28)$$

3.2 MATRIX CONVERTER FED INDUCTION MOTOR DTC STRATEGY

The principle of selecting the voltage vector is shown in Figure 3.14. If the stator flux rotates in counterclockwise and imposes vector V_2, the flux amplitude increased reaching the upper limits. If vector V_3 is applied, the flux amplitude is reduced and circulates to the lower limits. If the requirement is the clockwise rotation, the direction of the applied voltage vector applied are V_5 andV_6. The rule applies to other sectors.

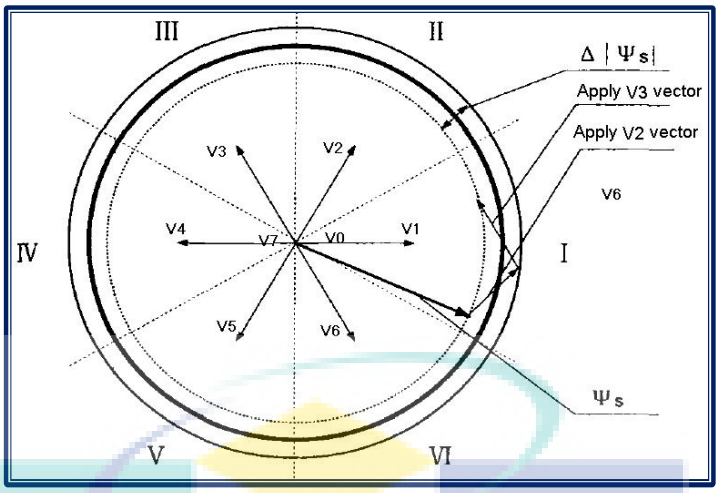


Figure 3.14: The voltage vector Circular flux trajectory

The movement direction of the stator flux depends on the selected voltage vector. Meanwhile, the speed rotation depends on the switching rate. The higher the switching frequency will cause the average rotation speed more uniform at the same time and caused the small torque ripple. However, the hardware requirements are increased. The imposition of the zero voltage space vector is significant as it does not generate new flux and does not produce the electromagnetic torque changes. Based on the above analysis, the complete selection of switching state is shown in look-up table in Table 3.1.

CHAPTER 4

RESULTS AND DISCUSSION

The experimental results of the proposed system which comprise of the combination of the SVM-DTC approach along with the PSO technique are compared with the performance of the basic MC-DTC here on will be referred as to conventional method.

4.1 EFFICIENCY AND POWER FACTOR

Figure 4.1 is the result of efficiency versus the rotor and slip frequency. When $\Delta\omega$ is fixed, the motor efficiency increases with the increasing of the rotor angular frequency. However, when ω_r is fixed, the motor efficiency is increases at first, and starting to show the decreasing trend with the maximum changing process. The value is the maximum efficiency with the increasing of the rotor angular frequency.

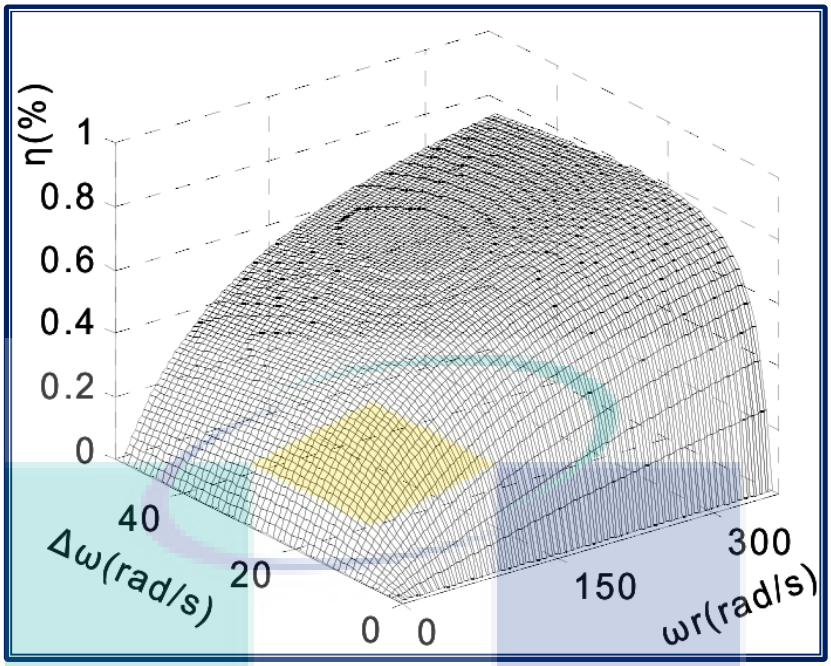


Figure 4.1: Efficiency versus rotor and slip frequency

Figure 4.2 shows that the power factor has small changes when the speed is large, but when the speed is lowered to its maximum of about 10%, the power factor increases rapidly. The curve bends of Figure 4.1 shows the clear trend. The power factor increases with the increases of the slip frequency when ω_r is fixed.

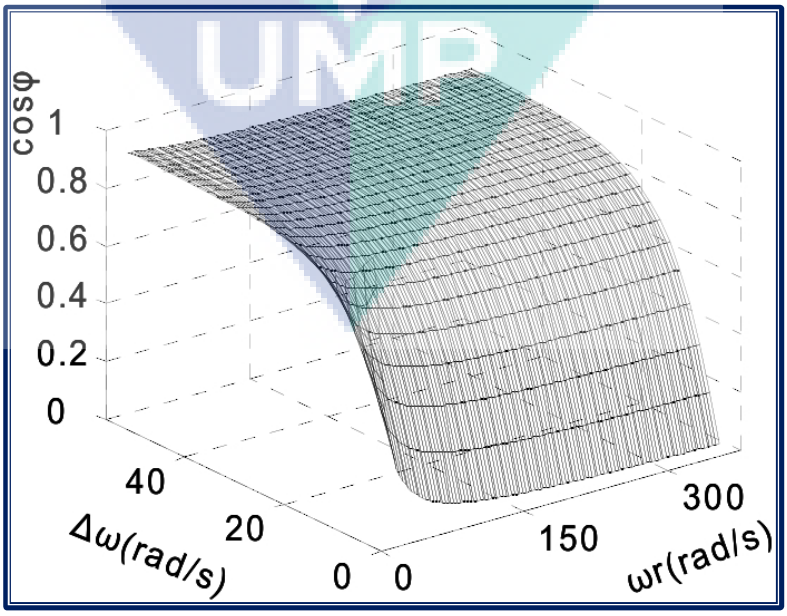


Figure 4.2: Power factor versus rotor and slip frequency

From the previous analysis, it was concluded that the power factor is not at its highest when the efficiency is maximized, but the relationship is one to one. Thus, the power factor can be used as the control volume. As can be seen from the figure, the power factor control is the motor slip frequency control for different operating conditions by adjusting the input voltage to keep the slip frequency $\Delta\omega^B$ around$\Delta\omega$. The best power factor angle of the rotor frequency curve is shown in Figure 4.3.

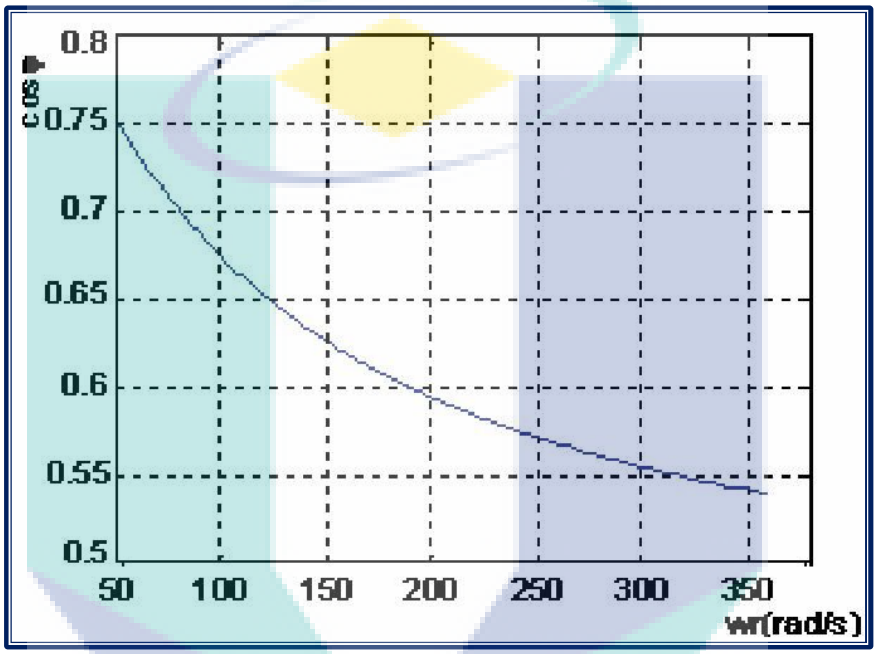


Figure 4.3: Relation between the rotor frequency and best power factor

It can be seen in the normal operating speed range, the best power factor changes between 0.55 to 0.75. From the control perspective, the power factor should be controlled along with the changes of a given speed so that it is always running at a maximum efficiency state. Figure 4.4 represents the plot of an MC efficiency at various speed from 25% to 100%.

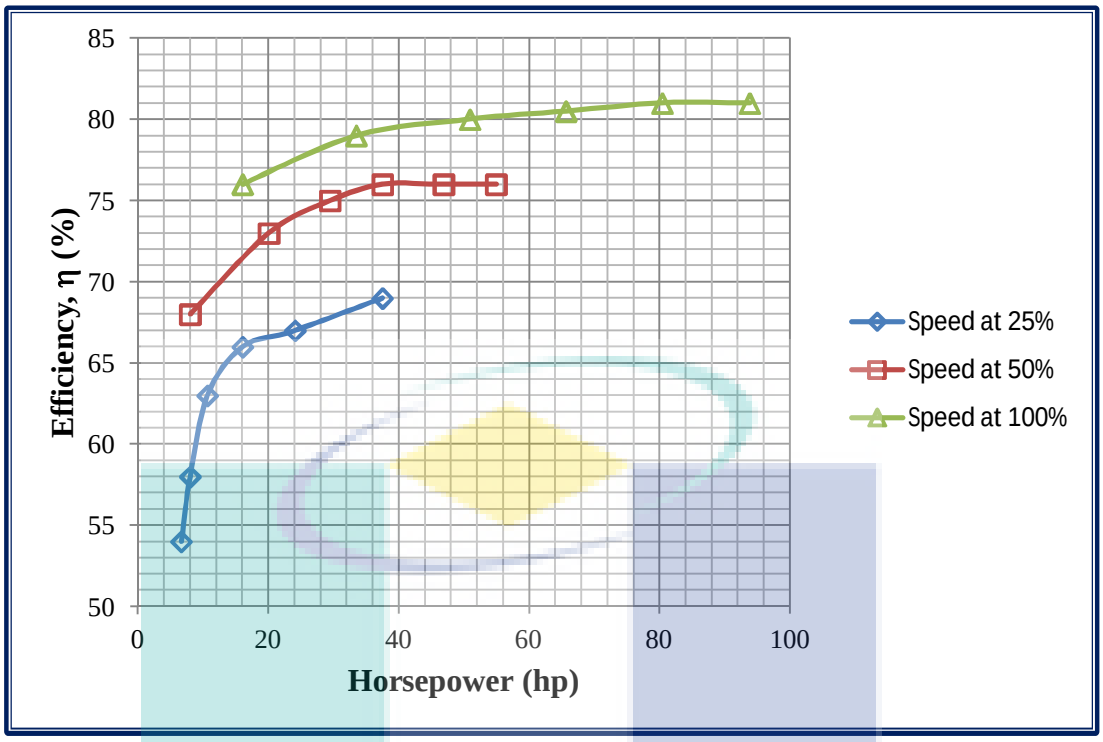


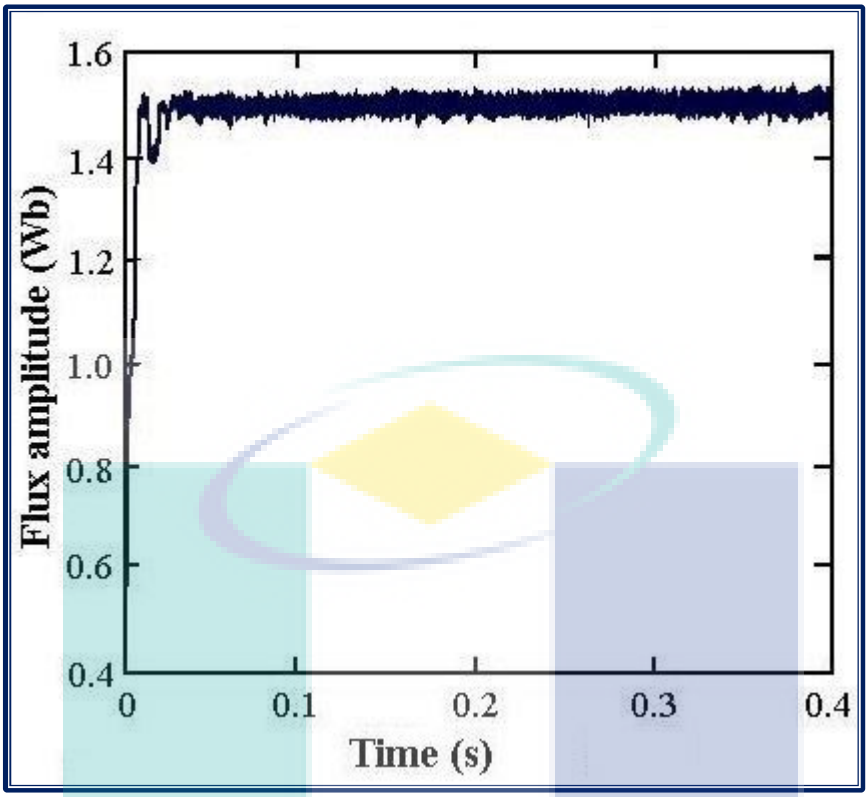
Figure 4.4: Matrix converter efficiency for various torques and speeds

The highest efficiency of 75% to 81% is achieved at the speed of 50% and 100% are considerably higher than others of a comparable hard switching PWM rectifier, DC-link voltage and inverter topology.

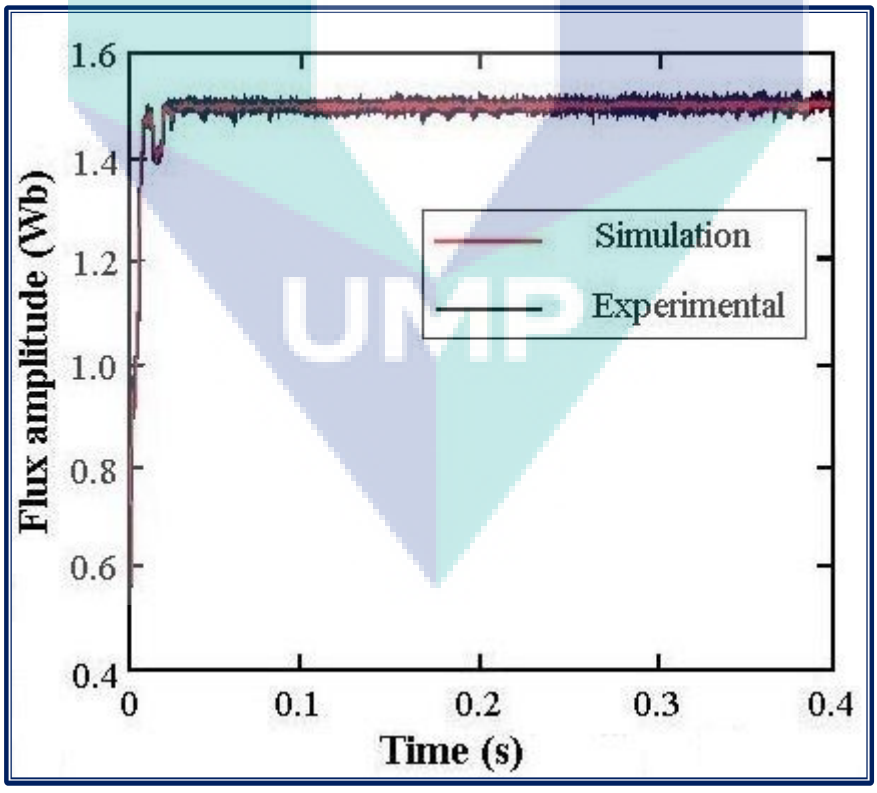
4.2 EXPERIMENTAL RESULTS

4.2.1 Steady-state system analysis

Figure 4.5 shows the simulation and experimental results for the flux transient response at given amplitude of 1.5Wb. The time taken to the flux motor to reach the steady-state is less than 0.05s.



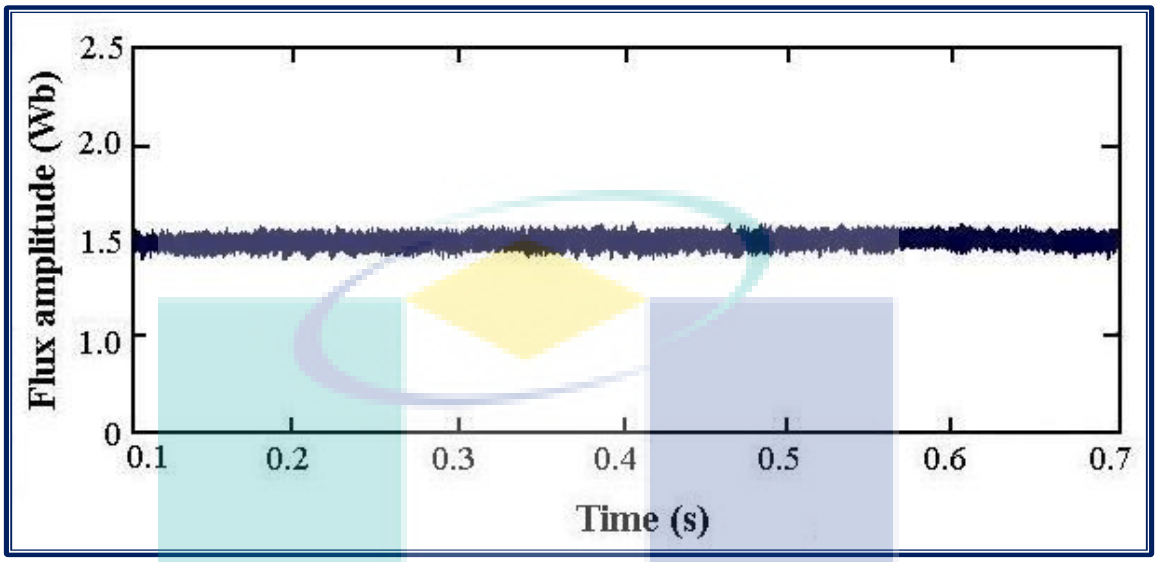
(a)



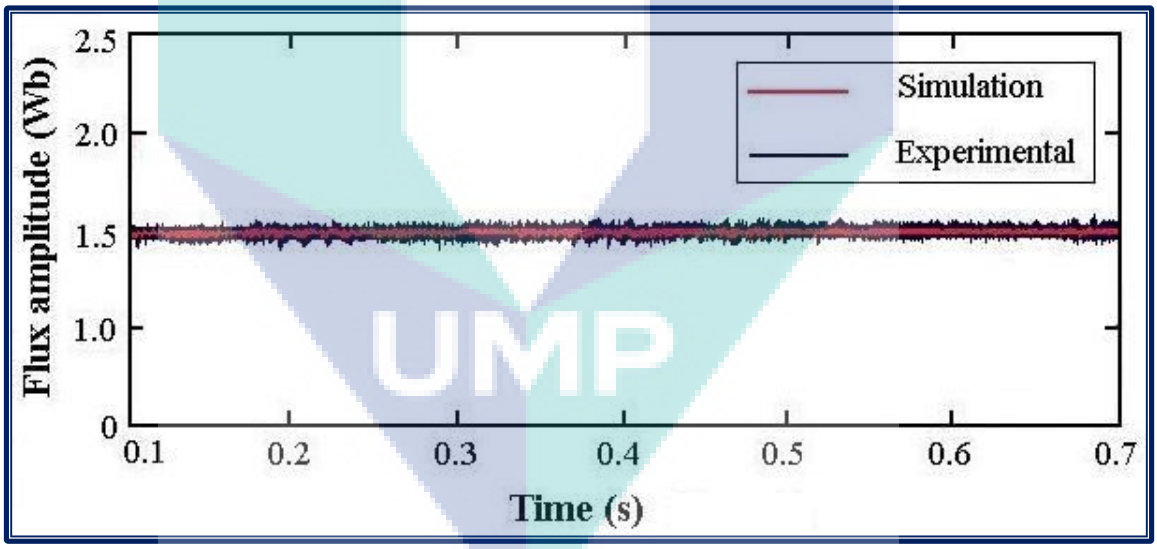
(b)

Figure 4.5: Flux amplitude at transient response; (a) Conventional method; (b) proposed method

Figure 4.6 shows the simulation and experimental results for the flux steady-state response at given amplitude of 1.5Wb.



(a)



(b)

Figure 4.6: Flux amplitude at steady-state response; (a) conventional method; (b) proposed method

The flux ripple of the proposed system is reduced to 0.05Wb. It is seen from this result that the flux ripple are reduced drastically by the proposed method. Figure 4.7 is

the stator flux vector trajectory at the motor start during the stable operation. The trajectory maintains a circular path.

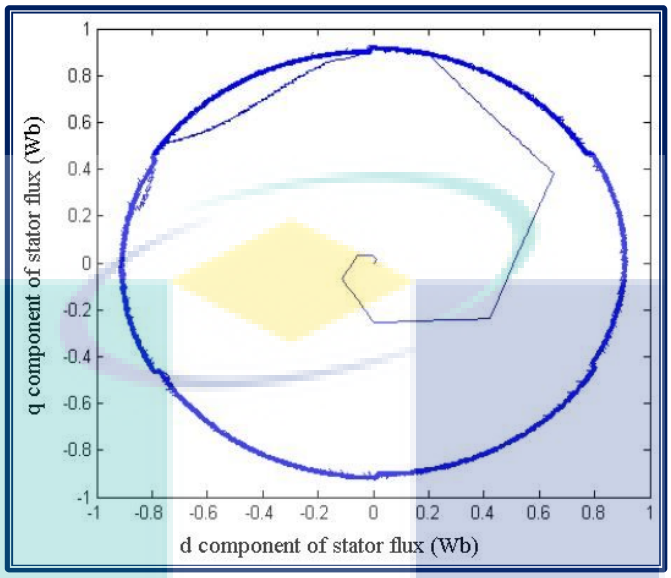
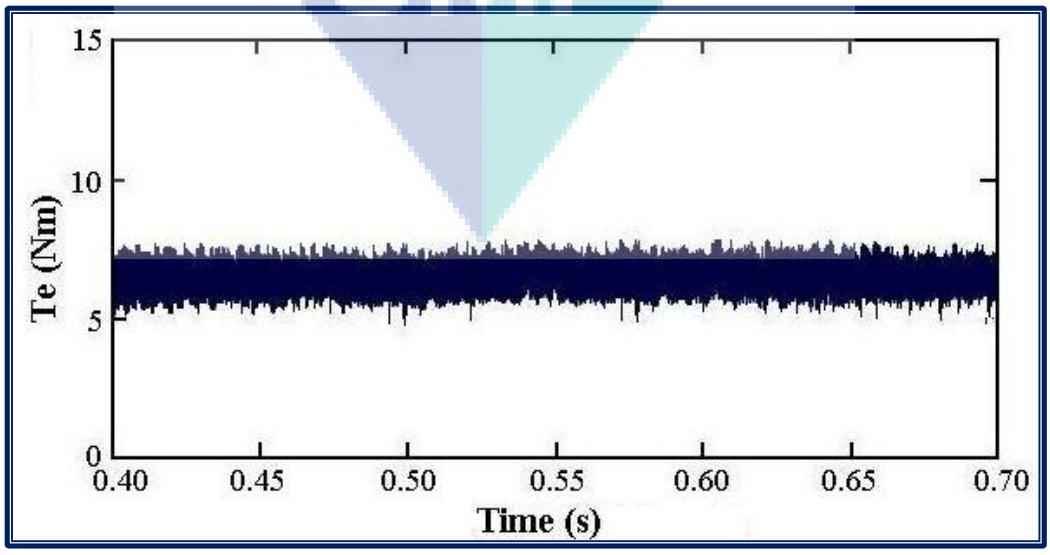
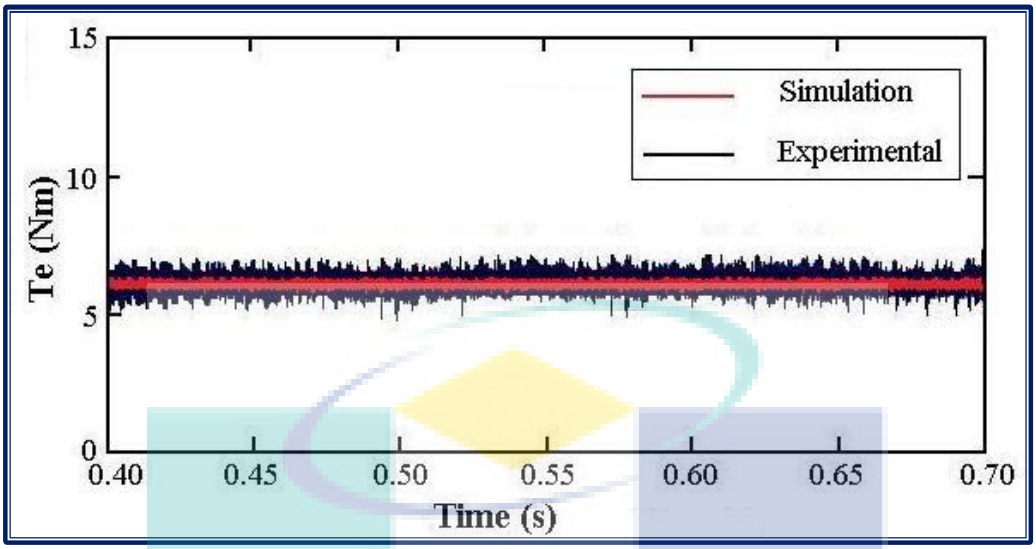


Figure 4.7: Stator flux trajectory

Figure 4.8(a) shows the torque response curve of 6Nm at a speed of 1000rpm using the conventional method. The torque ripple of the proposed system is reduced to 0.1 Nm. It is seen from this result that the torque ripple are reduced drastically by the proposed method.



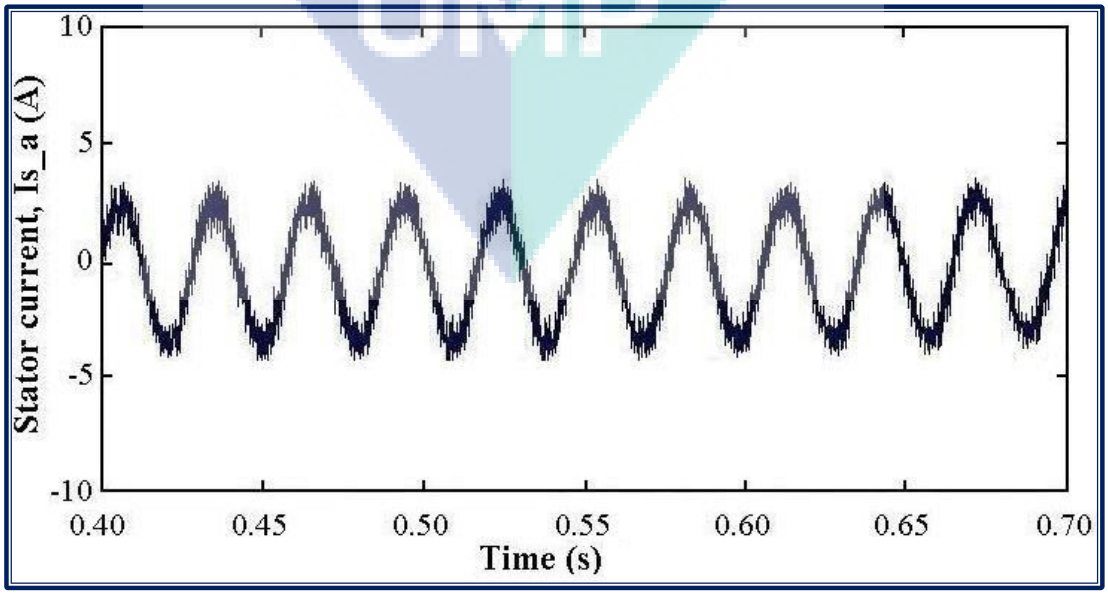
(a)



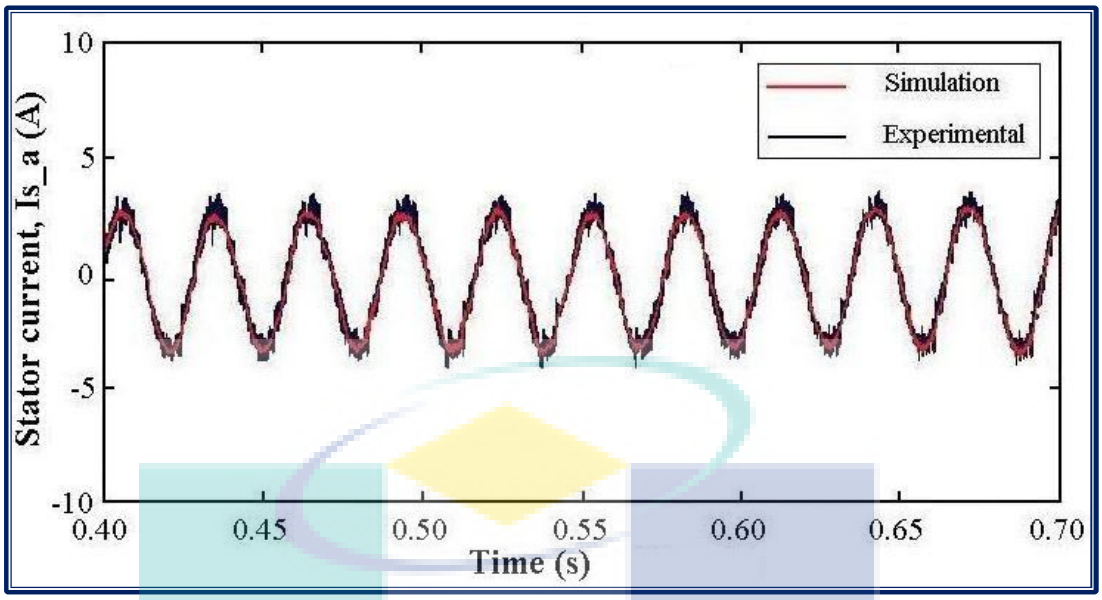
(b)

Figure 4.8: Steady state operation of the motor at speed of 1000rpm; (a) conventional method; (b) proposed system

Figure 4.9 is the phase *a* stator current at a speed of 1000rpm and torque of 6Nm, which shows a good sinusoidal in the proposed method. As can be seen in Figure 4.9 (b) the notching harmonic distortion is greatly reduced compared to the conventional method.



(a)

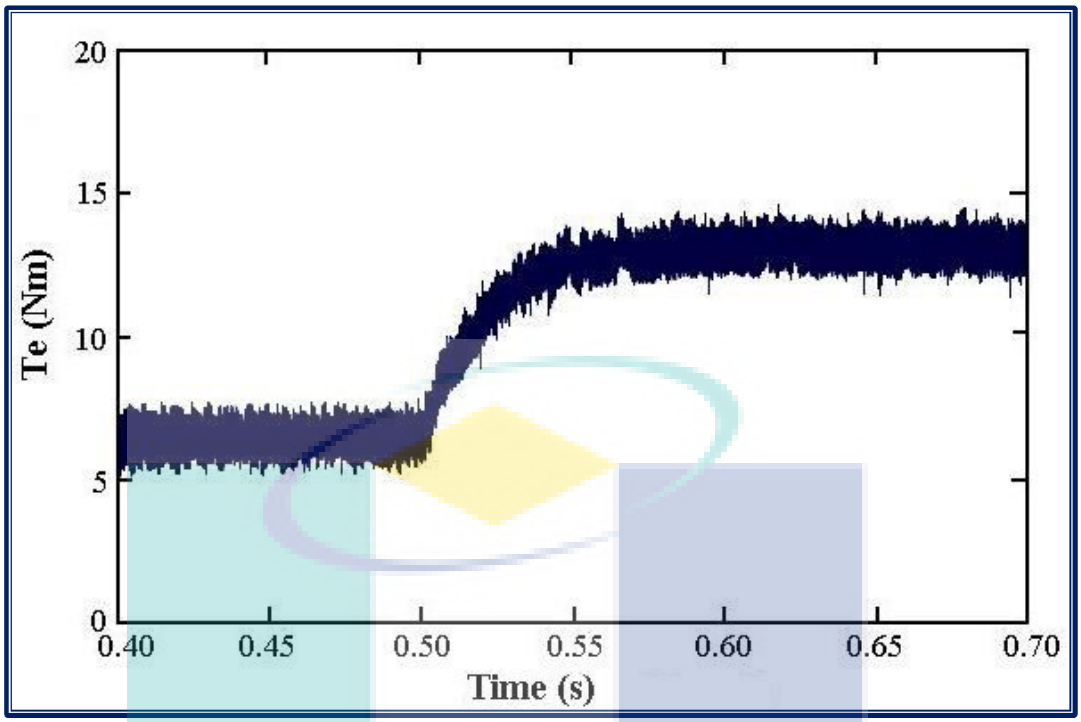


(b)

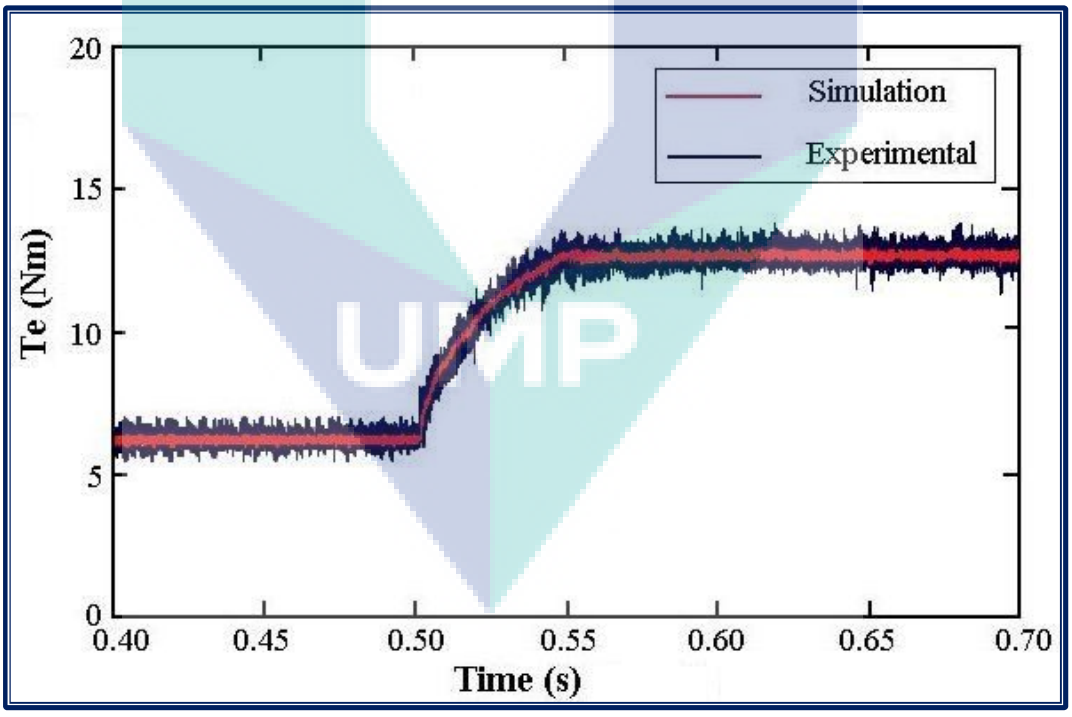
Figure 4.9: Induction motor stator current under steady state operation (a) conventional method; (b) proposed method

4.2.2 Dynamic system analysis

Figure 4.10 and Figure 4.11 shows the response of torque and phase *a* stator current when the torque is changed from 6Nm to 12Nm. It can be seen that the stator current response to the changes of torque command as shown in Figure 4.11(b).

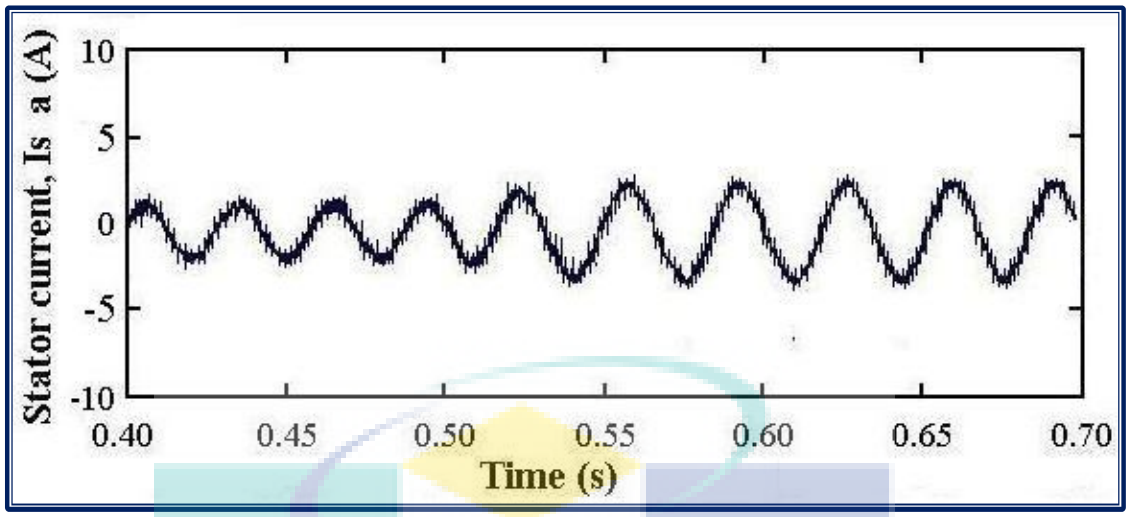


(a)

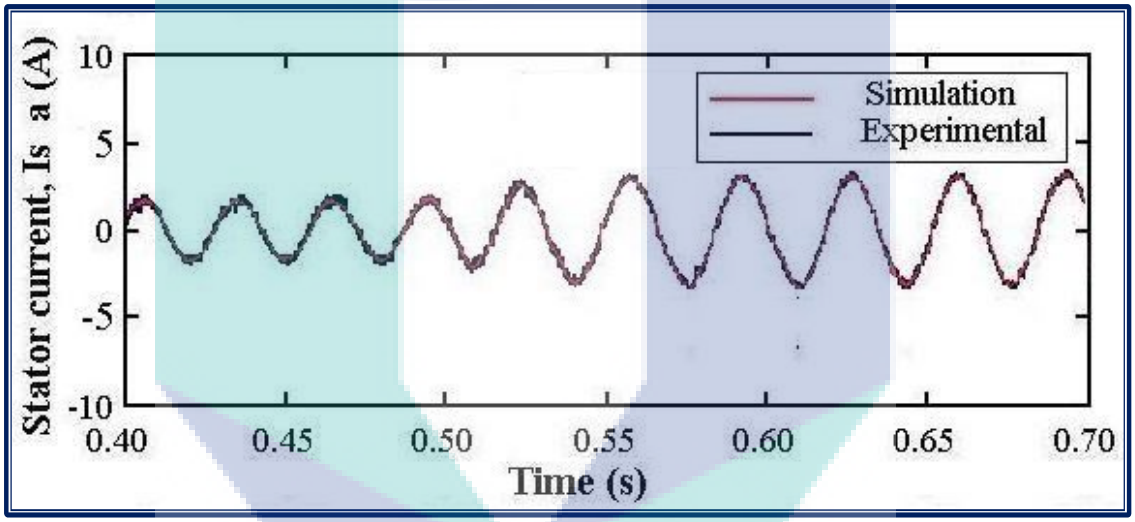


(b)

Figure 4.10: Torque changes from 6Nm to 12Nm; (a) conventional method; (b) proposed method



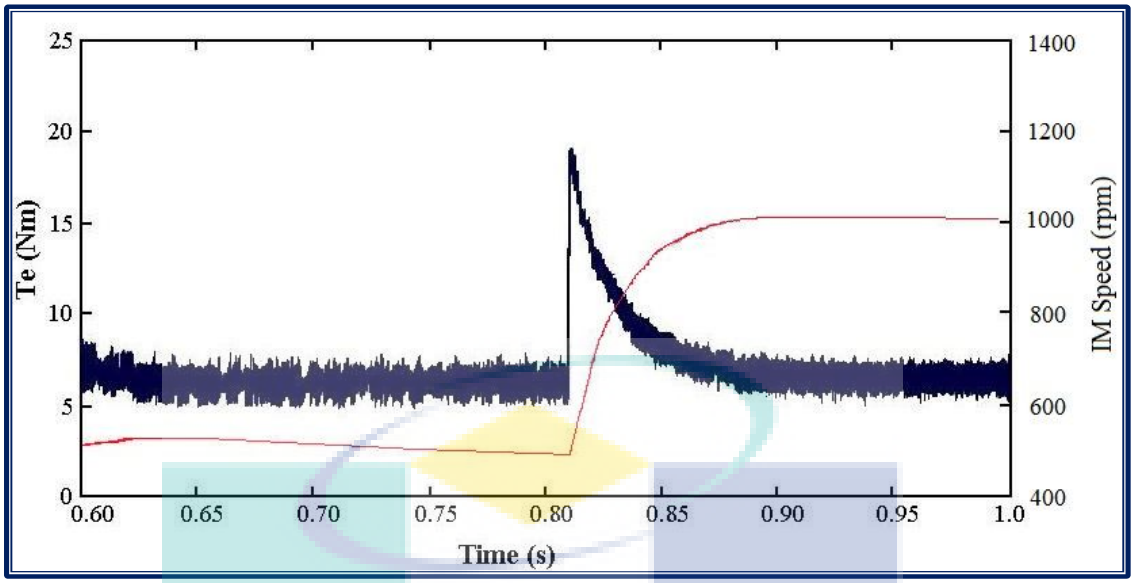
(a)



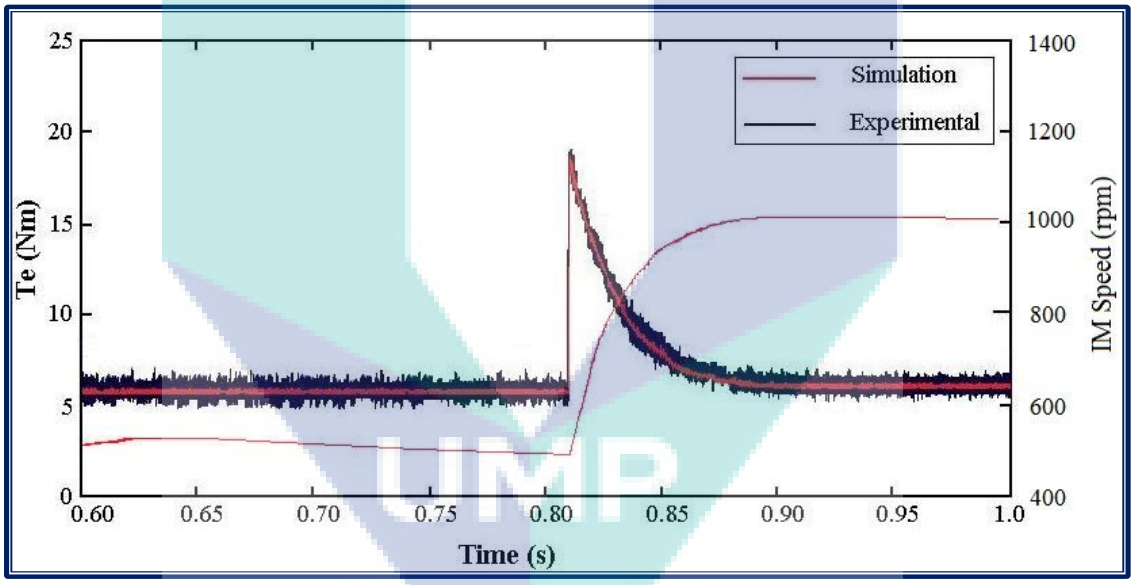
(b)

Figure 4.11: Stator current with torque changes; (a) conventional method; (b) proposed method

Figure 4.12 shows the torque response when the speed increased from 500rpm to 1000rpm, without using the proposed method. The greater torque impact is achieved with the speed increases at less than 0.05s.



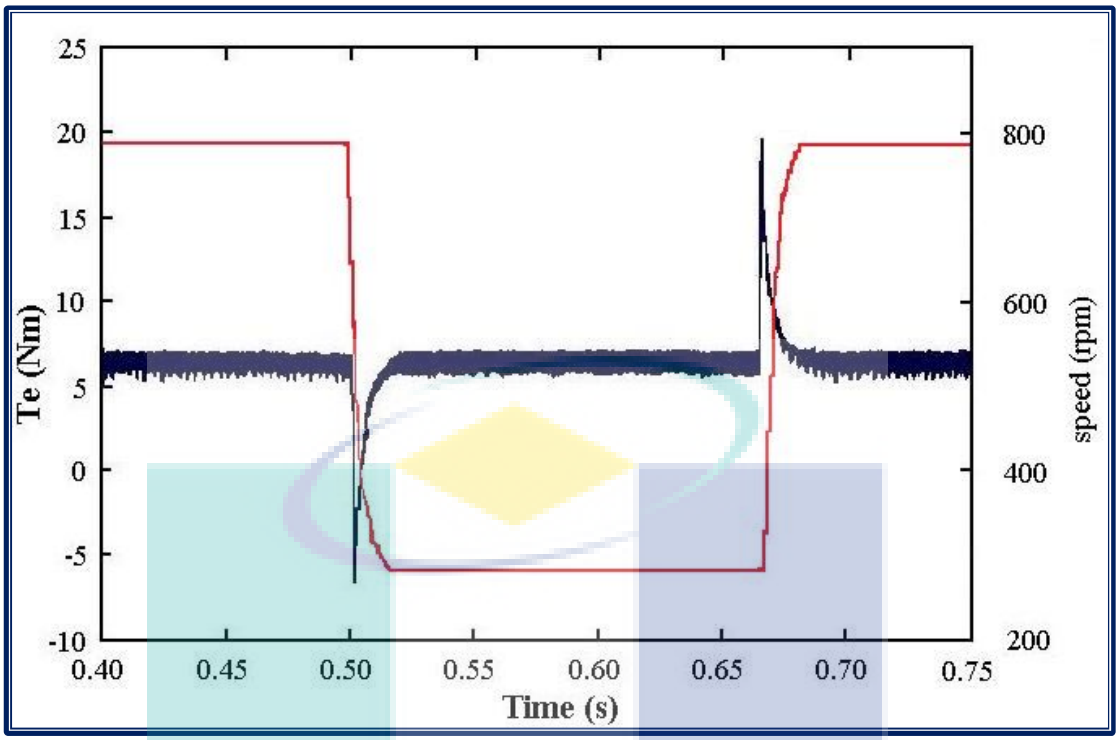
(a)



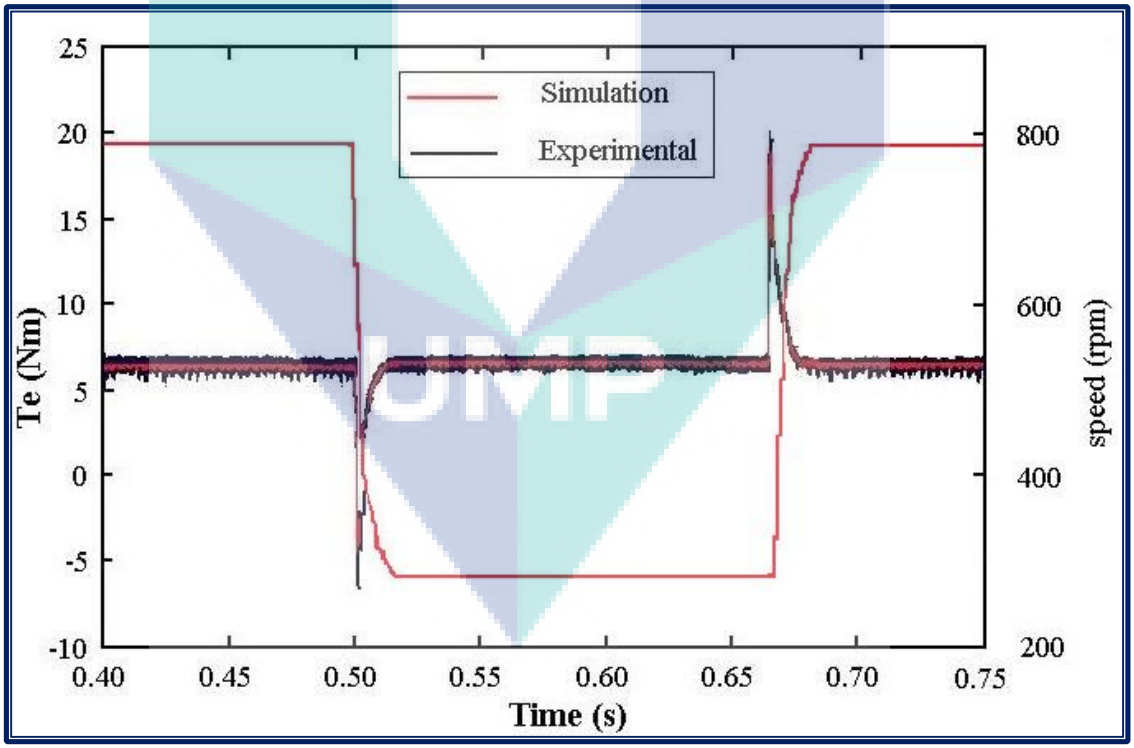
(b)

Figure 4.12: Effect of changes the motor speed of the torque response; (a) conventional method; (b) proposed method

When the curve of the speed changes in Figure 4.13, the torque response changes with the speed changes. The electromagnetic torque is reversed following the speed command as in Figure 4.13.



(a)



(b)

Figure 4.13: Torque response with dynamic changes of motor speed (a) conventional method (b) proposed method

Figure 4.14 shows the measured speed responses of the MC drive system with different control methods. The transient responses with a speed command of 500rpm are observed.

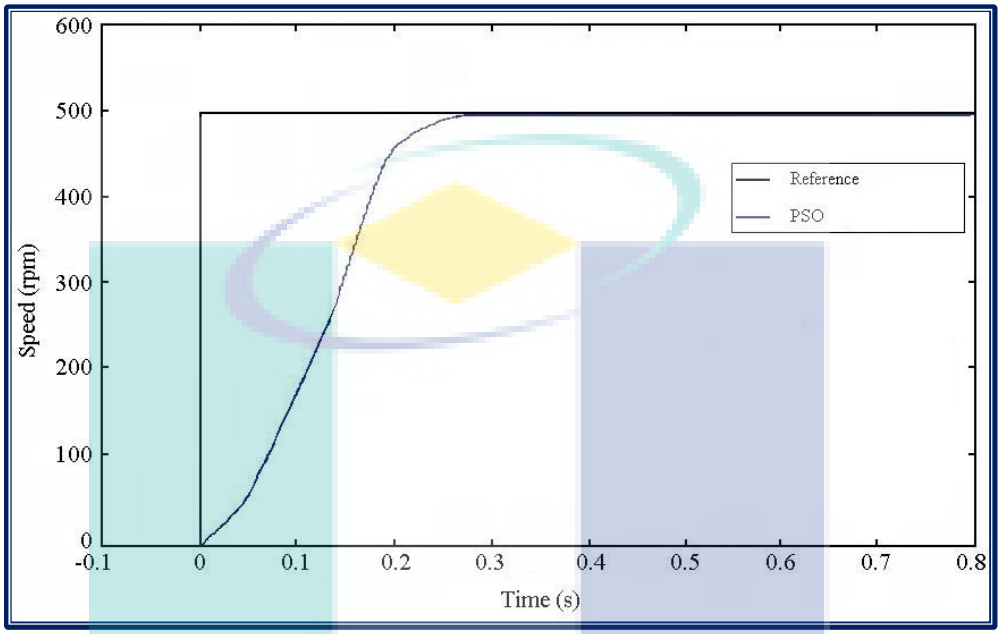


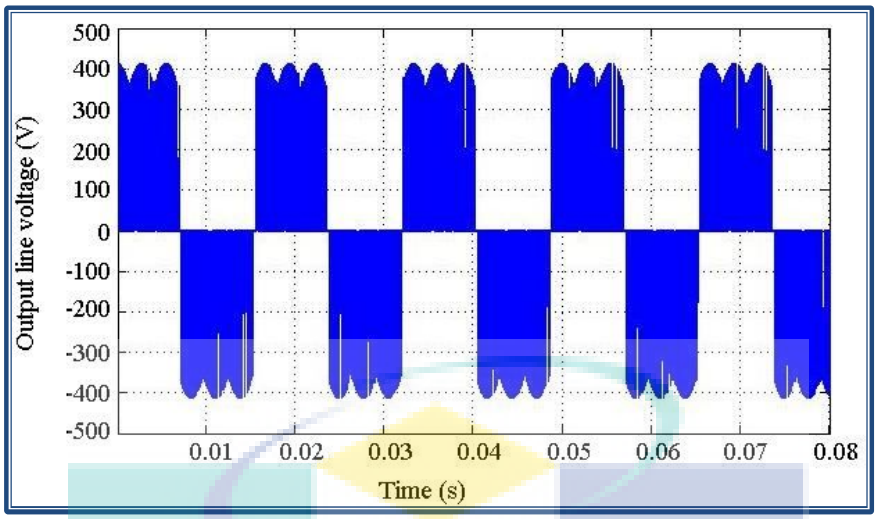
Figure 4.14: Speed response at a reference speed of 500rpm

According to Figure 5.11, the proposed control algorithm, which uses PSO to adjust the PI controller parameters, performs better than the fuzzy logic fixed PI controllers (Joshi et al. 2007) in terms of time response, as summarized in Table 4.1.

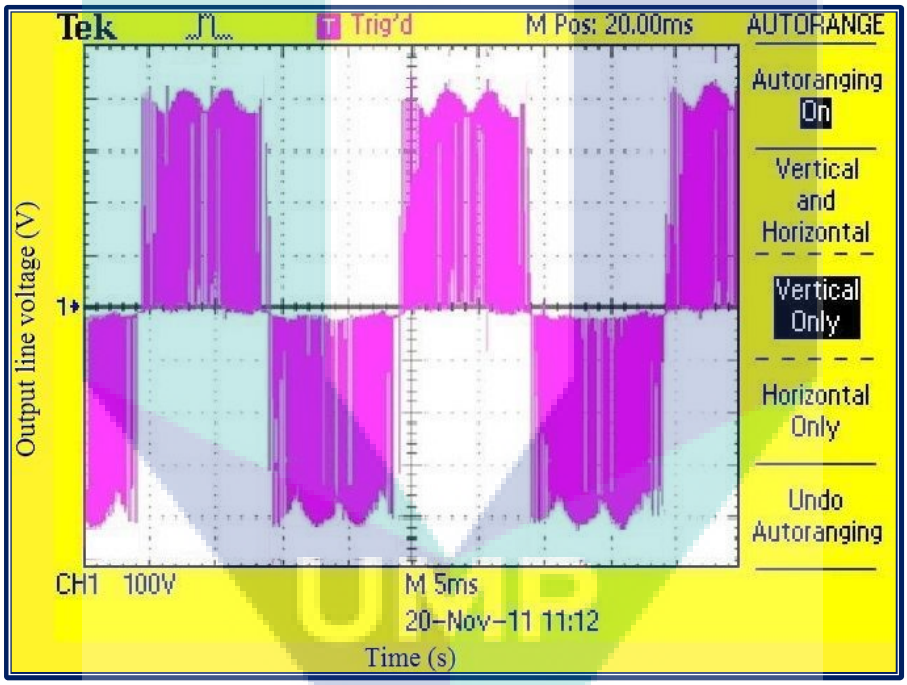
Table 4.1: Time response for PSO and fuzzy

	PSO	**Fuzzy**
T_r (s)	0.11	0.13

The output line voltage waveform is shown in Figure 4.15.



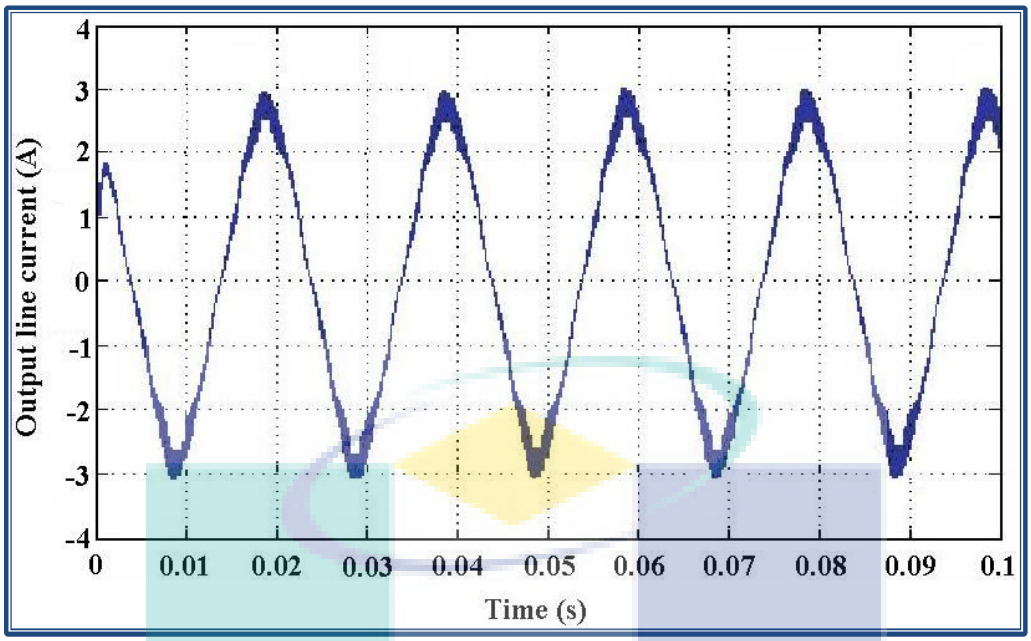
(a)



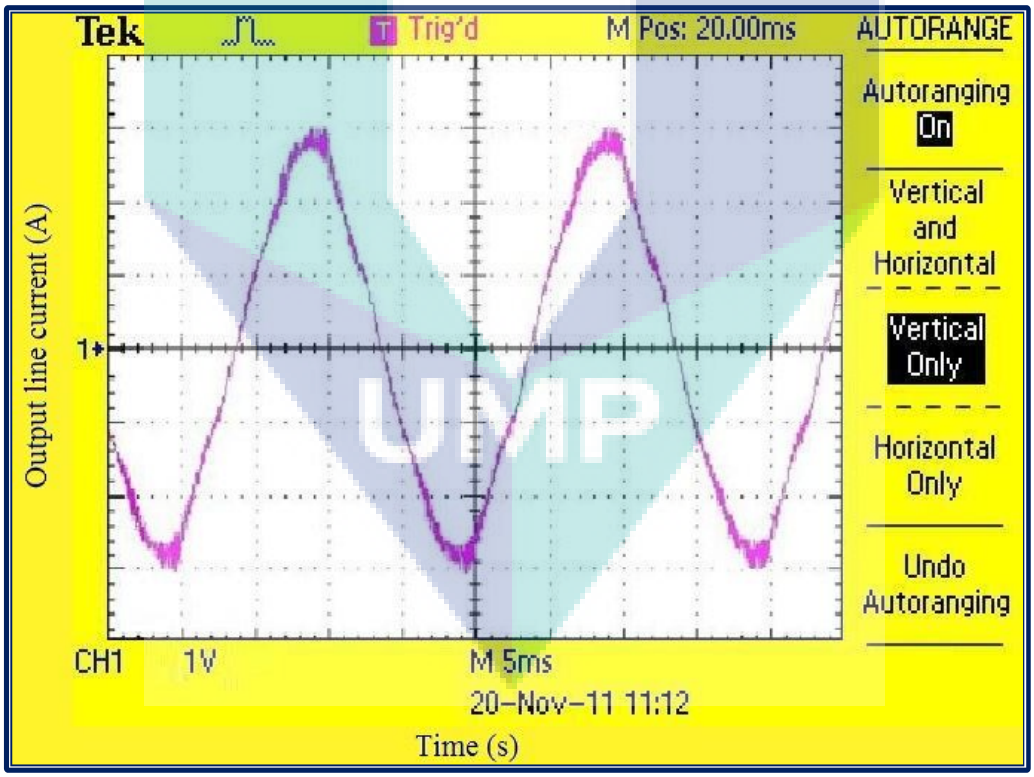
(b)

Figure 4.15: Output line voltage waveform; (a) Simulation; (b) Experimental

The output line and the input phase current waveforms are shown in Figure 4.16 and Figure 4.17 respectively.

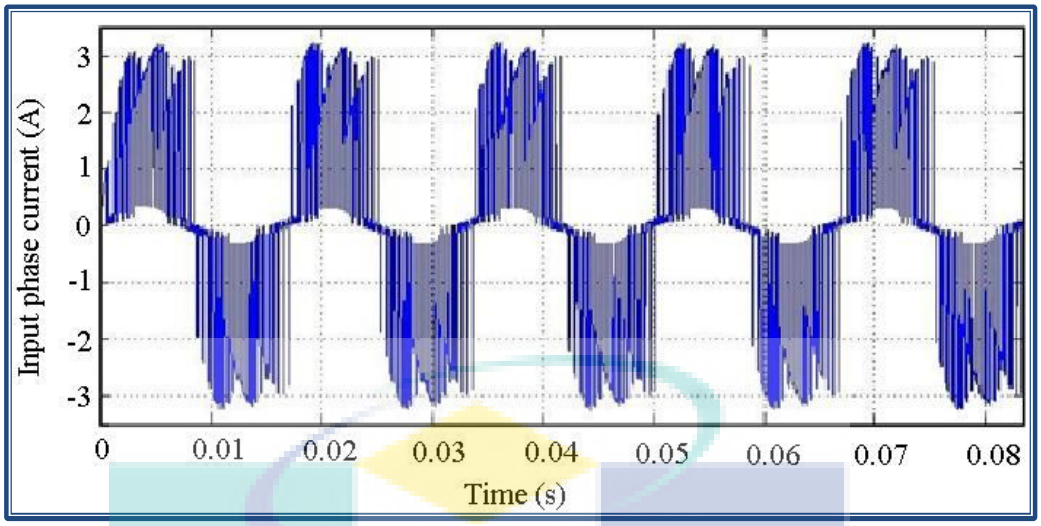


(a)

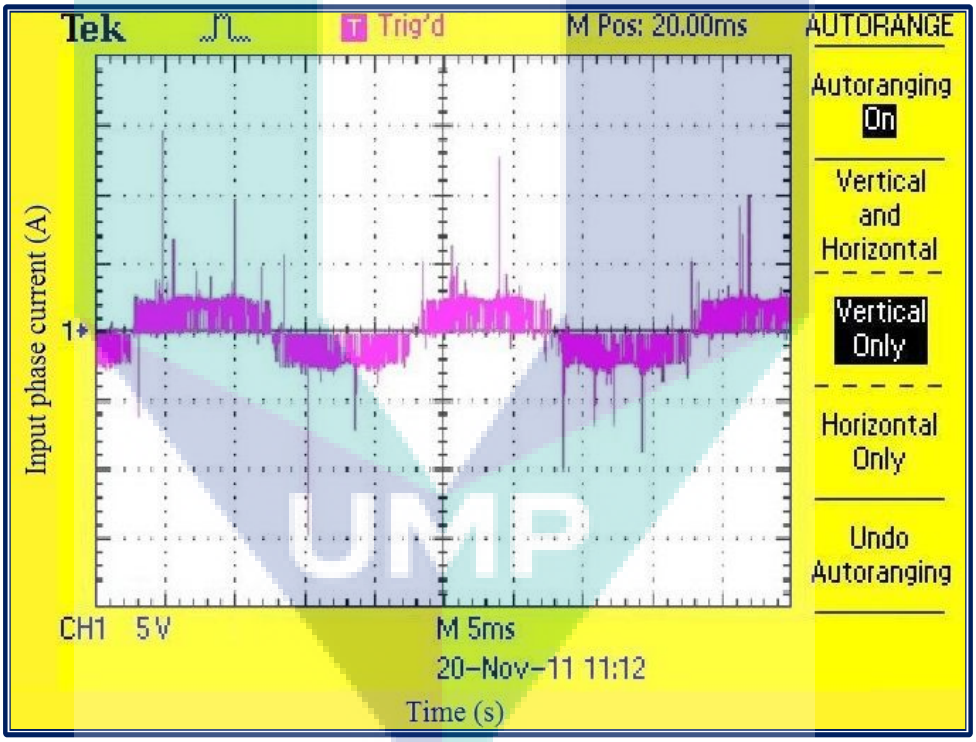


(b)

Figure 4.16: Output line current waveform; (a) Simulation; (b) Experimental



(a)

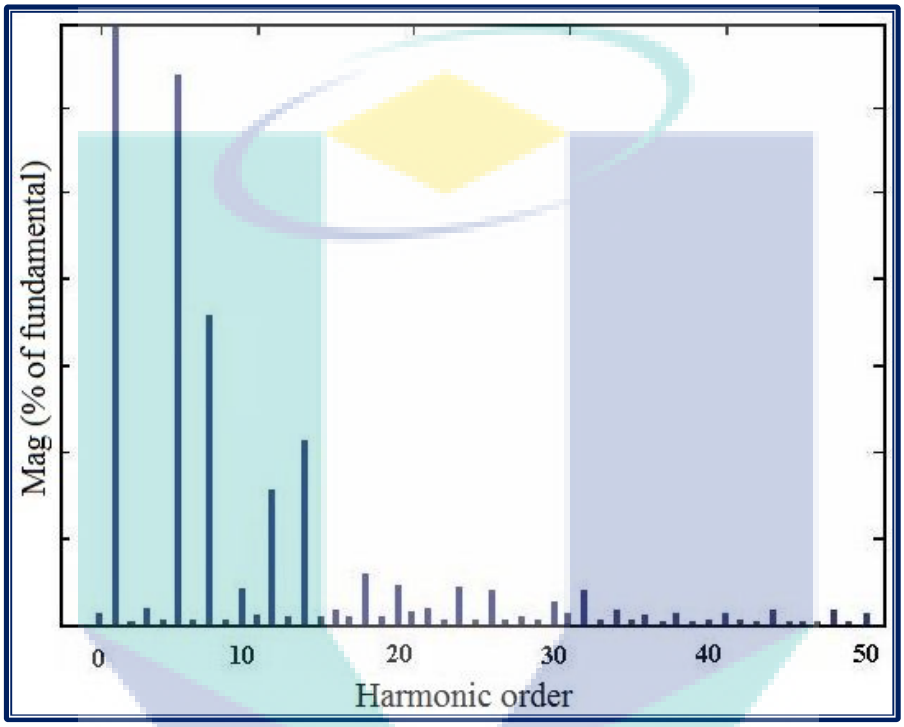


(b)

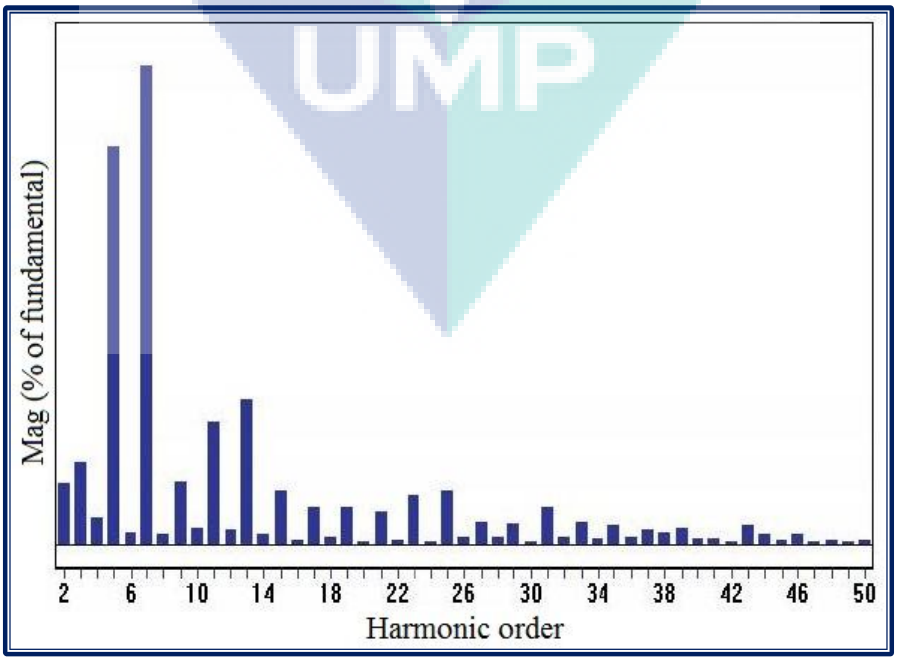
Figure 4.17: Input phase current; (a) Simulation; (b) Experimental

From the simulation and experimental waveforms, it can be seen that both waveforms are similar in shape, amplitude and period. As mentioned in the previous chapter, the input line current is the sine wave as shown in the simulation and experimental result. Similarly, some harmonics can be seen from the actual result despite the use of the input filter device that had smoothened most of the harmonics.

The spectrum analysis of the experimental and simulated output line current waveform is shown in Figure 4.18. The distribution of the output harmonic for the simulation is basically the same with the main low-order harmonics to 5, 7, 11and 13 times. The results prove the good performance of the proposed system.



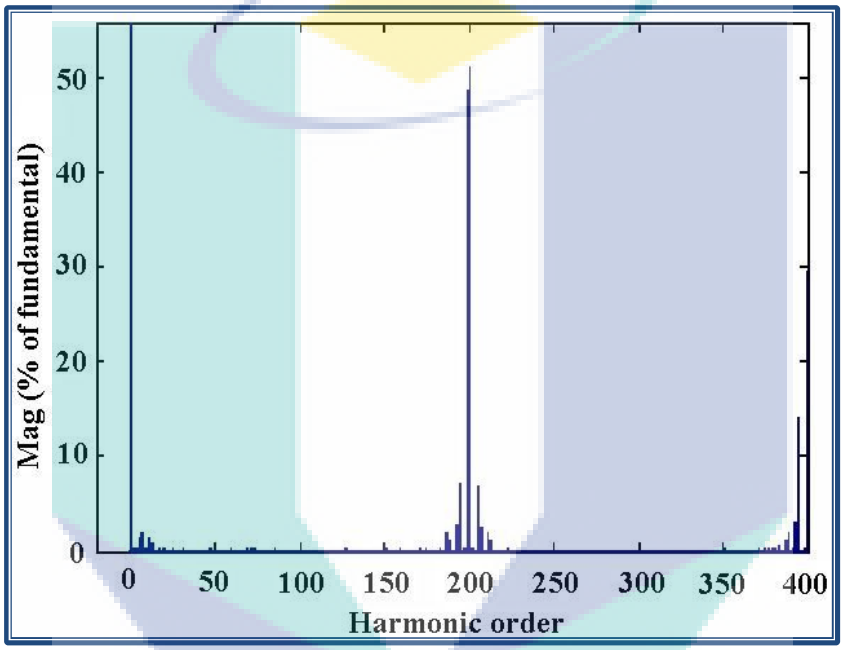
(a)



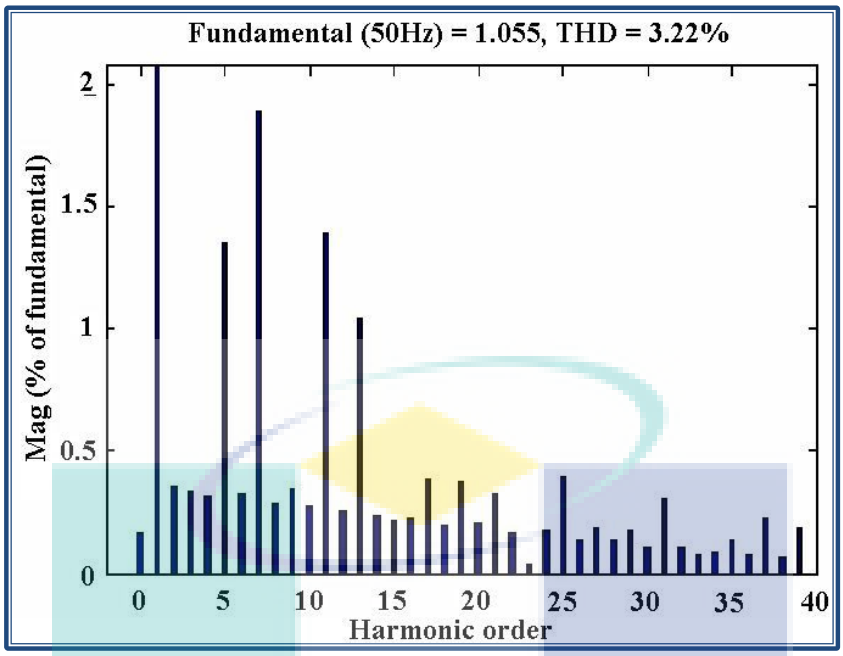
(b)

Figure 4.18: Spectrum analysis diagram; (a) Simulation; (b) Experimental

The analysis of the input current harmonic analysis is based on a simulation method of Figure 4.17 (a) with the use of *Power Systems* library *Powergui* module. The spectrum analysis is shown in Figure 4.19.



(a)



(b)

Figure 4.19: Input current spectrum analysis diagram

From the figure, the input current harmonics are mainly concentrated close to the switching frequency as in Figure 4.19 (a). According to the spectral analysis of the data, the input current THD is 3.22%, for low-order harmonics 5, 7, 11th and 13th harmonics. The amplitude of the fundamental relationship is concluded in Table 5.1.

Table 4.2: Input current harmonics and the amplitude of the fundamental relationship

Harmonic	5	7	11	13
Amplitude of the fundamental relationship (%)	1.35	1.89	1.39	1.04

CHAPTER 5

CONCLUSIONS AND FUTURE WORKS

5.1 CONCLUSION

Matrix converter has attracted wide interest and concern because of its excellent characteristics, small harmonic content, four-quadrant operation capability, and in accordance with the modular power supply or system integration direction. This thesis summarizes the research results of MC based on Space Vector Modulation strategy, Direct Torque Control, commutation method, intelligent control, etc. The proposed method is analyzed in depth using the *Matlab/Simulink*, and the prototype design was developed to validate the feasibility of the simulation model. In summary, the following tasks were completed:

- Analysis and study of the MC-SVM principle and modulation strategy. On this basis, the symmetrical modulation was also analyzed, which reducing the switching losses.
- Analyze the DTC principle based on the traditional VSI and the proposed DTC control for a matrix converter using PSO along with the power factor control feedback resulting in the reducing of electromagnetic torque and optimum efficiency.
- The realization of the MC main circuit and control system using the DSP TMS320F28335 to achieve the SVM-DTC strategy and the PSO technique. Designed the MC main circuit, control circuit, filter circuit, detection circuit and drive circuit and constructed the hardware circuit.

5.2 FUTURE WORKS

Matrix converter has been around for three decades with the matured control strategies, but still not widely used in industrial applications. In this thesis, MC system simulation model and experimental design have achieved certain results. On this basis, further development of the future work should be considered from the following aspects:

- This thesis was only for the three-phase induction motor, further study and analyze of the MC system's input-output performance could be done under different load conditions. Expand optimization on the SVM strategy based on the existing algorithms for easy software and hardware.
- Security for restricting the current flow remains a major factor in the development of MC. Although there have been four-step commutation, but they are not perfect. It is a more reliable way to control the error probability to a very low level.
- The use of other intelligent techniques can be further tested using various intelligent methods such as Fuzzy logic, Neural Network and RBFNN.

REFERENCES

Alesina, A. and Venturini, M. G. B.2002. Analysis and design of optimum-amplitude nine-switch direct AC-AC converters. *IEEE Transactions on Power Electronics*. **4**(1): 101-112.

Alves da Silva, A. P. and Abrao, P. J.2002. Applications of evolutionary computation in electric power systems. *Proceedings of the 2002 Congress on Evolutionary Computation*: 1057–1062.

Beasant, R. R., Beattie, W. C. and Refsum, A.2002. An approach to the realisation of a high power Venturini converter. *Power Electronics Specialists Conference*, 291-297.

Braun, M. and Hasse, K.1983. A direct frequency changer with control of input reactive power. *Control on Power Electronics and Electrical Drives*, 187-194.

Bruckmann, M., Simon, O., Springmann, W., Münzer, M. and Loddenkötter, M.2001. Application of a new IGBT module for matrix converter. *Proceedings of the 2001 European Conference on Power Electronics & Applications*, 1-6.

Buja, G. S. and Kazmierkowski, M. P.2004. Direct torque control of PWM inverter-fed AC motors: A survey. *IEEE Transactions on Industrial Electronics*. **51**: 744-758.

Burany, N.1989. Safe control of four-quadrant switches. *IEEE Industry Applications Society Annual Meeting* **1**: 1190-1194.

Casadei, D., Serra, G. and Tani, A.2000. Implementation of a direct torque control algorithm for induction motors based on discrete space vector modulation. *IEEE Transactions on Power Electronics*. **15**(4): 769-777.

Casadei, D., Serra, G., Trentin, A., Zarri, L. and Calvini, M.2005. Experimental analysis of a matrix converter prototype based on new IGBT modules *Proceedings of the IEEE International Symposium on Industrial Electronics*, **2**: 559-564

Chang, J. and Braun, D.2002. High frequency AC-AC converter using 3-in-1 IBPMs and adaptive commutation. *30th Annual IEEE Power Electronics Specialists Conference*.

Chen, D. F., Liao, C. W. and Yao, K. C.2008. Direct torque control for a matrix converter based on induction motor drive systems. *Second International Conference on Innovative Computing, Information and Control*

Clerc, M. and Kennedy, J.2002. The particle swarm-explosion, stability, and convergence in a multidimensional complex space. *IEEE Transactions on Evolutionary Computation* **6**: 58–73.

Deblon, A. R.2007. Combined DC and AC integration of energy sources in hybrid 3-phase off-grid systems. *4th World Conference on Photovoltaic Energy Conversion*

Depenbrock, M.1987. Direct self control of inverter fed induction machine. *IEEE Power Electronics.*

Dung, P. Q. and Thuong, H. T. N.2004. Direct torque control for induction motor using ANN. *The 2004 International Symposium on Advanced Science and Engineering.*

Empringham, L., Wheeler, P. W. and Clare, J. C.2000. A matrix converter induction motor drive using intelligent gate drive level current commutation techniques. *IEEE Industry Applications Conference*, **3**: 1936-1941.

Empringham, L., Wheeler, P. W. and Clare, J. C.2002. Intelligent commutation of matrix converter bidirectional switch cells using novel gate drive techniques. *29th Annual IEEE Power Electronics Specialists Conference*

Fang, X. and Chen, Z.2009. Current-fed Z-source matrix converter. *International Conference on Applied Superconductivity and Electromagnetic Devices*

Fang, X., Li, C., Chen, Z., Liu, J. and Zhao, X.2011. Three-phase voltage-fed Z-source matrix converter *International Conference on Electrical Machines and Systems*

Ge, B., Lei, Q., Qian, W. and Peng, F. Z.2012. A family of Z-source matrix converters *IEEE Transactions on Industrial Electronics.* **59**(1): 35-46

Gyugyi, L.1970. *Generalized theory of static power frequency changers.* Ph.D University of Salford, UK.

Gyugyi, L. and Pelly, B.1976. *Static power frequency changers.* New York, Wiley.

Habetler, T. G., Profumo, F., Pastorelli, M. and Tolbert, L. M.2002. Direct torque control of induction machines using space vector modulation. *IEEE Transactions on Industry Applications.* **28**(5): 1045 - 1053

Huber, L. and Borojevic, D.1989. Space vector modulator for forced commutated cycloconverters. *EEE Industry Applications Society Annual Meeting,* 871-876.

Huber, L. and Borojevic, D.1995. Space vector modulated three-phase matrix converter with input power factor correction *IEEE Transaction on Industry Applications* **31**(6): 1234-1246.

Huber, L. and Borojevic, D.2002. Space vector modulated three-phase to three-phase matrix converter with input power factor correction. *IEEE Transactions Industry Applications*. **31**(6): 1234-1246.

Huber, L., Borojevic, D. and Burany, N.1989. Voltage space vector based PWM control of forced commutated cycloconverters *15th Annual Conference of IEEE Industrial Electronics Society,* 106-111.

Huber, L., Borojevic, D. and Burany, N.1992. Analysis, design and implementation of the space vector modulator of forced commutated cycloconverters. *Electrical Power Applications* **139**(2): 103-113.

Huber, L., Borojevic, D., Xhuang, X. F. and Lee, F. C.1993. Design and implementation of a three-phase to three-phase matrix converter with input power factor correction. *Applied Poower Electronics Conference and Exposition,* 860-865.

Ishiguro, A., Furuhashi, T. and Okuma, S.1991. A novel control method for forced commutated cycloconverters using instantaneous values of input line-to-line voltages *IEEE Transaction on Electronics.* **38**(3): 166-172.

Itoh, J. I. and Nagayoshi, K. I.2007. A new AC bidirectional switch with regenerative snubber to realize a simple series connection for high power AC/AC direct converters *Power Electronics Specialists Conference.*

Jing, H. and Fahai, L.2005. AC motor and system analysis Beijing, Tsinghua University Press, 380-381.

Jussila, M., Salo, M. and Tuusa, H.2005. Induction motor drive-fed by a vector modulated indirect matrix converter. *35th Annual Power Electronics Specialists Conference.*

Jussila, M. and Tuusa, H.2007. Comparison of direct and indirect matrix converters in induction motor drive. *32nd Annual Conference on Industrial Electronics Society*

Kang, J. K., Hara, H., Yamamoto, E. and Watanabe, E.2002. Analysis and evaluation of bi-directional power switch losses for matrix converter drive. *37th IAS Annual Meeting of Industry Applications Conference.*

Kastner, G. and Rodriguez, J.1985. A forced commutated cycloconverter with control of the source and load currents *EPE,* 1141-1146.

Kazmierkowski, M. P., Krishnan, R. and Blaabjerg, F.2002. Control in power electronics -selected problems, Academic Press.

Kennedy, J.2006. In Search of the essential particle swarm. *Proceedings of the 2006 IEEE Congress on Evolutionary Computations*: 1694–1071.

Kennedy, J. and Mendes, R.2006. Neighborhood topologies in fully informed and best-of-neighborhood particle swarms. *IEEE Transactions on Systems, Man, and Cybernetics—Part C: Applications and Reviews.* **36**(4): 515–519.

Klumpner, C.2006. An indirect matrix converter with a cost effective protection and control. *11th European Conference on Power Electronics and Applications*

Klumpner, C. and Blaabjerg, F.2002. Experimental Evaluation of Ride-Through Capabilities for a Matrix Converter Under Short Power Interruptions. *IEEE Transactions on Industrial Electronics.* **49**(2): 315-324.

Klumpner, C. and Blaabjerg, F.2005. Modulation method for a multiple drive system based on a two-stage direct power conversion topology with reduced input current ripple. *IEEE Transactions on Power Electronics.* **20**: 922-929.

Klumpner, C., Nielsen, P., Boldea, I. and Blaabjerg, F.2000. . New Steps towards a low-cost Power Electronic Building block for Matrix Converters. *IEEE/IAS Annual Meeting 2000*, **3**: 1964-1971.

Klumpner, C., Nielsen, P., Boldea, I. and Blaabjerg, F.2002. A new matrix converter-motor (MCM) for industry applications. *IEEE Transactions on Industrial Electronics.* **49**(2): 325 - 335

Kolar, J. W., Baumann, M., Schafmeister, F. and Ertl, H.2002. Novel three- phase AC– DC–AC sparse matrix converter. *17th Annual IEEE Applied Power Electronics Conference and Exposition*

Kwak, S.2007. Indirect matrix converter drives for unity displacement factor and minimum switching losses. *Electric Power Systems Research.* **77**(5-6): 447–454.

Kwok, N. M., Ha, Q. P., Nguyen, T. H., Li, J. and Samali, B.2006. A novel hysteretic model for magnetorheological fluid dampers and parameter identification using particle swarm optimization. *Sensors and Actuators A: Physical* **132**(2): 441–451.

Kwon, B. H., Min, B. D. and Kim, J. H.2002. Novel commutation technique of AC-AC converters. *IEE Proceedings - Electronics Power Applications.* **145**(4): 295 - 300.

Kwon, W. H. and Cho, G. H. 1993. Analyses of static and dynamic characteristics of practical step-up nine-switch matrix converter. *IEEE Proceedings B.* **140**(2): 139-146.

Lascu, C., Boldea, I. and Blaabjerg, F.2002. A modified direct torque control for induction motor sensorless drive. *IEEE Transactions on Industry Applications.* **36**(1): 122 - 130.

Lee, H. H., Nguyen, H. M., Chun, T. W. and Choi, W. H.2009. Implementation of direct torque control method using matrix converter fed induction motor. *International Forum on Strategic Technology*

Linhart, L., Lettl, J. and Bauer, J.2010. Matrix converter two-step commutation method limitations *14th International Conferenceon Power Electronics and Motion Control*

Liu, W., Li, L. and Cartes, D. A.2007. Binary particle swarm optimization based defensive islanding of large-scale power systems. *International Journal of Computer Science and Applications* **4**(3): 69–83.

Liu, X., Loh, P. C., Peng, F. Z. and Wang, P.2010. Optimal modulation of indirect Z-source matrix converter *International Power Electronics Conference*

Mahlein, J., Bruckmann, M. and Braun, M.2002. Passive protection strategy for a drive system with a matrix converter and an induction machine. *IEEE Transactions on Industrial Electronics.* **49**(2): 297 - 303.

Mahlein, J., Igney, J., Braun, M. and Simon, O.2002. Matrix converter commutation strategies with and without explicit input voltage sign measurement *IEEE Transactions on Industrial Electronics.* **49**(2): 407 - 414

Martin, F.2004. Semikron power electronics. GmbH & Co. KG. Nuremberg, Germany.

Minari, Y., Shinohara, K. and Ueda, R.2002. PWM-rectifier/voltage-source inverter without DC link components for induction motor drive *IEE Proceedings B - Electric Power Applications.* **140**(6): 363 – 368.

Motto, E. R., Donlon, J. F., Tabata, M., Takahashi, H., Yu, Y. and Majumdar, G.2004. Application characteristics of an experimental RB-IGBT (reverse blocking IGBT) module *Industry Applications Conference, 2004. 39th IAS Annual Meeting*, **3**: 1540-1544

Musallam, M. and Johnson, C. M.2011. Impact of different control schemes on the life consumption of power electronic modules for variable speed wind turbines *Proceedings of the 14th European Conference on Power Electronics and Applications,* 1-9

Nath, S., Mohapatra, K. K., Basu, K. and Mohan, N.2010. Source based commutation in matrix converter fed power electronic transformer for power systems application.

Nielsen, P.1996. *The matrix converter for an induction motor drive.* Ph.D.Aalborg University, Denmark.

Nielsen, P., Blaabjerg, F. and Pedersen, J. K.2002. New protection issues of a matrix converter: design considerations for adjustable speed drives. *IEEE Transactions on Industry Applications.* **35**(5): 1150 - 1161.

Park, K. and Lee, K.-B.2009. A novel sparse matrix converter with a Z-source network *35th Annual Conference of IEEE Industrial Electronics.*

Park, K. and Lee, K.-B.2010. A Z-source sparse matrix converter under a voltage sag condition *IEEE Energy Conversion Congress and Exposition.*

Pena, R., Cardenas, R., Reyes, E., Clare, J. and Wheeler, P.2009. A topology for multiple generation system with doubly fed induction machines and indirect matrix converter *IEEE Transactions on Industrial Electronics.* **56**(10): 4181- 4193

Rodriguez, J.1983. A new control technique for AC-AC converters. *IFAC Control in Power Electronics and Electrical Drives Conference,* 203-208.

Rossiter Corrêa, M.B., Jacobina, C.B., Cabral da Silva, E.R. and Lima, A.M.N. 2006. A general PWM strategy for four-switch three-phase inverters. *IEEE Transactions on Power Electronics.* **21**(6). 1618-1627.

Schuster, A.2002. A matrix converter without reactive clamp elements for an induction motor drive system. *29th Annual IEEE Power Electronics Specialist Conference.*

Shi, K. L., Chan, T. F. and Wong, Y. K.2002. Direct self control of induction motor based on neural network. *IEEE Transactions on Industy Applications.* **37**(5): 1290 - 1298.

Svensson, T. and Alaküla, M.1991. The modulation and control of a matrix converter synchronous machine drive. *4th European Conference on Power Electronics and Applications.*

Takeshita, T. and Andou, Y.2010. PWM control of three-phase to three-phase matrix converters for reducing the number of commutations. *Electrical Engineering in Japan*. **170** (2): 60-69.

Tao.2007. *Induction motor direct torque control system simulation.* Master's degree Beijing Jiaotong

Venturini, M.1979. A new high switching rate direct frequency Converter. 2077 a- 79(GB2048588 A).

Venturini, M.1980. A new sine wave in sine wave out conversion technique eliminates reactive elements. *Proceedings of the Powercon* **7**.

Venturini, M. and Alesina, A.1980. The generalized transformer: a new bidirectional sinusoidal waveform converterr with continuously adjustable input power factor. *IEEE Industry Applications Society Annual Meeting,,* 242-252.

Wang, L., Xu, F., Sun, K. and Huang, L.2005. A novel safe shutdown strategy for matrix converter even under fault condition. *20th Annual IEEE Applied Power Electronics Conference and Exposition*

Wei, L. and Lipo, T. A.2004. Investigation of 9-switch dual-bridge matrix converter operating under low output power factor. *38th IAS Annual Meeting Industry Applications Conference*

Wei, L., Lipo, T. A. and Chan, H.2002. Matrix converter topologies with reduced number of switches. *IEEE 33rd Annual Power Electronics Specialist Conference*.

Wei, L., Lipo, T. A. and Chan, H.2003. Robust voltage commutation of conventional matrix converter. *Center for Power Electronics Systems,* 194-199.

Wheeler, P. W.1993. *A matrix converter for variable speed AC motor drives.* Ph.D.University of Bristol, UK.

Wheeler, P. W., Clare, J. C. and Empringham, L.2002. A vector controlled MCT matrix converter induction motor drive with minimized commutation times and enhanced waveform quality. *37th IAS Annual Meeting Industry Applications Conference*

Wheeler, P. W. and Grant, D. A.2002. A low loss matrix converter for AC variable-speed drives. *Fifth European Conference on Power Electronics and Applications*

Wheeler, P. W., Rodriguez, J., Claire, J. C., Empringham, L. and Weinstein, A.2002. Matrix converters : A technology review. *IEEE Transactions on Industrial Electronics*. **49**(2): 276-288.

Xiaohong, W., Yuan, H. and Lianfang, T.2009. Research of control strategy for matrix converter based on space vector modulation. *ISECS International Colloqium on Computing, Communication, Control, and Management*

Xinyi, Z.1994. AC-AC inverter control theory and experimental study. *Power Electronics*. **2**: l-6.

Yoshida, H., Kawata, K., Fukuyama, Y., Takayama, S. and Nakanishi, Y.2001. A particle swarm optimization for reactive power and voltage control considering voltage security assessment. *IEEE Transactions on Power Systems*. **15**(4): 1232–1239.

You, K., Xiao, D., Rahman, M. F. and Uddin, M. N.2011. Applying reduced general direct space vector modulation approach of AC-AC matrix converter theory to achieve unity power factor controlled three-phase AC-DC matrix rectifier *IEEE Industry Applications Society Annual Meeting*

Zaghloul, M. E., Meador, J. L. and Newcomb, R. W., Eds.1994. Silicon Implementation of Pulse Coded Neural Networks. Kluwer Academic Publishers.

Zhang, S., Tseng, K. J. and Nguyen, T. D.2009. Novel three-phase AC-AC Z-source converters using matrix converter theory. *IEEE Energy Conversion Congress and Exposition*

Zhang, W., Liu, W. and Clerc, M.2003. An adaptive PSO algorithm for reactive power optimization. *Proceedings of the Sixth International Conference on Advances in Power System Control, Operation and Management*: 302–307.

Ziegler, M. and Hoffman, W.2000. A new two steps commutation policy for low cost matrix converters. *Exhibition International conference and Exhibition*.

Ziegler, M. and Hoffman, W.2002. Semi natural two steps commutation strategy for matrix converters. *29th Annual IEEE Power Electronics Specialists Control*

Ziogas, P. D., Khan, S. I. and Rashid, M. H.1985. Some improved force commutated cycloconverters structures. *IEEE Transactions on Industry Applications*. **1A-21**(5): 1242-1253

APPENDIX A

MARIX CONVERTER SWITCHING VECTOR

Group	Switching Config. List	Switching Configuration									Switches ON			Output Voltages			Input Currents			Voltage vector		Current Vector	
		S_{au}	S_{bu}	S_{cu}	S_{cv}	S_{bv}	S_{av}	S_{aw}	S_{bw}	S_{cw}				V_u	V_v	V_w	I_a	I_b	I_c	Magnitude (V_o)	Phase (ω_o)	I_i	ω_i
I	+1	1	0	0	0	1	0	0	1	0	S_{au}	S_{bv}	S_{bw}	V_a	0	$-V_a$	I_u	$-I_u$	0	$^{2}/_{3V_a}$	0	$^{2}/_{\sqrt{3i_u}}$	$^{-\pi}/_{6}$
	-1	0	1	0	0	0	1	1	0	0	S_{bu}	S_{av}	S_{aw}	$-V_a$	0	V_a	$-I_u$	I_u	0	$^{-2}/_{3V_a}$	0	$^{-2}/_{\sqrt{3i_u}}$	$^{-\pi}/_{6}$
	+2	0	1	0	1	0	0	0	0	1	S_{bu}	S_{cv}	S_{cw}	V_b	0	$-V_b$	0	I_u	$-I_u$	$^{2}/_{3V_b}$	0	$^{2}/_{\sqrt{3i_u}}$	$^{\pi}/_{2}$
	-2	0	0	1	0	1	0	0	1	0	S_{cu}	S_{bv}	S_{bw}	$-V_b$	0	V_b	0	$-I_u$	I_u	$^{-2}/_{3V_b}$	0	$^{-2}/_{\sqrt{3i_u}}$	$^{\pi}/_{2}$
	+3	0	0	1	0	0	1	1	0	0	S_{cu}	S_{av}	S_{aw}	V_c	0	$-V_c$	$-I_u$	0	I_u	$^{2}/_{3V_c}$	0	$^{2}/_{\sqrt{3i_u}}$	$^{7\pi}/_{6}$
	-3	1	0	0	1	0	0	0	0	1	S_{au}	S_{cv}	S_{cw}	$-V_c$	0	V_c	I_u	0	$-I_u$	$^{-2}/_{3V_c}$	0	$^{-2}/_{\sqrt{3i_u}}$	$^{7\pi}/_{6}$
	+4	0	1	0	0	0	1	0	1	0	S_{bu}	S_{av}	S_{bw}	$-V_a$	V_a	0	I_v	$-I_v$	0	$^{2}/_{3V_a}$	$^{2\pi}/_{3}$	$^{2}/_{\sqrt{3i_v}}$	$^{-\pi}/_{6}$
	-4	1	0	0	0	1	0	1	0	0	S_{au}	S_{bv}	S_{aw}	V_a	$-V_a$	0	$-I_v$	I_v	0	$^{-2}/_{3V_a}$	$^{2\pi}/_{3}$	$^{-2}/_{\sqrt{3i_v}}$	$^{-\pi}/_{6}$
	+5	0	0	1	0	1	0	0	0	1	S_{cu}	S_{bv}	S_{cw}	$-V_b$	V_b	0	0	I_v	$-I_v$	$^{2}/_{3V_b}$	$^{2\pi}/_{3}$	$^{2}/_{\sqrt{3i_v}}$	$^{\pi}/_{2}$
	-5	0	1	0	1	0	0	0	1	0	S_{bu}	S_{cv}	S_{bw}	V_b	$-V_b$	0	0	$-I_v$	I_v	$^{-2}/_{3V_b}$	$^{2\pi}/_{3}$	$^{-2}/_{\sqrt{3i_v}}$	$^{\pi}/_{2}$
	+6	1	0	0	1	0	0	1	0	0	S_{au}	S_{cv}	S_{aw}	$-V_c$	V_c	0	$-I_v$	0	I_v	$^{2}/_{3V_c}$	$^{2\pi}/_{3}$	$^{2}/_{\sqrt{3i_v}}$	$^{7\pi}/_{6}$
	-6	0	0	1	0	0	1	0	0	1	S_{cu}	S_{av}	S_{cw}	V_c	$-V_c$	0	I_v	0	$-I_v$	$^{-2}/_{3V_c}$	$^{2\pi}/_{3}$	$^{-2}/_{\sqrt{3i_v}}$	$^{7\pi}/_{6}$
	+7	0	1	0	0	1	0	1	0	0	S_{bu}	S_{bv}	S_{aw}	0	$-V_a$	V_a	I_w	$-I_w$	0	$^{2}/_{3V_a}$	$^{4\pi}/_{3}$	$^{2}/_{\sqrt{3i_w}}$	$^{-\pi}/_{6}$
	-7	1	0	0	0	0	1	0	1	0	S_{au}	S_{av}	S_{bw}	0	V_a	$-V_a$	$-I_w$	I_w	0	$^{-2}/_{3V_a}$	$^{4\pi}/_{3}$	$^{-2}/_{\sqrt{3i_w}}$	$^{-\pi}/_{6}$
	+8	0	0	1	1	0	0	0	1	0	S_{cu}	S_{cv}	S_{bw}	0	$-V_b$	V_b	0	I_w	$-I_w$	$^{2}/_{3V_b}$	$^{4\pi}/_{3}$	$^{2}/_{\sqrt{3i_w}}$	$^{\pi}/_{2}$
	-8	0	1	0	1	0	0	0	0	1	S_{bu}	S_{bv}	S_{cw}	0	V_b	$-V_b$	0	$-I_w$	I_w	$^{-2}/_{3V_b}$	$^{4\pi}/_{3}$	$^{-2}/_{\sqrt{3i_w}}$	$^{\pi}/_{2}$
	+9	1	0	0	0	0	1	0	0	1	S_{au}	S_{av}	S_{cw}	0	$-V_c$	V_c	$-I_w$	0	I_w	$^{2}/_{3V_c}$	$^{4\pi}/_{3}$	$^{2}/_{\sqrt{3i_w}}$	$^{7\pi}/_{6}$

	-9	0	0	1	1	0	0	1	0	0	S_{cu}	S_{cv}	S_{aw}	0	V_c	$-V_c$	I_w	0	$-I_w$	$^{-2}/_{3V_c}$	$^{4\pi}/_{3}$	$^{-2}/_{\sqrt{3i_w}}$	$^{7\pi}/_{6}$
II	0_a	1	0	0	0	0	1	1	0	0	S_{au}	S_{av}	S_{aw}	0	0	0	0	0	0	0	-	0	-
	0_b	0	1	0	0	1	0	0	1	0	S_{bu}	S_{bv}	S_{bw}	0	0	0	0	0	0	0	-	0	-
	0_c	0	0	1	1	0	0	0	0	1	S_{cu}	S_{cv}	S_{cw}	0	0	0	0	0	0	0	-	0	-
III	X	1	0	0	0	1	0	0	0	1	S_{au}	S_{bv}	S_{cw}	V_a	V_b	V_c	I_u	I_v	I_w	V_i	$\omega_i t$	i_O	$\omega_O t$
	X	1	0	0	1	0	0	0	1	0	S_{au}	S_{cv}	S_{bw}	$-V_c$	$-V_b$	$-V_a$	I_u	I_w	I_v	$-V_i$	$-\omega_i t + {}^{4\pi}/_{3}$	i_O	$-\omega_O t$
	X	0	1	0	1	0	0	1	0	0	S_{bu}	S_{cv}	S_{aw}	$-V_{ab}$	$-V_{ca}$	$-V_{bc}$	I_v	I_u	I_w	$-V_i$	$-\omega_i t$	i_O	$-\omega_O t + {}^{2\pi}/_{3}$
	X	0	1	0	0	0	1	0	0	1	S_{bu}	S_{av}	S_{cw}	V_b	V_c	V_a	I_w	I_u	I_v	V_i	$\omega_i t + {}^{4\pi}/_{3}$	i_O	$\omega_O t + {}^{2\pi}/_{3}$
	X	0	0	1	0	0	1	0	1	0	S_{cu}	S_{av}	S_{bw}	V_c	V_a	V_b	I_v	I_w	I_u	V_i	$\omega_i t + {}^{2\pi}/_{3}$	i_O	$\omega_O t + {}^{4\pi}/_{3}$
	X	0	0	1	0	1	0	1	0	0	S_{cu}	S_{bv}	S_{aw}	$-V_b$	$-V_a$	$-V_c$	I_w	I_v	I_u	$-V_i$	$-\omega_i t + {}^{2\pi}/_{3}$	i_O	$-\omega_O t + {}^{4\pi}/_{3}$

APPENDIX B

C PROGRAMMING

```
/* File    : grt_main.c
 *
 * Abstract:
 *      A Generic "Real-Time (single tasking or pseudo-multitasking,
 *      statically allocated data)" main that runs under most
 *      operating systems.
 *
 *      This file may be a useful starting point when targeting a new
 *      processor or microcontroller.
 *
 *
 * Compiler specified defines:
 *        RT             - Required.
 *      MODEL=modelname - Required.
 *        NUMST=#        - Required. Number of sample times.
 *        NCSTATES=#     - Required. Number of continuous states.
 *      TID01EQ=1 or 0  - Optional. Only define to 1 if sample time task
 *                        id's 0 and 1 have equal rates.
 *      MULTITASKING    - Optional. (use MT for a synonym).
 *        SAVEFILE       - Optional (non-quoted) name of .mat file to create.
 *                         Default is <MODEL>.mat
 *      BORLAND        - Required if using Borland C/C++
 */

#include <float.h>
#include <stdio.h>
#include <stdlib.h>
#include <string.h>
```

```
#include "rtwtypes.h"
# include "rtmodel.h"
#include "rt_sim.h"
#include "rt_logging.h"
#ifdef UseMMIDataLogging
#include "rt_logging_mmi.h"
#endif
#include "rt_nonfinite.h"

/* Signal Handler header */
#ifdef BORLAND
#include <signal.h>
#include <float.h>
#endif

#include "ext_work.h"



/*=========*
 * Defines *
 *=========*/

#ifndef TRUE
#define FALSE (0)
#define TRUE  (1)
#endif

#ifndef EXIT_FAILURE
#define EXIT_FAILURE  1
#endif
#ifndef EXIT_SUCCESS
```

```
#define EXIT_SUCCESS  0
#endif

#define QUOTE1(name) #name
#define QUOTE(name) QUOTE1(name)    /* need to expand name    */

#ifndef RT
# error "must define RT"
#endif

#ifndef MODEL
# error "must define MODEL"
#endif

#ifndef NUMST
# error "must define number of sample times, NUMST"
#endif

#ifndef NCSTATES
# error "must define NCSTATES"
#endif

#ifndef SAVEFILE
# define MATFILE2(file) #file ".mat"
# define MATFILE1(file) MATFILE2(file)
# define MATFILE MATFILE1(MODEL)
#else
# define MATFILE QUOTE(SAVEFILE)
#endif

#define RUN_FOREVER -1.0

#define EXPAND_CONCAT(name1,name2) name1 ## name2
```

```
#define CONCAT(name1,name2) EXPAND_CONCAT(name1,name2)
#define RT_MODEL            CONCAT(MODEL,_rtModel)

/*====================*
 * External functions *
 *====================*/
#ifdef __cplusplus

extern "C" {

#endif

extern RT_MODEL *MODEL(void);

extern void MdlInitializeSizes(void);
extern void MdlInitializeSampleTimes(void);
extern void MdlStart(void);
extern void MdlOutputs(int_T tid);
extern void MdlUpdate(int_T tid);
extern void MdlTerminate(void);

#ifdef __cplusplus

}
#endif

#if NCSTATES > 0
#ifdef __cplusplus

extern "C" {

#endif
  extern void rt_ODECreateIntegrationData(RTWSolverInfo *si);
```

```
  extern void rt_ODEUpdateContinuousStates(RTWSolverInfo *si);
#ifdef __cplusplus

}
#endif

# define rt_CreateIntegrationData(S) \
    rt_ODECreateIntegrationData(rtmGetRTWSolverInfo(S));
# define rt_UpdateContinuousStates(S) \
    rt_ODEUpdateContinuousStates(rtmGetRTWSolverInfo(S));
# else
# define rt_CreateIntegrationData(S)  \
     rtsiSetSolverName(rtmGetRTWSolverInfo(S),"FixedStepDiscrete");
# define rt_UpdateContinuousStates(S) /* Do Nothing */
#endif



/*==================================*
 * Global data local to this module *
 *==================================*/

static struct {
  int_T    stopExecutionFlag;
  int_T    isrOverrun;
  int_T    overrunFlags[NUMST];
  int_T    eventFlags[NUMST];
  const    char_T *errmsg;
} GBLbuf;



#ifdef EXT_MODE
#  define rtExtModeSingleTaskUpload(S)                    \
   {                                                      \
```

```
        int stIdx;                                  \
        rtExtModeUploadCheckTrigger(rtmGetNumSampleTimes(S));   \
        for (stIdx=0; stIdx<NUMST; stIdx++) {               \
          if (rtmIsSampleHit(S, stIdx, 0 /*unused*/)) {       \
            rtExtModeUpload(stIdx,rtmGetTaskTime(S,stIdx)); \
          }                                         \
        }                                           \
      }
#else
#  define rtExtModeSingleTaskUpload(S) /* Do nothing */
#endif

/*==================*
 * Local functions *
 *==================*/

#ifdef BORLAND
/* Implemented for BC++ only*/

typedef void (*fptr)(int, int);

/*                          Function:                          divideByZero
=====================================================
 *
 * Abstract: Traps the error Division by zero and prints a warning
 *          Also catches other FP errors, but does not identify them
 *          specifically.
 */
void divideByZero(int sigName, int sigType)
{
   signal(SIGFPE, (fptr)divideByZero);
   if ((sigType == FPE_ZERODIVIDE)||(sigType == FPE_INTDIV0)){
      printf("*** Warning: Division by zero\n\n");
```

```
            return;
        }
        else{
            printf("*** Warning: Floating Point error\n\n");
            return;
        }
    } /* end divideByZero */

    #endif /* BORLAND */

    #if !defined(MULTITASKING)  /* SINGLETASKING */

    /*                                Function:                                rtOneStep
=========================================================
     *
     * Abstract:
     *      Perform one step of the model. This function is modeled such that
     *      it could be called from an interrupt service routine (ISR) with minor
     *      modifications.
     */
    static void rt_OneStep(RT_MODEL *S)
    {
        real_T tnext;

        /*********************************************
         * Check and see if base step time is too fast *
         *********************************************/
        if (GBLbuf.isrOverrun++) {
            GBLbuf.stopExecutionFlag = 1;
            return;
        }

        /*********************************************
```

```
 * Check and see if error status has been set  *
 *********************************************/
if (rtmGetErrorStatus(S) != NULL) {
   GBLbuf.stopExecutionFlag = 1;
   return;
}

/* enable interrupts here */

/*
 * In a multi-tasking environment, this would be removed from the base rate
 * and called as a "background" task.
 */
rtExtModeOneStep(rtmGetRTWExtModeInfo(S),
                 rtmGetNumSampleTimes(S),
                 (boolean_T *)&rtmGetStopRequested(S));

tnext = rt_SimGetNextSampleHit();
rtsiSetSolverStopTime(rtmGetRTWSolverInfo(S),tnext);

MdlOutputs(0);

rtExtModeSingleTaskUpload(S);

GBLbuf.errmsg = rt_UpdateTXYLogVars(rtmGetRTWLogInfo(S),
                                    rtmGetTPtr(S));
if (GBLbuf.errmsg != NULL) {
   GBLbuf.stopExecutionFlag = 1;
   return;
}

rt_UpdateSigLogVars(rtmGetRTWLogInfo(S), rtmGetTPtr(S));
```

```
    MdlUpdate(0);
    rt_SimUpdateDiscreteTaskSampleHits(rtmGetNumSampleTimes(S),
                                       rtmGetTimingData(S),
                                       rtmGetSampleHitPtr(S),
                                       rtmGetTPtr(S));

    if (rtmGetSampleTime(S,0) == CONTINUOUS_SAMPLE_TIME) {
      rt_UpdateContinuousStates(S);
    }

    GBLbuf.isrOverrun--;

    rtExtModeCheckEndTrigger();

  } /* end rtOneStep */

  #else /* MULTITASKING */

  # if TID01EQ == 1
  #  define FIRST_TID 1
  # else
  #  define FIRST_TID 0
  # endif

  /*                                Function:                                rtOneStep
  ========================================================================
   *
   * Abstract:
   *      Perform one step of the model. This function is modeled such that
   *      it could be called from an interrupt service routine (ISR) with minor
   *      modifications.
   *
   *      This routine is modeled for use in a multitasking environment and
```

```
 *         therefore needs to be fully re-entrant when it is called from an
 *         interrupt service routine.
 *
 * Note:
 *      Error checking is provided which will only be used if this routine
 *      is attached to an interrupt.
 *
 */
static void rt_OneStep(RT_MODEL *S)
{
    int_T  i;
    real_T tnext;
    int_T  *sampleHit = rtmGetSampleHitPtr(S);

    /*************************************************
     * Check and see if base step time is too fast *
     *************************************************/
    if (GBLbuf.isrOverrun++) {
        GBLbuf.stopExecutionFlag = 1;
        return;
    }

    /*************************************************
     * Check and see if error status has been set  *
     *************************************************/
    if (rtmGetErrorStatus(S) != NULL) {
        GBLbuf.stopExecutionFlag = 1;
        return;
    }
    /* enable interrupts here */

    /*
     * In a multi-tasking environment, this would be removed from the base rate
```

```
 * and called as a "background" task.
 */
rtExtModeOneStep(rtmGetRTWExtModeInfo(S),
                 rtmGetNumSampleTimes(S),
                 (boolean_T *)&rtmGetStopRequested(S));

/*********************************************
 * Update discrete events                    *
 *********************************************/
tnext = rt_SimUpdateDiscreteEvents(rtmGetNumSampleTimes(S),
                                   rtmGetTimingData(S),
                                   rtmGetSampleHitPtr(S),
                                   rtmGetPerTaskSampleHitsPtr(S));
rtsiSetSolverStopTime(rtmGetRTWSolverInfo(S),tnext);
for (i=FIRST_TID+1; i < NUMST; i++) {
   if (sampleHit[i] && GBLbuf.eventFlags[i]++) {
      GBLbuf.isrOverrun--;
      GBLbuf.overrunFlags[i]++;    /* Are we sampling too fast for */
      GBLbuf.stopExecutionFlag=1;  /*   sample time "i"?           */
      return;
   }
}
/*********************************************
 * Step the model for the base sample time *
 *********************************************/
MdlOutputs(FIRST_TID);

rtExtModeUploadCheckTrigger(rtmGetNumSampleTimes(S));
rtExtModeUpload(FIRST_TID,rtmGetTaskTime(S, FIRST_TID));

GBLbuf.errmsg = rt_UpdateTXYLogVars(rtmGetRTWLogInfo(S),
                                    rtmGetTPtr(S));
if (GBLbuf.errmsg != NULL) {
```

```
            GBLbuf.stopExecutionFlag = 1;
            return;
          }

          rt_UpdateSigLogVars(rtmGetRTWLogInfo(S), rtmGetTPtr(S));

          MdlUpdate(FIRST_TID);

          if (rtmGetSampleTime(S,0) == CONTINUOUS_SAMPLE_TIME) {
            rt_UpdateContinuousStates(S);
          }
           else {
            rt_SimUpdateDiscreteTaskTime(rtmGetTPtr(S),
                                  rtmGetTimingData(S), 0);
          }

        #if FIRST_TID == 1
          rt_SimUpdateDiscreteTaskTime(rtmGetTPtr(S),
                                rtmGetTimingData(S),1);
        #endif


/*********************************************************************
**
           * Model step complete for base sample time, now it is okay to        *
           * re-interrupt this ISR.                                              *

*********************************************************************
**/

          GBLbuf.isrOverrun--;
```

```
    /*********************************************
     * Step the model for any other sample times *
     *********************************************/
    for (i=FIRST_TID+1; i<NUMST; i++) {
      /* If task "i" is running, don't run any lower priority task */
      if (GBLbuf.overrunFlags[i]) return;

      if (GBLbuf.eventFlags[i]) {
        GBLbuf.overrunFlags[i]++;

        MdlOutputs(i);

        rtExtModeUpload(i, rtmGetTaskTime(S,i));

        MdlUpdate(i);

        rt_SimUpdateDiscreteTaskTime(rtmGetTPtr(S),
                                     rtmGetTimingData(S),i);

        /* Indicate task complete for sample time "i" */
        GBLbuf.overrunFlags[i]--;
        GBLbuf.eventFlags[i]--;
      }
    }

    rtExtModeCheckEndTrigger();

} /* end rtOneStep */

#endif /* MULTITASKING */
```

```
static void displayUsage (void)
{
  (void) printf("usage: %s -tf <finaltime> -w -port
<TCPport>\n",QUOTE(MODEL));
  (void) printf("arguments:\n");
  (void) printf("  -tf <finaltime> - overrides final time specified in "
          "Simulink (inf for no limit).\n");
  (void) printf("  -w          - waits for Simulink to start model "
          "in External Mode.\n");
  (void) printf("  -port <TCPport> - overrides 17725 default port in "
          "External Mode, valid range 256 to 65535.\n");
}

/*====================*
 * Visible functions *
 *====================*/

/*                                Function:                                main
=============================================================
 *
 * Abstract:
 *      Execute model on a generic target such as a workstation.
 */
int_T main(int_T argc, const char_T *argv[])
{
  RT_MODEL  *S;
  const char *status;
  real_T     finaltime = -2.0;

  int_T  oldStyle_argc;
  const char_T *oldStyle_argv[5];
```

```
    /*******************************
     * MathError Handling for BC++ *
     *******************************/
#ifdef BORLAND
    signal(SIGFPE, (fptr)divideByZero);
#endif

    /********************
     * Parse arguments *
     ********************/
    if ((argc > 1) && (argv[1][0] != '-')) {
        /* old style */
        if ( argc > 3 ) {
            displayUsage();
            exit(EXIT_FAILURE);
        }

        oldStyle_argc    = 1;
        oldStyle_argv[0] = argv[0];

        if (argc >= 2) {
            oldStyle_argc = 3;

            oldStyle_argv[1] = "-tf";
            oldStyle_argv[2] = argv[1];
        }

        if (argc == 3) {
            oldStyle_argc = 5;

            oldStyle_argv[3] = "-port";
            oldStyle_argv[4] = argv[2];
```

```
    }

    argc = oldStyle_argc;
    argv = oldStyle_argv;

}

{
    /* new style: */
    double    tmpDouble;
    char_T tmpStr2[200];
    int_T  count      = 1;
    int_T  parseError = FALSE;

    /*
     * Parse the standard RTW parameters.  Let all unrecognized parameters
     * pass through to external mode for parsing.  NULL out all args handled
     * so that the external mode parsing can ignore them.
     */
    while(count < argc) {
        const char_T *option = argv[count++];

        /* final time */
        if ((strcmp(option, "-tf") == 0) && (count != argc)) {
            const char_T *tfStr = argv[count++];

            sscanf(tfStr, "%200s", tmpStr2);
            if (strcmp(tmpStr2, "inf") == 0) {
                tmpDouble = RUN_FOREVER;
            } else {
                char_T tmpstr[2];

                if ( (sscanf(tmpStr2,"%lf%1s", &tmpDouble, tmpstr) != 1) ||
```

```
            (tmpDouble < 0.0) ) {
            (void)printf("finaltime must be a positive, real value or inf\n");
            parseError = TRUE;
            break;
        }
    }
    finaltime = (real_T) tmpDouble;

    argv[count-2] = NULL;
    argv[count-1] = NULL;
  }
}

if (parseError) {
  (void)printf("\nUsage: %s -option1 val1 -option2 val2 -option3 "
               "...\n\n", QUOTE(MODEL));
  (void)printf("\t-tf 20 - sets final time to 20 seconds\n");

  exit(EXIT_FAILURE);
}

rtExtModeParseArgs(argc, argv, NULL);

/*
 * Check for unprocessed ("unhandled") args.
 */
{
  int i;
  for (i=1; i<argc; i++) {
    if (argv[i] != NULL) {
      printf("Unexpected command line argument: %s\n",argv[i]);
      exit(EXIT_FAILURE);
    }
```

```
        }
      }
    }

    /*****************************
     * Initialize global memory *
     *****************************/
    (void)memset(&GBLbuf, 0, sizeof(GBLbuf));

    /*************************
     * Initialize the model *
     *************************/
    rt_InitInfAndNaN(sizeof(real_T));

    S = MODEL();
    if (rtmGetErrorStatus(S) != NULL) {
      (void)fprintf(stderr,"Error during model registration: %s\n",
                    rtmGetErrorStatus(S));
      exit(EXIT_FAILURE);
    }
    if (finaltime >= 0.0 || finaltime == RUN_FOREVER)
rtmSetTFinal(S,finaltime);

    MdlInitializeSizes();
    MdlInitializeSampleTimes();

    status = rt_SimInitTimingEngine(rtmGetNumSampleTimes(S),
                                    rtmGetStepSize(S),
                                    rtmGetSampleTimePtr(S),
                                    rtmGetOffsetTimePtr(S),
                                    rtmGetSampleHitPtr(S),
                                    rtmGetSampleTimeTaskIDPtr(S),
                                    rtmGetTStart(S),
```

```
                                &rtmGetSimTimeStep(S),
                                &rtmGetTimingData(S));

    if (status != NULL) {
      (void)fprintf(stderr,
            "Failed to initialize sample time engine: %s\n", status);
      exit(EXIT_FAILURE);
    }
    rt_CreateIntegrationData(S);

  #ifdef UseMMIDataLogging

rt_FillStateSigInfoFromMMI(rtmGetRTWLogInfo(S),&rtmGetErrorStatus(S));

rt_FillSigLogInfoFromMMI(rtmGetRTWLogInfo(S),&rtmGetErrorStatus(S));
  #endif
    GBLbuf.errmsg = rt_StartDataLogging(rtmGetRTWLogInfo(S),
                                rtmGetTFinal(S),
                                rtmGetStepSize(S),
                                &rtmGetErrorStatus(S));
    if (GBLbuf.errmsg != NULL) {
      (void)fprintf(stderr,"Error starting data logging: %s\n",GBLbuf.errmsg);
      return(EXIT_FAILURE);
    }

    rtExtModeCheckInit(rtmGetNumSampleTimes(S));
    rtExtModeWaitForStartPkt(rtmGetRTWExtModeInfo(S),
                        rtmGetNumSampleTimes(S),
                        (boolean_T *)&rtmGetStopRequested(S));

    (void)printf("\n** starting the model **\n");

    MdlStart();
```

```
        if (rtmGetErrorStatus(S) != NULL) {
          GBLbuf.stopExecutionFlag = 1;
        }


/*********************************************************************
***
         * Execute the model.  You may attach rtOneStep to an ISR, if so replace *
         * the call to rtOneStep (below) with a call to a background task       *
         * application.                                                         *

*********************************************************************
***/
        if (rtmGetTFinal(S) == RUN_FOREVER) {
          printf ("\n**May run forever. Model stop time set to infinity.**\n");
        }

        while (!GBLbuf.stopExecutionFlag &&
               (rtmGetTFinal(S) == RUN_FOREVER ||
                rtmGetTFinal(S)-rtmGetT(S) > rtmGetT(S)*DBL_EPSILON)) {

          rtExtModePauseIfNeeded(rtmGetRTWExtModeInfo(S),
                                 rtmGetNumSampleTimes(S),
                                 (boolean_T *)&rtmGetStopRequested(S));

          if (rtmGetStopRequested(S)) break;
          rt_OneStep(S);
        }

        if (!GBLbuf.stopExecutionFlag && !rtmGetStopRequested(S)) {
          /* Execute model last time step */
          rt_OneStep(S);
        }
```

```
    /*********************
     * Cleanup and exit *
     *********************/
#ifdef UseMMIDataLogging
    rt_CleanUpForStateLogWithMMI(rtmGetRTWLogInfo(S));
    rt_CleanUpForSigLogWithMMI(rtmGetRTWLogInfo(S));
#endif
    rt_StopDataLogging(MATFILE,rtmGetRTWLogInfo(S));

    rtExtModeShutdown(rtmGetNumSampleTimes(S));

    if (GBLbuf.errmsg) {
        (void)fprintf(stderr,"%s\n",GBLbuf.errmsg);
        exit(EXIT_FAILURE);
    }

    if (rtmGetErrorStatus(S) != NULL) {
        (void)fprintf(stderr,"ErrorStatus set: \"%s\"\n", rtmGetErrorStatus(S));
        exit(EXIT_FAILURE);
    }

    if (GBLbuf.isrOverrun) {
        (void)fprintf(stderr,
                      "%s: ISR overrun - base sampling rate is too fast\n",
                      QUOTE(MODEL));
        exit(EXIT_FAILURE);
    }

#ifdef MULTITASKING
    else {
        int_T i;
        for (i=1; i<NUMST; i++) {
```

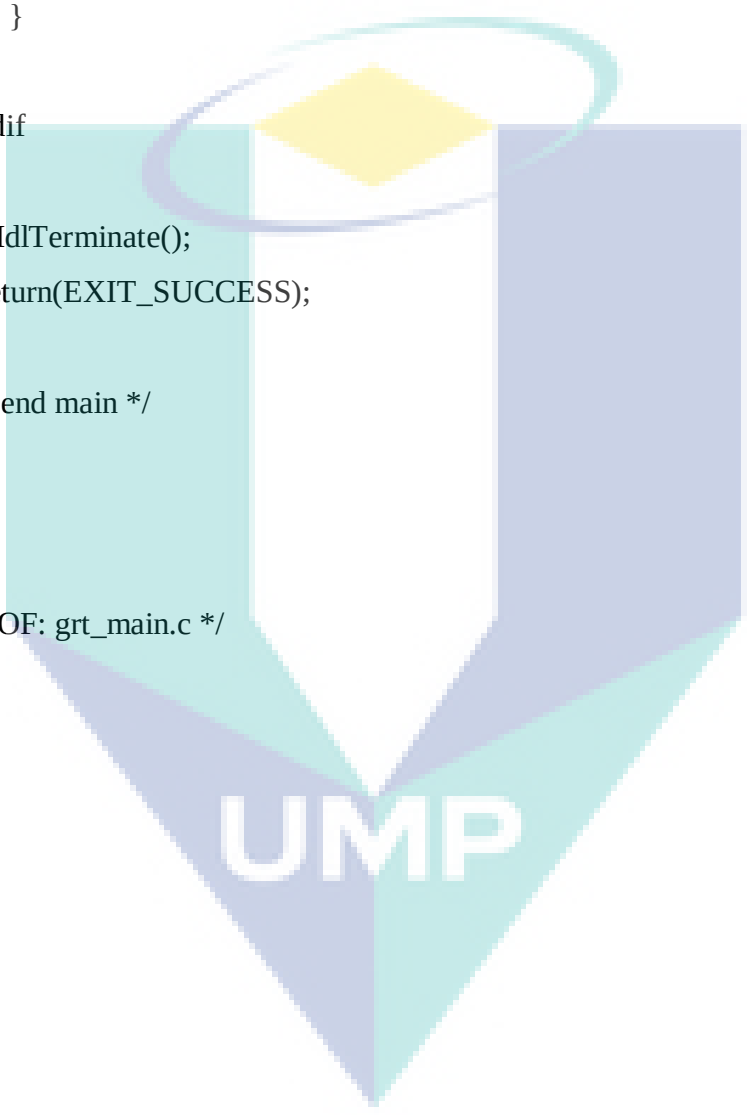
```
            if (GBLbuf.overrunFlags[i]) {
                (void)fprintf(stderr,
                      "%s ISR overrun - sampling rate is too fast for "
                      "sample time index %d\n", QUOTE(MODEL), i);
                exit(EXIT_FAILURE);
            }
        }
    }
#endif

    MdlTerminate();
    return(EXIT_SUCCESS);

} /* end main */



/* EOF: grt_main.c */
```



APPENDIX C

STANDARD OPERATION PROCEDURE OF THE RESEARCH

1. Perform a physical and mathematical modeling on *Matlab/Simulink*. The modeling was done by using the *Power Systems* toolbox.

2. Upload the mathematical modeling into TMS320F28335 and the gate trigger signal was obtained at port P2.3, P2.4, P2.5, P2.6, P2.40, P2.43, P2.44, P2.46 and P2.47. The signals are shown in Figure C.1.

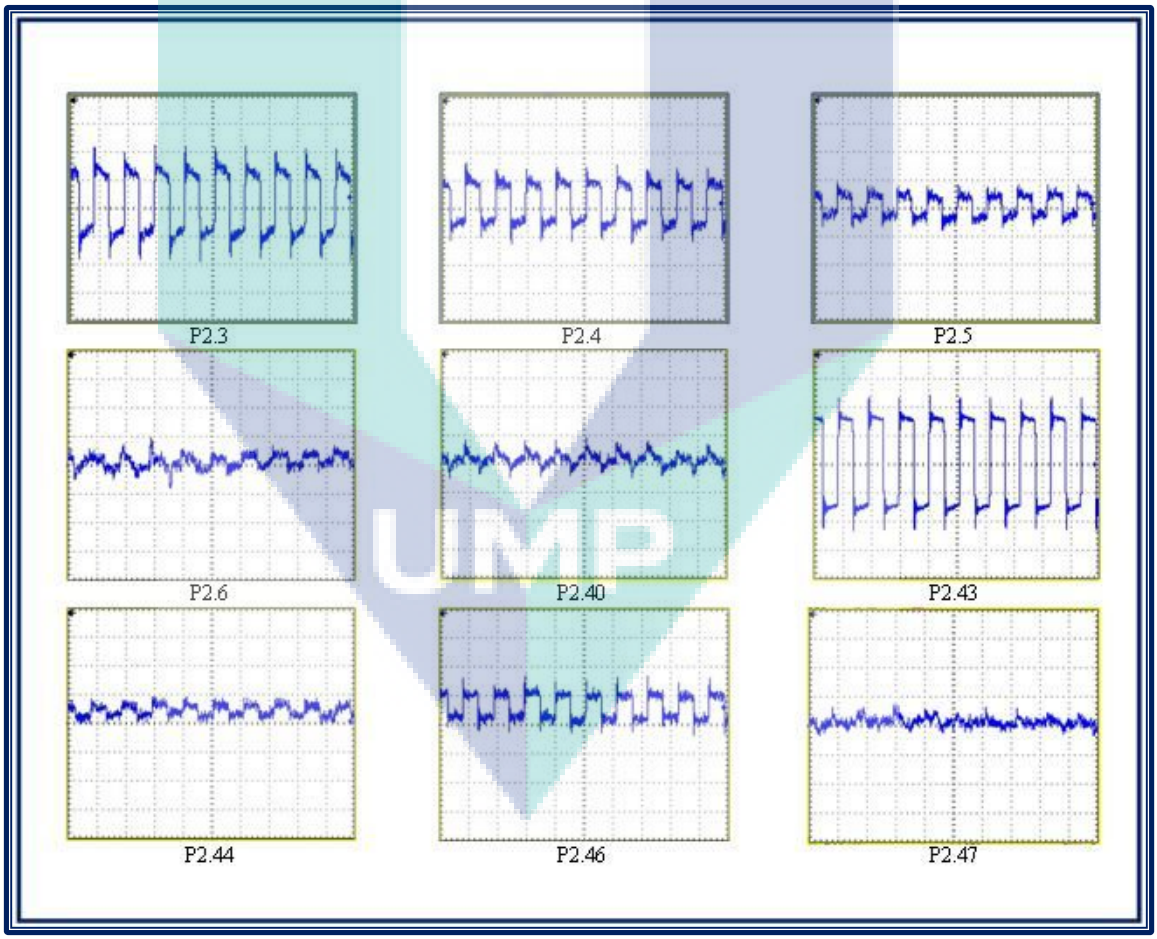


Figure C.1: Gate trigger signal

3. The pin connection from TMS320F28335 is connected to the *Semikron* IGBT driver as in Figure C.2.

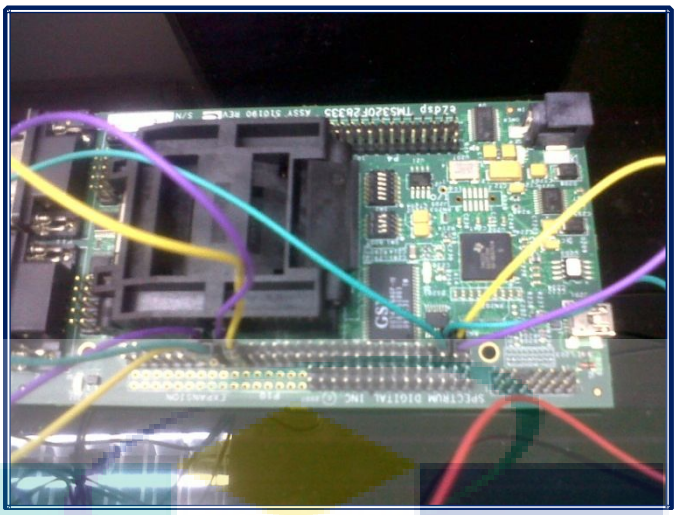


Figure C.2: Digital signal processing TMS320F28335

4. Construct the three-phase MC hardware. The construction included the 18 IGBT switches with freewheeling diodes, clamping circuit and six pack IGBT gate drivers. The IGBT switches hardware is shown in Figure C.3.

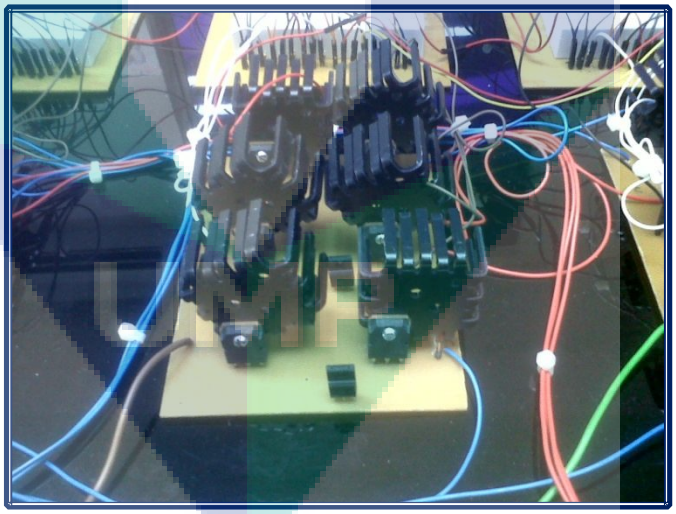


Figure C.3: 18 IGBT switches

5. The clamping is constructed from 12 ultrafast rectifier diodes, a capacitor and a varistor. It is practical in preventing the short-circuit of the inductive load by suppressing the high pressure generated from the output. A combination switch structure known as over-voltage snubber circuit was inserted between the input and output terminal of the clamping circuit. The varistor provides the energy release for

the capacitor circuit which guarantees the clamp circuit does not inhibit the output voltage. The clamping circuit is shown in Figure C.4.

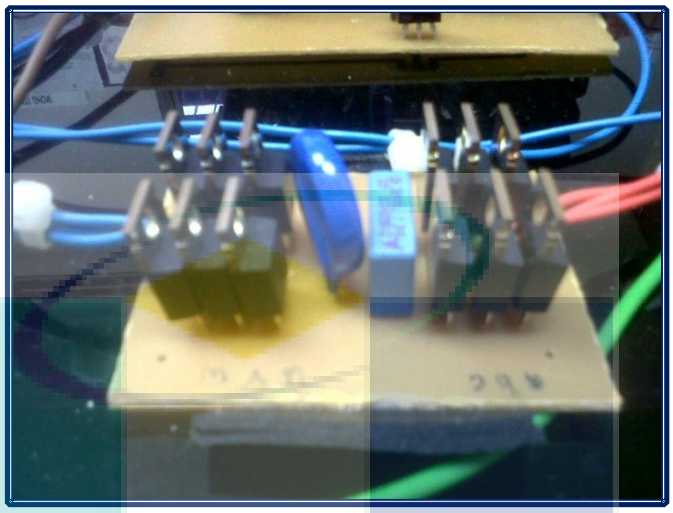


Figure C.4: Clamping circuit

6. The 18 IGBT gates were triggered by the *Semikron* IGBT driver as in Figure C.5. This driver is CMOS compatible and the signals were transmitted by the optocouplers which protects from the short-circuit.

Figure C.5: Six pack IGBT gate driver

7. The three-phase input of the IGBT is connected to the three-phase supply with star connection. The output was connected to the induction motor. The current and voltage waveform was measured using the *Tektronix* digital oscilloscope.

APPENDIX D

Hardware Equipment Datasheet

D.1. Silicon N-channel IGBT

D.2. IGBT and MOSFET driver

D.3. Ultrafast rectifier diode

D.4. Damper diode

D.5. DSP TMS320F28335

APPENDIX D.1

TOSHIBA GT10Q101

TOSHIBA Insulated Gate Bipolar Transistor Silicon N Channel IGBT

GT10Q101

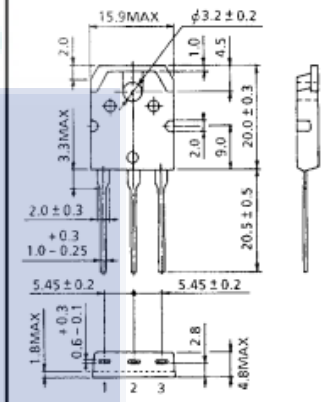
High Power Switching Applications

- The 3rd Generation
- Enhancement-Mode
- High Speed: t_f = 0.32 μs (max)
- Low Saturation Voltage: $V_{CE\ (sat)}$ = 2.7 V (max)

Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Collector-emitter voltage		V_{CES}	1200	V
Gate-emitter voltage		V_{GES}	±20	V
Collector current	DC	I_C	10	A
	1 ms	I_{CP}	20	
Collector power dissipation (Tc = 25°C)		P_C	140	W
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Unit: mm



1. GATE
2. COLLECTOR (HEAT SINK)
3. EMITTER

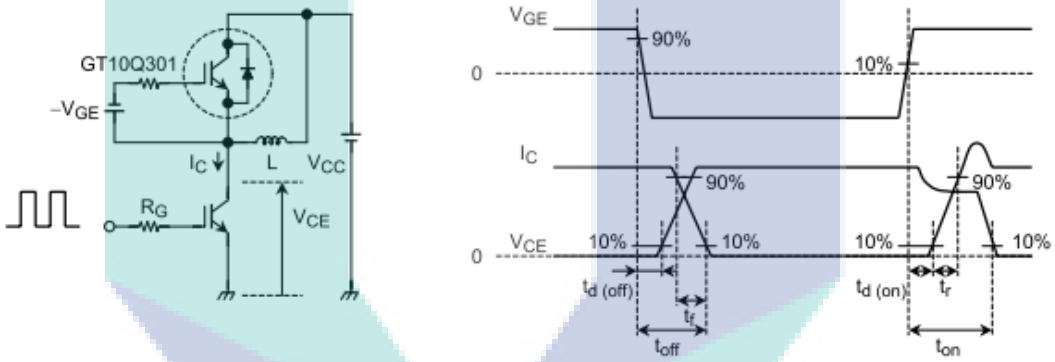
JEDEC	—
JEITA	—
TOSHIBA	2-16C1C

Weight: 4.6 g (typ.)

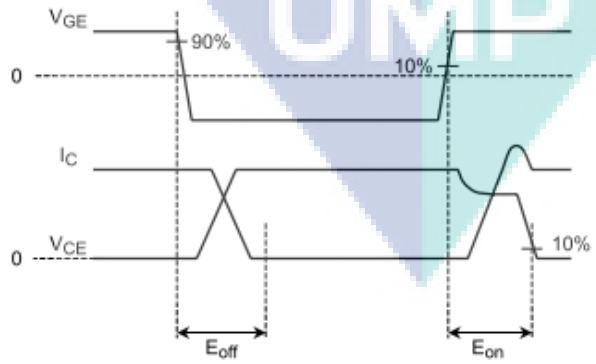
Electrical Characteristics (Ta = 25°C)

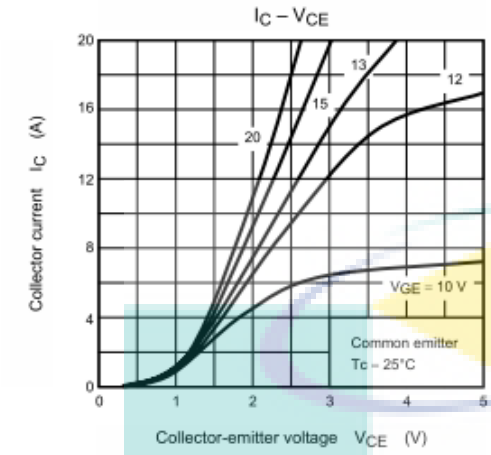
Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GES}	V_{GE} = ±20 V, V_{CE} = 0	—	—	±500	nA
Collector cut-off current		I_{CES}	V_{CE} = 1200 V, V_{GE} = 0	—	—	1.0	mA
Gate-emitter cut-off voltage		$V_{GE\ (OFF)}$	I_C = 1 mA, V_{CE} = 5 V	4.0	—	7.0	V
Collector-emitter saturation voltage		$V_{CE\ (sat)}$	I_C = 10 A, V_{GE} = 15 V	—	2.1	2.7	V
Input capacitance		C_{ies}	V_{CE} = 50 V, V_{GE} = 0, f = 1 MHz	—	600	—	pF
Switching time	Rise time	t_r	Inductive Load V_{CC} = 600 V, I_C = 10 A V_{GG} = ±15 V, R_G = 75 Ω (Note1)	—	0.07	—	μs
	Turn-on time	t_{on}		—	0.30	—	
	Fall time	t_f		—	0.16	0.32	
	Turn-off time	t_{off}		—	0.50	—	
Thermal resistance		$R_{th\ (j\text{-}c)}$	—	—	—	0.89	°C/W

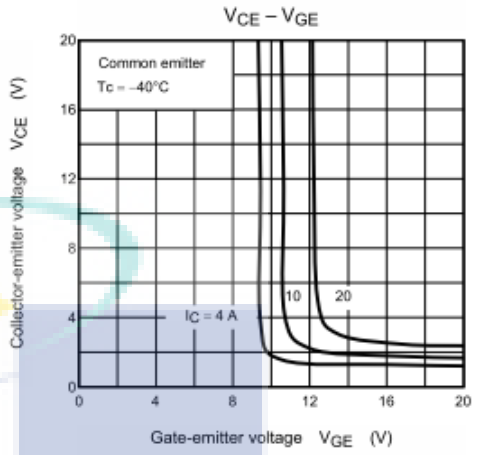
Note1: Switching time measurement circuit and input/output waveforms

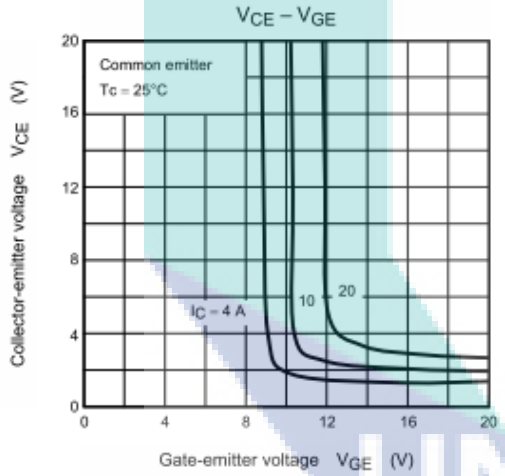


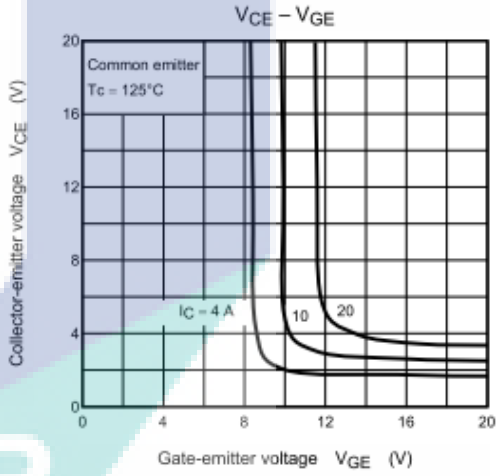
Note2: Switching loss measurement waveforms

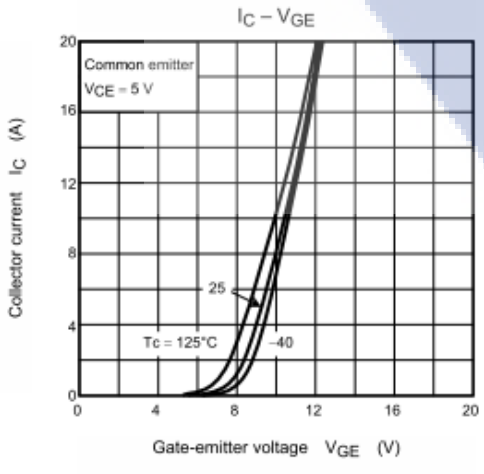


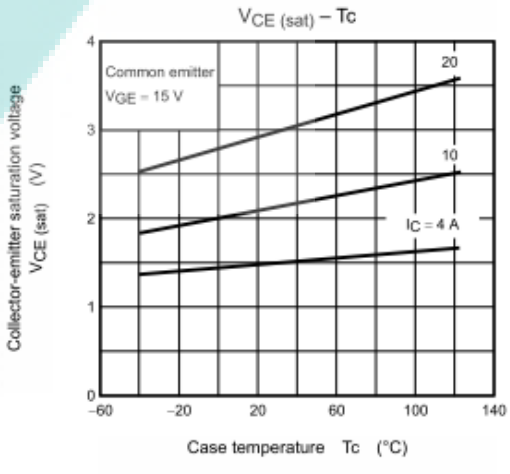

$I_C - V_{CE}$
Collector current I_C (A)
Collector-emitter voltage V_{CE} (V)
20
16
12
8
4
0
0
1
2
3
4
5
13
15
20
12
V_{GE} = 10 V
Common emitter
Tc = 25°C


$V_{CE} - V_{GE}$
Collector-emitter voltage V_{CE} (V)
Gate-emitter voltage V_{GE} (V)
Common emitter
Tc = −40°C
I_C = 4 A
10
20
0
4
8
12
16
20

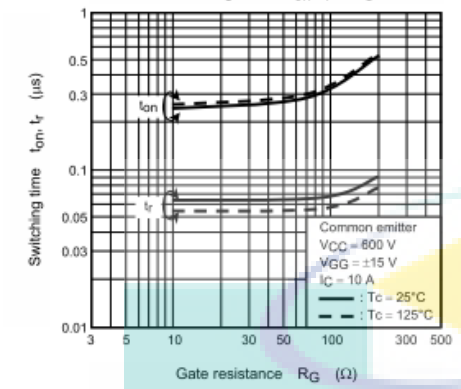

$V_{CE} - V_{GE}$
Collector-emitter voltage V_{CE} (V)
Gate-emitter voltage V_{GE} (V)
Common emitter
Tc = 25°C
I_C = 4 A
10
20
0
4
8
12
16
20


$V_{CE} - V_{GE}$
Collector-emitter voltage V_{CE} (V)
Gate-emitter voltage V_{GE} (V)
Common emitter
Tc = 125°C
I_C = 4 A
10
20
0
4
8
12
16
20

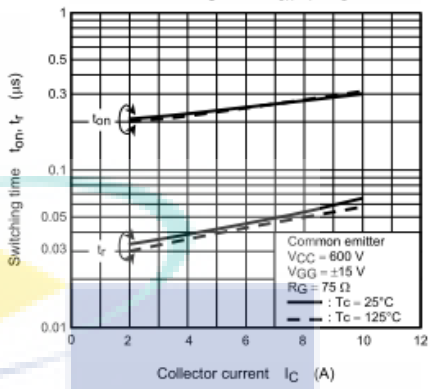

$I_C - V_{GE}$
Collector current I_C (A)
Gate-emitter voltage V_{GE} (V)
Common emitter
V_{CE} = 5 V
Tc = 125°C
25
−40
0
4
8
12
16
20


$V_{CE\ (sat)} - Tc$
Collector-emitter saturation voltage $V_{CE\ (sat)}$ (V)
Case temperature Tc (°C)
Common emitter
V_{GE} = 15 V
I_C = 4 A
20
10
0
1
2
3
4
−60
−20
20
60
100
140

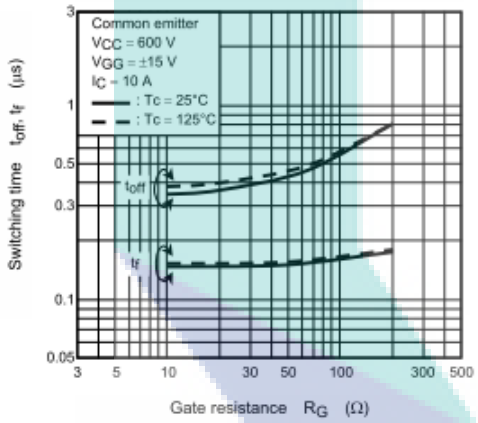
Switching time t_{on}, t_r – R_G



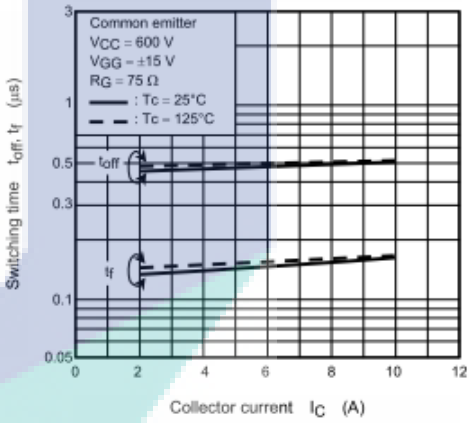
Switching time t_{on}, t_r – I_C



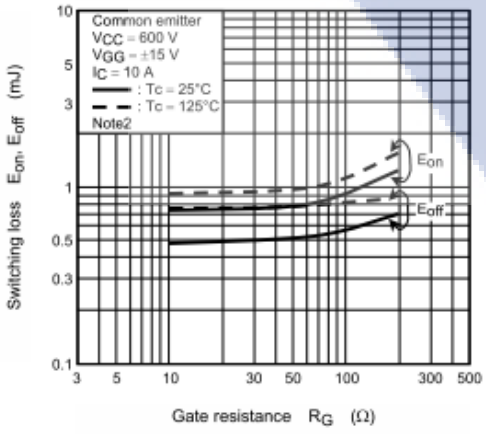
Switching time t_{off}, t_f – R_G



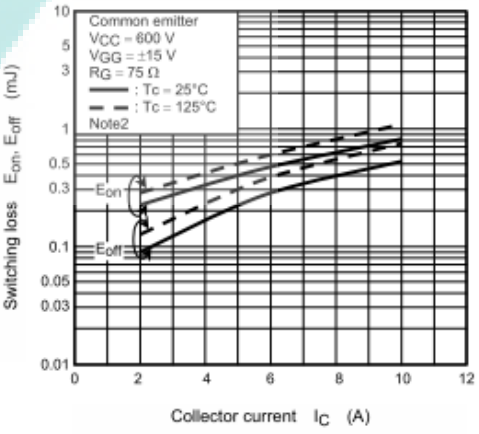
Switching time t_{off}, t_f – I_C



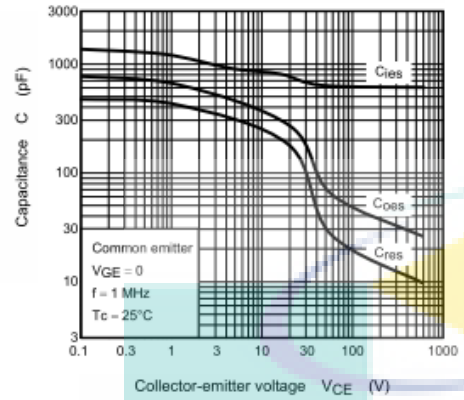
Switching loss E_{on}, E_{off} – R_G



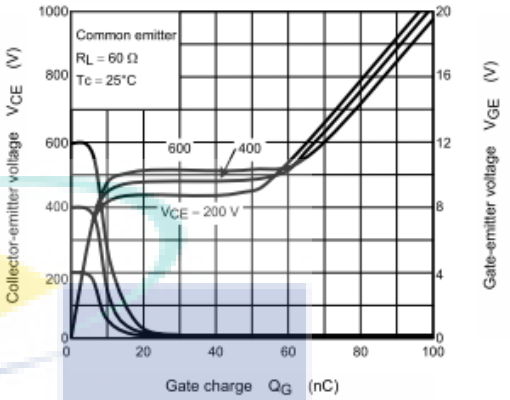
Switching loss E_{on}, E_{off} – I_C



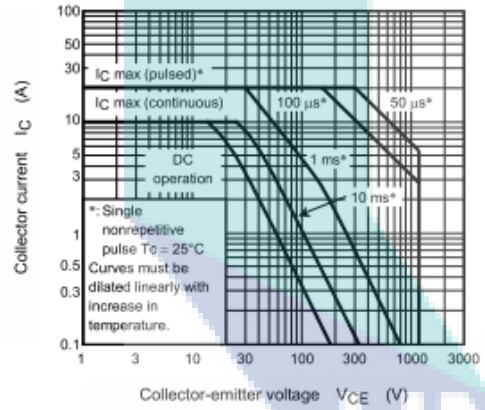
C – V_{CE}



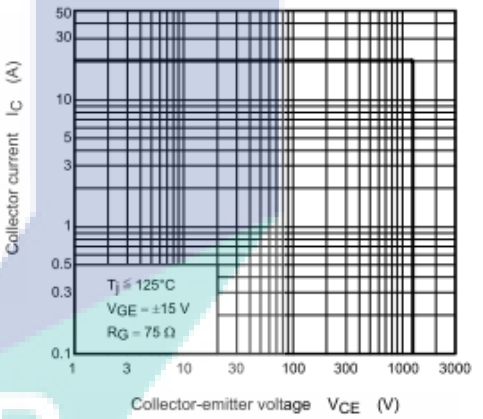
V_{CE}, V_{GE} – Q_G



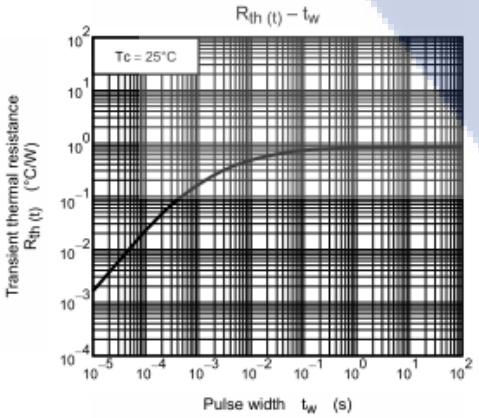
Safe operating area



Reverse bias SOA



$R_{th\ (t)}$ – t_w



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000707EAA

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APPENDIX D.2

SKHI 61 (R) ...

SEMIDRIVER™

Sixpack IGBT and MOSFET Driver

SKHI 61 (R)

Features

- CMOS-compatible input buffers at V_{DD}=5V
- Short-circuit protection by V_{CE}-monitoring and Soft-turn-Off
- Drive interlock top/bottom
- Signal transmission by opto-couplers
- Supply undervoltage protection (13V)
- Error latch / output

Typical Applications

- Driver for IGBT and MOSFET modules in three-phase-bridge circuits, inverter drives, UPS-facilities, etc.

1) At T_a < -25°C the current consumption can be 1,6 times the rated maximum current for the first three operating minutes.

Absolute Maximum Ratings

Symbol	Conditions	Values	Units
V_S	Supply voltage primary	15,6	V
V_{iH}	Input signal voltage	V_S + 0,3	V
$Iout_{PEAK}$	Output peak current	2	A
$Iout_{AVmax}$	Output average current (T_a = 85 °C)	20	mA
f_{max}	Max. switching frequency (C_{GE} < 9nF)	50	kHz
V_{CE}	Collector emitter voltage sense across the IGBT (for 1200V-IGBTs)	900	V
dv/dt	Rate of rise and fall of voltage (secondary to primary side)	15	kV/µs
V_{isolIO}	Isolation test voltage input - output (2 sec. AC)	2500	V
V_{isol12}	Isolation test voltage output 1 - output 2 (2 sec. AC)	1500	V
R_{Gonmin}	Minimum rating of R_{Gon}	10	Ω
$R_{Goffmin}$	Minimum rating for R_{Goff}	10	Ω
$Q_{out/pulse}$	Max. rating for gate T_a = 85 °C	0,7	µC
	charge per pulse T_a = 55 °C	1	µC
T_{op}	Operating temperature	- 40 ... + 85	°C
T_{stg}	Storage temperature	- 40 ... + 85	°C

Characteristics T_a = 25°C, unless otherwise specified

Symbol	Conditions	min.	typ.	max.	Units
V_S	Supply voltage primary	14,4	15,0	15,6	V
I_{SO} 1)	Supply current no load	160		200	mA
	primary side normal op.			450	mA
V_{iT+}	Input threshold voltage (High)	4,0			V
V_{iT-}	Input threshold voltage (LOW)			1,5	V
R_{in}	Input resistance		60		kΩ
$V_{G(on)}$	Turn on gate voltage output		14,9		V
$V_{G(off)}$	Turn off gate voltage output		-6,5		V
R_{GE}	Internal gate-emitter resistance		20		kΩ
f_{ASIC}	ASIC system switching frequency		8		MHz
$td(on)_{IO}$	Input-output turn-on propagation time	0,3	0,45	0,6	µs
$td(off)_{IO}$	Input-output turn-off propagation time	0,3	0,45	0,6	µs
$t_{d(err)}$	Error input-output propagation time	1,15	1,3	1,5	µs
$t_{pERRRESET}$	Error memory reset time	7	15	27	µs
t_{TD}	Interlock dead time adjustable	no interlock		4,1	µs
V_{CEstat}	Reference voltage for V_{CE}-monitoring		5,8		V
t_{blank}	Blanking time		3,5		µs
C_{ps}	Coupling capacitance primary-secondary		40		pF
MTBF	Mean Time Between Failure T_a = 40°C		1		10^6 h
w	weight		95		g
H x B x T	Dimensions		20x57x114		mm

PIN array

Primary side PIN array

Pin	Symbol	Function	Pin	Symbol	Function
01	BS	Auxiliary earth connection	11	+15V	Supply voltage
02	BOT3	Driver signal BOT HB3	12	+15V	Supply voltage
03	TOP3	Driver signal TOP HB3	13	TDT1	Deadtime bit #1
04	BOT2	Driver signal BOT HB2	14	TDT2	Deadtime bit #2
05	TOP2	Driver signal TOP HB2	15	SEL	Deadtime on/off
06	BOT1	Driver signal BOT HB1	16	BSTD	Aux. earth for deadtime adjustment
07	TOP1	Driver signal TOP HB1	17	_ERRIN	_External error signal input
08	_ERR	_Error output Sixpack-driver	18	NC	reserved
09	BSS	System earth connection	19	BRK	Driver signal additional switch
10	BSS	System earth connection	20	_BERR	_Error output additional switch

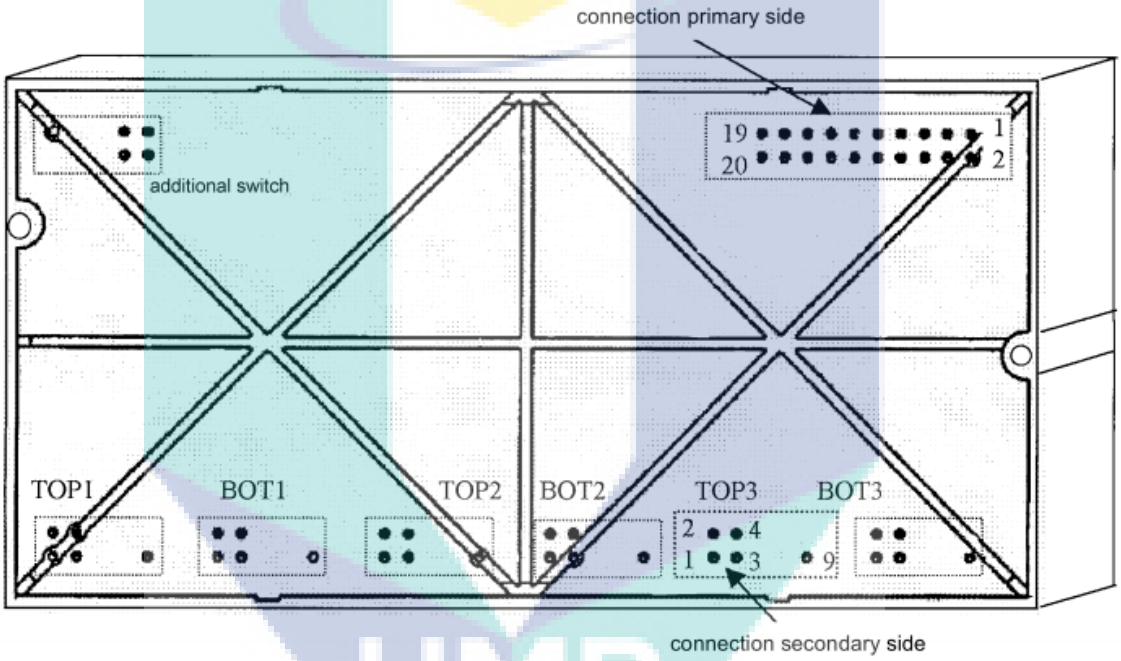


Fig. 1 Bottom view of the SKHI 61 / SKHI 71

Secondary side PIN array

Pin	Symbol	Function	Pin	Symbol	Function
01	R_{Gate}	Gate resistor input	04	$V_{CET}2$	VCE-threshold #2
02	$V_{CET}1$	VCE-threshold #1			
03	E	Emitter input	09	V_{CE}	Collector input

SEMIDRIVER™

SKHI 61 and SKHI 71

General properties and functions

The SKHI 61 and SKHI 71 are 6- and 7-channel drivers for IGBT- and MOSFET-modules and can be soldered directly onto the PCB. The drivers are physically separated.

Since all subassemblies necessary for operation have been integrated, there is no need for external components except for the gate resistors and the V_{CE}-circuitry. V_{CE}-thresholds and the blanking time are adjustable by integrating additional resistors and capacitors according to the customer's specifications.

Interlocking time can be adjusted by simple bridging of connector pins. The driver is equipped with a separate error input for immediate turn-off when receiving error signals from external components (e.g. over-temperature).

The independent seventh driver channel of the SKHI 71 guarantees for simple realisation of brake chopper, boost converter or PFC-circuit applications. By bridging of connector pins the driver error signal is transmitted directly to the SIXPACK-driver for turn-off.

Technical information

I. Primary side

The driver input signals may be transmitted directly to the driver inputs by the controller. The input signal circuit was designed to accept a wide voltage range (see table 1). The typical voltage level is at HCMOS level of V_{DD}=5V (0V=Off, +5V=On).

However, also 15V-signals may be applied with the same turn-on/turn-off thresholds without additional requirements. In this case the input resistance will be different (see table 1).

Status	Level / V			Input Impedance	
	min	typ	max	Ch. 1-6	Ch7
ON 5V	4,0	5,0	5,5	60 kΩ	2,4 kΩ
ON 15V	4,0	15,0	15,6	7 kΩ	1,6 kΩ
OFF 0V	-0,7	0	1,5	60 kΩ	2,4kΩ

Table 1: Input voltage level and input impedances

Error input signal

The error input signal can gather error signals of other hardware components, such as temperature sensors, in a "wired-or"-connection for direct turn-off of the driver. In this case an external pull-up resistor must not be connected.

Note: It is not possible to connect the error output of the SKHI 61/71 to an error input of the SKHI 61/71. But the error output of the chopper driver (SKHI 71) can be connected directly to the error input.

Error output signals

i) 6pack - driver

The error signal of the 6-PACK driver is equipped with an active push-pull output buffer which switches towards zero Volt in case of an error and actively towards + 5 V under operating conditions. The error memory may only be reset, if no error is pending and all cycle signal inputs are set to LOW for t > 9 µs at the same time. If any other external signals are intended to be connected to the error signal _ERR, the _ERR-signal must be uncoupled (see Figure 2)

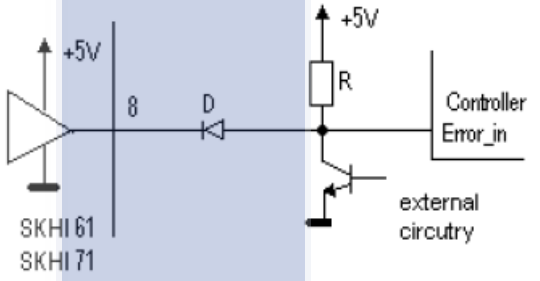


Fig. 2 _ERR-Signal in an „open-collector"-circuit

State _ERROR	Level / V		I / mA	Typical error memory set back time	
	min	max	max	6-PACK	seventh driver
Error	0	0.8	5	16µs	7µs
No error	4	5	5		

Table 2: Error output signal ratings

ii) chopper driver (only SKHI 71)

The error output signal of the additional driver has been designed as an open collector output. A pull-up resistor against the controller's +V_{CC} has to be connected to the controller input for error indication. In case of error, the signal is turned towards earth (zero Volt/ active LOW), otherwise the output will be highly resistive. The error signal of the additional switch will only be active as long as the input signal is on High-level. It is not logically connected to the other six input signals. The error signal of the additional switch may also be directly connected to the error input of the SIXPACK-driver, without requiring an external pull-up resistor. This may be advantageous, if the SIXPACK-driver has to be turned off in case of e.g. a brake chopper error or if only one error signal is evaluated by the controller.

Configuration pins

The configuration pins serve to adjust the TOP/BOTTOM interlocking time of all halfbridges. Due to the special pin design the interlocking time can be adjusted by a simple connection to the BSTD terminal (BSS potential) on the PCB without requiring external components.

Pin	4µs (factory set)	3 µs	2 µs	1 µs	no inter-lock)*
TDT1	open	open	GND	GND	X
TDT2	open	GND	open	GND	X
SEL	open	open	open	open	GND

Table 3: Values for interlocking time adjustment „X" = no effect

)+ TOP and BOTcan be switched simultaneously!

II. Secondary side

We have provided for five terminals per input. Two of them are required for driving the IGBT, one is for short-circuit protection. The remaining two have been designed for optional adjustment of the V_{CE}-threshold.

IGBT-driver signals

We have provided for one gate- and one emitter input pin per power switch, i.e. there is one gate resistor for turn-on and turn-off each. The earth connection of the driver is directly connected to the IGBT's emitter via the emitter input, whereas a resistor of at least 10 Ω has to be connected to the gate circuit. This resistance is the minimum limit value controlled by the driver output buffer in order to limit the pulse currents to their peak value.

A 20 kΩ-resistor has been interconnected between gate and emitter (for the case that the supply voltage breaks down).

Gate-Emitter-voltage	min	Typ	max	Unit
OFF (neg.)	-10	-6.5	-5	V
ON	14,4	14,9	15,4	V
Temperature drift	12	14	16	mV/K

Table 4: Gate-emitter-voltage at T_A = 25 °C

V_{CE} -threshold and V_{CE} -monitoring

V_{CE}-monitoring is done by connection of the driver collector pin to the collector of the power semiconductor.

If the turn-off threshold for short-circuit protection is to be reduced (standard 5,8 V), a resistor has to be connected between the V_{CET1}-threshold#1 pin 2 and V_{CET2}-threshold#2 pin 4 (see fig. 4; Value to be calculated by equation 1). Please do not forget to adapt the blanking time[1] accordingly.

This can be done by attaching a capacitor (value to be calculated by equation 2) between V_{CE}-threshold (pin 2) and earth (pin 3). The V_{CE}-threshold may be adjusted to a minimum value of about 3 V (R_{VCE} = 0 Ω).

1. Blanking time: time between turn-on of the power semiconductor and V_{CE}-registration

$$C_{VCE}[nF] = \frac{t_{blank}[\mu s] \cdot (72{,}75 + R_{VCE}[k\Omega])}{(R_{VCE}[k\Omega] + 4{,}75) \cdot 36{,}08} - 0{,}1$$

Equation 1

$$R_{VCE}[k\Omega] = \frac{11{,}86}{5{,}4 - 0{,}93\ V_{CE}} - 4{,}75$$

Equation 2

The V_{CE}-threshold cannot be increased, so that the preset value of 5,8 V is the maximum value.

V_{CE}-monitoring can also be suppressed by connecting the collector pin V_{CE} of one driver to the belonging emitter pin E and not to the collector of the power semiconductor.

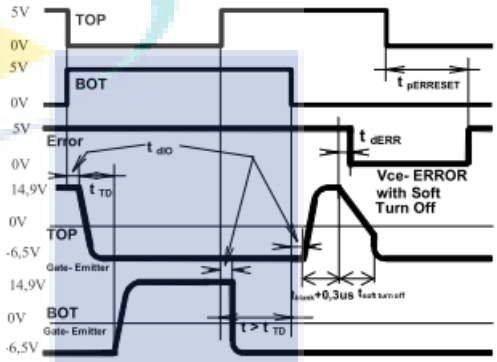


Fig. 3 Course diagram: TOP and BOT-inputs and signal Error compared to TOP and BOT-Gate-Emitter-signal (valid for all halfbridges).

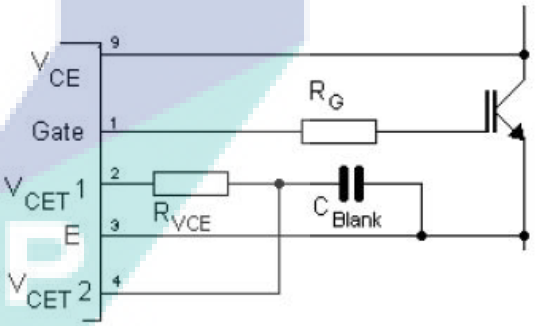


Fig. 4 Connection principle of a power switch with a specifically adjusted V_{CE}-threshold

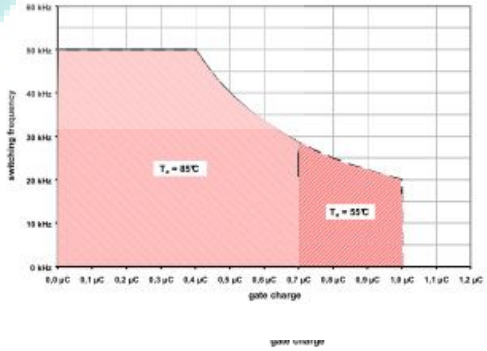


Fig. 5 Maximum rating for output gate charge per pulse

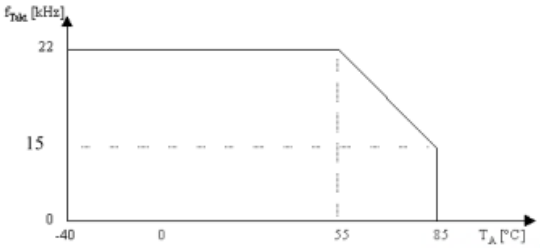


Fig. 6 Maximum cycling frequency at Q_{GE} = 1000 nC vs temperature

The application range can be calculated by the average output current of 20 mA and the repetetive acceptable peak current of 2 A. It has to be considered that the curves are valid for Q_{gmax} = 1 µC only.

The maximum switching frequency f_{max} may be calculated with the following formula, the maximum value however being 50 kHz due to switching reasons:

fmax (kHz) = $2*10^4$ / Q_{GE} (nC)

operating the SKHI 61: besides the operating voltage only the six driver signals TOP1...BOT3 and the driver error output signal are connected to the controller on the primary side. The secondary side is working with the preset V_{CE}-threshold of 5,8 V.

Fig. 7 and 8 show examples for connection of a SKHI 71 for the application with MiniSKiiP (SKiiP 32 NAB 12) and the following adjustments:

- Temperature monitoring of the power semiconductor
- V_{CE}-threshold : 4,8 V
- Interlocking time : 2 µs
- Error blanking time for V_{CE}-threshold : 4 µs

Application Hints

To adjust different V_{CE} thresholds there is needed an additional resistor R_{VCE} and a capacitor C_{VCE} for each switch.

Gate resistor : R_G = 33 Ω

V_{CE}-threshold resistor: intended U_{VCE} = 4,8 V

Applying equation 1 R_{VCE} will result in

$$R_{VCE}[k\Omega] = \frac{11,86}{5,4 - 0,93 \cdot 4,8} - 4,75[k\Omega] = 7,9k\Omega$$

Next value taken from the E24-range: 8,25 k. The threshold voltage is recalculated with 8,25 kΩ.

V_{CE}-threshold at 4,82 V.

For the capacitor the blanking time may be calculated as: $t_{blanking}$ = 4 µs

$$C_{VCE}[nF] = \frac{4 \cdot (72,75 + 8,25)}{(8,25 + 4,75) \cdot 36,08} - 0,1 = 590pF$$

Thus there can be chosen a capacitor of 680 pF.

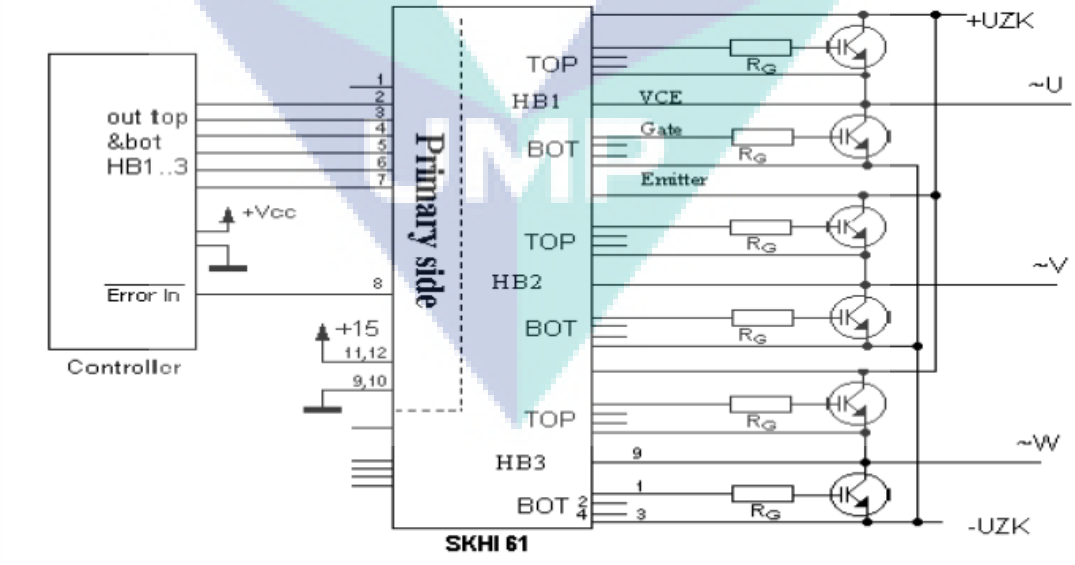


Fig. 7 SKHI 61 block diagram

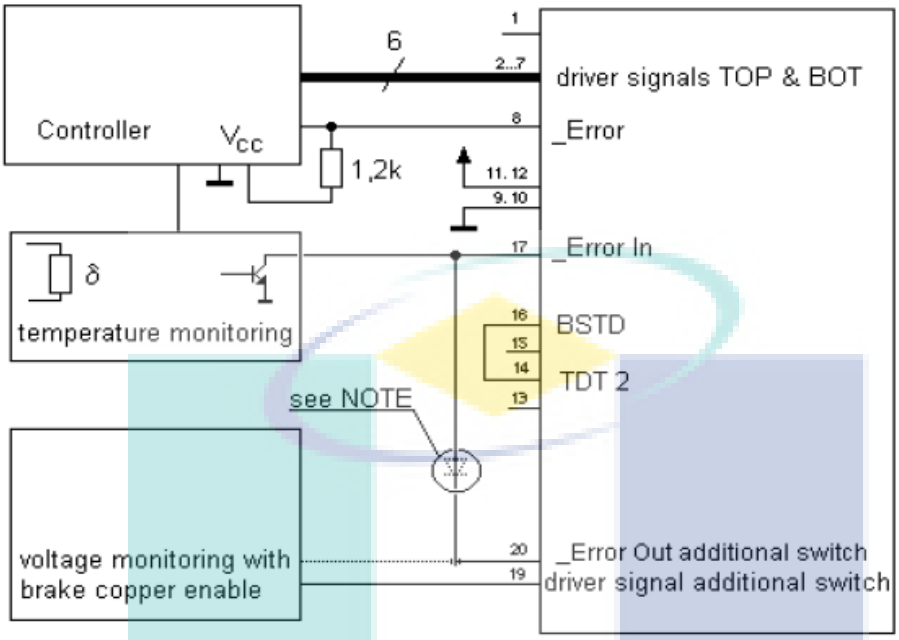


Fig. 8 Examply circuit for a SKHI 71 connected to the primary side

NOTE: If the _ErrorOut-signal of the additional switch (here brake chopper) is also needed for other evaluations, a Schottky diode has to be connected as shown in the figure above to uncouple the signal. Furthermore there has to be connected a pull-up resistor to the additional error output. It is useful to use a capacitor (typ. 100 pF, absolute maximum 2,2 nF) at the _ErrorIn to avoid undesired couplings.

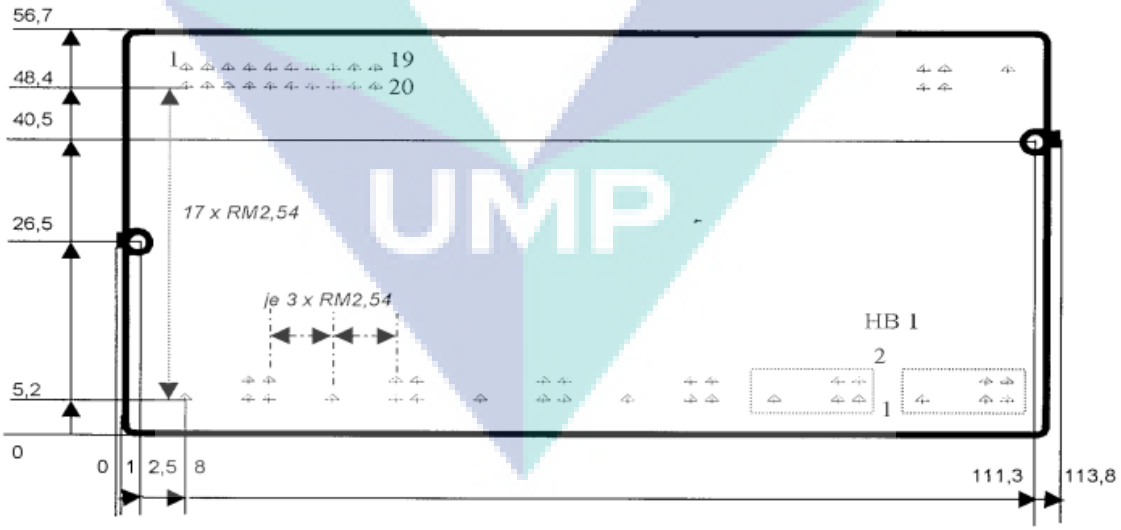


Fig. 9 Dimensional drawing, layout

View: tooling side (top view, driver put on top of the PCB)
Measurements taken in [mm]
Grid of connector pins; gaps between pins: RM2,54

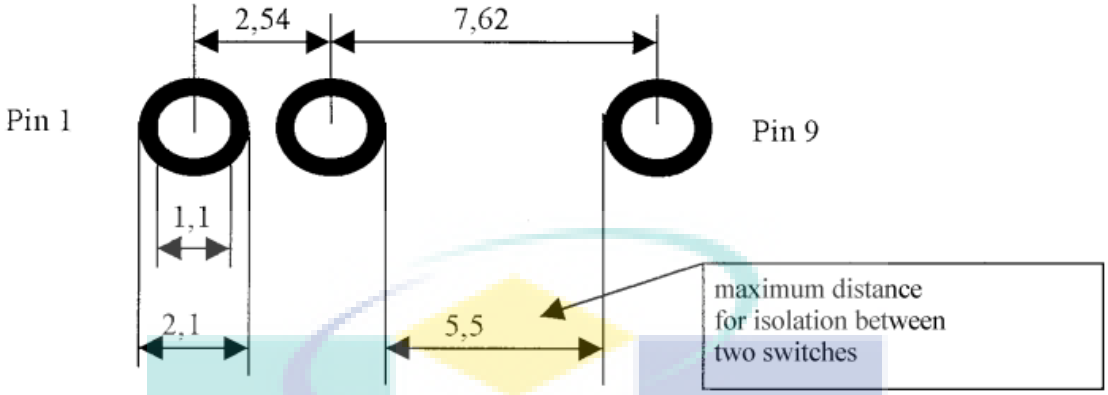


Fig. 10 Measurements in [mm] for solder pads (as a proposal for the design) and solder pad gaps (partial drawing)

Mounting Hints

The temperature of the solder must not exceed 265°C, and solder time must not exceed 4 seconds. The ambient temperature must not exceed the specified maximum storage temperature of the driver. The driver is not suited for hot air reflow or infrared reflow soldering processes.

The driver hast two drill holes (inner diameter: 1,8mm) for fixing the driver on PCB with self tapping screws 30x8 (e.g. EJOT PT). The maximum immersion depth of the screws may not exceed 9 mm. The details of screw head design can be chosen by the user.

All electrical and mechanical parameters should be validated by user´s technical experts for each application.

APPENDIX D.3

Rectifier diodes ultrafast — BYQ28X series

GENERAL DESCRIPTION

Glass passivated dual epitaxial rectifier diodes in a full pack plastic envelope, featuring low forward voltage drop, ultra-fast recovery times and soft recovery characteristic. They are intended for use in switched mode power supplies and high frequency circuits in general where low conduction and switching losses are essential.

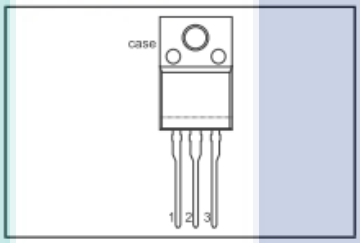
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BYQ28X-	100	150	200	
V_{RRM}	Repetitive peak reverse voltage	100	150	200	V
V_F	Forward voltage	0.895	0.895	0.895	V
$I_{O(AV)}$	Output current (both diodes conducting)	10	10	10	A
t_{rr}	Reverse recovery time	25	25	25	ns

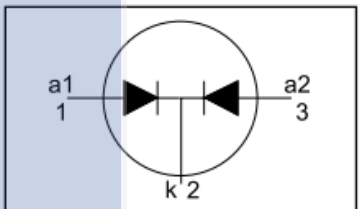
PINNING - SOT186A

PIN	DESCRIPTION
1	anode 1 (a)
2	cathode (k)
3	anode 2 (a)
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-100	-150	-200	
V_{RRM}	Repetitive peak reverse voltage		-	100	150	200	V
V_{RWM}	Crest working reverse voltage		-	100	150	200	V
V_R	Continuous reverse voltage[1]		-	100	150	200	V
$I_{O(AV)}$	Output current (both diodes conducting)[2]	square wave $\delta = 0.5$; $T_{hs} \leq 92$ ˚C	-		10		A
		sinusoidal $a = 1.57$; $T_{hs} \leq 95$ ˚C	-		9		A
$I_{O(RMS)}$	RMS forward current		-		14		A
I_{FRM}	Repetitive peak forward current per diode	$t = 25$ µs; $\delta = 0.5$; $T_{hs} \leq 92$ ˚C	-		10		A
I_{FSM}	Non-repetitive peak forward current per diode	$t = 10$ ms	-		50		A
		$t = 8.3$ ms sinusoidal; with reapplied $V_{RWM(max)}$	-		55		A
I^2t	I^2t for fusing	$t = 10$ ms	-		12.5		A^2s
T_{stg}	Storage temperature		-40		150		˚C
T_j	Operating junction temperature		-		150		˚C

1 $T_{hs} \leq 148$˚C for thermal stability.

2 Neglecting switching and reverse current losses

ISOLATION LIMITING VALUE & CHARACTERISTIC

T_{hs} = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	R.M.S. isolation voltage from all three terminals to external heatsink	f = 50-60 Hz; sinusoidal waveform; R.H. ≤ 65% ; clean and dustfree	-		2500	V
C_{isol}	Capacitance from T2 to external heatsink	f = 1 MHz	-	10	-	pF

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}hs}$	Thermal resistance junction to heatsink	with heatsink compound	-	-	5.7	K/W
		without heatsink compound	-	-	6.7	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	55	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_F	Forward voltage (per diode)	I_F = 5 A; T_j = 150˚C	-	0.80	0.895	V
		I_F = 5 A	-	0.95	1.10	V
		I_F = 10 A	-	1.10	1.25	V
I_R	Reverse current (per diode)	$V_R = V_{RWM}$; T_j = 100 ˚C	-	0.1	0.2	mA
		$V_R = V_{RWM}$	-	2	10	µA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Q_s	Reverse recovery charge (per diode)	I_F = 2 A; $V_R \geq$ 30 V; $-dI_F/dt$ = 20 A/µs	-	4	9	nC
t_{rr1}	Reverse recovery time (per diode)	I_F = 1 A; $V_R \geq$ 30 V; $-dI_F/dt$ = 100 A/µs	-	15	25	ns
t_{rr2}	Reverse recovery time (per diode)	I_F = 0.5 A to I_R = 1 A; I_{rec} = 0.25 A	-	10	20	ns
V_{fr}	Forward recovery voltage (per diode)	I_F = 1 A; dI_F/dt = 10 A/µs	-	1	-	V

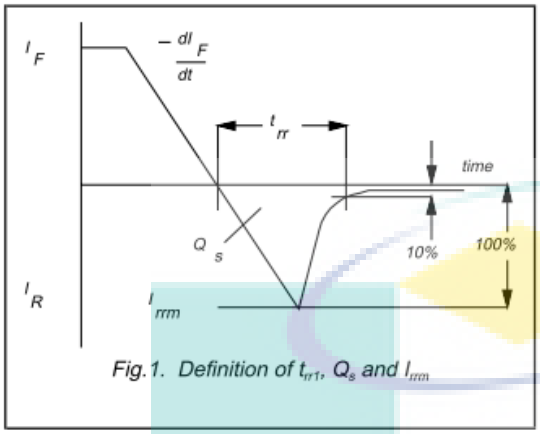


Fig.1. Definition of t_{rr1}, Q_s and I_{rrm}

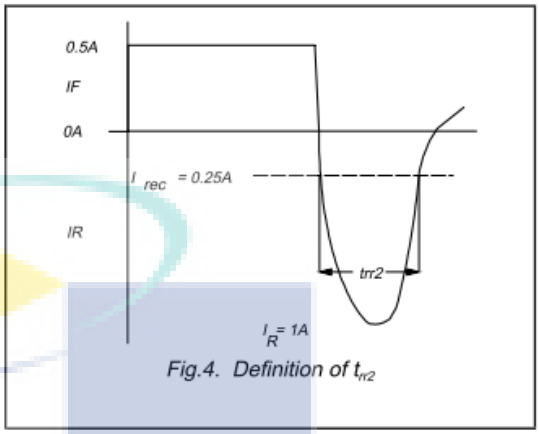


Fig.4. Definition of t_{rr2}

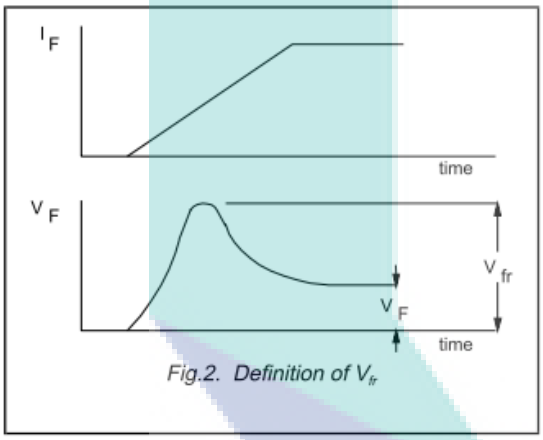


Fig.2. Definition of V_{fr}

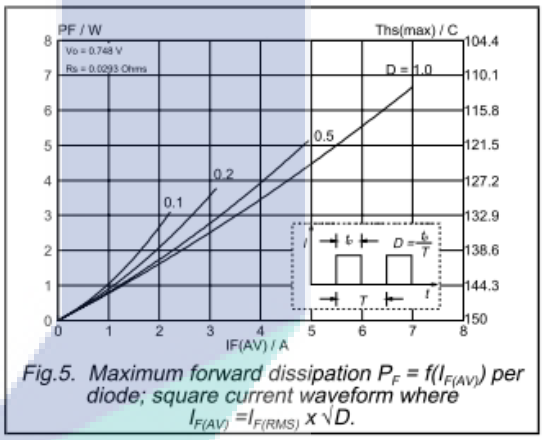


Fig.5. Maximum forward dissipation $P_F = f(I_{F(AV)})$ per diode; square current waveform where $I_{F(AV)} = I_{F(RMS)} \times \sqrt{D}$.

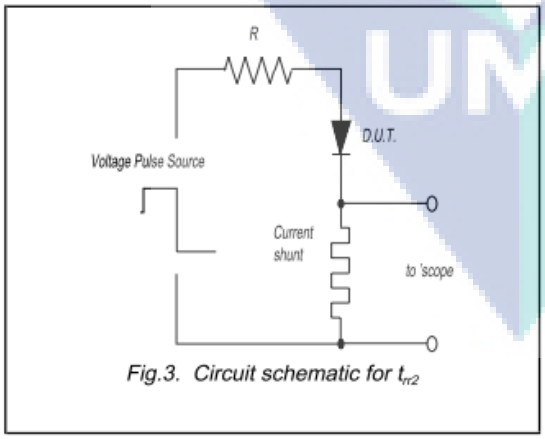


Fig.3. Circuit schematic for t_{rr2}

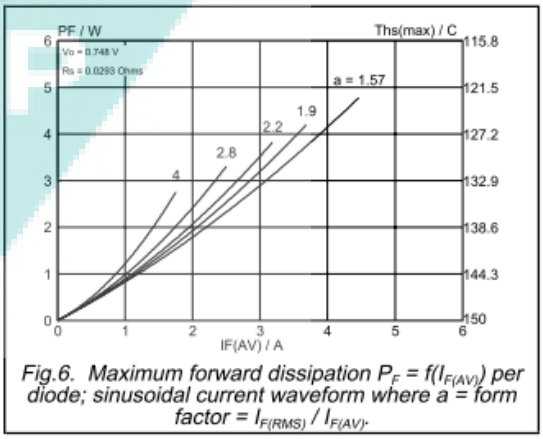


Fig.6. Maximum forward dissipation $P_F = f(I_{F(AV)})$ per diode; sinusoidal current waveform where a = form factor = $I_{F(RMS)} / I_{F(AV)}$.

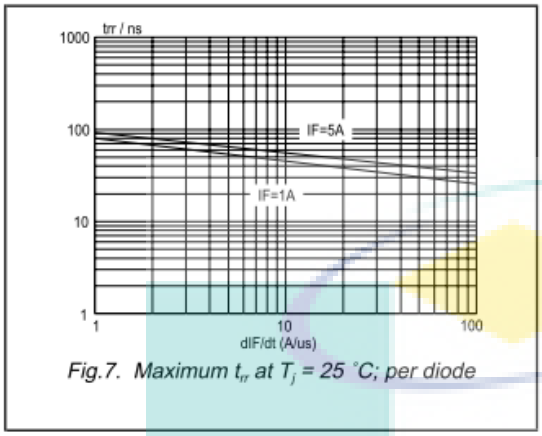


Fig.7. Maximum t_{rr} at T_j = 25 ˚C; per diode

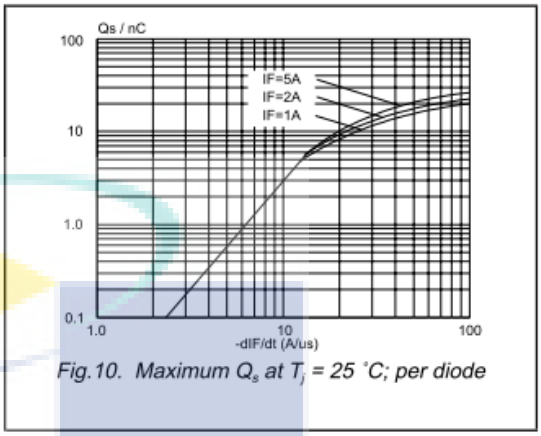


Fig.10. Maximum Q_s at T_j = 25 ˚C; per diode

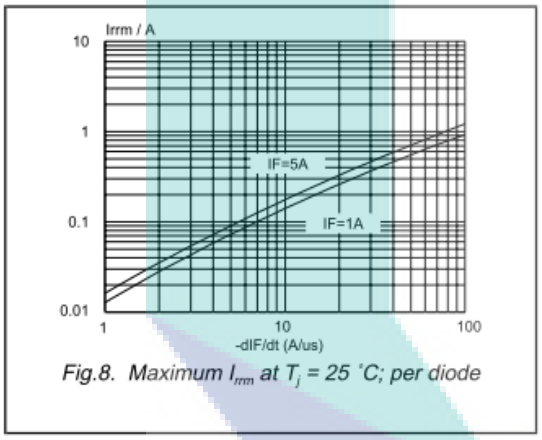


Fig.8. Maximum I_{rrm} at T_j = 25 ˚C; per diode

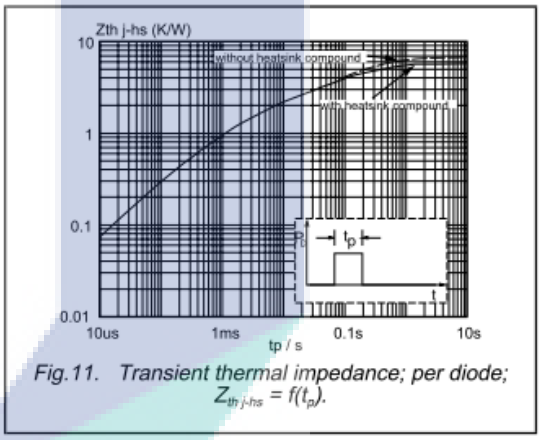


Fig.11. Transient thermal impedance; per diode; $Z_{th\ j\text{-}hs} = f(t_p)$.

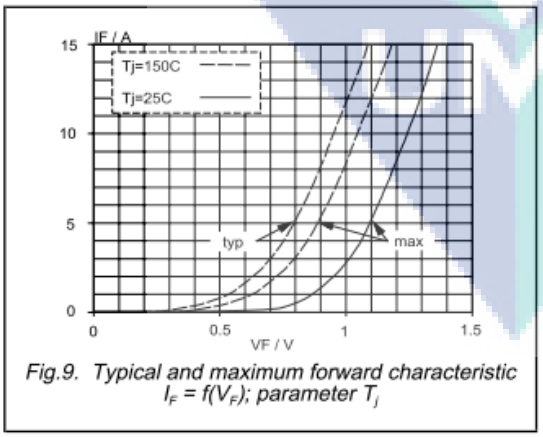


Fig.9. Typical and maximum forward characteristic $I_F = f(V_F)$; parameter T_j

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

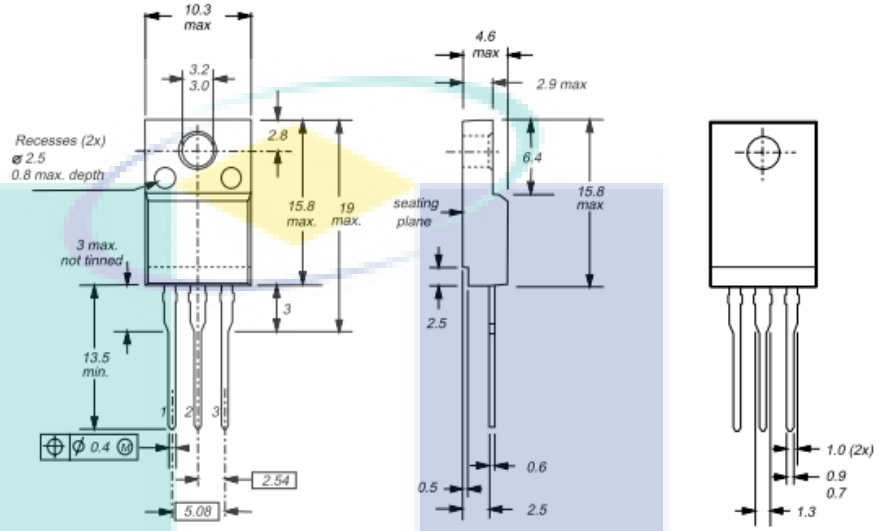


Fig.12. SOT186A; The seating plane is electrically isolated from all terminals.

Notes
1. Refer to mounting instructions for F-pack envelopes.
2. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

APPENDIX D.4

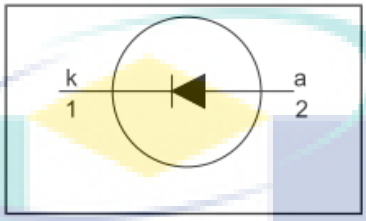
Philips Semiconductors — **Product specification**

Damper diode fast, high-voltage — BY359-1500, BY359-1500S

FEATURES

- Low forward volt drop
- Fast switching
- Soft recovery characteristic
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_R = 1500 V

$V_F \leq$ 1.8 V / 2 V

$I_{F(RMS)}$ = 15.7 A

$I_{FSM} \leq$ 60 A

$t_{rr} \leq$ 600 ns / 350 ns

GENERAL DESCRIPTION

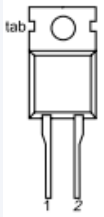
Glass-passivated double diffused rectifier diode featuring low forward voltage drop, fast reverse recovery and soft recovery characteristic. The device is intended for use in TV receivers and PC monitors.

The BY359 series is supplied in the conventional leaded SOD59 (TO220AC) package.

PINNING

PIN	DESCRIPTION
1	cathode
2	anode
tab	cathode

SOD59 (TO220AC)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS		MIN.	MAX.	UNIT
V_{RSM}	Peak non-repetitive reverse voltage			-	1500	V
V_{RRM}	Peak repetitive reverse voltage			-	1500	V
V_{RWM}	Crest working reverse voltage			-	1300	V
$I_{F(peak)}$	Peak forward current	16-32kHz TV	BY359-1500	-	10	A
		31-70kHz monitor	BY359-1500S	-	7	A
$I_{F(RMS)}$	RMS forward current			-	15.7	A
I_{FRM}	Peak repetitive forward current	sinusoidal; a = 1.57		-	60	A
I_{FSM}	Peak non-repetitive forward current	t = 10 ms		-	60	A
		t = 8.3 ms		-	66	A
		sinusoidal; T_j = 150 ˚C prior to surge; with reapplied $V_{RWM(max)}$				
T_{stg}	Storage temperature			-40	150	˚C
T_j	Operating junction temperature			-	150	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.0	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air.	-	60	-	K/W

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

			BY359-1500		BY359-1500S		
SYMBOL	**PARAMETER**	**CONDITIONS**	**TYP.**	**MAX.**	**TYP.**	**MAX.**	**UNIT**
V_F	Forward voltage	I_F = 20 A	1.3	1.8	1.5	2.0	V
		I_F = 10 A; T_j = 150˚C	1.00	1.5	1.25	1.75	V
I_R	Reverse current	V_R = 1300 V	10	100	10	100	µA
		V_R = 1300 V; T_j = 100 ˚C	50	300	100	600	µA

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

			BY359-1500		BY359-1500S		
SYMBOL	**PARAMETER**	**CONDITIONS**	**TYP.**	**MAX.**	**TYP.**	**MAX.**	**UNIT**
t_{rr}	Reverse recovery time	I_F = 2 A; $V_R \geq$ 30 V;	0.47	0.60	0.28	0.35	µs
Q_s	Reverse recovery charge	$-dI_F/dt$ = 20 A/µs	1.6	2.0	0.70	0.95	µC
V_{fr}	Peak forward recovery voltage	I_F = 10 A; dI_F/dt = 30 A/µs	11.0	-	17.0	-	V

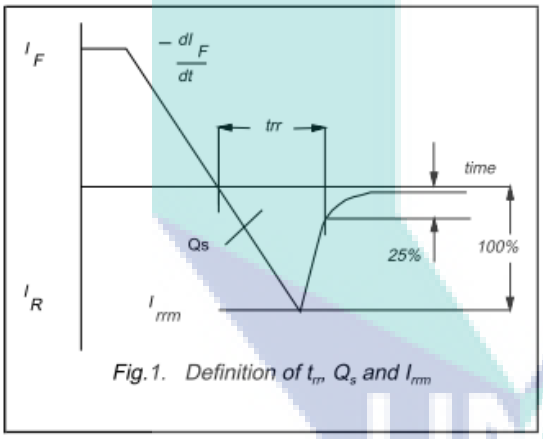


Fig.1. Definition of t_{rr}, Q_s and I_{rrm}

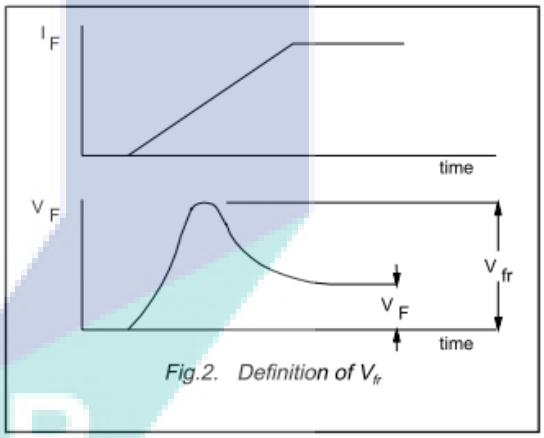


Fig.2. Definition of V_{fr}

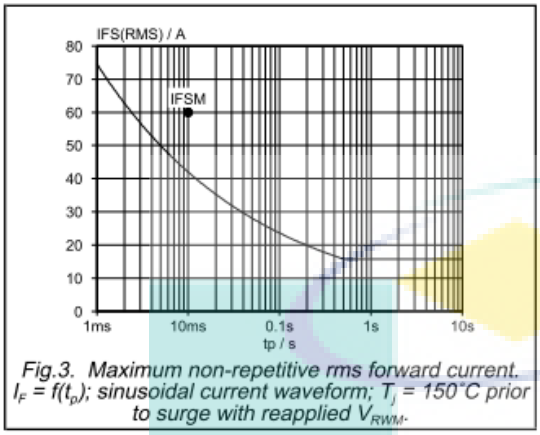


Fig.3. Maximum non-repetitive rms forward current. $I_F = f(t_p)$; sinusoidal current waveform; T_j = 150˚C prior to surge with reapplied V_{RWM}.

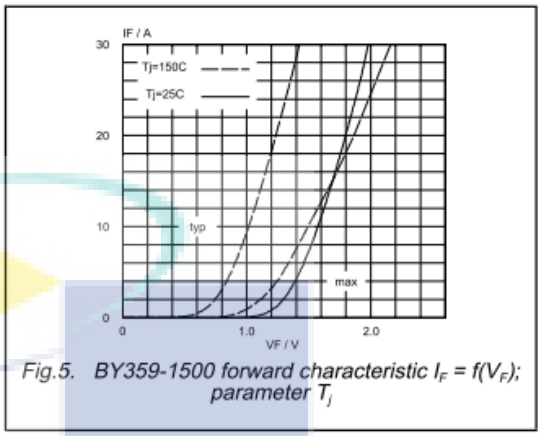


Fig.5. BY359-1500 forward characteristic $I_F = f(V_F)$; parameter T_j

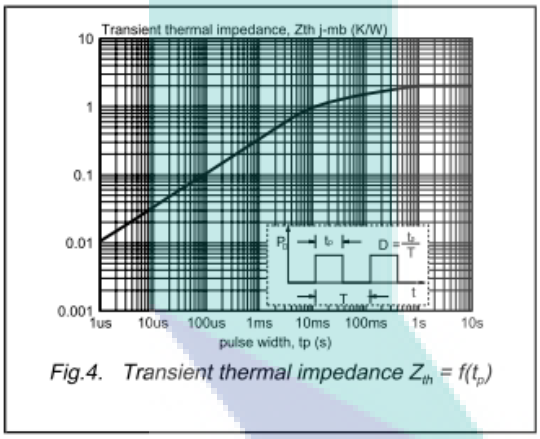


Fig.4. Transient thermal impedance $Z_{th} = f(t_p)$

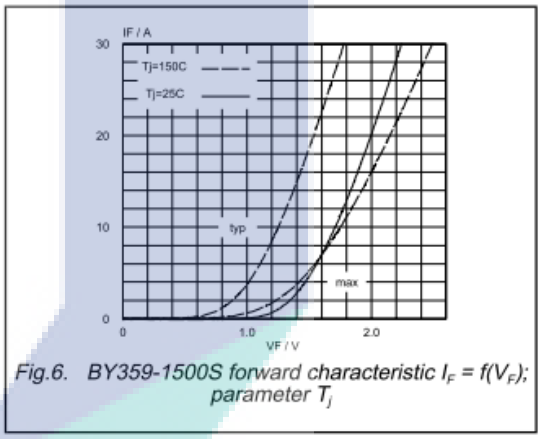


Fig.6. BY359-1500S forward characteristic $I_F = f(V_F)$; parameter T_j

MECHANICAL DATA

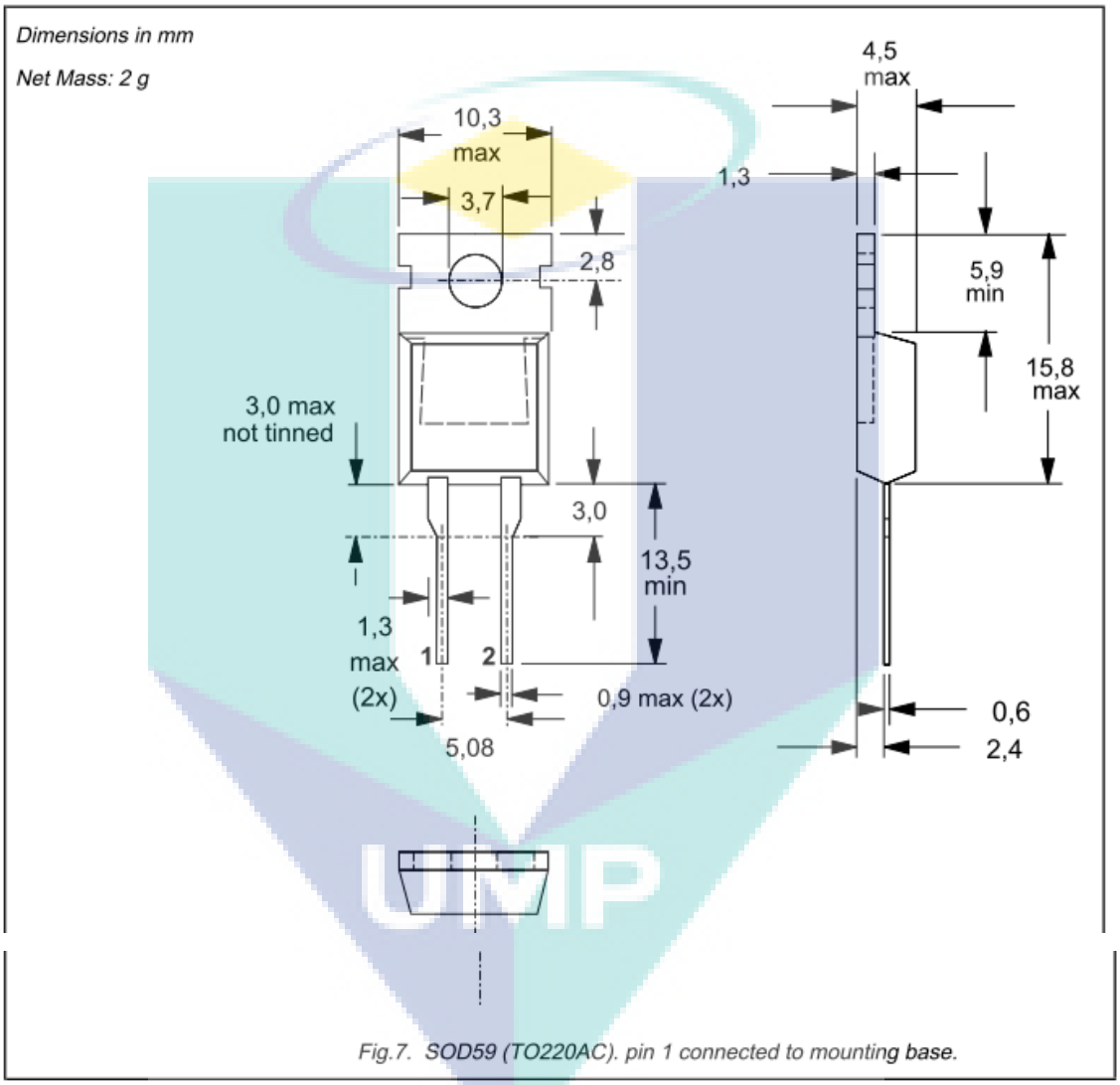


Fig.7. SOD59 (TO220AC). pin 1 connected to mounting base.

Notes
1. Refer to mounting instructions for TO220 envelopes.
2. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

APPENDIX D.5

Digital Signal Controllers (DSCs)

Check for Samples: TMS320F28335, TMS320F28334, TMS320F28332, TMS320F28235, TMS320F28234, TMS320F28232

1 TMS320F2833x, TMS320F2823x DSCs

1.1 Features

- High-Performance Static CMOS Technology
  - Up to 150 MHz (6.67-ns Cycle Time)
  - 1.9-V/1.8 -V Core, 3.3-V I/O Design
- High-Performance 32-Bit CPU (TMS320C28x)
  - IEEE-754 Single-Precision Floating-Point Unit (FPU) (F2833x only)
  - 16 x 16 and 32 x 32 MAC Operations
  - 16 x 16 Dual MAC
  - Harvard Bus Architecture
  - Fast Interrupt Response and Processing
  - Unified Memory Programming Model
  - Code-Efficient (in C/C++ and Assembly)
- Six-Channel DMA Controller (for ADC, McBSP, ePWM, XINTF, and SARAM)
- 16-Bit or 32-Bit External Interface (XINTF)
  - Over 2M x 16 Address Reach
- On-Chip Memory
  - F28335/F28235: 256K x 16 Flash, 34K x 16 SARAM
  - F28334/F28234: 128K x 16 Flash, 34K x 16 SARAM
  - F28332/F28232: 64K x 16 Flash, 26K x 16 SARAM
  - 1K x 16 OTP ROM
- Boot ROM (8K x 16)
  - With Software Boot Modes (via SCI, SPI, CAN, I2C, McBSP, XINTF, and Parallel I/O)
  - Standard Math Tables
- Clock and System Control
  - Dynamic PLL Ratio Changes Supported
  - On-Chip Oscillator
  - Watchdog Timer Module
- GPIO0 to GPIO63 Pins Can Be Connected to One of the Eight External Core Interrupts
- Peripheral Interrupt Expansion (PIE) Block That Supports All 58 Peripheral Interrupts
- 128-Bit Security Key/Lock
  - Protects Flash/OTP/RAM Blocks
  - Prevents Firmware Reverse Engineering
- Enhanced Control Peripherals
  - Up to 18 PWM Outputs
  - Up to 6 HRPWM Outputs With 150 ps MEP Resolution
  - Up to 6 Event Capture Inputs
  - Up to 2 Quadrature Encoder Interfaces
  - Up to 8 32-Bit/Nine 16-Bit Timers
- Three 32-Bit CPU Timers
- Serial Port Peripherals
  - Up to 2 CAN Modules
  - Up to 3 SCI (UART) Modules
  - Up to 2 McBSP Modules (Configurable as SPI)
  - One SPI Module
  - One Inter-Integrated-Circuit (I2C) Bus
- 12-Bit ADC, 16 Channels
  - 80-ns Conversion Rate
  - 2 x 8 Channel Input Multiplexer
  - Two Sample-and-Hold
  - Single/Simultaneous Conversions
  - Internal or External Reference
- Up to 88 Individually Programmable, Multiplexed GPIO Pins With Input Filtering
- JTAG Boundary Scan Support (1)
- Advanced Emulation Features
  - Analysis and Breakpoint Functions
  - Real-Time Debug via Hardware
- Development Support Includes
  - ANSI C/C++ Compiler/Assembler/Linker
  - Code Composer Studio™ IDE
  - DSP/BIOS™
  - Digital Motor Control and Digital Power Software Libraries
- Low-Power Modes and Power Savings
  - IDLE, STANDBY, HALT Modes Supported
  - Disable Individual Peripheral Clocks

(1) IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture

2.1 Pin Assignments

The 176-pin PGF/PTP low-profile quad flatpack (LQFP) pin assignments are shown in Figure 2-1. The 179-ball ZHH ball grid array (BGA) terminal assignments are shown in Figure 2-2 through Figure 2-5. The 176-ball ZJZ plastic ball grid array (PBGA) terminal assignments are shown in Figure 2-6 through Figure 2-9.Table 2-3 describes the function(s) of each pin.

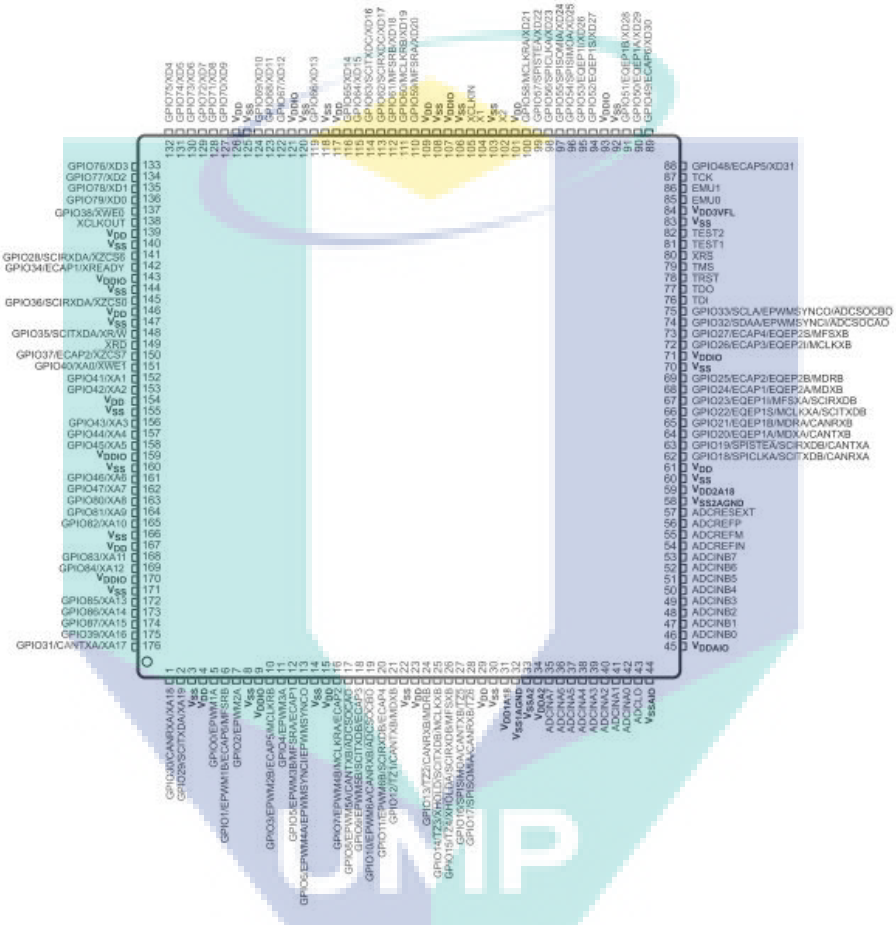


Figure 2-1. F2833x, F2823x 176-Pin PGF/PTP LQFP (Top View)

APPENDIX E

LIST OF PUBLICATIONS

1. **Ruzlaini Ghoni,** Ahmed N. Abdalla. 2013. An Intelligent Control of Sensorless Matrix Converter Induction Motor Drive Using PSO Model. *Technics Technologies Education Management.* **8**(1): 397-402 (***ISI Indexing; Impact Factor 0.351)***

2. **Ruzlaini Ghoni,** Ahmed N. Abdalla, Tarmizi Ibrahim, Damhuji Rifaie, Zulkarnain Lubis. 2012. A Ripple Torque Minimization Strategy for Matrix Converter Using Hybrid PSO. *Elsevier, Procedia Engineering*. 38: 111-124 (***Scopus and EI Indexing)***

3. **Ruzlaini Ghoni,** Ahmed N. Abdalla, S.P. Koh, Hassan Farhan Rashag, Ramdan Razali. 2011. Issues of Matrix Converters: Technical Review." International *Journal of Physical Sciences*. **6**(15): 3628-3640 ***(ISI Indexing; Impact Factor 0.554)***

4. Ahmed N. Abdalla, **Ruzlaini Ghoni**, and N.F. Zakaria. 2011. Simulation Model of Space Vector Modulated Control Matrix Converter-Fed Induction Motor. *Journal of Applied Sciences*, **11**(5):768-777 ***(ISI and Scopus Indexing; Impact Factor 0.033)***

5. **Ruzlaini Ghoni** and Ahmed N. Abdalla. 2010. Analysis And Mathematical Modelling Of Space Vector Modulated Direct Controlled Matrix Converter. *Journal of Theoretical & Information Technology*, **21**(1):36-40 (***Scopus Indexing***)

6. **Ruzlaini Ghoni**, Ahmed N. Abdalla, and Zahim Sujod. 2010. Direct Torque Control for Matrix Converter-Fed Three Phase Induction Motor with Hybrid PSO. *Journal of Theoretical & Information Technology*, **13**(1):36-40 ***(Scopus Indexing)***

7. Ramdan Razali, Ahmed N. Abdalla, **Ruzlaini Ghoni,** C. Venkataseshaiah. 2012. Improving Squirrel Cage Induction Motor Efficiency: Technical Review. *International Journal of Physical Sciences.* **7**(8): 1129-1140 ***(ISI Indexing; Impact Factor 0.554)***

8. Zulkarnain, Ahmed N. Abdalla, Mortaza, **Ruzlaini Ghoni**. 2009. Mathematical Modelling of the Three Phase Induction Motor Couple to DC Motor in Hybrid Electric Vehicle. *American Journal of Engineering and Applied Sciences.* **2**(4): 715-719.

9. **Ruzlaini Ghoni**, Ahmed N. Abdalla, Zulkarnain, Mohd Nuhairi, Mohd Yusri. 2009. Performance Analysis of Difference Matrix Converter Topologies on Three Phase Induction Motor Drive. *International Conference on Engineering Technology*: 22-26.

10. **Ruzlaini Ghoni**, Ahmed N. Abdalla, Zulkarnain, Mohd Nuhairi, Mohd Yusri.2009. Improved Sensorless Vector Control for Induction Motor Drives Fed by a Dual Bridge Matrix Converter. *International Conference on Software Engineering and Computer System*: 100-105.

11. Zulkarnain, Ahmed N. Abdalla, Mortaza, **Ruzlaini Ghoni**. 2009. A Novel Nonlinear Torque and Current Control of Induction Motor Couple DC Motor. *International Conference on Software Engineering and Computer System*: 53-56.

12. **Ruzlaini Ghoni**, Ahmed N. Abdalla, Tarmizi Ibrahim, Damhuji Rifai. 2012. A Ripple Minimization Strategy Using Improved Matrix Converter Drives. *Proceedings of Malaysian Postgraduate Conference on Electrical, electronic and Control Technology*.

13. **Ruzlaini Ghoni**, Ahmed N. Abdalla, Zulkarnain, Mohd Nuhairi, Mohd Yusri. 2009. Comparative Analysis of Matrix Converter Drives on Three Phase Induction Motor. *The Malaysian Technical Universities Conference and Exhibition on Engineering and Technology*: 18-21.

14. Zulkarnain, Ahmed N. Abdalla, **Ruzlaini Ghoni**. 2009. Performance Analysis Transient Torque Control of Induction Motor Couple to DC Motor in a Hybrid Electric Vehicle. *The Malaysian Technical Universities Conference and Exhibition on Engineering and Technology*: 14-18.