BOOST CONVERTER WITH POWER FACTOR CORRECTION

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DEDICATION

Dedicated, in thankful appreciation for support, encouragement and understanding to my beloved families, lecturers and fellow friends.

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ABSTRACT

The boost converter is a type of the switched mode power supply which normally to step up the voltage since the voltage output is large than the input voltage. A simple boost converter consists of at least two switching components such as diode and transistor with combine to an energy storage element which is capacitor. As a DC to DC converter, the input of the converter must be a direct voltage and the output with also in range of direct voltage with higher than the voltage input and the switching component control the operation of the converter with the capacitor as the energy storage and the added component is used for filtering purpose. The objective of this project mainly to feed the load of inverter for 3-phase AC motors which is for 300W application and able to supplied the constant voltage output from an AC input voltage. As the scope of this project, the chapter covered as much as to design a boost converter which has power factor correction to be feed on the 3-phase inverter.

ABSTRAK

Penukar rangsangan adalah jenis peningkat voltan yang menghidupkan bekalan kuasa yang biasanya untuk meningkatkan voltan yang mana voltan keluaran adalah besar daripada voltan input. Penukar rangsangan mudah terdiri daripada sekurang-kurangnya dua komponen bertukar seperti diod dan transistor dengan menggabungkan elemen penyimpanan tenaga seperti kapasitor. Sebagai DC ke DC converter, input penukar mestilah voltan langsung dan output dengan juga dalam julat voltan langsung dengan lebih tinggi daripada voltan input dan penukaran komponen kawalan operasi penukar dengan kapasitor sebagai simpanan tenaga dan komponen yang ditambah digunakan untuk tujuan penapisan.Objektif projek ini terutamanya untuk memberi bekalan kuasa kepada beban penyongsang 3 fasa bagi permohonan kuasa 300W dan boleh dibekalkan voltan keluaran malar daripada voltan input AC. Berdasarkan skop projek ini, bab ini meliputi sebanyak merekabentuk penukar rangsangan yang mempunyai pembetulan faktor kuasa untuk digunakan sebagai bekalan kuasa bagi penyongsang 3-fasa.

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LIST OF ABBREVIATIONS

AC	Alternating Current
PWM	Pulse Width Modulation
PC	Personal Computer
THD	Total Harmonics Distortion
DPF	Displacement Power Factor
PF	Power Factor
PSU	Power Supply Unit
SMPS	Switch Mode Power Supply
CCM	Continuous Conduction Mode
MOSFET	Metal Oxide silicon Field Effect Transistor
OVP	Over voltage Protection
UVP	Under voltage Protection
OPL	Over Power Limitation
EMI	Electromagnetic Interference

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CHAPTER 1

INTRODUCTION

1.1 Project Introduction

A 3-phase AC motor is widely used in many applications such as compressor, pump, conveyer, industrial drives and the added with software interfacing will ensure the ideal advantages of the 3-phase AC motor. In practice, most of these drives are based on ac induction motor because these motors are rugged, reliable, and relatively inexpensive. The proposed technique on this project are based on single phase to three phase conversion that was applications in rural areas and also in industries where three phase equipment or motors are to be operated from the easily available single phase supply [1].

These converters are excellent choice for situations where three phase power supply is not available. This needs a strong, efficient and cost effective with high quality single phase to three phase conversion. The added advantage over the single ac motor is that the three phase motor is more efficient and economical than the single phase motor. Advanced PWM techniques are employed to guarantee high quality output voltage with reduced harmonics and sinusoidal input current irrespective of the load. The boost converter with power factor correction is used to obtain the voltage ouput at constant 390V and typically for 300W for the load drive of continuous conduction mode.

1.2 Objective of the Project

The aim of this project is mainly to feed the load of inverter for 3-phase AC motors for the motor drive by using a single AC source. The main objectives are stated as follow:

a) To design a boost converter with having the power factor controller.
b) To test the designed converter for verification.

1.3 Problem Statement

Nowadays most of the installed AC motor was fixed to a certain level of speed and unstable to the load of the motor that distorted and changed at some level of speed. The changing cost is high when there is need of another replacement due to the speed requirement on the load sides. Besides, the speed of 3 phase AC motor installed is unable to monitor.

1.4 Scope of the Project

There have several scopes on achieving the objective mention and covered as much as the aspect of the project designs on finding the suitable method to be used. The development of PC based on frequency inverter for three phase AC motor is needed to be fed with the DC power supply, which is the used of boost converter alongside the power factor correction availability. At this rate, the main scope of this project is to provide the DC supply from an AC supply on the socket wall. The power factor correction controller is the used to verify the 300W that are used on the output stage with the nearly constant voltage output as well.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In this chapter, the basis theories of continuous conduction mode of boost converter alongside the architecture of the 3-phase induction motor will be reviewed. The switching scheme, power device and control technique are described.

2.2 Converter

Converter in power electronics field is an electrical device that converts power from of an electrical signal or power source, by converting it from one form to another. Generally, converter can be classified to 4 categories which are a rectifier, inverter, chopper and cycloconverter. Converters are used for applications such as rectification of AC to DC, or an inversion from DC to a controlled frequency of AC to supply variable speed AC motor, interfacing DC power sources to AC distribution systems such as photoelectric devices and also productions of DC from AC power for subway and for controlled DC voltage for speed control of DC motor in various industrial applications and etc [2].

2.3 Continuous Conduction Mode

In continuous conduction mode, the boost power stage assumes to be in the two states per switching cycle. In the on state, Switch is on and Diode is off. In the off state, Switch is off and Diode is on. The figure below has shown the simple boost converter equivalent circuit with voltage as the references.

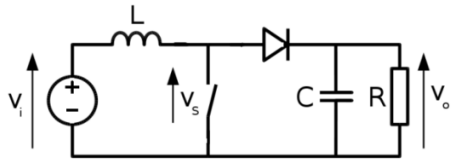


Figure 2.1 Boost converter circuit diagram.

In continuous-conduction-mode (CCM) the current in the energy transfer inductor never goes to zero between switching cycles, as the current continuous and the below figure show the graph of the current.

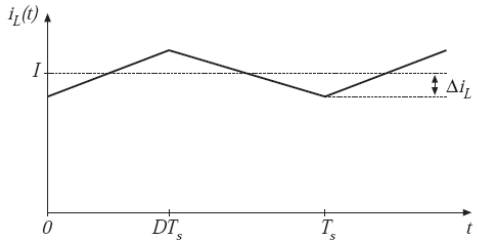


Figure 2.2 Continuous conduction mode inductor current.

At the ON-state, switch S is closed, which makes the input voltage (V_i) appear across the inductor, which cause a change in current (I_L) flowing through the inductor during a time period (t) by the formula:

$$\frac{\Delta \mathrm{IL}}{\Delta \mathrm{t}} = \frac{\mathrm{V}}{\mathrm{L}} \tag{2.0}$$

At the end of ON-state condition, the *L* increase as the increases of the inductor is calculated by the formula below:

$$\Delta \mathrm{IL_{On}} = \frac{1}{\mathrm{L}} \int_0^{\mathrm{DT}} \mathrm{Vi}\, \mathrm{dt} = \frac{\mathrm{DT}}{\mathrm{L}}\, \mathrm{Vi} \tag{2.1}$$

Where: *D is the duty cycle*

The duty cycle represents the fraction of the commutation period T during which the switch is ON. Therefore D ranges between 0 (S is never on) and 1 (S is always on). Meanwhile, at OFF-state condition, the switch S is open and the inductor current flows through the load. The voltage drop considered zero at the diode, and a capacitor large enough for its voltage to remain constant, the advancement of I_L is given as:

$$\mathrm{Vi} - \mathrm{Vo} = \mathrm{L}\, \frac{\mathrm{dIL}}{\mathrm{dt}} \tag{2.2}$$

Therefore, the variation of I_L during the OFF-period is:

$$\Delta \mathrm{IL_{Off}} = \int_{\mathrm{DT}}^{\mathrm{T}} \frac{(\mathrm{Vi} - \mathrm{Vo})\mathrm{dt}}{\mathrm{L}} = \frac{(\mathrm{Vi} - \mathrm{Vo})\ (1 - \mathrm{D})\mathrm{T}}{\mathrm{L}} \tag{2.3}$$

The inductor current has to be the same at the start and end of the commutation cycle due to the energy stored in the components. Therefore, the overall change current is zero as the equation below:

$$\Delta \mathrm{IL_{On}} + \Delta \mathrm{IL_{Off}} = 0 \tag{2.4}$$

Substituting ΔIL_{On} and ΔIL_{Off} by their expressions yields:

$$\Delta \mathrm{IL_{On}} + \Delta \mathrm{IL_{Off}} = \frac{\mathrm{Vi\ DT}}{\mathrm{L}} + \frac{(\mathrm{Vi} - \mathrm{Vo})(1 - \mathrm{D})\mathrm{T}}{\mathrm{L}} = 0 \tag{2.5}$$

This can be written as:

$$\frac{\mathrm{Vo}}{\mathrm{Vi}} = \frac{1}{1-\mathrm{D}} \tag{2.6}$$

This in turn reveals the duty cycle to be:

$$\mathrm{D} = 1 - \frac{\mathrm{Vi}}{\mathrm{Vo}} \tag{2.7}$$

From the above expression it can be seen that the output voltage is always higher than the input voltage (as the duty cycle goes from 0 to 1), and that it increases with D, theoretically to infinity as D approaches 1. This is why this converter is sometimes referred to as a *step-up* converter.

2.4 Power Factor Correction

The power factor of an ac source is determined as the ratio between the real power and apparent power flow to the load in the circuit at the rate from 0 to 1 [6]. Real power is requirement power of the work at the exact time when the work being performed and apparent power is the feedback power given by the components circuit when the circuit operate. At some point, the apparent power may exceed the real power when the energy stored in the load and returned to the source, or due to a non-linear load that distorts the wave shape of the current drawn from the source.

In an electric power system, the power factor problem can occur at in so many causes and the drawn current from the low power factor has increases the real power to be supply which also needs the large size of components. Therefore, the costs may remain the first priority on the charges from the utilities when the low power factor drawn by the consumer that normally the industrial or commercial sector. The domestic consumer is not count on the surcharge but the low power factor problem may affect the

equipment been used and also damage some of the other equipment that is sensitive to the distortion and some kind of problem cause by the low power factor.

2.4.1 Power Factor Correction of Linear Loads

The desirable power factor on the load is nearly unity or 1, when real and apparent power is in the same line. The angle between the two powers is 0, but due to the reactive power drawn by the components being use, the unity power factor is not achievable. Therefore, power factor correction may be applied by an electrical power transmission utility to improve the stability and efficiency of the transmission network. Individual electrical customers who are charged by their utility for low power factor may install correction equipment to reduce those costs.

Power factor correction brings the power factor of close to 1 by supplying reactive power of opposite sign by adding the capacitors or inductors that act to cancel the inductive or capacitive effects of the load, respectively. In the electricity industry, inductors are said to *consume* reactive power and capacitors are said to *supply* it, even though the reactive power is actually just moving back and forth on each AC cycle.

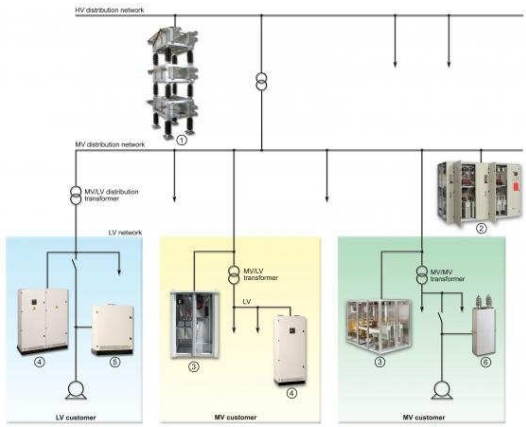


Figure 2.3 Capacitor Bank on the LV transmission Line.

2.4.2 Power Factor Correction in Non-linear Loads.

A non-linear load on a power system is typically a rectifier (such as used in a power supply), or some kind of arc discharge device such as a fluorescent lamp, electric welding machine, or arc furnace [7]. The current in these systems is interrupted by a switching action which containing the frequency components that are multiples with the power system frequency and create the harmonics distortion on the system. The distortion power factor describes how the harmonic distortion of a load current decreases the average power transferred to the load.

$$distortion\ power\ factor = \frac{1}{\sqrt{1 + THDi^2}} = \frac{I_{1,rms}}{I\ rms} \tag{2.8}$$

$THDi$ is the total harmonic distortion of the load current and assumes that the voltage stays undistorted (sinusoidal, without harmonics). This simplification is often a good approximation in practice. $I_{1,rms}$ is the fundamental component of the current and $I\ rms$ is the total current - both are root mean square-values. The result when multiplied with the displacement power factor (DPF) is the overall, true power factor or just power factor (PF):

$$PF = DPF\ \frac{I_{1,rms}}{I\ rms} \tag{2.9}$$

2.4.2.1 Passive Power Factor Correction

The simplest way to control the harmonic current is to use a filter which is possible to design a filter that passes current only at line frequency (e.g. 50 or 60 Hz). This filter reduces the harmonic current, which means that the non-linear device now looks like a linear load but the used of capacitor and inductor however to brings the

power factor will need to high current value of inductor and capacitor which is expensive and bulky. The design of passive power factor correction (PFC) is only used the passive components which are inductor and capacitor as the circuit below:

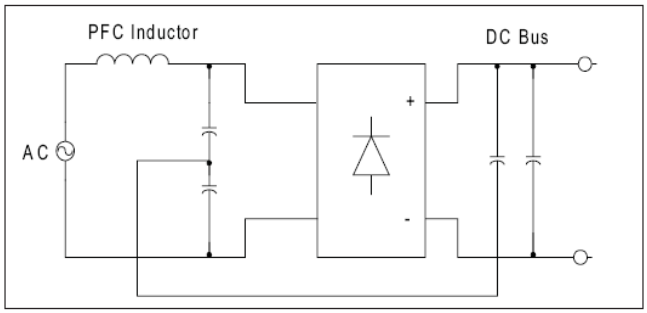


Figure 2.4 A Passive PFC circuit requires only a few components [11].

The passive PFCs are typically more power efficient than active PFCs when used for switching computer PSU with typically around 96% for passive, while an active PFC has efficiency of about 94% [12]. Although pleasantly simple and robust, a passive PFC rarely achieves low Total Harmonic Distortion (THD) and also because of the circuit has operates at the low line power frequency of 50Hz or 60Hz.

2.4.2.2 Active Power Factor Correction

The preferable type of PFC is Active Power Factor Correction and it a power electronic system that changes the wave shape of current drawn by a load to improve the power factor. The purpose is to make the load circuitry that is power factor corrected appear purely resistive (apparent power equal to real power) [9]. In this case, the voltage and current are in phase and the reactive power consumption is zero and that will be benefit to the efficiency of the used power by the consumer.

The active power factor correction manipulates the switched-mode power supply (SMPS), which is the conversion of power in the other form. First the SMPS convert an

AC source to a DC bus, using a bridge rectifier or similar circuit. The output voltage is then derived from this DC bus. The problem with this is that the rectifier is a non-linear device, so the input current is highly non-linear. That means that the input current has energy at harmonics of the frequency of the voltage. Therefore the active PFC is use to compensate with the DC link by control the switching scheme. The common types of active filter are:

1. Boost
2. Buck
3. Buck-Boost

In the case of a switched-mode power supply, a boost converter is inserted between the bridge rectifier and the main input capacitors. The boost converter attempts to maintain a constant DC bus voltage on its output while drawing a current that is always in phase with and at the same frequency as the line voltage. Another switch mode converter inside the power supply produces the desired output voltage from the DC bus. This approach requires additional semiconductor switches and control electronics, but permits cheaper and smaller passive components. It is frequently used in practice. For example, SMPS with passive PFC can achieve power factor of about 0.7–0.75, SMPS with active PFC, up to 0.99 power factor, while a SMPS without any power factor correction has a power factor of only about 0.55–0.65 [10].

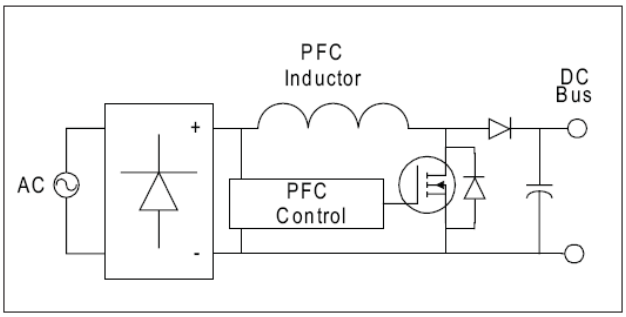


Figure 2.5 An active PFC circuit produces low THD [11].

Active PFC offers better THD and is significantly smaller and lighter than a passive PFC circuit. The reducing size and cost of passive filter elements, an active PFC operates at a higher switching frequency than the 50Hz/60Hz line frequency as the Figure 2.5 shown the active PFC.

2.5 3-Phases Induction Motor

An induction or asynchronous motor is a type of AC motor where power is supplied to the rotor by means of electromagnetic induction. These motors are widely used in industrial drives, particularly polyphone induction motors, because they are robust and have no brushes. Their speed can be controlled with a variable frequency drive [3]. The advantage is that the three phase motor is more efficient and economical than the single phase motor. Also the starting current in three phase motor is less severe than in single phase motor. The following table provides comparisons of the benefits of AC and DC drive technologies.

Table 2.1: Comparisons of the benefits of AC and DC drive technologies [4]

Criteria	DC Drives	AC Drives
Drive complexity	Low	High
Motor complexity	High	Low
Inherent fault protection	No (needs fuses)	Yes
Lifetime maintenance	Required (Motor brushes)	Low (Bearings)
Control performance	Low	High (Closed loop control)

2.5.1 Features of Standard AC Motors

The squirrel cage induction motor is the electrical motor type most widely used in industry. This leading position results mainly from certain excellent features of the squirrel cage motor such as:

a) Uncomplicated, rugged construction. For the user this means low initial cost and high reliability.
b) Good efficiency coupled with low maintenance costs resulting in low overall operating costs.

Squirrel cage motors are asynchronous induction machines whose speed depends upon applied frequency, pole pair number, and load torque. At a constant supply voltage and frequency, if the effect of temperature variations is disregarded, the motor torque will depend upon slip. At a positive slip, the squirrel cage machine will act as a motor - at a negative slip, as a generator. To reverse the machine's direction of rotation, the phase sequence to the motor must be changed. Assuming similar conditions, the phase current drawn by a squirrel cage motor will depend only on the slip. A motor running at synchronous speed will only draw minimum current.

2.5.2 Frequency Controlled Squirrel Cage Motors

In order to use the polyphase AC motor as an adjustable speed device, it is necessary to control and adjust the frequency of the 3 f power applied to its terminals. The operating speed of the AC motor is determined by the following relationship:

$$\text{Shaft Speed (RPM)} = \frac{120 \text{ x Supply Frequency}}{2 \text{ x Pole Pair Number}} - \text{ Slip (RPM)} \tag{2.10}$$

In frequency converter drives, squirrel cage motors are usually run within the range between the peak torques. The single-phase equivalent circuit of the motor, shown in Figure 2, can be used to obtain equations for the torque T, the peak torque T_h and the slip D_{nn} corresponding to the peak torque. The equations are based on the assumption that the magnitude of the phase current I_1, does not affect the voltage U_i.

$$T = 3p \left(\frac{Ui}{\omega 1}\right) 2 . \frac{R'2}{\omega 2} . \frac{1}{\left(\frac{R'2}{\omega 2}\right)^2 + (L'2\sigma)^2} \tag{2.11}$$

$$Th = 3p \left(\frac{Ui}{\omega 1}\right) 2 . \frac{1}{2L'2\sigma} \tag{2.12}$$

$$\Delta n_h = \frac{R'2}{L'2\sigma} . \frac{1}{2 \text{ x } p} \tag{2.13}$$

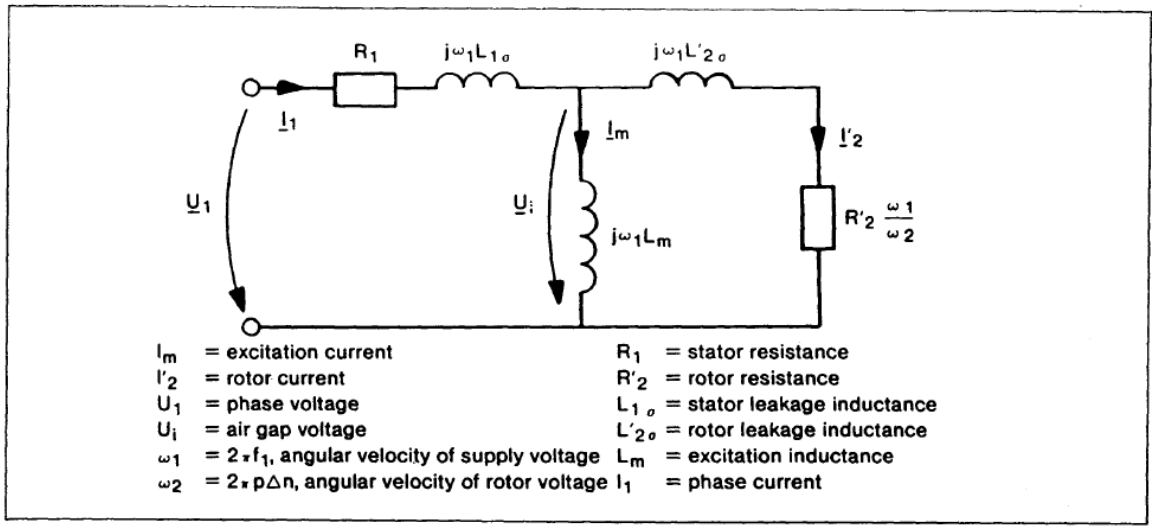


Figure 2.6 Single phase equivalent circuit for squirrel cage motor [5]

CHAPTER 3

METHODOLOGY

3.1 Introduction

The consequences of the method that have been used are described on this chapter, where the technique of the project was discussed. The methodology consists of systematic study of methods that are, can be, or have been applied within a discipline on the project title. On this chapter, the aspect of boost converter with power factor correction (PFC) is discussed as to find the technical on the objective achievement. In General, the methodology can be defined as:

a) Boost PFC characteristic:

1. Power Components Selection.
2. Feedback Arrangement.
3. Input Voltage Sensing.
4. Current Sense Network.

b) Testing procedure:

1. Start up at low line, full load.
2. PF, THD, Efficiency at 110 Vac, full load.
3. PF, THD, Efficiency at 230 Vac, full load.

3.2 Boost PFC Characteristic

A boost converter (step-up converter) is a power converter with an output DC voltage greater than its input DC voltage. It is a class of switching-mode power supply (SMPS) containing at least two semiconductor switches (a diode and a transistor) and at least one energy storage element. Filters made of capacitors (sometimes in combination with inductors) are normally added to the output of the converter to reduce output voltage ripple. The designed boost converter has the capability to effectively drive a high power, universal line application. The impotency, it is designed to meet the following specifications:

- Maximum output power: 300 W
- Input voltage range: from 85 V_{RMS} to 265 V_{RMS}
- Regulation output voltage: 390 V
- Switching frequency: 65 kHz

The design of boost power factor correction is generic as the NCP 1654 architecture recommended for the application between the 100 to 400W load power. Figure below show the reference schematic for the calculation:

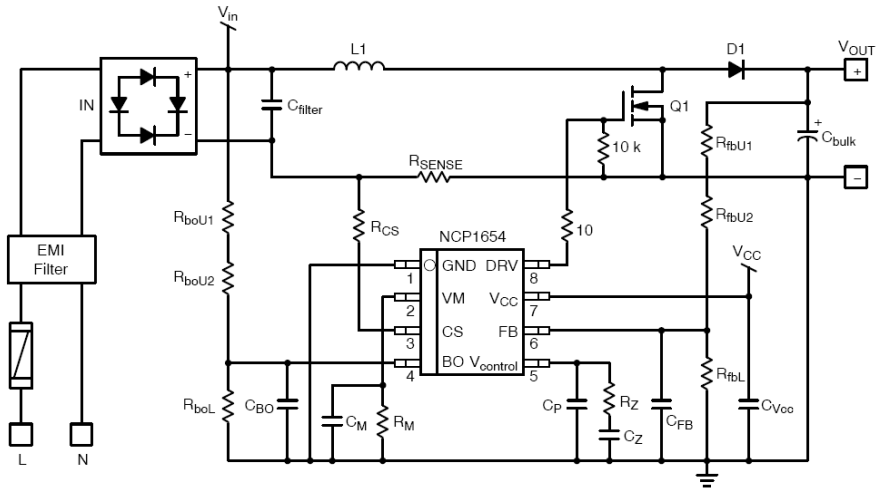


Figure 3.1 NCP 1654 schematic application for boost PFC [12].

The source of the converter is an AC source of single line, therefore the bridge rectifier is used to get the DC output on the load side. The regulation voltage is the important on the circuit design which the main result is considered to obtain the power factor at the high value that nearly 1. The critical option may come from the reselected of the components to design and compensated the power switch for regulate the value of DC output to the constant value. The key principle that drives the boost converter is the tendency of an inductor to resist changes in current between the states of the operation switch on the switching schemes. A boost converter is used as the voltage increase mechanism in the circuit known as the 'Joule thief'. This circuit topology is used with low power battery applications, and is aimed at the ability of a boost converter to 'steal' the remaining energy in a battery

3.2.1 Power Components Selection

Basically, the coil, the bulk capacitor and the power silicon devices are dimensioned “as usually”, that is, as done with any other CCM PFC. This section does not detail this process, but simply states some key points.

1. **Coil Selection**

One generally selects the coil to limit the current ripple below a certain pre−determined level, for instance ±15% when the input current is maximum. The input current amplitude, I_{in}, is maximum at low line and high power. Hence,

$$I_{in,max} = \frac{\sqrt{2}\ P\ out, max}{n\ .\ V_{acLL}} \tag{3.0}$$

Where $P_{out,\ max}$ is the maximum output power, η the efficiency and V_{acLL} the AC line lowest level. On the other hand, one could show that at the sinusoid top, the peak−to−peak ripple of the coil current is given by the following equation:

$$\frac{\sqrt{2}\,\mathrm{V}ac}{L\ .\ f_{sw}}\ (1-\frac{\sqrt{2}\,\mathrm{V}ac}{\mathrm{V}out}) \tag{3.1}$$

Where f_{sw} is the operating frequency. Typically, one targets the peak−to−peak ripple between 10 and 50% of the AC line current maximum amplitude, $I_{in,\ max}$. Therefore if the targets a ±18% ripple at low line, i.e. Icoil, pp is 36%, the coil inductance, L, is given by the following equation:

$$\frac{\sqrt{2}\,\mathrm{V}acLL}{L\ .\ f_{sw}}\left(1-\frac{\sqrt{2}\,\mathrm{V}acLL}{\mathrm{V}out}\right)=36\ \%\ \frac{\sqrt{2}\ P\ out,max}{n\ .\ VacLL} \tag{3.2}$$

Hence, the coil inductance is:

$$L=\frac{n\ .\ VacLL^2}{0.36\ .\ f_{sw}\ .\ P\ out,max}\ (1-\frac{\sqrt{2}\,VacLL}{Vout}) \tag{3.3}$$

Finally, if one neglects the switching ripple of the coil current, its rms value equates the rms AC line current. In other words:

$$I_{coil,rms}=\frac{P\ out}{n\ .\ Vac} \tag{3.4}$$

The maximum RMS current of the coil is then:

$$I_{coil,rms,max}=\frac{P\ out,max}{n\ .\ VacLL} \tag{3.5}$$

2. Power Silicon Devices

Generally, the diode bridge, the power MOSFET and the output diode will be placed on the same heatsink. As a rule of the thumb, one can estimate that the heatsink will have to dissipate around:

- 6% of the output power in wide mains applications
  (92% being generally the targeted minimum efficiency)
- 3% of the output power in European mains applications

Among the sources of losses that contribute to this heating, there are listed as:

i. The diodes bridge conduction losses that can be estimated by the following equation:

$$P\ bridge = \frac{4\sqrt{2}}{\pi}\ \frac{Vf}{VacLL}\ \frac{Pout}{n}\ \approx 1.8\ \frac{Vf}{VacLL}\ \frac{Pout}{n} \tag{3.6}$$

Where V_f is the forward voltage of the ridge diodes.

ii. The MOSFET conduction losses, that if one neglects the current ripple, are given by:

$$P_{on,max} = R_{DS\ (on)} \cdot \left(\frac{P_{in,max}}{VacLL}\right)^2 \cdot \left(1 - \frac{8\sqrt{2}\ VacLL}{3\pi Vout}\right) \tag{3.7}$$

iii. The output diode conduction losses: ($I_{out} \cdot V_f$), where I_{out} is the load current and V_f is the diode forward voltage. The maximum output current being nearly 0.77 A (= 300 W / 390 V), the diode conduction losses are in the range of 0.77 W (assuming Vf = 1.0 V).

The diode and MOSFET switching losses are highly dependent on the diode choice, on the MOSFET drive speed and on the possible presence of some snubbering circuitry. Hence, their prediction is tough and inaccurate exercises that will not be calculate on this methodology. Instead, they are just assumed to be part of the power budget initially specified for the heatsink (6% of Pout in our case).

3. Output Bulk Capacitor

The bulk capacitance had to satisfy two requirements, which are the output double line frequency ripple and hold−up time.

a) *Output Voltage Ripple Requirement*.

The bulk capacitance always presents the voltage ripple of double line frequency (100 or 120 Hz ripple exhibited by the bulk voltage. The voltage ripple constraint requires that:

$$C_{bulk} > \frac{Pout}{\delta V_{pp,max} \,.\, \omega \,.Vout} \tag{3.8}$$

Where Vpp, max is the maximum permissible peak to peak voltage ripple and ω is the AC line angular frequency.

b) Hold up Time Requirement.

If some hold−time requirement was specified, this would lead to the following additional constraint:

$$C_{bulk} > \frac{2P_{out} \,.\, t_{HOLD}}{{V_{out1}}^2 - {V_{out2}}^2} \tag{3.9}$$

Where V_{out1} is the nominal output voltage, V_{out2} is the minimum acceptable level of V*out*, and tHOLD is the hold−up time. The C_{bulk} capacitance should be higher than the calculated value from above two requirements.

c) Bulk Capacitor Heating.

It must also be checked that the ESR is low enough to prevent the rms current that flows through it, from overheating the bulk capacitor. This rms current depending on the input impedance of the downstream converter that is not computed here.

The calculation of the power components selected is referred to the formula as the table below:

Table 3.1 Formula for selected power components of boost PFC.

Steps	Components	Formula
Step 1: Coil Inductance, Bulk Capacitor and Power Silicon	Select the maximum switching peak to peak ripple of the coil current	Choose a value between 10 and 50% $\varrho = \frac{\Delta I_{coil,pp}}{I_{in,max}}$
	Coil inductance (L)	$L = \frac{\eta \cdot V_{acLL}{}^2}{\varrho \cdot f_{sw} \cdot P_{out,max}} \left(1 - \frac{\sqrt{2} V_{acLL}}{V_{out}}\right)$
	Maximum rms coil current	$I_{coil,rms,max} = \frac{P_{out,max}}{\eta \cdot V_{acLL}}$
	Maximum coil current	$I_{coil,max} = \sqrt{2}\left(1 + \frac{\varrho}{2}\right)\frac{P_{out,max}}{\eta \cdot V_{acLL}}$
	Bulk Capacitor (ripple voltage consideration)	$C_{bulk} > \frac{P_{out}}{\delta V_{pp,max} \cdot \omega \cdot V_{out}}$
	Bulk Capacitor (Hold up time consideration)	$C_{bulk} > \frac{2P_{out} \cdot t_{HOLD}}{V_{out1}{}^2 - V_{out2}{}^2}$

3.2.2 Feedback Arrangement

The feedback arrangement is for the MOSFET's applications where the feedback needed to generic the error of the on the system loop. This pin receives a feedback signal V_{FB} that is proportional to the PFC circuits' output voltage. This information is used for the output regulation, the overvoltage protection (OVP), and output under voltage protection (UVP) to protect the system from damage at feedback abnormal situation. When V_{FB} goes above 105% V_{REF}, OVP is activated and the Drive Output is disabled. When V_{FB} goes below 8% V_{REF}, the device enters a low−consumption shutdown mode. As shown by Figure 2.1 before, the feedback arrangement consists of:

a) CFB, a filtering capacitor to avoid that some switching noise may be injected into FB pin. A capacitor ranging from 100 pF to 1 nF is traditionally implemented.

b) R_{fbU1}, R_{fbU2}, and R_{fbL} set output voltage. In practice, one generally implements more resistors as upper side feedback loop for safety consideration. Refer to Figure 1, given that Vout is a high voltage, an accidental shortage of the feedback resistor would destroy the controller. That is why it is better to have several series resistors instead of only one.

First, there is need to choose the value of the lower resistor, R_{fbL}. There is a trade−off between the noise immunity and the power losses when choosing R_{fbL}. The value of upper resistor R_{fbU} is then given by:

$$R_{fbU} = \frac{V_{out} - V_{REF}}{V_{REF}} R_{fbL} \tag{3.10}$$

Where V_{REF} is the internal reference voltage for V_{out} feedback (2.5 V typical) and $R_{fbU} = R_{fbU1} + R_{fbU2}$ is the total feedback resistor placed between V_{out} and FB pin.

The compensation controller is set by the value of C_P, C_Z, and R_Z that were connected to $V_{control}$ pin acts as a type−2 compensation loop to set the regulation bandwidth. It is recommended to set the bandwidth below 20 Hz for an effective filtering of the 100 or 120 Hz ripple. If CZ is >> CP, the transformer of Vout to Vcontrol is state as:

$$\frac{V_{control}}{V_{out}} = \frac{R_{fbL} \,.\, G_{EA}\, R_Z}{R_{fbL} + R_{fbU}} \cdot \frac{1 + sR_ZC_Z}{sR_ZC_Z\,(1 + sR_ZC_P)} \tag{3.11}$$

Where G_{EA} is the error amplifier gain. Then this compensation provides one original pole, one low frequency zero:

$$f_Z = \frac{1}{2\pi \,.\, R_Z \,.\, C_Z} \tag{3.12}$$

and one high frequency pole:

$$f_P = \frac{1}{2\pi \,.\, R_Z \,.\, C_P} \tag{3.13}$$

The calculation of the feedback arrangement is referred to the formula as the table below:

Table 3.2 Formula for feedback arrangement.

Step 2: Feedback Arrangement	$R_{fbU1} + R_{fbU2} + R_{fbL}$	$(R_{fbU1} + R_{fbU2}) = \frac{V_{out} - V_{REF}}{V_{REF}} R_{fbL}$
	C_{FB}	C_{FB} = 100 pF ~ 1 nF
	C_P, C_Z, R_Z	$\frac{V_{control}}{V_{out}} = \frac{R_{fbL} \cdot G_{EA} R_Z}{R_{fbL} + R_{fbU}} \cdot \frac{1 + sR_ZC_Z}{sR_ZC_Z(1 + sR_ZC_P)}$

3.2.3 Input Voltage Sensing

At the input voltage sensing, the important work of pin V_{BO} and the pin connected a resistor network among the rectified input voltage, BO pin, and ground with connection of a capacitor between BO pins and ground. The BO pin detects a voltage signal proportional to the average input voltage. When V_{BO} goes below V_{BOL}, the circuit that detects too low input voltage conditions (brown− out), turns off the output driver and keeps it in low state until V_{BO} exceeds V_{BOH}. This signal which is proportional to the RMS input voltage Vac is also for overpower limitation (OPL) and PFC duty cycle modulation.

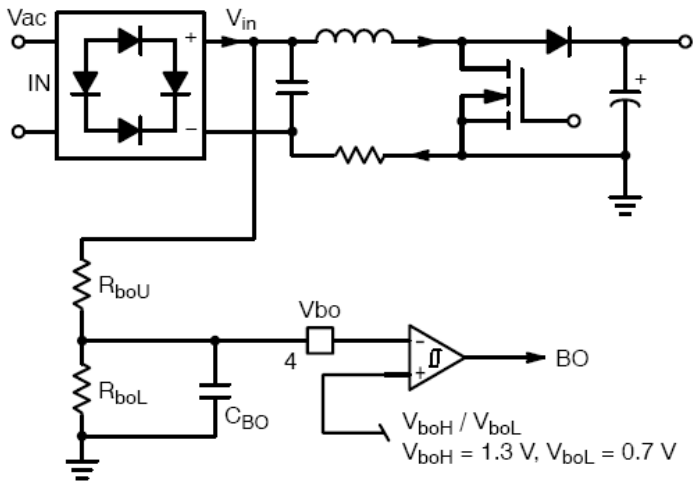


Figure 3.2 Brown−Out protections [12].

Refer to Figure 2.2, the NCP1654 monitors the input voltage, Vin, which is the rectified AC line sinusoid for brown−out, over−power limitation (OPL), and PFC duty cycle modulation. This sensing circuit consists of:

a) R_{boU} (= R_{boU1} + R_{boU2} in Figure 2.1) and R_{boL} are dimensioned to adjust the threshold of brown out protection. Because of the safety consideration, it is recommended to split this upper side brown out resistor into 2 or more resistors.

b) C_{BO} that forms a low pass filtering together with R_{boL} to get the average value of input signal. A time constant in the range of around 5 times the Vin period

should be targeted to make V_{bo} substantially constant and proportional to the mean input voltage as the rule of thumb:

$$V_{bo} = \frac{R_{boL}}{R_{boL} + R_{boU}} < V_{in} > \tag{3.14}$$

The NCP1654 starts to operate as V_{bo} exceeds 1.3 V and keeps operating until V_{BO} goes below 0.7 V. The 600 mV hysteresis prevents the system from oscillating. As shown in Figure 2.2, before the device operates, V_{in} is kept at peak value of the input ac line sinusoid, Vac, that is, $\sqrt{2}$ Vac which leads to:

$$V_{bo} = \frac{R_{boL}}{R_{boL} + R_{boU}} < V_{in} > = \frac{R_{boL}}{R_{boL} + R_{boU}} \sqrt{2} V_{ac} \tag{3.15}$$

After the device operates, V_{in} is the rectified sinusoidal input voltage, which average value becomes $\frac{2\sqrt{2}}{\pi} V_{ac}$ which leads to:

$$V_{bo} = \frac{R_{boL}}{R_{boL} + R_{boU}} \frac{2\sqrt{2}}{\pi} V_{ac} \tag{3.16}$$

First, the parameter of R_{boL}. R_{boL} should be relatively high impedance to limit the current within R_{boL} and R_{boL} and the associated losses. However, the given bias current of the brown−out comparator is 0.5 A maximum, it is recommended to set the current flowing through R_{boU} and R_{boL} to be in the range or higher than 5 _A at low line.

Second, select R_{boU} according to $V_{ac,on}$, the minimum AC input voltage to start PFC, which comes from:

$$R_{boU} = \frac{\sqrt{2} V_{ac,on} - V_{BOH}}{V_{BOH}} R_{boL} \tag{3.17}$$

Third, select C_{BO} to make the time constant be around 5 times TV_{in}, the cycle time of V_{in} by:

$$C_{BO} \approx \frac{5 \cdot T_{Vin}}{R_{boL}} \tag{3.18}$$

Fourthly, check $V_{ac,off}$, the PFC brown−out off threshold of AC input voltage due to the ripple voltage on V_{bo}, the minimum value of V_{bo} is around:

$$V_{bo} = K_{BO} \cdot \frac{2\sqrt{2}}{\pi} V_{ac} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}}\right) \tag{3.19}$$

Where K_{BO} is the scaling down factor of the BO network:

$$K_{BO} = \frac{R_{boL}}{R_{boU} + R_{boL}} \tag{3.20}$$

f_{BO} is the corner frequency of the BO filter:

$$f_{BO} = \frac{R_{boL} + R_{boU}}{2\pi \cdot R_{boL} \cdot R_{boU} \cdot C_{BO}} \tag{3.21}$$

The brown−out function turning off the device is when V_{BO}, minimum equal to V_{BOL}, the threshold voltage of brown out comparator, which leads to:

$$K_{BO} \cdot \frac{2\sqrt{2}}{\pi} V_{ac,off} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}}\right) = V_{BOL} \tag{3.22}$$

Hence , the $V_{ac,off}$ is equal to:

$$V_{ac,off} = \frac{V_{BOL}}{K_{BO} \cdot \frac{2\sqrt{2}}{\pi} V_{ac,off} \cdot \left(1 - \frac{f_{BO}}{3 \cdot f_{line}}\right)} \tag{3.23}$$

The calculation of the Input voltage sensing is referred to the formula as the table below:

Table 3.3 Formula of input voltage sensing for NCP 1654.

Step 3: Input Voltage Sensing	$R_{boU1} + R_{boU2} + R_{boL}$	$(R_{boU1} + R_{boU2}) = \frac{\sqrt{2}V_{ac,on} - V_{BOH}}{V_{BOH}} R_{boL}$
	C_{BO}	$C_{BO} \approx \frac{5 \cdot T_{Vin}}{R_{boL}}$

3.2.4 Current Sense Network

This pin sources a current I_{CS} which is proportional to the inductor current I_L. The sense current I_{CS} is for over current protection (OCP), overpower limitation (OPL) and PFC duty cycle modulation. When ICS goes above 200 _A, OCP is activated and the Drive Output is disabled. The current sense circuitry consists of:

a) A current sense resistor R_{SENSE}.

The resistor is free select and implement on the current sense resistor, R_{SENSE} but need to choose a second resistor R_{CS} to adjust the over current threshold. If one neglects the ripple current, maximum RSENSE losses can be estimated by the following equation:

$$PR_{SENSE}, \max = R_{SENSE} \cdot \left(\frac{P_{out,max}}{n \cdot V_{acLL}}\right)^2 \tag{3.24}$$

As a rule of the thumb, one can choose R_{SENSE} so that its dissipation does not exceed 0.5% of $P_{out,max}$. This criterion leads to:

$$R_{SENSE} \leq 05\% \cdot \frac{(n \cdot V_{acLL})^2}{P_{out,max}} \tag{3.25}$$

b) A resistor RCS that sets the current limit threshold.

Simply select RCS in order to set the desired over current limit:

$$R_{CS} = \frac{R_{SENSE} \cdot I_{coil,max}}{I_{S(OCP)}} \tag{3.26}$$

Where Icoil, max is the maximum coil current $I_{S(OCP)}$ is the internal over current protection threshold (200uA typical). To keep the design margin, it is recommended to use the minimum value of $I_{S(OCP)}$, 185uA to design R_{CS}.

c) A resistor R_M that adjusts the PFC stage power capability and a capacitor C_M.

The R_M adjusts the maximum power the PFC stage can supply given the chosen output voltage level. The following equation is use to select R_M:

$$R_M = 70\% \cdot n \frac{2\pi R_{CS} \cdot \Delta V_{CONTROL} \cdot V_{REF}}{\sqrt{2} R_{SENSE} K_{BO} V_{outLL} P_{out,max}} \cdot V_{acLL} \tag{3.27}$$

Where:

- $\Delta V_{CONTROL}$ is the operating range of $V_{control}$ (3 V).
-V_{REF} is the internal voltage reference (2.5 V).
-V_{acLL} is the lowest level of the AC line rms voltage.
-$P_{out,max}$ is the maximum output power with η is the efficiency of V_{acLL} and $P_{out,max}$.
-K_{BO} is the scale down factor betweenV_{in} and V_{BO}.
-V_{outLL} is the output voltage corresponding to V_{acLL} in full load conditions. In traditional mode, V_{outLL} is the targeted regulation level (390 V in general).
-70% is to take into account the i_m dispersion.

For a correct filtering of Ics, the time constant (RM .CM) should be taken in the range of 5 times the operating cycle period, i.e. 5. 1/fsw. This time constant is large

enough to filter the switching ripple and low enough not to distort the low frequency component, that is the 100 or 120 Hz rectified sinusoid. Hence:

$$C_M \approx 5 . \frac{1}{R_M f_{sw}} \tag{3.28}$$

The calculation of the Current Sense Network is referred to the formula as the table below:

Table 3.4 Formula of current sense network for NCP 1654.

Step 4: Current Sense Network	R_{SENSE}	Choose R_{SENSE} so that its dissipation keeps reasonable, e.g. select R_{SENSE} so that P_{Rsense} is less than 0.5% · $P_{out,max}$. $R_{SENSE} \leq 0.5\% \cdot \frac{(\eta \cdot V_{acLL})^2}{P_{out,max}}$
	R_{CS}	$R_{CS} = \frac{R_{SENSE} \cdot I_{coil,max}}{185\ \mu A}$
	R_M	$R_M = 70\% \cdot \eta \frac{2\pi R_{CS} \cdot \Delta V_{CONTROL} \cdot V_{REF}}{\sqrt{2} R_{SENSE} K_{BO} V_{outLL} P_{out,max}} \cdot V_{acLL}$
	C_M	$C_M \approx 5 \cdot \frac{1}{R_M f_{sw}}$

3.3 Testing Procedure

The load of the output boost PFC is needed to be verified via the testing of the power and other parameters related to the power control at a given load. As the procedure of testing equipment of the PFC, therefore the test is divided to different level of supply voltage to check the correction of the boost converter as a given supply varied from low voltage to full voltage of the supply. The testing diagram is placed as the Figure 3.3.

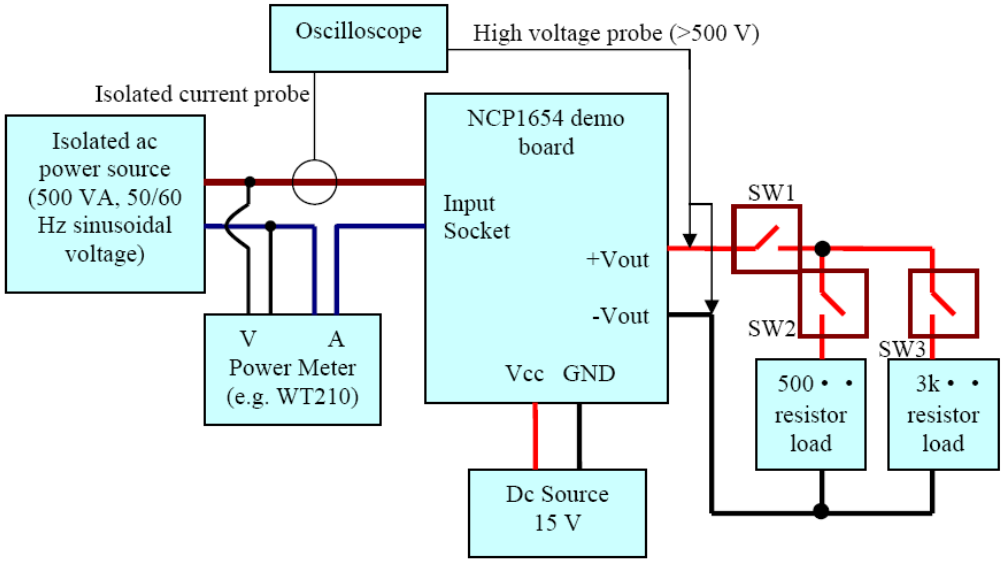


Figure 3.3 Testing diagram of the boost PFC.

3.3.1 Test 1: Start up at low line, full load

Test conditions:

1. SW1 and SW2 close SW3 open. (output load is full load)
2. AC input: 85 Vac, 50 Hz
3. V_{dc} value of 15 V dc source applied to TB3 to enable the operation.

Test criteria:

- V_{OUT} should be in the range from 378 V to 401 V.
- Input current should be sinusoidal without distortion, which is measured by oscilloscope.
- PF > 0.99
- THD < 10%

3.3.2 Test 2: PF, THD, Efficiency at 110 Vac, full load

Test conditions:

1. SW1 and SW2 close SW3 open. (output load is full load)
2. AC input: 110 Vac, 50 Hz
3. V_{DC} of 15 V dc source need to be applied to TB3 to enable the operation.

Test criteria:

- V_{OUT} should be in the range from 378 V to 401 V.
- PF > 0.99
- THD < 10%
- Efficiency > 94 %.

3.3.3 Test 3: PF, THD, Efficiency at 230 Vac, full load

Test conditions:

1. SW1 and SW 2 close, SW3 open (output load is full load)
2. AC input: 230 Vac, 50 Hz
3. Use 15 V dc source applied to TB3 to enable the operation.

Test criteria:

- V_{OUT} should be in the range from 378 V to 401 V.
- PF > 0.98
- THD < 10%
- Efficiency > 97 %.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Introduction.

At the end of the project, the objective of the project should be the most item need to be considered as achieving the goal. The title of the project, development of PC based on frequency inverter for 3-phase inverter is able to be applied as the input from the boost converter with power factor correction (PFC) is complete. On the result review, there is divided into two main views which is:

i. Simulation on the Boost with Power factor correction scheme.
ii. Hardware development

The result covered the scope of the project been specific at the chapter 1, therefore the added of the scope or other than the scope range are not considered as the main result, and that might be the outcome from the research only and not been included on this paper. However, the result consisted the part of simulation that is related but not specific on the components been used on the hardware level due to the lack of the libraries and part of the simulation tools.

4.2 Simulation of Boost converter with Power Factor Correction (PFC)

The simulation has used the PSim provided by Powersimtech Corporation which is a kind of simulation software, with the programmer are able to design a circuit and simulate with the lab view on the PSim software. The simulation has followed as the Figure 4.1.

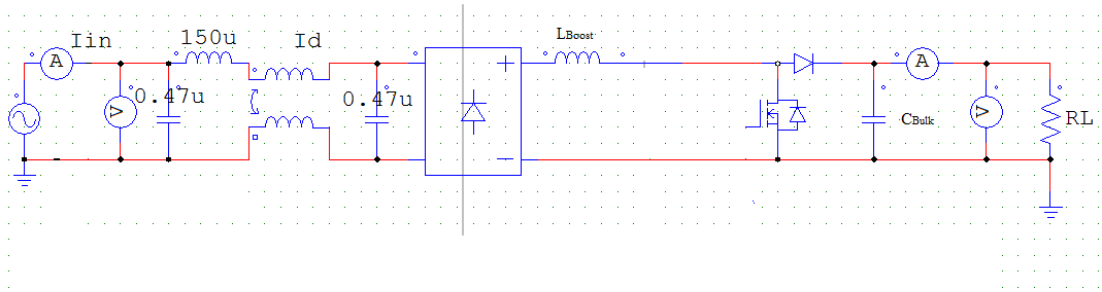


Figure 4.1 Power stage of switch mode power supply (SMPS) for Boost.

The boost converter, then applying the control circuit of the switching for compensated with the MOSFET's application. Where, the system operate in the closed loop system as the feedback from the load current is needed to generated the correction factor to feed as pulse width modulation on the MOSFET.

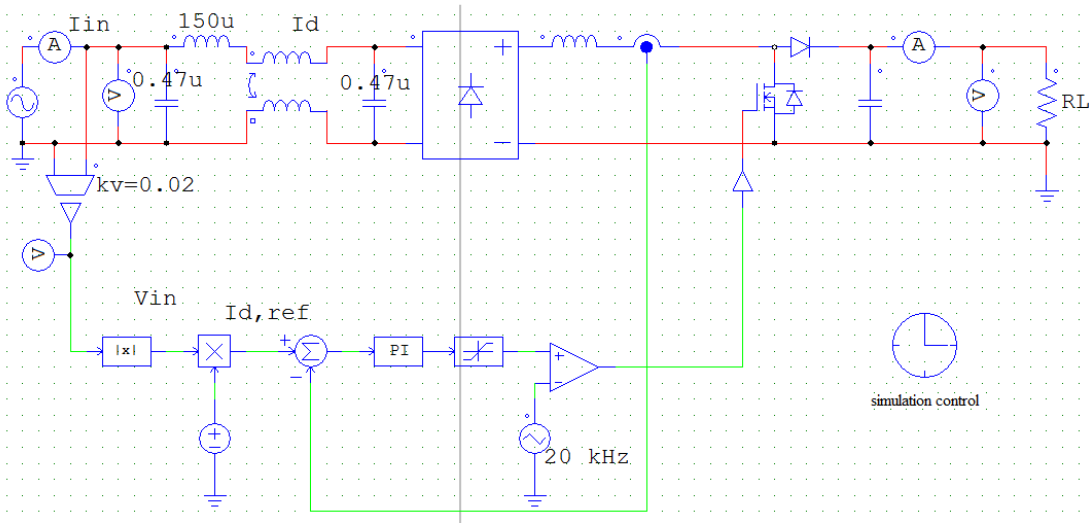


Figure 4.2 Boost PFC circuit diagram view on the PSIM software.

The simulation control on the circuit, control the simulation time been view as the simulation referred the time been added to the control. As the time put as 1 second, therefore the output for the simulation as follow:

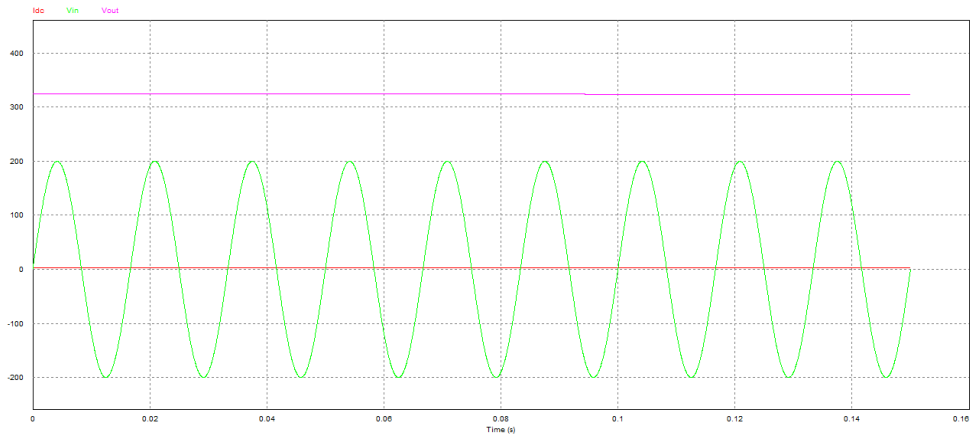


Figure 4.3 Output of the boost PFC with V_{dc}, V_{in} and I_{dc}.

The specification of the simulation components as specific as:

1. Vin, sinusoidal = 200 Vac
2. RL, as the R load = 144 Ω
3. LBoost, inductor = 470uH
4. CBulk, capacitor = 0.1F

FFT analysis has performed as to check the distortion on the voltage at the input and, the result as follow:

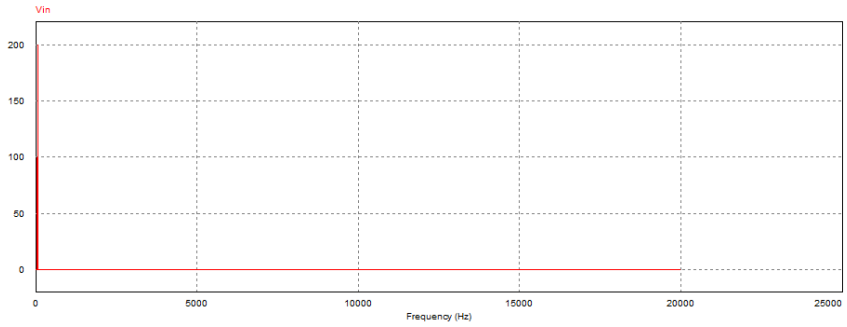


Figure 4. 4 FFT analysis of the input voltage of the circuit.

4.3 Hardware Development

On the hardware review, the boost converter with power factor correction is design as the Figure 4.5. The IC's selected on the circuit is NCP 1654 which is having the specification of the boost PFC and also consist of benefit as:

- Inrush Currents Detection
- Overvoltage Protection
- Under voltage Detection for Open Loop Detection or Shutdown
- Brown−Out Detection
- Soft−Start
- Accurate Over current Limitation
- Overpower Limitation

The NCP1654 is a controller for Continuous Conduction Mode (CCM) Power Factor Correction step−up pre−converters [13]. It controls the power switch conduction time (PWM) in a fixed frequency mode and in dependence on the instantaneous coil current. It is housed in a SO8 package, the circuit minimizes the number of external components and drastically simplifies the PFC implementation. It also integrates high safety protection features that make the NCP1654 a driver for robust and compact PFC stages like an effective input power runaway clamping circuitry. The features as:

- IEC61000−3−2 Compliant *(Note: see Appendix E)*
- Average Current Continuous Conduction Mode
- Fast Transient Response
- Very Few External Components
- Low Operating Consumption
- ±1.5 A Totem Pole Gate Drive
- Accurate Fully Integrated 65/133/200 kHz Oscillator
- Latching PWM for cycle−by−cycle Duty−Cycle Control

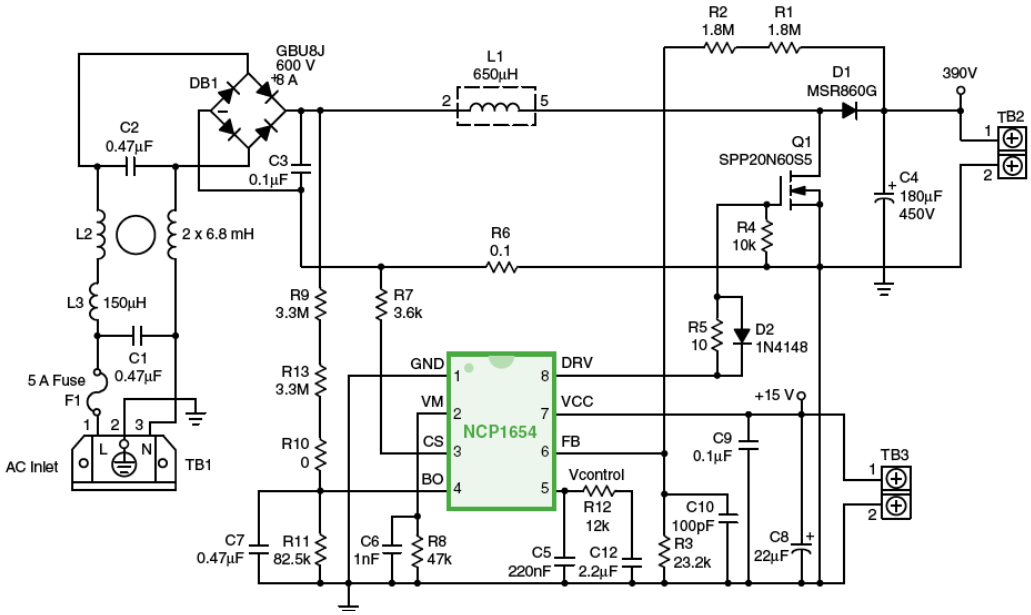


Figure 4.5 Boosts PFC with NCP Drive for 300W application load.

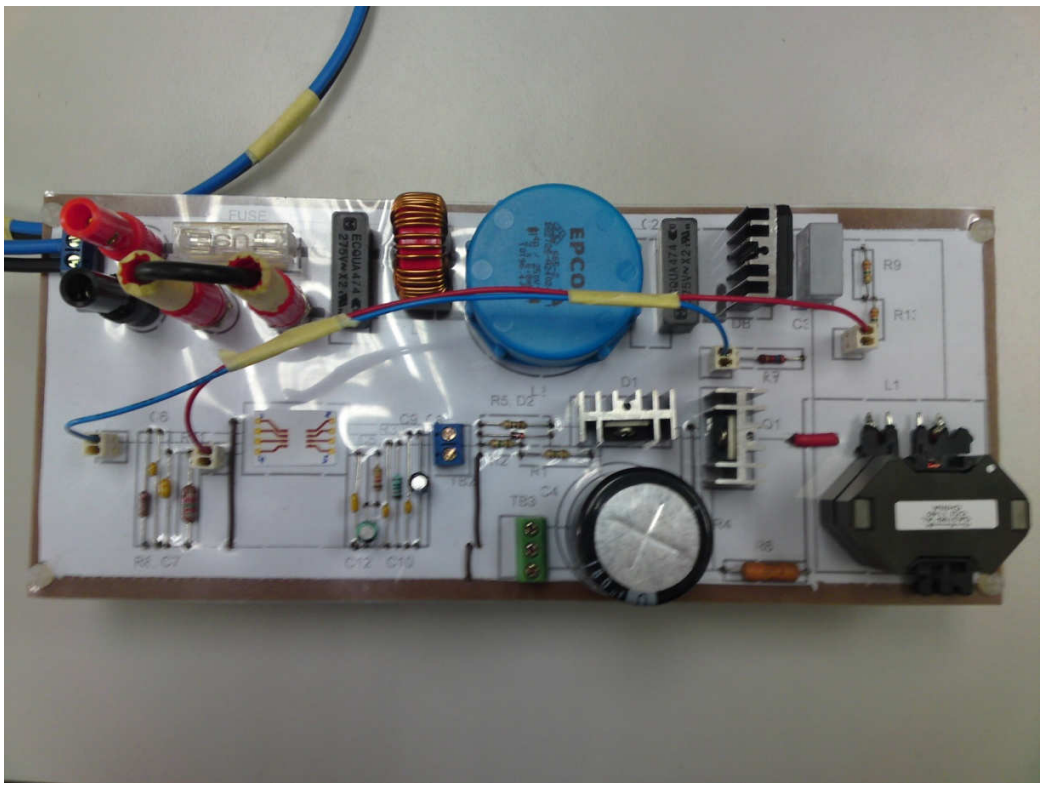


Figure 4.6 Hardware installations on the board without IC controller.

The above Figure 4.6 is the hardware installation on the board for the project without the IC controller NCP 1654 as the power stage. The NCP 1654 is a mount surface, therefore is needed an adapter to be fit on the parallel board afterward. The installation consists of power stage, from the AC inlet to the EMI filter and then connected to the boost inductor and fed on the rectifier circuit. The results of the circuit are without the controller interrupted and therefore, the only outcome of this circuit is the value of the output at the end of the terminal output DC. Figure 4.7 show the result on the volt measurement on the terminal output DC on the TB3.

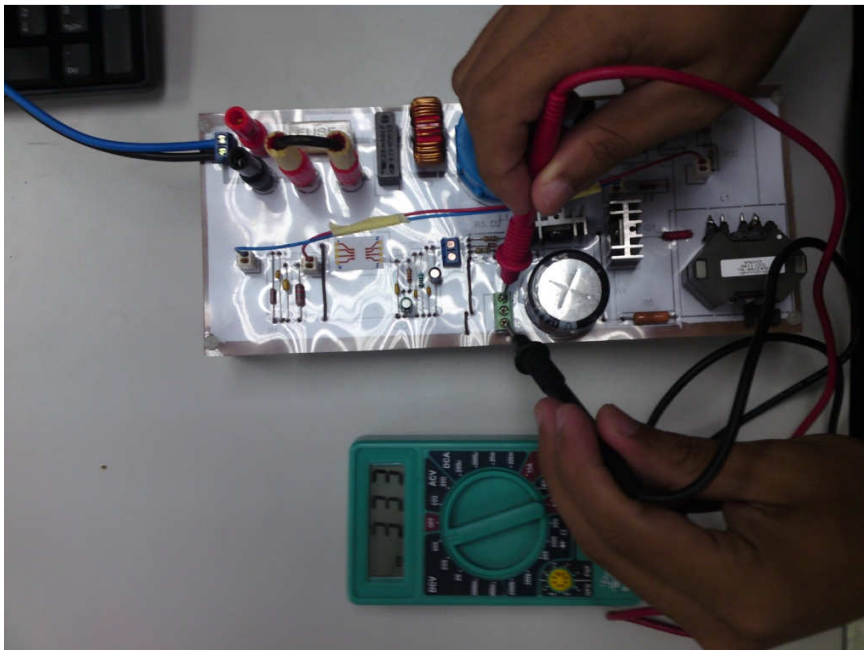


Figure 4.7 Measurements on the Output Terminal TB3.

On the measurement, the value of the output DC is 333 Vdc which rectified from 240 Vac in single phase source of the socket outlet. The power stage of this board is working as the output is constant and without disturbance due to the non-load test measurement and also the EMI used on the incoming side of the circuit. The limited of measurement to only on the voltage output which the main important point as the MOSFET switching has been used.

On the second stage, the circuit is closed loop with the installation of the NCP 1654 on the board, with the IC propose as the controller of all the circuit as refer to Figure 4.8 below.

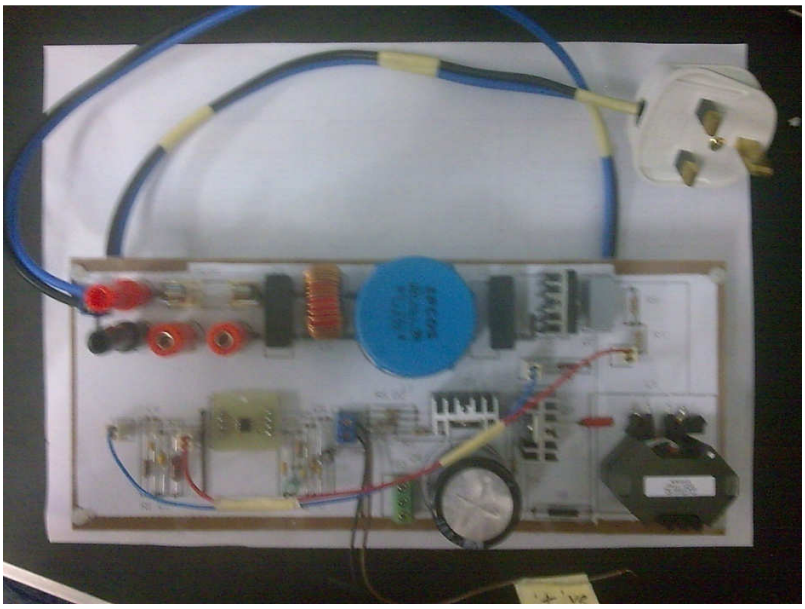


Figure 4.8 Full specification of boost PFC installed.

The circuit however is not compensated as the calculation and the value of the output voltage at output terminal is constantly same as the first stage. At same level, the controller is not on the operation mode due to same factor or problem occurs on the circuit installation. The non operation mode of the IC resulted on the apparent of constant output voltage as the regulation of the AC-DC rectifier on behalf of the power stage as elaborate on the Figure 4.7 before.

At the range of oscillation control parameter test, the disappointed misfortunes occur on the process. The first touches of the oscilloscope on the ground have suddenly increases the current and blow the 5A fuse with also bust the R_{sense}. Therefore, consequently point to the end of the process and the trouble shooting is following on the line.

The boost converter combine with the power factor correction was become the efficiency type of SMPS that are able to demonstrate the power in linear regulation either interrupted by the supply or the load. The boost circuit specific offers from the NCP 1654 given an opportunity to maintain the output voltage V_{out} to whenever the rms input voltage Vac is lower. The power electronics switching operate by the MOSFET, SPP 20N60S5 was design to control the switching scheme to specific order from PWM generate from the NCP 1654 as the sense of voltage and current on the power stage. The power factor controller is sense by the Vcontrol on the NCP 1654 where, the bandwidth is controller to near unity power factor at below 20 Hz and the soft start begin at the moment till reach it maximum power.

An EMI elimination circuit is the main important consideration on the factor that effect to the output voltage on the boost converter. The interruption from the induction or the external source may affect the power factor as well. On this project, the EMI is subject to remove by the additional circuit filter at the incoming AC inlet. The other contemplation point is the testing method, where the point of view is stress on the power factor (PF), total harmonics distortion (THD) and the voltage output when the supply drop with the variable of load switching. The consisted components are rate at several to maximum 8 Ampere, therefore the precaution on the hazardous current much occur as to respect all the components and always switch off the supply when operate the wiring or trouble shooting.

Table 4.1 Reading Value of Current and Effects

Condition	**Reading**	**Effects**
Safe current value	1mA - 8mA	Bearable to control
Unsafe current value	>8mA	Cause to burn, or worst to fatal.

4.4 Troubleshooting

The apparent result are not as expected due to the problems occurred to the circuit on the installations design. Therefore, the following lines describe the trouble shooting and procedure of implementation to the problem.

1. **Connectivity of the soldered board.**

As result of the fuse blow, the first expectation is on the short circuit that might happen between the connections on the board. Therefore, even before the supply is ON, the connectivity is count. The figure below shows the short circuit or jump current between positive and negative DC output resulted the fuse to blow.

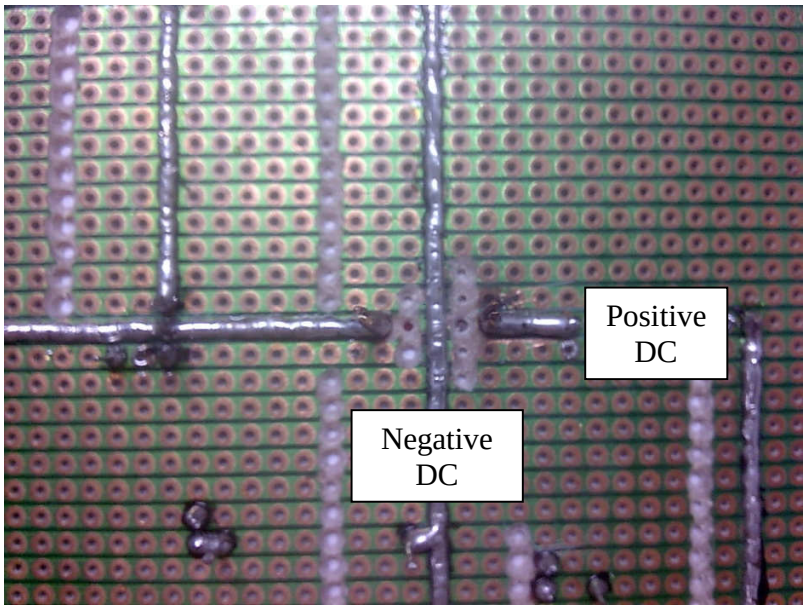


Figure 4.9 Short circuit between positive DC and negative DC.

4.5 Problem Encountered

The high power of boost converter required the high speed of switching which is unable to select the small components of inductor. Therefore, the value of boost inductor much equivalent with the current on the coil and able to bear with the selected switching frequency. On the selected switching frequency, the whole aspect of the components is considerate as the contribution on the factor of which of the controller is suitable. Therefore, the selection of the components required the theoretical aspect and put in the calculation method to verify the suitable and related value of the components selected.

On the other hand, the item selected is specific due to manufacturer output regulation and that will be limitation on the components selection. As time viewing, the selection of components is acquire some sort of time which can be as much as a month and the time occupied alongside the ordering to delivery plot.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

5.1 Conclusions

Application of Power Electronics on the SMPS has given the opportunity to gain power with the use of a fixed input even for the biggest needed output. The boost converter has generated more power from the low input that to be used on the biggest output. At this paper, the boost converter is been used as the input for the frequency inverter for 3-phase AC motor drive. The boost PFC IC's, NCP1654 is an ideal components in the systems where cost effectiveness, reliability and high power factor as the parameters. It incorporates all the necessary features to build a compact and rugged PFC stage such as Compactness and Flexibility with also featuring with safety precaution on the system by attempted with under voltage Protection for Open Loop Protection or Shut down.

This project surely ensure the profitability in term of power used and the major problem of power factor are neglected as the power factor is controller and the harmonics distortion of the system under the relative small value. Interruption of the supply might not be the main cause to consider either from the load itself, the circuit has what it is necessary to overcome the problem on the circuit since the problem is in range

of it capability of interchange. Therefore, the boost power factor correction is the most efficiency of SMPS type where the load is given at the nearly unity power factor with able to feed on the 300 W application.

5.2 Recommendations on the Future Design

Future recommendation on the design should be able to develop the PC based on frequency inverter for 3-phase AC motor, since at this point the development of 3-phase inverter are not been applied due to time and cost involve on this matter. The boost converter with PFC is integrated with the overall system to achieve the target and able to perform as the source for the 3-phase inverter to be supply the 3-phase AC motor. The testing and refund the limitation of the boost converter to be verified with the high power application with the lowest cost involve by using the NCP 1654 as the controller.

REFERENCES

[1] ACSE Journal, Volume (6), Issue (3), Oct. , 2006 "*Speed control of three phase induction motor using single phase supply along with active power factor correction*" by Pradeep M Patil and Sanjay L Kurkute.

[2] September 2009, "*Design of a microcontroller based converter for 3-phase brushless DC motor drives*" by Nor KharzianaMohdNayan.

[3] (London, England: E. & F.N. Span, 1895) "*Polyphase electric currents and alternate-current motors"*bySilvanus Phillips Thompson.

[4] May 2000, "Production Line Drives: Understanding the Control System" by Hristina Stefanova.

[5] November 2009, "Frequency controlled AC motor drive" by *www.ab.com/support/abdrives/documentation.*

[6] *IEEE Std. 100 Authoritative Dictionary of Standards Terms, 7th edition* ISBN 0-7381 -2601 -2

[7] "Quasi-active power factor correction with a variable inductive filter: theory, design and practice" and "Quasi-active Power Factor Correction: The Role of Variable Inductance" by Wolfle, W.H.; Hurley, W.G.

[8] "Comparison between passive and active PFC solutions for a 250-W ATX application." By ATX power solution.

[9] June, 2004. *"Application Note 42047 Power Factor Correction (PFC) Basics"* By Fairchild Semiconductor.

[10] Year 1997, "*Experimental studies on active and passive PFC circuits*" 571-578. doi 10.1109/INTLEC.1997.646051 By Sugawara, I., Suzuki, Y., Takeuchi, A., & Teshima, T.

[11] Year 2010. "Power Factor Correction (PFC) Application Notes" By Cooper Bussmann.

[12] Feb, 2011. "Power Factor correction handbook" HBD835D/2 By ON semiconductor.

[13] "Power Factor Controller for Compact and Robust, Continuous Conduction Mode Pre-Converters" NCP1654/D By On semiconductor.

APPENDIX A

NCP 1654 Data Sheet

NCP1654

Power Factor Controller for Compact and Robust, Continuous Conduction Mode Pre-Converters

The NCP1654 is a controller for Continuous Conduction Mode (CCM) Power Factor Correction step−up pre−converters. It controls the power switch conduction time (PWM) in a fixed frequency mode and in dependence on the instantaneous coil current.

Housed in a SO8 package, the circuit minimizes the number of external components and drastically simplifies the PFC implementation. It also integrates high safety protection features that make the NCP1654 a driver for robust and compact PFC stages like an effective input power runaway clamping circuitry.

Features

- IEC61000−3−2 Compliant
- Average Current Continuous Conduction Mode
- Fast Transient Response
- Very Few External Components
- Very Low Startup Currents (<75 μA)
- Very Low Shutdown Currents (< 400 μA)
- Low Operating Consumption
- ±1.5 A Totem Pole Gate Drive
- Accurate Fully Integrated 65/133/200 kHz Oscillator
- Latching PWM for cycle−by−cycle Duty−Cycle Control
- Internally Trimmed Internal Reference
- Undervoltage Lockout with Hysteresis
- Soft−Start for Smoothly Startup Operation
- Shutdown Function
- Pin to Pin Compatible with Industry Standard
- This is a Pb−Free Device

Safety Features

- Inrush Currents Detection
- Overvoltage Protection
- Undervoltage Detection for Open Loop Detection or Shutdown
- Brown−Out Detection
- Soft−Start
- Accurate Overcurrent Limitation
- Overpower Limitation

Typical Applications

- Flat TVs, PC Desktops
- AC Adapters
- White Goods, other Off−line SMPS

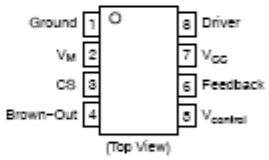
ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM

xx	= 65, 133 or 200
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
*	= Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP1654BD65R2G	SO−8 (Pb−Free)	2500 / Tape & Reel
NCP1654BD133R2G	SO−8 (Pb−Free)	2500 / Tape & Reel
NCP1654BD200R2G	SO−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MAXIMUM RATINGS TABLE

Symbol	Pin	Rating	Value	Unit
DRV	8	Output Drive Capability − Source Output Drive Capability − Sink	−1.5 +1.5	A
V_{CC}	7	Power Supply Voltage, V_{CC} pin, continuous voltage	−0.3, +20	V
	7	Transient Power Supply Voltage, duration < 10 ms, I_{VCC} < 10 mA	+25	V
Vin	2, 3, 4, 5, 6	Input Voltage	−0.3, +10	V
$P_D(SO)$ $R_{\theta JA}(SO)$		Power Dissipation and Thermal Characteristics D suffix, Plastic Package, Case 751 Maximum Power Dissipation @ T_A = 70°C Thermal Resistance Junction−to−Air	 450 178	 mW °C/W
T_J		Operating Junction Temperature Range	−40 to +125	°C
T_{Jmax}		Maximum Junction Temperature	150	°C
T_{Stmax}		Storage Temperature Range	−65 to +150	°C
T_{Lmax}		Lead Temperature (Soldering, 10 s)	300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) 2000 V per JEDEC standard JESD22, Method A114E
   Machine Model (MM) 200 V (except pin#7 which complies 150 V) per JEDEC standard JESD22, Method A115A.
2. This device contains Latch−up Protection and exceeds ±100 mA per JEDEC Standard JESD78.

TYPICAL ELECTRICAL CHARACTERISTICS TABLE (V_{CC} = 15 V, T_J from −40°C to +125°C, unless otherwise specified) (Note 3)

Symbol	Rating	Min	Typ	Max	Unit
GATE DRIVE SECTION					
R_{OH}	Source Resistance @ I_{source} = 100 mA	–	9.0	20	Ω
R_{OL}	Sink Resistance @ I_{sink} = −100 mA	–	6.6	18	Ω
T_r	Gate Drive Voltage Rise Time from 1.5 V to 13.5 V (C_L = 2.2 nF)	–	60	–	ns
T_f	Gate Drive Voltage Fall Time from 13.5 V to 1.5 V (C_L = 2.2 nF)	–	40	–	ns
REGULATION BLOCK					
V_{REF}	Voltage Reference	2.425	2.5	2.575	V
I_{EA}	Error Amplifier Current Capability	–	±28	–	μA
G_{EA}	Error Amplifier Gain	100	200	300	μS
I_{Bpin6}	Pin 6 Bias Current @ V_{FB} = V_{REF}	−500	–	500	nA
$V_{control}$	Pin5 Voltage				V
$V_{control(max)}$	Maximum Control Voltage @ V_{FB} = 2 V	–	3.6	–	
$V_{control(min)}$	Minimum Control Voltage @ V_{FB} = 3 V	–	0.6	–	
$\Delta V_{control}$	$\Delta V_{control}$ = $V_{control(max)}$ − $V_{control(min)}$	2.7	3.0	3.3	
V_{OUTL} / V_{REF}	Ratio (V_{OUT} Low Detect Threshold / V_{REF})	94	95	96	%
H_{OUTL} / V_{REF}	Ratio (V_{OUT} Low Detect Hysteresis / V_{REF})	–	0.5	–	%
I_{BOOST}	Pin 5 Source Current when (V_{OUT} Low Detect) is activated	190	228	260	μA
CURRENT SENSE BLOCK					
V_S	Current Sense Pin Offset Voltage, (I_{CS} = 100 μA)	–	10	–	mV
$I_{S(OCP)}$	Overcurrent Protection Threshold	185	200	215	μA
POWER LIMITATION BLOCK					
I_{CS} x V_{BO}	Overpower Limitation Threshold		200		μVA
$I_{CS(OPL1)}$	Overpower Current Threshold (V_{BO} = 0.9 V, V_M = 3 V)	186	222	308	μA
$I_{CS(OPL2)}$	Overpower Current Threshold (V_{BO} = 2.67 V, V_M = 3 V)	62	75	110	
PWM BLOCK					
Dcycle	Duty Cycle Range		0−97		%
OSCILLATOR / RAMP GENERATOR BLOCK					
fsw	Switching Frequency 65 kHz	58	65	72	kHz
	133 kHz	120	133	146	
	200 kHz	180	200	220	
BROWN−OUT DETECTION BLOCK					
V_{BOH}	Brown−Out Voltage Threshold (rising)	1.22	1.30	1.38	V
V_{BOL}	Brown−Out Voltage Threshold (falling)	0.65	0.7	0.75	V
I_{IB}	Pin 4 Input Bias Current @ V_{BO} = 1 V	−500	–	500	nA
CURRENT MODULATION BLOCK					
I_{M1}	Multiplier Output Current ($V_{control}$ = $V_{control(max)}$, V_{BO} = 0.9 V, I_{CS} = 25 μA)	–	1.9	–	μA
I_{M2}	Multiplier Output Current ($V_{control}$ = $V_{control(max)}$, V_{BO} = 0.9 V, I_{CS} = 75 μA, 65 kHz)	2.1	5.6	8.1	
	(133 kHz, 200 kHz @ 0 ~ 125°C)	2.1	5.6	8.1	
	(133 kHz, 200 kHz @ −40 ~ 125°C)	1.5	5.6	8.5	
I_{M3}	Multiplier Output Current ($V_{control}$ = $V_{control(min)}$ + 0.2 V, V_{BO} = 0.9 V, I_{CS} = 25 μA	–	28.1	–	
I_{M4}	Multiplier Output Current ($V_{control}$ = $V_{control(min)}$ + 0.2 V, V_{BO} = 0.9 V, I_{CS} = 75 μA	–	84.4	–	

3. The above specification gives the targeted values of the parameters. The final specification will be available once the complete circuit characterization has been performed.

TYPICAL ELECTRICAL CHARACTERISTICS TABLE (V_{CC} = 15 V, T_J from −40°C to +125°C, unless otherwise specified) (Note 3)

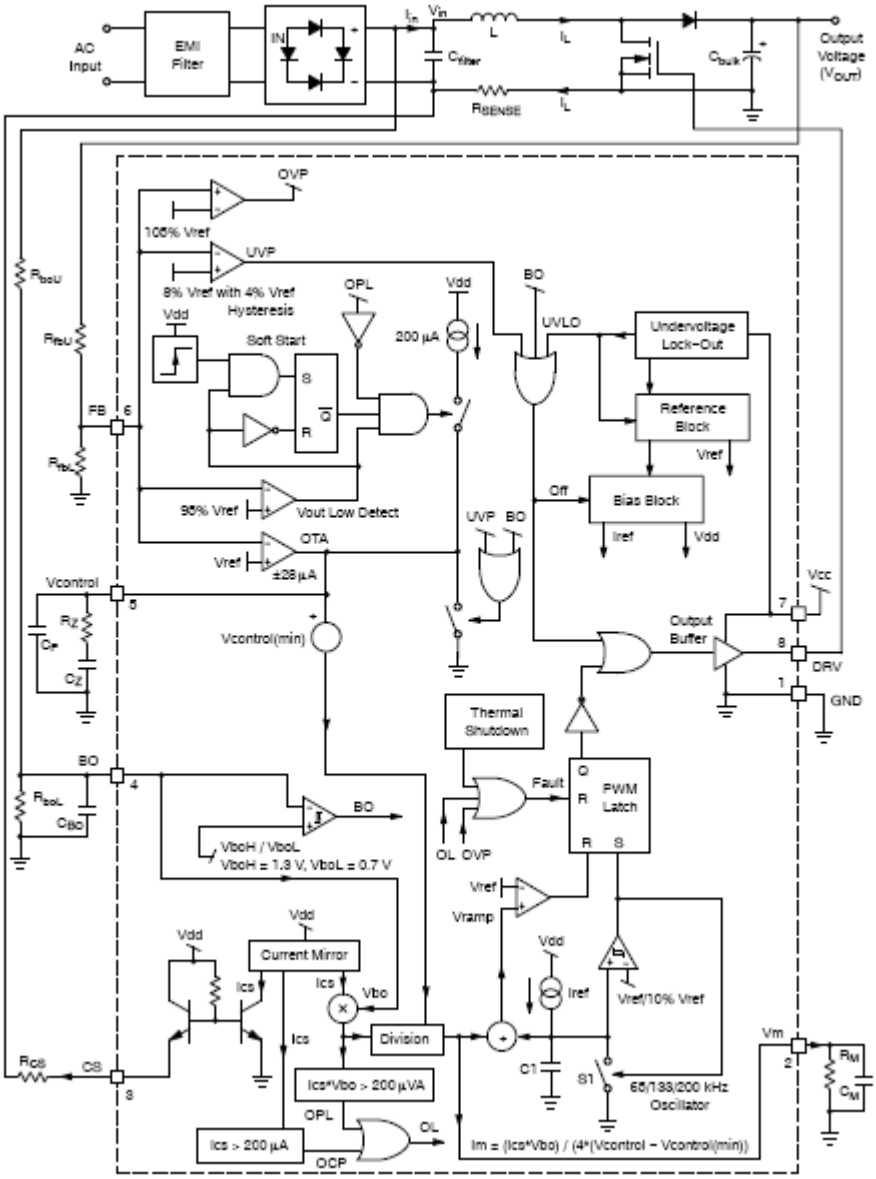
Symbol	Rating	Min	Typ	Max	Unit
OVERVOLTAGE PROTECTION					
V_{OVP} / V_{REF}	Ratio (Overvoltage Threshold / V_{REF})	103	105	107	%
T_{OVP}	Propagation Delay (V_{FB} − 107% V_{REF}) to Drive Low	−	500	−	ns
UNDERVOLTAGE PROTECTION / SHUTDOWN					
$V_{UVP(on)}/V_{REF}$	UVP Activate Threshold Ratio (T_J = 0°C to +105°C)	4	8	12	%
$V_{UVP(off)}/V_{REF}$	UVP Deactivate Threshold Ratio (T_J = 0°C to +105°C)	6	12	18	%
$V_{UVP(H)}$	UVP Lockout Hysteresis	−	4	−	%
T_{UVP}	Propagation Delay (V_{FB} < 8% V_{REF}) to Drive Low	−	500	−	ns
THERMAL SHUTDOWN					
T_{SD}	Thermal Shutdown Threshold	150	−	−	°C
H_{SD}	Thermal Shutdown Hysteresis	−	30	−	°C
V_{CC} UNDERVOLTAGE LOCKOUT SECTION					
$V_{CC(on)}$	Start−Up Threshold (Undervoltage Lockout Threshold, V_{CC} rising)	9.6	10.5	11.4	V
$V_{CC(off)}$	Disable Voltage after Turn−On (Undervoltage Lockout Threshold, V_{CC} falling)	8.25	9.0	9.75	V
$V_{CC(H)}$	Undervoltage Lockout Hysteresis	1.0	1.5	−	V
DEVICE CONSUMPTION					
	Power Supply Current:				
I_{STUP}	Start−Up (@ V_{CC} = 9.4 V)	−	−	75	μA
I_{CC1}	Operating (@ V_{CC} = 15 V, no load, no switching)	−	3.7	5.0	mA
I_{CC2}	Operating (@ V_{CC} = 15 V, no load, switching)	−	4.7	6.0	mA
I_{STDN}	Shutdown Mode (@ V_{CC} = 15 V and V_{FB} = 0 V)	−	300	400	μA

3. The above specification gives the targeted values of the parameters. The final specification will be available once the complete circuit characterization has been performed.

NOTE: $I_M = \dfrac{I_{cs} \times V_{BO}}{4 \times \left(V_{control} - V_{control(min)}\right)}$

DETAILED PIN DESCRIPTIONS

Pin	Symbol	Name	Function
1	GND	Ground	–
2	V_{in}	Multiplier Voltage	This pin provides a voltage V_M for the PFC duty cycle modulation. The input impedance of the PFC circuits is proportional to the resistor R_M externally connected to this pin. The device operates in average current mode if an external capacitor C_M is connected to the pin. Otherwise, it operates in peak current mode.
3	CS	Current Sense Input	This pin sources a current I_{CS} which is proportional to the inductor current I_L. The sense current I_{CS} is for overcurrent protection (OCP), overpower limitation (OPL) and PFC duty cycle modulation. When I_{CS} goes above 200 μA, OCP is activated and the Drive Output is disabled.
4	V_{BO}	Brown−Out / In	Connect a resistor network among the rectified input voltage, BO pin, and ground. And connect a capacitor between BO pin and ground. BO pin detects a voltage signal proportional to the average input voltage. When V_{BO} goes below V_{BOL}, the circuit that detects too low input voltage conditions (brown−out), turns off the output driver and keeps it in low state until V_{BO} exceeds V_{BOH}. This signal which is proportional to the RMS input voltage V_{ac} is also for overpower limitation (OPL) and PFC duty cycle modulation.
5	$V_{control}$	Control Voltage / Soft−Start	The voltage of this pin $V_{control}$ directly controls the input impedance. This pin is connected to external type−2 compensation components to limit the $V_{control}$ bandwidth typically below 20 Hz to achieve near unity power factor. The device provides no output when $V_{control} < V_{control(min)}$. When it starts operation, the power increases slowly (soft−start).
6	V_{FB}	Feed−Back / Shutdown	This pin receives a feedback signal V_{FB} that is proportional to the PFC circuits output voltage. This information is used for both the output regulation, the overvoltage protection (OVP), and output undervoltage protection (UVP) to protect the system from damage at feedback abnormal situation. When V_{FB} goes above 105% V_{FBR} OVP is activated and the Drive Output is disabled. When V_{FB} goes below 8% V_{FBR} the device enters a low−consumption shutdown mode.
7	V_{CC}	Supply Voltage	This pin is the positive supply of the IC. The circuit typically starts to operate when V_{CC} exceeds 10.5 V and turns off when V_{CC} goes below 9 V. After start−up, the operating range is 9 V up to 20 V.
8	DRV	Drive Output	The high current capability of the totem pole gate drive (±1.5 A) makes it suitable to effectively drive high gate charge power MOSFET.


AC Input
EMI Filter
IN
Output Voltage (V_{OUT})
C_{filter}
R_{SENSE}
C_{bulk}
OVP
105% Vref
UVP
8% Vref with 4% Vref Hysteresis
OPL
Vdd
200 µA
BO
UVLO
Undervoltage Lock-Out
Soft Start
Reference Block
Vref
FB
6
Off
Bias Block
Iref
95% Vref
Vout Low Detect
OTA
±28 µA
Vcontrol
5
Vcontrol(min)
Vcc
7
Output Buffer
8
DRV
1
GND
Thermal Shutdown
Fault
PWM Latch
OL
OVP
BO
4
VboH / VboL
VboH = 1.3 V, VboL = 0.7 V
Vramp
Current Mirror
Ics
Vbo
Division
Vref/10% Vref
Vm
2
R_M
C_M
R_{CS}
CS
3
Ics*Vbo > 200 µVA
C1
S1
65/133/200 kHz Oscillator
Ics > 200 µA
OCP
Im = (Ics*Vbo) / (4*(Vcontrol − Vcontrol(min))

APPENDIX B

Power Inductor GA1399-AL Sheet

NEW!

Power Inductor – GA3199-AL

For ON Semiconductor NCP1654 PFC Controller

- Designed for ON Semiconductor for their 300 Watt, wide mains, PFC stage, driven by the NCP1654 PFC Controller
- Shown as L1 on Application Note AND8324/D
- High inductance: 650 µH; high saturating current: 6.3 A

Core material Ferrite

Terminations RoHS compliant tin-silver over tin over nickel over phos bronze. Other terminations available at additional cost.

Weight 94 g

Ambient temperature –40°C to +85°C with Irms current, +85°C to +125°C with derated current

Storage temperature Component: –40°C to +85°C. Packaging: –40°C to +80°C

Moisture Sensitivity Level (MSL) 1 (unlimited floor life at <30°C / 85% relative humidity)

Mean Time Between Failures (MTBF) 26,315,789 hours

Packaging 20 per tray

PCB washing Only pure water or alcohol recommended

Part number	Inductance[1] ±10% (µH)	DCR max (Ohm)	SRF typ[2] (kHz)	Isat (A)[3] 10% drop	20% drop	30% drop	Irms (A)[4] 20°C rise	40°C rise
GA3199-AL	650	0.165	770	5.9	6.1	6.3	2.9	3.9

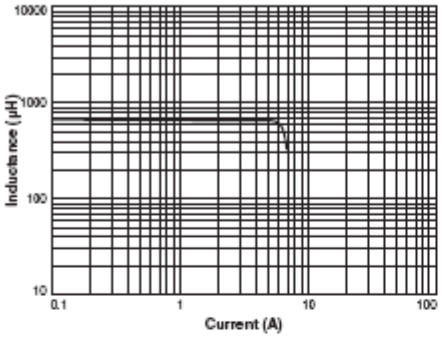
1. Inductance measured at 10 kHz, 0.1 Vrms, 0 Adc.
2. SRF measured on an Agilent/ HP 4192A impedance analyzer or equivalent
3. DC current at which the inductance drops the specified amount from its value without current.
4. Current that causes the specified temperature rise from 25°C ambient.
5. Electrical specifications at 25°C.

Refer to Doc 362 "Soldering Surface Mount Components" before soldering.

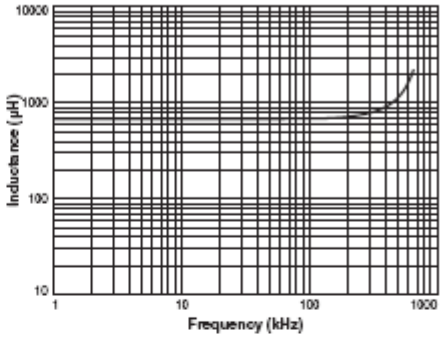
NEW!

Power Inductor – GA3199-AL

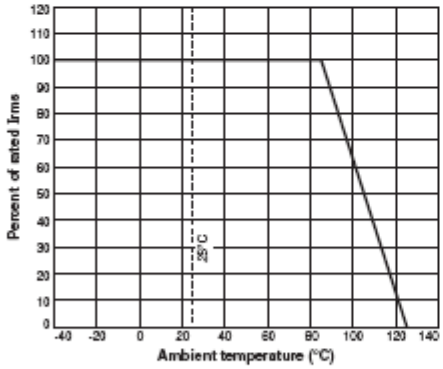
Inductance vs Current

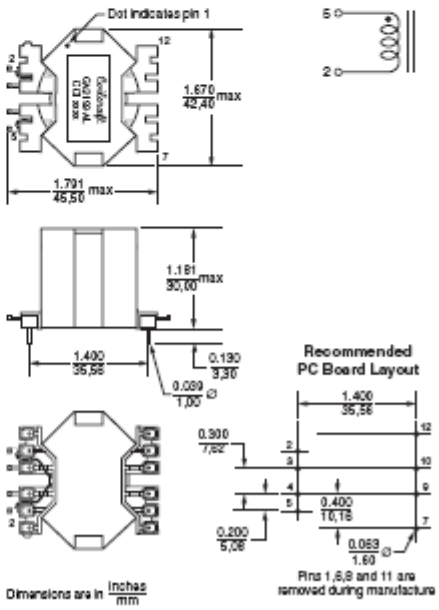


Inductance vs Frequency



Irms Derating





APPENDIX C

Power Transistor SPP20N60S5 Data Sheet

Cool MOS™ Power Transistor

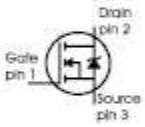
V_{DS} @ T_{jmax}	650	V
$R_{DS(on)}$	0.19	Ω
I_D	20.7	A

Feature

- New revolutionary high voltage technology
- Worldwide best $R_{DS(on)}$ in TO 220
- Ultra low gate charge
- Periodic avalanche rated
- Extreme dv/dt rated
- High peak current capability
- Improved transconductance
- PG-TO-220-3-31: Fully isolated package (2500 VAC; 1 minute)
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[3] for target applications

PG-TO220-3-31 PG-TO262-3 PG-TO220

Type	Package	Ordering Code	Marking
SPP20N60C3	PG-TO220	Q67040-S4398	20N60C3
SPI20N60C3	PG-TO262-3	Q67040-S4550	20N60C3
SPA20N60C3	PG-TO220-3-31	SP000216354	20N60C3



Maximum Ratings

Parameter	Symbol	Value		Unit
		SPP_I	SPA	
Continuous drain current	I_D			A
T_C = 25 °C		20.7	20.7 1)	
T_C = 100 °C		13.1	13.1 1)	
Pulsed drain current, t_p limited by T_{jmax}	$I_{D\,puls}$	62.1	62.1	A
Avalanche energy, single pulse	E_{AS}	690	690	mJ
I_D=10A, V_{DD}=50V				
Avalanche energy, repetitive t_{AR} limited by T_{jmax} 2)	E_{AR}	1	1	
I_D=20A, V_{DD}=50V				
Avalanche current, repetitive t_{AR} limited by T_{jmax}	I_{AR}	20	20	A
Gate source voltage static	V_{GS}	±20	±20	V
Gate source voltage AC (f >1Hz)	V_{GS}	±30	±30	
Power dissipation, T_C = 25°C	P_{tot}	208	34.5	W
Operating and storage temperature	T_j, T_{stg}	-55...+150		°C
Reverse diode dv/dt 7)	dv/dt	15		V/ns

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain Source voltage slope V_{DS} = 480 V, I_D = 20.7 A, T_j = 125 °C	dv/dt	50	V/ns

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	-	-	0.6	K/W
Thermal resistance, junction - case, FullPAK	R_{thJC_FP}	-	-	3.6	
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	62	
Thermal resistance, junction - ambient, FullPAK	R_{thJA_FP}	-	-	80	
SMD version, device on PCB: @ min. footprint @ 6 cm² cooling area [3]	R_{thJA}	 - -	 - 35	 62 -	
Soldering temperature, wavesoldering 1.6 mm (0.063 in.) from case for 10s [4]	T_{sold}	-	-	260	°C

Electrical Characteristics, at T_j=25°C unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=0.25mA	600	-	-	V
Drain-Source avalanche breakdown voltage	$V_{(BR)DS}$	V_{GS}=0V, I_D=20A	-	700	-	
Gate threshold voltage	$V_{GS(th)}$	I_D=1000µA, V_{GS}=V_{DS}	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	V_{DS}=600V, V_{GS}=0V, T_j=25°C T_j=150°C	 - -	 0.1 -	 1 100	µA
Gate-source leakage current	I_{GSS}	V_{GS}=30V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=13.1A T_j=25°C T_j=150°C	 - -	 0.16 0.43	 0.19 -	Ω
Gate input resistance	R_G	f=1MHz, open drain	-	0.54	-	

Electrical Characteristics

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Transconductance	g_{fs}	$V_{DS}\geq 2^*I_D^*R_{DS(on)max}$, I_D=13.1A	-	17.5	-	S
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	2400	-	pF
Output capacitance	C_{oss}		-	780	-	
Reverse transfer capacitance	C_{rss}		-	50	-	
Effective output capacitance,[5] energy related	$C_{o(er)}$	V_{GS}=0V, V_{DS}=0V to 480V	-	83	-	
Effective output capacitance,[6] time related	$C_{o(tr)}$		-	160	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=380V, V_{GS}=0/13V, I_D=20.7A, R_G=3.6Ω, T_j=125	-	10	-	ns
Rise time	t_r	V_{DD}=380V, V_{GS}=0/13V, I_D=20.7A, R_G=3.6Ω	-	5	-	
Turn-off delay time	$t_{d(off)}$		-	67	100	
Fall time	t_f		-	4.5	12	

Gate Charge Characteristics

Gate to source charge	Q_{gs}	V_{DD}=480V, I_D=20.7A	-	11	-	nC
Gate to drain charge	Q_{gd}		-	33	-	
Gate charge total	Q_g	V_{DD}=480V, I_D=20.7A, V_{GS}=0 to 10V	-	87	114	
Gate plateau voltage	$V_{(plateau)}$	V_{DD}=480V, I_D=20.7A	-	5.5	-	V

[6] J-STD20 and JESD22

[1] Limited only by maximum temperature

[2] Repetitive avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR}*f$.

[3] Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical without blown air.

[4] Soldering temperature for TO-263: 220°C, reflow

[5] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

[6] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

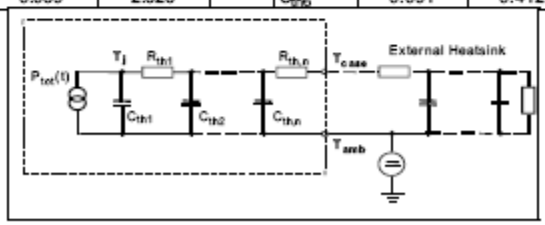
[7] $I_{SD}<=I_D$, di/dt<=400A/us, V_{DClink}=400V, $V_{peak}<V_{BR,DSS}$, $T_j<T_{j,max}$.
Identical low-side and high-side switch.

Electrical Characteristics

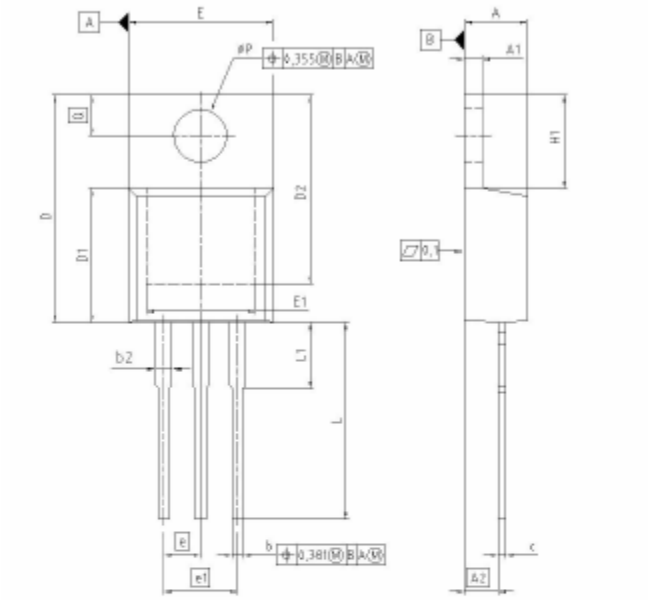
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Inverse diode continuous forward current	I_S	T_C=25°C	-	-	20.7	A
Inverse diode direct current, pulsed	I_{SM}		-	-	62.1	
Inverse diode forward voltage	V_{SD}	V_{GS}=0V, I_F=I_S	-	1	1.2	V
Reverse recovery time	t_{rr}	V_R=480V, I_F=I_S, di_F/dt=100A/µs	-	500	800	ns
Reverse recovery charge	Q_{rr}		-	11	-	µC
Peak reverse recovery current	I_{rrm}		-	70	-	A
Peak rate of fall of reverse recovery current	di_n/dt	T_j=25°C	-	1400	-	A/µs

Typical Transient Thermal Characteristics

Symbol	Value		Unit	Symbol	Value		Unit
	SPP_I	SPA			SPP_I	SPA	
R_{th1}	0.00769	0.00769	K/W	C_{th1}	0.0003763	0.0003763	Ws/K
R_{th2}	0.015	0.015		C_{th2}	0.001411	0.001411	
R_{th3}	0.029	0.029		C_{th3}	0.001931	0.001931	
R_{th4}	0.114	0.163		C_{th4}	0.005297	0.005297	
R_{th5}	0.136	0.323		C_{th5}	0.012	0.008453	
R_{th6}	0.059	2.526		C_{th6}	0.091	0.412	



PG-TO220-3-1, PG-TO220-3-21 : Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.300	4.572	0.169	0.180
A1	1.170	1.400	0.046	0.055
A2	2.215	2.719	0.087	0.107
b	0.650	0.864	0.026	0.034
b2	0.635	1.778	0.025	0.070
c	0.330	0.580	0.013	0.024
D	14.808	15.950	0.583	0.628
D1	8.509	9.450	0.335	0.372
D2	12.050	13.100	0.506	0.516
E	9.700	10.365	0.382	0.408
E1	6.500	8.500	0.256	0.339
e	2.540		0.100	
e1	5.080		0.200	
N	3		3	
H1	5.900	6.900	0.232	0.272
L	13.000	14.000	0.512	0.551
L1	-	4.500	-	0.159
øP	3.700	3.950	0.146	0.153
Q	2.600	3.000	0.102	0.118

REFERENCE
JEDEC TO220

SCALE
0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
01-06-2005

FILE
TO220_5

APPENDIX D

GBU8A-GBU8M Bridge Rectifier Sheet

FAIRCHILD
SEMICONDUCTOR®

GBU8A - GBU8M

Bridge Rectifiers

Features

- Glass passivated junction
- Surge overload rating: 200 amperes peak
- Reliable low cost construction utilizing molded plastic technique.
- Ideal for printed circuit board.

GBU

Absolute Maximum Ratings * T_A = 25°C unless otherwise noted

Symbol	Parameter	Value							Units
		8A	8B	8D	8G	8J	8K	8M	
V_{RRM}	Maximum Repetitive Reverse Voltage	50	100	200	400	600	800	1000	V
V_{RMS}	Maximum RMS Bridge Input Voltage	35	70	140	280	420	560	700	V
V_R	DC Reverse Voltage (Rated V_R)	50	100	200	400	600	800	1000	V
$I_{F(AV)}$	Average Rectified Forward Current, @ T_A = 100°C @ T_A = 45° C	8.0 6.0							A A
I_{FSM}	Non-Repetitive Peak Forward Surge Current 8.3ms Single Half-Sine-Wave	200							A
T_{STG}	Storage Temperature Range	-55 to +150							°C
T_J	Operating Junction Temperature	-55 to +150							°C

* These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

Thermal Characteristics

Symbol	Parameter	Value	Units
P_D	Power Dissipation	18	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, * per leg	15	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case, * per leg	3	°C/W

* Device mounted on PCB with 0.5 " (13 " 13mm).

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_F	Forward Voltage, per element @ 8.0A	1.0	V
I_R	Reverse Current, per element @ Rated V_R T_A = 25°C T_A = 100°C	 50 500	 µA µA
	I^2t Rating for Fusing t < 8.35ms	166	A^2s

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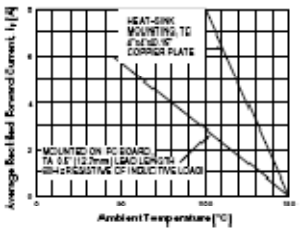
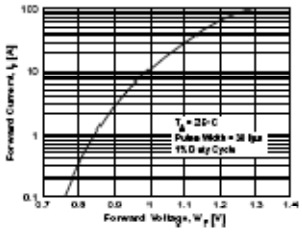
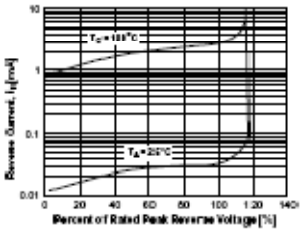
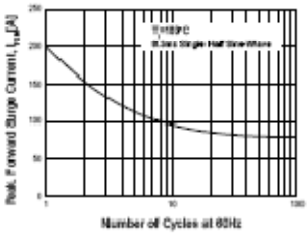
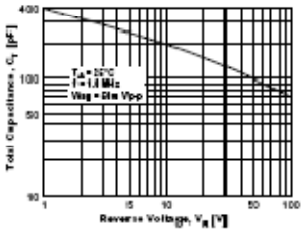
Typical Performance Characteristics











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EnSigna™	i-Lo™	OCX™	RapidConfigure™	TruTranslation™
FACT™	ImpliedDisconnect™	OCXPro™	RapidConnect™	UHC™
FACT Quiet Series™		OPTOLOGIC®	µSerDes™	UltraFET®
Across the board. Around the world.™		OPTOPLANAR™	SILENT SWITCHER®	UniFET™
The Power Franchise®		PACMAN™	SMART START™	VCX™
Programmable Active Droop™		POP™	SPM™	

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I14

APPENDIX E

EIC 61000-3-2 compliant sheet

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IEC 61000-3-2 Harmonics Standards Overview

By Muhamad Nazarudin Zainal Abidin, Schaffner EMC Inc., Edison, NJ, USA

Introduction

There have been recent changes to the European Union's Directive to assess compliance of a product's AC mains current harmonics. The purpose of this document is to provide an executive overview of pertinent details and make them easier to understand. For more detailed information please refer to the relevant standards available from the organization concerned.

Harmonics standard IEC 61000-3-2 Ed. 3 2005

This standard assesses and sets the limit for equipment that draws input current ≤16A per phase. Equipment that draws current >16A and ≤75A per phase is covered by IEC/TS 61000-3-12. Harmonics measurement and evaluation methods for both standards are governed by IEC 61000-4-7.

Classification of equipment

Equipment can be grouped into one of 4 classes based on the following criteria as evaluated by the IEC committee members:

- Number of pieces of equipment in use (how many (volume) are being used by consumers)
- Duration of use (number of hours in operation)
- Simultaneity of use (are the same type of equipment used on the same time frame)
- Power consumption
- Harmonics spectrum, including phase (how clean or distorted is the current drawn by the equipment)

After all the above criteria are taken into consideration equipment are classified as follows:

Class A	▪ Balanced three-phase equipment ▪ Household appliances, excluding equipment identified by Class D ▪ Tools, excluding portable tools ▪ Dimmers for incandescent lamps ▪ Audio equipment ▪ Everything else that is not classified as B, C or D
Class B	▪ Portable tools ▪ Arc welding equipment which is not professional equipment
Class C	▪ Lighting equipment
Class D	▪ Personal computers and personal computer monitors ▪ Television receivers Note: Equipment must have power level 75W up to and not exceeding 600W

Table 1: Equipment classification

Measurement methods and evaluation

Measurement methods have also gone through a process of evolution. Measuring equipment that has constant power consumption is relatively easier as the harmonics current spectrum remains relatively unchanged in amplitude and phase throughout the test duration. However, if the power level varies over the test duration, the measurement becomes more complicated and complex. Examples of such products are washing machines, photocopiers, printers, air conditioners and variable speed vacuum cleaners. The two measurement methods used to be separate tests but were combined when amendment 14 to IEC 61000-3-2 1995 was introduced in the year 2000.

As mentioned earlier, the whole construction of the analyzer used for testing is governed by IEC 61000-4-7. This standard goes into great detail on how one should measure harmonics emissions for compliance testing. There are two versions of this standard published with amendments that employ two different data acquisition techniques. The older version published in 1991 requires data acquisition in blocks of 320ms data and the later version published in 2001 uses 200ms, both with no gap or overlap between the acquired data blocks. The other variation between the two versions is the introduction of grouped inter-harmonics (harmonics that are not the integer multiple of the fundamental frequency) which are then added to the nearest integer harmonic. All measurements now in use must employ the 1.5s first order filter before the averaging calculation is processed, for each block of data, regardless of product power consumption behavior.

Another important clarification in the Nov 2005 version is that the current harmonics measurement must be done on the line conductor and not the neutral conductor. However, for single phase applications this can be done on the neutral conductor but not in three-phase applications where the values can differ significantly if the EUT is not balanced.

Harmonics [n]	Class A [A]	Class B [A]	Class C [% of fund]	Class D [mA/W]
		Odd harmonics		
3	2.30	3.45	30 x λ	3.4
5	1.14	1.71	10	1.9
7	0.77	1.155	7	1.0
9	0.40	0.60	5	0.5
11	0.33	0.495	3	0.35
13	0.21	0.315	3	3.85/13
15 ≤n ≤39	0.15 x 15/n	0.225 X 15/n	3	3.85/n
		Even harmonics		
2	1.08	1.62	2	-
4	0.43	0.645	-	-
6	0.30	0.45	-	-
8 ≤n ≤40	0.23 x 8/n	0.345 x 8/n	-	-

Table 2: Harmonics limit

Relaxation against applicable limits

There is an existing relaxation as per A14 in 2000 for higher order harmonics that only applies to a range of high odd harmonics current from the 21st harmonic (1050Hz) to the 39th (1950Hz). This allows the high order harmonic currents to exceed the limits per table 2 (100% of limit) but not exceeding 150% (individual limit x 1.5) as long the Partial Odd Harmonic Current (POHC) average does not exceed the POHC limit.

Example 1:
In a Class A test, harmonics orders 37 and 39 exceeded their respective 100% limit and is <150% of the limit. POHC can then be applied by taking the measured values of H21 to H39 and applying them in the formula below. Do the same calculation for the applicable limits of H21 to H39 per Class A limit and compare the values.

Even though the test report should indicate H37 and H39 as failed (>100% of limit) the overall result for the EUT would be a Pass should measured values be less than the limit calculated.

$$\text{partial odd harmonic current} = \sqrt{\sum_{n=21,23}^{39} I_n^2}$$

Quote from IEC 61000-3-2 ed.2.1 2001

> For the 21st and higher odd order harmonics, the average values obtained for each individual odd harmonic over the full observation period, calculated from the 1.5s smoothed r.m.s. values according to 6.2.2 may exceed the applicable limits by 50% provided that the following conditions are met:
>
> - the measured partial odd harmonic current does not exceed the partial odd harmonic current which can be calculate from the applicable limits;
> - all 1.5s smoothed r.m.s. individual harmonic current values shall be less than or equal to 150% of the applicable limits.

In this latest version of the harmonics standard, there is a further relaxation for Class A equipment that a manufacturer could employ (please refer to the above excerpt from the standard.). This relaxation would help a Class A product that has short bursts (<10% of test time) that would go beyond the transitory or 150% limit but are less than 200% of the applicable limit. This is allowed as long as the average of the harmonic current is <90% of its limit.

Example 2:
If a 5th order harmonic (250Hz) for a Class A product exceeds 1.71A (1.14A limit x 1.5) but is still below 2.28A (1.14A limit x 2) and this happens for less than 1min of a 10min test duration then the following applies:
The 5th harmonic is considered to have failed the test (it exceeded the 100% limit) but the overall result for that Class A EUT is a pass when the new relaxation is applied.

> However, if the same EUT also has high order odd harmonic currents H21-39, per example 1, which exceeded the 100% limit, then one cannot apply both relaxations at the same time as they are mutually exclusive. You can only apply one relaxation for a given test.

Quote from IEC 61000-3-2 Nov 2005

6.2.3.3 Application of limits

The average values for the individual harmonic currents, taken over the entire test observation period shall be less than or equal to the applicable limits.

For each harmonic order, all 1.5s smoothed r.m.s. harmonic current values, as defined in 6.2.2 shall be either:

a) less than or equal to 150% of the applicable limits, or

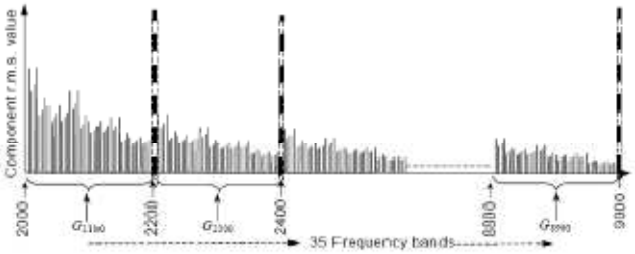
b) less than or equal to 200% of the applicable limits under the following conditions, which apply all together:

1) the EUT belongs to Class A for harmonics;

2) the excursion beyond 150% of the applicable limits lasts less than 10% of the test observation period or in total 10min (within the test observation period), whichever is smaller, and

3) the average value of the harmonic current, taken over the entire test observation period, is less than 90% of the applicable limits.

The other little known requirement is that the 1% power accuracy as per IEC 61000-4-7 2000, section 5.3 table 1 is now a requirement for all power analyzers testing to IEC 61000-3-2. Measurement of inter-harmonics up to 2kHz (harmonics that have no relation to the 50Hz fundamental frequency) should also be considered as part of the testing requirement. In the not too distant future, measurement of harmonics and inter-harmonics from 2kHz to 9kHz with the aid of a device called AMN (Artificial Mains Network) would be implemented in bands or group of 200Hz as shown below.



Summary

The impact of all the changes discussed above indicate that both hardware and software modifications for existing test systems will be required. Therefore it is advantageous to consider measurement systems with an easy upgrade path that will accommodate current standards changes as well as future changes. While dedicated harmonics analyzers require both firmware and software modifications, PC-based analyzers required only software updates, making them a better choice.

	IEC 61000-3-2:1995 Edition 1.0	IEC 61000-3-2:2001 Edition 2.1	IEC 61000-3-2:2005 Edition 3.0
Class D definition	Special waveform envelope (75W to 600W)	TV, PC and PC monitor (75 to 600W)	TV, PC and PC monitor (75 to 600W)
Measurement methods	Steady and transitory	Transitory only	Transitory only
Measurement window	16 cycles (320/267ms @ 50/60Hz)	200ms (10/12 cycles @ 50/60Hz) (16 cycles permitted through 2004) See IEC 61000-4-7 Ed. 2	200ms (10/12 cycles @ 50/60Hz)
Data manipulation	Transitory only	All data must be smoothed using the 1.5s first order filter	All data must be smoothed using the 1.5s first order filter
Pass/Fail for individual harmonics	Every window result <150% of limit 10% of test time >100% permitted	Every window result <150% of limit 10% of test time >100% permitted	Every window result <150% of limit 10% of test time >100% permitted
Class A relaxation*	No special provision	No special provision	<200% of limit only IF >150% for 10% of test time AND Average <90% of limit
Odd harmonics 21-39*	No special provision	Provision for POHC calculation permitting the average of some individual harmonics to >100% (<150%)	Provision for POHC calculation permitting the average of some individual harmonics to >100% (<150%)
Class C & D limits	Proportional to measured power (Class D) Or Current & PF (Class C)	Allows the manufacturer to specify test power or current level, provided it is within ±10% of measured value	Allows the manufacturer to specify test power or current level, provided it is within ±10% of measured value
Test/observation period	Not specifically defined but to find the max. harmonics emission	Specified to be significantly long enough to acquire ±5% repeatability. If too long, select the 2.5min with max. harmonics	Specified to be significantly long enough to acquire ±5% repeatability. If too long, select the 2.5min with max. harmonics
Test conditions	Specified for some products	Detailed test procedure for certain product categories	Detailed test procedure for certain product categories. Amended procedure for testing TV and vacuum cleaners from 2001 version

Table 3: Important differences from various versions of IEC 61000-3-2

* Note: Use either one of the exemption and they cannot be applied together