Optimization of Nanowire Resistance Load Logic Inverter

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ABSTRACT
This study is the first to demonstrate characteristics optimization of nanowire resistance load inverter. Noise margins and inflection voltage of transfer characteristics are used as limiting factors in this optimization. Results indicate that optimization depends on resistance value. Increasing of load resistor tends to increasing in noise margins until saturation point, increasing load resistor after this point will not improve noise margins significantly.

KEYWORDS: Nanowire, Transistor, Noise Margins, Inverter