Experimental Study of SBPWM for Z-Source Inverter Five Phase

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Abstract

On the basis of a conventional Z-source inverter, this paper presents an extension of the existing study about a driving scheme implementation of a simple boost pulse width modulation under open loop system for five phase two level system. The impact of design parameter (fixed modulation index and switching frequency) versus performance parameter (capacitor voltage, inductor current, total harmonic distortion and DC link voltage) are studied and analysed. To validate the advantages of Z-source five-phase inverter, the driving scheme are simulated using Matlab/Simulink and verified with real-time target board eZdsp TMS320F28335. From the study, it was found that under specified modulation index and switching frequency, the THD of an output current fulfilled the EN61000-3-2 standard.

Keywords: Five-phase inverter, Modulation index, Pulse width modulation, Total harmonic distortion, Z-source inverter

1. INTRODUCTION

Over the past forty years, there has been a dramatic increase in the use of five-phase voltage source inverter (VSI) fed motor drive [1], a well-known system that can be fabricated using low-cost, high-performance insulated gate bipolar transistor (IGBT) modules or intelligent power modules [2]. Recent developments in VSI fed motor drive have heightened the need for analyzing the topology, driving scheme, control technique and application. One type of VSI fed motor drive is the Z-source inverter (ZSI), as proposed by F.Z. Peng [3]. Other researcher found [4] that ZSI has progressed actively with the electric vehicle whereby the drive voltage is stress in huge and its investigation has also become a continuing concern within the scope of multiphase systems. There is a large volume of published studies describing the roles of ZSI in multiphase systems [5]-[7]; however, this paper focuses only on the five phase inverter since it commonly used and the smallest number of phases in a multiphase systems [8].

ZSI has the capability to resolve mutual problems either in VSI fed or in current source inverter (CSI) fed motor drive, which are [3]:

a) Issues in bucking and boosting mode operation. The output produced by a H-bridge inverter is restricted either to greater than or smaller than the input voltage. By controlling the modulation index \( M_i \) of the driving scheme, there is a range of \( M_i \) that can be used for bucking and boosting purposes.

b) The input circuit to the H-bridge inverter is fixed. During bucking mode, a specific buck converter circuit must be added, while during boosting mode, a boost converter circuit must be provided. With ZSI, bucking and boosting modes can be provided using with similar topology and single stage conversion.
c) The effect of electromagnetic interference (EMI) in conventional inverter system contributes to the level of harmonic content. By avoiding a dead time application in ZSI for each of the upper and lower leg would minimise the harmonic content in the system.

Given ZSI’s many benefits, this paper presents an investigation as follows. Section 2 describes the motivation and research goal using ZSI fivephase that employs a simple boost pulse width modulation (SBPWM). Detailed explanation of the SBPWM process is presented in Section 3. Simulation and experimental results are illustrated in Section 4 to show that the harmonic content based on the EN61000-3-2 standard for class D order is complied. In Sections 5, 6 and 7, the details experimental test platform is clarified under open loop system with selected component conditions. Conclusions are given in Section 8.

2. MOTIVATION & RESEARCH GOAL

Pulse width modulation (PWM) has become a vital and significant element of a multiphase system [9]. A preliminary work conducted using PWM for four-phase ZSI was undertaken by [2]. In the study, PWM for single, three and four phases under continuous and discontinuous mode were analysed using simulation platform. The hardware verification was done under three-phase system.

In 2013, A. Kouzou [5] reported the use of PWM in multiphase systems, in which case amaximum boost control (MBC) strategy for multiphase system from 3, 5, 7, 11, 13, 15, 17, 19 and 21 phases under simulation task were employed. In the experimental setup, the researchers fed two parallel loads, a five-phase resistive load and a five-phase induction machine to verify the simulation result. They found that the system could accomplish any desired output multiphase AC voltage whose magnitude is greater than the input DC voltage [5]. The performance parameters of the system was also improved, which include the decrease in the Z-source capacitor voltage and Z-source inductor current ripple [5].

The findings above became the motivations for this research to investigate other PWM driving schemes, such as SBPWM with DSP based for ZSI fivephase. SBPWM is a well-known driving scheme in ZSI, as it mathematically uncomplicated [10], easy to implement [10], and has been tested using many new topologies of ZSI [11]–[15].

3. BACKGROUND ZSI FIVE-PHASE TOPOLOGY AND ITS OPERATION

The topology of ZSI fivephaseused in this research is shown in Figure 1. The load is connected in a star formation and the load on each phase consists of a parallel connection of a resistance, a capacitance and an inductance. The front end of the topology consists of a DC input voltage that is assumed to be a ripple-free constant DC voltage source, an ultrafast diode used to prevent circulation of the reverse current towards the DC power supply, a Z-source network acting as a second order filter (consisting of two identical capacitors and inductors) and an H-bridge inverter (consisting of ten IGBTs).

A derivation of ZSI fivephaseis similar to that of a conventional five phase VSI but, referring to Figure 1, with the addition of a Z-source network as an input to the five phase H-bridge inverter makes the analysis different from that of the conventional five phase VSI. The Z-source network voltage of the ZSI five phase must satisfy the following equalities [3]:

\[ V_{L1} = V_{L2} = V_L \]  

(1)
Experimental Study of SBPWM for Z-Source Inverter Five Phase (M.S.Bakar)

\[ V_{C_i} = V_{C_j} = V_C \]  

\[ (2) \]

Two levels of ZSI five phase produces three states [16], namely, normal state (active state), non-shoot through state (zero state) and shoot through state, which represent synchronized switching condition for any two power devices within the leg. In active and non-shoot through state the ZSI five phase operates under conventional PWM strategy. However, in the shoot-through state, the output five phase H-bridge inverter terminals are shorted at both the upper and the lower switching devices of any of the phase legs [16], while simultaneously, the capacitor voltage is boosted by receiving the energy from the inductor [17]. The total number of shoot-through states of ZSI five phase dealing with the standard formulation is \(2^n-1\) [5], where \(n\) represents the number of phases. Thus, for ZSI five phase, the available total shoot-through states are 31, as shown in Table 1 that has been adopted from [2]. The shoot-through states short-circuit all five AC output terminals and produce 0 V across the AC load. The odd and even number of switches represent the upper and lower switches, respectively.

<table>
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4. SIMPLE BOOST PWM WORKING PRINCIPLE

The SBPWM was the early driving scheme in ZSI. The scheme was approved for boosting criteria by turning the zero state into shoot-through state, keeping the active state unchanged, maintaining the output load in sinusoidal form and, most important, boosting the DC link voltage from the shoot-through affect. This driving scheme was used to control the shoot-through duty ratio, in which the maximum shoot-through duty ratio is limited by \(1-M_i\) [3], [18]. As noted by [3], [18], the relationship between \(M_i\) and boost factor \(B\) under SBPWM that is used to determine voltage gain \(G\) can be described as:

\[
\frac{V_{AC}}{V_{DC}} = M_iB \div 2
\]  

\[ (3) \]
Where $V_{AC}$ is the output peak phase voltage and $V_{DC}$ is the input DC voltage. By rearranging Equation (3), the DC link voltage can be obtained under specific $M_i$ as:

$$V_{DC_{link}} = B V_{DC}$$  \hspace{1cm} (4)

Where $V_{DC_{link}}$ is the voltage across the input to the H-bridge inverter. The effect of $M_i$ and $V_{DC_{link}}$ will be analyzed and compared with the result of simulation established on the Matlab/Simulink and the result of experimental. In SBPWM, a shoot-through periods are generated by a few processes [19]. A sample for the driving scheme of SBPWM for phase A is derived as shown in Figure 2. First, the two constant signals (upper and lower level) are compared to the peak of a triangular carrier signal. Second, the carrier signal is compared to a 50Hz sinusoidal reference signal as in conventional PWM. Third, the product of the two comparisons is loaded into the logical process to obtain a final PWM for ZSI five phase. The PWM signals are then sent to control the power devices (IGBTs) through isolation and gate drive.

![Figure 2. Driving scheme ZSI fivephase for Phase A](image)

5. DESIGN CONSIDERATIONS FOR KEY COMPONENTS

To verify the feasibility of the topology, a maximum 2-kW (under star formation) laboratory prototype operated at 1.5kHz switching frequency was built. The simulation and experimental results will be shown and discussed in the next section. The design considerations for the key components for this research will be discussed in detail as follows. The laboratory prototype for ZSI fivephase used in this study, shown in Figure 3 and Figure 4, is capable of performing open-loop operation for five-phase resistive load with variable $M_i$ up to a maximum of 125 Watt/phase (maximum of 625 Watt under star formation). Table 2 shows the detail parameters of the laboratory prototype.

![Figure 3. The laboratory prototype of ZSI five-phase for linear load and LC filter](image)

![Figure 4. Closer view of the of IGBTs, gate drives and controller systems](image)
Table 2. Z-source inverter five phase system parameters for the simulation and experiment

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tr>
<td>DC input voltage ($V_{DC}$)</td>
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<tr>
<td>Sampling time</td>
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</tr>
<tr>
<td>Switching frequency ($f_s$)</td>
<td>1.5 kHz</td>
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<tr>
<td>Fundamental frequency</td>
<td>50 Hz</td>
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<td>Z-source capacitor ($C_1$ &amp; $C_2$) ($V_{DC}$)</td>
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</tr>
<tr>
<td>Z-source inductor ($L_1$ &amp; $L_2$) (Arms)</td>
<td>1000 µH, 10.6 A</td>
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<td>Load capacitance/phase ($V_{AC}$)</td>
<td>30 µF, 420 V</td>
</tr>
<tr>
<td>Load inductance/phase ($A_{in}$)</td>
<td>5 mH, 10 A</td>
</tr>
<tr>
<td>Load resistance/phase</td>
<td>25 Ω, 125 Watt</td>
</tr>
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</table>

5.1. Component Selection in Z-source Network

The selection of Z-source network component (capacitor and inductor) in ZSI five phase is not straightforward. The fundamental concept that needs to be considered is that the capacitor voltage is assumed to be constant [20]. This is done by selecting a large enough capacitor so that its ripple voltage is sensible low [20]. Once the capacitor has been decided, the inductor is selected using a trial-and-error procedure as its value is related to that of the capacitor. According to the procedure, after fulfilling all the requirements, the value of the inductor can be incrementally increased while following the procedure so as to meet the requirement.

5.2. Main controller ezDSP TMS320F28335

A ezdsp™ TMS320F2812 DSP was selected to apply the control algorithm as it has a 32-bit CPU performing at 150MHz [21], [22]. A feature of this target board is its general purpose input-output (GPIO) ports: GPIOA, B and C that contains 88 pins. These ports are able to integrate with the target support package tool box in Matlab/Simulink and easily loaded to the target board. In this study, the development of SBPWM was performed in the Matlab/Simulink platform and been connected to the specific port of GPIO by setting the appropriate pin assignment. The logical algorithm has also been developed in the Matlab/Simulink platform to gain a final signal of PWM.

6. PERFORMANCE INDICATOR

In this research, the focus is on the system’s performance indicator, which has been defined as its performance and design parameters. Performance parameter [23] is associated with the output control (THD of output voltage/current, and $V_{DClink}$, voltage capacitor and inductor current of Z-source network), while design parameter is related to the input control ($M_i$ and switching frequency).

6.1. Performance Parameter

Total harmonic distortion (THD) is generally used to measure distortion for an inverter [24]. In this study, the output current THD of the system was made to comply with EN61000-3-2 standard, which stated that the maximum permissible current of the 3rd harmonic is 2.3 A [25].

6.2. Design Parameter

The $M_i$ used in this research is in the range of 0.56 to 1.0 (linear modulation). The results obtained from simulation show that the modulation indices were capable of boosting and producing voltage gains that are equal to that predicted from theory as many parameters are set as ideal components in the simulation platform. However, the voltage gains obtained from the experiments are only equal to that predicted from theory when $M_i$ in the range of 0.6 to 1.0 is used. Smaller $M_i$ results in bigger shoot-through period that causes more current to flow through the IGBT. Other factors such as the soldering technique used in the IGBT pre-module, interference from the length of the wiring system among the passive components and equipment noise also affect the shoot-through period, which contribute to the overall interference of the system. To stabilize the system, the problem is compensated by limiting the shoot-through period, which can be achieved by confining the range of $M_i$ is used.

The relationship between $M_i$, shoot-through duty ratio ($D_0$) and voltage gain ($G$) can be expressed as follows [10]:

$$D_0 = 1 - M_i$$

(5)
Equation (5) shows that $D_0$ is inversely proportional to $M_i$. Rearranging Equation (6) results in the following expression [10]:

$$M_i = \frac{G}{2G-1}$$

And $V_{DC_{\text{link}}}$ can be determined as:

$$V_{DC_{\text{link}}} = (2G-1)V_{DC}$$

Based on Equation (7) and (8), the smaller the value of $M_i$, the bigger the value of $V_{DC_{\text{link}}}$ achieved, and the bigger the current flows through the IGBT.

7. RESULTS AND DISCUSSIONS

7.1. Simulation Results

To verify the effectiveness of the topology, simulations were performed to validate the consistency of the boost factor, voltage gain, the limitation of the capacitors voltage stress and the inductors current ripple using Matlab/Simulink. The simulation model uses the parameter as stated in Table 2, with two levels fivephase H-bridge inverter that consists of ten (10) IGBTs. The switching frequency and the sampling frequency are $f_s = 1.5$ kHz and $f_{\text{sam}}=76$ kHz, respectively. The $M_i$ is 0.62, which results in $D_0=0.38$, $B=4.17$ and $G=2.58$. The theoretical peak output phase voltage to neutral is $V_{ac}=51.7$ V, while that obtained from the simulation, shown in Figure 5, is $V_{AC_{\text{simulation}}} \approx 55.6$ V with THD = 2.0%. Figure 6 shows the output current of the resistive load that is connected in star formation. Under steady state condition, THD = 2% and the peak magnitude = 1.96A. Under steady state condition, the theoretical DC link voltage $V_{DC_{\text{link}}} \approx 166.8$ V, while that obtained from the simulation $V_{DC_{\text{link(simulation)}}} \approx 150$ V, as shown in Figure 7. This difference is believed due to the parasitic effects that cause in reducing the voltage gain the experiment.

The steady state condition for the capacitor voltage is 93.6 V, while the average value of inductor current under steady state is 7.14 A, as shown in Figure 8. The ripple capacitor voltage obtained in this simulation is 0.92%, while the ripple inductor current gained for this result is 10A, which is considered as high. The results above should be considered as a great advantage for using ZSI five phase instead of the conventional five-phase inverter since the simulation result nearly equaled that of the theoretical values.
Experimental Study of SBPWM for Z-Source Inverter Five Phase (M.S.Bakar)

7.2. Experimental Results

Real-time laboratory prototype is based on ezdsp™ TMS320F2812DSP. Parameters of the Z-source network, the load and the five phase H-bridge inverter used in the simulation were kept the same as in Table 2. The sampling time used in the experimental setup is similar to that applied in the simulation environment, which is 13µsec. The sampling time was chosen as it must be at least twice the highest analog frequency components (1500Hz switching frequency and 50Hz fundamental frequency).

The output voltage is measured for the four phases in the steady state condition and is as shown in Figure 9. The fifth phase is not shown due to the limited number of channels available on the oscilloscope. Figure 10 shows the output voltage and current for Phase A under steady state condition. These results are nearly the same as the ones presented in the simulation. In order to confirm the shoot-through period, which occurred in each leg of the five-phase H-bridge inverter, the PWM signals during the steady state are experimentally measured in real-time, where the PWM signals for S1, S2, S3 and S4 are shown in Figure 11. The PWM signals for S5, S6, S7 and S8 are shown in Figure 12 and the PWM signals for S9 and S10 are shown in Figure 13. The shoot-through condition (indicated in black dotted-circle) can be clearly observed in each leg, where the PWM gate signals of each leg are in the “ON” high state simultaneously, which means that the two switches of the same leg are in the conduction state. Consequently, the output of the five-phase H-bridge inverter is short-circuited and equal to zero.
In order to measure the THD, the inverter output current waveform during one fundamental period is recorded using a digital storage oscilloscope TPS2024B. Figure 14 shows the THD for output current of phase A for $M_i = 0.62$ with 25 ohm resistive load. Based on the EN61000-3-2 standard under class D specification, the maximum permissible current of 3rd harmonic is 2.3 A [25]. The data in the oscilloscope are subsequently analyzed using a personal computer to determine the current for the 3rd order harmonic, which is found to be 50mA. Hence, this proved that the result for this research complies with EN61000-3-2 standard.

Figure 14. THD output current of phase A under $M_i = 0.62$, with 25 ohm resistive load

Figure 15 shows the $V_{DCLINK} = 162V$ under $M_i = 0.62$ with 25 ohm resistive load compared to 150V achieved in the simulation, as shown in Figure 7. There is a good agreement between the simulated and experimental results as the error between the two is 7%.

The measured capacitor voltage and inductor current under $M_i = 0.62$ with 25 ohm resistive load is shown in Figure 16. Compared to the results obtained from simulation, the error in the capacitor voltage and the inductor current is 8%. As shown in Figure 8(b), the inductor current ripple obtained from the experiment
is 9.2A, which is nearly similar to that obtained from the simulation. This is one feature of SBPWM that produces high DC link voltage.

![Image](image1.png)

**Figure 15.** $V_{DClink}$ under $M_i = 0.62$ with 25 ohm resistive load

![Image](image2.png)

**Figure 16.** Experimental results for Z-source network: (a) inductor current (CH2), and (b) capacitor voltage (CH3) for Phase A under $M_i = 0.62$ with 25 ohm load

8. CONCLUSION AND FUTURE WORK

In this paper, the performance of SBPWM was investigated and analysed, after which the experimental results were compared with that obtained from simulation. The boosting and bucking mode of ZSI five phase was found to operate as predicted when the modulation index $M_i$ is limited to the range of 0.6 to 1.0. Also, THD of the output current complied with the requirements of EN61000-3-2 standard. It is highly recommended that this work be further studied by investigating the reliability of ZSI five phase under close-loop control.

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