Five-Level Diode-Clamped Inverter With Three-Level Boost Converter

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***Abstract*—This paper proposes an active front-end solution to balance the dc-link capacitor voltage of the five-level diode-clamped inverter. Capacitor voltage balancing is performed by a three-level boost converter connected to the two inner capacitors of a five-level diode-clamped inverter and additional balancing circuits at the other two outer capacitors. The proposed configuration is tested through simulation and experiment for various load power factor conditions at a high modulation index. The result demonstrates the reliability of the proposed configuration to balance the dc-link capacitor voltage at the desired level.**

***Index Terms*—DC-link capacitor voltage balancing, diode-clamped, multilevel inverter, three-level boost converter (TLBC).**

I. Introduction

THREE highly popular voltage-source multilevel inverters can be divided into three categories according to their topology: neutral point clamped, flying capacitor, and cascade H-bridge [1]–[3], [40], [41]. Studies on three-, four-, five- and six-level diode-clamped inverters for such use like static VAR compensators, high voltage grid interconnections, and variable speed motor drives have been considered [4]–[16]. It has long been recognized that, for the diode-clamped inverter with more than three levels, a passive front-end capacitor voltage balancing method is only achievable if the modulation index is limited to about 60% of its maximum value for loads with a typical 0.8 power factor [17]–[20]. If the modulation index is increased more than this value, the center capacitors gradually discharge, and finally, the inverter output converges at three levels [21]. To overcome this limitation, a multilevel inverter can be supplied by isolated dc sources [16], [22] such as external circuit as the active front-end solution of dc-link capacitor balancing [17], [21], [23]–[26], using balancing circuit by transferring charge from one capacitor to another capacitor to equilibrium level [11], [12], [27] or the modification of the pulsewidth modulation (PWM) switching pattern [9], [10], [13]–[15], [18], [28]–[32].

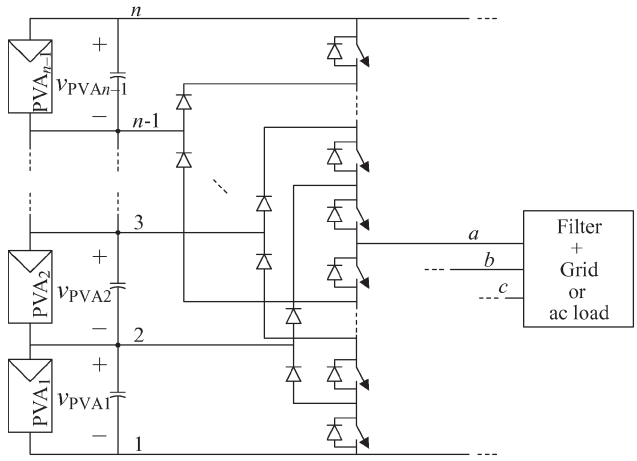

Fig. 1. Connection of $n-1$ series-connected PVAs to the grid (or ac load) through an n-level three-phase diode-clamped inverter.

Many authors proposed PWM strategies for capacitor voltage balancing to avoid extra cost when using active front-end or balancing circuit. This method is found to have limitation on the range of operation with the changing of the power factor and modulation index [19], [20], [29]. Once a PWM strategy is employed for dc-link capacitor voltage balancing, solving problems such as total harmonic distortion, common-mode voltage cancellation, and leakage current elimination with the same strategy is not feasible. It has been pointed out in the introduction of [33] that capacitor voltage balancing and common-mode voltage cancellation cannot be achieved concurrently in a multilevel inverter.

In photovoltaic (PV) power systems, a conventional two-level inverter is supplied by the series connection of PV arrays (PVAs). Partial shading, dust, and disparity in panel aging (yellowing) cause differences in the $V-I$ characteristic of the PV string. The differences result to the rise of several local maximum power points in the string $P-V$ curve that leads to the reduction of the power generated from its potential maximum [15], [28]. It is more practical to install PV with fewer series connections and more on parallel connection [34]. Some authors proposed a substitution of the conventional two-level inverter by a multilevel inverter [28], [35]–[38]. The series of independently controlled PVAs placed parallel to every dc-link capacitor is shown in Fig. 1. By using this configuration, the n-level inverter will need $n-1$ sets of PVAs.

In this paper, a three-level boost converter (TLBC) is used to supply a five-level diode-clamped inverter as shown in Fig. 2.

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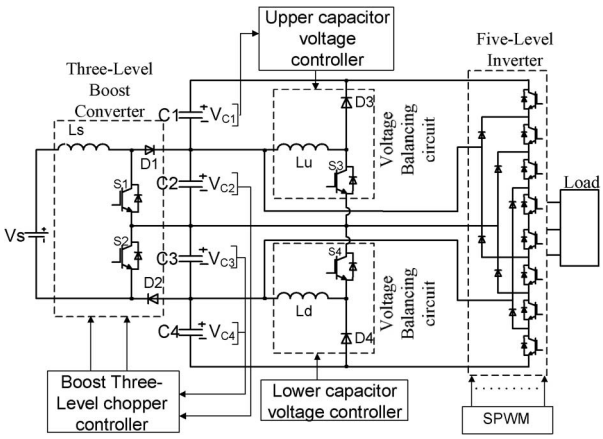


Fig. 2. Proposed three-level (TL) boost chopper and balancer circuit for C1 and C4.

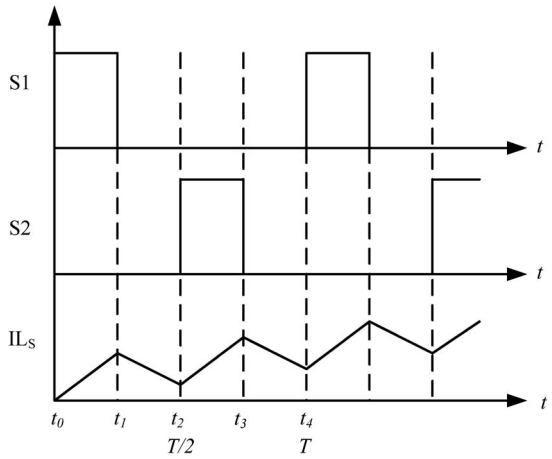


Fig. 3. Switching signal and inductance current waves of boost TL chopper.

In energy conversion system, a boost chopper is often used due to its simple topology and control method [23]–[25], [39]. The TLBC has advantages in high power applications such as reduced switching losses and reduced reverse recovery losses of the diode [23]. With reduced inductor current ripple in TLBC, a smaller size inductor can be used in TLBC compared to the conventional boost converter [26].

DC-link capacitor voltage balancing is performed using a combination of active front-end and balancing circuits. TLBC is used to balance the two inner capacitors, C1 and C2, and another balancing circuit is used to balance the outer capacitors, C1 and C4, by transferring the charge from the inner capacitors to the outer capacitors. All control functions for TLBC, balancing circuits, and the five-level inverter are implemented fully in software with a Texas Instruments TMS320F28335 digital signal controller (DSC). Laboratory experiment results are obtained from a 1.1-kW prototype. The proposed configuration is suitable for a grid-connected PV system which operates in unidirectional power flow. The prototype is tested for various load power factor conditions to evaluate its performance at a high modulation index.

II. Inner Capacitor Balancing With TLBC

The circuit diagram of TLBC is shown in Fig. 2. The switches S1 and S2 are turned on and off alternately. Fig. 3

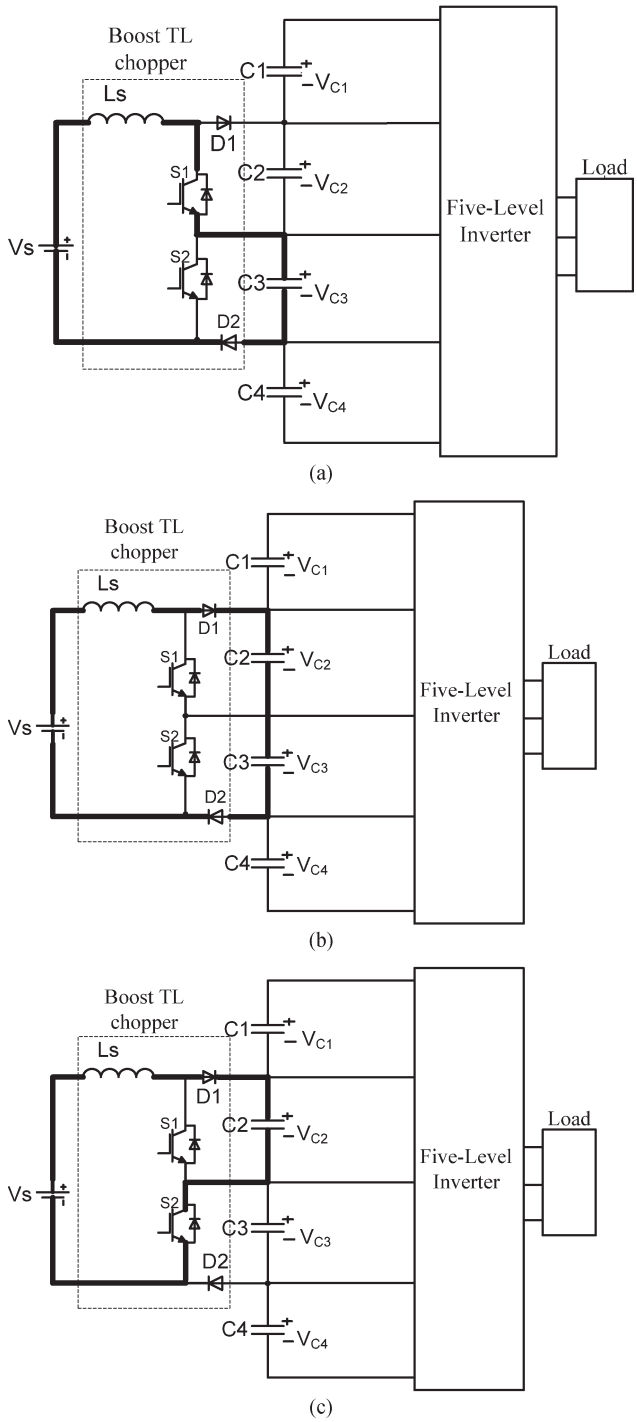


Fig. 4. Inner capacitor balancing using boost TL chopper.

shows the switching signal waveforms and inductor current i_{Ls} for duty ratios $(D < 0.5)$. From t_0 to t_1, S1 is on, and S2 is off; moreover, the inductance current flows in the circuit marked with thick solid lines in Fig. 4(a). The energy is stored in the inductance, capacitor C3 is charged, and V_{C3} gradually rises. From t_1 to t_2 and t_3 to t_4, S1 and S2 are off, and current flow is marked in Fig. 4(b). The energy stored in the inductance is transferred to C2 and C3. From t_2 to t_3, S1 is off, and S2 is on. The inductance current flows in the circuit marked in Fig. 4(c). The energy is stored in inductance, capacitor C2 is charged, and V_{C2} gradually rises.

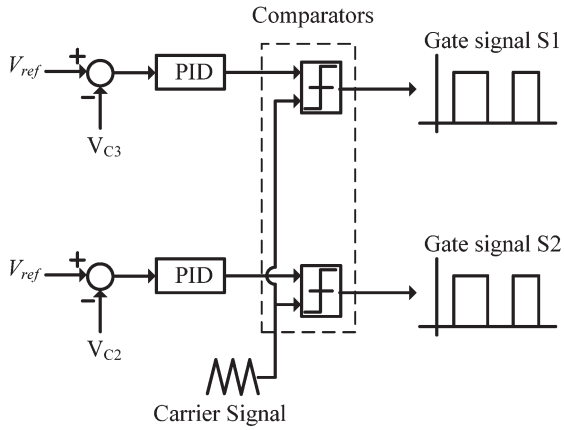


Fig. 5. Control diagram of the boost TL chopper.

Capacitors C2 and C3 can be charged differently to the desired voltage level by controlling the duty ratios D. Increasing the time duration from t_0 to t_1 will increase the voltage at capacitor C3, and increasing the time duration from t_2 to t_3 will increase the voltage at capacitor C2.

TLBC can be operated in five different algorithms [26]. In this paper, only one algorithm where the time switching of S1 and that of S2 do not overlapped each other is used.

The boost feature of the TLBC can be written as

$$V_o = V_{\mathrm{C2}} + V_{\mathrm{C2}} = \frac{2V_s}{(2-D)} \tag{1}$$

where D is the duty ratio of this algorithm $(2t_1/T)$. D is varied from 0 to 1.

The current ripple for the conventional boost inverter can be written as

$$\Delta I = V_s D T_{\mathrm{sw}}/L_s \tag{2}$$

where T_{sw} is the switching frequency of the conventional boost converter.

The current ripple for TLBC operation is

$$\Delta I = \frac{V_o(1-V_s/V_o)(2V_s/V_o-1)}{2L_s f_{\mathrm{sw}}} \tag{3}$$

where f_{sw} is the switching frequency of the conventional boost converter.

From (2) and (3), it shows that the current ripple of TLBC is half of the ripple produced by the conventional boost converter. It suggests that an inductor of smaller size can be used in the TLBC.

To ensure the equal voltage of capacitors C2 and C3, a voltage balancing controller for TLBC, shown in Fig. 5, is used. The duty ratio of the boost switches S1 and S2 is controlled by using a proportional-integral-derivative (PID) controller where V_{ref} is the desired dc voltage at C2 and C3. The PID controller for voltage regulation is designed to have a proportional gain (Kp) of 20, an integral gain (Ki) of 0.003, and a derivative gain (Kd) of 10.

Normally, by using a passive method [11], [12], the dc source is connected between outer capacitors C1 and C4 as shown in Fig. 2, which is four times the individual capacitor voltage level. More series strings of PV panels need to be used to provide higher voltage which is impractical in PV installation [34]. The proposed configuration requires lower voltage level as shown in Fig. 4, where the outer capacitors are not supplied directly from the TLBC. This method is more practical since only one set of PVAs with fewer series-connected PV panels is used.

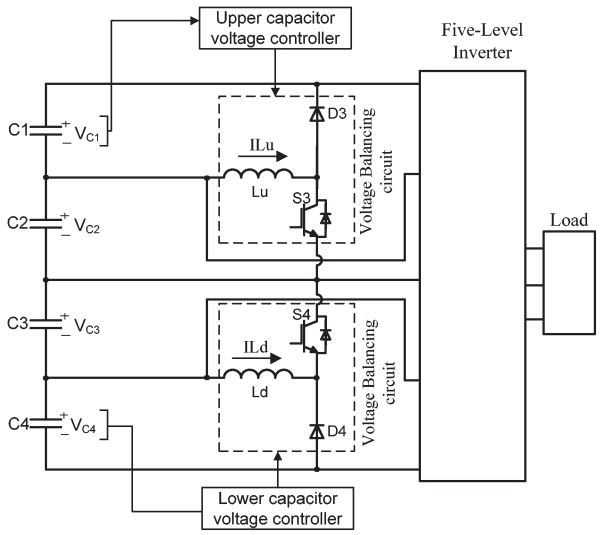


Fig. 6. Outer capacitor balancing circuit.

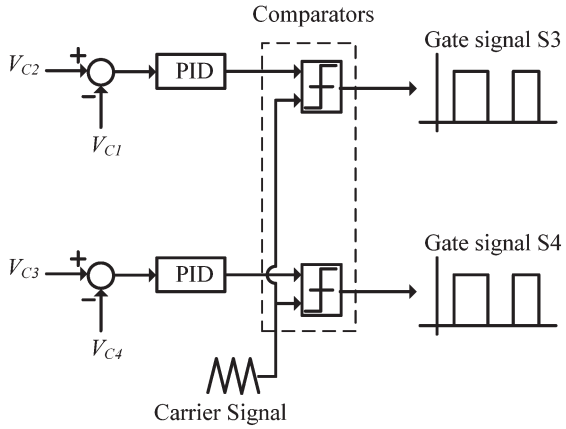


Fig. 7. Balancing circuit control diagram.

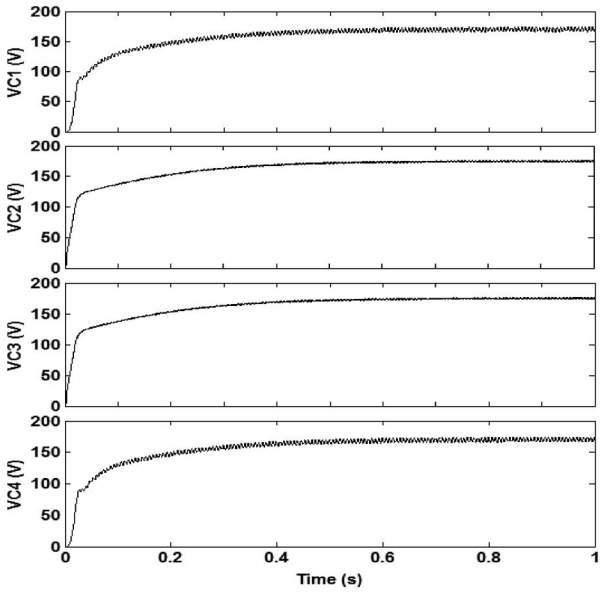


Fig. 8. DC-link capacitor voltage balancing using PID controller.

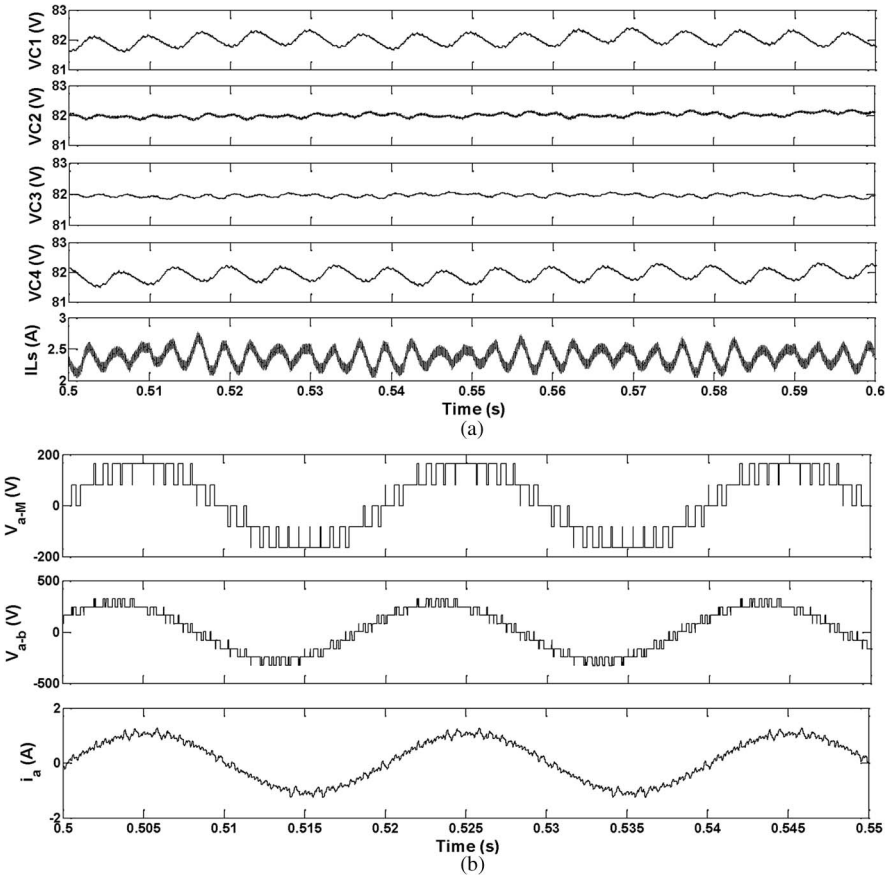


Fig. 9. Simulation results. High resistive load (power factor (PF) $= 0.999$). (a) DC-link voltage and inductor current. (b) Inverter output phase voltage, line–line output voltage, and output line current.

III. Outer Capacitor Balancing

Outer capacitors C1 and C4 are controlled by using the balancing circuit shown in Fig. 6. The voltage at C1, $V_{\rm c1}$, is charged to the voltage level equal to $V_{\rm c2}$, and the voltage at C4, $V_{\rm c4}$, is charged to the voltage level equal to $V_{\rm c3}$ by adjusting the duty ratio of S3 and S4, respectively. Fig. 7 shows the PID controllers used to balance the upper capacitor C1 and lower capacitor C4.

The controller is designed with the value Kp $= 10$, Ki $= 0.001$, and Kd $= 10$. Increasing the duty ratio of S3 and S4 will reduce the charging time of $V_{\rm C1}$ and $V_{\rm C4}$, respectively. However, if the duty ratio is too high, the middle capacitors C2 and C3 will overdischarge and reduce the voltage at these capacitors. To solve this problem, the controller in Fig. 7 must operate at a slower rate than the TLBC controller shown in Fig. 5. Fig. 8 shows the simulation result performance of both the PID controllers balancing all four dc-link capacitors.

During steady state, the upper inductor and lower inductor currents flow continuously ($ILu(t) > 0$ and $ILd(t) > 0$). Therefore, the time integral of the inductor voltage over one time period must be zero

$$V_{\rm C2} t_{\rm 3on} + V_{\rm C1} t_{\rm 3off} = 0. \tag{4}$$

If $V_{\rm C2}$ and $V_{\rm C1}$ are equal in magnitude, the steady-state duty cycle of switch S3 will be 0.5. The duty cycle for switch S4 will also be 0.5 if $V_{\rm C3}$ is equal to $V_{\rm C4}$.

IV. Simulation Results

The proposed configuration has been simulated using MATLAB/Simulink for the BLTC connected to a five-level diode-clamped inverter. The switching frequency of the BLTC was 5 kHz. To examine the balancing of dc-link capacitor voltage, a five-level diode-clamped inverter with a high modulation index of 1.0 is connected to variations of the load power factor.

The results, including dc-link capacitor voltages, inductor current $(I_{\rm Ls})$, inverter load voltages, and inverter load current, are shown in Fig. 9. The magnitude of the reference load voltage is 200 Vrms, the magnitude of the reference dc-link capacitor voltage is 82 V, and the RL load is 150 Ω and 28.7 mH. The frequency of the load voltage is 50 Hz, and the power factor of the load is 0.99. Fig. 9(a) shows the dc-link voltage of 82 V and the BLTC inductor current of 3.2 A. The dc-link voltages have been regulated with small errors, and the performance of the five-level inverter is shown in Fig. 9(b).

The performance of the system is examined for lower power factor and higher frequency. The inverter reference frequency is increased to 100 Hz, and the load power factor is reduced to 0.95 with the RL load of 54.7 Ω and 28.7 mH. The dc-link capacitor voltage, load output voltage, and load current are illustrated in Fig. 10.

To examine with more inductive load, the load resistance is decreased to 24 Ω. Therefore, the power factor has decreased to 0.8, and the dc-link capacitor voltage, load output voltage, and load current are presented in Fig. 11. It can be observed from

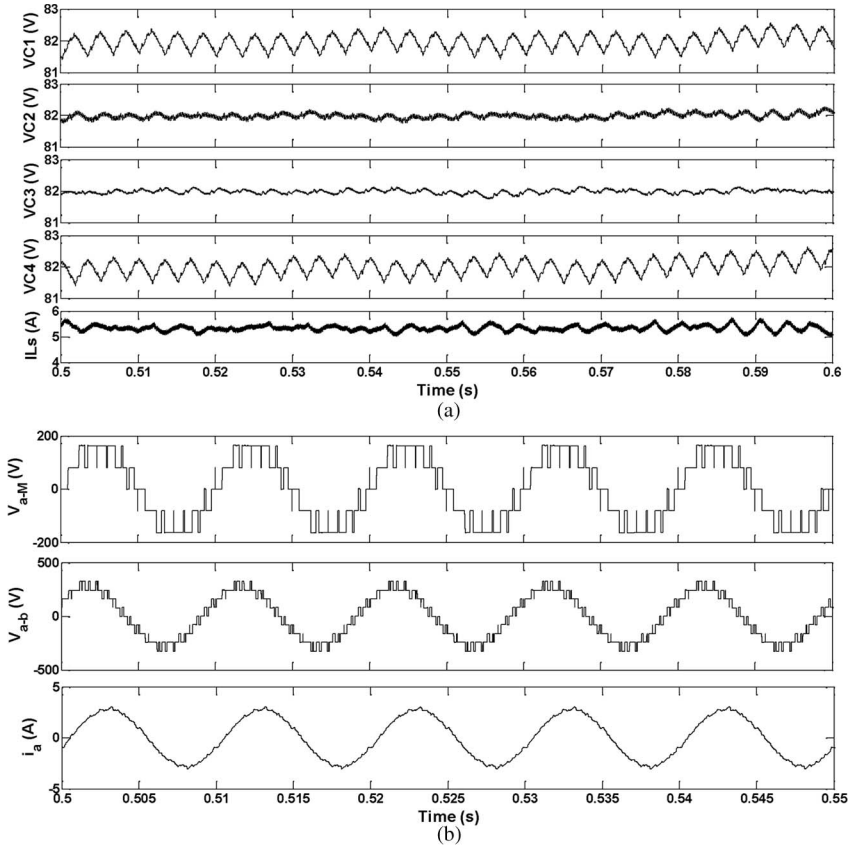


Fig. 10. Simulation results. Low inductive load (power factor (PF) $= 0.95$). (a) DC-link voltage and inductor current. (b) Inverter output phase voltage, line–line output voltage, and output line current.

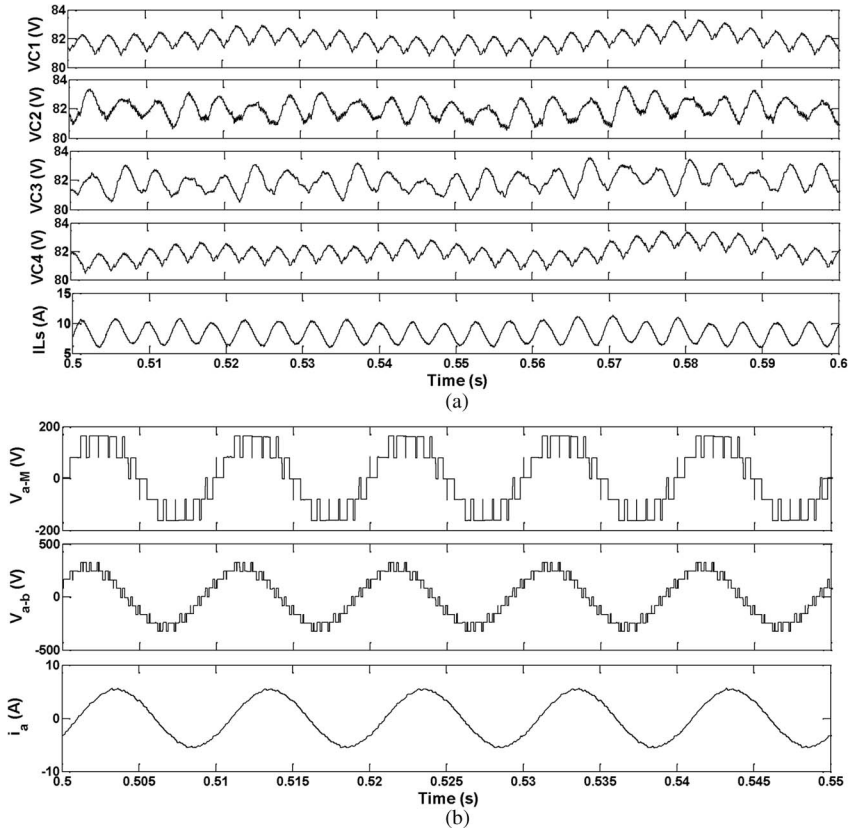


Fig. 11. Simulation results. Highly inductive load (power factor (PF) $= 0.8$). (a) DC-link voltage and inductor current. (b) Inverter output phase voltage, line–line output voltage, and output line current.

TABLE I
PARAMETERS OF THE EXPERIMENTAL CIRCUIT IN FIG. 1

Power rating	P	1.1 kW
DC voltage source	Vs	90 V – 136 V
Inductance of TL boost chopper inductor	Ls	12mH
DC capacitor voltage	V_{C1}, V_{C2}, V_{C3}, V_{C4}	82 V
DC capacitor	C1, C2, C3, C4	2200 µF
Inductance of balancing circuit inductor	Lu, Ld	7 mH
Carrier frequency in five-level inverter		1.5 kHz
Carrier frequency in TL boost chopper		5 kHz
Carrier frequency in balancing circuit		5 kHz
Line-to-line rms output voltage		200 V
R Load		150 Ohm
L Load		28.7 mH
Five-level inverter modulation index		1.0

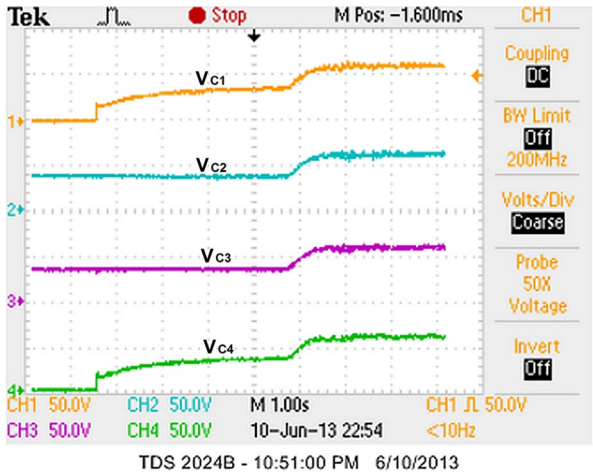


Fig. 12. Capacitor voltages V_{C1}, V_{C2}, V_{C3}, and V_{C4} when TLBC controller operated and both inner capacitor controller and outer capacitor controller operated.

Figs. 9–11 that the dc-link voltage balancing performs well at a high modulation index and various power factor conditions. The inverter performance also has not been affected by the power factor change.

V. EXPERIMENTAL RESULTS

For the verification of the simulation results, the laboratory experiment setup shown in Fig. 1 has been developed and tested. The controllers for the boost three-level converter and inverter have been developed on a Texas Instruments TMS320F28335 DSC. The parameters of the system are shown in Table I.

Fig. 12 presents the voltage waveforms measured at the capacitors C1, C2, C3, and C4. To examine the response of the system, initially, the TLBC controller is operated to regulate the inner capacitor voltage to the desired target value of 40 V, whereas the outer capacitor voltage controller is turned off. Then, the outer capacitor voltage controller is turned on, and the outer capacitor voltage is increased to 40 V. When all dc-link capacitors' voltages exceed 40 V, a new capacitor value $V_{\rm ref}$ of 60 V is set. It can be observed that the dc-link capacitor

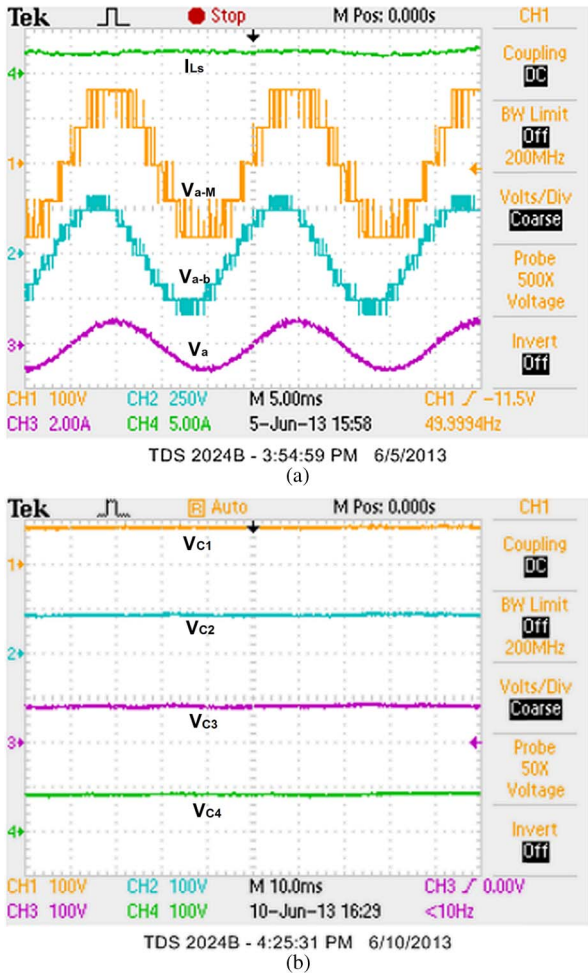


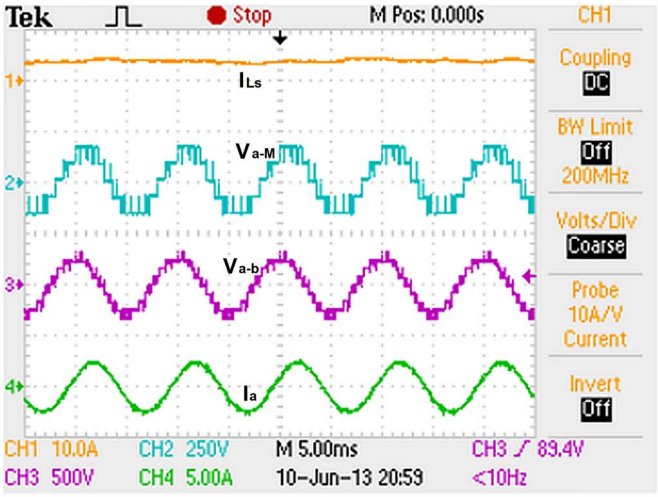
Fig. 13. Experimental results. High power factor (0.99). (a) Inductor current ($I_{\rm Ls}$), load voltage ($V_{\rm aM}$ and $V_{\rm ab}$), and load current ($I_{\rm a}$). (b) Capacitor voltages V_{C1}, V_{C2}, V_{C3}, and V_{C4} at 82 V.

voltage controller operates satisfactorily when regulating all of the dc-link capacitors to the new reference value of 60 V.

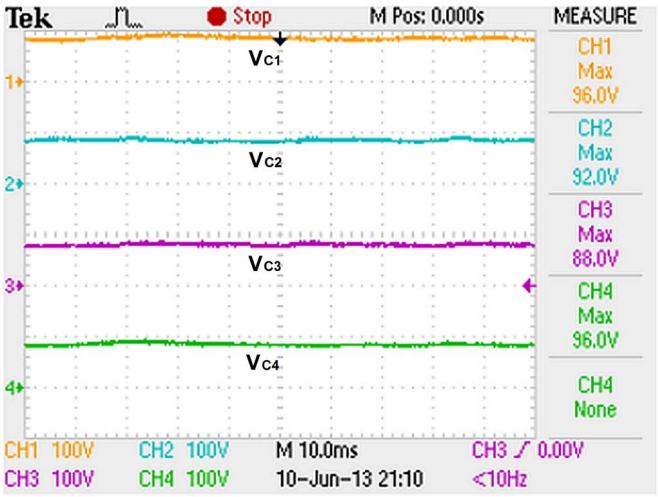
To validate the performance of the system with a high modulation index regardless of changing the load power factor, three experiments have been conducted and evaluated. Fig. 13 shows the experiment results when the inverter is supplying a highly resistive load (power factor of 0.9). The frequency of the inverter reference is 50 Hz, and the RL load of the inverter is 150 Ω and 28.7 mH. It can be observed that the dc-link capacitor voltage regulates at 82 V with small errors and the five-level diode-clamped inverter operates satisfactorily.

To examine the performance of the system for higher frequency and lower power factor, the inverter reference frequency is increased to 100 Hz, and the resistor load is decreased to 54.7 Ω. Therefore, the load power factor decreases to 0.95. The TLBC inductor current, load voltage, and load current are illustrated in Fig. 14(a). DC-link voltages are shown in Fig. 14(b).

To examine a more inductive load, the resistive load is decreased to 20 Ω; therefore, the power factor has decreased to 0.8. The TLBC inductor current, load voltage, and load current are illustrated in Fig. 15(a), and dc-link voltages are shown in Fig. 15(b).

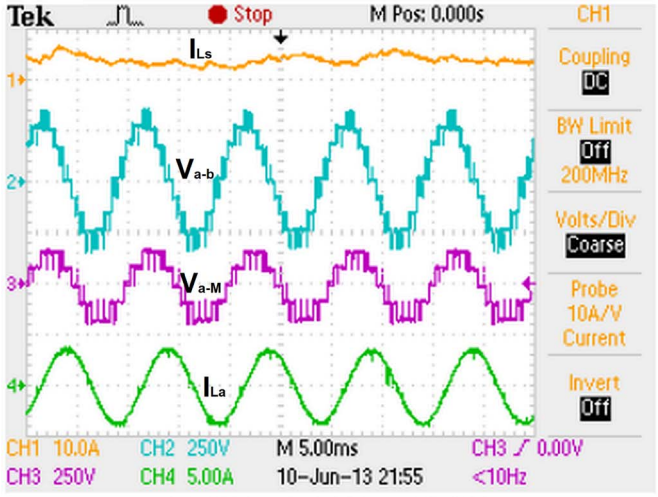


(a)

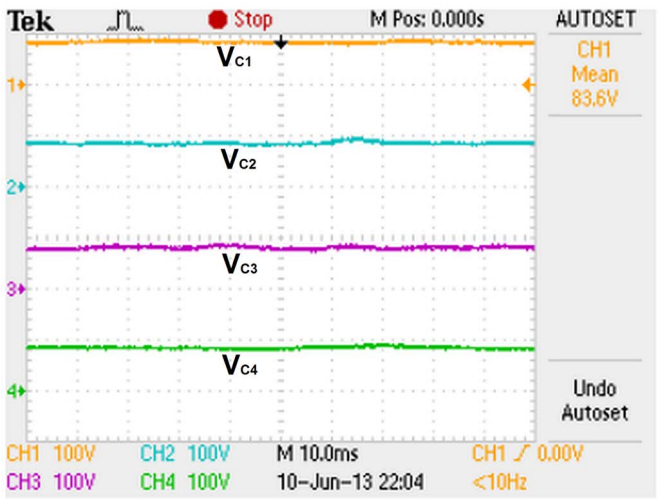


(b)

Fig. 14. Experimental results. Low inductive load (power factor = 0.95). (a) Inductor current (I_{Ls}), load voltage (V_{aM} and V_{ab}), and load current (I_a). (b) Capacitor voltages V_{C1}, V_{C2}, V_{C3}, and V_{C4} at 82 V.



(a)



(b)

Fig. 15. Experimental results. High inductive load (power factor = 0.8). (a) Inductor current (I_{Ls}), load voltage (V_{aM} and V_{ab}), and load current (I_a). (b) Capacitor voltages V_{C1}, V_{C2}, V_{C3}, and V_{C4} at 82 V.

It can be seen from Figs. 13–15 that the dc-link capacitor balancing performance is not affected by the changing of the load power factor, even though the inverter has operated at a high modulation index.

VI. Conclusion

This paper has proposed a new configuration to balance the dc-link capacitor voltages of the five-level diode-clamped inverter. Connecting a TLBC at the input of the inverter regulates the two inner dc-link capacitors' voltage at the desired level with the changing of the converter dc source and, at the same time, provides voltage balancing. Balancing circuits are added to balance the voltage of the two outer capacitors.

Overall, the investigations show that the proposed converter operates well in various load power factor conditions. This configuration is suitable for the grid-connected PV system due to the unidirectional power transfer. In addition, only one set of PVAs is needed instead of four sets of independently controlled PVAs required to supply the inverter in the conventional system.

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