UNIVERSITI MALAYSIA PAHANG

BORANG PENGESAHAN STATUS TESIS♦

JUDUL: MODELING AND SIMULATION OF SINGLE PHASE INVERTER WITH PWM USING MATLAB/SIMULINK

SESI PENGAJIAN: 2007/2008

Saya **MOHAMMAD ARIFF BIN YAAKOB (851015-01-6693)**
(HURUF BESAR)

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Name : MUHAMAD ZAHIM BIN SUJOD

Date : 22 NOVEMBER 2007

DEVELOPMENT OF SINGLE PHASE PWM INVERTER FOR UPS APPLICATION

MOHAMMAD ARIFF BIN YAAKOB

This thesis is submitted as partial fulfillment of the requirement for the award of the Bachelor Degree Electrical Engineering (Power System)

Faculty of Electrical & Electronic Engineering
Universiti Malaysia Pahang

NOVEMBER, 2007

DECLARATION

I declare that this thesis entitled "*Development of Single Phase PWM Inverter for Ups Application*" is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature : .....
Author : MOHAMMAD ARIFF BIN YAAKOB
Date : NOVEMBER 2007

Specially dedicated to
My beloved parent

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ABSTRACT

This project is to develop an inverter circuit for Uninterruptable Power Supply (UPS) application. Inverters are circuit that convert DC to AC. The function of inverter is to create an AC voltage by using a DC voltage source and in UPS system, the voltage source that used DC voltage commonly batteries. Pulse-width modulation (PWM) technique is use in this project because with PWM, the amplitude of the output voltage can be controlled with the modulating waveforms. In this project, Metal Oxide Field Effect Transistor (MOSFET) is used as switch in the full bridge inverter circuit design. For alternated control purpose, sequential switching is designed for PWM get-way through the MOSFET driver. The function of the driver is to control the ON/OFF of the MOSFET. Driver of the MOSFET is essential in the inverter circuit because the driver use to interface between control circuits (low voltage) and inverter circuit (high voltage). The objective of this project is to develop single phase PWM Inverter for UPS application and to design the circuit, simulate and analyze the switching characteristic of single phase PWM inverter. The simulation of full-bridge single phase inverter for this project has been done by using Unipolar scheme and the output waveform is successfully generated. The switching process in hardware is control by PIC 16F877a and the MOSFET driver is using IR2110. At the end of this project, the results from simulation were compared with hardware.

ABSTRAK

Projek ini adalah mengenai pembangunan litar penyongsang untuk aplikasi Bekalan kuasa tidak terganggu (UPS). Penyongsang adalah litar yang mengubah DC ke AC. Fungsi penyongsang adalah untuk menghasilkan voltan AC dengan menggunakan voltan DC dan dalam sistem UPS, sumber voltan DC yang digunakan biasanya bateri. Teknik pemodulatan lebar denyut (PWM) digunakan dalam projek ini kerana dengan PWM, amplitud voltan keluaran boleh dikawal. Dalam projek ini, Metal Oxide Field Effect Transistor (MOSFET) digunakan sebagai suis di dalam litar penyongsang. Untuk tujuan kawalan yang berulang, pensuisan berkala direkabentuk sebagai penghubung kepada pemandu MOSFET. Fungsi pemandu adalah untuk mengawal "ON/OFF" MOSFET. Pemandu MOSFET adalah penting dalam litar penyongsang kerana ianya digunakan sebagai penghubung antara litar kawalan (voltan rendah) dan litar penyongsang (voltan tinggi). Objektif projek ini adalah untuk merekabentuk litar, mesimulasi dan menganalisis ciri-ciri pengsuisan penyongsang fasa tunggal. Simulasi penyongsang fasa tunggal dijalankan dengan menggunakan skim unipolar. Proses pensuisan didalam perkakas dikawal dengan menggunakan PIC 16F877 dan pemandu MOSFET yang digunakan ialah IR2110. Pada pengakhir projek ini, keputusan daripada simulasi dibanding dengan keputusan perkakas.

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LIST OF ABBREVIATION

DC	-	Direct Current
AC	-	Alternate Current
PWM	-	Pulse Width Modulation
SPWM	-	Sinusoidal Pulse Width Modulation
IGBT	-	Insulated Gate Bipolar Transistor
MOSFET	-	Metal Oxide Field Effect Transistor
UPS	-	Uninterruptable Power Supply
PIC	-	Programmable Intelligent Computer

LIST OF APPENDICES

CHAPTER 1

INTRODUCTION

1.1 Background

This chapter explains briefly about Inverter and its operation. This chapter also explains the overview of project objectives, scopes and thesis outline.

1.2 Overview of Inverter Project

Inverters are circuits that convert DC to AC. More precisely, inverters transfer power from a DC source to an AC load. The function of inverter is to create an AC voltage by using a DC voltage source and in UPS system, the voltage source that used DC voltage commonly batteries. Inverters are used in applications such as adjustable-speed AC motor drives, uninterruptable power supplies (UPS), and AC appliances run from an automobile battery.

In this report, a design for a power inverter circuit is presented for conversion of energy from DC battery to AC power to be used mainly for Uninterruptable Power Supply (UPS) applications. The configuration is achieved using a full-bridge PWM

inverter. DC-DC converter circuit not been constructed in this project and DC supply from High voltage DC supply been used.

In this project, PIC microcontroller used to control the output by using sinusoidal pulse width modulation technique based on open loop configuration system. The proposed practical circuit operates from a 340V DC input and outputs a regulated 240V AC, 50Hz voltage. A complete circuit analysis, design and cost evaluation is presented and supported by PSPICE simulation results.

1.3 Objective

The objective of this project is to develop single phase PWM Inverter for UPS application. In this part, the development of PWM Inverter circuit is the main task of this project to convert DC power from battery to AC. These projects also develop an open-loop control system by using PIC microcontroller to control output voltage. The other objectives of this project are to design the circuit, simulate and analyze the switching characteristic of single phase PWM inverter.

1.4 Scope of the Project

The main scopes of this project are;

i. Design PWM Inverter circuit that generates $240V_{RMS,}$ 50Hz and 500W of power.
ii. Microcontroller used as a controller to control switching process. The type of PIC used is PIC16F877.
iii. ORCAD PSpice and Multisim PSpice program are used to simulate and design the circuit.

CHAPTER 2

THEORY AND LITERATURE REVIEW

2.1 Uninterruptible Power Supply (UPS)

Figure 2.1: Small UPS

An uninterruptible power supply (UPS), uninterruptible power source or sometimes called a battery backup is a device which maintains a continuous supply of electric power to connected equipment by supplying power from a separate source when utility power is not available [1].

A UPS is inserted between the source of power (typically commercial utility power) and the load it is protecting. When a power failure or abnormality occurs, the UPS will effectively switch from utility power to its own power source almost instantaneously [1].

While not limited to any particular type of equipment, a UPS is typically used to protect computers, telecommunication equipment or other electrical equipment where an unexpected power disruption could cause injuries, fatalities, serious business disruption or data loss. UPS units come in sizes ranging from units which will back up a single computer without monitor (around 200 VA) to units which will power entire data centers or buildings (several megawatts). Larger UPS units typically work in conjunction with generators [1].

Historically, UPS were very expensive and were most likely to be used on expensive computer systems and in areas where the power supply is interrupted frequently. However, UPS units are now more affordable, and have become an essential piece of equipment for data centers and business computers, but are also used for personal computers, entertainment systems and more [1].

In certain countries, where the electrical grid is under strain, providers struggle to ensure supply during times of peak demand (such as summer, during which air-conditioning usage increases). In order to prevent blackouts, electrical utilities will sometimes use a process called rolling blackouts or load shedding, which involves cutting the power to large groups of customers for short periods of time. Several major blackouts occurred in 2003, most notably the 2003 North America blackout in the north-eastern US and eastern Canada and the 2003 Italy blackout, both of which affected over 50 million people, and brought attention to the need for UPS power backup units [1].

A UPS is not to be confused with a standby generator, which does not provide protection from a momentary power interruption and may result in an interruption when it is switched into service, whether manually or automatically. However, such generators are typically placed before the UPS to provide cover for lengthy outages [1].

2.2 Microcontroller (PIC 16F877A).

PIC is a family of Harvard architecture microcontrollers made by Microchip Technology, derived from the PIC1650 originally developed by General Instrument's Microelectronics Division. The name PIC was originally an acronym for "**Programmable Intelligent Computer**".

Figure 2.2: PIC16F8777A

In this project, a microcontroller; PIC16F877a (Figure 2.2) is use to control the output. The reason for use microcontroller is the PIC architecture is distinctively minimalist. It is characterized by the following features:

- separate code and data spaces
- a small number of fixed length instructions
- most instructions are single cycle execution (4 clock cycles), with single delay cycles upon branches and skips

- a single accumulator (W), the use of which (as source operand) is implied
- All RAM locations function as registers as both source and/or destination of math and other functions.
- data space mapped CPU, port, and peripheral registers
- the program counter is also mapped into the data space and writable (this is used to synthesize indirect jumps)
- 10-bit multi-channel Analog-to-Digital converter
- has 33 input or output ports (see Figure 2.3)

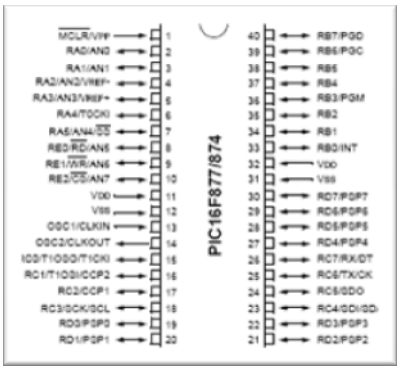


Figure 2.3: PIC Schematic

Unlike most other CPUs, there is no distinction between "memory" and "register" space because the ram serves the job of both memory and registers, and the ram is usually just referred to as the register file or simply as the registers.

PIC microcontroller have a very small set of instructions (only 35 instruction), leading some to consider them as RISC devices, however many salient features of RISC CPU's are not reflected in the PIC architecture. For example:

- it does not have load-store architecture, as memory is directly referenced in arithmetic and logic operations
- it has a singleton working register, whereas most modern architectures have significantly more

PIC have a set of register files that function as general purpose RAM, special purpose control registers for on-chip hardware resources are also mapped into the data space. The addressability of memory varies depending on device series, and all PIC devices have some banking mechanism to extend the addressing to additional memory. Later series of devices feature move instructions which can cover the whole addressable space, independent of the selected bank. In earlier devices (ie. the baseline and mid-range cores), any register move had to be through the accumulator.

To synthesize indirect addressing, a "file select register" (FSR) and "indirect register" (INDF) are used: A read or write to INDF will be to the memory pointed to by FSR. Later devices extended this concept with post and pre increment/decrement for greater efficiency in accessing sequentially stored data. This also allows FSR to be treated like a stack pointer.

All PICs feature Harvard architecture, so the code space and the data space are separate. PIC code space is generally implemented as EPROM, ROM, or FLASH ROM. In general, external code memory is not directly addressable due to the lack of an external memory interface.

The PIC architecture has no (or very meager) hardware support for saving processor state when servicing interrupts. The 18 series improved this situation by implementing shadow registers which save several important registers during an interrupt. The PIC architecture may be criticized on a few important points.

- The few instructions, limited addressing modes, code obfuscations due to the "skip" instruction and accumulator register passing makes it difficult to program in assembly language, and resulting code difficult to comprehend. This drawback has been alleviated by the increasing availability of high level language compilers.

- Data stored in program memory is space inefficient and/or time consuming to access, as it is not directly addressable.

2.3 HV Floating MOS-Gate Driver IC

2.3.1 Gate Drive Requirements of High-Side Devices

The gate drive requirements for a power MOSFET or IGBT utilized as a high-side switch (the drain is connected to the high voltage rail, as shown in Figure 2.4) driven in full enhancement (i.e., lowest voltage drop across its terminals) can be summarized as follows:

1. Gate voltage must be 10 V to 15 V higher than the drain voltage. Being a high-side switch, such gate voltage would have to be higher than the rail voltage, which is frequently the highest voltage available in the system.

2. The gate voltage must be controllable from the logic, which is normally referenced to ground. Thus, the control signals have to be level-shifted to the source of the high-side power device, which, in most applications, swings between the two rails.

3. The power absorbed by the gate drive circuitry should not significantly affect the overall efficiency.

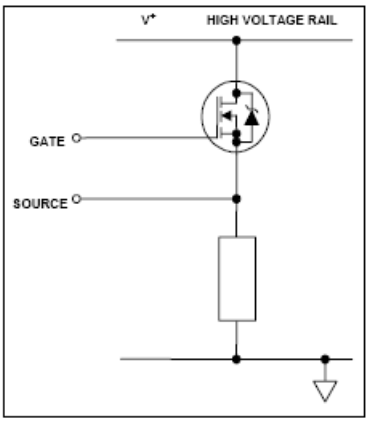


Figure 2.4: Power MOSFET in the High-Side Configuration

With these constraints in mind, several techniques are presently used to perform this function. Each basic circuit can be implemented in a wide variety of configurations [2].

International Rectifier's family of MOS-gate drivers (MGDs) integrate most of the functions required to drive one high-side and one low-side power MOSFET or IGBT in a compact, high performance package. With the addition of few components, they provide very fast switching speeds and low power dissipation. They can operate on the bootstrap principle or with a floating power supply. Used in the bootstrap mode, they can operate in most applications from frequencies in the tens of Hz up to hundreds of kHz [2].

2.3.2 Low-Side Channel

The driver's output stage is implemented either with two n-channel MOSFETs in the totem pole configuration (source follower as a current source and common source for current sinking), or with an n-channel and a p-channel CMOS inverter stage. Each MOSFET can sink or source gate currents from 0.12 A to 4 A, depending on the MGD. The source of the lower driver is independently brought out

to the COM pin so that a direct connection can be made to the source of the power device for the return of the gate drive current. An under voltage lockout prevents either channel from operating if V_{CC} is below the specified value (typically 8.6/8.2 V) [2].

Any pulse that is present at the input pin for the low-side channel when the UV lockout is released turns on the power transistor from the moment the UV lockout is released. This behavior is different from that of the high-side channel [2].

2.3.3 High-Side Channel

This channel has been built into an "isolation tub" capable of floating from 500 V or 1200 V to -5 V with respect to power ground (COM). The tub "floats" at the potential of V_S. Typically this pin is connected to the source of the high-side device, as shown in Figure 2 and swings with it between the two rails [2].

If an isolated supply is connected between V_B and V_S, the high-side channel will switch the output (HO) between the positive of this supply and its ground in accordance with the input command [2].

One significant feature of MOS-gated transistors is their capacitive input characteristic (i.e., the fact that they are turned on by supplying a charge to the gate rather than a continuous current). If the high-side channel is driving one such device, the isolated supply can be replaced by a bootstrap capacitor (C_{BOOT}) [2].

The gate charge for the high-side MOSFET is provided by the bootstrap capacitor which is charged by the 15 V supply through the bootstrap diode during the

time when the device is off (assuming that V_S swings to ground during that time, as it does in most applications). Since the capacitor is charged from a low voltage source the power consumed to drive the gate is small. The input commands for the high-side channel have to be level-shifted from the level of COM to whatever potential the tub is floating at which can be as high as 1200 V. As shown in Figure 2 the on/off commands are transmitted in the form of narrow pulses at the rising and falling edges of the input command. They are latched by a set/reset flip-flop referenced to the floating potential [2].

The use of pulses greatly reduces the power dissipation associated with the level translation. The pulse discriminator filters the set/reset pulses from fast dv/dt transients appearing on the V_S node so that switching rates as high as 50 V/ns in the power devices will not adversely affect the operation of the MGD. This channel has its own under voltage lockout (on some MGDs) which blocks the gate drive if the voltage between V_B and V_S (i.e., the voltage across the upper totem pole) is below its limits. The operation of the UV lockout differs from the one on V_{CC} in one detail: the first pulse *after* the UV lockout has released the channel changes the state of the output. The high voltage level translator circuit is designed to function properly even when the V_S node swings below the COM pin by a voltage indicated in the datasheet (typically 5 V). This occurs due to the forward recovery of the lower power diode or to the LdI/dt induced voltage transient [2].

2.3.4 How to Select the Bootstrap Components

The bootstrap diode and capacitor are the only external components strictly required for operation in a standard PWM application. Local decoupling capacitors on the V_{CC} (and digital) supply are useful in practice to compensate for the inductance of the supply lines [3].

The voltage seen by the bootstrap capacitor is the V_{CC} supply only. Its capacitance is determined by the following constraints:

1. Gate voltage required to enhance MGT
2. I_{QBS} - quiescent current for the high-side driver circuitry
3. Currents within the level shifter of the control IC
4. MGT gate-source forward leakage current
5. Bootstrap capacitor leakage current

Factor 5 is only relevant if the bootstrap capacitor is an electrolytic capacitor, and can be ignored if other types of capacitor are used. Therefore it is always better to use a non-electrolytic capacitor if possible [3].

The minimum bootstrap capacitor value can be calculated from the following equation:

$$C \geq \frac{2\left[2Q_g + \frac{I_{qbs(max)}}{f} + Q_{ls} + \frac{I_{Cbs(leak)}}{f}\right]}{V_{cc} - V_f - V_{LS} - V_{min}} \qquad (2.1)$$

Where:

Q_g = Gate charge of high-side FET

f = frequency of operation

$I_{Cbs\ (leak\ )}$ = bootstrap capacitor leakage current

$I_{qbs\ (max)}$ = Maximum VBS quiescent current

V_{CC} = Logic section voltage source

V_f = Forward voltage drop across the bootstrap diode

V_{LS} = Voltage drop across the low-side FET or load

V_{Min} = Minimum voltage between VB and VS.

Q_{ls} = level shift charge required per cycle (typically 5 nC for 500 V/600 V MGDs and 20 nC for 1200 V MGDs)

The bootstrap diode must be able to block the full voltage, this occurs when the top device is on and is about equal to the voltage across the power rail. The current rating of the diode is the product of gate charge times switching frequency. For an IRF450 HEXFET power MOSFET operating at 100 kHz it is approximately 12 mA [3].

The high temperature reverse leakage characteristic of this diode can be an important parameter in those applications where the capacitor has to hold the charge for a prolonged period of time. For the same reason it is important that this diode have an ultra-fast recovery to reduce the amount of charge that is fed back from the bootstrap capacitor into the supply [3].

2.3.5 How to Deal With Negative Transients on the V_s Pin

Of the problems caused by parasitics, one of the main issues for control ICs is a tendency for the V_S node to undershoot the ground following switching events. Conversely, overshoot does not generally present a problem due to the high differential voltage capability of International Rectifier's proven HVIC process [2].

International Rectifier's control ICs are guaranteed to be completely immune to V_S undershoot of at least 5 V, measured with respect to COM. If undershoot exceeds this level, the high-side output will temporarily latch in its current state. Provided V_S remains within absolute maximum limits the IC will not suffer damage, however the high-side output buffer will not respond to input transitions while undershoot persists beyond 5 V. This mode should be noted but proves trivial in most applications, as the high-side is not usually required to change state immediately following a switching event [2].

The signals listed below should be observed both in normal operation and during high-stress events such as short circuit or over-current shutdown, when di/dt is highest. Readings should always be taken directly across IC pins as shown in Figure 2.5, so that contributions from the parasitics in the drive coupling are included in the measurement [2].

(1) High-side offset with respect to common; V_S-COM

(2) The floating supply; V_B - V_S

The following guidelines represent good practice in control IC circuits and warrant attention regardless of the observed latch-up safety margin [2].

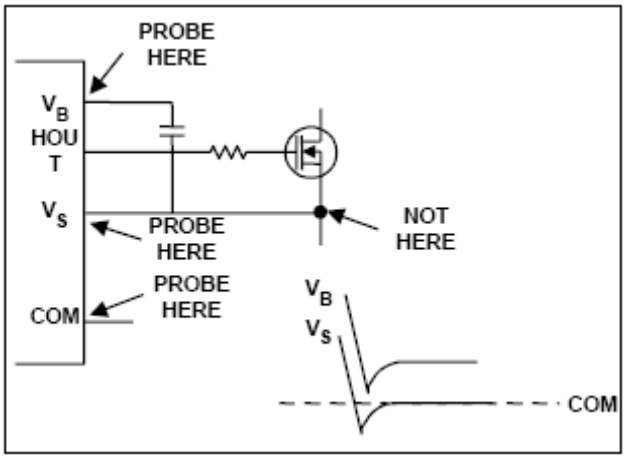


Figure 2.5: Considering the V_S Spike during the Reverse Recovery

2.3.6 Minimize the Parasitics

1) Use thick, direct tracks between switches with no loops or deviation.
2) Avoid interconnect links. These can add significant inductance.
3) Reduce the effect of lead-inductance by lowering package height above the PCB.
4) Consider co-locating both power switches to reduce track lengths.

2.3.7 Reduce Control IC Exposure

1) Connect V_S and COM as shown in Figure 2.6.
2) Minimize parasitics in the gate drive circuit by using short, direct tracks.
3) Locate the control IC as close as possible to the power switches.

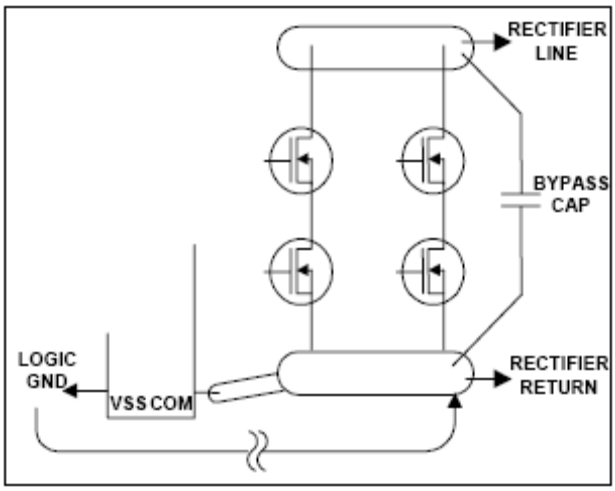


Figure 2.6: Ground Connections and Layout

2.3.8 Improve Local Decoupling

1) Increase the bootstrap capacitor (C_B) value to above 0.47 µF using at least one low-ESR capacitor. This will reduce overcharging from severe V_S undershoot.
2) Use a second low-ESR capacitor from V_{CC} to COM. As this capacitor supports both the low-side output buffer and bootstrap recharge, we recommend a value at least ten times higher than C_B.
3) Connect decoupling capacitors directly across the appropriate pins as shown in Figure 2.7.
4) If a resistor is needed in series with the bootstrap diode, verify that V_B does not

fall below COM, especially during start-up and extremes of frequency and duty cycle.

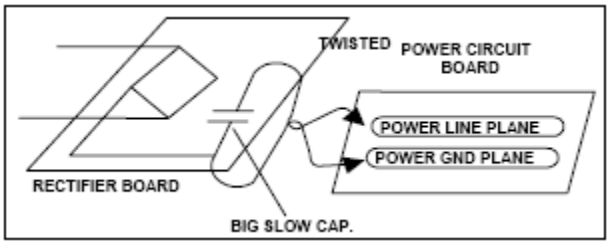


Figure 2.7: Power Bypass Capacitor

Granted proper application of the above guidelines, the effects of V_S undershoot will be minimized at source. If the level of undershoot is still considered too high, then some reduction of dv/dt may be necessary [2].

External snubbing and/or increasing gate drive resistance may be used to trade efficiency for lower switching rate. If the system will not tolerate this, then fast anti-parallel clamping diodes may be considered appropriate. HEXFRED diodes are ideal for this purpose [2].

2.4 Inverter

2.4.1 Power Inverter

A power inverter is a device that converts DC (Direct Current) power into AC (Alternating Current) power. The AC output is usually 120 VAC, 60 Hz (USA domestic power) or 230 VAC, 50 Hz (International power). Aircraft applications often require 115 VAC, 400 Hz. Nova Electric offers all three of these common output voltages, in both single and three-phase configurations, as well as other special / custom outputs [4].

2.4.2 Inverter Applications

With a large enough battery bank, or a large enough alternator output from a vehicle, almost anything within reason can be operated from a power inverter – this assumes that the inverter has the proper power output for the given load. Everyday appliances such as microwaves, power tools, TVs and VCRs, lights, audio/visual equipment, battery chargers and computers are common loads. An inverter sized for loads with heavy inrush current can be used to power air compressors, water pumps, heaters, ventilation fans, and air conditioners. Nova Electric's Pure Sine Wave inverters are ideal for running sensitive test equipment such as communications equipment, oscilloscopes, scales, high end stereos & video equipment, communications equipment, etc [4].

2.4.3 Types of Inverter

Square Wave: Square Wave units could be harmful to some electronic equipment, especially equipment with transformers or motors. The square wave output has a high harmonic content which can lead such equipment components to overheat Square Wave units were the pioneers of inverter development and, like the horse and buggy, are no longer relevant for modern use [4].

Modified Square Wave: The most common, general-use inverters available are "Modified Sine Wave". Usually available at more moderate pricing compared to pure sine wave models. Modified Square Wave (or "Modified Sine Wave" and "Quasi Sine Wave") output inverters are designed to have somewhat better characteristics than Square Wave units, while still being relatively inexpensive. Although designed emulate a Pure Sine Wave output, Modified Square Wave inverters do not offer the same perfect electrical output. As such, a negative by-product of Modified output units is electrical

noise, which can prevent these inverters from properly powering certain loads. For example, many TVs and stereos use power supplies incapable of eliminating common mode noise. As a result, powering such equipment with a Modified Square Wave may cause a "grain" or small amount of "snow" on your video picture, or "hum" on your sound system. Likewise, most appliances with timing devices, light dimmers, battery chargers, and variable speed devices may not work well, or indeed, may not work at all [4].

Pure Sine Wave: Pure or True Sine Wave inverters provide electrical power similar to the utility power you receive from the outlets in your home or office, which is highly reliable and does not produce electrical noise interference associated with the other types of inverters. With its "perfect" sine wave output, the power produced by the inverter fully assures that your sensitive loads will be correctly powered, with no interference. Some appliances which are likely to require Pure Sine Wave include computers, digital clocks, battery chargers, light dimmers, variable speed motors, and audio/visual equipment. If your application is an important video presentation at work, opera on your expensive sound system, surveillance video, a telecommunications application, any calibrated measuring equipment, or any other sensitive load, you must use a Pure Sine Wave inverter [4].

2.4.4 Basic Half-Bridge Inverter Circuit Resistive Load

To illustrate the basic concept of a DC-to-AC inverter circuit we consider a half-bridge voltage-source inverter circuit under resistive load as shown in Fig. 2.8 (a). Its switching waveforms for S1, S2 and the result output voltage are shown in Fig. 2.8 (b).

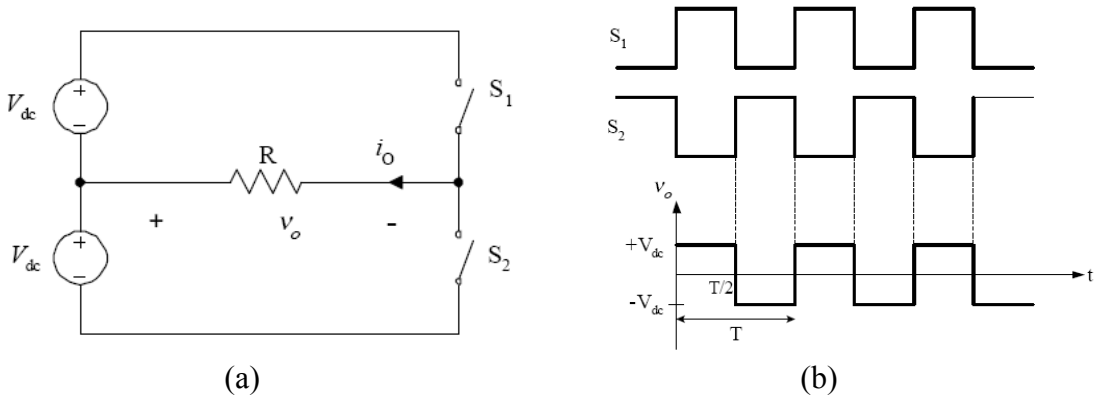


Figure 2.8: (a) Half-bridge Inverter under resistive load (b) Switching and output voltage waveform

The circuit operation is very simple since S1 and S2 are switched on and off alternatively at 50% duty cycle as shown in the switching waveform in Fig. 2.8 (b). This shows that the circuit generates a square ac voltage waveform across the load from a constant dc source. The voltages, V_{DC} and $-V_{DC}$ are across R when S1 ON while S2 OFF and when S2 is ON while S1 is OFF, respectively. One observation to be made here is that the frequency of the output voltage is equal to $f = 1/T$ and is determined by the switching frequency. This is true as long as S1 and S2 are switched complementarily. Moreover, the *rms* value of the output voltage is simply V_{DC}. Hence, to control the *rms* value of the output voltage we must control the rectified V_{DC} voltage source. Another observation is that the load power factor is unity since we have purely resistive load. That is rarely encountered in practical application.

Finally, we should note that in practice the above circuit does not require two equal dc voltage sources as shown in Fig. 2.8 (a). Instead, large splitting capacitors are used to produce two equal DC voltage sources [5].

The two capacitors are equal and very large so that RC is much larger than the half-switching period. This will guarantee that the mid-point, *a*, between the capacitors has a fixed potential at one-half of the supply voltage V_{DC} [5].

2.4.5 Inductive-Resistive Load

Figure 2.9 (a) shows a half-bridge inverter under inductive resistive load with the equivalent circuit and the output waveforms shown in Fig. 2.9 (b) and (c), respectively.

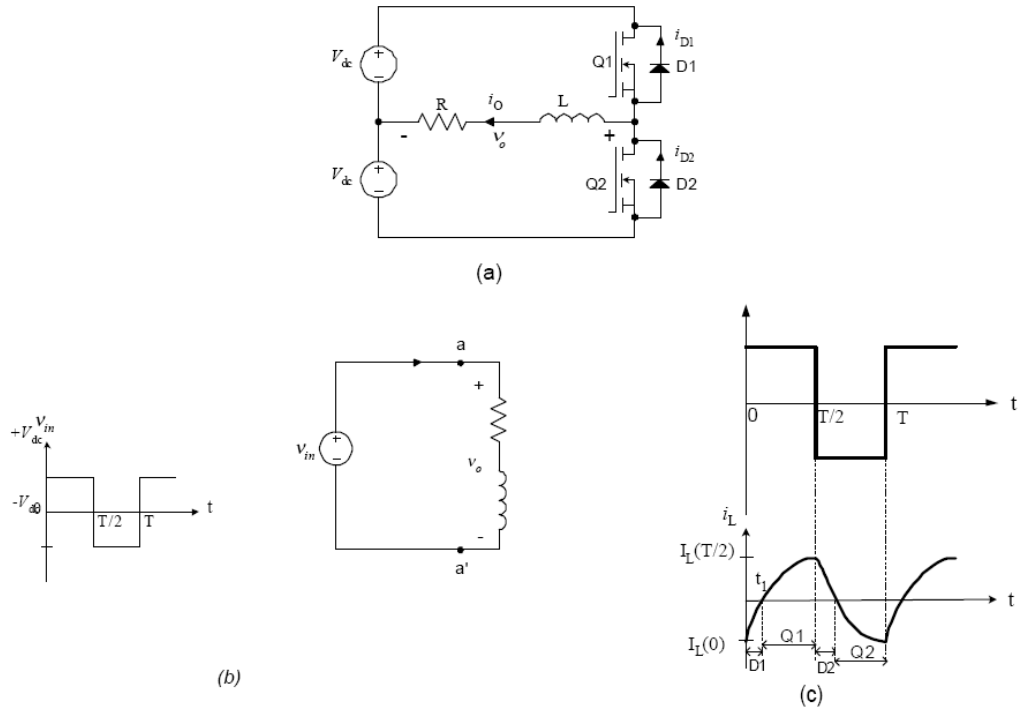


Figure 2.9 (a) Half-bridge inverter with inductive resistive load (b) Equivalent circuit and (c) Steady state waveforms.

With Q1 and Q2 switched complementary each at 50% duty cycle with switching frequency f , then the load between terminal a and $a¢$ is excited by square voltage waveform v (*t*) *in* of amplitudes $+V$ *dc* and $–V$ *dc* as shown in Fig. 2.9 (b), i.e. v (*t*) *in* is defined as follows:

$$v_{in}(t) = \begin{cases} +V_{dc} & 0 \le t < T/2 \\ -V_{dc} & T/2 \le t < T \end{cases} \qquad (2.2)$$

The switches are implemented by using conventional SCR (that require external forced commutation circuit) or fully controlled power switching devices such as IGBTs,

GTOs, BTJs or MOSFETs. Notice from the load current i_L direction, these switches must be bi-directional. Assume the inverter operates in steady state and its inductor current waveform is shown in Fig. 2.9(c) for 1 $0 < t < t$, *the* inductor current is negative which means while Q1 is ON the current actually flows in the reverse direction, i.e. in the body diode of the bi-directional switch Q1. At 1 $t = t$, the current flows through the transistor Q1 as shown. At $t = T$ 2, when S2 is turned ON, since the current direction is positive, the flyback diode, D2, turns ON until 1 $t = T$ 2 + t when Q2 starts conducting [5].

2.4.6 Sinusoidal PWM Waveforms

In Sinusoidal Pulse Width Modulation, SPWM, multiple pulses are generated, each having different width time. The width of each pulse is varied in proportion to the instantaneous integrated value of the required fundamental component at the time of its event. In other words, the pulse width becomes a sinusoidal function of the angular position. The repetition frequency of the output voltage will be a frequency higher than the fundamental. In applying SPWM, the lower order harmonics of the modulated voltage wave are highly reduced in contrast to the use of uniform pulse width modulation [5].

In SPWM the output voltage signal can be obtained by comparing a control signal, *cont v* , against a sinusoidal reference signal, *ref v* , at the desired frequency as shown in Fig 2.10. At the first half of the output period, output voltage takes a positive value (+ *dc V*), whenever the reference signal is greater than the control signal. At the same way, at the second half of the output period, the output voltage takes a negative value (- *dc V*) whenever the reference signal is less than the control signal [5].

The control frequency *cont f* determines the number of pulses per half of cycle for the output voltage signal. Also, the output frequency O_f is determined by the

reference frequency *ref f.* The modulation index Ma is defined as the ratio between the sinusoidal magnitude and the control signal magnitude [5].

To obtain a vary train of pulses, each pulse has to vary proportional to the necessary fundamental component precisely at the time when this pulse occurs. The frequency of the output waveform needs to be higher than the frequency of the fundamental component. By varying the width of each pulse, the inverter is able to produce different levels of output voltage for the corresponding pulse event [5].

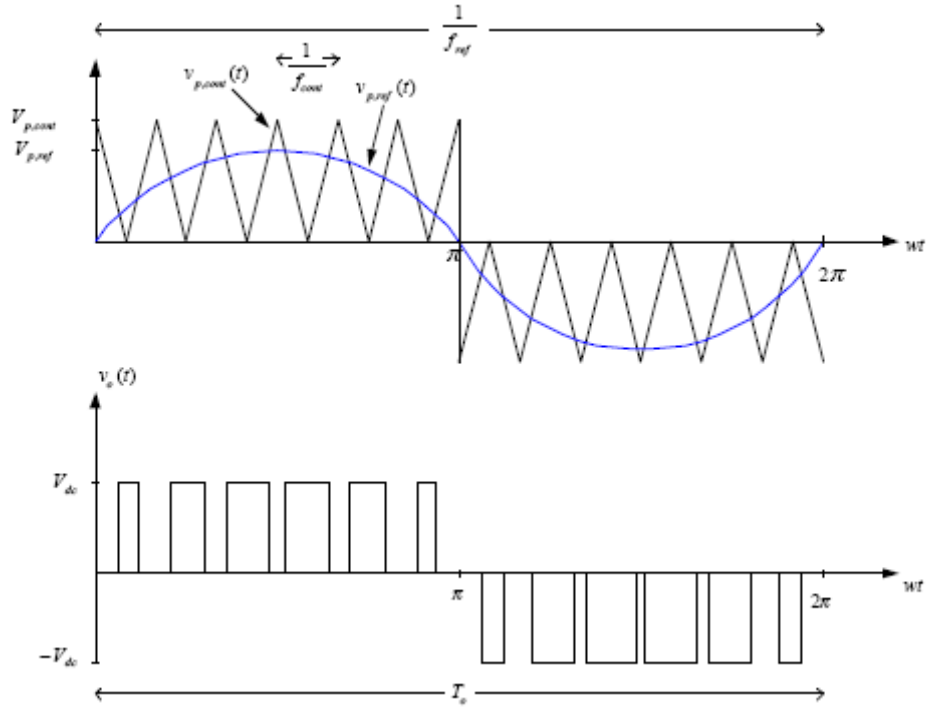


Figure 2.10: SPWM and Inverter Output Voltage.

CHAPTER 3

METHODOLOGY

3.1 Background

This chapter explains about hardware design for the inverter including PIC microcontroller circuit, H-bridge Inverter circuit and MOSFET driver circuit. This chapter also explains the calculation involve in designing the hardware.

Before looking at the detail of all the methods below, it is best to begin with brief review the correlation of all methods. The Figure 3.1 below show the correlation of all methods in this project.

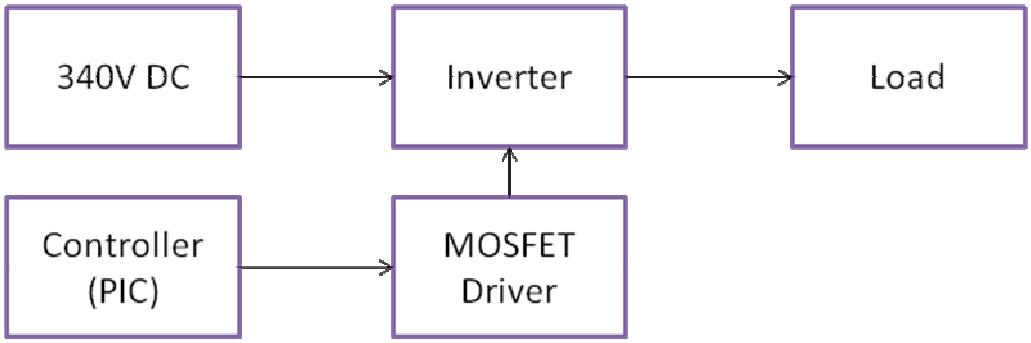


Figure 3.1: System design of Inverter system

3.2 Overall System Design

Design Specifications

Input Voltage	:	340 V_{DC}
Output Voltage	:	Single-phase 240V_{AC} RMS
Output Frequency	:	50Hz ± 0.1Hz
Output Power Range	:	>500Watts
Efficiency	:	> 90%
Switching Frequency	:	50 Hz, 25% Duty cycle
PIC Controls	:	PIC 16F877

There are 4 main circuit in this inverter design, the first is the supply, second is the microcontroller, third is the MOSFET driver and the forth is the inverter. For the supply circuit, 240Vrms AC voltage is step down, rectify and regulate to get 15V and 5V DC.

The second circuit is microcontroller circuit. The PIC 16F877 is used to generate PWM pulses. For this system design, PWM technique is used to control the switching pulses that used to drive MOSFET.

The third circuit for this inverter design consist MOSFET driver, a driver that used to drive MOSFET. Based on MOSFET datasheet, the minimum voltage used to fully turn on MOSFET is 10V. So, the microcontroller cannot connect directly to the MOSFET because it only produces 5V output and it doesn't have electrical isolation between the upper control pulses and the upper gate of the full-bridge inverter circuit.

The forth circuit design is an inverter circuit. Inverter is a circuit that convert DC source to AC source. For this design, the method used to generate AC is using Full-

bridge inverter configuration. The DC source used is a 340V and the output waveform produce the switching scheme is a modified square wave.

3.3 Hardware Design

The hardware design is divided into 4 parts. The power supply design, PIC microcontroller design, MOSFET driver design and Inverter design.

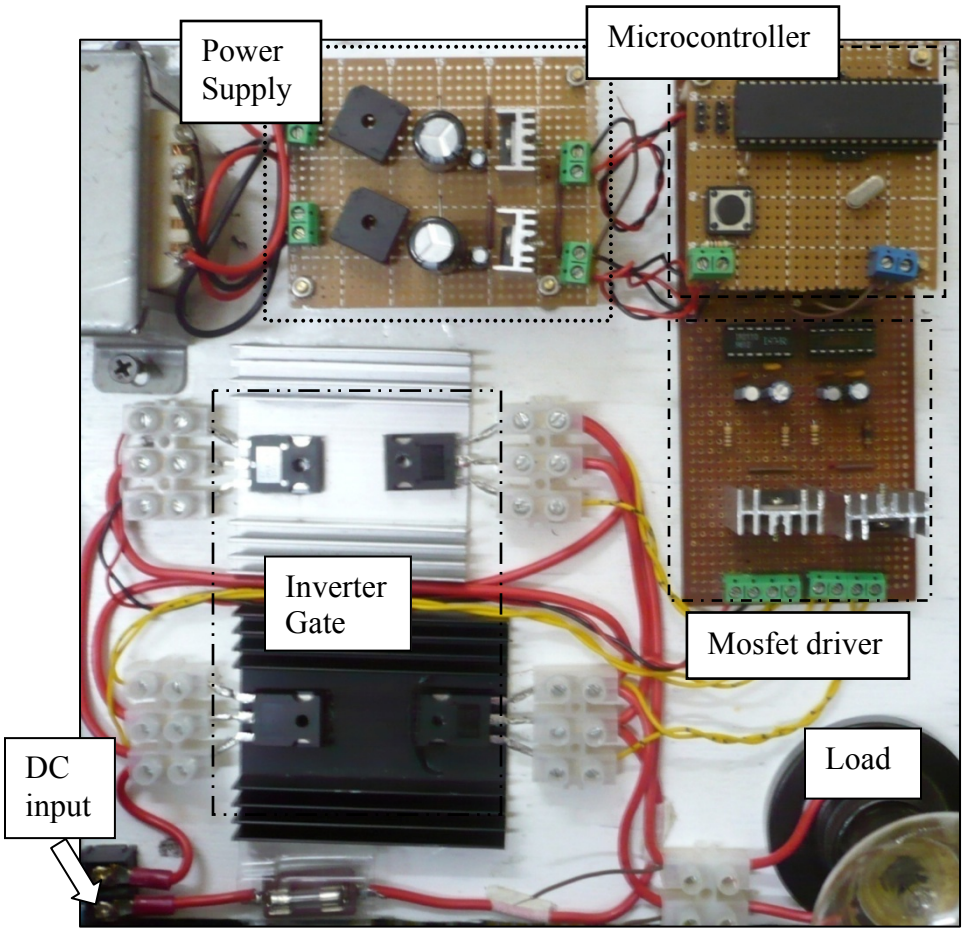


Figure 3.2: The full picture of hardware

3.3.1 Power Supply Design

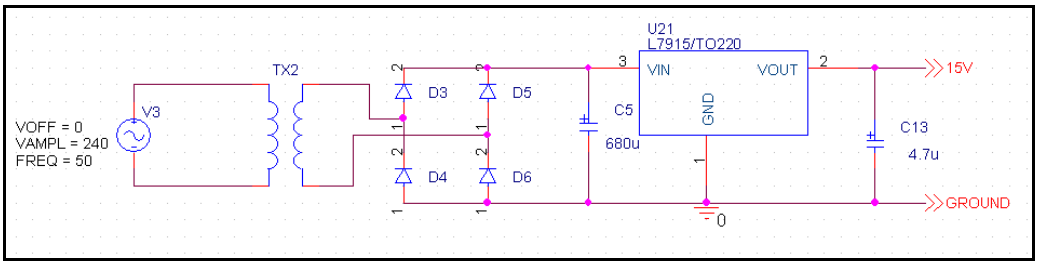


Figure 3.3: Power supply circuit

The power supply is developed by using full bridge rectifier and regulator to convert AC power supply to DC. This power supply is used as a replacement of battery that been used as a supply in UPS. This supply produces two voltages at the output, one is 5V and the other is 15V. The voltage is step down by power transformer from 240Vrms socket supply to 20Vrms and 12Vrms. The step down AC voltage been rectified by bridge rectifier and then voltage regulator LM7805 and LM7815 been used to regulate and stabilize the voltage at the output of the power supply. The 5V voltage is used to supply control circuit that contain PIC microcontroller and the 15V voltage is used to supply MOSFET driver circuit. The figure of power supply circuit is shown in Figure 3.3. Figure 3.4 is the power supply designed.

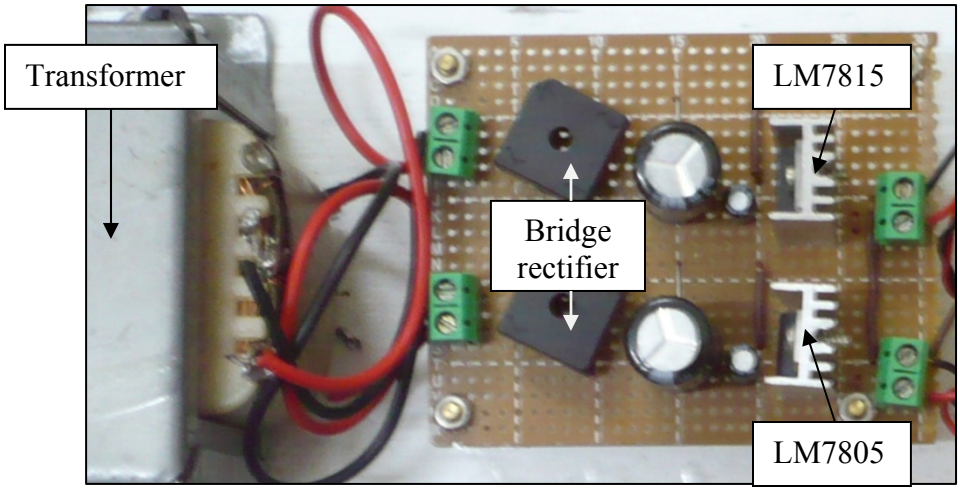


Figure 3.4: Picture of power supply designed

3.3.2 Controller Design

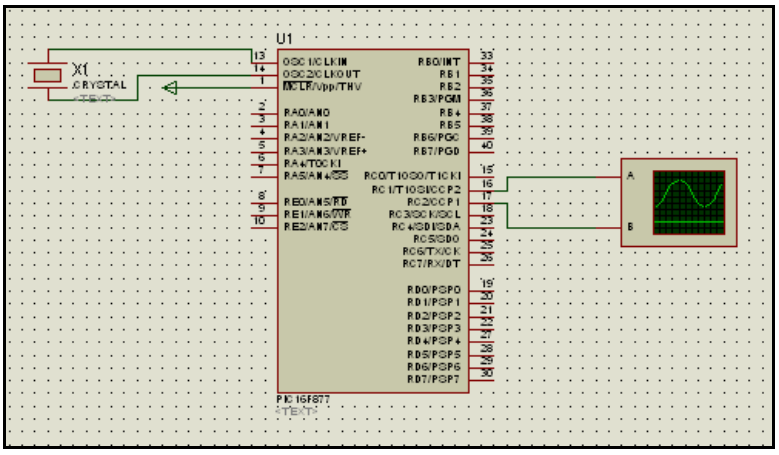


Figure 3.5: Microcontroller circuit

The microcontroller that used in designing the switching controller is 16F877 and the crystal used is 20MHz. This PIC is chosen because it can generate high switching pulses and easy to get in the market. The high frequency crystal is used so it can support high switching pulses that can be used in further improvement of the inverter. The output pin used in this design is pin 16 and pin 17. Figure 3.6 below is the picture of controller designed.

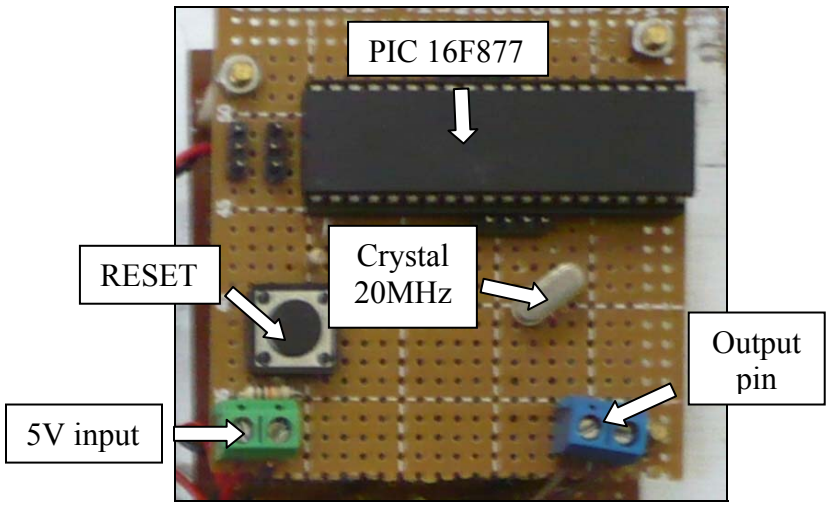


Figure 3.6: Picture of controller designed

The programming used to program PIC is using C and the compiler is PCW C compiler. The program for controlling the pulse is very short and just about half page. It is short because the project is open loop and the output is fixed, so the microcontroller does not have external input to be fed on. The other factor is the switching technique used for this project. The switching technique used for this project is just normal PWM and not SPWM (sine PWM). For the normal PWM, the programming is just about controlling period and ON time (t_{on}).

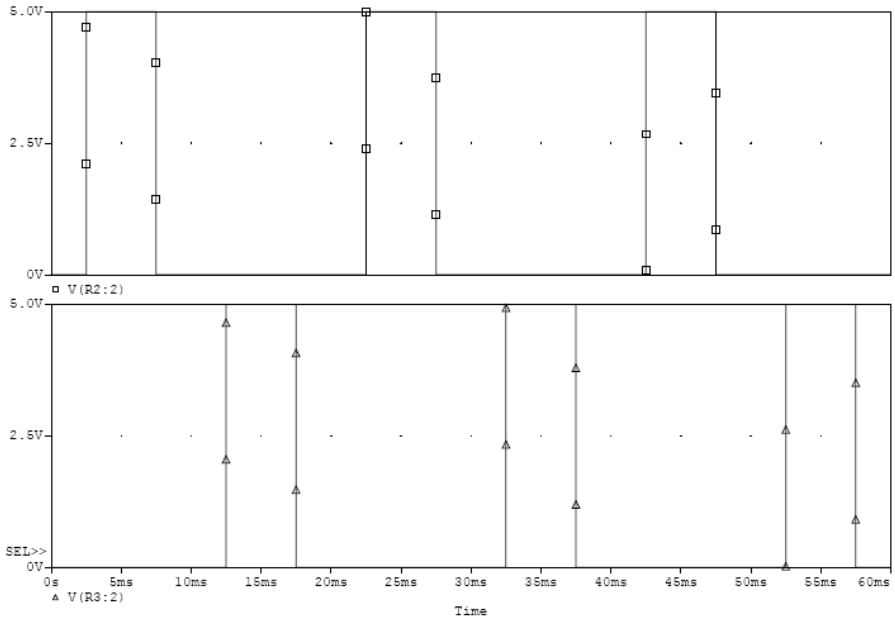


Figure 3.7: Desired output pulses

Figure 3.7 is the desired output pulses. The program is made based on pulses on Figure 3.6. For the pulse of PIN_C1 (the upper pulse on Figure 3.6), the time delay is 2.5 ms and for pulse of PIN_C2 (the bottom pulse on Figure 3.6), the time delay is 12.5 ms. The period of both pulse is 20 ms, so the frequency generated is 50Hz. The pulse width of both pulses is 5 ms because the desired Duty cycle is 25%. The duty cycle can be calculated based on equation 3.1 below:

$$Duty\ Cycle, \% = \frac{t_{on}}{Period} \times 100 \qquad (3.1)$$

3.3.3 Driver Design

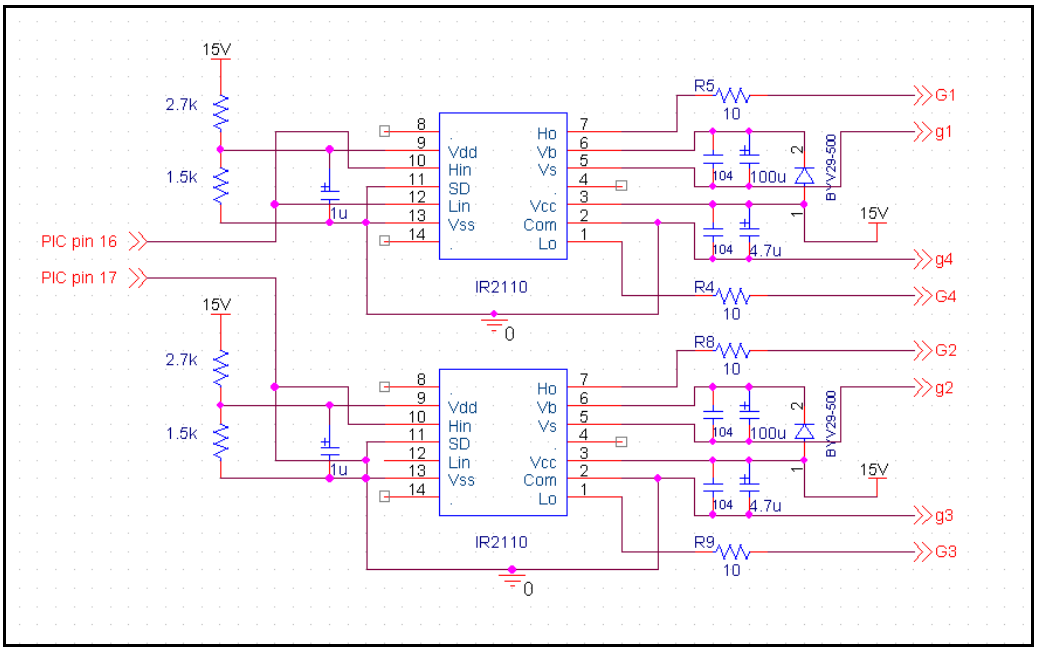


Figure 3.8: IR2110 MOSFET driver circuit

The IR2110 MOSFET gate driver chips play two vital roles in creating drive pulses suitable for operation of a full-bridge inverter circuit. First of all, the IR2110's amplify the 5-volt logic signals output by the microcontroller to obtain a 15 volt signal necessary to fully turn on the gate of the full-bridge circuit. A gate drive pulse of less than 10 volts could result in excessive heating which occurs when the MOSFET is driven are operating in the linear mode of operation, which by the physical MOSFET construction, happens to be the most resistive regions of operation.

The other role played by the IR2110 chips is to provide electrical isolation between the upper control pulses and the upper gate of the full-bridge inverter circuit. Electrical isolation is extremely important in biasing the upper full-bridge gate with the appropriate drive signal voltages. Without proper electrical isolation, the upper gate would be considered "floating". In other words, the upper full-bridge MOSFETs would

have a gate-to-source voltage ranging from 0 VDC to 340 VDC because they are not directly referenced to ground potential.

The IR2110 gate driver chips provide electrical isolation by inserting a capacitor and diode, also known as a "bootstrap supply", are shown in Figure 3.9 below. When Vs is pulled down to ground (either through the low side FET or the load, depending on the circuit configuration), the bootstrap capacitor (Cbs) charges through the bootstrap diode (Dbs) from the 15 Vcc supply. This provides a supply to Vbs.

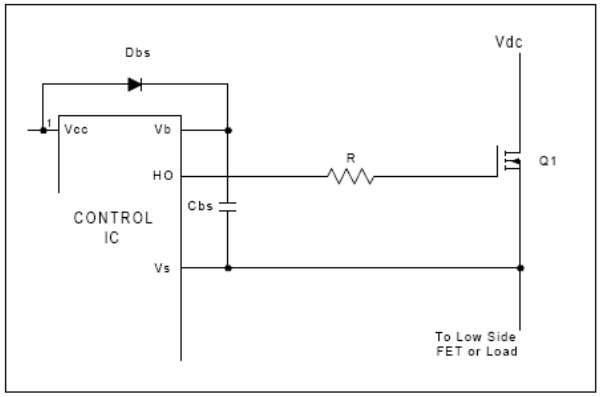


Figure 3.9: Bootstrap diode/capacitor circuit used with IR 2110 control IC's

3.3.3.1 Calculating the Bootstrap Capacitor Value

The following equation gives the minimum charge which needs to be supplied by the capacitor:

$$Q_{bs} = 2Q_g + \frac{I_{qbs(max)}}{f} + Q + \frac{I_{cbs(leak)}}{f} \qquad (3.2)$$

Q_g = Gate charge of high side FET (refer to IRFP450 datasheet)

f = frequency of operation

$I_{cbs(leak)}$ = Bootstrap capacitor leakage current (neglected if using ceramic capacitor)

Q_{ls} = level shift charge required per cycle = 5nC (500V/600V IC's) or 20nC (1200V IC's)

$$Q_{bs} = 2(75n) + \frac{230u}{50} + 5n + \frac{0}{50}$$
$$= 4.755uC$$

The bootstrap capacitor must be able to supply the charge given by equation 3.2 and retain its full voltage. Otherwise, there will be a significant amount of ripple on the Vbs voltage which could cause the Ho output to stop functioning. Therefore, the charge in the Cbs capacitor must be a minimum of twice the value given by equation 3.2. The minimum capacitor value can be calculated from the equation 3.3 below:

$$C \geq \frac{2[Q_{bs}]}{V_{cc} - V_f - V_{LS} - V_{min}} \qquad (3.3)$$

Where:

V_f = Forward voltage drop across the bootstrap diode (refer to BYV29-500 datasheet)

V_{LS} = Voltage drop across the low side FET (V_{SD} in IRFP450 datasheet)

V_{Min} = Minimum voltage between V_B and V_S (minimum V_{BSUV-} in IR2110 datasheet)

$$C \geq \frac{2[4.755u]}{15 - 1 - 1.4 - 7}$$

≥ 1.698uF

The C_{bs} Capacitor value obtained from the above equation above is the absolute minimum required, however due to the nature of the bootstrap circuit operation, a low value capacitor can lead to overcharging, which could in turn damage the IC. Therefore to minimize the risk of overcharging and further reduce ripple on the V_{bs} voltage the C_{bs} value obtained from the above equation should be should be multiplied by a factor of 15 (rule of thumb).

$$C_{new} \geq 1.698uF \times 15$$
$$\geq 25.47uF$$
$$\geq 47uF \text{ (nearest available value)}$$

3.3.3.2 Selecting the Bootstrap Diode

The bootstrap diode (D_{bs}) needs to be able to block the full power rail voltage, which is seen when the high side device is switched on. It must be a fast recovery device to minimize the amount of charge fed back from the bootstrap capacitor into the V_{cc} supply, and similarly the high temperature reverse leakage current would be important if the capacitor has to store charge for long periods of time.

Therefore:

Diode Characteristics

V_{RRM} = Power rail voltage

$\geq$ 400 V

Chosen diode (BYV29-500); V_{RRM} = 500 V

Maximum t_{rr} = 100 ns

$\leq$ 100ns

Chosen diode (BYV29-500); $t_{rr} \leq$ 60ns

$I_F = Q_{bs}$ x f

= 4.755uC × 50Hz

= 0.238 mA

Chosen diode (BYV29-500); I_F = 9A

3.3.3.3 IR2110 Circuit Layout Considerations

For the layout of IR2110 circuit, the bootstrap capacitor is placed closed to the pins of the IC (as shown in Figure 3.10). At least one low ESR capacitor should be used to provide good local decoupling. If an aluminium electrolytic capacitor is used for the bootstap capacitor, a separate ceramic capacitor need to be placed close to the IC. If the bootstap capacitor is a ceramic or tantalum type, the capacitor alone should be sufficient as the local decoupling.

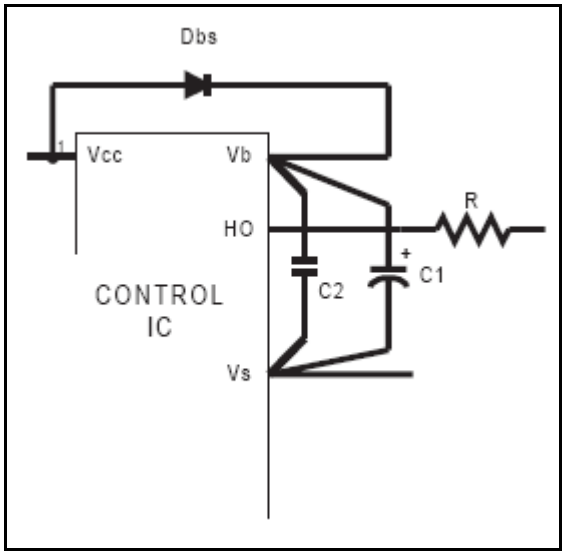


Figure 3.10: Recommended layout of the Bootstrap Components

3.3.4 Inverter Design

There are 3 main type of inverter in the market today. The most simple and cheapest type is square wave inverter, the improved version of square wave inverter is a modified square wave inverter, the best and most expensive type is true sine wave inverter. The type chosen for this project is the common type used in the market that is modified square wave inverter.

The full-bridge inverter used for this project is very simple to construct because it only consists 4 switches, as shown in Figure 3.11. The function of the full-bridge inverter is to convert 340 VDC from supply into 240Vrms, 50 Hz. The gate chosen for the full-bridge inverter circuit were the IRFP450's. The IRFP450 MOSFET were chosen because they have appropriate voltage and current ratings ($V_{DS\ max}$ = 500V, $I_{D\ max}$ = 14A).

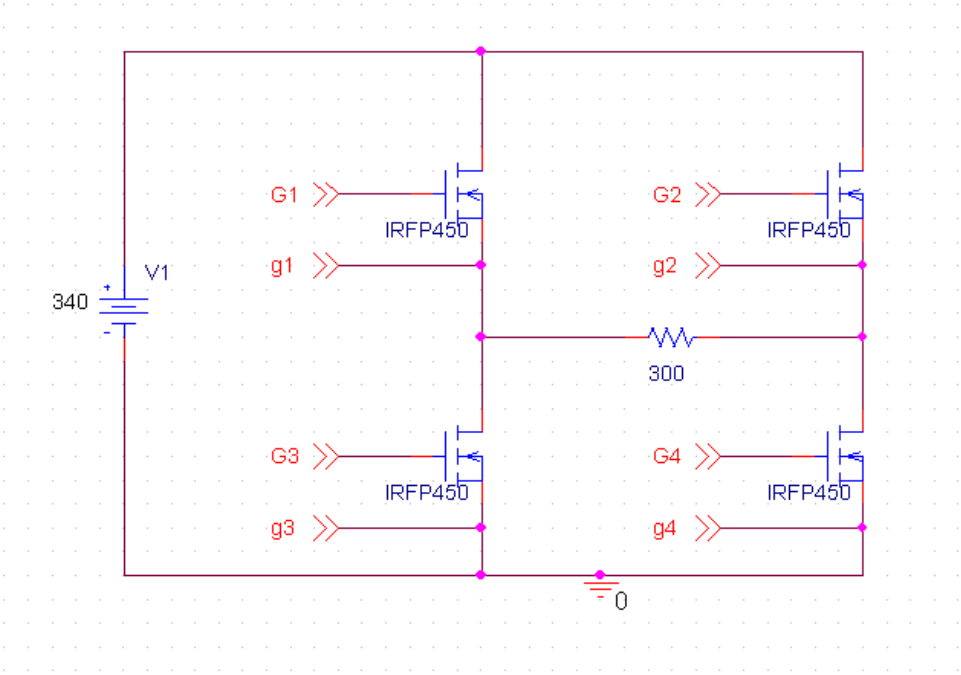


Figure 3.11: Full-bridge inverter

The two PWM pulses produced by the microcontroller circuit are fed into the full-bridge inverter. One signal is sent in parallel to MOSFET gate G1 and G4. The other signal is sent in parallel to MOSFET gate G2 and G3. The signal programmed in the microcontroller will allow for MOSFET gate G1 and G4 to be ON while MOSFET gate G2 and G3 are OFF, and vice versa.

The load chosen for this inverter is resistive load lamp that has resistivity of 300Ω. The power draw from this load when supplied with full voltage (240Vrms) can be calculated by using equation 3.4 below:

$$P = IV \qquad (3.4)$$

$$= \frac{V^2}{R}$$

$$= \frac{240^2}{300}$$

$$= 192W$$

The value above is not the maximum output power for this inverter because the design inverter can sustain up to 14A maximum current in normal heat condition (T_c=25°) and 8.7A in worst heat condition (T_c=100°). So, the maximum power in theory can be calculated by using equation below:

$$P = IV$$

$$= \frac{14A}{\sqrt{2}} \times 240V$$

$$= 2375W$$ (in normal heat condition)

Or

$$= \frac{8.7A}{\sqrt{2}} \times 240V$$

$$= 1476W$$ (in worst heat condition)

The actual value of power that can be sustained by the design inverter may not up to 1476W practically, but it surely can sustain up to 500W.

3.3.4.1 Low-Pass Filter

Low-pass filter can result a great reduction of the inverter output harmonics and hence provide clean power for the load. The filter is inserted after the output of full-bridge inverter in order to eliminate any frequency higher than cutoff frequency. The cutoff frequency can be calculated by using following formula:

$$f_{cutoff} = \frac{1}{2\pi\sqrt{LC}} \qquad (3.5)$$

The switching frequency used in this project is 50 Hz and from the equation above, either L (inductor) or C (capacitor) can be set as a constant. In order to make it easier, capacitor been selected as a constant because the inductor will be custom made in either way. By using 100uF for the capacitor value and using formula in equation 3.5 above, the inductor value been calculated.

$$f_{cutoff} = \frac{1}{2\pi\sqrt{LC}}$$

$$L = \left(\frac{1}{2\pi \times f_{cutoff} \times \sqrt{C}}\right)^2$$

$$= \left(\frac{1}{2\pi \times 50 \times \sqrt{100u}}\right)^2$$

$$= 101.3\ mH$$

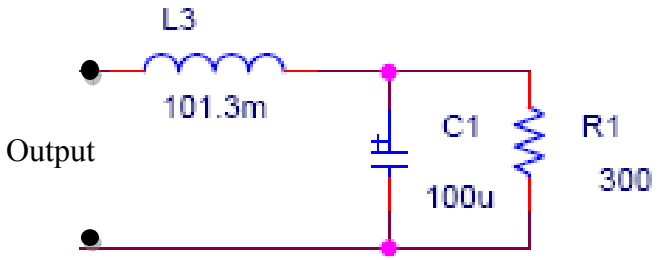


Figure 3.12: L-C low-pass filter schematic

The Figure 3.12 shown is the configuration of L-C filter. The capacitor is placed parallel with load and the inductor is placed series with capacitor and load.

CHAPTER 4

RESULT AND ANALYSIS

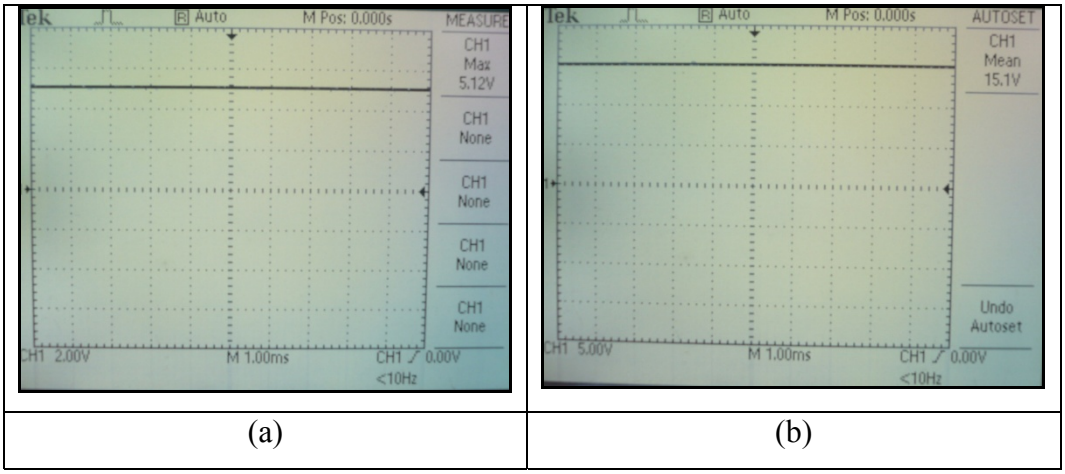
4.1 Introduction

This chapter will show the result and analysis of the Inverter. The comparison between hardware result and simulation by using Orcad Pspice 9.1 will be analyzed. The measurement of hardware output is using oscilloscope. The analysis is divided into 4 parts:

i. Power supply output voltages
ii. Microcontroller output pulses
iii. MOSFET driver output pulses
iv. Analysis of Inverter output

4.2 Power Supply Circuit Output Voltages

The analysis of supply voltage is important to ensure the voltage is not exceeding the required value. Electronic component such as PIC just need 5V to operate. If the component is supplied with high voltage, the component will be hot and in some cases it can blow. The other factor need to be considered is voltage ripple. The ripple will bring effect to generated pulses and it will make the output of the inverter not smooth.



(a) (b)

Figure 4.1: Power supply output voltage (a) output1 (b) output2

The Figure 4.1(a) and 4.1(b) is the output of power supply. From the figure we can see that the output is very smooth and the voltage is near to the desired value. The voltage magnitude of the power supply output is show at Table 4.1.

Table 4.1: Supply output versus design constrain

	Design constrain	Supply output
Output 1	5V	5.12V
Output 2	15V	15.1V

4.3 Microcontroller Output Pulses

The PWM pulses needed to drive MOSFETs driver is generated by PIC microcontroller through programming. The output pin is set at pin 16 (C1) and pin 17 (C2) and the pulses have 15 ms delay with each other. The maximum voltage of the output pulses is same as the voltage supplied to the PIC that is in 5V voltage range.

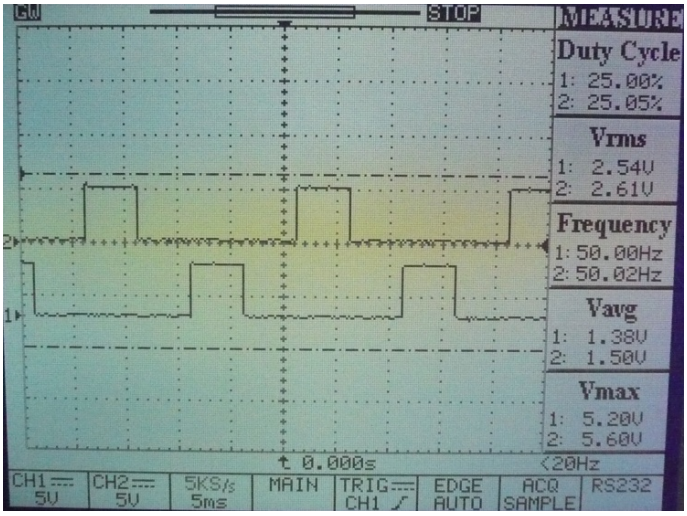


Figure 4.2: Output pulses at pin 16 and pin 17

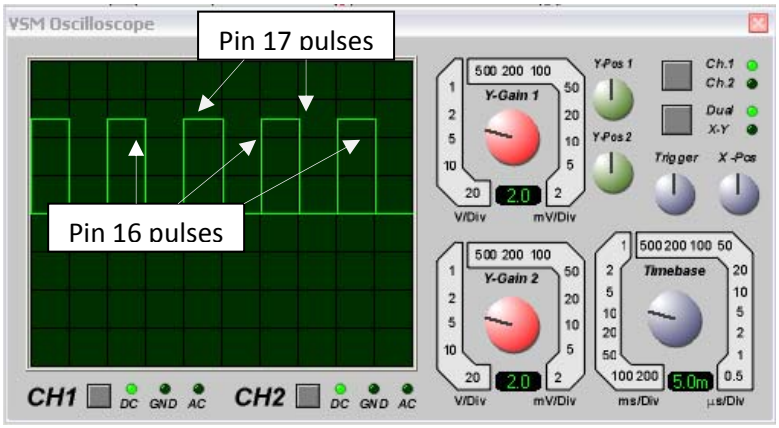


Figure 4.3: Simulation output pulses at both pin by using ISIS

From the observation at oscilloscope output, the ON pulse width and OFF pulse width of the hardware and simulation is similar. The ON pulse width is 5 ms, the OFF pulse width is 15 ms and the frequency of the pulses is 50 Hz. The output of PIC is same as the desired output and can be used to drive MOSFETs driver. The comparisons between designs constrain and microcontroller output can be seen at Table 4.2.

Table 4.2: Comparisons between designs constrain and microcontroller output

	Design constrain	Pin 16 output	Pin 17 output
Vmax	5V	5.2V	5.6V
Frequency	50 Hz	50 Hz	50.02 Hz
Duty Cycle	25%	25%	25.05%

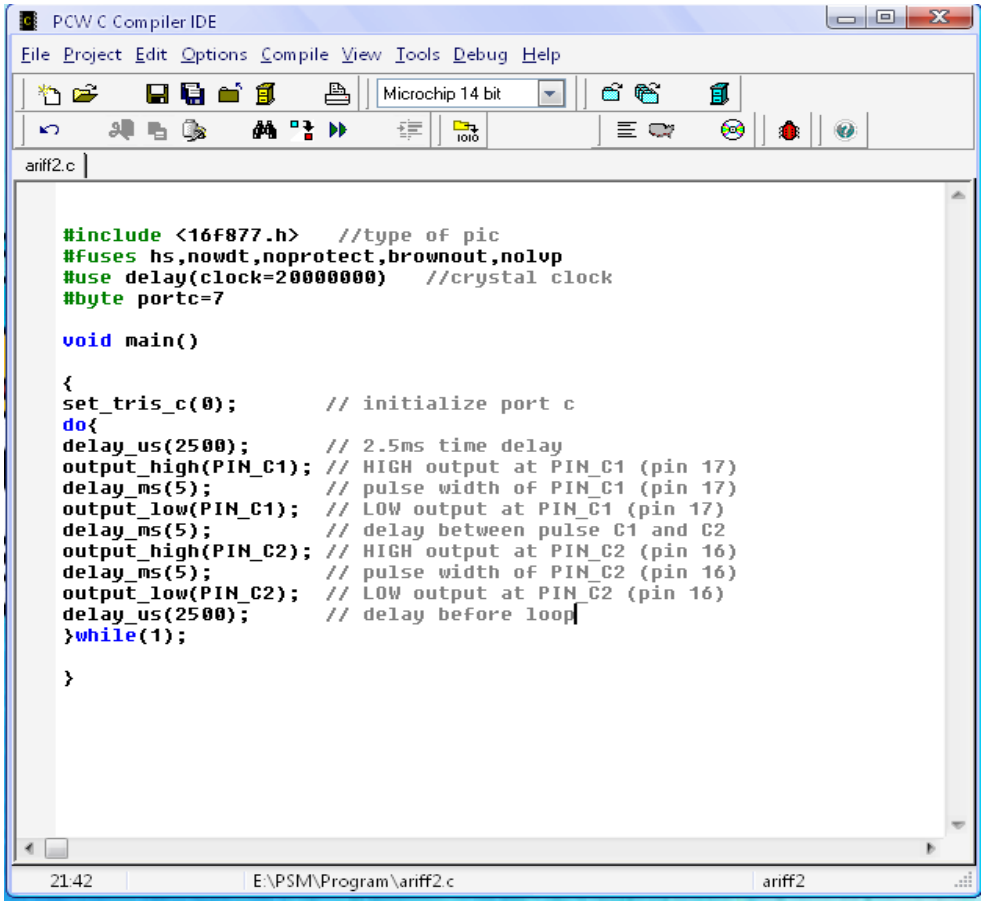


Figure 4.4: Program used to generated pulses

4.4 MOSFET Driver Output Pulses

The minimum voltage need to fully turn on MOSFET is 10V, so the drivers need to be supply with voltage larger than 10 V. For this project, the voltage supplied to the V_{cc} input of IR2110 is 15V. The IR2110 will receive pulses from PIC and then convert it to the voltage based on V_{cc} input (in this case 15V). The output of IR2110 is shown at Figure 4.5.

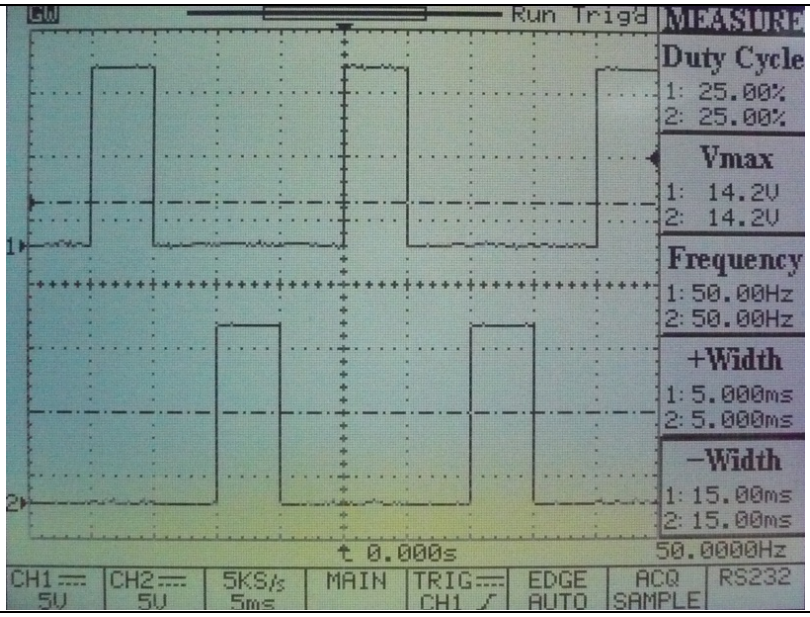


Figure 4.5: Ho pin output pulses of both drivers.

Figure 4.5 shows the result from Ho pin of IR2110. The result of both drivers is same except there is 5ms delay between pulse of driver1 and driver2. The V_{max} on the oscilloscope shows a few drops in voltage because there is a voltage drop across bootstrap diode. The voltage magnitude at Lo pin of both IR2110 is near to V_{cc} value because the voltage output of Lo pin is using the voltage supplied to V_{cc}. The result is as desired value and the voltage magnitude (14.2V) is enough to fully turn on MOSFET.

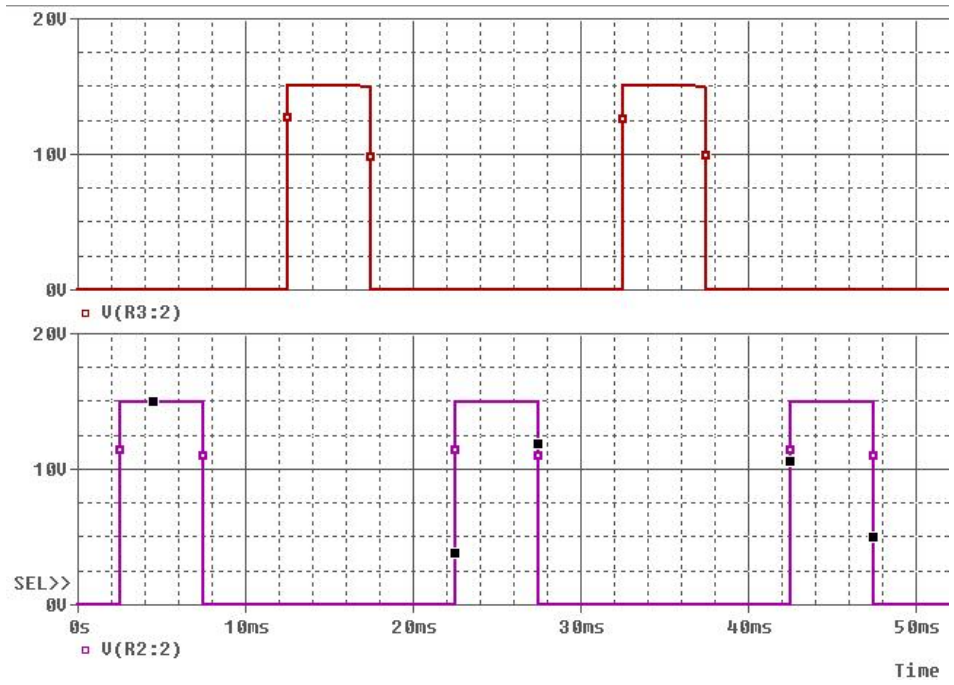


Figure 4.6: Orcad PSpice simulation output pulses

The result from PSpice simulation is shown in Figure 4.6. The pulses from simulation can be considered ideal because the simulation not considering other disturbance factor such as noise, heat and loss. The voltage magnitude for PSpice simulation is different with the real output value because the pulses is generated by using VPULSE and the gate for the full-bridge is using ideal switch. The table that listed all driver output is shown below:

Table 4.3: IR2110 MOSFET driver output

	Design constrain	Ho Driver1	Ho Driver2	Lo Driver1	Lo Driver2
V_{max}	>10V	14.2V	14.2V	15.1V	15.1V
Frequency	50 Hz	50 Hz	50 Hz	50 Hz	50 Hz
Duty Cycle	25%	25%	25 %	25 %	25 %

4.5 Analysis of Inverter Output

This part will show the result and analysis of the Inverter. Before fabricating the hardware, the analysis is done using Orcad Pspice 9.1 After the hardware is finalized, the inverter circuit will be analyzed using oscilloscope.

4.5.1 Analysis of Voltage, Current, and Power Relation with Load

For this analysis, the load resistance value for the inverter is changed. The minimum resistance value set is 50 Ω, with 50 increments and the maximum value is 300 Ω. The total reading is 6 and the parameters taken are voltage, current and power. The result for the parameter is on Figure 4.7, 4.8 and 4.9.

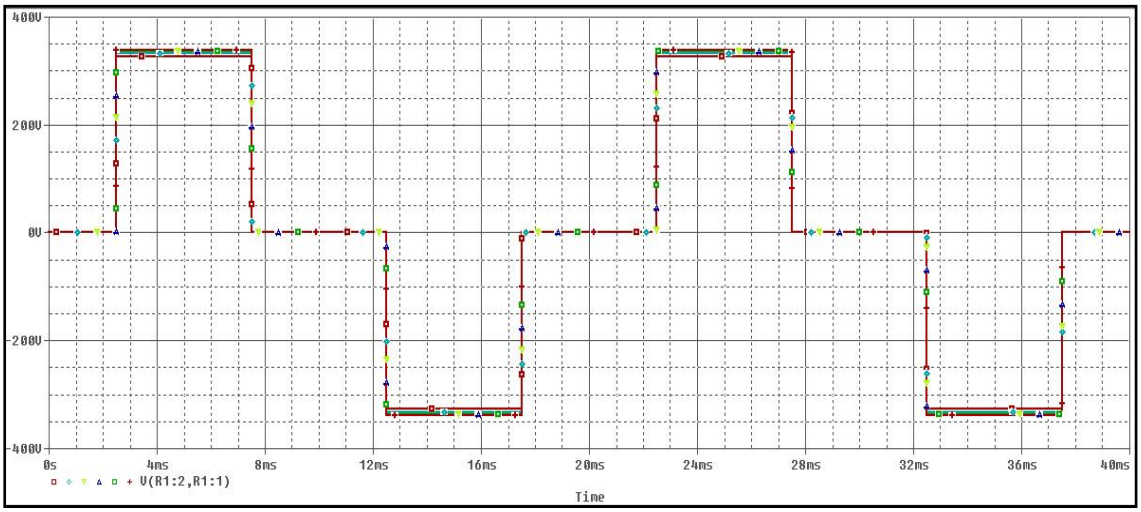


Figure 4.7: The output voltage of different load

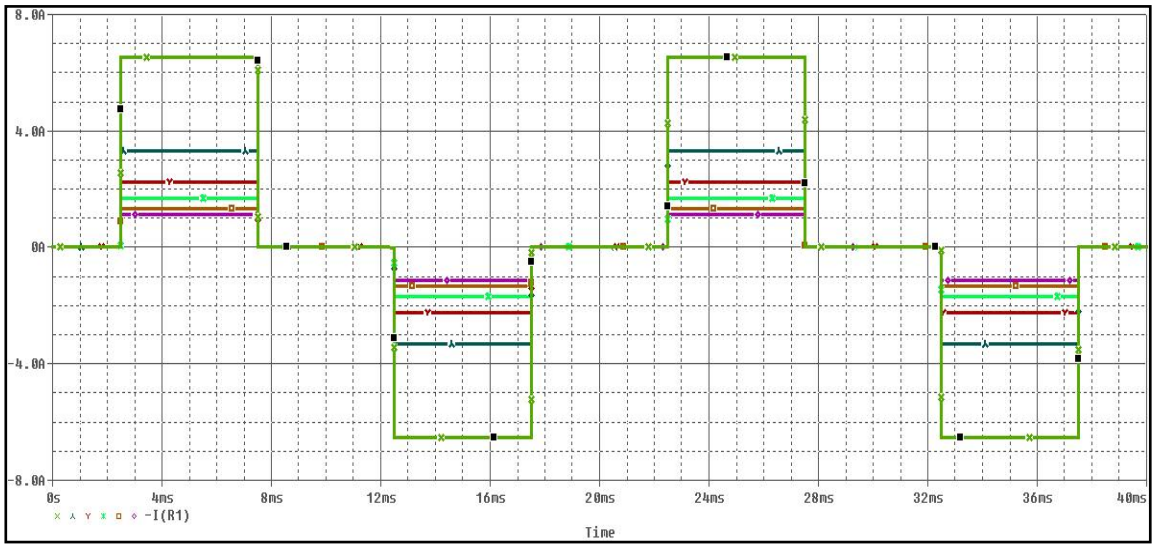


Figure 4.8: The output current with different load

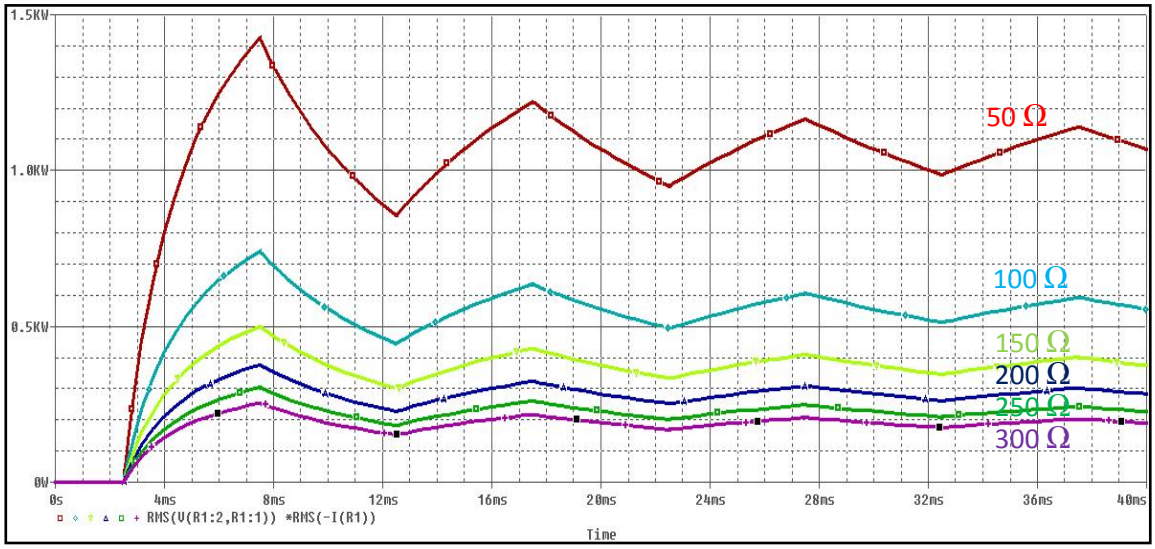


Figure 4.9: The output power with different load

All the result for Figure 4.7, 4.8 and 4.9 is compress into Table 4.4. The Table 4.4 below lists the values of voltage, current and power when the load is changed.

Table 4.4: Voltage, current and power value based on the load resistance

Load (Ω)	50	100	150	200	250	300
V_{peak} (V)	326.92	333.33	335.53	336.63	337.3	337.75
V_{RMS} (V)	231.27	235.8	237.36	238.14	238.61	238.93
I_{peak} (A)	6.54	3.33	2.24	1.68	1.35	1.13
I_{RMS} (A)	4.62	2.36	1.58	1.19	0.95	0.8
Power (W)	1067.8	555.03	374.9	283.04	227.33	189.94

From Table 4.4, the changes in load will affect the value of voltage, current and power. The lower value of resistance, the higher current will flow through the load and the higher power at the load. This is because the value of voltage is same. The relation between current, resistance and power can be seen on equation below:

$$P = IV \qquad (4.1)$$

$$= I(IR)$$

$$P = I^2R \qquad (4.2)$$

4.5.2 Analysis of Total Harmonic Distortion (THD)

For this analysis, the THD for three type of inverter is compared. The first type is modified square wave inverter used for this project and the second one is modified square wave inverter with filter. The THD of the current is computed using truncated Fourier series and it's based on frequency spectrum. The equation used for the calculation is as below:

$$THD_I = \frac{\sqrt{\sum_{n=2}^{\infty}(I_{n,rms})^2}}{I_{Irms}} \qquad (4.3)$$

The figure of frequency spectrum for all three type of inverter is on figure below:

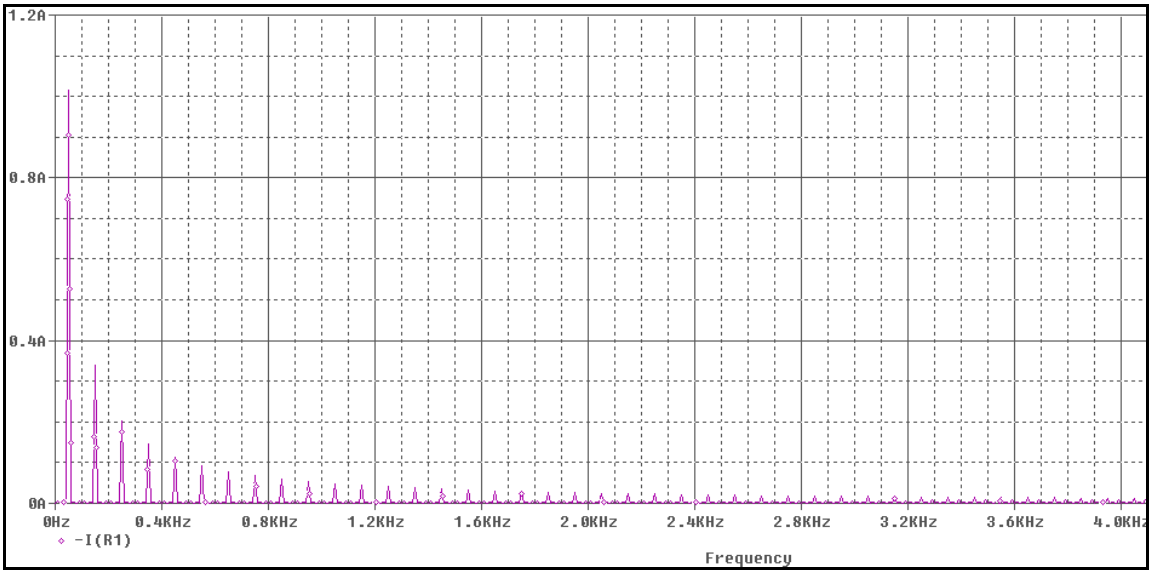


Figure 4.10: Frequency spectrum of modified square wave inverter (without filter)

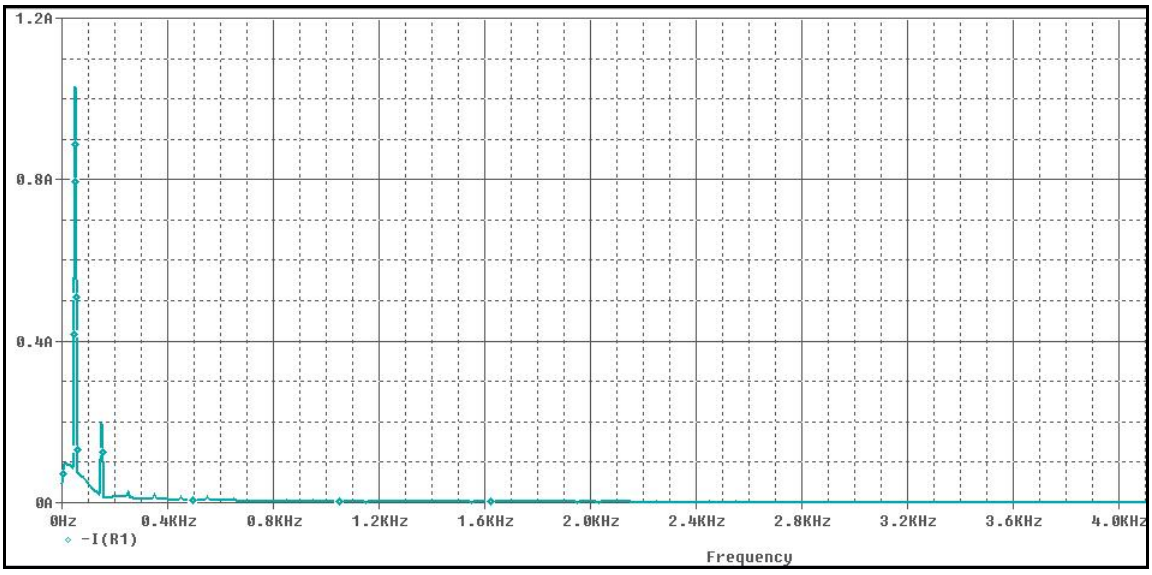


Figure 4.11: Frequency spectrum of modified square wave inverter with filter

The configuration of all three inverter is defined on table below:

Table 4.5: Inverters configuration

	Modified square wave	Modified square wave with filter
Vin (DC)	340 V	340 V
f	50 Hz	50 Hz
Filter capacitor value	-	100 uF
Filter inductor value	-	101.3 mH

The value from the frequency spectrum Figure 4.11 is inserted into Table 4.6 and the value from the frequency spectrum Figure 4.12 is inserted into Table 4.7. All value inside the table is calculated using Microsoft Office Excel.

Table 4.6: Modified square wave inverter data from frequency spectrum

n	Frequency	In	√2	In /√2	(In /√2)²
1	50	1.0146	1.414214	0.717431	
3	150	0.338201	1.414214	0.239144	0.05719
5	250	0.202926	1.414214	0.14349	0.020589
7	350	0.144953	1.414214	0.102497	0.010506
9	450	0.112747	1.414214	0.079724	0.006356
11	550	0.092253	1.414214	0.065233	0.004255
13	650	0.078066	1.414214	0.055201	0.003047
15	750	0.067663	1.414214	0.047845	0.002289
17	850	0.059709	1.414214	0.042221	0.001783
19	950	0.05343	1.414214	0.037781	0.001427
21	1050	0.048347	1.414214	0.034186	0.001169
				Total	0.108611
√ Total	0.32956236				
THD_I	0.45936483				
$\%THD_I$	45.936483				

Table 4.7: Modified square wave inverter with filter data from frequency spectrum

n	Frequency	In	√2	In /√2	(In /√2)²
1	50	1.0314	1.414214	0.72931	
3	150	0.195183	1.414214	0.138015	0.019048
5	250	0.027884	1.414214	0.019717	0.000389
7	350	0.020675	1.414214	0.014619	0.000214
9	450	0.013975	1.414214	0.009882	9.77E-05
				Total	0.019748
√ Total	0.14052878				
THD_I	0.19268733				
$\%THD_I$	19.2687327				

From the result of Table 4.6 and 4.7, the THD of an inverter can be reduced by using low past filter. By comparing the value of THD from both tables, we can see that there is about 26% reduction in THD if low pass filter been added.

4.5.3 Hardware Output

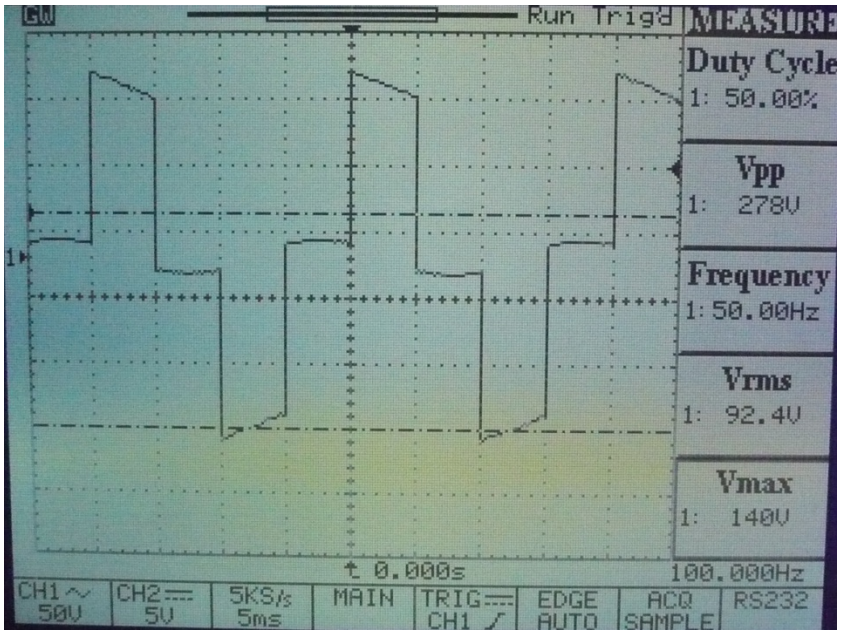


Figure 4.12: Inverter output waveform from oscilloscope

Figure 4.12 shown is the output of the full bridge inverter as constructed on hardware circuit. The full-bridge inverter is supposed to produce a 340 V_{AC} peak voltage but because the DC voltage supplied to inverter is 140 V (by connecting two power supply in series), the highest peak voltage can be generated is same as supplied DC voltage (140 V). The inverter converted the 140 V_{DC} input to 278 V_{pp} or 92.4 V_{RMS}. The voltage supplied is sufficient to light the bulb as seen in Figure 4.13.

Figure 4.13: Hardware output result

The intensity of the light bulb can be increase if the input DC voltage is increase. The required value is 340 V_{DC} (to generate 240 V_{RMS}) and the value can be obtained by using DC-DC converter or High Voltage DC (HVDC) generator.

CHAPTER 5

CONCLUSION AND RECOMMENDATION

5.1 Conclusion

The function of inverter is to create an ac voltage by using dc voltage and in UPS system, the voltage source is batteries. In this project, an inverter being develop to generate $240V_{RMS}$, 50Hz AC voltage supply by using full-bridge configuration. The inverter operates at 50 Hz using MOSFETs and the modified square wave output pattern is obtained by setting the duty cycle of the pulses. The gate pulses are obtained from microcontroller running at 20 MHz.

5.2 Recommendation

Here is some enhancement of this project that should add in future:

i. Enhance this project with the close loop system. In general, close loop systems are superior to open loop system. In the close loop system, it consist sensor or measurement device which is used to detect the value of output during the operation and compared with desired output. Through programming, the error can be self corrected and the desired output will be more accurate.

ii. Change the switching technique by using SPWM. SPWM technique with filter at the output produced low Total Harmonic Distortion (THD) and true sine wave output. The advantage of true sine wave is it is compatible with all AC equipment including the sensitive equipment like laser printer that needed true sine wave supply to operate.

5.3 Costing and Commercialization

5.3.1 Costing

This part explains about the costing of this project. The total project cost for all components is estimated to be RM 230.40. The highest cost is reflected in the price in the price of power electronic device such as MOSFET (IRFP 450), MOSFET driver (IR2110) and high rating fast recovery diode (BYV29-500). Even though the price of these components is expensive, it is still a necessary item and the less expensive substitutes are nonexistent. The component chosen based on the performance of the component, means that the chosen component rating is above designed value. The table of component cost is on Table 5.1.

Table 5.1: The cost of component

Device	Manufacture	Qty	Unit	Unit Cost (RM)	Extended Cost (RM)
IRFP 450	International Rectifier	4		6.50	26.00
IR2110	International Rectifier	2		18.00	36.00
BYV29-500	Philips	2		20.00	40.00
Capacitor ceramic		4	0.1uF	0.20	0.80
Capacitor 50V		2	1uF	0.20	0.40
Capacitor 50V		4	4.7uF	0.40	1.60
Capacitor 50V		2	680uF	2.00	4.00
Capacitor 50V		2	100uF	0.40	0.80
Resistor		2	1.5kΩ	0.10	0.20
Resistor		2	2.7kΩ	0.10	0.20
Resistor		4	10Ω	0.10	0.40
LM7815	Bay Linear	1		1.50	1.50
LM7805	Bay Linear	1		1.50	1.50
KBPC 610		2		3.00	6.00
Transformer		1	240V -20V	20.00	20.00
Crystal		1	20MHz	5.00	5.00
16F877	Microchip	1		30.00	30.00
touch switch		1		1.50	1.50
Strip board		2		2.00	4.00
Heat sink (small)		4		1.50	6.00
Heat sink (big)		2		8.00	16.00
Plug		1		2.00	2.00
Connector 0384		13		1.50	19.50
Fuse		1	10A	0.30	0.30
3 core cable		1	1m	2.80	2.80
jumper wire		2	1m	0.30	0.60
black red cable		2	1m	0.40	0.80
IC Base		2	14 pin	0.50	1.00
IC Base		1	40 pin	1.00	1.00
IC Base		1	16 pin	0.50	0.50
				TOTAL	RM 230.40

5.3.1 Commercialization

The total project cost is RM 230.40. Even though the price is quite expensive and it does not have DC-DC converter component, the price is still considered reasonable because the power rating for the inverter designed is high (up to 1000W). Usually the price of inverter sold in the market based on power rating and it is about RM 1 per watt. The estimated price of DC-DC converter is about RM 300 and if it been added, the full inverter system price is about RM 550. The price of the full system is considered low because it just about half of market price. The cost can be reduced if the inverter is mass-produced.

Modified square wave inverter designed in this project is suitable for many AC devices and as the plus point, the inverter can be upgraded to Sinusoidal PWM inverter with just changing the program in PIC. The inverter can be more efficient and reliable if the close-loop system is used.

The size of the inverter designed in this project is large but the size can be reduced by using Printed Circuit Board (PCB) instead of using strip board. It will be an advantage when the designed circuit is small but have same capability with original circuit.

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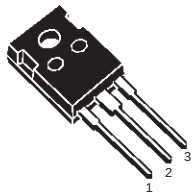
APPENDIX A

IRFP450

N - CHANNEL 500V - 0.33Ω - 14A - TO-247
PowerMESH™ MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
IRFP450	500 V	< 0.4 Ω	14 A

- TYPICAL $R_{DS(on)}$ = 0.33 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- VERY LOW INTRINSIC CAPACITANCES
- GATE CHARGE MINIMIZED



TO-247

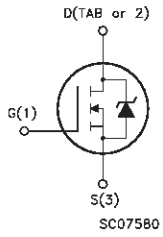
DESCRIPTION

This power MOSFET is designed using the company's consolidated strip layout-based MESH OVERLAY™ process. This technology matches and improves the performances compared with standard parts from various sources.

APPLICATIONS

- HIGH CURRENT SWITCHING
- UNINTERRUPTIBLE POWER SUPPLY (UPS)
- DC/DC COVERTERS FOR TELECOM, INDUSTRIAL, AND LIGHTING EQUIPMENT.

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	500	V
V_{DGR}	Drain- gate Voltage (R_{GS} = 20 kΩ)	500	V
V_{GS}	Gate-source Voltage	± 20	V
I_D	Drain Current (continuous) at T_c = 25 °C	14	A
I_D	Drain Current (continuous) at T_c = 100 °C	8.7	A
I_{DM}(•)	Drain Current (pulsed)	56	A
P_{tot}	Total Dissipation at T_c = 25 °C	190	W
	Derating Factor	1.5	W/°C
dv/dt(1)	Peak Diode Recovery voltage slope	3.5	V/ns
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤14 A, di/dt ≤ 130 A/µs, V_{DD} ≤ $V_{(BR)DSS}$, Tj ≤ T_{JMAX}

THERMAL DATA

$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	0.66	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	30	oC/W
$R_{thc\text{-}sink}$	Thermal Resistance Case-sink	Typ	0.1	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	14	A
E_{AS}	Single Pulse Avalanche Energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 50 V)	800	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA V_{GS} = 0	500			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_c = 125 °C			1 50	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V I_D = 8.4 A		0.33	0.4	Ω
$I_{D(on)}$	On State Drain Current	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$ V_{GS} = 10 V	14			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$ I_D = 8.4 A	9.3	13		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25 V f = 1 MHz V_{GS} = 0		2600 330 40		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 250 V I_D = 7A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 1)		24 14		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 400 V I_D = 14A V_{GS} = 10 V		75 13.5 27		nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 400 V I_D = 14 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 3)		15 25 35		ns ns ns

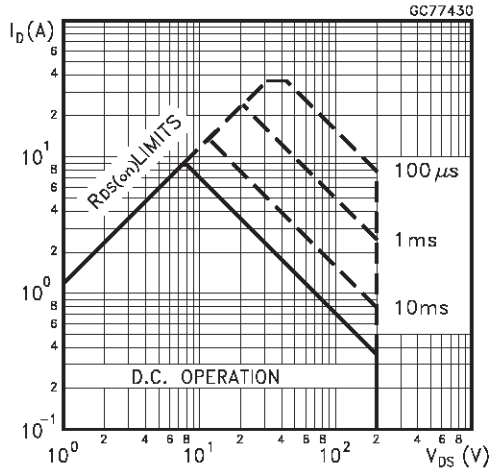
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(•)	Source-drain Current Source-drain Current (pulsed)				14 56	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 14 A V_{GS} = 0			1.4	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 14 A di/dt = 100 A/µs V_{DD} = 100 V T_j = 150 °C (see test circuit, figure 3)		680 9 26		ns µC A

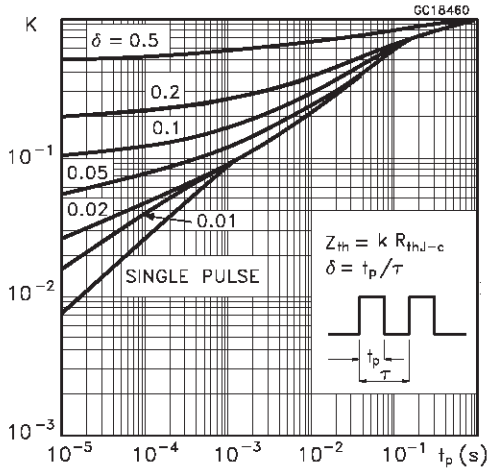
(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

(•) Pulse width limited by safe operating area

Safe Operating Area



Thermal Impedance



APPENDIX B

Data Sheet No. PD60147 rev.U

International
IOR Rectifier

IR2110(-1-2)(S)PbF/IR2113(-1-2)(S)PbF

HIGH AND LOW SIDE DRIVER

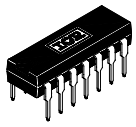
Features

- Floating channel designed for bootstrap operation
  Fully operational to +500V or +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
  Separate logic supply range from 3.3V to 20V
  Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

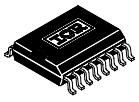
Product Summary

V_{OFFSET}	(IR2110)	500V max.
	(IR2113)	600V max.
I_O+/-		2A / 2A
V_{OUT}		10 - 20V
$t_{on/off}$ (typ.)		120 & 94 ns
Delay Matching	(IR2110)	10 ns max.
	(IR2113)	20ns max.

Packages



14-Lead PDIP
IR2110/IR2113

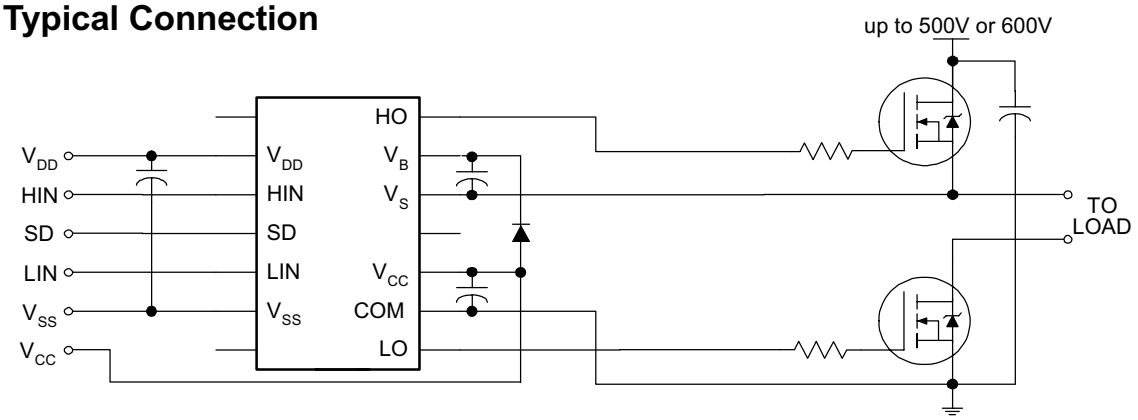


16-Lead SOIC
IR2110S/IR2113S

Description

The IR2110/IR2113 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 or 600 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage	(IR2110)	-0.3	525	V
		(IR2113)	-0.3	625	
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{DD}	Logic supply voltage		-0.3	V_{SS} + 25	
V_{SS}	Logic supply offset voltage		V_{CC} - 25	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN, LIN & SD)		V_{SS} - 0.3	V_{DD} + 0.3	
dV_s/dt	Allowable offset supply voltage transient (figure 2)		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(14 lead DIP)	—	1.6	W
		(16 lead SOIC)	—	1.25	
R_{THJA}	Thermal resistance, junction to ambient	(14 lead DIP)	—	75	°C/W
		(16 lead SOIC)	—	100	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in figures 36 and 37.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply absolute voltage		V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	(IR2110)	Note 1	500	
		(IR2113)	Note 1	600	
V_{HO}	High side floating output voltage		V_S	V_B	
V_{CC}	Low side fixed supply voltage		10	20	
V_{LO}	Low side output voltage		0	Vcc	
V_{DD}	Logic supply voltage		V_{SS} + 3	V_{SS} + 20	
V_{SS}	Logic supply offset voltage		-5 (Note 2)	5	
V_{IN}	Logic input voltage (HIN, LIN & SD)		V_{SS}	V_{DD}	
T_A	Ambient temperature		-40	125	°C

Note 1: Logic operational for V_S of -4 to +500V. Logic state held for V_S of -4V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).
Note 2: When V_{DD} < 5V, the minimum V_{SS} offset is limited to $-V_{DD}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

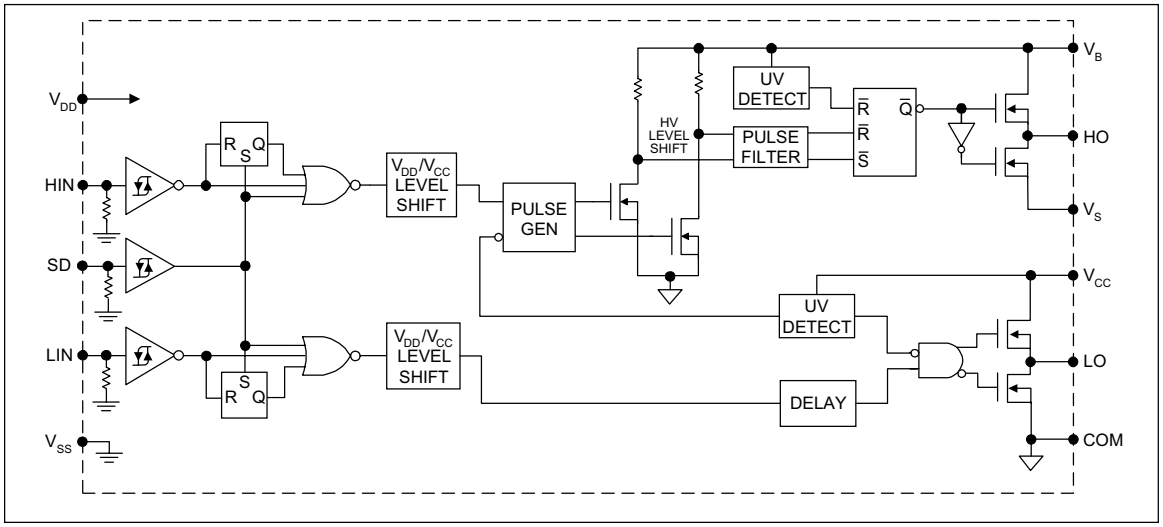
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	7	—	120	150	ns	V_S = 0V
t_{off}	Turn-off propagation delay	8	—	94	125		V_S = 500V/600V
t_{sd}	Shutdown propagation delay	9	—	110	140		V_S = 500V/600V
t_r	Turn-on rise time	10	—	25	35		
t_f	Turn-off fall time	11	—	17	25		
MT	Delay matching, HS & LS turn-on/off (IR2110)	—	—	—	10		
	Delay matching, HS & LS turn-on/off (IR2113)	—	—	—	20		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic “1” input voltage	12	9.5	—	—	V	
V_{IL}	Logic “0” input voltage	13	—	—	6.0		
V_{OH}	High level output voltage, V_{BIAS} - V_O	14	—	—	1.2		I_O = 0A
V_{OL}	Low level output voltage, V_O	15	—	—	0.1		I_O = 0A
I_{LK}	Offset supply leakage current	16	—	—	50	µA	V_B=V_S = 500V/600V
I_{QBS}	Quiescent V_{BS} supply current	17	—	125	230		V_{IN} = 0V or V_{DD}
I_{QCC}	Quiescent V_{CC} supply current	18	—	180	340		V_{IN} = 0V or V_{DD}
I_{QDD}	Quiescent V_{DD} supply current	19	—	15	30		V_{IN} = 0V or V_{DD}
I_{IN+}	Logic “1” input bias current	20	—	20	40		V_{IN} = V_{DD}
I_{IN-}	Logic “0” input bias current	21	—	—	1.0		V_{IN} = 0V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	22	7.5	8.6	9.7	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	23	7.0	8.2	9.4		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	24	7.4	8.5	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	25	7.0	8.2	9.4		
I_{O+}	Output high short circuit pulsed current	26	2.0	2.5	—	A	V_O = 0V, V_{IN} = V_{DD} PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	27	2.0	2.5	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

Functional Block Diagram



Lead Definitions

Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

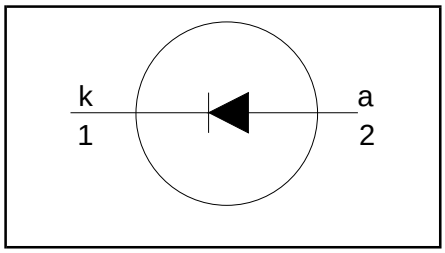
APPENDIX C

Rectifier diodes ultrafast BYV29 series

FEATURES

- Low forward volt drop
- Fast switching
- Soft recovery characteristic
- High thermal cycling performance
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_R = 300 V/ 400 V/ 500 V

$V_F \leq 1.03$ V

$I_{F(AV)} = 9$ A

$t_{rr} \leq 60$ ns

GENERAL DESCRIPTION

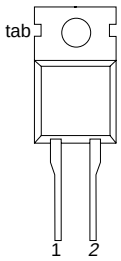
Ultra-fast, epitaxial rectifier diodes intended for use as output rectifiers in high frequency switched mode power supplies.

The BYV29 series is supplied in the conventional leaded SOD59 (TO220AC) package.

PINNING

PIN	DESCRIPTION
1	cathode
2	anode
tab	cathode

SOD59 (TO220AC)



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
		BYV29		**-300**	**-400**	**-500**	
V_{RRM}	Peak repetitive reverse voltage		-	300	400	500	V
V_{RWM}	Crest working reverse voltage		-	300	400	500	V
V_R	Continuous reverse voltage		-	300	400	500	V
$I_{F(AV)}$	Average forward current[1]	square wave; $\delta = 0.5$; $T_{mb} \leq 123$ ˚C	-	9			A
I_{FRM}	Repetitive peak forward current	t = 25 µs; $\delta = 0.5$; $T_{mb} \leq 123$ ˚C	-	18			A
I_{FSM}	Non-repetitive peak forward current.	t = 10 ms	-	100			A
		t = 8.3 ms sinusoidal; with reapplied $V_{RRM(max)}$	-	110			A
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	150			˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.5	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air.	-	60	-	K/W

1 Neglecting switching and reverse current losses.

ELECTRICAL CHARACTERISTICS

T_j = 25 ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_F	Forward voltage	I_F = 8 A; T_j = 150˚C	-	0.90	1.03	V
		I_F = 8 A	-	1.05	1.25	V
		I_F = 20 A	-	1.20	1.40	V
I_R	Reverse current	$V_R = V_{RRM}$	-	2.0	50	µA
		$V_R = V_{RRM}$; T_j = 100 ˚C	-	0.1	0.35	mA
Q_s	Reverse recovery charge	I_F = 2 A to $V_R \geq$ 30 V; dI_F/dt = 20 A/µs	-	40	60	nC
t_{rr}	Reverse recovery time	I_F = 1 A to $V_R \geq$ 30 V; dI_F/dt = 100 A/µs	-	50	60	ns
I_{rrm}	Peak reverse recovery current	I_F = 10 A to $V_R \geq$ 30 V; dI_F/dt = 50 A/µs; T_j = 100˚C	-	4.0	5.5	A
V_{fr}	Forward recovery voltage	I_F = 10 A; dI_F/dt = 10 A/µs	-	2.5	-	V

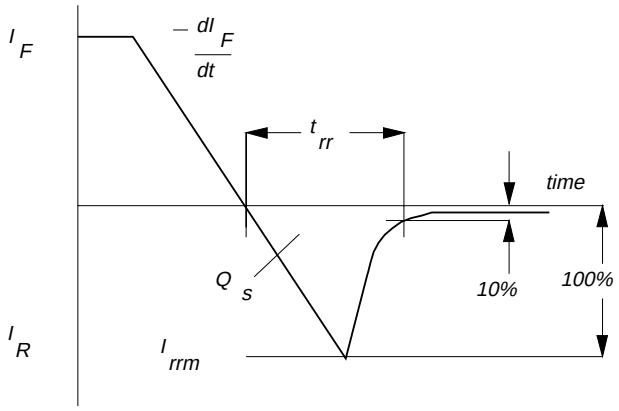


Fig.1. Definition of t_{rr}, Q_s and I_{rrm}

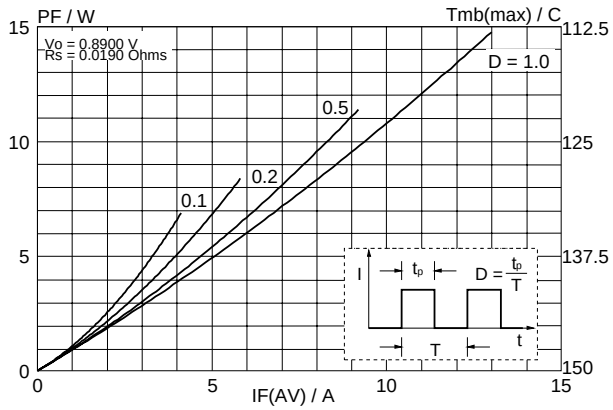


Fig.3. Maximum forward dissipation $P_F = f(I_{F(AV)})$; square wave where $I_{F(AV)} = I_{F(RMS)} \times \sqrt{D}$.

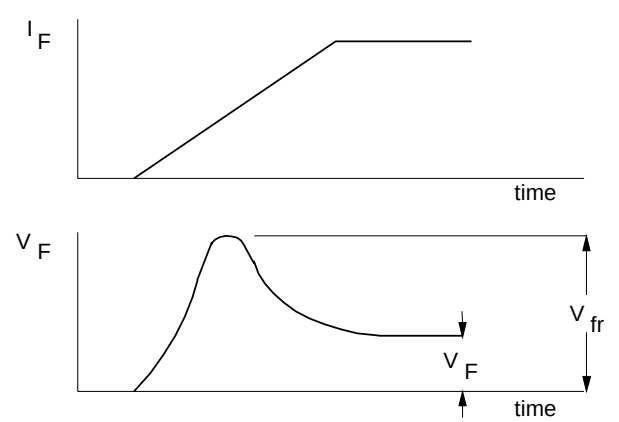


Fig.2. Definition of V_{fr}

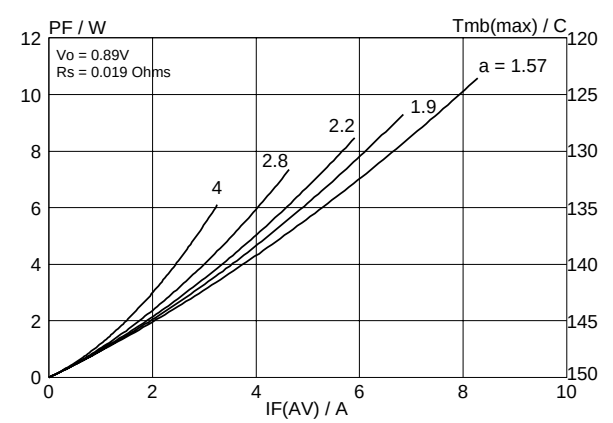


Fig.4. Maximum forward dissipation $P_F = f(I_{F(AV)})$; sinusoidal current waveform where a = form factor = $I_{F(RMS)} / I_{F(AV)}$.

APPENDIX D

MICROCHIP

PIC16F87X

28/40-Pin 8-Bit CMOS FLASH Microcontrollers

Devices Included in this Data Sheet:

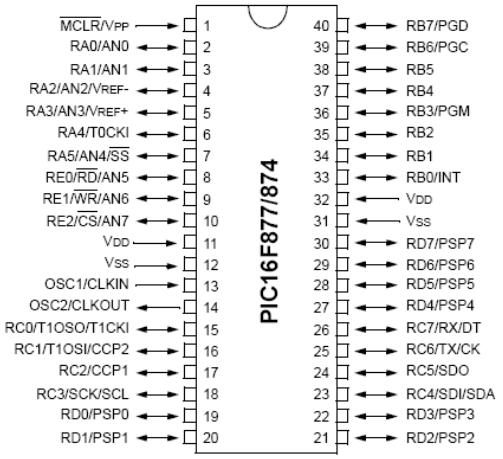
- PIC16F873
- PIC16F874
- PIC16F876
- PIC16F877

Microcontroller Core Features:

- High performance RISC CPU
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle
- Up to 8K x 14 words of FLASH Program Memory,
  Up to 368 x 8 bytes of Data Memory (RAM)
  Up to 256 x 8 bytes of EEPROM Data Memory
- Pinout compatible to the PIC16C73B/74B/76/77
- Interrupt capability (up to 14 sources)
- Eight level deep hardware stack
- Direct, indirect and relative addressing modes
- Power-on Reset (POR)
- Power-up Timer (PWRT) and
  Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- Low power, high speed CMOS FLASH/EEPROM technology
- Fully static design
- In-Circuit Serial Programming™ (ICSP) via two pins
- Single 5V In-Circuit Serial Programming capability
- In-Circuit Debugging via two pins
- Processor read/write access to program memory
- Wide operating voltage range: 2.0V to 5.5V
- High Sink/Source Current: 25 mA
- Commercial, Industrial and Extended temperature ranges
- Low-power consumption:
  - < 0.6 mA typical @ 3V, 4 MHz
  - 20 μA typical @ 3V, 32 kHz
  - < 1 μA typical standby current

Pin Diagram

PDIP

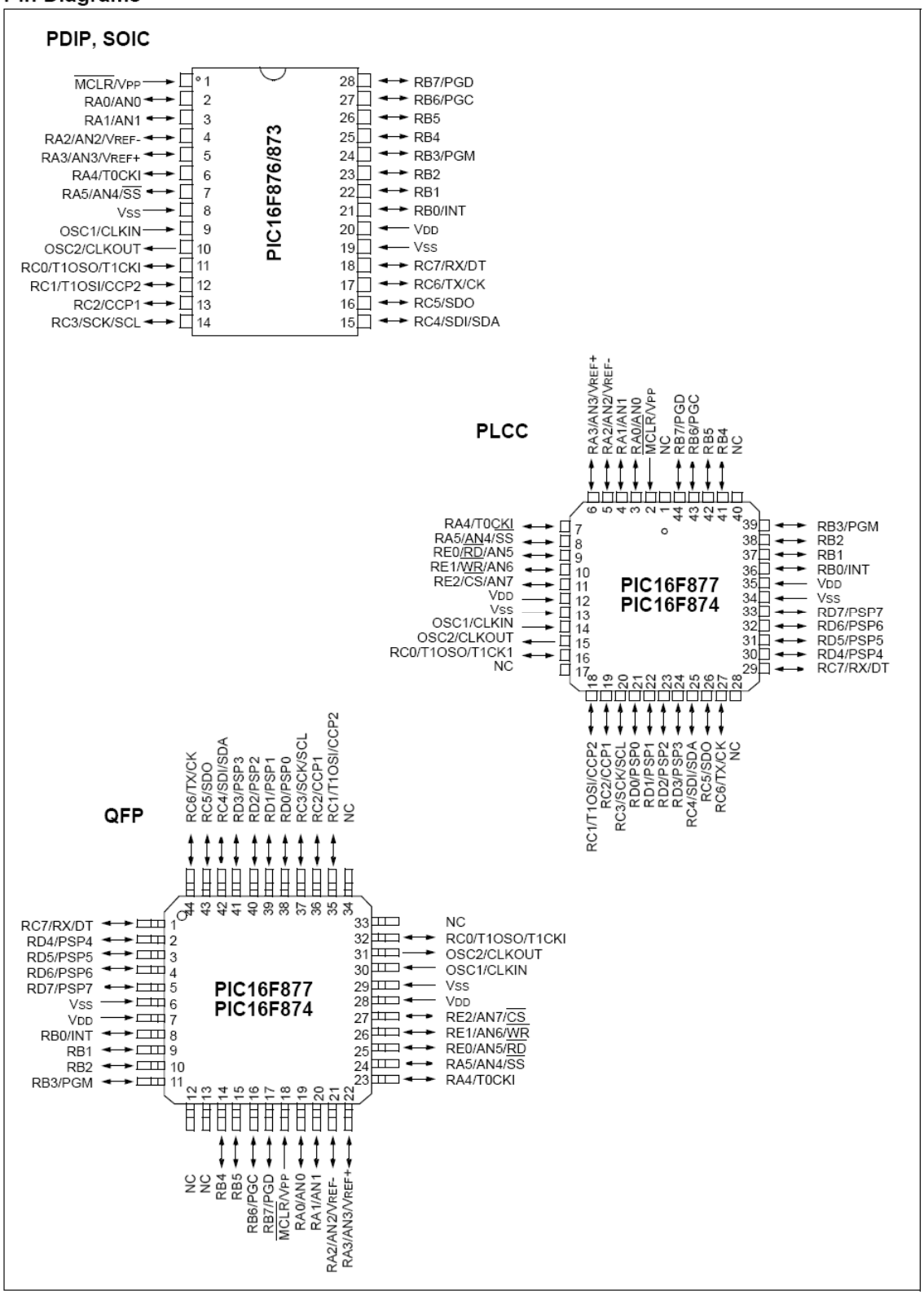


Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during SLEEP via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
  - Capture is 16-bit, max. resolution is 12.5 ns
  - Compare is 16-bit, max. resolution is 200 ns
  - PWM max. resolution is 10-bit
- 10-bit multi-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI™ (Master mode) and I²C™ (Master/Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection
- Parallel Slave Port (PSP) 8-bits wide, with external RD, WR and CS controls (40/44-pin only)
- Brown-out detection circuitry for Brown-out Reset (BOR)

PIC16F87X

Pin Diagrams



Key Features PICmicro™ Mid-Range Reference Manual (DS33023)	PIC16F873	PIC16F874	PIC16F876	PIC16F877
Operating Frequency	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz	DC - 20 MHz
RESETS (and Delays)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)	POR, BOR (PWRT, OST)
FLASH Program Memory (14-bit words)	4K	4K	8K	8K
Data Memory (bytes)	192	192	368	368
EEPROM Data Memory	128	128	256	256
Interrupts	13	14	13	14
I/O Ports	Ports A,B,C	Ports A,B,C,D,E	Ports A,B,C	Ports A,B,C,D,E
Timers	3	3	3	3
Capture/Compare/PWM Modules	2	2	2	2
Serial Communications	MSSP, USART	MSSP, USART	MSSP, USART	MSSP, USART
Parallel Communications	—	PSP	—	PSP
10-bit Analog-to-Digital Module	5 input channels	8 input channels	5 input channels	8 input channels
Instruction Set	35 instructions	35 instructions	35 instructions	35 instructions

TABLE 1-1: PIC16F873 AND PIC16F876 PINOUT DESCRIPTION

Pin Name	DIP Pin#	SOIC Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	9	9	I	ST/CMOS(3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	10	10	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	1	1	I/P	ST	Master Clear (Reset) input or programming voltage input. This pin is an active low RESET to the device.
					PORTA is a bi-directional I/O port.
RA0/AN0	2	2	I/O	TTL	RA0 can also be analog input0.
RA1/AN1	3	3	I/O	TTL	RA1 can also be analog input1.
RA2/AN2/VREF-	4	4	I/O	TTL	RA2 can also be analog input2 or negative analog reference voltage.
RA3/AN3/VREF+	5	5	I/O	TTL	RA3 can also be analog input3 or positive analog reference voltage.
RA4/T0CKI	6	6	I/O	ST	RA4 can also be the clock input to the Timer0 module. Output is open drain type.
RA5/$\overline{SS}$/AN4	7	7	I/O	TTL	RA5 can also be analog input4 or the slave select for the synchronous serial port.
					PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	21	21	I/O	TTL/ST(1)	RB0 can also be the external interrupt pin.
RB1	22	22	I/O	TTL	
RB2	23	23	I/O	TTL	
RB3/PGM	24	24	I/O	TTL	RB3 can also be the low voltage programming input.
RB4	25	25	I/O	TTL	Interrupt-on-change pin.
RB5	26	26	I/O	TTL	Interrupt-on-change pin.
RB6/PGC	27	27	I/O	TTL/ST(2)	Interrupt-on-change pin or In-Circuit Debugger pin. Serial programming clock.
RB7/PGD	28	28	I/O	TTL/ST(2)	Interrupt-on-change pin or In-Circuit Debugger pin. Serial programming data.
					PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	11	11	I/O	ST	RC0 can also be the Timer1 oscillator output or Timer1 clock input.
RC1/T1OSI/CCP2	12	12	I/O	ST	RC1 can also be the Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output.
RC2/CCP1	13	13	I/O	ST	RC2 can also be the Capture1 input/Compare1 output/ PWM1 output.
RC3/SCK/SCL	14	14	I/O	ST	RC3 can also be the synchronous serial clock input/output for both SPI and I^2C modes.
RC4/SDI/SDA	15	15	I/O	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	16	16	I/O	ST	RC5 can also be the SPI Data Out (SPI mode).
RC6/TX/CK	17	17	I/O	ST	RC6 can also be the USART Asynchronous Transmit or Synchronous Clock.
RC7/RX/DT	18	18	I/O	ST	RC7 can also be the USART Asynchronous Receive or Synchronous Data.
VSS	8, 19	8, 19	P	—	Ground reference for logic and I/O pins.
VDD	20	20	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

TABLE 1-2: PIC16F874 AND PIC16F877 PINOUT DESCRIPTION

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	13	14	30	I	ST/CMOS(4)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	14	15	31	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	1	2	18	I/P	ST	Master Clear (Reset) input or programming voltage input. This pin is an active low RESET to the device.
						PORTA is a bi-directional I/O port.
RA0/AN0	2	3	19	I/O	TTL	RA0 can also be analog input0.
RA1/AN1	3	4	20	I/O	TTL	RA1 can also be analog input1.
RA2/AN2/VREF-	4	5	21	I/O	TTL	RA2 can also be analog input2 or negative analog reference voltage.
RA3/AN3/VREF+	5	6	22	I/O	TTL	RA3 can also be analog input3 or positive analog reference voltage.
RA4/T0CKI	6	7	23	I/O	ST	RA4 can also be the clock input to the Timer0 timer/ counter. Output is open drain type.
RA5/$\overline{SS}$/AN4	7	8	24	I/O	TTL	RA5 can also be analog input4 or the slave select for the synchronous serial port.
						PORTB is a bi-directional I/O port. PORTB can be soft-ware programmed for internal weak pull-up on all inputs.
RB0/INT	33	36	8	I/O	TTL/ST(1)	RB0 can also be the external interrupt pin.
RB1	34	37	9	I/O	TTL	
RB2	35	38	10	I/O	TTL	
RB3/PGM	36	39	11	I/O	TTL	RB3 can also be the low voltage programming input.
RB4	37	41	14	I/O	TTL	Interrupt-on-change pin.
RB5	38	42	15	I/O	TTL	Interrupt-on-change pin.
RB6/PGC	39	43	16	I/O	TTL/ST(2)	Interrupt-on-change pin or In-Circuit Debugger pin. Serial programming clock.
RB7/PGD	40	44	17	I/O	TTL/ST(2)	Interrupt-on-change pin or In-Circuit Debugger pin. Serial programming data.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).
4: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

TABLE 1-2: PIC16F874 AND PIC16F877 PINOUT DESCRIPTION (CONTINUED)

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
						PORTC is a bi-directional I/O port.
RC0/T1OSO/T1CKI	15	16	32	I/O	ST	RC0 can also be the Timer1 oscillator output or a Timer1 clock input.
RC1/T1OSI/CCP2	16	18	35	I/O	ST	RC1 can also be the Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output.
RC2/CCP1	17	19	36	I/O	ST	RC2 can also be the Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	18	20	37	I/O	ST	RC3 can also be the synchronous serial clock input/ output for both SPI and I^2C modes.
RC4/SDI/SDA	23	25	42	I/O	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	24	26	43	I/O	ST	RC5 can also be the SPI Data Out (SPI mode).
RC6/TX/CK	25	27	44	I/O	ST	RC6 can also be the USART Asynchronous Transmit or Synchronous Clock.
RC7/RX/DT	26	29	1	I/O	ST	RC7 can also be the USART Asynchronous Receive or Synchronous Data.
						PORTD is a bi-directional I/O port or parallel slave port when interfacing to a microprocessor bus.
RD0/PSP0	19	21	38	I/O	ST/TTL(3)	
RD1/PSP1	20	22	39	I/O	ST/TTL(3)	
RD2/PSP2	21	23	40	I/O	ST/TTL(3)	
RD3/PSP3	22	24	41	I/O	ST/TTL(3)	
RD4/PSP4	27	30	2	I/O	ST/TTL(3)	
RD5/PSP5	28	31	3	I/O	ST/TTL(3)	
RD6/PSP6	29	32	4	I/O	ST/TTL(3)	
RD7/PSP7	30	33	5	I/O	ST/TTL(3)	
						PORTE is a bi-directional I/O port.
RE0/$\overline{RD}$/AN5	8	9	25	I/O	ST/TTL(3)	RE0 can also be read control for the parallel slave port, or analog input5.
RE1/$\overline{WR}$/AN6	9	10	26	I/O	ST/TTL(3)	RE1 can also be write control for the parallel slave port, or analog input6.
RE2/$\overline{CS}$/AN7	10	11	27	I/O	ST/TTL(3)	RE2 can also be select control for the parallel slave port, or analog input7.
VSS	12,31	13,34	6,29	P	—	Ground reference for logic and I/O pins.
VDD	11,32	12,35	7,28	P	—	Positive supply for logic and I/O pins.
NC	—	1,17,28, 40	12,13, 33,34		—	These pins are not internally connected. These pins should be left unconnected.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).
4: This buffer is a Schmitt Trigger input when configured in RC oscillator mode and a CMOS input otherwise.

8.0 CAPTURE/COMPARE/PWM MODULES

Each Capture/Compare/PWM (CCP) module contains a 16-bit register which can operate as a:

- 16-bit Capture register
- 16-bit Compare register
- PWM Master/Slave Duty Cycle register

Both the CCP1 and CCP2 modules are identical in operation, with the exception being the operation of the special event trigger. Table 8-1 and Table 8-2 show the resources and interactions of the CCP module(s). In the following sections, the operation of a CCP module is described with respect to CCP1. CCP2 operates the same as CCP1, except where noted.

CCP1 Module:

Capture/Compare/PWM Register1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. The special event trigger is generated by a compare match and will reset Timer1.

CCP2 Module:

Capture/Compare/PWM Register2 (CCPR2) is comprised of two 8-bit registers: CCPR2L (low byte) and CCPR2H (high byte). The CCP2CON register controls the operation of CCP2. The special event trigger is generated by a compare match and will reset Timer1 and start an A/D conversion (if the A/D module is enabled).

Additional information on CCP modules is available in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023) and in application note AN594, "Using the CCP Modules" (DS00594).

TABLE 8-1: CCP MODE - TIMER RESOURCES REQUIRED

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

TABLE 8-2: INTERACTION OF TWO CCP MODULES

CCPx Mode	CCPy Mode	Interaction
Capture	Capture	Same TMR1 time-base
Capture	Compare	The compare should be configured for the special event trigger, which clears TMR1
Compare	Compare	The compare(s) should be configured for the special event trigger, which clears TMR1
PWM	PWM	The PWMs will have the same frequency and update rate (TMR2 interrupt)
PWM	Capture	None
PWM	Compare	None

8.1 Capture Mode

In Capture mode, CCPR1H:CCPR1L captures the 16-bit value of the TMR1 register when an event occurs on pin RC2/CCP1. An event is defined as one of the following:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

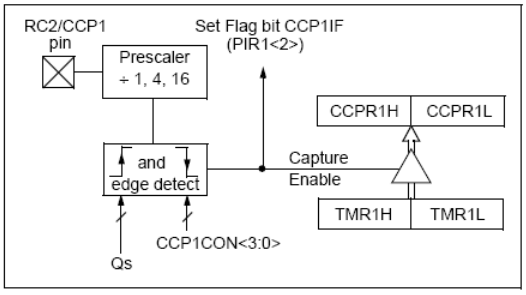
The type of event is configured by control bits CCP1M3:CCP1M0 (CCPxCON<3:0>). When a capture is made, the interrupt request flag bit CCP1IF (PIR1<2>) is set. The interrupt flag must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value is overwritten by the new value.

8.1.1 CCP PIN CONFIGURATION

In Capture mode, the RC2/CCP1 pin should be configured as an input by setting the TRISC<2> bit.

Note:	If the RC2/CCP1 pin is configured as an output, a write to the port can cause a capture condition.

FIGURE 8-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



8.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode, or Synchronized Counter mode, for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

8.1.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep bit CCP1IE (PIE1<2>) clear to avoid false interrupts and should clear the flag bit CCP1IF, following any such change in operating mode.

8.1.4 CCP PRESCALER

There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. Any RESET will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore, the first capture may be from a non-zero prescaler. Example 8-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

EXAMPLE 8-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
CLRF    CCP1CON      ; Turn CCP module off
MOVLW   NEW_CAPT_PS  ; Load the W reg with
                     ; the new prescaler
                     ; move value and CCP ON
MOVWF   CCP1CON      ; Load CCP1CON with this
                     ; value
```

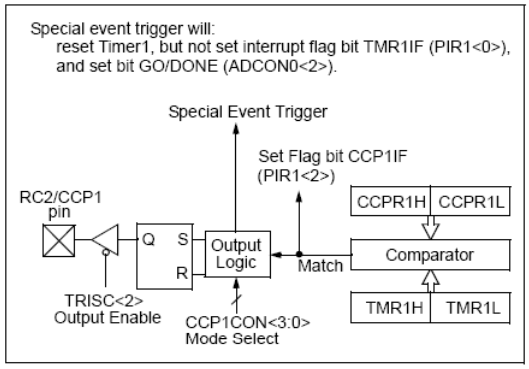
8.2 Compare Mode

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the RC2/CCP1 pin is:

- Driven high
- Driven low
- Remains unchanged

The action on the pin is based on the value of control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). At the same time, interrupt flag bit CCP1IF is set.

FIGURE 8-2: COMPARE MODE OPERATION BLOCK DIAGRAM



8.2.1 CCP PIN CONFIGURATION

The user must configure the RC2/CCP1 pin as an output by clearing the TRISC<2> bit.

Note:	Clearing the CCP1CON register will force the RC2/CCP1 compare output latch to the default low level. This is not the PORTC I/O data latch.

8.2.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode, or Synchronized Counter mode, if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

8.2.3 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt mode is chosen, the CCP1 pin is not affected. The CCPIF bit is set, causing a CCP interrupt (if enabled).

8.2.4 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated, which may be used to initiate an action.

The special event trigger output of CCP1 resets the TMR1 register pair. This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

The special event trigger output of CCP2 resets the TMR1 register pair and starts an A/D conversion (if the A/D module is enabled).

Note:	The special event trigger from the CCP1and CCP2 modules will not set interrupt flag bit TMR1IF (PIR1<0>).

8.3 PWM Mode (PWM)

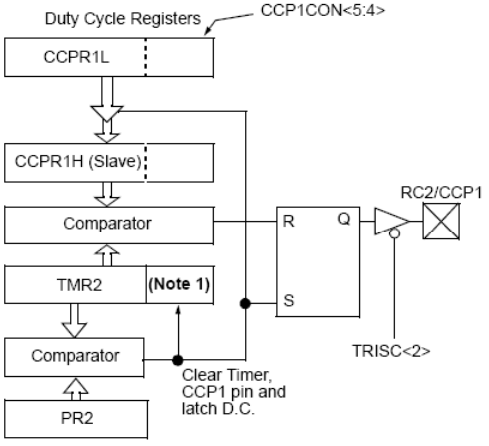
In Pulse Width Modulation mode, the CCPx pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

Note:	Clearing the CCP1CON register will force the CCP1 PWM output latch to the default low level. This is not the PORTC I/O data latch.

Figure 8-3 shows a simplified block diagram of the CCP module in PWM mode.

For a step-by-step procedure on how to set up the CCP module for PWM operation, see Section 8.3.3.

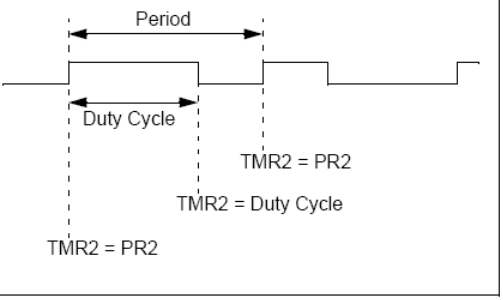
FIGURE 8-3: SIMPLIFIED PWM BLOCK DIAGRAM



Note 1: The 8-bit timer is concatenated with 2-bit internal Q clock, or 2 bits of the prescaler, to create 10-bit time-base.

A PWM output (Figure 8-4) has a time-base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 8-4: PWM OUTPUT



8.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

$$\text{PWM period} = [(PR2) + 1] \cdot 4 \cdot T_{OSC} \cdot (\text{TMR2 prescale value})$$

PWM frequency is defined as 1 / [PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note:	The Timer2 postscaler (see Section 7.1) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

8.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

$$\text{PWM duty cycle} = (CCPR1L{:}CCP1CON\langle 5{:}4\rangle) \cdot T_{OSC} \cdot (\text{TMR2 prescale value})$$

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitch-free PWM operation.

When the CCPR1H and 2-bit latch match TMR2, concatenated with an internal 2-bit Q clock, or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

The maximum PWM resolution (bits) for a given PWM frequency is given by the formula:

$$\text{Resolution} = \frac{\log\left(\frac{F_{OSC}}{F_{PWM}}\right)}{\log(2)} \text{ bits}$$

Note:	If the PWM duty cycle value is longer than the PWM period, the CCP1 pin will not be cleared.

8.3.3 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
3. Make the CCP1 pin an output by clearing the TRISC<2> bit.
4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP1 module for PWM operation.

TABLE 8-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12kHz	156.3 kHz	208.3 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFFh	0xFFh	0xFFh	0x3Fh	0x1Fh	0x17h
Maximum Resolution (bits)	10	10	10	8	7	5.5

TABLE 8-4: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, AND TIMER1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh,8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
0Dh	PIR2	—	—	—	—	—	—	—	CCP2IF	---- ---0	---- ---0
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
8Dh	PIE2	—	—	—	—	—	—	—	CCP2IE	---- ---0	---- ---0
87h	TRISC	PORTC Data Direction Register								1111 1111	1111 1111
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	--00 0000	--uu uuuu
15h	CCPR1L	Capture/Compare/PWM Register1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM Register1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000
1Bh	CCPR2L	Capture/Compare/PWM Register2 (LSB)								xxxx xxxx	uuuu uuuu
1Ch	CCPR2H	Capture/Compare/PWM Register2 (MSB)								xxxx xxxx	uuuu uuuu
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by Capture and Timer1.
Note 1: The PSP is not implemented on the PIC16F873/876; always maintain these bits clear.

APPENDIX E

```
;*****************************************************************
        TITLE "PWM based sine wave generator"
         LIST P=16C620, R=DEC

        INCLUDE         <P16C620.INC>
        __CONFIG        _BODEN_OFF&_CP_OFF&_PWRTE_ON&_WDT_OFF&_XT_OSC
;
;*****************************************************************
;       File:           SINE.ASM
;       Author:         Rob Stein
;        Date:          12/20/95
;       Assembler:      MPASM V01.40
;        Xtal:          20 Mhz
;        Inst Clk:      5 Mhz (200nSec)
;*****************************************************************
;    Description:
;       Outputs a 60 Hz synthizied sine wave (32 step) via a general
;       purpose I/O pin (RB1) into a low pass filter. A software PWM
;       routine is used to create 32 seperate sinewave steps.    This
;       software was prototyped with the PICDEM1 board.
;
;       ROM Usage: 98 words
;
;       RAM Usage: 6 bytes
;
;************************ Constant Definition   **********************

FXTAL           EQU   .20000000       ; Crystal Frequency
FINST           EQU   FXTAL/4         ; Instruction Cycle Frequency
FSINE           EQU   .60             ; Sine function frequency
STEP#           EQU    .32            ; Number of steps
FSTEP           EQU   FSINE * STEP#   ; Step frequency

;************************  Register Definition  **********************

TEMPW           EQU    0x20           ; Temporary interupt storage for W
DELAYCNT1       EQU    0x21           ; Delay routine counter low
DELAYCNT2       EQU   0x22            ; Delay routine counter high
STEPCOUNT       EQU    0x23           ; Sine step counter
OUTLOW                 EQU   0x24             ; PWM low cycle load for TMR0
OUTHIGH                EQU    0x25            ; PWM high cycle load for TMR0

;************************    Bit Definition    **********************

PWM   EQU    0x01                     ; RB1 used for PWM output

;*****************************************************************
;                               Reset Vector
```

```
;*****************************************************************

     org    0x000
     goto   Start          ; Begining of Program

;*****************************************************************
;          Interupt Vector and Service Routine
;         This interupt routine is entered via an overflow of TMR0 from
;         0xFF to 0x00.  A test of RB1 determines if the next time state
;         is a high or low cycle.  The next interupt will occure based the
;         TMR0 reload value (OUTLOW or OUTHIGH).
;
;         The interupt routine was designed to use a minimial number of
;         instruction cycles.  This was done to maximize the PWM duty cycle
;         range (ie. a 5 % to 95 % range is achievable with this ISR).  Note
;         that 'swapf' instructions are used to perform register moves without
;         effecting the STATUS flags (this saves instruction cycles by
;         eliminating the need to temporarily save the STATUS register).
;
;*****************************************************************

         org    0x004              ; Interupt vector location
IntVector
         movwf  TEMPW              ; Temporarily save W
         btfsc  PORTB,PWM          ; Was this a Low cycle ?
         goto   PWMLow             ; No ...
PWMHigh
         swapf  OUTHIGH,W          ; Yes... Load high time without affecting STATUS flags
         bsf    PORTB,PWM
         nop                       ; Delay to equalize high/low TMR0 load cycles
         movwf  TMR0               ; Load next edge interupt time
         bcf    INTCON,T0IF        ; Clear TMR0 overflow flag
         swapf  TEMPW,F            ; Swap saved W
         swapf  TEMPW,W            ; Restore W
IntEndHi
     retfie              ; Return from Interupt
PWMLow
         bcf    PORTB,PWM
         swapf  OUTLOW,W           ; Load low time
         movwf  TMR0               ; Load next edge interupt time
         bcf    INTCON,T0IF        ; Clear TMR0 overflow flag
         swapf  TEMPW,F            ; Swap saved W
         swapf  TEMPW,W            ; Restore W
IntEndLo
     retfie                         ; Return from Interupt

;*****************************************************************
;                  Main Routine
```

```
;*****************************************************************
Start
     clrf   STATUS                ; Intitialize STATUS & select bank 0
     bsf    STATUS,RP0             ; Select register bank 1
          movlw  0x88
          movwf  OPTION_REG    ; 1:1 TMR0 prescaler, PORTB pull-ups disabled
     movlw  0xFF
     movwf  TRISA         ; Set Port_A as inputs
     clrf   TRISB         ; Set Port_B as outputs
     bcf    STATUS,RP0     ; Select register bank 0
          movwf  PORTB              ; PORT_B pins high
          clrf   TMR0               ; Initialize TMR0
          movlw  0xA0
          movwf  INTCON             ; Enable TMRO and global interupt
ResetStep
     movlw  STEP#
     movwf  STEPCOUNT          ; Load counter for 32 steps
StepLoop
     call   Delay            ; Software delay
     movf   STEPCOUNT,W        ; Pass table offset via W
     call   SineTable       ; Get table value
          call   SetPWM                  ; Set-up low & high PWM values
     decfsz STEPCOUNT,F         ; Next step
     goto   StepLoop
     goto   ResetStep

;*****************************************************************
;                    Set PWM Subroutine
;          The following calculates the next low and high PWM time values.
;          The two time values, OUTLOW and OUTHIGH, will be passed to the
;          interupt service routine.
;*****************************************************************
SetPWM
          bcf    INTCON,GIE      ; Disable interupts to protect ISR from...
                                 ; corrupting OUTLOW & OUTHIGH values
          movwf  OUTLOW                  ; Set PWM Duty Cycle
          comf   OUTLOW,W

          addlw  IntEndHi-IntVector ; Adjust for Int Service time
          movwf  OUTHIGH
          movf   OUTLOW,W
          addlw  IntEndHi-IntVector ; Adjust for Int Service time
          movwf  OUTLOW

          swapf  OUTLOW,F       ; Swap nibbles so that interupt service...
          swapf  OUTHIGH,F      ; will not corrupt STATUS
          bsf    INTCON,GIE      ; Re-enable interupts
          return
```

```
;*****************************************************************
;                       Look-up Table for Sine Wave
;       This 32 entry table was generated to produce a 0.1*Vdd to
;       0.9*Vdd (typicaly 0.5 to 4.5 volt) sine function.
;*****************************************************************
SineTable
        addwf   PCL,F           ; Increment into table
    retlw   .0          ; Dummy table value
    retlw   .128        ; 0 degree, 2.5 volt
    retlw   .148
    retlw   .167
    retlw   .185
    retlw   .200
    retlw   .213
    retlw   .222
    retlw   .228
    retlw   .230        ; 90 degree, 4.5 volt
    retlw   .228
    retlw   .222
    retlw   .213
    retlw   .200
    retlw   .185
    retlw   .167
    retlw   .148
    retlw   .128        ; 180 degree, 2.5 volt
    retlw   .108
    retlw   .89
    retlw   .71
    retlw   .56
    retlw   .43
    retlw   .34
    retlw   .28
    retlw   .26         ; 270 degree, 0.5 volt
    retlw   .28
    retlw   .34
    retlw   .43
    retlw   .56
    retlw   .71
    retlw   .89
    retlw   .108

;*****************************************************************
;               Time Delay Sub-routine
;       The time delay is used to create the precision 32 steps.  The
;       32 step times totaled together add up to a 60 Hz rate. Note that
;       constants DELAYCNT# are used so that other frequencies can easily
;       generated (example: FSINE equ .50 for a 50 Hz sinewave).
```

```
;*****************************************************************
TDELAY          EQU     FINST/FSTEP     ; # of delay count cycles
ADJTDELAY       EQU     TDELAY/3 - 55   ; Adjust for main routine cycles
TDELAYHI        EQU     high ADJTDELAY          ; Most Significant Byte of TDELAY
TDELAYLO        EQU     low ADJTDELAY ; Least Sig. Byte of TDELAY

Delay
        movlw  TDELAYHI
        movwf  DELAYCNT2      ; Load high byte delay counter
        clrf       DELAYCNT1
LoopD1
    decfsz  DELAYCNT1,F         ; Finished with 256 loops ?
    goto    LoopD1              ; No ... keep going
        decfsz   DELAYCNT2,F    ; Yes... Done with TDELAYHI loops ?
        goto     LoopD1         ; No ...

        movlw  TDELAYLO         ; Yes... Load low byte with adjust for...
    movwf   DELAYCNT1           ; main routine cycles.
LoopD2
    decfsz  DELAYCNT1,F         ; Finished with TDELAYLO loops ?
    goto    LoopD2              ; No ... keep going
    return                      ; Yes... Finished

    END                         ; That's all Folks !
```